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ELECTRIC PROTOTYPE POWER PROCESSOR
FOR A
30CM ION THRUSTER

FINAL REPORT

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16. Abstract An electrical prototype power processor unit was designed, fabricated and tested with a 30cm mercury ion engine for primary space propulsion. The power processor unit used the Thyristor Series Resonant Inverter as the basic power stage for the high power beam and discharge supplies. A transistorized Series Resonant Inverter processed the remaining power for the low power outputs. The power processor included a digital interface unit to process all input commands and internal telemetry signals so that electric propulsion systems could be operated with a central computer system. The electrical prototype unit included design improvement in the power components such as thyristors, transistors, filters and resonant capacitors and power transformers and inductors in order to reduce component weight, to minimize losses and to control the component temperature rise. A design analysis for the electrical prototype is also presented on the component weight, losses, part count and reliability estimate. The electrical prototype was tested in a thermal vacuum environment. Integration tests were performed with a 30cm ion engine and demonstrated operational compatibility. Electromagnetic interference data was also recorded on the design to provide information for spacecraft integration.					
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FORWARD

This work is a continuation of the development effort on the 30cm Ion Thruster Power Processor reported in NASA CR-134785, "Power Processor for a 30cm Ion Thruster."

The development of the 50kHz transistor series resonant inverter for the low voltage ion engine outputs was supported by Dr. F.C. Schwarz of Power Electronics Associates.

Mr. Dave Kellerman of Components Research Corp. supplied the specialized power capacitors used in the high power input/output filters and in the series resonant inverter circuit.

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TABLE OF CONTENTS

	<u>Page No.</u>
1.0 SUMMARY	1-1
2.0 INTRODUCTION	2-1
3.0 ELECTRICAL PROTOTYPE POWER PROCESSOR DESIGN	3-1
3.1 Power Processor System Block Diagram	3-2
3.2 Electrical Design	3-7
3.3 Electrical Component Development	3-26
3.4 Mechanical Design	3-29
3.5 Thermal Control	3-33
3.6 Design Analysis	3-36
4.0 ELECTRICAL PROTOTYPE POWER PROCESSOR TEST RESULTS	4-1
4.1 Load Bank Test	4-2
4.2 Ion Engine Integration Tests	4-17
4.3 Thermal Vacuum Test	4-31
4.4 Electromagnetic Interference Tests	4-41
5.0 CONCLUSIONS	5-1
6.0 APPENDICES, TABLE OF CONTENTS	6-1
7.0 DISTRIBUTION LIST	7-1

1.0 SUMMARY

An Electrical Prototype Power Processor Unit was designed, fabricated and tested for use with the 30cm Mercury Ion Thruster. The ion engine was operated with the power processor for over 77 hours at TRW under all operating conditions - startup, shutdown, arcing and recovery, steady-state operation at fixed (1100V) and variable (1100V-600V) beam voltage and over the 0.5A to 2.0A beam current extremes. Continued Ion Engine Power Processor testing is in progress at NASA/Lewis Research Center.

The power processor includes three series resonant inverter power stages to process the 200 to 400Vdc input to meet the output requirements for (12) separate ion engine functions. The beam inverter supplies 2.4kW to the screen/accelerator electrodes. The discharge inverter supplies a maximum 700W to the ion engine for the generation of the mercury ions. The multiple output inverter supplies a maximum of 389W for the remaining (9) ion engine heater, vaporizer, keeper, and magnetic baffle supplies.

Extensive component improvement work was performed on the thyristor, transistor, filter capacitors, series resonant capacitors, series resonant inductor and high voltage high power transformers. As a result of this component work, the component weight was reduced about 30% from previous power processor designs, while at the same time, controlling the maximum component operating temperatures.

The power processor was configured into seven separate modules that would allow subassembly testing and then integration into a complete power processor unit assembly. The conceptual packaging of the electrical prototype power processor unit demonstrated the relative location of power, high voltage and control electronic components to minimize electrical interaction and to provide adequate thermal vacuum cooling in conjunction with a heat pipe simulator attached to the base of the module.

Based on the results of this packaging effort, NASA Lewis Research Center is designing and fabricating a Functional Model Unit that would further improve the packaging concept to reduce weight and improve component thermal control.

Special test equipment was designed and fabricated in support of the electrical prototype power processor test program. The test program at TRW included:

- Module test (seven types)
- Unit load bank test
- Thermal vacuum test
- Ion engine integration test
- Electromagnetic interference test

It was most rewarding that during this entire development program, which included numerous repeated short circuit and arc over testing not a single power semiconductor has failed.

2.0 INTRODUCTION

Solar Electric Propulsion (SEP) using mercury bombardment ion thrusters has been in a research and development stage for well over a decade. Two experimental flights, SERT I in 1964 and SERT II in 1970, have demonstrated the feasibility of this type of propulsion for long-term space flights.

Recent achievements in standardization, reliability and performance of the 30cm ion thruster have brought operational SEP missions nearer to reality. The proposed missions cover a wide range of environmental conditions from near Sun to deep space planetary probes. The electric thrust subsystem for the SEP missions under consideration would consist of a cluster of from two to ten 30cm ion thrusters each with its associated power processor unit (PPU). The power processor unit provides the interface function between the thruster and various spacecraft subsystems such as the central computer, command/telemetry units, and the solar array power bus. Additionally, the power processor unit contains internal logic which provides rapid corrective control action during periods of abnormal thruster operation.

The basic characteristics of an ion thruster, namely the generation acceleration, discharge, and neutralization of an ionized gas plasma require rather unique electrical power supplies. In all, twelve separate power supplies with widely varying requirements of power, voltage and regulation are needed to operate a thruster. A characteristically severe requirement is placed upon the power processor unit due to the natural tendency of ion thrusters to arc. Consequently, all power supplies have to be able to sustain direct shorts between their output terminals, while selected outputs have to be able to sustain shorts between one another and some outputs have to be able to sustain direct shorts to ground.

TRW Systems has developed 30cm Ion Thruster Power Processors under Contracts NAS3-14383, "Development and Improvement of Ion Engine Power Processor," and NAS3-18924, "Breadboard Power Supply," for NASA Lewis Research Center.

In the process of performing these programs, new power processing technology has been developed that ensures superior performance and protection characteristics of the power processor and the electric propulsion subsystem. These features include:

- Series LC Resonant Inverter power stage which acts as a current source and protects the ion engine, power source and power switching semiconductors from any over-stress condition during startup, steady-state or arc-over conditions.
- High frequency series resonant circuit operation of thyristors and transistors thereby assuring a low weight power processor.
- A low part count design, since high power thyristors can readily handle the peak power requirement of the 30cm ion thruster.
- A simplified recycle system due to the current source power stage that allows the clearing of ion engine faults without an elaborate turn-off and sequencing of output power supplies.
- Output fault protection circuitry that allows a short circuit across any output or between high and low voltage outputs without any damage or overstress of components.
- Demonstrated high operating efficiency over the 1/4 to full power throttling range due to power processor system mechanization.
- Extensive use of the multiple feedback loop control system to provide the required regulation, the no load to full load transient response and the low impedance output that eliminates any oscillation with the negative impedance of ion engine plasma discharge.

The two breadboards delivered on the previous contracts have demonstrated reliable circuit operation for a combined total of over 18,000 hours with no power switching semiconductor failures during all the different test phases including extensive operation with the various 30cm ion thrusters.

The Electrical Prototype/Power Processor Unit (EP/PPU) Program is seen as a logical step in producing the flight type power processing equipment necessary for Solar Electric Propulsion mission planned for the future.

The EP/PPU is a fully functional electronic package which meets the requirements of the 30cm ion engine. The design philosophy is such that the electrical design is of flight-type quality, and it is thermally and structurally packaged in a form similar to the Lewis Research Center's projection of the Functional Model (FM) mechanical configuration, yet providing maximum electrical circuit accessibility, (refer to NASA TM X-71683, "A Thruster Subsystem Module for Solar Electric Propulsion," and NASA TM X-71686, "A Structural and Thermal Packaging Approach for Power Processing Units for 30cm Ion Thrusters"). The electrical design utilizes commercial equivalents of Hi Rel parts in all cases except for special contractor fabricated magnetic devices which were of flight configuration with screening of high voltage magnetics. Selection and/or design of electrical components was such as to minimize weight and assure their direct utilization in the Lewis Research Center FM/PPU.

All high voltage isolation was accomplished within the EP/PPU. The serial digital-to-parallel digital command and control interface unit (IU) is considered part of the EP/PPU.

The program was divided into eight basic tasks:

TASK I	EP/PPU Design and Analysis
TASK II	EP/PPU Fabrication
TASK III	Test Support Equipment
TASK IV	EP/PPU Testing
TASK V	Reliability
TASK VI	Reports of Work
TASK VII	Project Management
TASK VIII	Electrical Components for the NASA FM/PPU's

The contracted effort involved the design, fabrication and testing of an Electrical Prototype Power Processor Unit (EP/PPU) which meets the requirements of potential future solar electric propulsion missions. The direct utilization of applicable technology from past and present related activities was maximized to the extent practicable. This approach provided the most useful and cost effective EP/PPU.

Specifically, the technology produced under three contracts, NAS12-2183 (Development of a Multikilowatt Ion Thruster Power Processor), NAS3-14383 (Improvement of Ion Engine Power Processor) and NAS3-18924 (Breadboard Power Supply) provided the baseline for the EP/PPU program. These three previous contracts dealt solely with developing the Series Resonant Inverter circuit technology using silicon controlled rectifiers and with demonstrating the ability to suitably power and control ion thrusters using this technology. The new contracted effort used the successful results of the previous efforts and took the next logical steps, i.e., updating the existing technology to meet the requirements of the current generation of ion thrusters and the proposed missions, and secondly, to take the initial steps toward packaging the circuitry into a flight configuration.

As part of the technology updating, the series resonant inverter technology was extended to the use of transistors in addition to thyristors. The lowest power rated inverter, namely the 389W multiple output inverter was implemented as a series resonant inverter with transistor power switches at a 50kHz operating frequency. The higher operating frequency of the transistorized series resonant inverter not only resulted in lower weight of the EP/PPU but it also paved the way to further weight reduction by pointing to the use of a transistorized series inverter for the 700W discharge supply as well.

3.0 ELECTRICAL PROTOTYPE POWER PROCESSOR DESIGN

A detail block diagram was generated for the power processor to identify both the input/output power and control interface. Special attention was placed on the grounding/isolation system to improve the noise susceptibility of the low level electronics and input power lines to output power transients.

Detail electrical designs were performed for each function which includes schematic diagrams, part list, magnetic design and component electrical stress analysis to ensure adequate component derating.

In order to minimize component weight and to control component maximum hot spot temperature for high reliability, component development were performed on the following type of components:

- Semiconductors
- Capacitors
- Magnetics

As a result of the power circuits and components design optimization, a savings in component weight of 6.25 lbs was obtained over the thermal vacuum breadboard developed under contract NAS3-14383 and reported in NASA CR-134785, "Power Processor for a 30cm Ion Thruster." This weight improvement was achieved in addition to having realized a 3% higher EP/PPU efficiency compared to the efficiency of the thermal vacuum breadboard.

The electrical design was subdivided into seven separable mechanical module assemblies to develop a mechanical spacecraft structure. The modularization of the EP/PPU was implemented so as to minimize the interwiring and electrical interference between modules, to isolate the high voltage supplies from the low voltage supplies and to form independently testable subassemblies for ease of integration and maintenance of the power processor unit.

All heat generated in the modules were removed by means of a heat pipe simulator attached to the base flanges of each of the modules.

The electrical prototype design was analyzed to determine the component weight, losses and efficiency, part count and finally the reliability projection for the design. Additional areas of improvement have been identified for the final power processor configuration.

3.1 POWER PROCESSOR SYSTEM BLOCK DIAGRAM

Figure 3-1 presents the power processor block diagram. Each function is identified with its respective mechanical module sub-assembly to illustrate where the particular function is located in the power processor mechanical package.

The 200 to 400Vdc power bus goes into a common input line filter which attenuates the high frequency switching currents being generated by three separate dc to ac series resonant inverters. The series resonant inverters include the following:

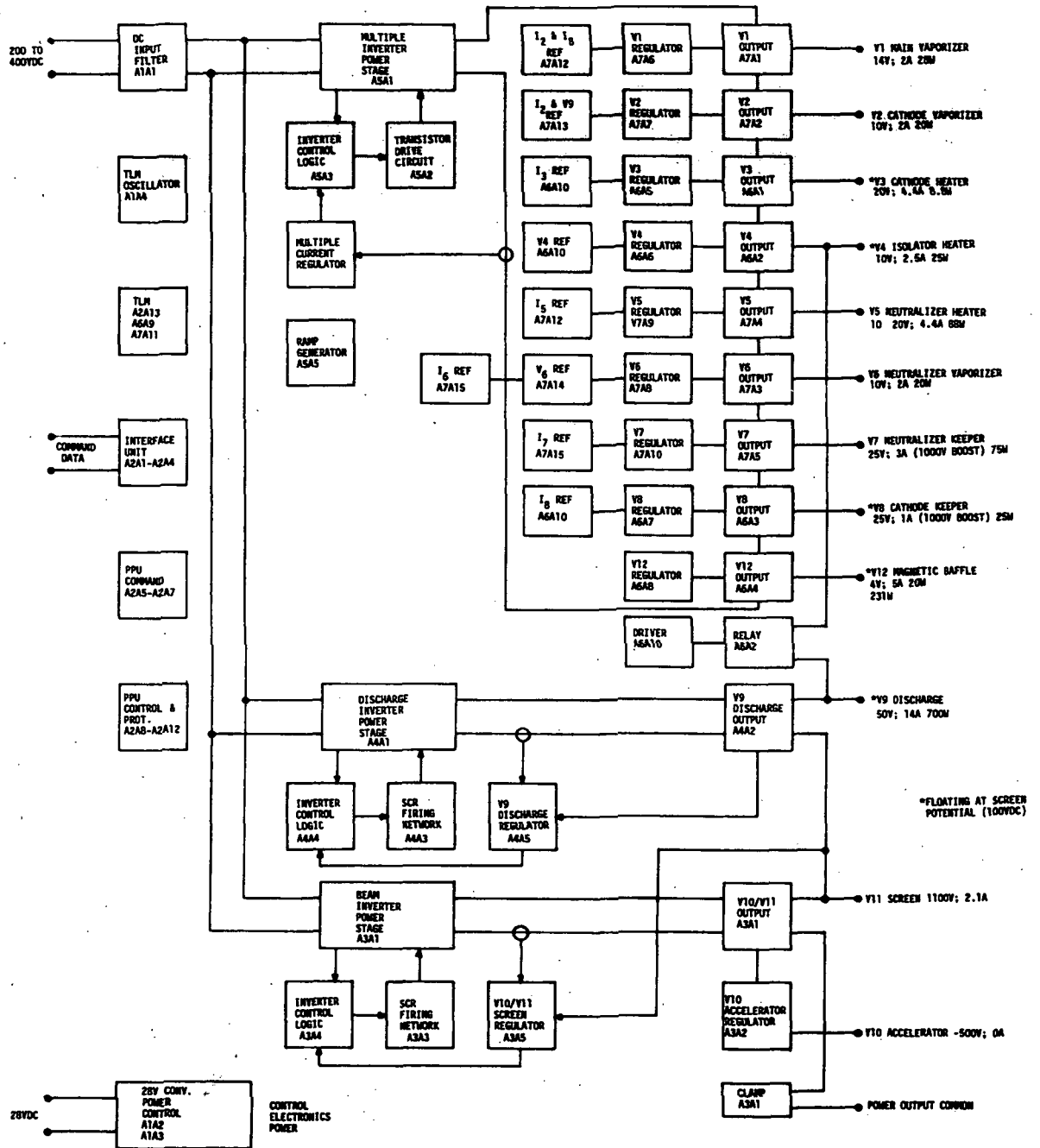
- 50kHz transistor multiple series resonant inverter power stage (A5A1).
- 20kHz thyristor discharge series resonant inverter power stage (A4A1).
- 20kHz thyristor beam series resonant inverter power stage (A3A1).

Each inverter includes its respective transistor drive circuit or SCR firing network for the turn-on of power semiconductors, inverter control logic which senses the power stage current and voltage levels to ensure correct sequencing of the turn-on and off of the power semiconductors and output regulator control electronics that establishes the turn-on frequency or duty cycle of the power semiconductors as a function of the output voltage or current requirement.

The 50kHz ac current source from the multiple inverter is fed to the respective low voltage output stages of supplies V1, V2, V3, V4, V5, V6, V7, V8 and V12. Each of the respective output stages has its own output isolation transformer and output rectifier filter network.

The output regulator electronics and reference electronics sub-assemblies that control the respective outputs are also noted in the block diagram.

The ramp generator A5A5 is used in conjunction with the different output regulators of the multiple inverter, and is synchronized with the multiple inverter operation.



LEGEND: AXAY

X = module no. (1 through 7), Y = subassembly no. (1, 2---n)

FIGURE 3-1 POWER PROCESSOR BLOCK DIAGRAM

The discharge inverter power stage supplies the output power to the discharge output transformer and its output rectifier-filter network.

The beam inverter power stage supplies output power to the main high voltage transformer for the screen electrodes. A separate voltage is generated for the accelerator regulator and supplies power to the accelerator electrodes. The negative line of the screen supply output goes to a power zener diode clamp to limit the maximum voltage that the ion engine ground can separate from spacecraft structure or neutralizer ground return.

An internal 28Vdc/dc converter processes the unregulated dc input power and establishes the different supply voltages for the respective digital and analog control electronics.

A common 2kHz oscillator is used to supply power to the different output current telemetry monitors.

The input/output serial command data is processed within the interface unit. Parallel output lines are decoded by the PPU Command Electronics to establish the turn-on or off of the different outputs and to establish the many different set points for the different output reference generators.

The PPU Control and Protection Electronics monitors both the 200 to 400Vdc bus and 28Vdc bus and provides correct sequential shutdown of the power processor unit if either of the two supply busses are out of specification. The PPU Control Protection Electronics also provides the correct recycling during ion engine arcing and the necessary interrupt signals during abnormal ion engine operation or power source out of limits.

Figure 3-2 illustrates the grounding/isolation system that was designed into the electrical prototype power processor unit. The grounding philosophy includes:

- Isolation of 200 to 400Vdc bus
- Isolation of 28Vdc bus
- Isolation of ion engine
- Isolation of spacecraft computer control box
- Isolation of digital interface unit
- Isolation of PPU commands
- Isolation of PPU telemetry conditioning

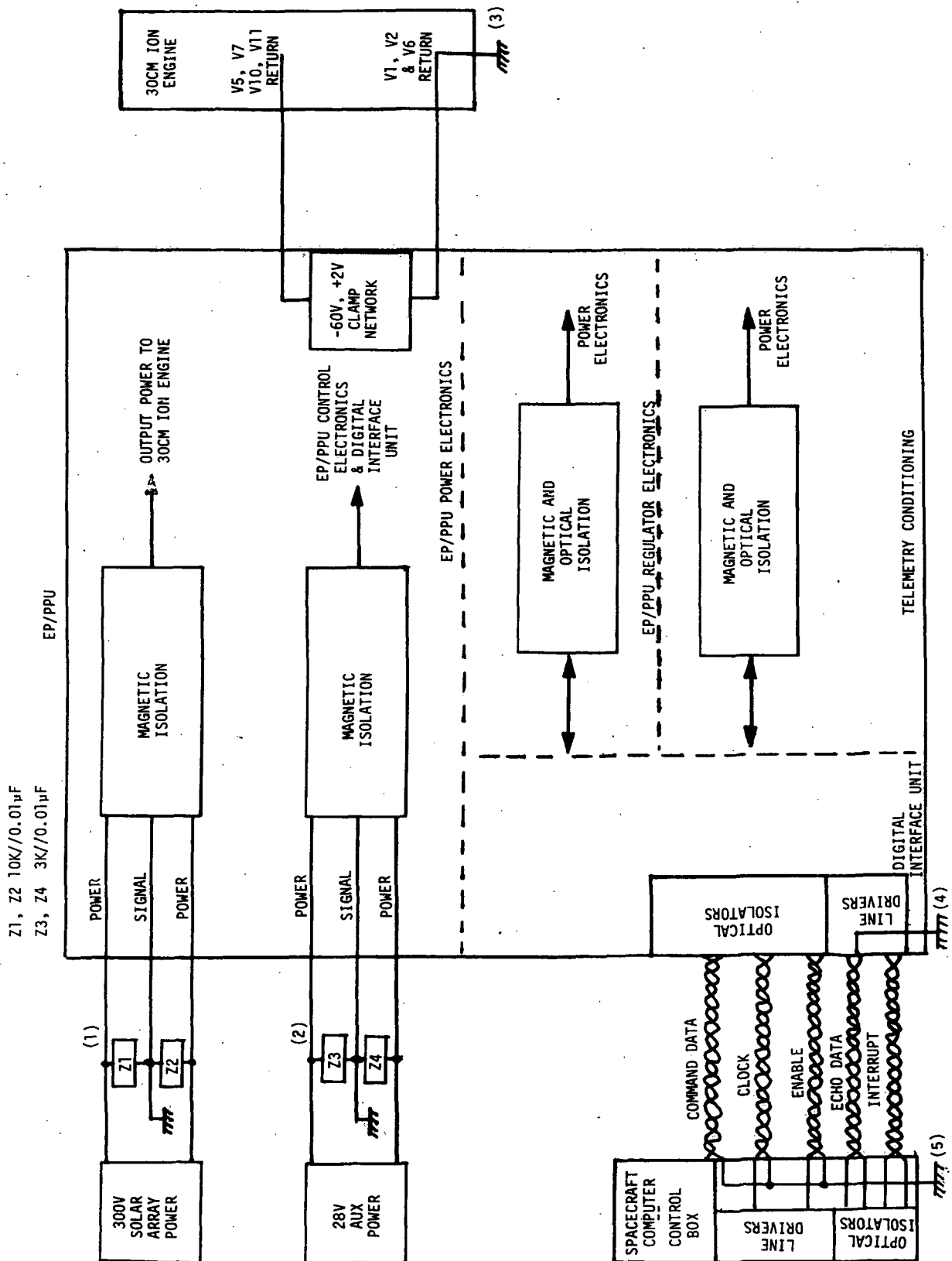


FIGURE 3-2 EP/PPU GROUNDING DIAGRAM

By means of this magnetic and optical isolation, ground loop current and ground return noise is greatly reduced during ion engine arcing and for normal operation of the power processor, switching power electronics.

3.2 ELECTRICAL DESIGN

Electrical design was performed on all major elements of the Power Processor Unit consisting of:

- Beam Supply
- Discharge Supply
- Multiple Inverter and its Nine (9) Separate Outputs
- Command and Protection
- Digital Interface Unit

The electrical design included schematic diagrams, selection of components, magnetic design, generation of part lists and electrical stress analysis to ensure that all components were operating within their allowable stress levels and did not violate the predetermined stress derating factors during normal and abnormal operation due to ion engine startup or arcing.

3.2.1 Beam Supply

The main design changes for the beam supply from contract NAS3-18924, "Breadboard Power Supply," are:

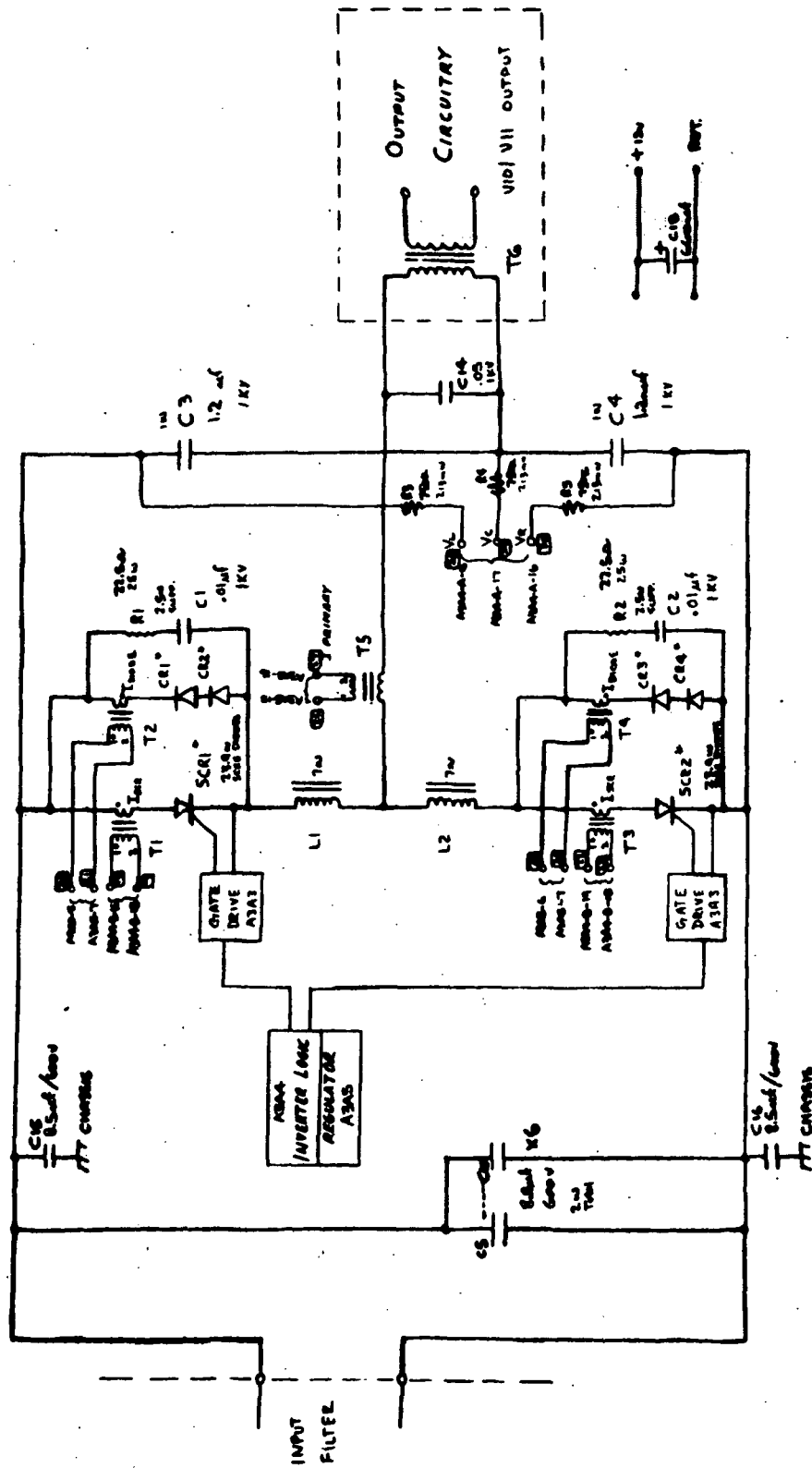
- Operation at 20kHz
- Use of Gate Assisted Turn-Off Thyristor (GATT) as the power switching element to obtain the required turn-off time.

Figure 3-3 presents the schematic of the power stage and its interfaces with the different control electronics.

SCR 1 and 2 are the main power switching semiconductors and the series resonant tank is formed by capacitors C3 and C4 and inductors L1 and L2. The different voltage sensing dividers and current sensing magnetics are identified.

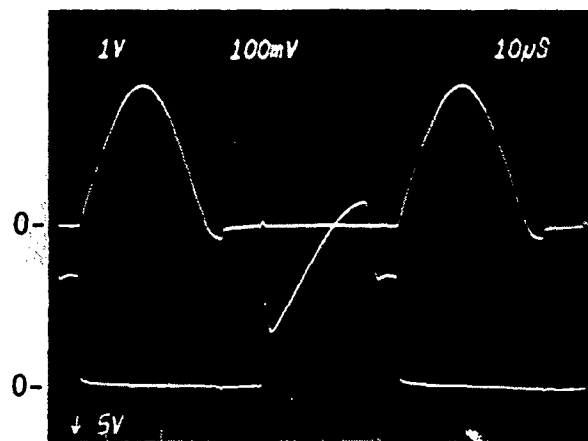
Figure 3-4 presents the schematics of the output power transformer and the high voltage rectifier/filter network. All voltage sensing dividers and magnetic current sensor are identified along with their interfaces with the control electronics.

Figure 3-5 illustrates the thyristor current and voltage during normal operation for 200, 300 and 400Vdc input line voltages. The maximum peak current is 80A and the maximum peak voltage is 620V blocking at the high input line condition of 400Vdc.



- * NOTES
1. SCR1, SCR2 WESTLAWHOUSE A348779, 1KV, 25DA
 2. C1, C2 SEMTECH SA 6795, 500V, 50A
 3. C3, C4 SEMTECH SA 6796, 500V, 50A

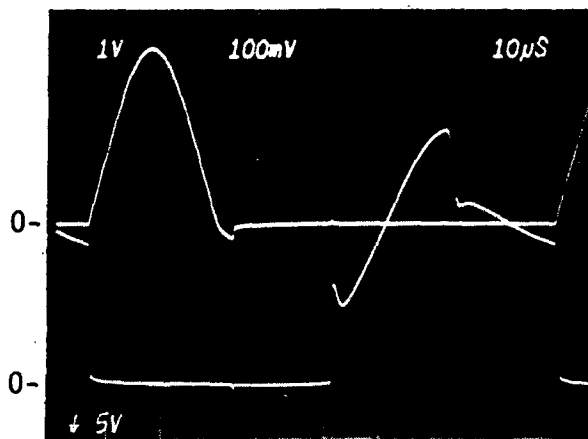
FIGURE 3-3 SCREEN SUPPLY - SERIES RESONANT INVERTER (A3A1) Sheet 1 of 2



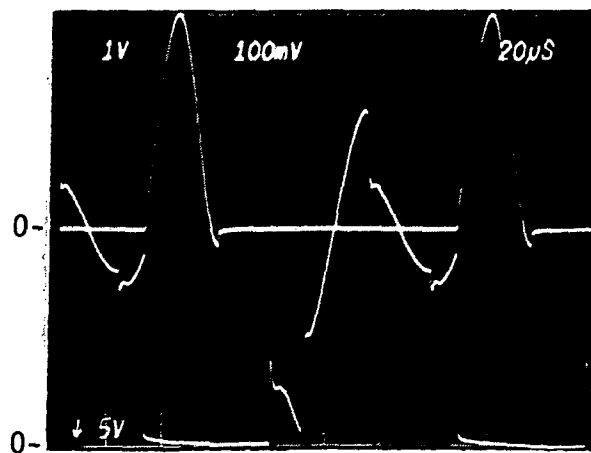
SCR Current
I = 20A/div

SCR Voltage
V = 100V/div

Vin = 200V
Normal Output



Vin = 300V
Normal Output



Vin = 400V
Normal Output

FIGURE 3-5 SCR SERIES RESONANT INVERTER WAVEFORMS (NORMAL OUTPUT)
SCR CURRENT AND VOLTAGE

Figure 3-6 illustrates the thyristor current and voltage during output short circuit where the peak current is 58A and the peak blocking voltage is 560V at the high input line condition of 400Vdc.

These two figures demonstrate the inherent current limiting feature of the series resonant tank circuit to pass only sine wave currents in the power semiconductors and of the protection logic to also keep the system under energy control over the input voltage range and abnormal load conditions.

The transformer primary current and series capacitor voltage during normal output and with a shorted output respectively are given in the Appendix, Figures A-1 and A-2. The transformer current is the combination of the shunt diode current used for energy control of the series resonant capacitors and the higher peak due to the normal conduction of the power thyristors.

Figure A-3 in the Appendix presents transformer current and voltage over the different line conditions.

Figure 3-7 presents the schematic of the accelerator output, regulator and different set points for changing the voltage reference. The schematic of the SCR firing network, Transformers T1 and T2 are the gate control transformers for the two power thyristors, is given in the Appendix, Figure A-4. Each transformer has three different output states:

- Turn on of thyristor (forward gate drive)
- Turn off of thyristor (reverse gate drive)
- Short on control transformer

A short is placed on the transformer during the off period to ensure that no noise pulses will cause premature thyristor turn on. This firing network is controlled by the inverter control logic shown in the Appendix, Figures A-5 and A-6.

The inverter control logic of Figure A-5 provides the basic command signals as a function of the regulator input signal, as a function of the thyristor turn-off signal from the thyristor current monitor and as a function of the series resonant capacitor voltage sensor which limits the maximum energy stored in the capacitors.

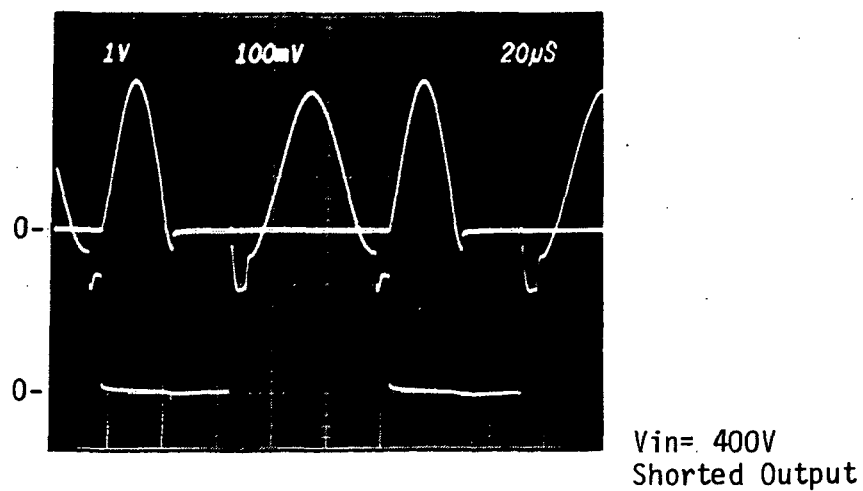
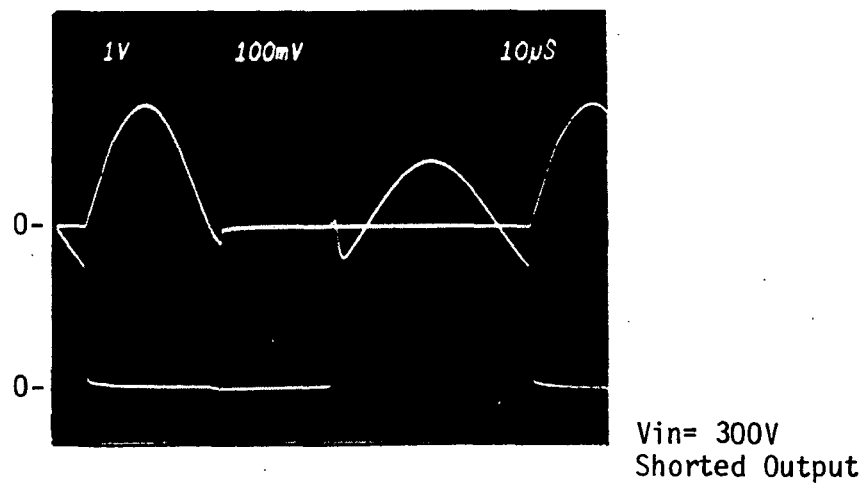
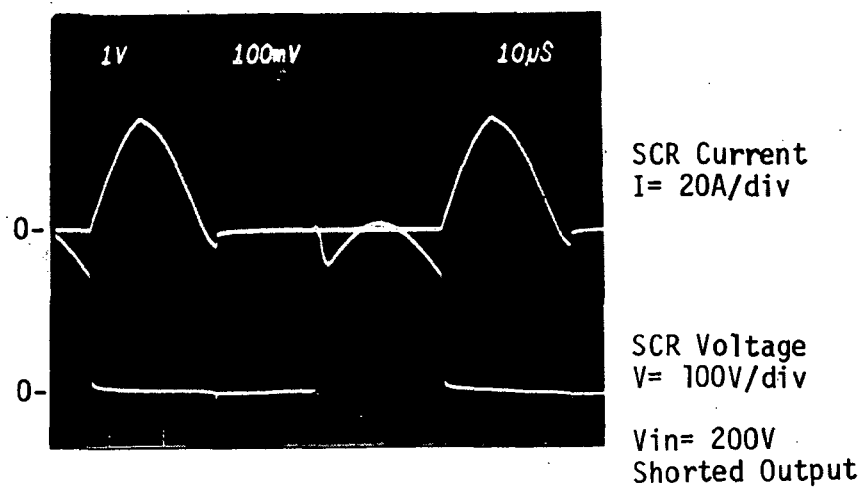


FIGURE 3-6 SCR SERIES RESONANT INVERTER WAVEFORMS (SHORTED OUTPUT)
SCR CURRENT AND VOLTAGE

The inverter control logic of Figure A-6 generates the signals for the turn-on, turn-off and clamping of the thyristor gate control transformers.

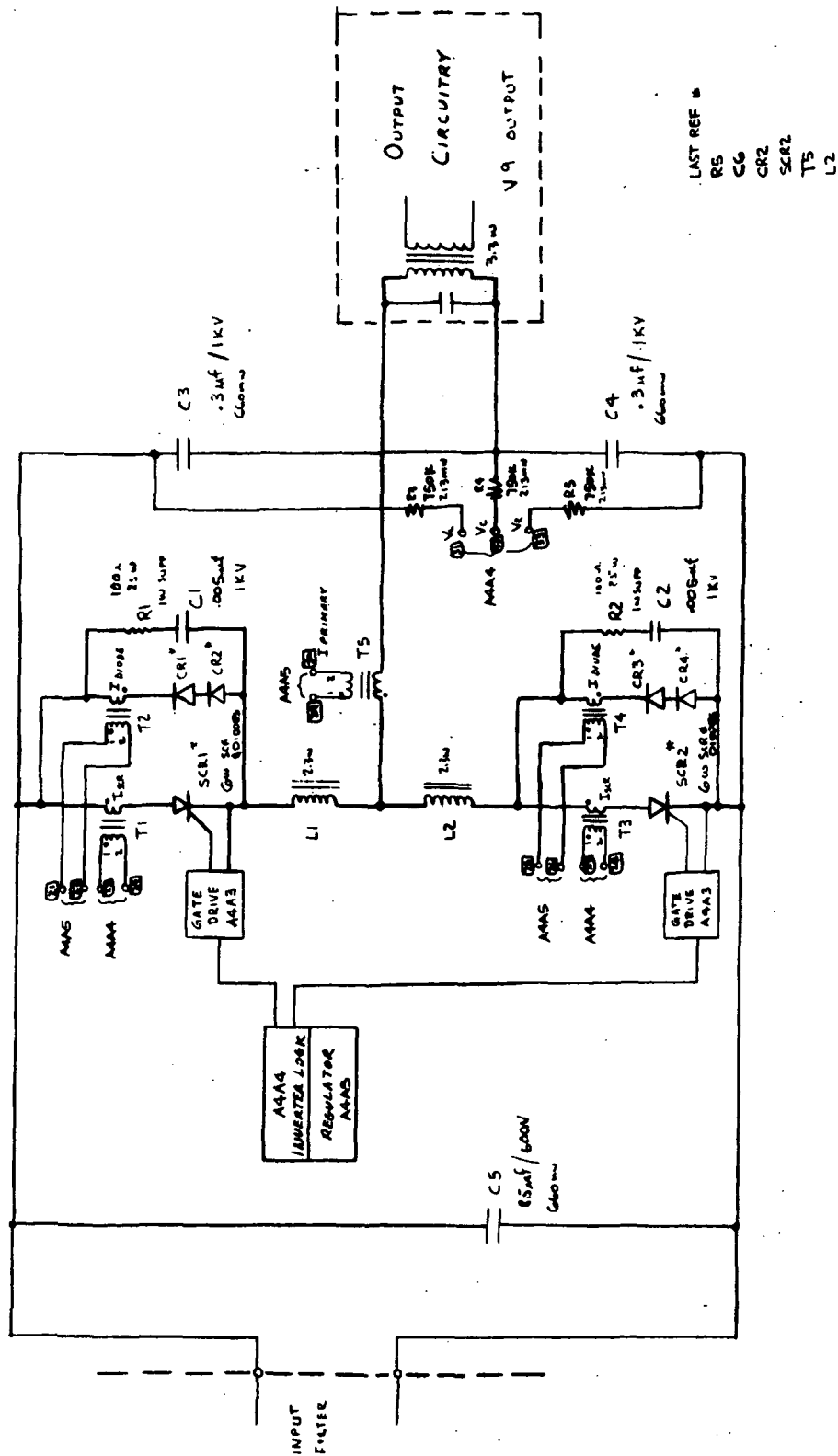
The schematic of the screen voltage regulator is given in the Appendix Figure A-7. The regulator circuit is configured for 2 out of 3 majority voting in order to improve circuit reliability. The circuit includes the output voltage regulator (U1, U2 and U3), primary current regulator (U4, U5, U6) and the accelerator current regulator (U7, U8, and U9). The three different regulator circuits are or-gated together so that each function can independently control the operating condition of the screen supply. During normal operation, the voltage regulator is in command and during engine arcing, the accelerator or screen current regulator takes over control of the screen supply to limit input power current demand.

3.2.2 Discharge Supply

The discharge supply power stage (Figures 3-8 and -9) is very similar to that of the beam supply, discussed in Section 3.2.1, except the maximum output power level is 700W instead of 2.4kW for the discharge supply. The power capacitors, inductors and transformers are scaled down for the lower power level. The power thyristor is the same part type as used in the beam supply. The thyristor firing system is the same as shown in Figure A-4. The inverter control logic is the same as shown in Figures A-5 and A-6.

The output regulator electronics, to provide the necessary current regulation and voltage limit, is given in the Appendix, Figure A-8.

The power component voltage and current waveforms are very similar to those presented in Figures 3-5, 3-6, A-1, A-2 and A-3, except that the peak current is about one-third of the beam inverter current values. The voltage levels are the same.



* NOTE

1. SCR1, SCR2 WETTINGHOUSE A348779, 1VJ, 250A
2. CR1, CR2 SEMTECH SA6798, 500V, 16A
3. CR3, CR4 SEMTECH SA6797, 500V, 16A

FIGURE 3-8 DISCHARGE SUPPLY - SERIES RESONANT INVERTER (A4A1)

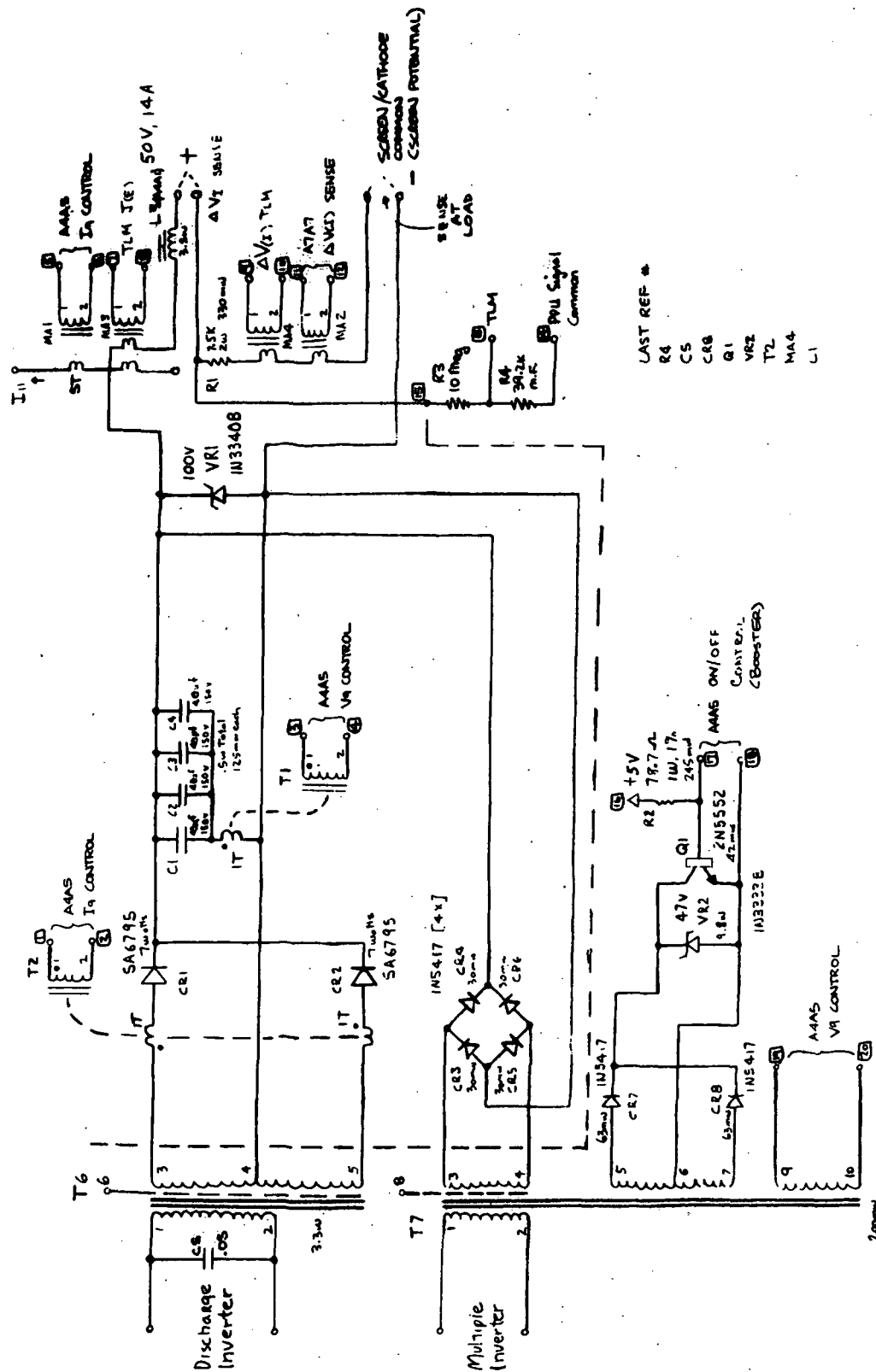


FIGURE 3-9 DISCHARGE SUPPLY - V9 OUTPUT (A4A1/A4A2)

3.2.3 Multiple Inverter

Circuit design and development were performed on the multiple inverter in order to increase the frequency of the internal ac power distribution from 20kHz to 50kHz and thereby reduce the power transformer and filter capacitor weight of the low power, low voltage supplies.

Figure 3-10 presents the schematic of the 50kHz transistorized series resonant inverter used to supply power to nine separate regulated low voltage outputs. Transistors are used, because of their inherent faster turn-off time, of about 1 μ s compared to the seven μ s turn-off time for the power thyristors used in the beam and discharge supplies.

The schematic of the transistor inverter drive network is given in the Appendix, Figure A-9. The turn-on signal initiates current flow in the proportional current drive transformers T6 and T7 (one for each power transistor).

The inverter control logic is the same as used in the beam and discharge supplies and is shown in Figures A-5 and A-6, and the schematic of the output regulator is given in the Appendix, Figure A-10.

Figure 3-11 presents the power transistor voltage and current waveforms and the power transistor turn-on characteristics. The power transformer current and voltage waveshapes are given in the Appendix, Figure A-11.

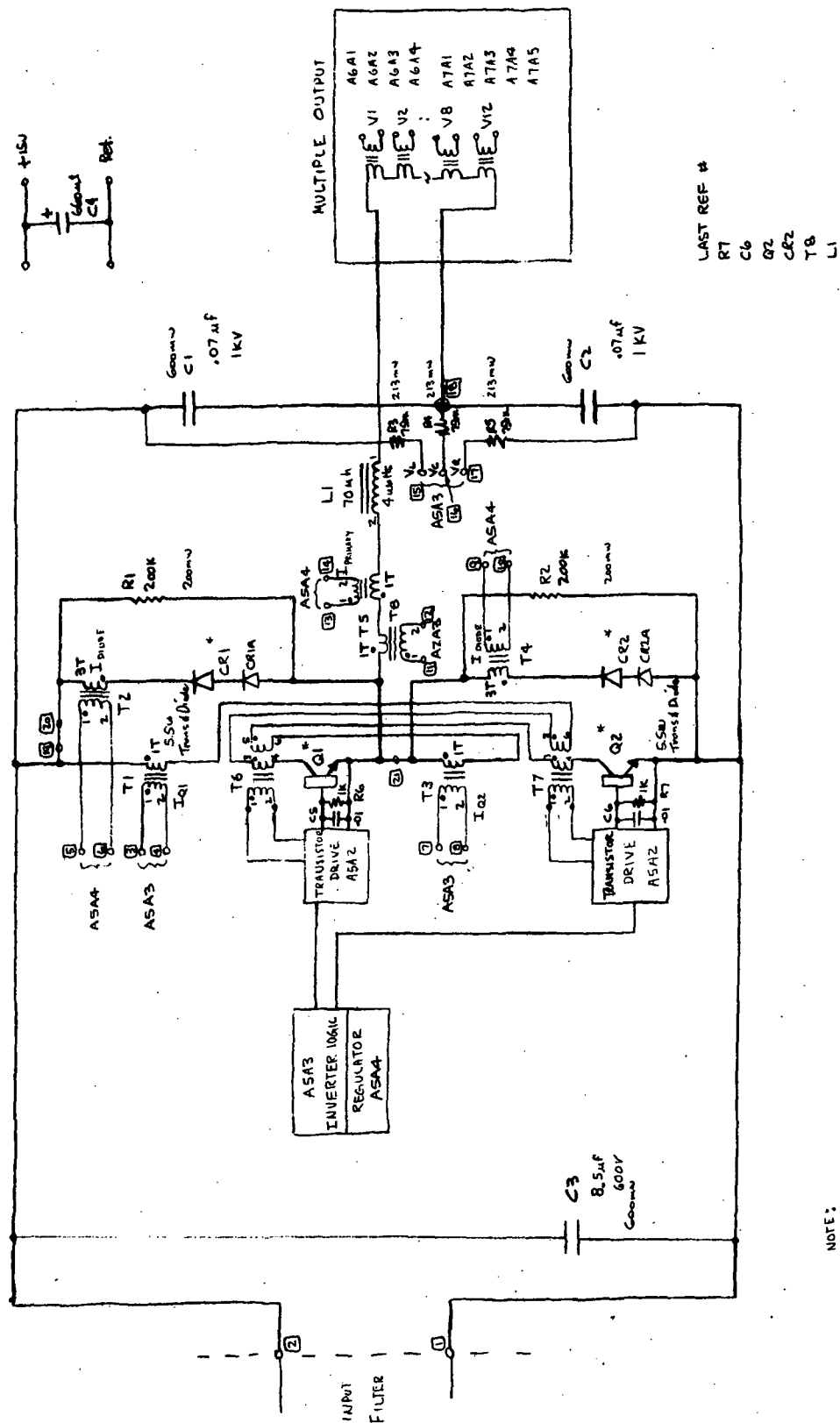
Figure 3-12 presents the schematic of the Cathode Tip Heater Supply (V3) output stage. This is typical for the other eight low voltage outputs. The 50kHz output current passes through the series connection of the primary winding of all nine power transformers, where transformer T1 is a typical unit. Transformer T1 has an isolated output winding (terminals 3, 4, and 5) and a regulation winding (terminals 6, 7, and 8).

Transistor Q1 is turned on to terminate power flow from the primary winding to the output rectifier filter network. By controlling the duty cycle of Q1, both output voltage and current regulation is obtained.

The V3 supply output regulator electronic schematic with its 2 out of 3 majority voting circuit redundancy is given in the Appendix, Figure A-11.

The schematic of the ramp generator which is used in conjunction with the output regulator to provide stable control system operation is given in the Appendix, Figure A-13. The output transformers T1, T2 and T3 have multiple windings where one winding on each transformer is fed to the appropriate redundant output regulator channel.

Figure A-13 presents the operation of shorting transistor Q1 (Figure A-11), both at normal operation and short circuit output delivering regulated output current.



NOTE:
 1. Q1, Q2 - TRU SEMICONDUCTORS, 1P221-001W-001
 2. CR1, CR2 - TRU SEMICONDUCTORS, 1D173-001W-001

FIGURE 3-10 MULTIPLE INVERTER (A5A1)

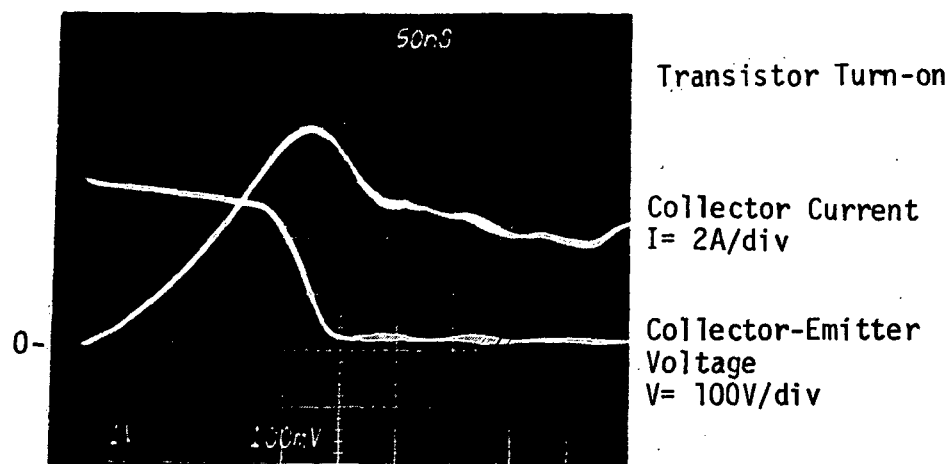
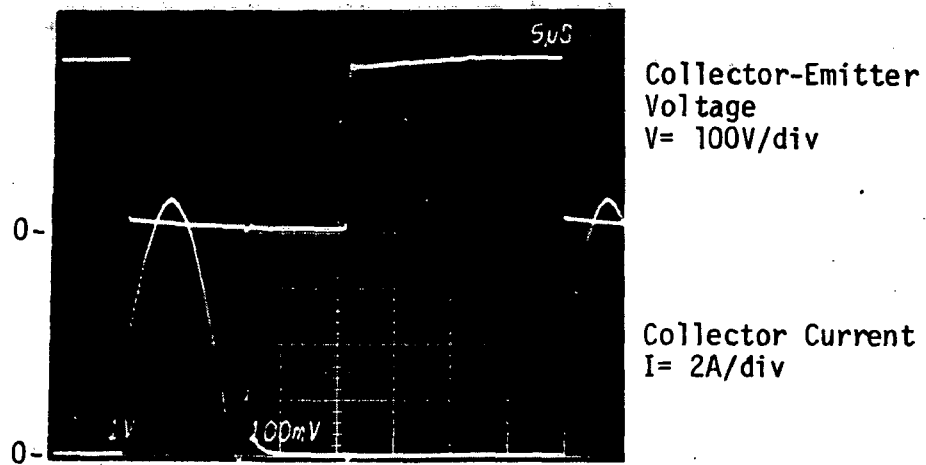
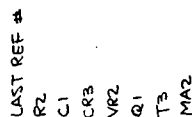


FIGURE 3-11 50 KHZ TRANSISTOR SERIES RESONANT INVERTER WAVEFORMS
TRANSISTOR CURRENT AND VOLTAGE



3-22

3.2.4 Interface Unit, Command, Control and Protection System

The command and protection system was designed to meet the new requirements for the electrical prototype power processor unit. Figure 3-13 shows the basic block diagram for the interface unit, PPU commands, control and protection system.

The interface unit provides electrically isolated, compatible interface between the system computer and the power processor. The following functions are performed:

- Decodes commands
- Performs hard wire logic functions such as turning off appropriate heaters when cathode or neutralizer commission occurs and provides a recycle sequence to allow the thruster to recover from accelerator or screen shorts or current overloads.
- Generates an interrupt when the following abnormal system operation occurs: input voltage out-of-range, neutralizer failure, excessive arcing, and when excessive accelerator current, beam current out-of-range or screen supply voltage out-of-range persists for more than one second.
- Provides requested telemetry

The input includes 40kHz clock line, enable line, and 16 bit serial input data line. Each line goes through an optical isolator to provide the necessary ground isolation and to eliminate ground loop currents and false digital input data.

The heart of the interface unit includes its own timing logic and shift registers to store the serial input data. The parallel output lines are decoded and provide the necessary type of commands:

- Reference set point
- ON/OFF command for each power supply
- Analog references for the beam current, discharge current, magnetic baffle current and screen voltage.
- Selection of a telemetry channel

The return data includes an echo back of the input serial data and the digital coding of a particular TLM channel if commanded and an interrupt signal to the control computer when there is an abnormal operational condition existing in the power processor unit and ion engine combination.

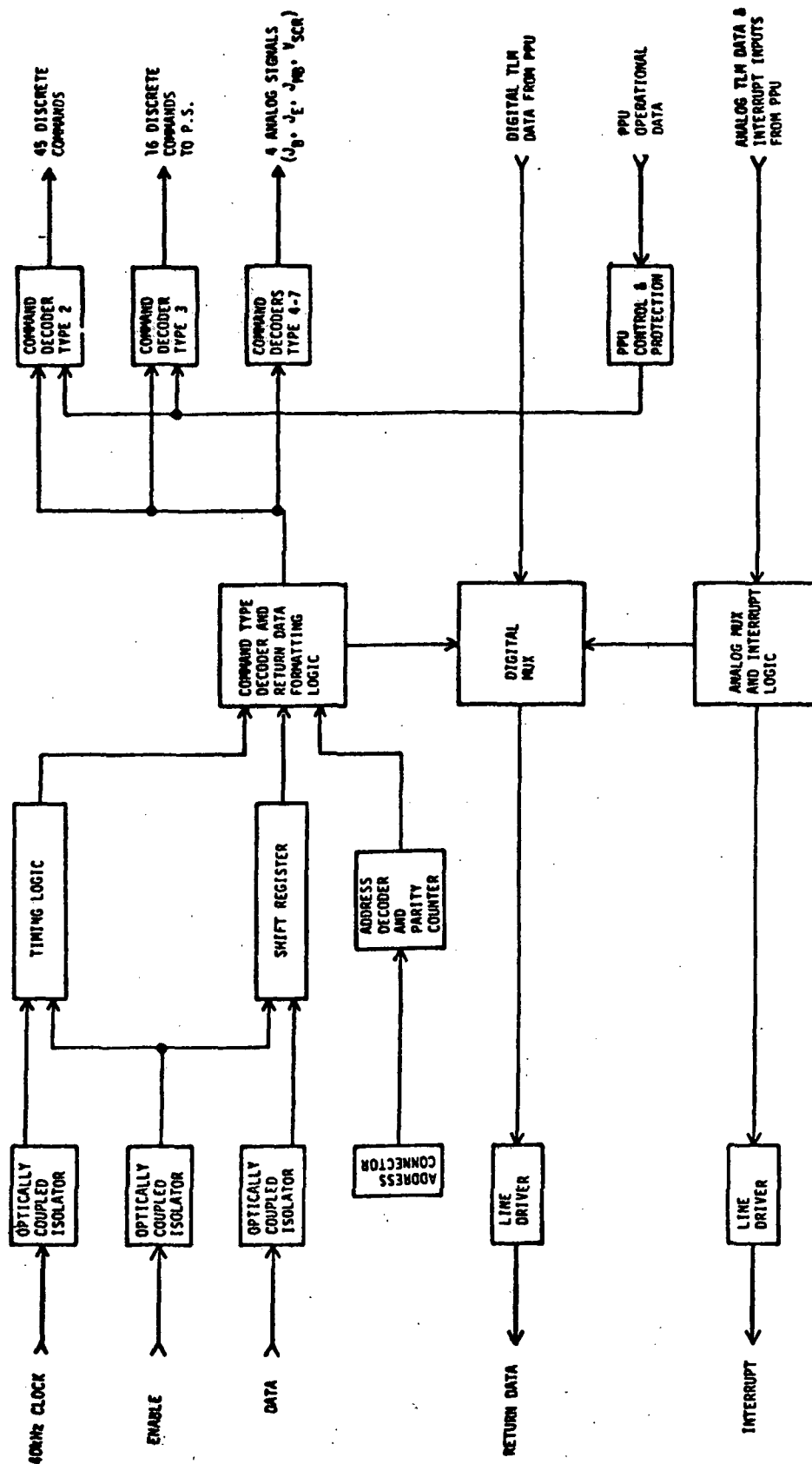


FIGURE 3-13 BLOCK DIAGRAM INTERFACE UNIT, PPU COMMANDS, CONTROL AND PROTECTION SYSTEM

The following schematic diagrams are provided in the Appendix:

Figure A-15, the schematic showing the generation of timing logic and input shift register.

Figure A-16, the schematic of the response data, interrupt line drivers and interrupt status register.

Figure A-17, the schematic of the arc counter register, arc interrupt signal, and two spare status registers.

Figure A-18, the schematic of the 2kHz clock used in the timing of the arc counter and the input address decoder.

Figure A-19 and A-20, the schematics of the decoding and command latches for the different set points.

Figure A-21, the schematic of the decoding and command latches for the power supply ON/OFF commands.

Figure A-22, the schematic of the analog reference commands for beam current, discharge current, magnetic baffle current and screen voltage. Ground isolation is provided for the beam current and magnetic baffle current reference signals.

Figure A-23, the schematic of the TLM channel selector, A to D converter and the 200 to 400VDC voltage sensor used for the PPU power electronics protection during input under or overvoltage operation.

Figure A-24, the schematic of the neutralizer failure detector circuit, beam current interrupt signal, and accelerator current interrupt and screen voltage interrupt signal circuits.

Figure A-25, the schematic of the PPU recycle circuit when there is an arc in the ion engine.

Figure A-26, the schematic of the screen voltage and discharge current analog signal isolator and the 28VDC bus voltage under and overvoltage sensor to turn off the PPU in case of abnormal condition on the control logic power bus.

3.3 ELECTRICAL COMPONENT DEVELOPMENT

The power processor electrical design greatly benefited by the power component development work performed on the contract. The development effort included the following:

- a) Power thyristor mechanical package for component thermal control.
- b) Power transistors evaluation for application in the 50kHz transistor series resonant inverter.
- c) High voltage output diodes with good thermal control.
- d) Series resonant and input/output filter capacitors with reduced weight, good electrical termination with low losses and good mechanical mounting configuration.
- e) High voltage output transformer with good internal voltage gradient control and low internal corona; with good thermal control to maintain low hot spot temperature; and with an impregnation material that will stand the thermal cycling and not develop cracks that could lead to failures due to corona occurring at these crack sites.

The predominant design problem area for these high power, high voltage components is to determine the best thermal control while operating in a thermal vacuum environment where the predominant heat removal is by conduction to a cold plate or heat pipe, and the remainder is by radiation to the surrounding mechanical package.

The EP/PPU design objective of high reliability, high efficiency and minimum weight was translated to the design of all magnetics and, in particular, the beam power transformer. Prior experience with the high voltage transformer used in the Transmitter Experiment Package of the Communication Technology Satellite emphasized the importance of controlling transformer internal temperature rise when operating in space environments. It was decided early in the program that the maximum average winding temperature, as measured by winding dc resistance, would be limited as a goal to 85°C or 35°C rise over the maximum allowable 50°C baseplate or heat sink. The basic reason for this temperature limit is the desire for long life performance of the polyurethane potting compound. Since there is no data for determination of reduced dielectric strength behavior as a function of life for polyurethane operating in

space vacuum conditions, a most conservative approach was taken. While polyurethane is used for long life applications between 100°C and 125°C, it is generally agreed that there is no evidence of polyurethane degradation at 85°C or below.

The transformer electrical, mechanical and thermal designs were governed by the design philosophy to first minimize the losses and second to permit short, direct, low thermal impedance paths to the heat sink.

The results were worth the effort. Maximum temperature rise of any winding when tested at full load in vacuum met the design objectives. A calorimeter loss measurement of the transformer was 28W loss at full load at a 50°C heat sink. Voltage control objectives were verified by corona test data.

The beam power transformer design features are highlighted in Figures 3-14 and 3-15.

A more detailed discussion on the power transformers design and testing, power capacitors selection and development, and power semiconductors characterization and development can be found in the Appendix, Section B.

Continued component work is recommended to further reduce the weight of components, to enhance thermal control, to develop final flight component specification and to qualify these few special components for space flight.

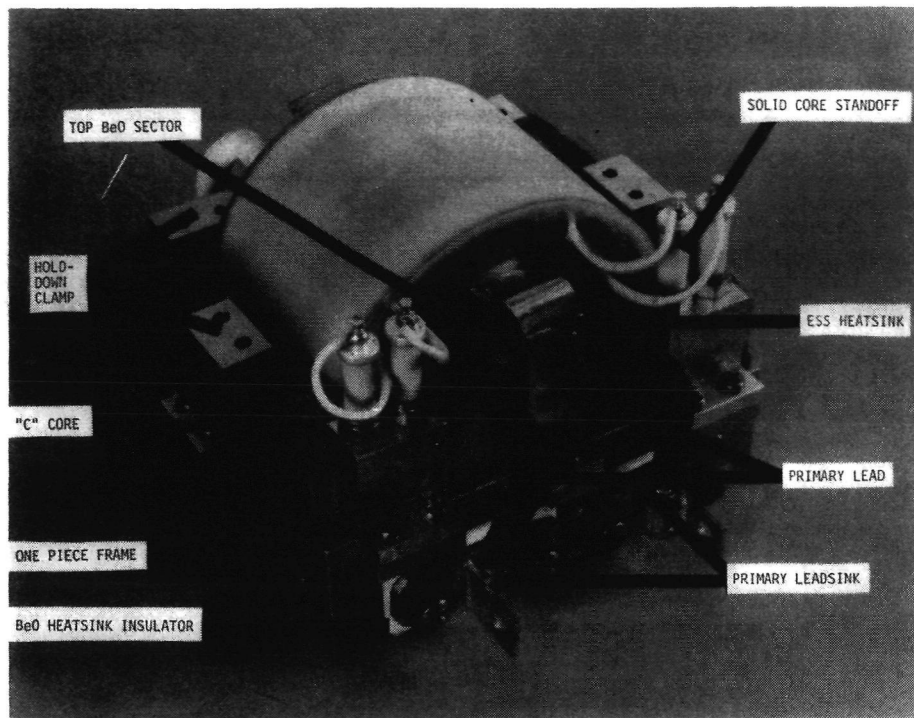


FIGURE 3-14 SCREEN TRANSFORMER

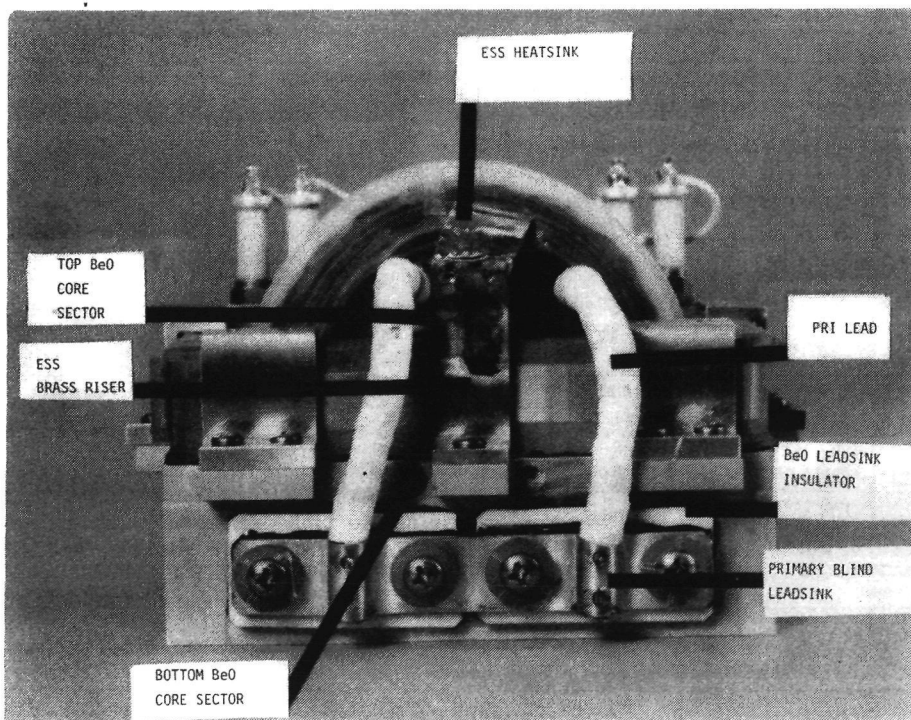


FIGURE 3-15 SCREEN TRANSFORMER, REAR VIEW

3.4 MECHANICAL DESIGN

The electrical prototype power processor unit (EP/PPU) brassboard was fabricated having the modular configuration, shown in Figure 3-51. It represents the logical division into seven functional modules provides the necessary thermal control of the components in thermal vacuum, and provides the necessary separation between the power components, high voltage components and low level control electronics.

In Figure 3-16 the input connectors are located on the left side and include, from top to bottom, the interface unit, 28Vdc input, 200 to 400Vdc input and temperature sensor connectors. Separate cover assemblies are placed over each cable assembly to provide the necessary shielding between the power and signal cabling.

The high voltage output cabling is seen on the right side of the unit. The high and low voltage outputs are connected to the power processor by means of terminal strips and lugs instead of connectors.

Figure 3-17 illustrates the relative location of each of the modules providing shielding for low level electronics and shielding between high voltage and low voltage components.

The EP/PPU includes the relative location of each of the modules providing shielding for low level electronics and shielding between high voltage and low voltage components.

The EP/PPU includes the following modules:

- A1, Input power
- A2, Command interface
- A3, Screen supply
- A4, Discharge supply
- A5, Multiple inverter
- A6, High voltage output
- A7, Low voltage output

Figure 3-18 shows the seven modules with the interconnecting cable harness in the open position. The functional module power processor unit (FM/PPU) being designed by NASA Lewis Research Center will reduce the overall size. The intent of the EP/PPU program was to develop the modular concept and allow for ease of checkout during development testing of the initial brassboard design.

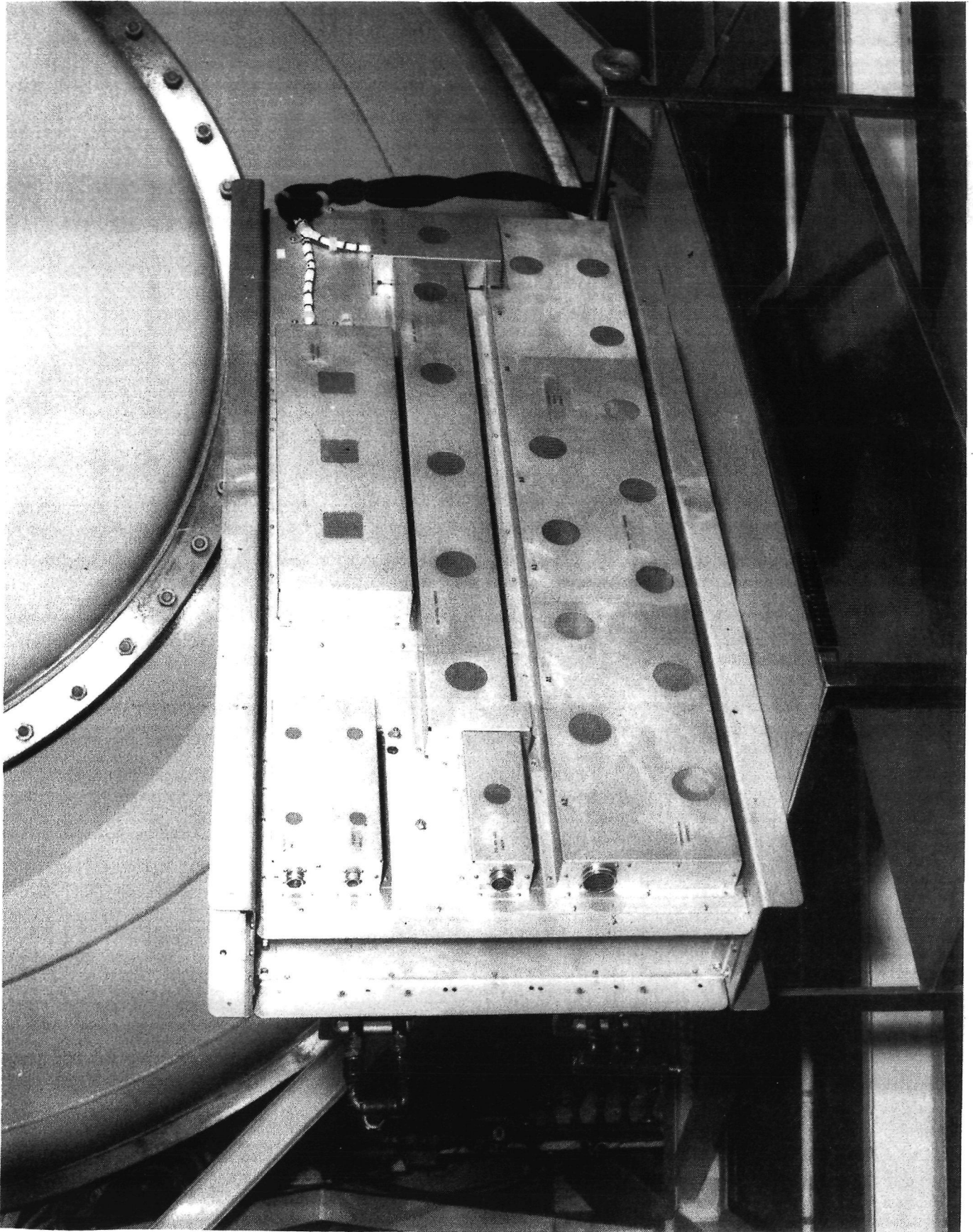


FIGURE 3-16 ELECTRICAL PROTOTYPE POWER PROCESSOR

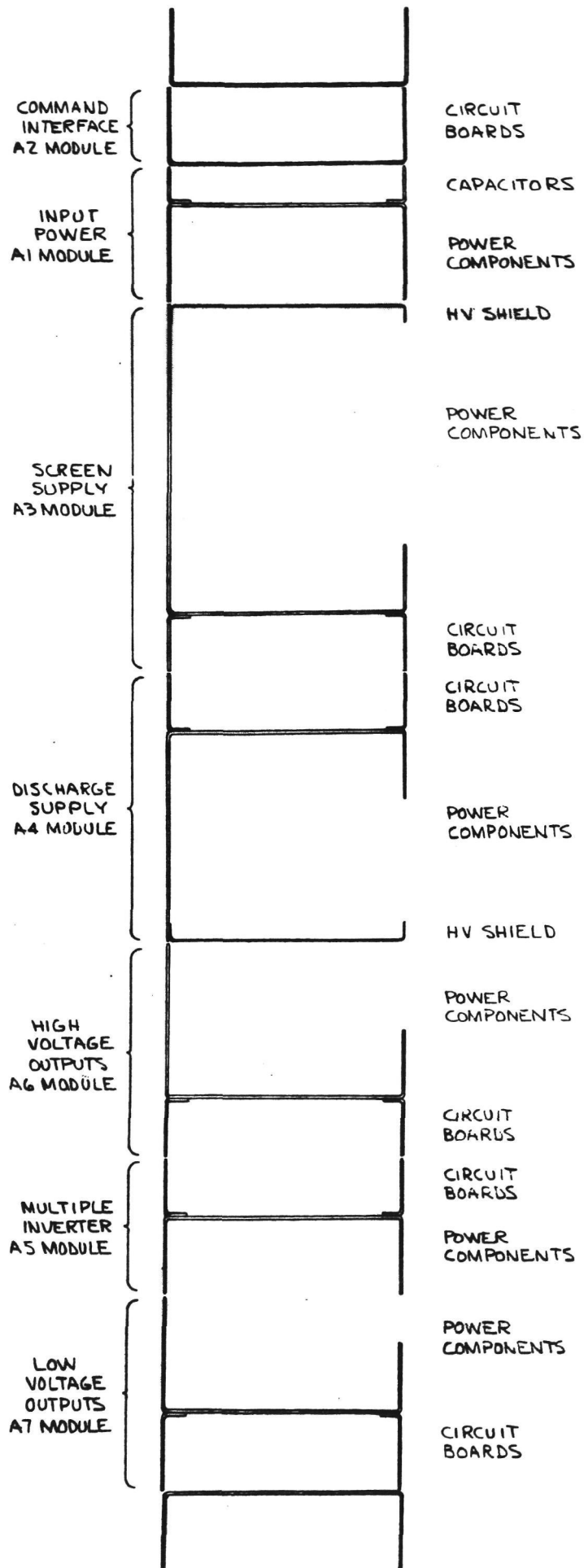


FIGURE 3-17 EP/PPU PARTITIONING

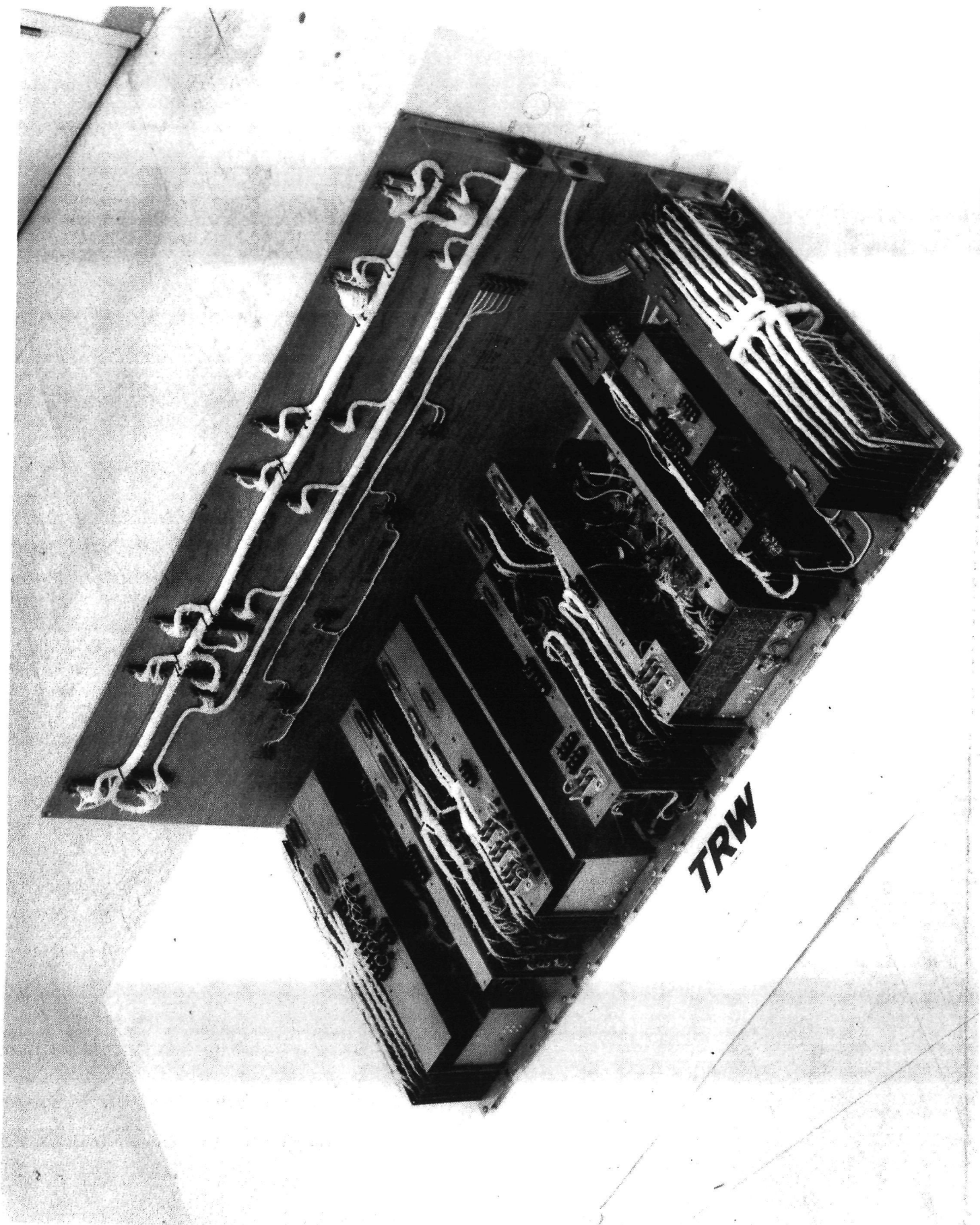


FIGURE 3-18. EP/PPU MODULES

3.5 THERMAL CONTROL

All power components dissipating more than one watt were mounted on the bottom flange of each module. A heat pipe simulator was then connected to the base in order to remove the internally generated heat.

Figure 3-19 shows the heat pipe simulator connected to the electrical prototype unit. Due to the unbalanced heat distribution in the power processor, one saddle had two pipes and the other saddle had three pipes in order to handle the thermal heat and still provide a redundant pipe in case of a heat pipe failure.

Figure 3-20 shows the relative module location and the power dissipation estimated at each heat pipe saddle connection.

Additional thermal control was provided on each printed circuit board in order to transfer heat from hot low level electronic components to the printed circuit board mounting frame and then into the module flange.

During the mechanical layout of each module, critical components were identified which were monitored with a thermistor. During thermal vacuum tests these temperatures were recorded in support of the detail mechanical and thermal design being performed at NASA Lewis Research Center on the Functional Module.

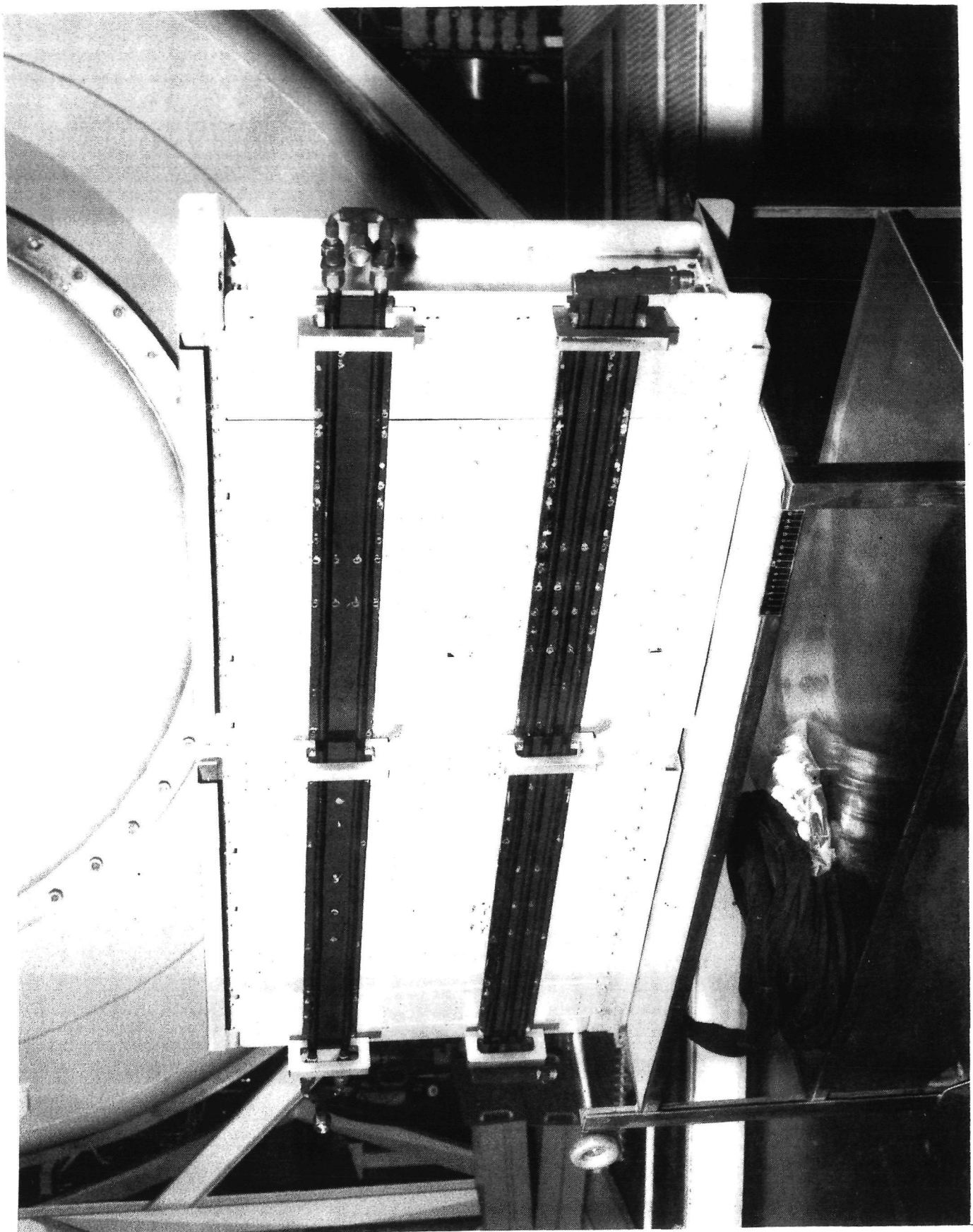


FIGURE 3-19 EP/PPU HEAT PIPE SIMULATOR

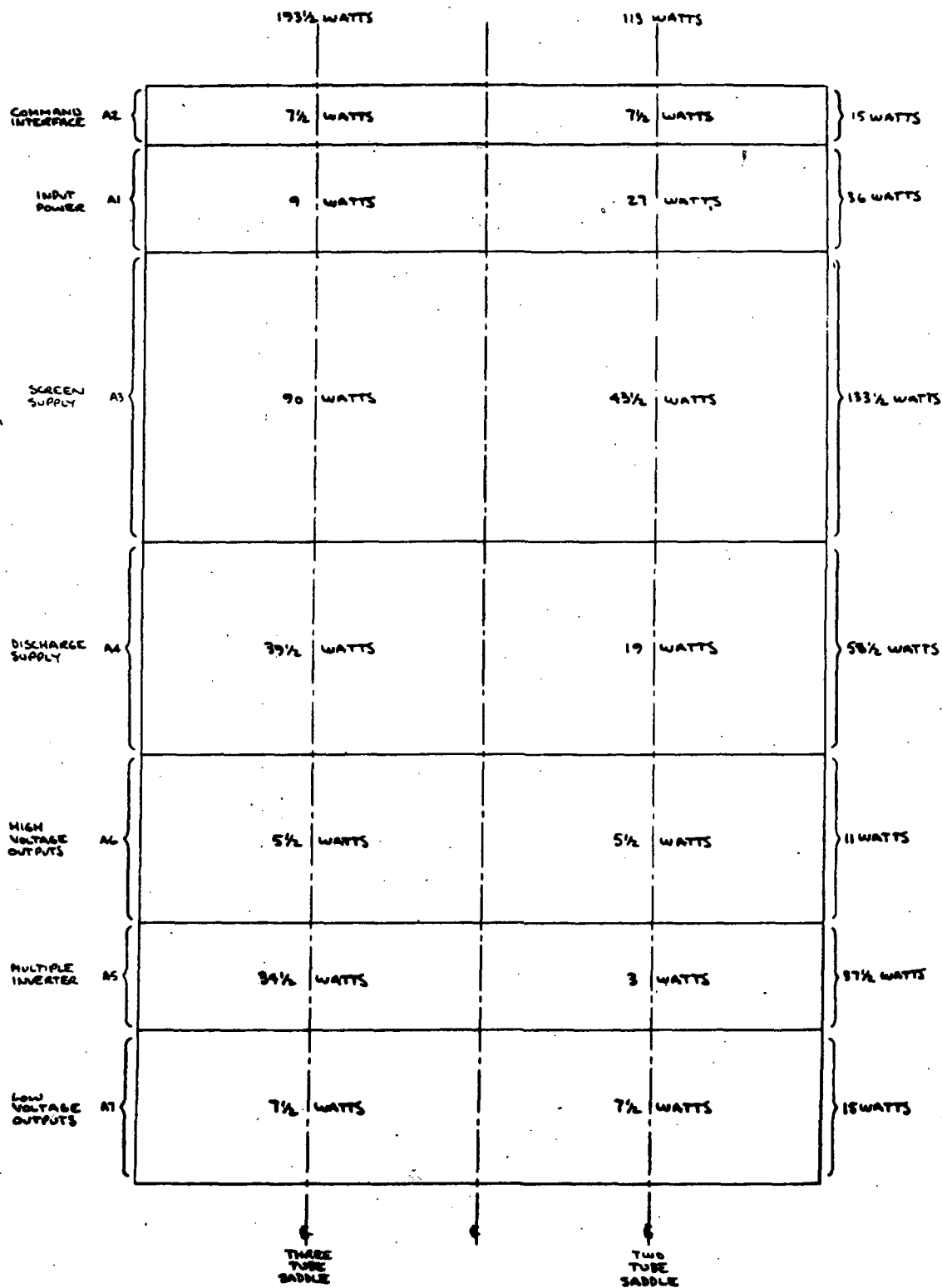


FIGURE 3-20 MODULAR THERMAL HEAT FLOW

3.6 DESIGN ANALYSIS

The electrical prototype power processor design was reviewed in the following areas in order to better understand the power processor design characteristics and to identify design areas for further improvement:

- Weight
- Loss/efficiency
- Part count
- Reliability

Table 3-I presents component weight information. This table identifies the different mechanical subassemblies and the component weight as to the type of component (control electronics, power magnetics, power capacitors, power semiconductors, magnetic sensors and miscellaneous parts). In reviewing the weight totals, the following basic observations and conclusions can be projected:

- (1) Power magnetic components account for 48% of the total component weight.
- (2) Magnetic current sensor components account for 5% of the total component weight.
- (3) Low voltage outputs (A5, A6, A7) account for 24% of the total component weight.
- (4) Power capacitors components account for 23% of the total component weight.
- (5) Control electronic components account for 14% of the total component weight.

The EP/PPU weight can be further reduced by improved component thermal characteristics, by improved component packaging configurations or by circuit simplification.

Table 3-II presents an estimate of the component losses for each mechanical subassembly in the control electronics, power magnetics, power capacitors, power semiconductors, magnetic sensors and miscellaneous components. In reviewing the loss data, the following basic observations and conclusions can be projected:

TABLE 3-1 EP/PPU COMPONENT WEIGHT ANALYSIS

MODULE	SUBASSEMBLY	COMPONENT WEIGHT-GRAMS						TOTAL
		CONTROL ELECT.	POWER MAGNETICS	POWER CAPACITORS	POWER SEMI-COND.	SENSORS (MAGNETIC)	MISC	
A1 Module Input Power	A1A1 DC Input Filter	--	1336	1660	--	12.3	30.3	3038.6
	A1A2 28V Converter-Power Stage	--	245.3	244	47.1	13	44.3	590.7
	A1A3 28V Converter-Control	20.2	--	--	--	--	--	20.2
	A1A4 TLH Oscillator	24.35	42.2	--	--	--	--	66.55
	A1 Module Subtotal	44.55	1623.5	1809	47.1	25.3	74.6	3724.05
A2 Module Command Interface	A2A1 Digital Interface	15.55	--	--	--	--	--	15.55
	A2A2 Digital Interface	13.05	--	--	--	--	--	13.05
	A2A3 Digital Interface	8.05	--	--	--	--	--	8.05
	A2A4 Digital Interface	14.65	--	--	--	--	--	14.65
	A2A5 PPU Commands	25.25	--	--	--	--	--	25.25
	A2A6 PPU Commands	20.9	--	--	--	--	--	20.9
	A2A7 PPU Commands	21.4	--	--	--	--	--	21.4
	A2A8 PPU Control and Protection	82.8	--	--	--	--	--	82.8
	A2A9 PPU Control and Protection	41.15	--	--	--	--	--	41.15
	A2A10 PPU Control and Protection	57.9	--	--	--	--	--	57.9
	A2A11 PPU Control and Protection	71.0	--	--	--	--	--	71.0
	A2A12 PPU Control and Protection	103.35	--	--	--	--	--	103.35
	A2A13 Telemetry	49.95	--	--	--	--	--	49.95
	A2 Module Subtotal	525	--	--	--	--	--	525
A3 Module Beam Supply	A3A1 Power Stage-Baseplate	--	3180	939.1	617.5	122	82.9	4941.5
	A3A2 Accelerator Regulator	33.7	--	10.5	65.6	--	3.5	113.3
	A3A3 SCR Firing	35.5	32.8	--	20.4	--	--	88.7
	A3A4 Control Logic	107.35	--	--	--	--	--	107.35
	A3A5 Screen Regulator	84.5	--	--	--	--	--	84.5
	A3A6 Telemetry	102.95	--	--	--	--	--	102.95
	A3 Module Subtotal	364	3212.8	949.6	703.5	122	86.4	5438.3
A4 Module Discharge Supply	AAA1 Power Stage-Baseplate	--	1715	244.8	488.4	46.5	50.1	2544.8
	AAA2 High Voltage Assembly	--	--	323.2	68.6	88.4	1.15	481.35
	AAA3 SCR Firing	35.5	32.8	--	20.4	--	--	88.7
	AAA4 Control Logic	107.35	--	--	--	--	--	107.35
	AAA5 Discharge Regulator	83.85	--	--	--	--	--	83.85
	AAA6 Telemetry	51	--	--	--	--	--	51
	A4 Module Subtotal	277.7	1747.8	568	577.4	134.9	51.25	3357.05
A5 Module Multiple Inverter	ASA1 Power Stage-Baseplate	--	111.8	132.4	37.6	53	40.1	374.9
	ASA2 Transistor Drive Network	72.9	--	18.6	20.4	--	--	111.9
	ASA3 Control Logic	88.45	--	--	--	--	--	88.45
	ASA4 Multiple Inverter Regulator	58.6	--	--	--	--	--	58.6
	ASA5 Ramp Generator	16.85	122.4	--	--	--	--	139.25
	A5 Module Subtotal	236.8	234.2	151	58	53	40.1	773.1
A6 Module High Voltage Outputs	A6	--	--	--	--	--	63	63
	AGA1 V3 Output	--	126.3	19.8	39.95	82.5	1.8	270.35
	AGA2 V4 Output	--	75.7	19.8	8.4	54.55	0.2	158.65
	AGA2A Relay Driver	--	37.6	20.5	5.2	--	40.15	103.45
	AGA3 V8 Output	--	112.1	28.4	31.3	61.8	2.0	235.6
	AGA4 V12 Output	--	94.49	95	15.1	35.5	0.1	240.19
	AGA5 V3 Regulator	42.75	--	--	--	--	--	42.75
	AGA6 V4 Regulator	42.45	--	--	--	--	--	42.45
	AGA7 V8 Regulator	44.5	--	--	--	--	--	44.5
	AGA8 V12 Regulator	41.6	--	--	--	--	--	41.6
	AGA9 Telemetry	53.5	--	--	--	--	--	53.5
	AGA10 Reference	48.45	--	--	--	--	--	48.45
	A6 Module Subtotal	273.25	446.19	183.5	99.95	234.35	107.25	1344.49
A7 Module Low Voltage Outputs	A7	--	--	--	--	--	81	81
	A7A1 V1 Output	--	67.3	19.8	7.1	49.5	1.0	144.7
	A7A2 V2 Output	--	59	19.8	7.1	49.5	0.2	135.6
	A7A3 V6 Output	--	59	19.8	7.1	49.5	0.2	135.6
	A7A4 V5 Output	--	126.3	19.8	39.95	82.5	1.55	270.1
	A7A5 V7 Output	--	478.95	28.4	56.75	108.8	2.75	675.65
	A7A6 V1 Regulator	54.6	--	--	--	--	--	54.6
	A7A7 V2 Regulator	54.6	--	--	--	--	--	54.6
	A7A8 V6 Regulator	54.6	--	--	--	--	--	54.6
	A7A9 V5 Regulator	42.75	--	--	--	--	--	42.75
	A7A10 V7 Regulator	44.45	--	--	--	--	--	44.45
	A7A11 Telemetry	58.15	--	--	--	--	--	58.15
	A7A12 Reference	74.35	--	--	--	--	--	74.35
	A7A13 Reference	69.9	--	--	--	--	--	69.9
	A7A14 Reference	70.95	--	--	--	--	--	70.95
	A7A15 Reference	38.1	--	--	--	--	--	38.1
	A7 Module Subtotal	562.45	790.55	107.6	118	339.8	86.7	2005.1
Total EP/PPU		2283.75	8055.04	3868.7	1603.95	909.35	446.3	17167.09

TABLE 3-II EP/PPU COMPONENT LOSS ANALYSIS

MODULE	SUBASSEMBLY	COMPONENT LOSS-WATTS						TOTAL
		CONTROL ELECT.	POWER MAGNETICS	POWER CAPACITORS	POWER SEMI-COND.	SENSORS (MAGNETIC)	MISC.	
A1 Module Input Power	A1A1 DC Input Filter	--	6.400	--	--	.080	--	6.480
	A1A2 28V Converter-Power Stage	--	2.625	2.100	12.60	.525	1.050	18.900
	A1A3 28V Converter-Control	.235	--	--	--	--	--	.235
	A1A4 TLM Oscillator	2.500	.250	--	--	--	--	2.750
	A1 Module Subtotal	2.735	9.275	2.100	12.60	.605	1.050	28.365
A2 Module Command Interface	A2A1 Digital Interface	1.930	--	--	--	--	--	1.930
	A2A2 Digital Interface	1.180	--	--	--	--	--	1.180
	A2A3 Digital Interface	1.490	--	--	--	--	--	1.490
	A2A4 Digital Interface	1.150	--	--	--	--	--	1.150
	A2A5 PPU Commands	.850	--	--	--	--	--	.850
	A2A6 PPU Commands	1.197	--	--	--	--	--	1.197
	A2A7 PPU Commands	1.210	--	--	--	--	--	1.210
	A2A8 PPU Control and Protection	2.290	--	--	--	--	--	2.290
	A2A9 PPU Control and Protection	1.780	--	--	--	--	--	1.780
	A2A10 PPU Control and Protection	1.930	--	--	--	--	--	1.930
	A2A11 PPU Control and Protection	2.660	--	--	--	--	--	2.660
	A2A12 PPU Control and Protection	2.320	--	--	--	--	--	2.320
	A2A13 Telemetry	.156	--	--	--	--	--	.156
	A2 Module Subtotal	20.143	--	--	--	--	--	20.143
A3 Module Beam Supply	A3A1 Power Stage-Baseplate	--	52.000	7.600	81.000	3.000	12.970	156.570
	A3A2 Accelerator Regulator	.552	--	--	1.200	--	2.268	4.021
	A3A3 SCR Firing	.410	.200	--	4.575	--	6.672	11.857
	A3A4 Control Logic	3.408	--	--	--	--	--	3.408
	A3A5 Screen Regulator	2.020	--	--	--	--	--	2.020
	A3A6 Telemetry	.110	--	--	--	--	--	.110
	A3 Module Subtotal	6.501	52.200	7.600	86.775	3.000	21.910	177.986
A4 Module Discharge Supply	A4A1 Power Stage-Baseplate	--	17.000	1.100	18.000	.500	.500	37.100
	A4A2 High Voltage Assembly	--	--	3.000	19.000	.500	.500	23.000
	A4A3 SCR Firing	.430	.200	--	4.575	--	6.652	11.857
	A4A4 Control Logic	3.408	--	--	--	--	--	3.408
	A4A5 Discharge Regulator	1.115	--	--	--	--	--	1.115
	A4A6 Telemetry	.110	--	--	--	--	--	.110
	A4 Module Subtotal	5.063	17.200	4.100	41.575	1.000	7.652	76.590
A5 Module Multiple Inverter	A5A1 Power Stage-Baseplate	--	4.000	1.220	15.700	1.000	1.000	22.920
	A5A2 Transistor Drive Network	1.672	--	--	1.717	--	4.591	8.000
	A5A3 Control Logic	3.286	--	--	--	--	--	3.286
	A5A4 Multiple Inverter Regulator	.639	--	--	--	--	--	.639
	A5A5 Ramp Generator	.494	.050	--	--	--	--	.544
	A5 Module Subtotal	6.091	4.050	1.220	17.437	1.000	5.591	35.389
A6 Module High Voltage Outputs	A6A1 V3 Output	--	4.620	--	1.984	.050	.855	7.509
	A6A2 V4 Output	--	1.500	--	.643	.050	.277	2.470
	A6A2A Relay Driver	--	.638	--	.267	--	.120	1.025
	A6A3 V8 Output	--	1.140	--	1.902	.050	.166	3.254
	A6A4 V12 Output	--	.960	--	2.567	.050	.177	3.754
	A6A5 V3 Regulator	.736	--	--	--	--	--	.736
	A6A6 V4 Regulator	.745	--	--	--	--	--	.745
	A6A7 V8 Regulator	.896	--	--	--	--	--	.896
	A6A8 V12 Regulator	.683	--	--	--	--	--	.683
	A6A9 Telemetry	.120	--	--	--	--	--	.120
	A6A10 Reference	.818	--	--	--	--	--	.818
	A6 Module Subtotal	3.998	8.858	--	7.363	.200	1.595	22.014
A7 Module Low Voltage Outputs	A7	--	--	--	--	--	--	--
	A7A1 V1 Output	--	.900	--	.954	.050	.175	2.079
	A7A2 V2 Output	--	.900	--	.954	.050	.175	2.079
	A7A3 V6 Output	--	.900	--	.954	.050	.175	2.079
	A7A4 V5 Output	--	4.620	--	1.984	.050	.855	7.509
	A7A5 V7 Output	--	3.815	--	9.328	.050	.611	13.804
	A7A6 V1 Regulator	.998	--	--	--	--	--	.998
	A7A7 V2 Regulator	.899	--	--	--	--	--	.899
	A7A8 V6 Regulator	.886	--	--	--	--	--	.886
	A7A9 V5 Regulator	.737	--	--	--	--	--	.737
	A7A10 A7 Regulator	.738	--	--	--	--	--	.738
	A7A11 Telemetry	.150	--	--	--	--	--	.150
	A7A12 Reference	.855	--	--	--	--	--	.855
	A7A13 Reference	1.013	--	--	--	--	--	1.013
	A7A14 Reference	1.060	--	--	--	--	--	1.060
	A7A15 Reference	.809	--	--	--	--	--	.809
	A7 Module Subtotal	8.145	11.135	--	14.174	.250	1.991	35.695
Total EP/PPU		52.676	102.718	15.020	179.824	6.055	39.789	396.182
Total EP/PPU Output Power = 2690 Watts								

- (1) The power semiconductor losses account for 45% of the total component losses.
- (2) The power magnetic losses account for 25% of the total component losses.
- (3) The control electronic losses account for 13% of the total component losses.

By reducing the losses in these areas, the overall efficiency of the power processor can be further improved. These improvements include improved power semiconductors with lower forward drops and switching losses, improved magnetic designs and simplification of the control electronics.

Table 3-III presents the component parts count for each mechanical subassembly as a function of control electronics, power magnetics, power capacitors, power semiconductors, magnetic sensors and miscellaneous components.

The following observation and conclusion can be made based on the results of the analysis of the total part count:

The control electronics account for 85% of the total part count.

The EP/PPU part count can be reduced by circuit simplification and miniaturization of Control Electronics. Prime candidates are elimination of non-essential auxiliary functions, the use of multiple voltage comparators and resistors in a single package and the use of hybridized regulators (Standard Control Module with multiple loop control concept, developed on the NASA/LeRC sponsored SCM Program, of which 24 are used on the EP/PPU).

In many areas circuit redundancy was included for reliability improvements. In general the high part count was also affected by the large number of commands and operating set points for the different power processor outputs.

Figure 3-21 shows power processor unit reliability block diagram, where each mechanical subassembly is identified with its particular redundancy configuration. The command interface module A2 does not have any redundancy in the present design, but the reliability estimate was performed including redundancy in this particular high part count area.

TABLE 3-III EP/PPU COMPONENT PART COUNT ANALYSIS

MODULE	SUBASSEMBLY	COMPONENT PART COUNT						TOTAL
		CONTROL ELECT.	POWER MAGNETICS	POWER CAPACITORS	POWER SEMI-COND	SENSORS (MAGNETIC)	MISC.	
A1 Module Input Power	A1A1 DC Input Filter	--	3	20	--	1	7	31
	A1A2 28V Converter-Power Stage	--	10	36	17	2	28	93
	A1A3 28V Converter-Control	26	--	--	--	--	--	26
	A1A4 TLM Oscillator	22	1	--	--	--	--	23
	A1 Module Subtotal	48	14	56	17	3	35	173
A2 Module Command Interface	A2A1 Digital Interface	49	--	--	--	--	--	49
	A2A2 Digital Interface	45	--	--	--	--	--	45
	A2A3 Digital Interface	23	--	--	--	--	--	23
	A2A4 Digital Interface	39	--	--	--	--	--	39
	A2A5 PPU Commands	40	--	--	--	--	--	40
	A2A6 PPU Commands	38	--	--	--	--	--	38
	A2A7 PPU Commands	38	--	--	--	--	--	38
	A2A8 PPU Control and Protection	63	--	--	--	--	--	63
	A2A9 PPU Control and Protection	79	--	--	--	--	--	79
	A2A10 PPU Control and Protection	82	--	--	--	--	--	82
	A2A11 PPU Control and Protection	94	--	--	--	--	--	94
	A2A12 PPU Control and Protection	110	--	--	--	--	--	110
	A2A13 Telemetry	25	--	--	--	--	--	25
	A2 Module Subtotal	725	--	--	--	--	--	725
A3 Module Beam Supply	A3A1 Power Stage-Baseplate	--	3	16	27	11	23	80
	A3A2 Accelerator Regulator	82	--	2	10	--	1	95
	A3A3 SCR Firing	88	2	--	4	--	--	94
	A3A4 Control Logic	131	--	--	--	--	--	131
	A3A5 Screen Regulator	139	--	--	--	--	--	139
	A3A6 Telemetry	47	--	--	--	--	--	47
	A3 Module Subtotal	487	5	18	41	11	24	586
A4 Module Discharge Supply	A4A1 Power Stage-Baseplate	--	5	6	6	5	7	29
	A4A2 High Voltage Assembly	--	--	5	11	6	4	26
	A4A3 SCR Firing	88	2	--	4	--	--	94
	A4A4 Control Logic	131	--	--	--	--	--	131
	A4A5 Discharge Regulator	147	--	--	--	--	--	147
	A4A6 Telemetry	25	--	--	--	--	--	25
	A4 Module Subtotal	391	7	11	21	11	11	452
A5 Module Multiple Inverter	A5A1 Power Stage-Baseplate	--	1	4	4	8	9	26
	A5A2 Transistor Drive Network	95	--	2	4	--	--	101
	A5A3 Control Logic	124	--	--	--	--	--	124
	A5A4 Multiple Inverter Regulator	82	--	--	--	--	--	82
	A5A5 Ramp Generator	24	3	--	--	--	--	27
	A5 Module Subtotal	325	4	6	8	8	9	360
A6 Module High Voltage Outputs	A6	--	--	--	--	--	7	7
	A6A1 V3 Output	--	1	1	6	4	2	14
	A6A2 V4 Output	--	1	1	8	4	2	16
	A6A2A Relay Driver	--	1	1	7	--	2	11
	A6A3 V8 Output	--	2	3	20	4	5	34
	A6A4 V12 Output	--	1	2	6	3	2	14
	A6A5 V3 Regulator	96	--	--	--	--	--	96
	A6A6 V4 Regulator	99	--	--	--	--	--	99
	A6A7 V8 Regulator	98	--	--	--	--	--	98
	A6A8 V12 Regulator	93	--	--	--	--	--	93
	A6A9 Telemetry	38	--	--	--	--	--	38
	A6A10 Reference	68	--	--	--	--	--	68
	A6 Module Subtotal	512	6	8	47	15	20	608
A7 Module Low Voltage Outputs	A7	--	--	--	--	--	9	9
	A7A1 V1 Output	--	1	1	7	3	2	14
	A7A2 V2 Output	--	1	1	7	3	2	14
	A7A3 V6 Output	--	1	1	7	3	2	14
	A7A4 V5 Output	--	1	1	6	4	2	14
	A7A5 V7 Output	--	3	3	21	6	6	39
	A7A6 V1 Regulator	123	--	--	--	--	--	123
	A7A7 V2 Regulator	123	--	--	--	--	--	123
	A7A8 V6 Regulator	123	--	--	--	--	--	123
	A7A9 V5 Regulator	96	--	--	--	--	--	96
	A7A10 V7 Regulator	98	--	--	--	--	--	98
	A7A11 Telemetry	50	--	--	--	--	--	50
	A7A12 Reference	100	--	--	--	--	--	100
	A7A13 Reference	104	--	--	--	--	--	104
	A7A14 Reference	109	--	--	--	--	--	109
	A7A15 Reference	64	--	--	--	--	--	64
	A7 Module Subtotal	990	7	7	48	19	23	1094
Total EP/PPU		3478	43	106	182	67	122	3998

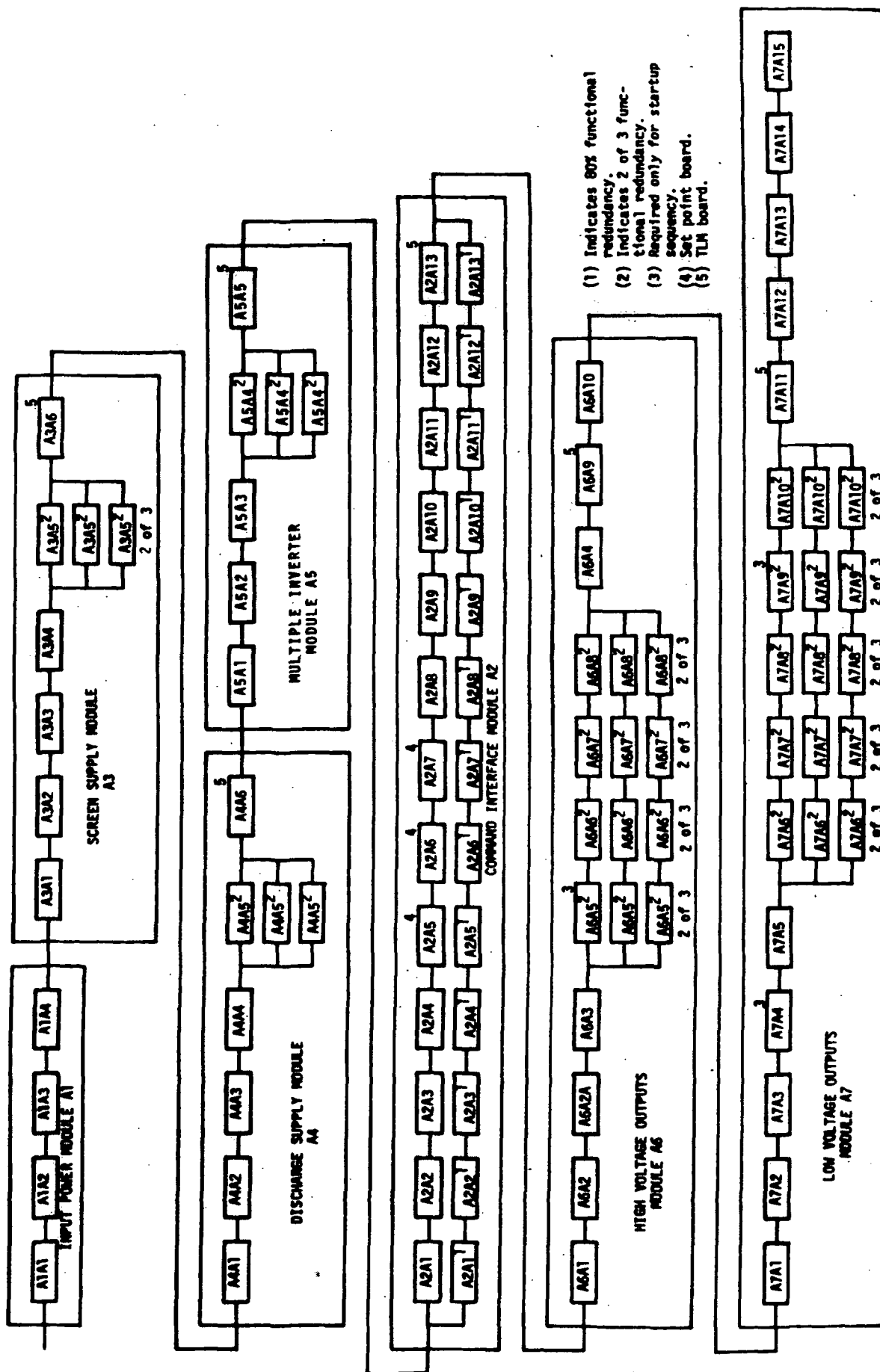


FIGURE 3-21 PPU RELIABILITY BLOCK DIAGRAM

Table 3-IV shows the reliability estimate for each module sub-assembly at two different component temperatures and with different levels of component reliability. In order to maximize the reliability, it is necessary that both component operating temperatures be minimized and that screened components be used throughout.

Table 3-V presents the reliability estimate for each module and for the total unit. The following observations can be reached from the analysis of Table 3-V:

- (1) The A2 module accounts for 33% of the total failure rate.
- (2) The low voltage outputs (A5, A6 & A7) account for 35% of the total failure rate.

Redundancy techniques would greatly improve the reliability of the A2 module. Reliability can also be improved by optimizing or simplifying the design of the low voltage outputs and by the redesign of the control electronics using improved integrated circuit components microminiaturized standard control modules and by the minimization of command requirements.

TABLE 3-IV PPU BOARD RELIABILITY SUMMARY

MODULE/ BOARD		FAILURE RATE X 10 ⁻⁹ FAILURES/HOUR				MODULE/ BOARD		FAILURE RATE X 10 ⁻⁹ FAILURES/HOUR			
		70°C AMBIENT		80°C AMBIENT				70°C AMBIENT		80°C AMBIENT	
		HIGH Q	LOWER Q	HIGH Q	LOWER Q			HIGH Q	LOWER Q	HIGH Q	LOWER Q
A1	A1A2	26.30	49.40	32.45	65.23	A5	A5A1	50.05	101.41	58.64	118.64
	A1A3	120.27	247.45	177.61	364.84		A5A2	70.11	142.94	87.55	178.45
	A1A4	59.63	121.41	98.03	198.67		A5A3	258.88	524.35	719.54	1448.57
	A1A5	37.75	77.74	61.18	124.47		A5A4	71.66	141.21	110.62	222.63
	SUBTOTAL	243.95	496.20	369.27	753.21		A5A5	138.63	278.43	239.99	481.40
							SUBTOTAL	589.33	1188.34	1216.34	2449.69
A2	A2A1	200.56	402.85	270.59	545.19	A6	A6A1	32.33	65.97	39.87	82.06
	A2A2	164.14	329.29	234.35	470.03		A6A2	27.57	55.72	32.38	65.64
	A2A3	163.47	327.22	332.43	465.22		A6A2A	22.08	44.80	29.40	60.05
	A2A4	192.67	386.68	286.70	575.01		A6A3	36.78	75.20	43.76	90.23
	A2A5 ¹						A6A4	20.12	41.21	23.79	49.11
	A2A6 ¹						A6A5	19.15	29.71	23.45	48.31
	A2A7 ¹						A6A6	19.36	30.16	23.58	48.65
	A2A8	362.07	726.56	659.59	1321.99		A6A7	19.36	30.16	23.58	48.65
	A2A9	213.71	428.33	328.67	658.52		A6A8	16.73	34.90	20.72	42.93
	A2A10	254.98	514.40	563.38	1091.59		A6A9 ²				
	A2A11	249.89	505.25	421.92	849.84		A6A10	247.56	502.48	442.46	893.97
	A2A12	376.55	741.70	650.53	1310.33		SUBTOTAL	462.04	910.31	702.99	1429.60
	A2A13 ²					A7	A7A1	36.84	74.46	45.23	91.87
	SUBTOTAL	2178.04	4362.28	3748.15	7287.72		A7A2	19.45	39.47	22.75	46.39
A3	A3A1	109.77	225.95	129.50	365.42		A7A3	19.45	39.47	22.75	46.39
	A3A2	243.65	491.84	434.72	874.75		A7A4	25.74	52.79	31.93	66.18
	A3A3	52.53	107.58	63.32	130.42		A7A5	47.89	98.28	71.96	150.51
	A3A4	422.87	849.78	717.53	1453.71		A7A6	29.77	61.31	35.49	73.59
	A3A5	73.25	148.74	113.46	229.46		A7A7	29.77	61.31	35.49	73.59
	A3A6 ²						A7A8	29.77	61.31	35.49	73.59
	SUBTOTAL	902.07	1823.89	1458.53	3053.76		A7A9	10.04	21.00	12.79	26.64
A4	A4A1	59.22	119.71	72.42	146.46		A7A10	10.04	21.00	12.79	26.64
	A4A2	22.59	46.77	26.79	55.64		A7A11 ²				
	A4A3	54.17	113.84	64.82	136.40		A7A12	279.97	603.52	530.32	1070.13
	A4A4	422.63	849.39	715.89	1441.01		A7A13	336.95	683.85	600.80	1211.20
	A4A5	84.80	175.62	127.21	259.01		A7A14	290.84	710.55	532.88	1075.36
	A4A6 ²						A7A15	182.58	370.04	294.66	594.74
	SUBTOTAL	643.41	1305.33	1007.13	2038.52		SUBTOTAL	1349.10	2898.36	2285.33	4626.82

1 - Set Point not Required for Mission Success.

2 - TLM not Required for Mission Success.

TABLE 3-V PPU MODULE RELIABILITY SUMMARY

Module	λ -Failure Rate x 10^{-9}		Failures/Hr & MTBF (Hrs)	
	70°C Ambient		80°C Ambient	
	High Q	Lower Q	High Q	Lower Q
A1 λ MTBF	244 4.10×10^6	496 2.01×10^6	369 2.71×10^6	753 1.33×10^6
A2 λ^1 MTBF ¹ λ^2 MTBF ²	2178 4.59×10^5 436 2.29×10^6	4362 2.92×10^5 872 1.14×10^6	3748 2.67×10^5 750 1.33×10^6	7288 1.37×10^5 1458 6.86×10^5
A3 λ MTBF	902 1.11×10^6	1824 5.48×10^5	1459 6.69×10^5	3054 3.27×10^5
A4 λ MTBF	643 1.56×10^6	1305 7.66×10^5	1007 9.93×10^5	2039 4.90×10^5
A5 λ MTBF	589 1.70×10^6	1188 8.42×10^5	1216 8.82×10^5	2450 4.08×10^5
A6 λ MTBF	462 2.16×10^6	910 1.10×10^6	703 1.42×10^6	1430 6.99×10^5
A7 λ MTBF	1349 7.14×10^5	2898 3.45×10^5	2285 4.38×10^5	4627 2.16×10^5
Totals	6367 ¹ 1.56×10^5 ¹ 4625 ² 2.1×10^5 ²	12983 ¹ 7.7×10^4 ¹ 9493 ² 1.05×10^5 ²	10787 ¹ 9.2×10^4 ¹ 7789 ² 1.28×10^5 ²	21641 ¹ 4.6×10^4 ¹ 15811 6.32×10^4
Mission ³ Reliability For 15,000Hr Mission	.9191 ¹ .9342 ²	.8251 ¹ .8695 ²	.8519 ¹ .8912 ²	.7252 ¹ .7915 ²

1 - Non Redundant A2 Module.

2 - 80% Redundant A2 Module

3 - Heater Power Modules A6A1, A6A5, A7A4 and A7A9 on only During Startup.

4.0 ELECTRICAL PROTOTYPE POWER PROCESSOR TEST RESULTS

Test plans were generated for the power processor unit. The tests performed on the EP/PPU included:

- (a) Load bank tests, where the power processor was loaded with nominal and light loading on the 12 separate outputs, and regulation, input ripple and efficiency was measured over the 200Vdc to 400Vdc input voltage range.
- (b) Ion engine integration tests, where the power processor started up a 30cm mercury ion engine and demonstrated operation in the range of 0.5 to 2.0A beam current.
- (c) Thermal vacuum tests, where the power processor demonstrated cold temperature starting capability at -10°C and steady-state operation at 0°C and at 20°C so that thermal mapping of component temperatures could be performed.
- (d) Electromagnetic Interference Tests, where conducted interference tests were performed with the ion engine and both radiated and conducted interference tests were performed with the load bank simulator in a screen room.

The following section presents a summary of the test data and analyses of the test results.

4.1 LOAD BANK TESTS

Tests were conducted to verify the electrical design and performance of the EP/PPU, and to provide test data concerning important performance parameters. A resistive load bank was used to simulate the ion engine loads for all of the tests.

4.1.1 Line/Load Regulation and Ripple Test

Tests were conducted to verify performance of the EP/PPU for variations in input line voltage and output load changes. Telemetry data were also recorded. Table 4-I is a summary of the input ripple and efficiencies for several operating conditions. Figure 4-1 is a plot of input ripple for the above operating conditions. Input ripple varied between 0.07% at JB = 2A, $V_{in} = 200V$ to 1.08% at JB = 0.5A, $V_{in} = 400V$. Figure 4-2 is an efficiency plot of the EP/PPU for the same operating conditions. The efficiency varied between 76% at JB = 0.5A to 87% at JB = 2.0A.

Tables 4-II through 4-VI, and tables C-I through C-XX in the Appendix, document the detail data for the EP/PPU load bank tests. Startup power data is presented in Table 4-II. Maximum load data is presented in Table 4-III. Tables C-I through C-IX lists the steady state data for JB = 0.5A to JB = 2.0A.

Tables C-X through C-XX documents the efficiency data for the beam, discharge and multiple inverters separately. The efficiency numbers represent power stage efficiencies only and do not include the losses associated with the inverter control logic or regulators. Table C-XX lists the summary of EP/PPU data.

Tables 4-IV and 4-V document the EP/PPU output regulation, ripple and telemetry for several different loading conditions and line conditions.

Table 4-VI lists output regulation as a function of heat pipe simulator temperature and input line variations.

Since all outputs have a variable set point output voltage or current, the voltage and current regulations in tables 4-V and 4-VI were calculated with reference to the maximum specified voltage or respectively current of each output, as given in table 4-IV.

TABLE 4-1 EP/PPU LOAD BANK TESTS
SUMMARY OF INPUT RIPPLE AND EFFICIENCY

Operating Conditions		Amps	Input Ripple mA p-p	Ripple %	Pin Watts	Pout Watts	Eff %
JB	Vin						
0.5A	200	4.605	12	0.26%	1016.042	778.083	76.58%
	300	3.093	20	0.65%	1020.841	778.046	76.22%
	400	2.320	25	1.08%	1019.181	783.027	76.83%
1.0A	200	7.861	15	0.19%	1672.800	1398.342	83.59%
	300	5.297	24	0.45%	1684.251	1398.091	83.01%
	400	3.981	32	0.80%	1685.777	1400.311	83.07%
2.0A	200	14.752	10	0.07%	3128.517	2726.891	87.16%
	300	10.046	22	0.22%	3116.735	2722.831	87.36%
	400	7.602	30	0.39%	3140.064	2722.517	86.70%

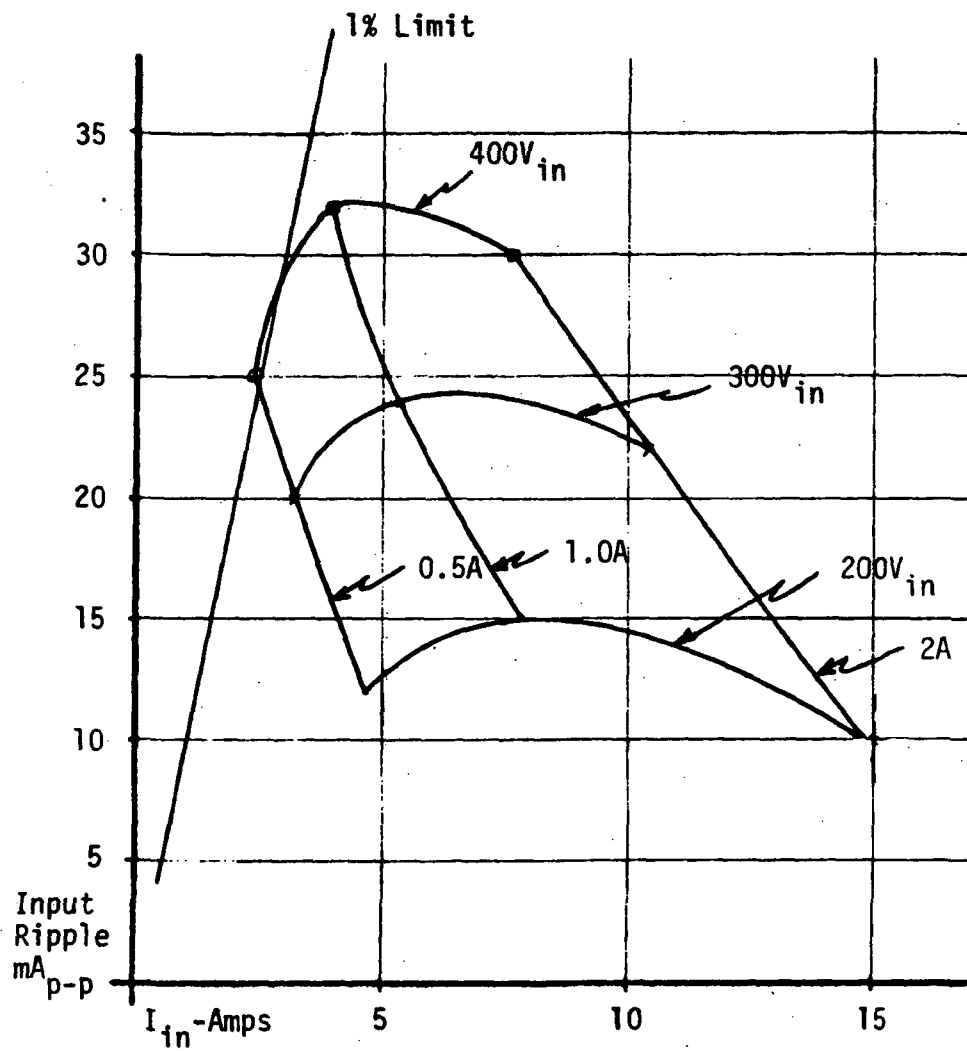
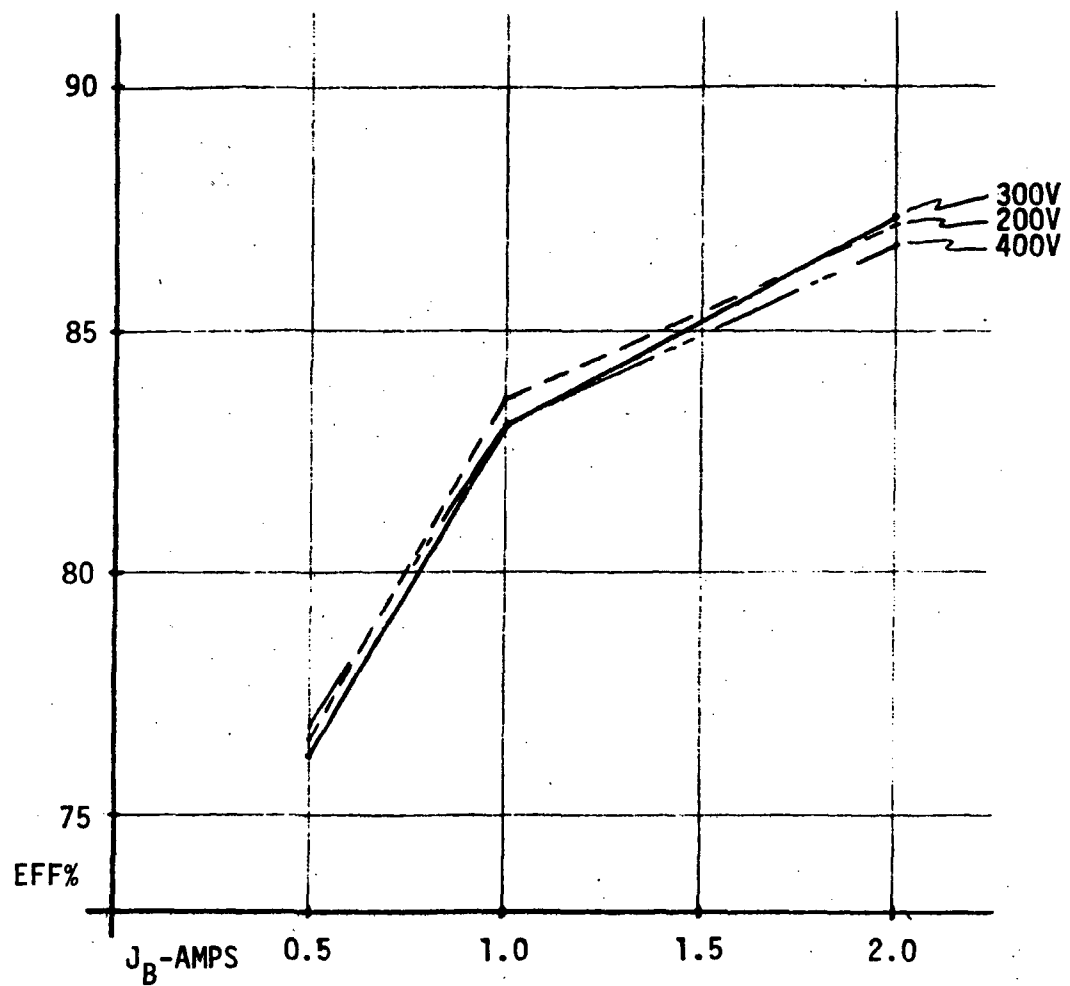


FIGURE 4-1EP/PPU INPUT RIPPLE-LOAD BANK TESTS



Note: The efficiency at 1.5A is probably better than shown. Data reflects test result at the three specified operating conditions of 0.5, 1.0 and 2A beam current.

FIGURE 4-2 EP/PPU EFFICIENCY-LOAD BANK TESTS

TABLE 4-II EP/PPU LOAD BANK TESTS

JB = Startup Power

Vin = 300V

POWER SUPPLY	V	I	POWER
V1	--	--	--
V2	8.9820	1.8716	16.811
V3	19.695	4.4174	87.001
V4	--	--	--
V5	20.159	4.4100	88.901
V6	8.8778	1.9434	17.253
V7	24.263	1.1965	29.031
V8	20.345	1.0100	20.548
V9	38.302	4.0657	155.724
V10	--	--	--
V11	--	--	--
V12	3.9926	4.8229	19.256
TOTAL OUTPUT POWER			434.525
Input			
<u>Ripple</u> (mA p-p)			
200 - 400V			
28v			
<u>Power</u>			
200 - 400V	300.40	1.8113	544.130
28v	28.226	3.0193	85.223
TOTAL INPUT POWER			629.353
EFFICIENCY			69.04%

TABLE 4-III EP/PPU LOAD BANK TESTS

JB = Max Load

V_{in} = 300VV_{SCR} = 1100V

POWER SUPPLY	V	I	POWER
V1	11.09	1.001	11.10
V2	7.49	2.011	15.06
V3	14.43	4.441	64.08
V4	7.58	2.512	19.04
V5	14.83	4.425	65.62
V6	7.41	1.998	14.80
V7	20.97	3.022	63.37
V8	20.68	.500	10.34
V9	40.49	11.951	483.89
V10	299.60	.0039	1.17
V11	1099.77	1.966	2162.15
V12	2.615	2.464	6.44
TOTAL OUTPUT POWER			2917.06
Input			
<u>Ripple</u> (mA p-p)			
200 - 400V			
28v			
<u>Power</u>			
200 - 400V	300.58	10.780	3240.25
28v	27.398	3.831	104.96
TOTAL INPUT POWER			3345.21
EFFICIENCY			87.20%

TABLE 4-IV

LINE AND LOAD REGULATION; RIPPLE AND TELEMETRY DATA
MAXIMUM VOLTAGE AND CURRENT RATINGS

POWER SUPPLY	LOADING		INPUT Volts	OUTPUT		Regulation Type	a%	Ripple		Telemetry	
	V Volts	I Amps		V Volts	I Amps			AC p-p	%	V	I
V1 Main Vaporizer	0	2	200	.977	2.001	I	0.27	160mA	--	--	4.841
			300	.976	1.998			200	--	--	4.880
			400	.980	2.000			250	--	--	4.880
	7	2	200	7.070	1.996			90	4.5	--	4.841
			300	7.057	1.992			100	5	--	4.880
			400	7.065	1.996			140	7	--	4.880
	14	2	200	12.119	1.993			60	3	--	4.841
			300	12.089	1.990			70	3.5	--	4.880
			400	12.130	1.993			90	4.5	--	4.880
V2 Cathode Vaporizer	0	2	200	.516	2.007	I	0.27	120mA	--	--	4.841
			300	.513	2.005			160	--	--	4.880
			400	.507	2.004			260	--	--	4.880
	7	2	200	4.938	2.001			100	5	--	4.841
			300	4.934	2.000			100	5	--	4.880
			400	4.934	1.999			150	7.5	--	4.880
	10	2	200	9.326	2.000			80	4	--	4.841
			300	9.279	1.996			80	4	--	4.880
			400	9.243	1.996			105	5.2	--	4.880
V3 Cathode Heater	0	4.4	200	.783	4.402	I	0.25	90mA	--	0.358	2.144
			300	.793	4.409			140	--	0.357	2.143
			400	.793	4.415			230	--	0.358	2.143
	10	4.4	200	10.620	4.397			50	1.1	2.657	2.144
			300	10.664	4.407			75	1.7	2.696	2.144
			400	10.648	4.413			130	2.9	2.657	2.182
	20	4.4	200	19.173	4.393			48	1.1	4.722	2.144
			300	19.123	4.402			60	1.4	4.682	2.143
			400	19.017	4.409			100	2.3	4.721	2.144
V4 Isolator Heater	10	0	200	10.118	0	V	1.98	--	--	--	0.040
			300	10.124	0			--	--	--	0.040
			400	10.120	0			--	--	--	0.040
	10	1.25	200	10.151	1.162			--	--	--	0.595
			300	10.166	1.163			--	--	--	0.595
			400	10.101	1.159			--	--	--	0.595
	10	2.5	200	9.769	2.499			--	--	--	1.271
			300	9.849	2.512			--	--	--	1.310
			400	9.863	2.517			--	--	--	1.271
V5 Neutralizer Heater	0	4.4	200	1.654	4.388	I	0.35	240mA	--	0.595	2.144
			300	1.658	4.402			200	--	0.595	2.143
			400	1.652	4.392			640	--	0.595	2.144
	10	4.4	200	9.964	4.383			130	2.9	2.538	2.143
			300	9.990	4.399			140	3.2	2.577	2.143
			400	10.019	4.407			260	5.9	2.538	2.144
	20	4.4	200	19.378	4.376			190	4.3	4.801	2.144
			300	19.419	4.393			120	2.7	4.761	2.143
			400	19.429	4.404			220	5	4.761	2.144
V6 Neutralizer Vaporizer	0	2	200	1.021	1.997	I	0.20	140mA	--	--	4.880
			300	1.021	1.996			240	--	--	4.880
			400	1.002	1.999			360	--	--	4.920
	5	2	200	5.127	1.994			90	4.5	--	4.880
			300	5.122	1.992			130	6.5	--	4.880
			400	5.131	1.996			190	9.5	--	4.880
	10	2	200	9.190	1.992			80	4	--	4.880
			300	9.173	1.991			100	5	--	4.881
			400	9.172	1.994			120	6	--	4.920

TABLE 4-IV (Cont'd)
LINE AND LOAD REGULATION; RIPPLE AND TELEMETRY DATA
MAXIMUM VOLTAGE AND CURRENT RATINGS

POWER SUPPLY	LOADING		INPUT VOLTS	OUTPUT							
	V Volts	I Amps		V Volts	I Amps	Regulation		Ripple		Telemetry	
						Type	±%	AC p-p	%	V	I
V7 Neutralizer Keeper	0	3	200	1.595	3.012	I	0.83	16mA	--	0.516	3.649
			300	1.599	3.014			16	--	0.516	3.688
			400	1.602	3.017			16	--	0.517	3.689
	12.5	3	200	12.649	3.006			10	.33	1.430	3.649
			300	12.684	3.008			12	.4	1.469	3.649
			400	12.768	3.012			16	.53	1.429	3.688
	25	3	200	24.919	2.995			16	.53	2.500	3.649
			300	24.770	2.981			16	.53	2.501	3.649
			400	24.599	2.967			16	.53	2.538	3.609
V8 Cathode Keeper	0	1	200	.890	1.021	I	0.50	180mA	--	0.319	3.848
			300	.882	1.019			260	--	0.318	3.848
			400	.883	1.019			600	--	0.319	3.888
	12.5	1	200	13.047	1.016			40	4	1.509	3.848
			300	13.026	1.015			48	4.8	1.469	3.888
			400	13.029	1.014			72	7.2	1.509	3.888
	25	1	200	23.657	1.012			24	2.4	2.577	3.848
			300	23.629	1.012			28	2.8	2.538	3.848
			400	23.639	1.011			40	4	2.577	3.888
V9 Discharge	0	14	200	6.468	13.547	I	1.43	36mA	--	0.517	4.166
			300	6.755	14.132			40	--	0.516	4.245
			400	7.217	15.097			36	--	0.556	4.721
	25	14	200	25.309	14.074			64	.46	2.421	4.245
			300	25.285	14.057			50	.36	2.382	4.444
			400	25.789	14.331			59	.42	2.460	4.444
	50	14	200	45.520	13.930			64	.46	4.444	4.206
			300	45.620	13.942			52	.37	4.524	4.364
			400	45.869	14.008			64	.46	4.404	4.483
V10 Accelerator	500	0	200	500.74	0	V	0.06	2.5V	.5	3.938	0.197
			300	500.80	0			2.5	.5	3.978	0.198
			400	500.83	0			2.6	.52	3.938	0.197
	500	0.01	200	500.41	.010			2.5	.5	3.968	0.280
			300	500.45	.010			2.5	.5	3.966	0.278
			400	500.48	.010			2.6	.52	3.999	0.278
	500	0.02	200	500.23	.020			2.5	.5	3.978	0.355
			300	500.27	.020			2.5	.5	3.965	0.355
			400	500.33	.020			2.5	.5	3.965	0.358
V11 Screen	1100	0	200	1100.54	0	V	0.09	31V	2.82	--	0.278
			300	1100.52	0			30	2.73	--	0.278
			400	1099.95	0			34	3.09	--	0.278
	1100	1	200	1101.59	1.007			9.5	.86	--	2.025
			300	1101.64	1.007			15	1.36	--	2.025
			400	1101.24	1.007			24	2.18	--	1.985
	1100	2	200	1100.15	1.990			6	.54	--	3.968
			300	1099.94	1.996			10.5	.95	--	3.967
			400	1099.54	1.992			15	1.36	--	3.968
V12 Magnetic Baffle	0	5	200	1.874	5.076	I	0.17	80mA	--	--	3.927
			300	1.854	5.069			70	--	--	3.927
			400	1.830	5.066			100	--	--	3.927
	2	5	200	2.207	5.074			70	1.4	--	3.927
			300	2.200	5.062			50	1	--	3.927
			400	2.210	5.059			100	2	--	3.928
	4	5	200	3.654	5.070			60	1.2	--	3.927
			300	3.649	5.067			50	1	--	3.927
			400	3.653	5.063			80	1.6	--	3.928

TABLE 4-V
LINE AND LOAD REGULATION; RIPPLE AND TELEMETRY DATA
NOMINAL VOLTAGE AND CURRENT RATINGS

	LOADING			INPUT Volts	INPUT		OUTPUT					
	V Volts	I Amps	V Volts		I Amps	Regulation		Ripple		Telemetry		
						Type	%	AC p-p	%	V	I	
V1 Main Vaporizer	0	0.9	200	.482	1.007	I	0.27	90mA	--	--	2.381	
			300	.481	1.003			130	--	--	2.420	
			400	.485	1.007			300	--	--	2.420	
	7	0.9	200	6.701	1.002			40	2%	--	2.388	
			300	6.776	.998			60	3	--	2.380	
			400	6.775	1.003			90	4.5	--	2.420	
	14	0.9	200	13.111	.999			40	2	--	2.380	
			300	13.175	.996			40	2	--	2.420	
			400	13.146	.998			60	3%	--	2.420	
V2 Cathode Vaporizer	0	0.82	200	.287	1.079	I	0.32	80mA	--	--	2.576	
			300	.284	1.076			100	--	--	2.576	
			400	.277	1.073			200	--	--	2.577	
	5	0.82	200	5.129	1.071			50	2.5%	--	2.576	
			300	5.120	1.070			70	3.5	--	2.577	
			400	5.116	1.069			80	4	--	2.577	
	10	0.82	200	9.539	1.068			30	1.5	--	2.577	
			300	9.511	1.067			35	1.5	--	2.576	
			400	9.479	1.066			50	2.5%	--	2.576	
V3 Cathode Heater	0	2.2	200	.402	2.508	I	0.54	190mA	--	0.278	1.190	
			300	.407	2.506			240	--	0.278	1.190	
			400	.387	2.460			800	--	0.278	1.190	
	10	2.2	200	10.193	2.503			95	2.2%	2.537	1.190	
			300	10.173	2.501			130	2.9	2.577	1.190	
			400	10.152	2.501			200	4.5	2.537	1.190	
	20	2.2	200	19.700	2.499			60	1.4	4.880	1.190	
			300	19.685	2.497			80	1.8	4.880	1.190	
			400	19.577	2.489			126	2.9%	4.880	1.190	
V4 Isolator Heater	4	0	200	5.604	0	--	--	--	--	--	0.040	
			300	5.704	0			--	--	--	0.040	
			400	5.647	0			--	--	--	0.040	
	4	1.25	200	4.052	1.174			--	--	--	0.590	
			300	4.124	1.194			--	--	--	0.590	
			400	3.799	1.112			--	--	--	0.551	
	4	2.5	200	4.250	2.522			--	--	--	1.260	
			300	4.250	2.521			--	--	--	1.260	
			400	4.242	2.522			--	--	--	1.260	
V5 Neutralizer Heater	0	2.2	200	.862	2.504	I	0.18	120mA	--	0.397	1.190	
			300	.861	2.505			250	--	0.397	1.190	
			400	.858	2.502			500	--	0.397	1.190	
	10	2.2	200	9.319	2.499			100	2.3%	2.381	1.190	
			300	9.327	2.501			120	2.7	2.381	1.190	
			400	9.326	2.502			180	4.1	2.341	1.190	
	20	2.2	200	19.965	2.493			60	1.4	4.880	1.190	
			300	19.918	2.496			80	1.8	4.880	1.190	
			400	19.775	2.489			105	2.4%	4.880	1.190	
V6 Neutralizer Vaporizer	0	0.7	200	.522	1.052	I	0.25	80mA	--	--	2.538	
			300	.522	1.048			150	--	--	2.538	
			400	.527	1.051			250	--	--	2.538	
	5	0.7	200	5.134	1.048			50	2.5%	--	2.538	
			300	5.116	1.044			70	3.5	--	2.538	
			400	5.135	1.048			100	5	--	2.538	
	10	0.7	200	9.410	1.045			35	1.7	--	2.538	
			300	9.382	1.042			50	2.5	--	2.538	
			400	9.425	1.045			70	3.5%	--	2.538	

TABLE 4-V (Cont'd)
LINE AND LOAD REGULATION; RIPPLE AND TELEMETRY DATA
NOMINAL VOLTAGE AND CURRENT RATINGS

POWER SUPPLY	LOADING		INPUT VOLTS	OUTPUT							
	V Volts	I Amps		V Volts	I Amps	Regulation		Ripple		Telemetry	
						Type	±%	AC p-p	%	V	I
V7 Neutralizer Keeper	0	2	200	.951	1.807	I	0.25	6mA	--	0.437	2.143
			300	.951	1.805			10	--	0.438	2.143
			400	.953	1.806			6	--	0.437	2.143
	12.5	2	200	12.834	1.800			4	.1	1.429	2.143
			300	12.825	1.798			4	.1	1.429	2.143
			400	12.820	1.798			8	.2	1.429	2.143
	25	2	200	24.468	1.793			10	.3	2.461	2.143
			300	24.416	1.792			5	.2	2.461	2.143
			400	24.450	1.792			10	.3	2.461	2.143
V8 Cathode Keeper	0	0.5	200	.673	.510	I	0.55	90mA	--	0.278	1.865
			300	.665	.508			150	--	0.278	1.865
			400	.667	.507			200	--	0.278	1.865
	12.5	0.5	200	11.958	.505			12	1.2	1.389	1.865
			300	11.929	.504			17	1.7	1.389	1.865
			400	11.906	.503			25	2.5	1.389	1.865
	25	0.5	200	24.164	.501			9	.9	2.577	1.865
			300	24.160	.500			10	1.0	2.577	1.865
			400	24.156	.499			14	1.4	2.577	1.865
V9 Discharge	0	10.3	200	4.643	11.323	I	1.11	32mA	--	.358	3.371
			300	5.248	12.787			40	--	.398	3.967
			400	5.578	13.596			36	--	.398	4.285
	25	10.3	200	23.962	10.243			50	.36	2.342	3.133
			300	24.028	10.270			60	.43	2.342	3.014
			400	24.653	10.533			68	.48	2.421	3.173
	50	10.3	200	47.396	10.220			48	.34	4.762	3.094
			300	47.434	10.226			60	.43	4.760	3.133
			400	47.864	10.315			80	.57	4.761	3.054
V10 Accelerator	300	0	200	300.74	0	V	0.07	2V	.4	2.403	0.158
			300	300.77	0			2	.4	2.402	0.158
			400	300.78	0			2	.4	2.403	0.158
	300	0.01	200	300.27	.010			2	.4	2.401	0.236
			300	300.30	.010			2	.4	2.400	0.236
			400	300.32	.010			2.1	.4	2.401	0.236
	300	0.02	200	300.06	.020			2	.4	2.401	0.354
			300	300.09	.020			2	.4	2.401	0.354
			400	300.11	.020			2.2	.4	2.401	0.355
V11 Screen	900	0	200	900.49	0	V	0.36	10.5V	.9	--	0.080
			300	900.53	0			19	1.7	--	0.080
			400	908.41	0			38	3.4	--	0.080
	900	1	200	902.73	1.006			9	.8	--	2.063
			300	902.65	1.006			15	1.4	--	2.024
			400	902.30	1.006			24	2.2	--	2.048
	900	2	200	902.13	1.997			6.5	.6	--	3.939
			300	901.85	2.001			9.5	.9	--	3.899
			400	901.42	1.997			14	1.3	--	3.938
V12 Magnetic Baffle	0	2	200	.741	2.073	I	0.35	200mA	--	--	1.544
			300	.723	2.065			110	--	--	1.544
			400	.700	2.061			90	--	--	1.544
	2	2	200	2.148	2.050			130	2.6	--	1.544
			300	2.140	2.045			50	1	--	1.544
			400	2.147	2.043			50	1	--	1.544
	4	2	200	3.995	2.045			60	1.2	--	1.544
			300	3.981	2.040			40	.8	--	1.544
			400	3.985	2.038			40	.8	--	1.544

TABLE 4-VI OUTPUT REGULATION DUE TO TEMPERATURE - 2A BEAM CONDITION

POWER SUPPLY	Vin	-10°C*			0°C*			20°C*			REGULATION ±%
		V	I		V	I		V	I		
V1	200				6.213	1.002		6.246	1.006		I - 1.72
	300	6.214	1.002		6.234	1.071		6.244	1.006		
	400				6.235	1.071		6.260	1.008		
V2	200				3.593	1.072		4.267	1.076		I - 0.17
	300	4.174	1.069		3.951	1.071		4.262	1.075		
	400				3.945	1.071		4.259	1.075		
V6	200				3.709	1.048		3.514	1.050		I - 0.15
	300	3.660	1.049		3.727	1.049		3.512	1.050		
	400				3.711	1.052		3.524	1.054		
V7	200				15.510	1.808		15.577	1.810		I - 0.06
	300	16.165	1.807		15.513	1.808		15.582	1.810		
	400				15.514	1.809		15.568	1.811		
V8	200				5.710	.506		5.644	.509		I - 0.25
	300	5.919	.504		5.703	.506		5.644	.509		
	400				5.688	.505		5.618	.507		
V9	200				36.692	12.270		36.484	12.209		I - 0.40
	300	38.497	12.315		36.744	12.288		36.525	12.223		
	400				36.847	12.322		36.599	12.249		
V10	200				300.06	.0038		300.33	.0038		V - 0.08
	300	299.74	.004		300.11	.0038		300.38	.0038		
	400				300.24	.0038		300.52	.0038		
V11	200				1102.58	2.005		1098.90	2.004		V - 0.80
	300	1084.95	2.004		1102.35	2.005		1098.71	2.005		
	400				1102.48	2.005		1098.57	2.005		
V12	200				.914	2.029		.955	2.106		I - 0.87
	300	.938	2.087		.909	2.024		.950	2.101		
	400				.894	2.019		.935	2.096		

*Temperature of heat pipe simulator coolant.

4.1.2 Shorting and Overload Test

The EP/PPU power supplies were tested for overload capability and recovery by application of a short across the designated output given in Table 4-VII. The power supplies suffered no degradation after completion of the shorting test.

4.1.3 Transient and Recycle Test

The main advantage of the series resonant inverter is that it is a current source and does not reflect a high peak surge current back to the power source. Figure 4-3 is an oscilloscope photo of the input current during turn on of the high power beam supply.

Figure 4-4 is an oscilloscope photo of the input current upon application and release of a short on the output of the screen supply.

Figure 4-5 is an oscilloscope photo of the screen voltage, accelerator voltage, and discharge current during a simulated recycle event.

During all of these transient conditions, no large current surge was drawn from the dc power bus. No additional current regulator circuitry was needed to provide this protection feature which is inherent in the series resonant inverter design.

TABLE 4-VII SHORTING LIST FOR EP/PPU OUTPUTS

FROM		TO
1	Main vaporizer (V1)	Vaporizer return
2	Cathode vaporizer (V2)	Vaporizer return
3	Neutralizer vaporizer (V6)	Vaporizer return
4	Main and cathode isolator (V4)	Cathode common (Screen)
5	Neutralizer heater (V5)	Neutralizer common
6	Neutralizer keeper (V7)	Neutralizer common
7	Cathode heater (V3)	Cathode common
8	Cathode keeper (V8)	Cathode common
9	Discharge (Anode-V9)	Cathode common
10	Accelerator (V10)	Neutralizer common
11	Cathode common (Screen)	Neutralizer common
12	Magnetic baffle positive (V12)	Magnetic baffle negative
13	Power output common (S/C com.)	Cathode common
14	Power output common	Neutralizer keeper (V7)
15	Power output common	Cathode keeper (V8)
16	Power output common	Discharge (Anode-V9)
17	Power output common	Accelerator (V10)
18	Neutralizer common	Cathode keeper (V8)
19	Neutralizer common	Cathode keeper (V8)
20	Cathode common	Accelerator (V10)
21	Neutralizer keeper (V7)	Cathode keeper (V8)
22	Neutralizer keeper (V7)	Discharge (Anode-V9)
23	Neutralizer keeper (V7)	Accelerator (V10)
24	Cathode Keepre (V8)	Discharge (Anode-V9)
25	Cathode Keeper (V8)	Accelerator (V10)
26	Discharge (Anode-V9)	Accelerator (V10)

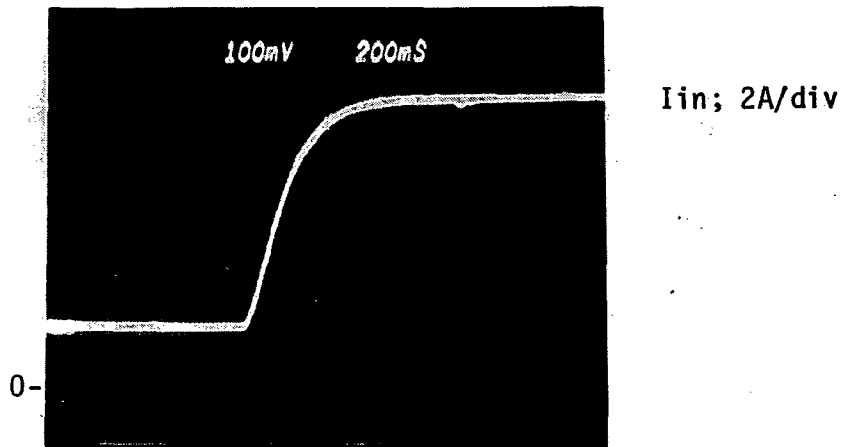


FIGURE 4-3 INPUT CURRENT, BEAM INVERTER TURN-ON

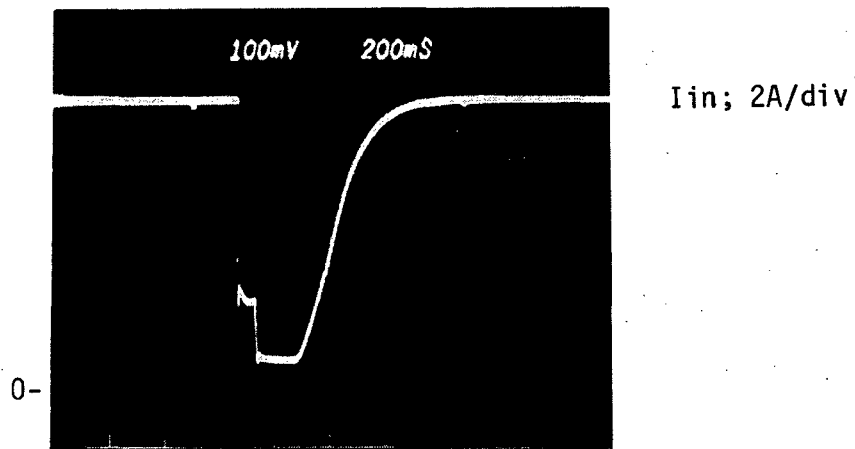
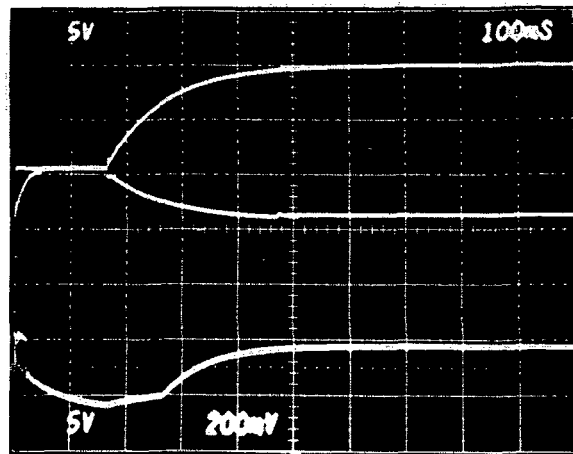


FIGURE 4-4 INPUT CURRENT, SHORT APPLIED AND RELEASED ON SCREEN OUTPUT



Screen Voltage

Accel Voltage

Discharge Current

FIGURE 4-5 ARC RECYCLE - LOAD BANK

4.2 EP/PPU ION ENGINE INTEGRATION TEST

The EP/PPU - Ion Engine integration test followed an extensive testing program of the EP/PPU using a resistive load bank to represent the thruster. Load bank testing alone cannot simulate the dynamic conditions of the ion engine as a load on the EP/PPU, therefore, it was necessary to perform the integration tests to fully evaluate the performance of the EP/PPU.

The integration testing consisted of four sections: EP/PPU functional checkout, EP/PPU steady state operational checks, an eight hour uninterrupted run, and an EMI measurement of the inputs and outputs of the EP/PPU.

4.2.1 EP/PPU Functional Checkout

The ion engine was installed in a vertical vacuum chamber and the EP/PPU and the test console was positioned alongside the chamber. After plumbing and electrical connections were completed to the ion engine, the chamber was brought to hard vacuum and the EP/PPU energized. The following functional operations were demonstrated:

- 1.) Neutralizer keeper ignition
- 2.) Neutralizer keeper-neutralizer vaporizer control loop.
- 3.) Cathode keeper ignition
- 4.) Discharge ignition
- 5.) Discharge voltage - cathode vaporizer control loop
- 6.) Magnetic baffle operation
- 7.) High voltage application to accelerator and screen
- 8.) Beam current regulation from 0.5 amps to 2.0 amps
- 9.) Recovery from internal engine arcs
- 10.) Shut down of ion engine

The time constants for the fault or arc clearing circuitry was modified to provide reliable recycles after an engine arc. Figure 4-6 shows the screen and accelerator voltage and input current during the recycle mode of operation.

Figure 4-7 shows screen and accelerator voltage and current during a recycle. Perturbations of the screen and accelerator voltages and input current are minimal during the recycle interval.

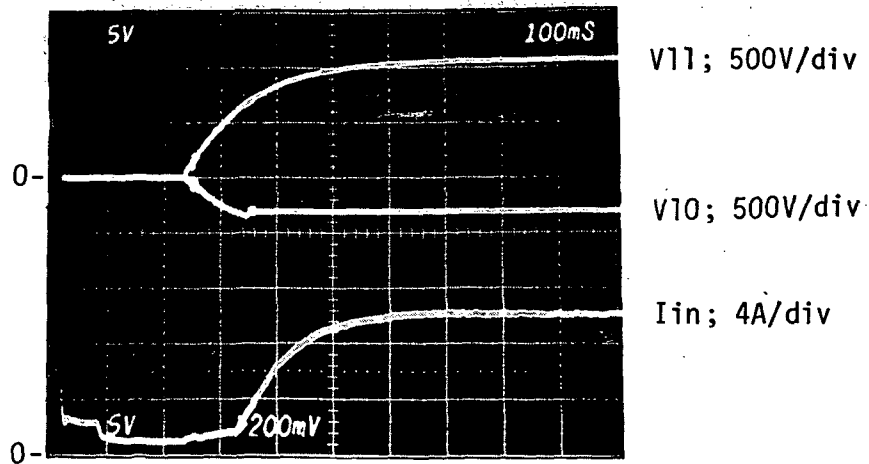


FIGURE 4-6 ARC RECYCLE 2Amp Beam; 300V Input

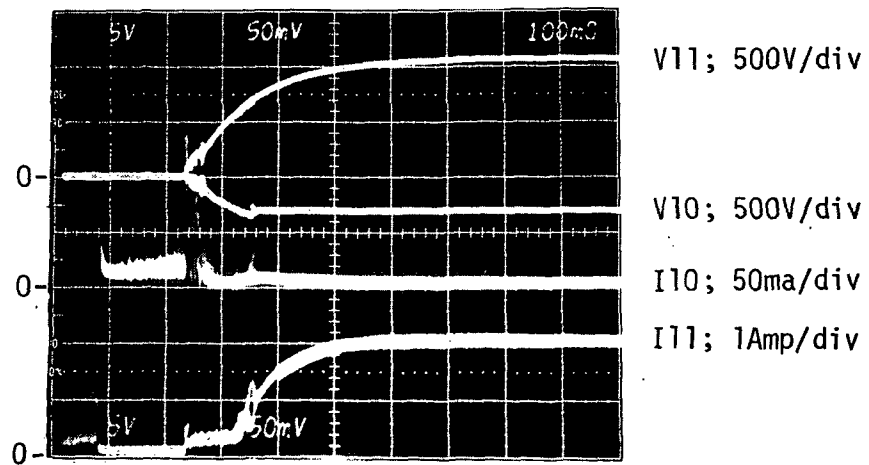


FIGURE 4-7 ARC RECYCLE 2Amp Beam; 300V Input

4.2.2 EP/PPU Ion Engine Steady State Operation

After it was determined that the EP/PPU and the ion engine was operating normally, the following tests were performed:

- 1.) Ion engine operation at 2.0 Amp beam current
- 2.) Ion engine operation at 1.0 Amp beam current
- 3.) Ion engine operation at 0.5 Amp beam current

Noise in all power lines to the ion engine and the input power line was monitored and oscilloscope photos taken of the current waveforms.

Figures 4-8 through 4-11 show the ripple on the input and output lines of the EP/PPU when operating the ion engine at a beam current of 2.0 A and input voltages of 200, 300, and 400 V.

Tables 4-VIII through 4-X show typical EP/PPU characteristics when operating an ion engine at a beam current of 2A.

Current waveform photographs were also taken at 0.5 Amp and 1.0 Amp beam currents and are given in the Appendix, Figures D-1 through D-6.

Tables D-I through D-VI in the Appendix show the EP/PPU characteristics at beam currents of 0.5 Amp and 1.0 Amp.

Overall efficiency of the EP/PPU when operating with an engine as a function of input voltage and beam current is plotted in Figure 4-12.

The EP/PPU efficiency measurements during engine integration, Tables 4-VIII through 4-X, D-1 through D-VI, and Figure 4-12 are inherently inaccurate because the engine represents a continuously varying load. An accurate efficiency measurement requires the simultaneous reading of all the input and output voltages and current whereas the above data was read and recorded sequentially.

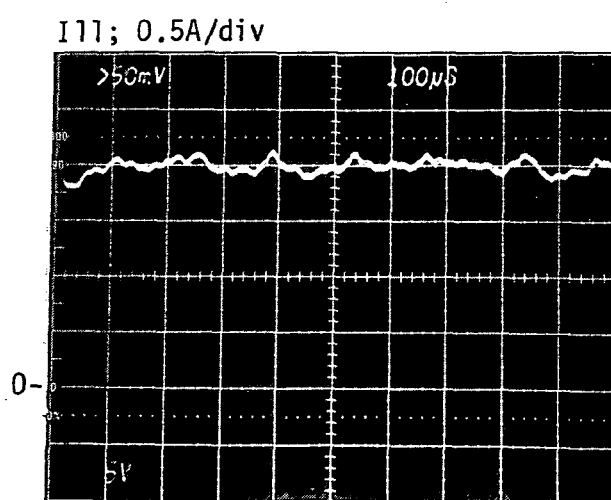
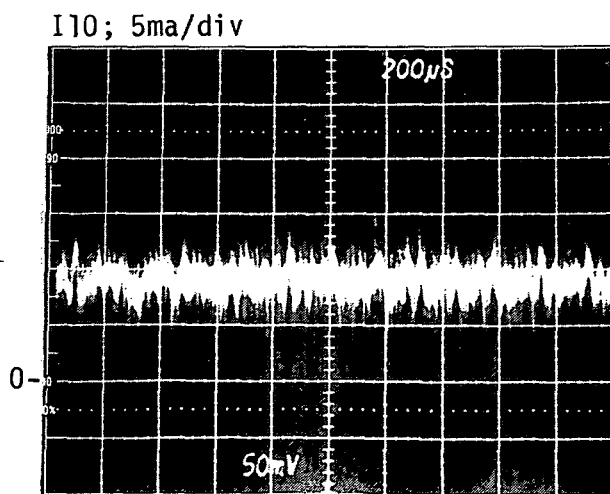
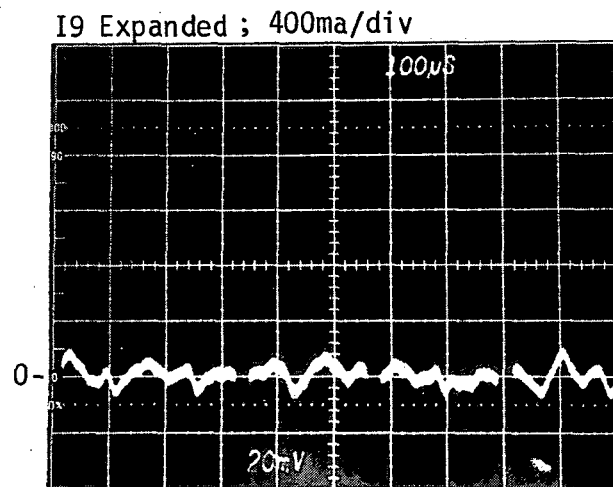
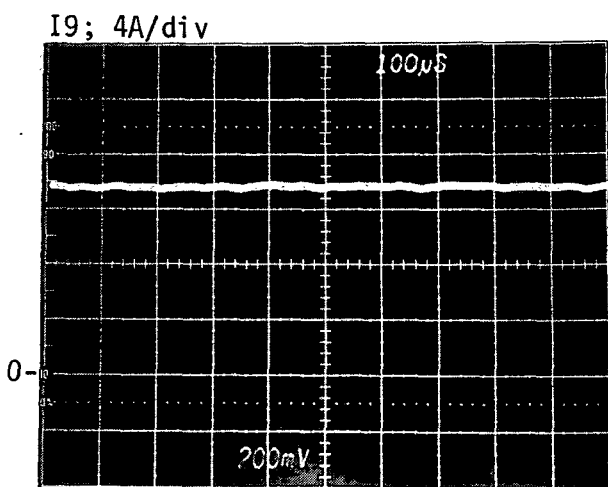
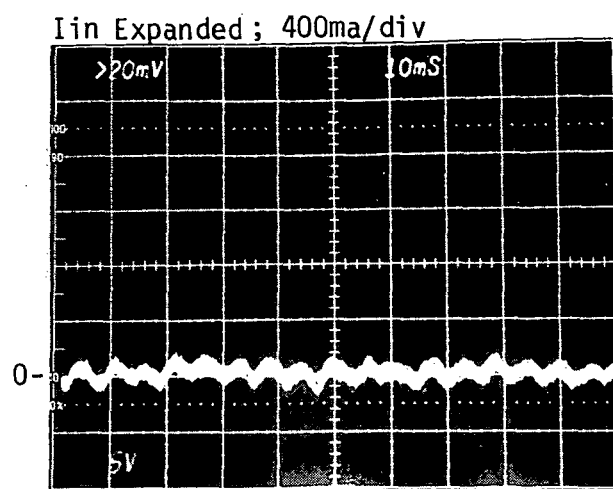
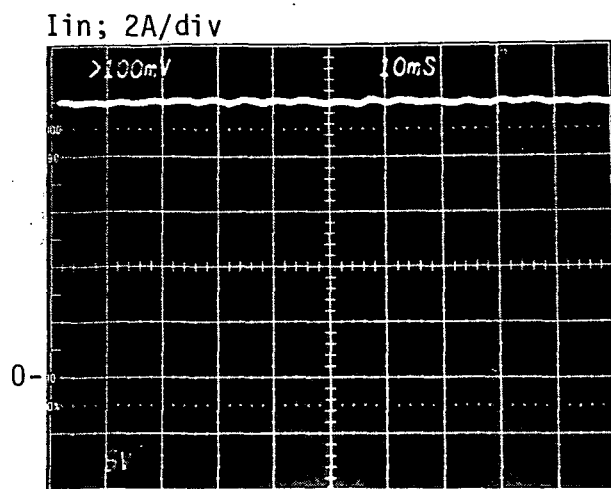


FIGURE 4-8 EP/PPU CURRENT WAVEFORMS WITH ION ENGINE 2Amp Beam; 300V Input

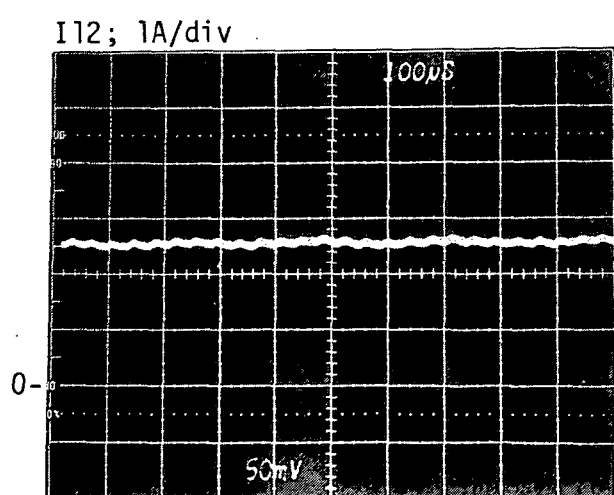
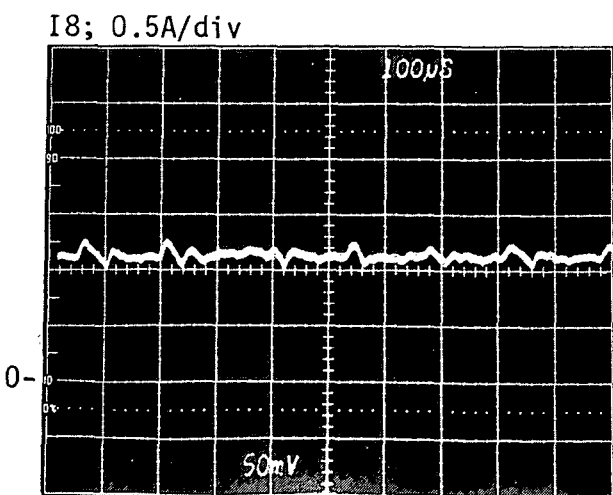
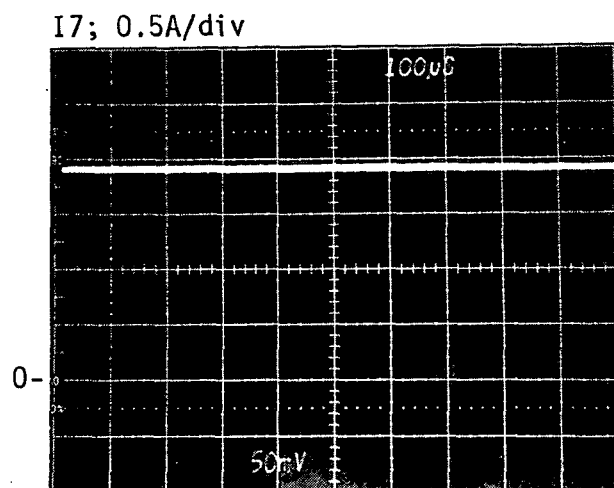
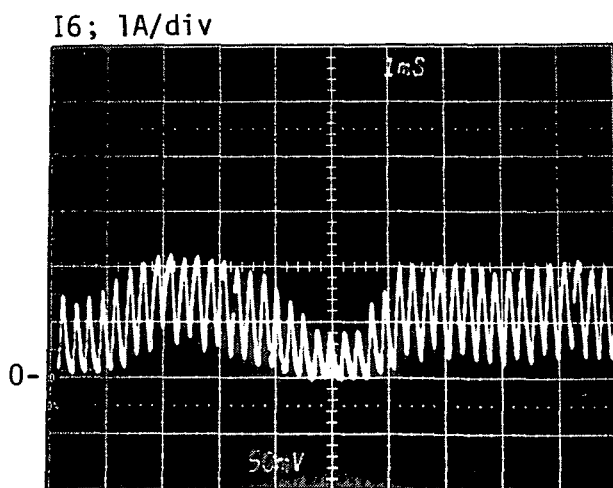
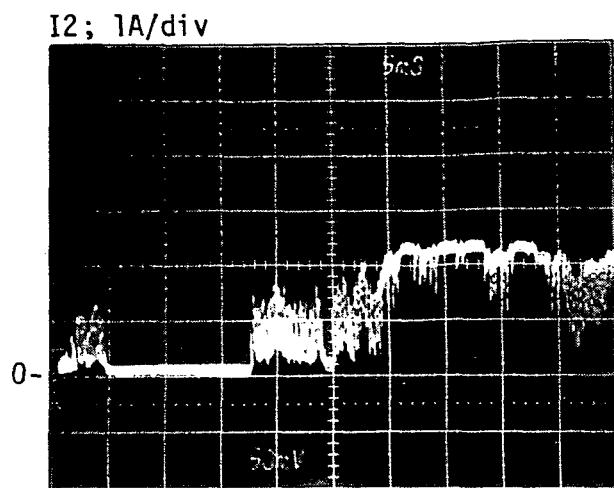
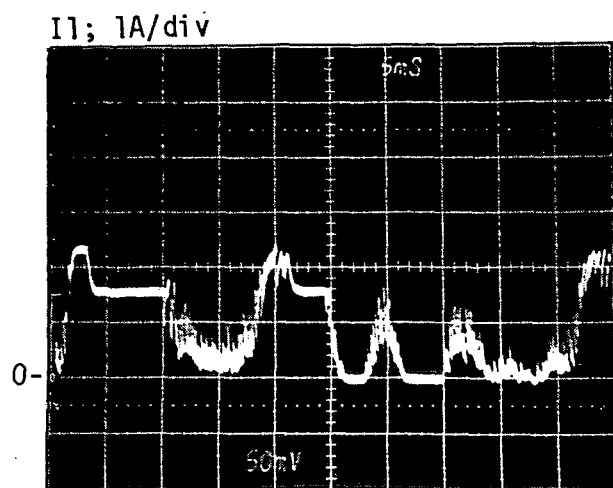


FIGURE 4-9 EP/PPU CURRENT WAVEFORMS WITH ION ENGINE 2Amp Beam; 300V Input

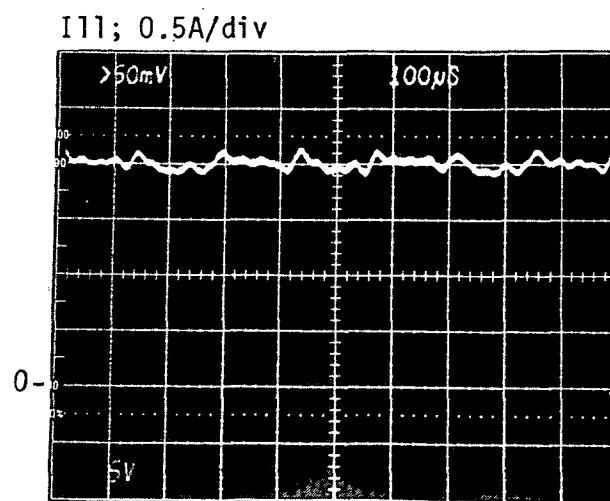
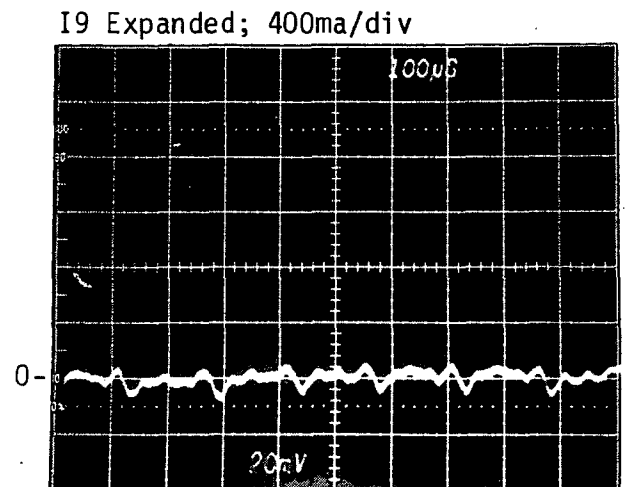
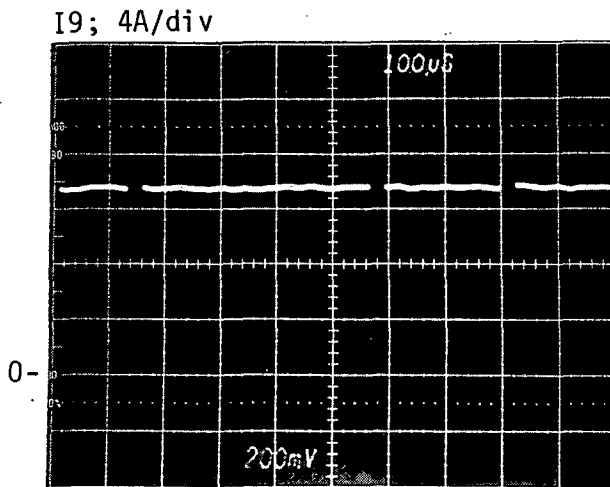
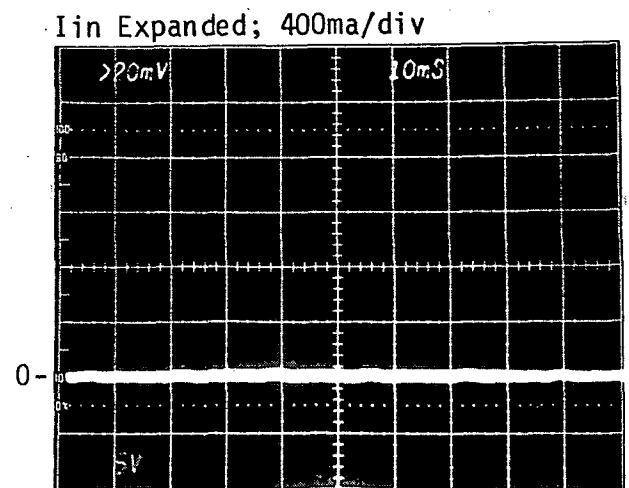
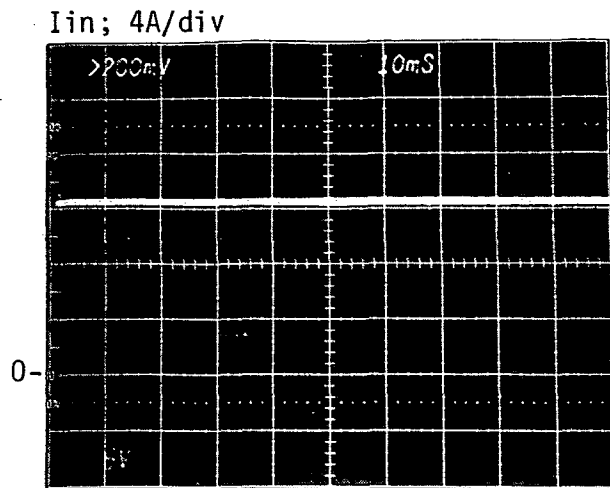


FIGURE 4-10 EP/PPU CURRENT WAVEFORMS WITH ION ENGINE 2Amp Beam; 200V Input

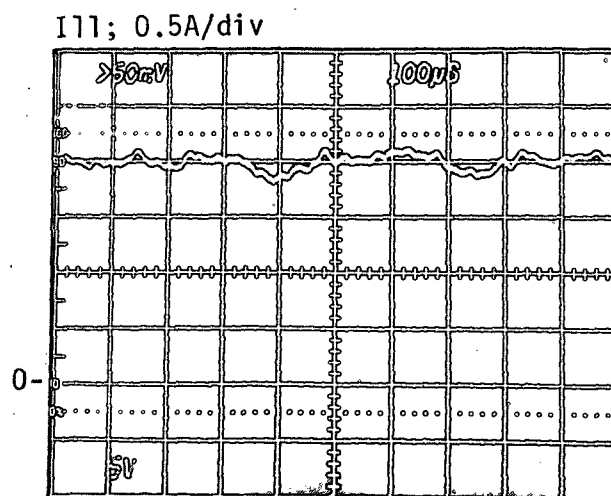
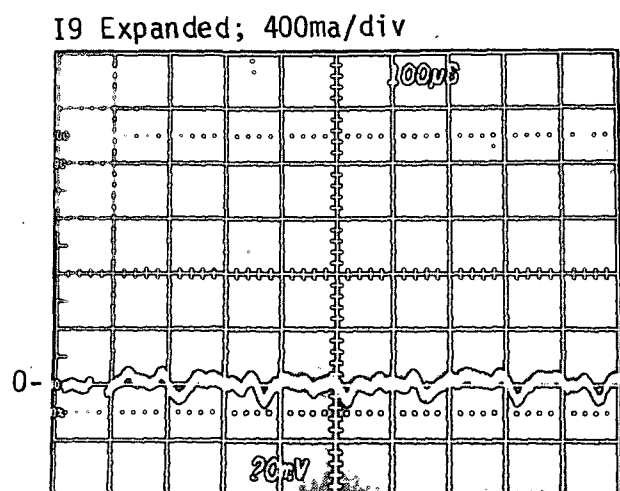
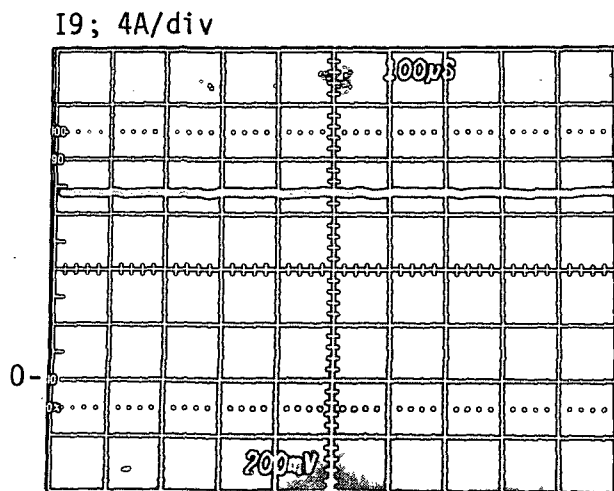
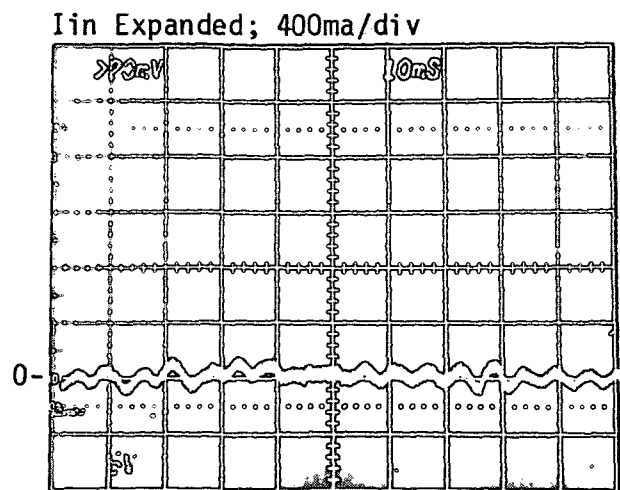
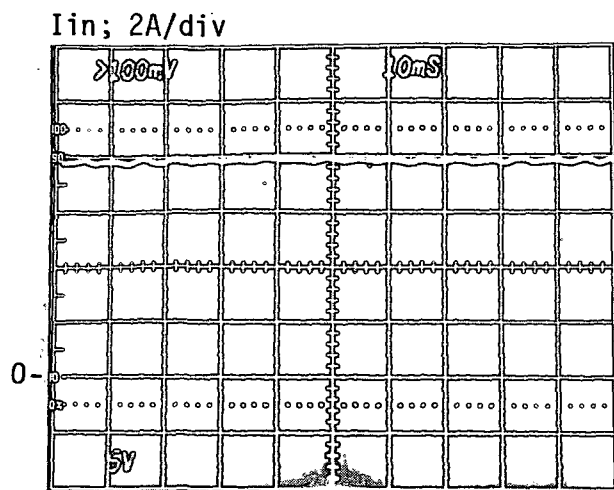


FIGURE 4-11 EP/PPU CURRENT WAVEFORMS WITH ION ENGINE 2 Amp Beam; 400V Input

TABLE 4-VIII EP/PPU ENGINE INTEGRATION TESTS

$J_B = 2A$
 $V_{in} = 200V$
 $V_{SCR} = 1100V$

POWER SUPPLY	V	I	POWER
V1	5.2	.76	3.95
V2	2.9	.8	2.32
V3	-	-	-
V4	-	-	-
V5	-	-	-
V6	2.7	.86	1.945
V7	15.09	1.80	27.16
V8	6.07	11019	6.83
V9	39.57	13.04	515.99
V10	299.64	.00713	2.14
V11	1095.10	2.005	2195.67
V12	1.36	2.40	3.26
TOTAL OUTPUT POWER			2759.64
200 - 400V	232.12	13.28	3082.55
28V	28.15	3.73	105.00
TOTAL INPUT POWER			3187.55
EFFICIENCY			86.57
VAPORIZER THERMOCOUPLE TEMPERATURE		°C	
MAIN VAPORIZER		316	
CATHODE VAPORIZER		211	
NEUTRALIZER VAPORIZER		242	
TANK PRESSURE 2.3x10 ⁻⁶ TORR			

TABLE 4-IX EP/PPU ENGINE INTEGRATION TESTS

$J_B = 2A$
 $V_{in} = 300V$
 $V_{SCR} = 1100V$

POWER SUPPLY	V	I	POWER
V1	6.4	1.01	6.46
V2	3.7	1.07	3.96
V3	-	-	-
V4	-	-	-
V5	-	-	-
V6	2.7	.86	2.32
V7	15.08	1.799	27.13
V8	6.88	1.018	7.00
V9	39.60	13.04	516.38
V10	299.58	.00784	2.35
V11	1098.0	2.008	2204.78
V12	1.32	2.39	3.15
TOTAL OUTPUT POWER			2773.53
200 - 400V	300.10	10.27	3082.03
28V	28.26	3.59	101.45
TOTAL INPUT POWER			3183.48
EFFICIENCY			87.12%
VAPORIZER THERMOCOUPLE TEMPERATURE		°C	
MAIN VAPORIZER		314	
CATHODE VAPORIZER		175	
NEUTRALIZER VAPORIZER		240	
TANK PRESSURE 2.25×10^{-6} TORR			

TABLE 4-X EP/PPU ENGINE INTEGRATION TESTS

$J_B = 2A$
 $V_{in} = 400V$
 $V_{SCR} = 1100V$

POWER SUPPLY	V	I	POWER
V1	4.5	.75	3.37
V2	3.2	.65	2.08
V3	-	-	-
V4	-	-	-
V5	-	-	-
V6	2.5	.83	2.07
V7	15.09	1.799	27.15
V8	6.73	1.018	6.85
V9	39.54	13.09	517.58
V10	299.76	.00746	2.24
V11	1097.4	2.005	2200.29
V12	1.32	2.33	3.07
TOTAL OUTPUT POWER			2764.70
200 - 400V	390.95	7.93	3100.23
28V	28.35	3.46	98.09
TOTAL INPUT POWER			3198.32
EFFICIENCY			86.44%
VAPORIZER THERMOCOUPLE TEMPERATURE		°C	
MAIN VAPORIZER		314	
CATHODE VAPORIZER		206	
NEUTRALIZER VAPORIZER		242	
TANK PRESSURE 2.42×10^{-6} TORR			

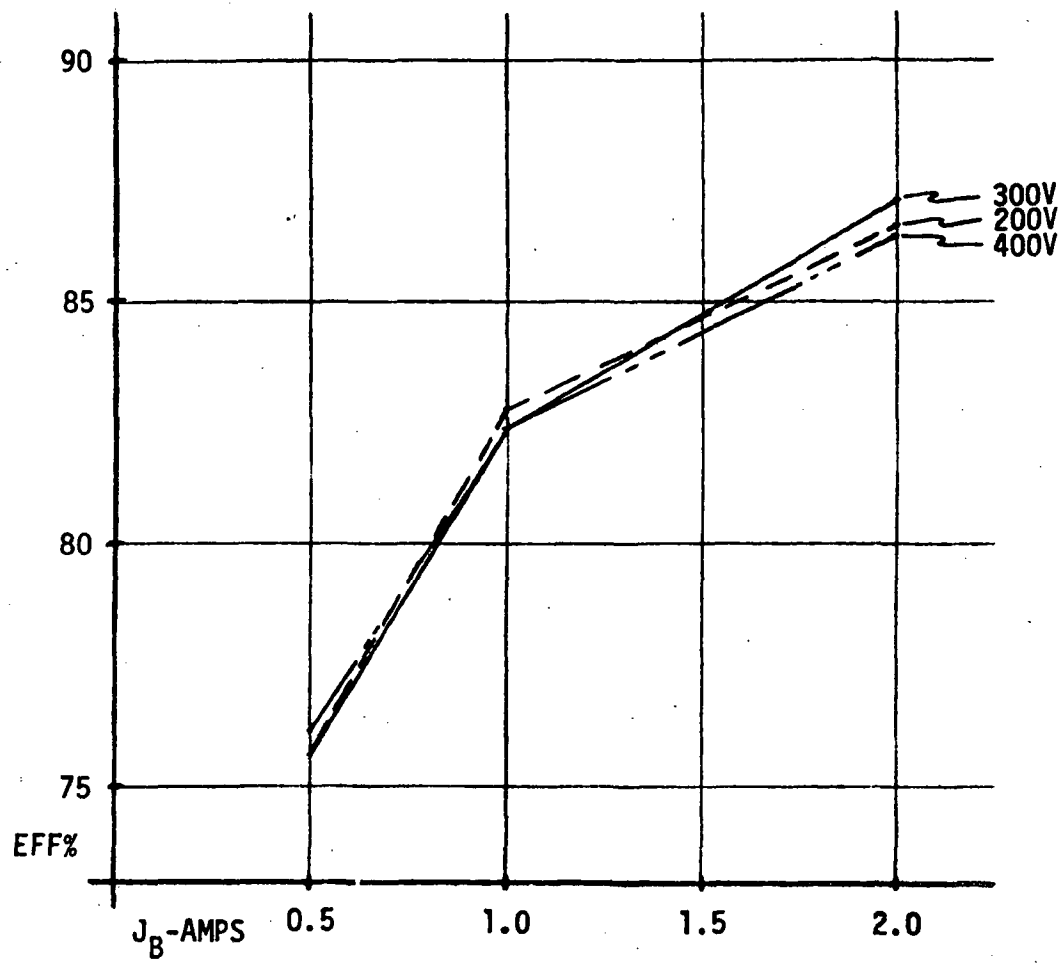


FIGURE 4-12 EP/PPU EFFICIENCY-ENGINE INTEGRATION

4.2.3 Uninterrupted EP/PPU Operation

An eight hour continuous operation of the EP/PPU - ion engine combination was run to demonstrate control loop compatibility and recycle capability of the EP/PPU. Table 4-XI lists the operating parameters of the EP/PPU during the eight hour test period. The test was conducted at a beam current of 2 amperes and input voltage of 300V.

TABLE 4-XI EP/PPU ENGINE INTEGRATION

8 Hour Test 12-15-76 Sheet 1 of 2

	Start - 0 Hour			1 Hour			2 Hours			3 Hours			4 Hours		
	V	I	Power	V	I	Power	V	I	Power	V	I	Power	V	I	Power
V1	5.8	1.0	5.80	4.1	.86	3.53	4.4	.76	3.34	5.2	.7	3.64	5.6	.65	3.64
V2	3.4	.73	2.48	2.6	.75	1.95	3.1	.62	1.92	3.2	.57	1.82	2.5	.75	1.87
V6	3.0	.83	2.49	2.9	.79	2.29	2.9	.71	2.06	2.9	.82	2.38	2.9	.81	2.35
V7	15.09	1.799	27.15	15.08	1.799	27.13	15.08	1.798	27.11	15.07	1.799	27.11	15.08	1.799	27.13
V10	299.81	7.11mA	2.13	300.00	5.65mA	1.69	300.02	5.32mA	1.60	300.03	5.12mA	1.54	300.05	4.91mA	1.47
V8	6.61	1.018	6.73	6.72	1.018	6.84	6.83	1.018	6.95	6.83	1.018	6.95	6.82	1.018	6.94
V9	39.55	13.047	516.01	39.43	13.04	514.17	39.55	13.04	515.73	39.40	13.04	513.78	39.50	13.04	515.08
ΔVI	35.85			35.87			35.83			36.01			35.80		
V11	1098.63	2.005	2202.75	1097.89	2.004	2200.17	1097.56	2.003	2198.41	1097.80	2.003	2198.89	1097.83	2.003	2198.95
V12	1.34	2.38	3.19	1.35	2.40	3.24	1.35	2.39	3.23	1.35	2.39	3.23	1.35	2.39	3.23
Σ Po			2768.73			2761.01			2760.35			2759.34			2760.66
V _{in}	300.49	10.27	3086.03	300.39	10.24	3075.99	300.38	10.23	3072.89	300.29	10.23	3071.97	300.20	10.25	3077.05
28V	28.26	3.57	100.89	28.34	3.56	100.89	28.34	3.57	101.17	28.34	3.56	100.89	28.30	3.56	100.75
Σ Pin			3186.92			3176.88			3174.06			3172.86			3177.80
Eff(%)			86.88			86.91			86.96			86.97			86.87
T _{OmV}	16.2	316°C		16.2	316°C		16.2	316°C		16.2	316°C		16.2	316°C	
CV	9.4	193		10.5	213		10.6	215		10.6	215		10.6	215	
NV	12.1	242		12.1	242		12.1	242		12.1	242		12.1	242	
Tank	3.4x10 ⁻⁶ TORR			2.65x10 ⁻⁶ TORR			2.5x10 ⁻⁶ TORR			2.4x10 ⁻⁶ TORR			2.4x10 ⁻⁶ TORR		
Arcs				2			2			3			2		

TABLE 4-XI (Continued) EP/PPU ENGINE INTEGRATION
8 Hours Test 12-15-76 Sheet 2 of 2

	5 Hours			6 Hours			7 Hours			8 Hours		
	V	I	Power	V	I	Power	V	I	Power	V	I	Power
V1	4.3	.71	3.05	4.5	.7	3.15	5.3	.84	4.45	5.6	.77	4.31
V2	2.3	.7	1.61	3.1	.92	2.85	2.7	.92	2.48	2.5	.68	1.70
V6	3.0	.83	2.49	3.0	.81	2.43	2.9	.82	2.38	2.9	.79	2.29
V7	15.08	1.798	27.11	15.08	1.798	27.11	15.08	1.799	27.13	15.08	1.799	27.13
V10	300.07	4.69mA	1.41	300.07	4.55mA	1.36	300.09	4.61mA	1.38	300.08	4.67mA	1.40
V8	6.82	1.018	6.94	6.82	1.018	6.94	6.82	1.018	6.94	6.83	1.018	6.95
V9	39.63	13.04	516.77	39.54	13.04	515.60	39.50	13.04	515.08	39.55	13.04	515.73
ΔVI	35.90			36.01			35.85			35.70		
V11	1097.81	2.003	2198.91	1097.80	2.002	2197.79	1097.64	2.002	2197.47	1097.55	2.003	2198.39
V12	1.35	2.39	3.23	1.35	2.39	3.23	1.35	2.38	3.21	1.35	2.39	3.23
Σ Po			2761.52			2760.46			2760.52			2761.13
V _{in} 28V	300.20	10.24	3074.05	300.21	10.23	3071.15	300.21	10.25	3077.15	300.18	10.26	3079.85
Σ P _{in} Eff(%)	28.29	3.57	100.99	28.29	3.57	100.99	28.29	3.57	100.99	28.29	3.57	100.99
			3175.04			3172.14			3178.14			3180.84
			86.97			86.02			86.86			86.80
TCmv	16.1	314°C		16.1	314°C		16.1	314°C		16.1	314°C	
CV	10.6	215		10.6	215		10.6	215		10.6	215	
NV	12.1	242		12.0	240		12.0	240		12.0	240	
Tank	2.3x10 ⁻⁶ TORR			2.25x10 ⁻⁶ TORR			2.3x10 ⁻⁶ TORR			2.3x10 ⁻⁶ TORR		
Arcs	3			1			1			1		

4.3 EP/PPU THERMAL VACUUM TEST

The EP/PPU was installed in the thermal vacuum chamber and after the coolant lines and electrical connections were completed, an operational test was conducted to check the cable connections and instrumentation. The chamber door was then closed and the chamber was brought to high vacuum. The EP/PPU was left at high vacuum for 72 hours to allow the unit to outgas.

After the 72 hour outgas period, the heat pipe simulator temperature was decreased to -10°C and after temperature stability, the EP/PPU was turned ON.

The following functional tests were conducted:

- o Startup of the EP/PPU at -10°C heat pipe simulator temperature.
- o Steady state operating test at nominal conditions.
- o A low temperature storage test followed by an operational test at ambient temperature.

4.3.1 EP/PPU Thermal Vacuum Test Setup

Thermal vacuum test of the EP/PPU was conducted in a 5ft x 6ft horizontal thermal vacuum chamber. The EP/PPU was suspended edgewise by cables from an overhead bar in the vacuum chamber. The temperature of the EP/PPU was controlled by a heat pipe simulator mounted to the EP/PPU. Fluid was circulated through the simulator at a rate which maintained the temperature difference between the inlet and the outlet at less than one degree Fahrenheit. A thermal blanket was wrapped around the EP/PPU to minimize the effects of radiation from the EP/PPU to the chamber walls.

The EP/PPU was instrumented with thermistors on all representative critical components and structural elements. Table 4-XII lists the thermistor number and locations in the EP/PPU.

The resistive load bank and the control console was placed alongside the vacuum chamber and connections to the EP/PPU made through feed-thru connectors mounted on the access ports of the vacuum chamber.

TABLE 4-XII

EP/PPU THERMISTOR LOCATIONS

Module	Thermistor No.	Location
A1	1	Input Filter-1st Stage
	2	Input Filter-2nd Stage
	3	Hot Spot-TLM Osc.
	4	Hot Spot-28VDC Conv. Pwr. Stage
	5	Hot Spot-28VDC Conv. Control
	6	A1 Module Flange
A2	1	Hot Spot-A2A1
	2	Hot Spot-A2A3
	3	Hot Spot-A2A8
	4	Hot Spot-A2A9
	5	Hot Spot-A2A10
	6	Hot Spot-A2A11
	7	A2 Module Flange
	8	Hot Spot-A2A6
	9	Hot Spot-A2A12
A3	1	SCR 1 or Output Transformer
	2	SCR 2
	3	Diode 1
	4	Diode 2
	5	Series Resonant Inductor
	6	Output Transformer
	7	H.V. Bridge Diode
	8	Hot Spot A3A3
	9	Hot Spot-SCR Firing
	10	Hot Spot-A3A5
	11	Hot Spot-A3A4-A
	12	A3 Module Flange
	13	Hot Spot-A3A4-A

TABLE 4-XII (Cont'd)

EP/PPU THERMISTOR LOCATIONS

Module	Thermistor No.	Location
A4	1	SCR 1
	2	SCR 2
	3	Diode 1
	4	Diode 2
	5	Series Resonant Inductor
	6	Output Transformer
	7	Output Diode
	8	Output Inductor
	9	Hot Spot-SCR Firing Circuit
	10	Hot Spot-A4A5
	11	Hot Spot-A4A4-A
	12	A4 Module Flange
	13	Hot Spot-A4A4-A
A5	1	Transistor 1
	2	Transistor 2
	3	Shunt Diode
	4	Series Resonant Inductor
	5	Hot Spot-A5A2
	6	Hot Spot-A5A5
	7	Hot Spot-A5A3-B
	8	A5 Module Flange
	9	Hot Spot-A5A3-A

TABLE 4-XII (Continued)

EP/PPU THERMISTOR LOCATIONS

Module	Thermistor No.	Location
A6	1	Hot Spot-V3 Output
	2	Hot Spot-V4 Output
	3	Hot Spot-V8 Output
	4	Hot Spot-V8 Boost
	5	Hot Spot-V12 Output
	6	Hot Spot-V6A10
	7	Hot Spot-A6A6
	8	Hot Spot-A6A7
	9	Hot Spot-A6A8
	10	A6 Module Flange
A7	1	Hot Spot-V1 Output
	2	Hot Spot-V2 Output
	3	Hot Spot-V5 Output
	4	Hot Spot-V6 Output
	5	Hot Spot-V7 Output
	6	Hot Spot-V7 Boost
	7	Hot Spot-V7 Output Inductor
	8	Hot Spot-A7A15
	9	Hot Spot-A7A14
	10	Hot Spot-A7A9
	11	Hot Spot-A7A8
	12	Hot Spot-A7A10
	13	A7 Module Flange

4.3.2 EP/PPU Thermal Vacuum Test

Thermal vacuum testing of the EP/PPU was conducted after a single cold solder joint, which, manifested itself at low pressures only and resulted in normal EP/PPU performance whenever the vacuum chamber was returned to atmospheric pressure, was identified and resolved.

Cold Start

The EP/PPU was cold soaked in vacuum for 16 hours at a heat pipe simulator temperature of -10°C . After the 16 hour soak period, the EP/PPU was commanded ON with startup loads of Condition A in Table 4-XIII applied. Data was recorded when the temperatures had stabilized ($2^{\circ}\text{C/hr. max. change}$). Table E-I in the Appendix lists the data for Condition A operation. Loads were changed to Condition D in Table 4-XIII and after temperature stability, data was recorded. Table E-II in the Appendix lists the data for Condition D operation. Mounting and component temperatures were all within limits under the above two operation conditions.

Steady State Operation

The temperature of the heat pipe simulator was set at 0°C . After temperature stabilization the EP/PPU was turned on with loads of Condition D applied. When component temperatures had stabilized, data was recorded. Table E-III in the Appendix lists the data for Condition D, 0°C operation. Tests were conducted for load Conditions C and B as well. At each instant, component temperatures were allowed to stabilize before data were taken. At 0°C heat pipe simulator temperature, and under all line and load conditions, all component temperatures were within prescribed limits.

The heat pipe simulator temperature was increased to 20°C . Tests were conducted for load Condition A, B, C, and D. Data for Condition D, 2A beam current is presented in Table 4-XIV. Condition D loading represents the most severe operating condition. At 20°C heat pipe simulator temperature, all component temperatures were below the maximum limits.

Low Temperature Storage

The EP/PPU was subjected to a 16 hour storage test at a pressure of less than 1×10^{-5} torr and a temperature of -35°C . After the 16 hour soak period, the temperature of the EP/PPU was increased. The EP/PPU responded to all input commands and the outputs were operating normally.

TABLE 4-XIII EP/PPU LOADING

POWER SUPPLY	(STARTUP) CONDITION A	(0.5A BEAM) CONDITION B	(1.0A BEAM) CONDITION C	(2.0A BEAM) CONDITION D
1 Vv	0	6.1V	6.1V	6.1V
Jv	0	0.9A	0.9A	0.9A
2 Vcv	10.0V	4.0V	4.0V	4.0V
Jcv	2.0A	0.82A	0.82A	0.82A
6 Nnv	10.0V	3.5V	3.5V	3.5V
Jnv	2.0A	0.7A	0.7A	0.7A
9 ΔV_I	36.0V	36.0V	36.0V	36.0V
$J_I = J_E + J_{SCR}$	11.0A	4.5A	6.4A	12.3A
8 Vck	20.0V	7.0V	6.0V	5.0V
Jck	1.0A	0.5A	0.5A	0.5A
12 V _{MB}	1.0V	0.5V	0.5V	0.5V
J _{MB}	5.0A	2.0A	2.0A	2.0A
3 V _{CT}	17.8V	0	0	0
J _{CT}	4.0A	0	0	0
4 V _{HTR}	0	4.0V	0	0
J _{HTR}	0	2.0A	0	0
7 V _{nk}	20.0V	15.5V	15.5V	15.5V
J _{nk}	2.1A	2.5A	2.0A	2.0A
5 V _{NT}	17.8V	0	0	0
J _{NT}	4.0A	0	0	0
11 V _{SCR}	0	1100.0V	1100.0V	1100.0V
J _{SCR}	0	0.5A	1.0A	2.0A
10 V _A	0	300.0V	300.0V	300.0V
J _A	0	.005A	.005A	.004A

TABLE 4-XIV EP/PPU THERMAL VACUUM TESTS - CONDITION D

HEAT PIPE SIMULATOR COOLANT TEMPERATURE 20°C - (WITH RTV ON H.P.S.)

JB = 2A
 V_{in} = 300V

POWER SUPPLY	V	I	POWER
V1	6.262	1.005	6.293
V2	4.203	1.074	4.514
V3	--	--	--
V4	--	--	--
V5	--	--	--
V6	3.625	1.051	3.810
V7	16.186	1.809	29.280
V8	5.844	.5060	2.957
V9	38.160	12.2526	467.560
V10	300.29	.0039	1.162
V11	1097.95	2.0043	2200.655
V12	.946	2.098	1.985
TOTAL OUTPUT POWER			2718.216
Input			
<u>Ripple</u> (mA p-p)			
200 - 400V		6	
28V		32	
<u>Power</u>			
200 - 400V	300.33	10.0396	3015.185
28V	27.528	3.696	101.743
TOTAL INPUT POWER			3116.928
EFFICIENCY			87.21%

TABLE 4-XIV (Cont'd) EP/PPU THERMAL VACUUM TEST - CONDITION D

HEAT PIPE SIMULATOR COOLANT TEMPERATURE 20°C - (WITH RTV ON H.P.S.)

JB = 2A
 V_{in} = 300V

MODULE	THERMISTOR NO.		LIMIT °C	TEMP °C
A1	1	Input Filter Inductor-1st Stage	85	25
	2	Input Filter Inductor-2nd Stage	85	23
	3	Hot Spot-TLM Osc.	70	27
	4	Hot Spot-28Vdc Conv. Pwr. Stg.	70	40
	5	Hot Spot-28Vdc Conv. Control	70	35
	6	A1 Module Flange		23
A2	1	Hot Spot-A2A1	70	35
	2	Hot Spot-A2A3	70	39
	3	Hot Spot-A2A8	70	38
	4	Hot Spot-A2A9	70	38
	5	Hot Spot-A2A10	70	33
	6	Hot Spot-A2A11	70	43
	7	A2 Module Flange		24
	8	Hot Spot-A2A6	70	36
	9	Hot Spot-A2A12	70	41
A3	1	Output Transformer	85	41
	2	SCR 2	75	59
	3	Diode 1	86	50
	4	Diode 2	86	50
	5	Series Resonant Inductor	85	53
	6	Output Transformer	85	34
	7	H.V. Bridge Diode	72	44
	8	Hot Spot-A3A3	70	48
	9	Hot Spot-SCR Firing Circuit	70	34
	10	Hot Spot-A3A5	70	43
	11	Hot Spot-A3A4-A	70	57
	12	A3 Module Flangw		30
	13	Hot Spot-A3A4-A	70	47

TABLE 4-XIV (Cont'd) EP/PPU THERMAL VACUUM TEST-CONDITION D
HEAT PIPE SIMULATOR COOLANT TEMPERATURE 20°C (WITH RTV ON H.P.S.)

JB - 2A

V_{in} - 300V

MODULE	THERMISTOR NO.	LOCATION	LIMIT °C	TEMP °C
A4	1	SCR 1	78	30
	2	SCR 2	78	32
	3	Diode 1	95	38
	4	Diode 2	93	37
	5	Series Resonant Inductor	85	40
	6	Output Transformer	85	55
	7	Output Diode	85	57
	8	Output Inductor	85	45
	9	Hot Spot-SCR Firing Circuit	70	38
	10	Hot Spot-A4A5	70	52
	11	Hot Spot-A4A4-A	70	57
	12	A4 Module Flange		26
	13	Hot Spot-A4A4-A	70	46
A5	1	Transistor 1	90	38
	2	Transistor 2	90	38
	3	Shunt Diode	70	34
	4	Series Resonant Inductor	85	46
	5	Hot Spot-A5A2	70	36
	6	Hot Spot-A5A5	70	40
	7	Hot Spot-A5A3-B	70	45
	8	A5 Module Flange		30
	9	Hot Spot-A5A3-A	70	36

TABLE 4-XIV (Cont'd) EP/PPU THERMAL VACUUM TEST - CONDITION D
HEAT PIPE SIMULATOR COOLANT TEMPERATURE 20°C (WITH RTV ON H.P.S.)

JB = 2A

V_{in} = 300V

MODULE	THERMISTOR NO.	LOCATION	LIMIT °C	TEMP °C
A6	1	Hot Spot-V3 Output	87	27
	2	Hot Spot-V4 Output	70	30
	3	Hot Spot-V8 Output	86	25
	4	Hot Spot-V8 Boost	83	26
	5	Hot Spot-V12 Output	85	40
	6	Hot Spot-A6A10	70	38
	7	Hot Spot-A6A6	70	39
	8	Hot Spot-A6A7	70	40
	9	Hot Spot-A6A8	70	39
	10	A6 Module Flange		24
A7	1	Hot Spot-V1 Output	70	27
	2	Hot Spot-V2 Output	70	28
	3	Hot Spot-V5 Output	87	24
	4	Hot Spot-V6 Output	70	28
	5	Hot Spot-V7 Output	58	30
	6	Hot Spot-V7 Boost	83	28
	7	Hot Spot-V7 Output Inductor	85	31
	8	Hot Spot-A7A15	70	36
	9	Hot Spot-A7A14	70	34
	10	Hot Spot-A7A9	70	37
	11	Hot Spot-A7A8	70	39
	12	Hot Spot-A7A10	70	37
	13	A7 Module Flange		22

4.4 ELECTROMAGNETIC INTERFERENCE TESTS

Electromagnetic interference tests were performed on the 30cm electrical prototype power processor so that baseline information would be available to spacecraft system engineers to conduct interaction studies for spacecraft subsystems and scientific experiments.

Good engineering practices were used in the design of the input power line filters and the application of EMI feedthrough filters, both on the high voltage and low voltage outputs of the EP/PPU. The EMI test data will also serve as a data base for EMC requirements versus filter weight trade-off studies and thereby help define realistic EMI levels and EMC system design approaches.

Two basic sets of tests were performed:

- (1) Conducted narrowband and broadband interference with the power processor and ion engine operating at the 2A beam current level.
- (2) Radiation and conducted narrowband and broadband interference with the power processor operating with an ion engine load bank simulator in an EMC screen room.

A summary of the conducted narrowband and broadband interference test results for the power processor operating with an ion engine is presented, since this mode of operation produces the higher electromagnetic interference levels.

Data is presented for the following lines:

- 200-400VDC main input power line
- 28VDC auxiliary input power line
- V9 discharge supply output line (current level of 12-14 ADC)
- V11 screen output line (high output power of 2.2W)
- Interface unit command line bundle.

The narrowband radiation levels for these five lines are presented in Figures 4-13 through 4-17. Figures F-1 through F-5 in the Appendix present the broadband data for the above five lines.

The narrowband data is close to meeting the MIL-461A, Notice 3, Specification levels.

It is suspected that the high broadband conducted emissions are due to the operational noise of the ion engine coupling from the unshielded output cables.

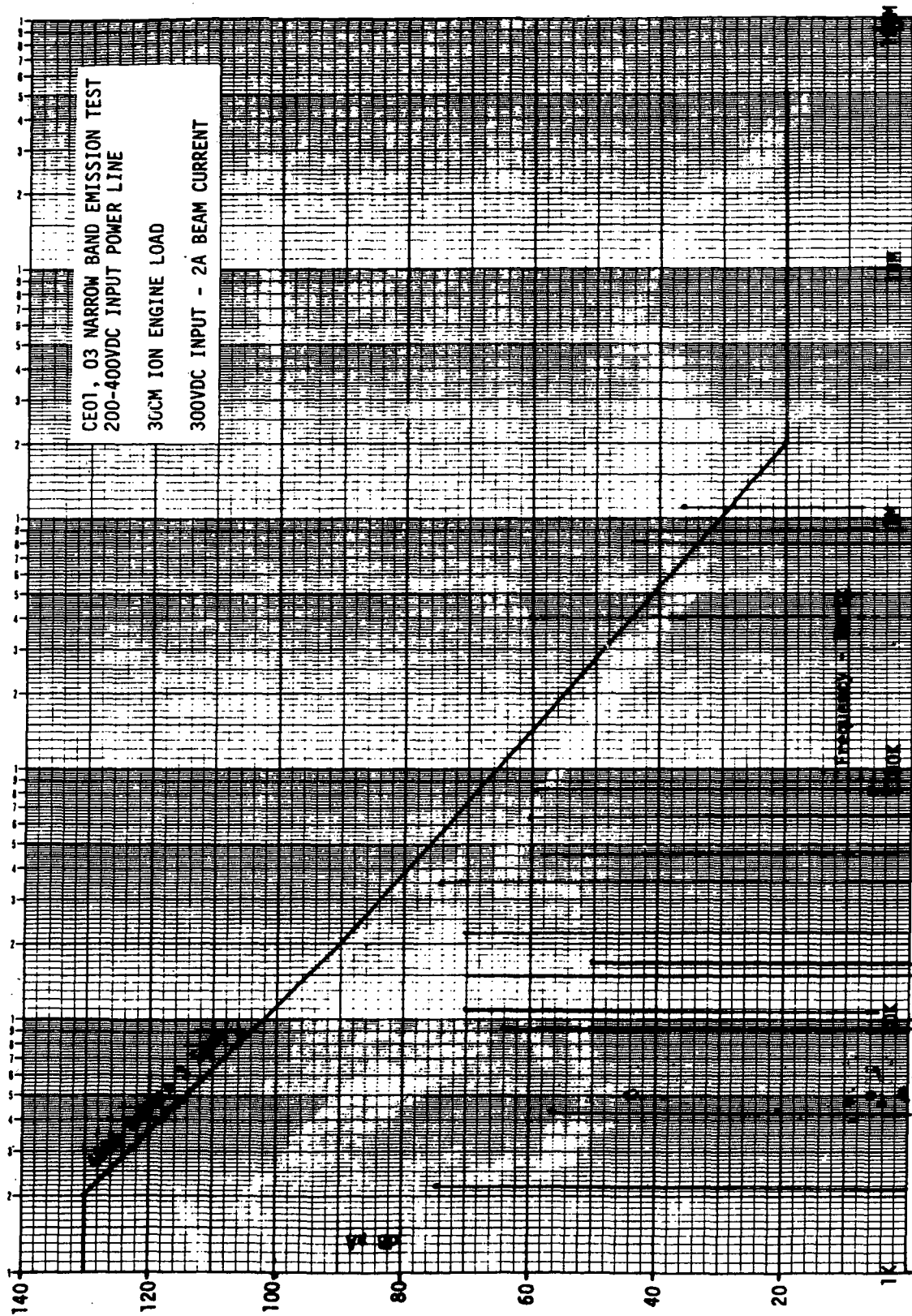


FIGURE 4-13. 300V INPUT POWER LINE, NARROWBAND EMISSION

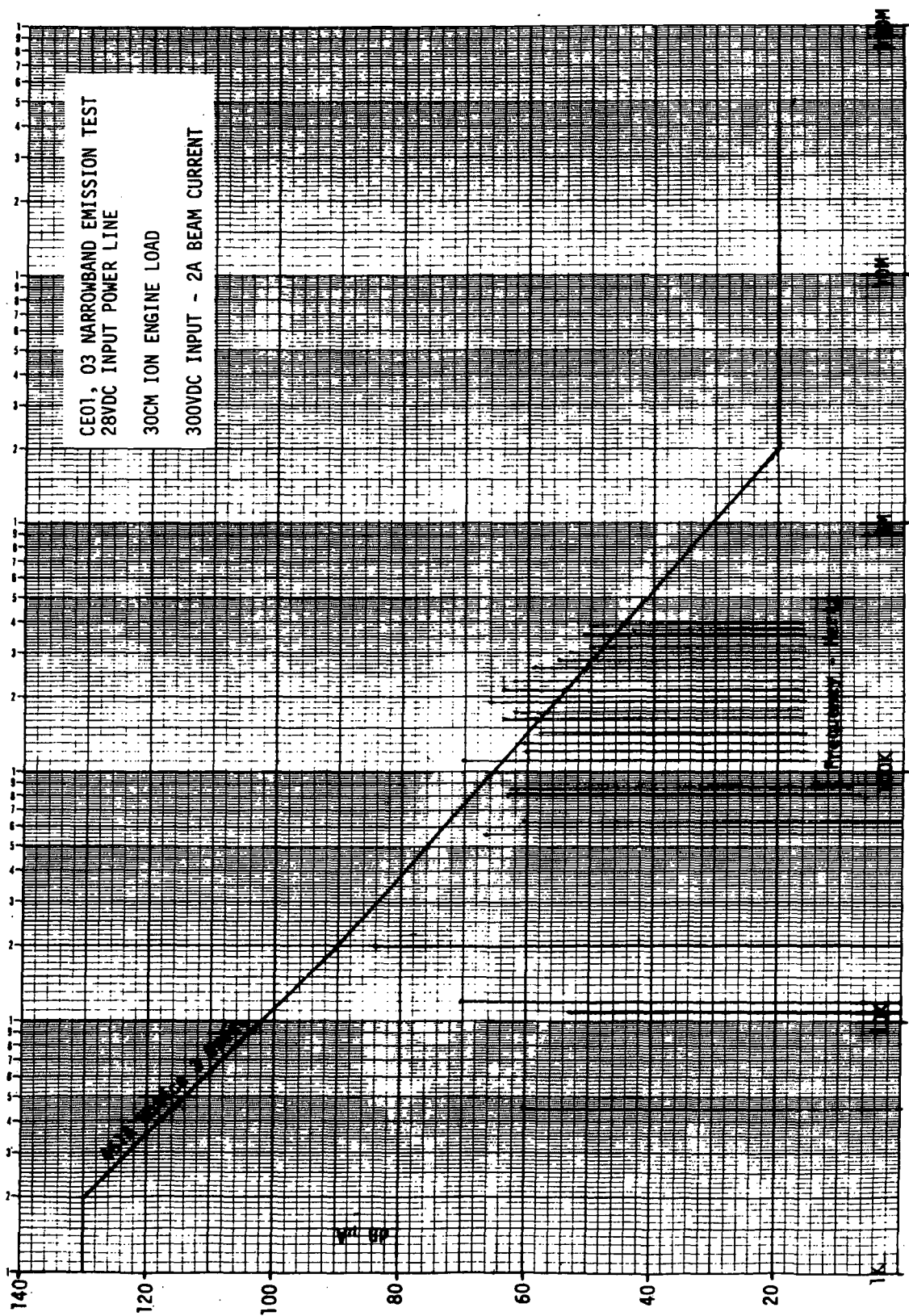


FIGURE 4-14. 28V INPUT POWER LINE NARROWBAND EMISSION

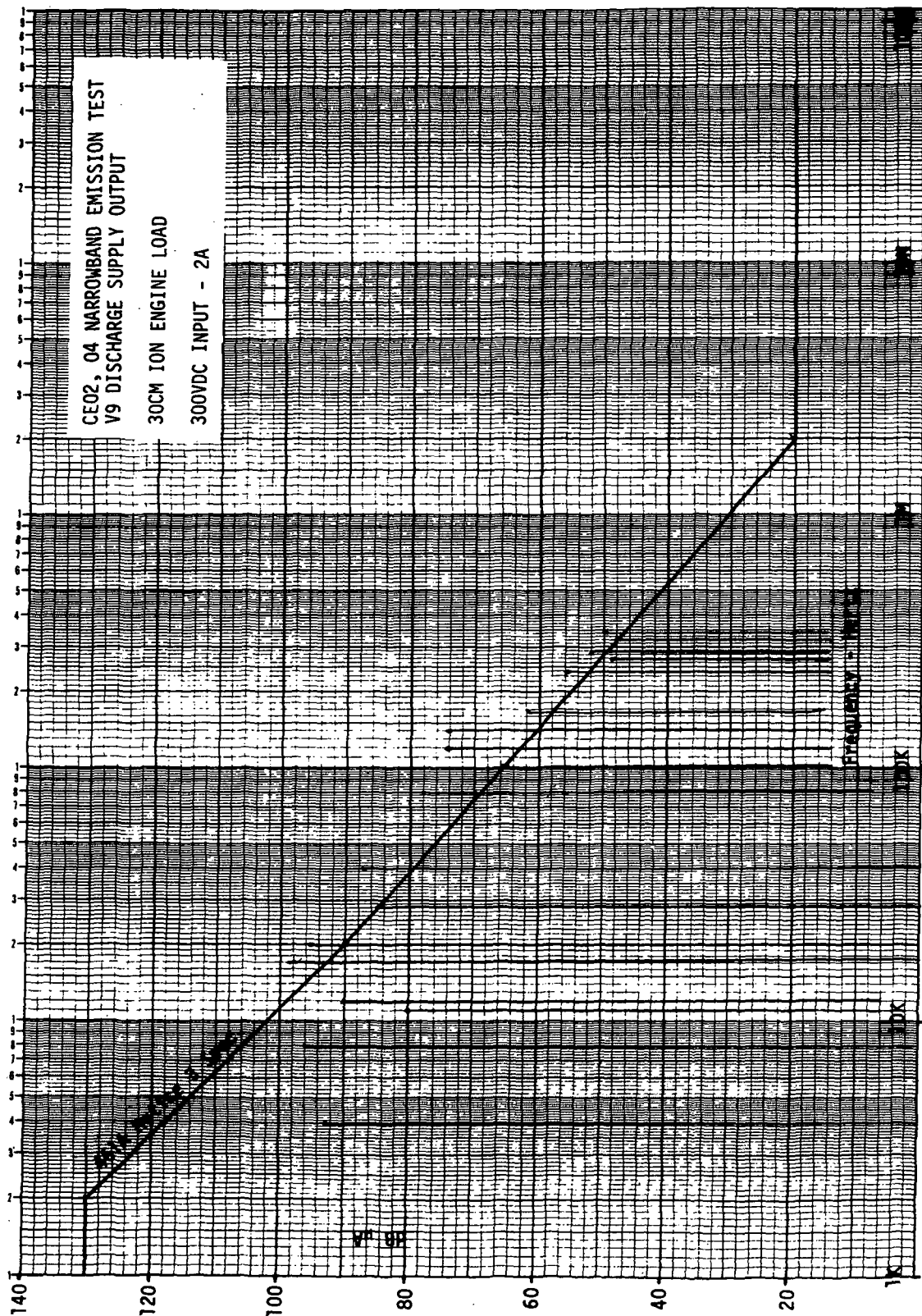


FIGURE 4-15. V9 DISCHARGE SUPPLY NARROWBAND EMISSION

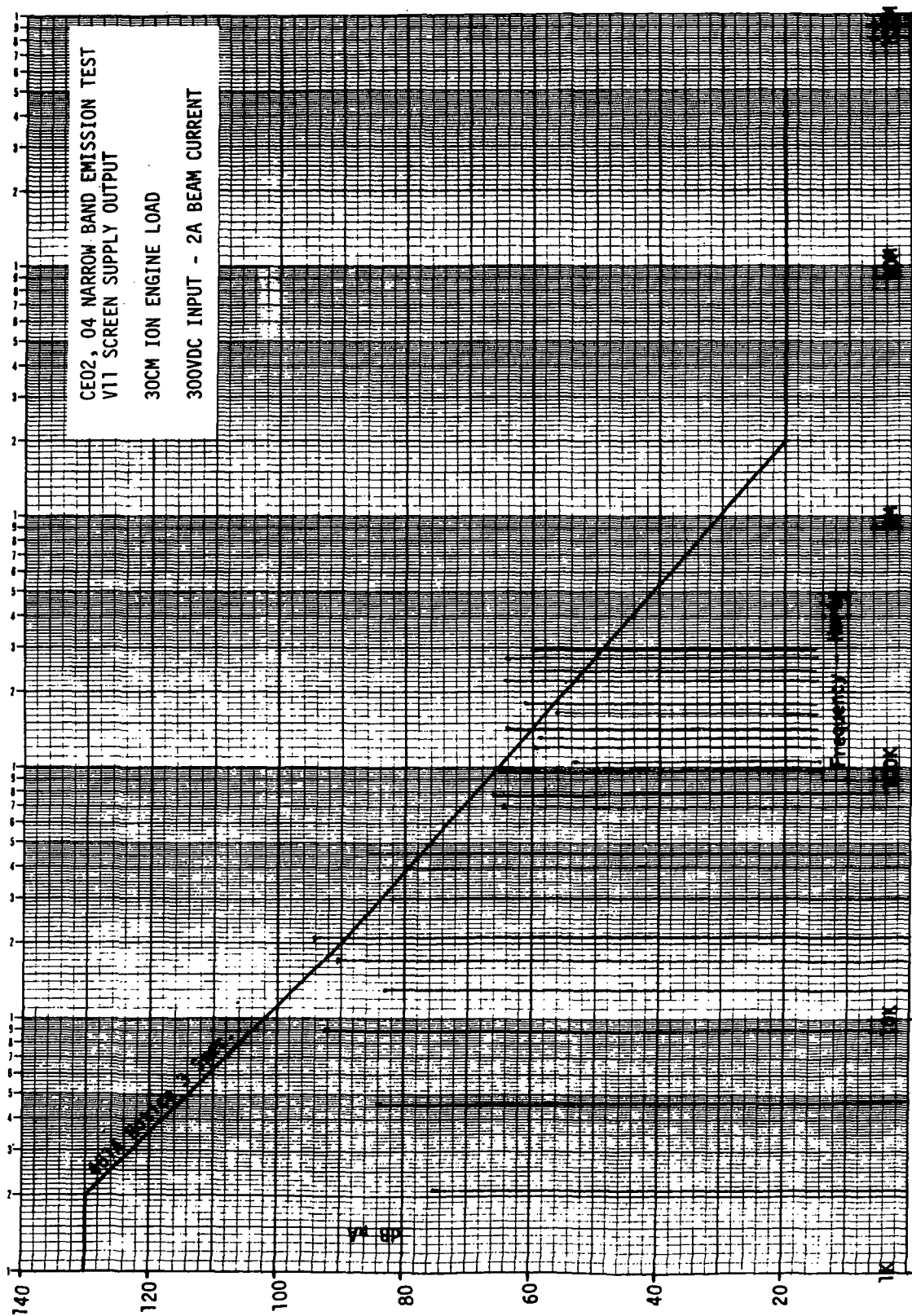


FIGURE 4-16. V11 - SCREEN SUPPLY NARROWBAND EMISSION

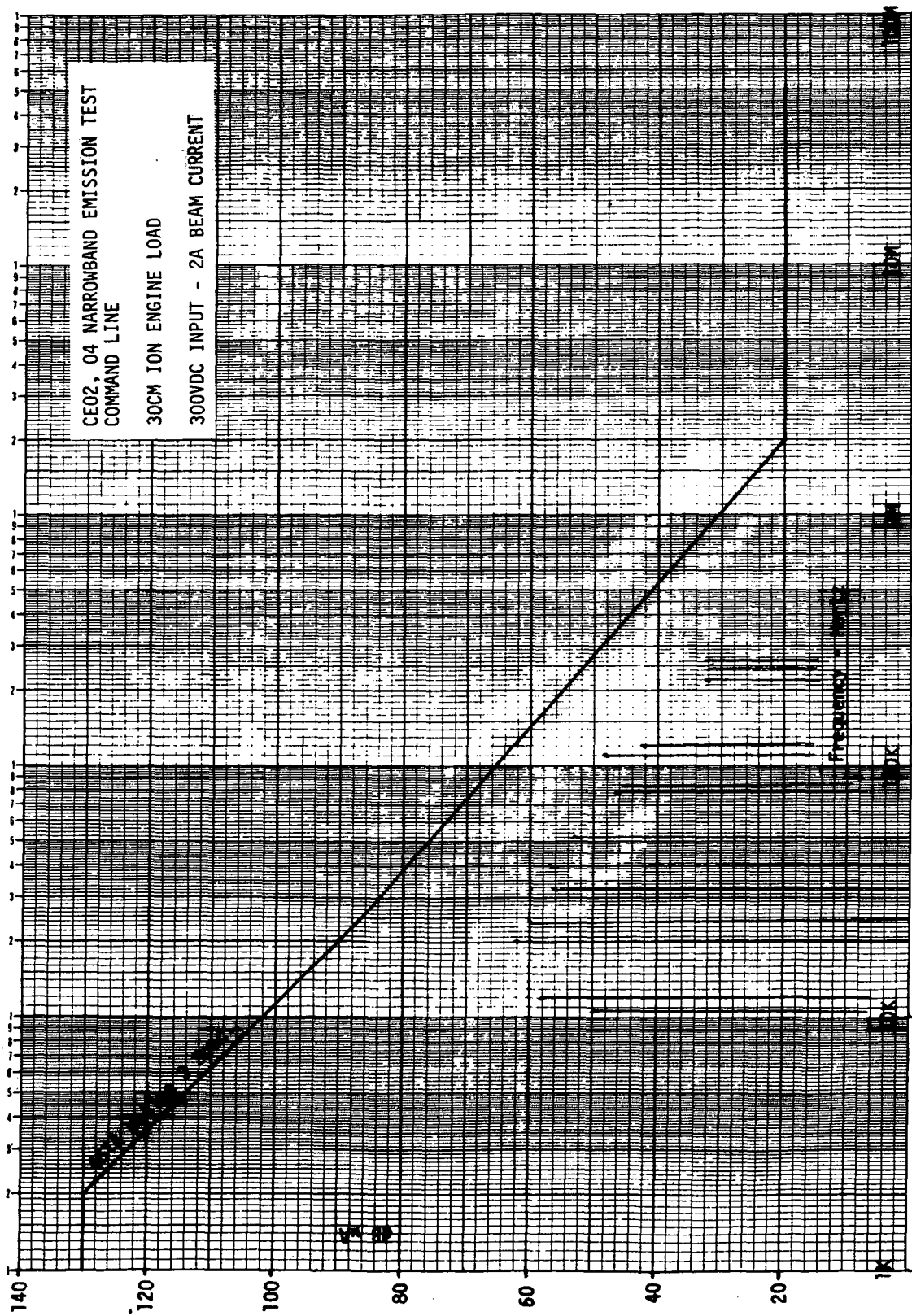


FIGURE 4-17. COMMAND LINE NARROWBAND EMISSION

5.0 CONCLUSIONS

An Electrical Prototype/Power Processor Unit (EP/PPU; a brass-board model) was designed to meet the latest 30cm Ion Engine power requirements. The EP/PPU packaging demonstrates the relative placement and thermal control techniques of the electrical components recommended for the layout and thermal design of the Functional Model/Power Processor Unit (FM/PPU). The FM/PPU is being designed by NASA LeRC to meet all the environmental requirements including structural and operation over the full thermal-vacuum temperature range.

The EP/PPU was fabricated with electrical parts that have flight types equivalents, wherever possible, and all magnetic devices are flight type components. Extensive power component improvements were performed on the program to reduce weight and to control component temperature rise. Additional component work is required to generate flight component specifications and component qualification. Power losses and part count of the control electronics have shown to be potential problem areas. Circuit and component areas were identified where additional development effort can improve overall efficiency weight and reliability.

The EP/PPU is composed of seven separate testable modules. The conceptual mechanical design identified the logical separation of functions, relative location of power components for thermal control and voltage control. Additional packaging effort is required in the command interface unit to increase its noise immunity and serviceability.

The test program demonstrated the overall capability of the EP/PPU to be operated in a thermal vacuum environment so that meaningful thermal control information can be obtained in support of the Functional Model Unit mechanical and thermal design, and to operate a 30cm Ion Thruster over its total output power range by means of an external central computer system. The series resonant inverter used as the main dc to ac inversion power stage demonstrated reliable trouble free operation throughout all the testing phases.

6.0 APPENDICES

TABLE OF CONTENTS

- A - ELECTRICAL DESIGN
- B - ELECTRICAL COMPONENT DEVELOPMENT
- C - EP/PPU LOAD BANK TEST RESULTS
- D - EP/PPU-ION ENGINE TEST RESULTS
- E - EP/PPU THERMAL VACUUM TEST RESULTS
- F - EP/PPU-ION ENGINE EMI TEST RESULTS

NOTE: Appendices are available upon request from
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