NASA CR-156705

DC AMPLIFIER FOR NUCLEAR PARTICLE MEASUREMENT

(NASA-CR-156705) A dc AMPLIFIER FOR NUCLEAR PARTICLE MEASUREMENT Final Report, Dec. 1975 - Nov. 1977 (Michigan Univ.) 107 p
HC A06/MF A01 CSCL 09A
N78-19394
Unclas
G3/33 07317

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January 1978
Final Report for Period
December 4, 1975 to November 3, 1977
014393-F

Prepared for
National Aeronautics & Space Administration, Code 663
GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland 20771

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.

4. Title and Subtitle	5. Report Date
DC AMPLIFIER FOR NUCLEAR PARTICLE MEASUREMENT	January 1978
	6. Performing Organization Code

7. Author(s)	8. Performing Organization Report No.
A. B. Macnee and N. A. Masnari	014393-F

9. Performing Organization Name and Address	10. Work Unit No.
Cooley Electronics Laboratory University of Michigan Ann Arbor, Michigan 48109	
	11. Contract or Grant No. NAS5-22875
	13. Type of Report and Period Covered Final - Dec. 1975 - Nov. 1977
12. Sponsoring Agency Name and Address National Aeronautics & Space Admin. Goddard Space Flight Center Greenbelt, Maryland 20771 J. Trainor, Technical Officer	14. Sponsoring Agency Code 663

15. Supplementary Notes

16. Abstract

A monolithic preamplifier-postamplifier combination has been developed for use with solid state particle detectors. The direct coupled amplifiers employ interdigitated n-channel JFET's, diodes, and diffused resistors.

The circuits developed demonstrate the feasibility of matching the performance of existing discrete component designs. The fabrication procedures for the monolithic amplifier fabrication are presented and the results of measurements on a limited number of sample amplifiers are given.

17. Key Words (Selected by Author(s))	18. Distribution Statement
Charge sensitive preamplifier JFET monolithic amplifier Low noise amplifier	

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price*
		106	

*For sale by the National Technical Information Service, Springfield, Virginia 22151.

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont.)

I. INTRODUCTION

A. B. Macnee

This is the final report on contract NAS5-22875 for the period December 4, 1975 to November 3, 1977. The objectives of this contract were to develop a fully-integrated circuit version of the preamp/postamp used with the solid state detectors on MTS; to carry out the necessary development to match the performance of existing discrete component designs; and to carry out pilot fabrication runs to verify the performance of the designs.

The development of circuit designs suitable for monolithic fabrication has been completed. The pre- and post-amplifiers utilize JFET's as the active, gain-producing elements plus diffused resistors and diodes for supplying the needed biasing and interstage coupling. There circuits are described in Section II.

The fabrication processes necessary for the monolithic realization of these circuit designs are given in Section III. Initially the fabrication of single JFET's was carried out, and sample transistors were employed in the breadboarding of the preamplifier and postamplifier circuits. When the performance of these breadboarded circuits was comparable to that of earlier discrete designs (using bipolar as well as JFET transistors), the fabrication of

complete monolithic amplifiers was planned and carried out. These monolithic designs and the necessary fabrication sequences are described in Section III.

Testing of samples from the pilot production runs is presented in Section IV. The best postamplifier samples achieve the desired dynamic performance, but they require more dc power than planned. The increased power is caused by unanticipated current flow to the amplifier substrate. The substrate currents can be prevented by straight-forward modifications of the fabrication sequence. Within the period of the contract, the pilot fabrication runs did not produce preamplifiers in which the device parameters fell within the circuit design limits. A limited number of the "out of limits" units were tested, and there is every indication that once the desired device parameters are achieved, the monolithic units will match the performance of the design breadboard.

Section V summarizes the results achieved under this contract, and presents suggestions for further work.

II. CIRCUIT DESIGN OF PRE- AND POST-AMPLIFIERS FOR A NUCLEAR PARTICLE MEASUREMENT SYSTEM

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Staff: William Goldes, Jr.

2.1 General Circuit Considerations

The project objective was to develop charge-sensitive preamplifier and postamplifier circuit designs suitable for fabrication in monolithic circuit form, using junction field effect devices (JFET's) as the active, gain producing elements. A typical nuclear particle measurement system is indicated schematically in Fig. 2.1. In this figure the discrete R's and C's represent components which will normally be connected external to the pre- and post-amplifiers, which are represented by blocks. C_D represents the capacitance of the nuclear particle detector which can lie in the range 25 to 1500 picofarads. The combination of C_3 and R_L represent the input of a pulse height analysis system that analyzes and stores the pulses processed by the circuit. In typical earlier and existing systems the pre- and post-amplifier are fabricated using discrete components: resistors, capacitors, bipolar transistors (npn and pnp), and junction field effect transistors. The objective of this contract was to develop amplifiers which could be fabricated in monolithic

form and which could match the system performance of existing discrete component designs. The immediate system benefits should be a reduction in size and weight.

Previous experience has indicated that junction field effect transistors represent the best choice for the input stage of a charge sensitive preamplifier.[1] Because the fabrication of JFET and bipolar transistors in a single monolithic integrated circuit is much more difficult than the fabrication of either device alone, we elected to design both the pre- and post-amplifiers using only JFET transistors as the gain producing components. As long as the two amplifiers are fabricated on separate silicon chips, one could fabricate the postamplifier with bipolar devices. The construction of the amplifiers on separate chips is forced on us, at present, by the maximum area limitation of our mask making facilities (maximum chip size we can handle is 75 mils by 75 mils), but it is anticipated that ultimately fabrication on a single chip may be used for flight components. A further expected benefit of the designs using JFET's is the superior resistance of JFET's to radiation damage.

2.2 Amplifier Specifications

If the input to the system shown in Fig. 2.1 is considered to be a current impulse carrying a charge $-Q$, the

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[1] F. S. Goulding, "Preamplifiers," Semiconductor Nuclear Particle Detectors and Circuits; Publication 1593, National Academy of Sciences, Washington, D.C., 1969, pp. 381-390.
V. Radeka, "Field-Effect Transistor Noise as a Function of Temperature and Frequency," Ibid, pp. 393-401.

output of the postamplifier should be

$$v_o(t) \simeq \frac{-\frac{R_2}{R_1}\left(\frac{A_2}{1+A_2+\frac{R_2}{R_1}}\right)Q}{\left(C_F + \frac{C_F+C_D}{A_1}\right)} \times \frac{t}{\tau} e^{-\frac{t}{\tau}} \qquad (2.1)$$

where $-A_1$ = preamplifier voltage gain

$-A_2$ = postamplifier voltage gain

$\tau = R_1C_1 = R_2C_2$ = postamplifier time constant.

This pulse reaches a peak value of

$$v_o(t)\Big|_{max} = 0.368 \frac{\frac{R_2}{R_1}\left(\frac{A_2}{1+A_2+\frac{R_2}{R_1}}\right)}{\left(C_F + \frac{C_F+C_D}{A_1}\right)} \times Q = KQ \qquad (2.2)$$

at $t = \tau$.

This expression shows the dependence of the system charge sensitivity, $v_o|_{max}/Q$, on the amplifier voltage gains, which can be expected to show some variability with life and environmental conditions. Typical values used in the early Pioneer satellite systems were $A_1 = -5000$, $A_2 = -1500$, and $R_2/R_1 = 4.8$. The sensitivity of K to changes in A_1 is

$$S^K_{A_1} = \frac{1}{1+\frac{A_1C_F}{C_F+C_D}} \qquad (2.3)$$

and the sensitivity to changes in A_2 is

$$S^K_{A_2} = \frac{1}{1+\frac{A_2 R_1}{R_1+R_2}} \tag{2.4}$$

For the above numbers $S^K_{A_2} = 3.85 \times 10^{-3}$; and if $C_D/C_F = 25/2$, $S^K_{A_1} = 2.69 \times 10^{-3}$. The sensitivity with respect to A_1 is a strong function of the ratio of the detector and feedback capacitances. For $C_F = 2$ pF and $C_D = 1500$ pF with $A_1 = -5000$, the sensitivity $S^K_{A_1}$ is increased to 0.131! It is evident that one would like to have A_1 and A_2 as large as possible, and that if large detector capacitances are anticipated, the gain of A_1 is particularly important.

To achieve high gains one is led to multistage amplifier designs. Generally, one increases the overall gain by increasing the number of stages and the quiescent operating currents of the active devices used. Both of these increases tend to increase the power consumption of the amplifiers. For space flight applications one wishes to hold power consumption to a minimum. Again, taking an early Pioneer charge measuring system as a reference point, typical values were 12.6 milliwatts for the preamplifier and 5.2 milliwatts for the postamplifier.

The output voltage from the preamplifier-postamplifier charge measurement system is supplied to a pulse height

analysis system which is represented in Fig. 2.1 by a load resistance R_L. Typically this is several thousand ohms, and in all of our testing we have taken it to be 3.9 kilohms. The preamplifier should be capable of delivering a pulse of up to 5 volts peak amplitude to this load.

The expression for $v_o(t)$ in Eq. 2.1 and its maximum amplitude, Eq. 2.2, are calculated for amplifiers with perfect high-frequency response. This assumption makes the impulse response of the preamplifier-integrator have zero risetime. Assuming the preamplifier has a single dominant high-frequency pole at $s = -\omega_h$, makes the risetime of the output $2.2/\omega_h$ seconds. Calculation shows that this finite risetime reduces the maximum value given by (2.2) by the factor

$$R = \frac{(\omega_h\tau-2)\ (\omega_h\tau)}{(\omega_h\tau-1)^2}$$

where τ is the postamplifier pulse shaping time constant. A few values of this correction factor are tabulated below.

$\omega_h\tau$	R
10	0.9877
20	0.9972
30	0.9988
50	0.9996

For τ = 3 microseconds and $\omega_h\tau = 30$, $\omega_h = 10^7$ radians per second. Therefore an integrator risetime of 0.22 microseconds or less will change the output pulse amplitude less than a tenth of one percent. Even an integrator risetime as long as one microsecond, giving $\omega_h\tau = 6.6$, would only reduce the peak output of the postamplifier by 3.2 percent. Such a reduction can be accounted for easily in the calibration of the complete system. For any given amplifier, ω_h should be relatively independent of the system's life or environment.

2.3 Preamplifier Design

The intended fabrication in monolithic form precludes the use of capacitors for coupling or bypassing within the preamplifier. This means it must be direct coupled. In our initial designs we consider a cascade of three common-source JFET stages followed by a JFET source follower at the output as indicated in Fig. 2.2. The source follower's low output impedance allows the preamplifier to drive a relatively low impedance load and could be important if the pre- and post-amplifiers were to be physically separated by a large distance. It also contributes something to the preamplifier's voltage gain by raising the load resistance seen by the last common-source stage.

When we considered realizing the source follower circuit in monolithic form, however, a serious limitation became apparent. When the JFET's are fabricated in the

monolithic form, each transistor gate is formed by a p-diffusion into a thin epitaxial n-region which sits on a p-substrate as shown in Fig. 2.3. The channel is the thin n-layer remaining between the bottom of the gate diffusion and the p-substrate. This channel can be pinched off from either side which means that each transistor has, in effect, two gates: one on the top of the wafer which is created by design, and a second one which is the substrate layer. The p-substrate must be operated at a fixed negative dc potential in the circuit to assure that no transistor substrate gate is forward biased. Figure 2.2 shows that all the JFET's have second gates which are connected to the V^- supply. These gates are indicated by the dotted lines. For the transistors operating with fixed source potentials, this extra gate only serves to narrow the "zero bias" channel width. This reduces the effective values of I_{DSS} and V_p below what one measures with the substrate at the source potential. In the case of the source follower, however, the fixed potential of the substrate gate negates the follower action. The incremental voltage gain for this stage is reduced to

$$\frac{V_o}{V_i} = \frac{G_{m1} R_L}{1 + (G_{m1}+G_{m2}) R_L} \qquad (2.6)$$

where G_{m1} = transconductance for gate #1

G_{m2} = transconductance for substrate gate

R_L = load from source to ground

This gain can never exceed $G_{m1}/(G_{m1}+G_{m2})$ even if R_L is made very large.

Recognition of this incremental gain loss plus the large drop in the effective value of I_{DSS} prompted us to remove the source follower from Fig. 2.2. Without the source follower it is important to have the postamplifier circuit (a) located as close to the preamplifier as possible, and (b) to keep its input impedance as large as possible compared to the load resistor of the preamplifier output stage.

The resistive coupling circuits of the basic amplifier shown in Fig. 2.2 have two drawbacks: (1) They introduce a coupling loss and (2) they generate thermal noise. The coupling loss can be eliminated by replacing the resistors between the gates and the V^- supply by current sources. Small JFET's connected with gate to source shorts represent an easy way of generating the needed small current sources. The area of these small JFET's can be selected to give the desired current values (values of I_{DSS}).

An incremental noise model of the input JFET and its coupling network to the second stage is drawn in Fig. 2.4. The noise of the JFET, Q_1 , is represented by the i_{n1} and v_{n1} sources. The noise sources in the coupling circuit

are i_c and i_L, which represent thermal noise generated by the resistors R_C and R_L, and i_{J2} which is the shot noise associated with the current source JFET, Q_2. Analysis of this circuit shows that all of the coupling circuit noises can be represented by increases in the value of equivalent noise resistance R_{nv} associated with the v_{n1} noise voltage. The total equivalent noise resistance is then

$$R_{nv} = \frac{K_1}{g_{m1}} + \frac{1}{g_{m1}^2 R_L} + \frac{R_C}{(g_{m1}R_L)^2} + \frac{g_{m2}K_2}{g_{m1}^2}\left(1+\frac{R_C}{R_L}\right)^2 \qquad (2.7)$$

The first term in this expression is due to the Q_1 transistor alone. The next two terms are the contributions of the thermal noise from R_L and R_C respectively, and the last term is due to the shot noise from Q_2. The constants K_1 and K_2 are of the order of unity. A typical design might run 1 milliampere through Q_1, 0.2 milliampere through Q_2, R_L = 3.9 kilohm, and R_C = 9.5 kilohm. Then for our JFET's we get g_{m1} = 3.3 mA/volt and g_{m2} = 0.167 mA/volt. Putting these numbers into Eq. 2.7 gives

$$R_{nv} = 303 + 23.5 + 57.3 + 181 = 565 \text{ ohms}$$

This example shows that: (1) the coupling circuit noise can almost double the equivalent series input noise and (2) most of the extra noise comes from the JFET current source. The analysis also shows that this extra noise can be greatly reduced by making R_C small. In practice this

can be achieved by replacing R_C by a series connection of an appropriate number of pn junction diodes.

The circuit of our final preamplifier design is given in Fig. 2.5. As discussed above, the coupling circuit between the first and second transistors uses a string of four diodes. Noise measurements on a discrete component breadboard of this circuit verified the substantial noise reduction predicted by Eq. 2.7 when R_C was replaced by the diode string. The transistor quiescent operating points in this design are tabulated below the circuit along with the design values of I_{DSS} and V_p when the substrate is tied to the source. This is the way in which Q_5 and Q_6 are connected, but for Q_2, Q_3, and Q_4 the substrate is at -4 volts relative to the source. This reduces the effective values of V_p and I_{DSS} for these transistors, but it increases the transconductance at a fixed quiescent current.[1]

To predict the dc performance of the preamplifier design in Fig. 2.5, and the postamplifier design of the subsequent section, one needs a dc model of the dual-gate JFET. Our measurements of typical JFET's fabricated in our laboratory show that in the pinch-off region the dependence of the drain current on the gate-source and substrate-source voltages can be modeled approximately by

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[1] Quarterly No. 6, Section 3.1, Table 3.1.

$$i_D \simeq I_{DSS} \left(1 + \frac{V_{GS}}{V_{p1}} + \frac{V_{SS}}{V_{p2}}\right)^2 \tag{2.8}$$

The reference directions for the current and voltages in Eq. 2.8 are given in Fig. 2.6(a). If the substrate is held at a fixed potential V_{SS}, this can be rearranged to

$$i_D \simeq I_{DSS} \left(1 + \frac{V_{SS}}{V_{p2}}\right)^2 \left[1 + \frac{V_{GS}}{V_{p1}\left(1+\frac{V_{SS}}{V_{p2}}\right)}\right]^2 \tag{2.9}$$

$$= I'_{DSS} \left(1 + \frac{V_{GS}}{V'_p}\right)^2$$

which shows that a negative substrate bias lowers the effective values of I_{DSS} and V_p for the transistor to

$$I'_{DSS} = I_{DSS} \left(1 + \frac{V_{SS}}{V_{p2}}\right)^2 \tag{2.10}$$

and

$$V'_p = V_p \left(1 + \frac{V_{SS}}{V_{p2}}\right) \tag{2.11}$$

At a fixed quiescent current I_D^Q, this predicts the gate-source transconductance to be

$$g_m = \frac{\partial i_D}{\partial V_{GS}} \doteq \frac{2\sqrt{I_D^Q \cdot I'_{DSS}}}{V'_p} = \frac{2\sqrt{I_D^Q \cdot I_{DSS}}}{V_p} \tag{2.12}$$

which does not depend upon V_{p2} and V_{SS}. In practice, the g_m shows an increase with more negative values of V_{SS}, but for analysis of a circuit's performance around a quiescent point, (2.8) is reasonably accurate. Equation 2.8 can be implemented simply in any dc analysis program equipped to model JFET's without the substrate gate. An analysis program model, which is valid for negative substrate biases, is drawn in Fig. 2.6(b). In this model J_4 is the conventional dc JFET model which assumes the current is independent of the drain-source voltage in the pinch-off region ($V_{DS} > V_p + V_{GS}$). The resistance r_o is added to account for the finite resistance observed in real devices, and the controlled voltage source, v_1, models the control of the substrate gate. In the preamplifier design (Fig. 2.5) the substrate is at a fixed negative potential, and therefore v_1 in the model becomes a small fixed voltage source.

The dc performance of the amplifier circuit design in Fig. 2.5 was analyzed using our computer analysis program DCAP.[1] Each transistor was modeled as indicated in Fig. 2.6(b) and the 166 pF "load" capacitor was replaced by a 1.4 volt battery.[2] Some results of these calculations are summarized in Table 2.1. With the nominal transistor parameters the incremental voltage gain is -2080, and the power required

[1]Calahan et al., Introduction to Modern Circuit Analysis, Holt, Rinehart, & Winston, 1974, Section 5.8.

[2]This is a worst-case assumption for the preamplifier.

is 12.7 milliwatts. The first, third, and fourth columns in the table show the calculated effect of variations in the transistor parameters due to changes in the undepleted channel width.[1] The assumed ±20 percent changes result in a 3.38:1 range for I_{DSS} of each transistor and a 2.25:1 range of V_p.

Table 2.1 Calculated preamplifier performance with varying transistor parameters

Channel Width	-20%	Nominal	+10%	+20%
Normalized pinch-off voltage	0.64	1.0	1.21	1.44
Normalized I_{DSS}	0.512	1.0	1.331	1.728
Quiescent Point Values				
V_{DS}^{Q2} (volts)	1.40	1.40	1.40	1.455
V_{GS}^{Q4} (volts)	+0.0194	-0.595	-0.986	-1.412
Voltage gain	-3310.0	-2080.0	-1600.0	-401.0
Power required (in milliwatts)	11.12	12.7	13.7	14.9

For the channel's 20 percent narrower than nominal, the gain is increased to -3310 and the power consumption is reduced to 11.1 milliwatts. It will be noticed, however,

[1] The expected dependence of V_p and I_{DSS} on the undepleted channel width is discussed in Quarterly 014393-1, Section 2.2 and Quarterly 014393-3, Section 3.3.

that to maintain the same quiescent point for the output transistor, Q_2, the gate source voltage of the first transistor Q_4 is 19.4 millivolts positive. Any further reduction in channel width would lead to operation of the first transistor with a more positive gate, and the resulting gate current would lower the input impedance and increase the noise current associated with this transistor (i_{n1} in Fig. 2.4(b)).

When all the channel widths are increased 20 percent, there is a sharp reduction in the incremental gain to -401 and the power consumption rises to 14.9 milliwatts. Investigation reveals that this large loss of gain is caused by the input transistor (Q_4 in Fig. 2.5) operating in its resistive or saturation region. The Q-point drain-source voltage is down to +0.47 volts. This shift of Q-point is accentuated by the increased current taken by Q_6 at the wider channel width. For a +10% increase in channel width the gain is still a very reasonable -1600.

The calculations summarized in Table 2.1 assume that the only parameter available for adjustment is the external resistor R_S, and that it is always adjusted to make the quiescent drain-source voltage of the output transistor 1.4 volts. One could increase the tolerance to changes in undepleted channel width by bringing the source of transistor Q_6 out to the external circuit instead of connecting it internally to the -4 volt supply lead as

shown. A resistor inserted between the source and the -4 volt supply would allow a reduction of the current taken by Q_6.

The calculated voltage gains in Table 2.1 assume an external 16 kilohm load, as indicated in Fig. 2.5. The gain is proportional to the parallel resistance associated with this external resistor and the 15 kilohm resistor, R_5. For example, doubling the impedance level of the load (making it 87 pF in series with 36 kilohms) would multiply all the gains in Table 2.1 by 1.29.

The preamplifier design given in Fig. 2.5 was built up on a printed circuit board using transistors fabricated on individual test chips and discrete 1/4 watt composition resistors.[1] The performance of the breadboard was in reasonable agreement with the values calculated using DCAP. Table 2.2 shows the measured values and the nominal calculated values. The Q-points of Q_2 and Q_3 easily could be adjusted closer to the nominal values tabulated (by reducing the value of R_S slightly). The input transistor, Q_4, in the breadboard was from a later fabrication run than Q_2 and Q_3. Therefore its characteristics do not match those of Q_2 and Q_3, and it had to be operated close to zero bias to give the desired quiescent drain current.

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[1] These transistors are the interdigital units discussed in Quarterly 014393-6, Section 2.3.

Table 2.2 Comparison of breadboard measurements with computer calculations for pre-amplifier Design 4 (Fig. 2.5)

Parameters	Calculated	Measured
V_{DS}^{Q4} (volts)	1.43	1.493
V_{GS}^{Q4} (volts)	-0.595	-0.035
Q_4 gain	-13.0	-10.0
V_{DS}^{Q3} (volts)	1.40	1.29
V_{GS}^{Q3} (volts)	-0.715	-0.726
Q_3 gain	-14.8	-16.0
V_{DS}^{Q2} (volts)	1.40	2.05
V_{GS}^{Q2} (volts)	-0.695	-0.685
Q_2 gain	-10.7	-15.6
Overall gain	-2050	-2500

Q_4 - Sample No. 2.5 N/P 8L

Q_3 - Sample No. 2.5 N/P 5-6

Q_2 - Sample No. 2.5 N/P 5-11

The measured noise performance of this preamplifier breadboard is plotted in Fig. 2.7 for varying shunt input capacitance. This measurement was made for Q_4 transistor 2.5 N/P 8L which has a "metallized" gate and for SFB8558 #6. Without this metallization the noise increased by a factor of 2.[1] The measured performance with this metallized JFET is about 60 percent poorer than the best we have measured using SFB8558's. At the quiescent drain current of 1 mA, the SFB8558's have transconductances about 40 percent greater than 2.5 N/P 8L.

2.4 Postamplifier Design

The postamplifier must have a net phase shift of 180 degrees; it must be capable of delivering a negative-going 5 volt pulse across an external 3900 ohm load; and the gain must be large enough to achieve a low sensitivity to gain changes. The preamplifier is designed to deliver a positive voltage step of up to +1.0 volt, and this input should produce a -5 volt preamplifier output. For the external feedback circuits shown in Fig. 2.1, a positive unit step at the preamplifier input will produce an output pulse

$$v_o(t) = -\frac{R_2}{R_1}\frac{t}{\tau}e^{-\frac{t}{\tau}} \qquad (2.12)$$

provided $R_1C_1 = R_2C_2 = \tau$ and

[1] This confirms our hypothesis concerning the source of the excess noise reported in Quarterly 014393-5, Section 3.2.2.

$$A_2 >> 1 + R_2 \left(\frac{1}{4R_1} + \frac{1}{R_3}\right) \qquad (2.13)$$

The maximum amplitude of $v_o(t)$ is $0.368\ R_2/R_1$ volts, and if this is to be 5 volts, one requires $R_2 = 13.6\ R_1$, and the voltage gain should be large compared to $(4.4 + R_2/R_3)$. Typically in our designs R_2/R_3 lies in the range of 5 to 10 which implies a voltage gain large compared to 10 to 15.

The postamplifier design developed for this project is given in Fig. 2.8.[1] The circuit consists of a common-source output JFET, Q_1, driven by a source coupled pair, Q_3 and Q_2. Q_3, connected as a source follower, drives Q_2, which is a common-gate amplifier. The gate of Q_2 is held at a fixed potential by the diode string D_2, ..., D_7. In Fig. 2.8 the resistors R_S, R_F, and R_L as well as C_L are outside of the integrated circuit. The table in the figure lists the nominal zero bias currents and pinch-off voltages as well as the quiescent point currents for each transistor. The voltages on the circuit are the design quiescent values.

In the evolution of this design, we originally had a small JFET connected as a current source in place of the source resistor, R_4. The offset diode, D_1, was inserted to keep both this current source transistor and Q_2 out of

[1] The fabrication and testing of this circuit is described in Sections 3 and 4.

saturation. Subsequent analysis of the effect of transistor channel width changes showed that replacing the current source transistor with R_4 gave a design more tolerant of changes in transistor parameters.

The amplifier circuit given in Fig. 2.8 was analyzed with DCAP to verify both the large signal, and the incremental performance as a function of quiescent operating point and transistor channel width. As in the preamplifier design, the transistors were modeled as shown in Fig. 2.6. Figure 2.9 shows the calculated voltage transfer characteristics for nominal transistor parameters and for transistors whose undepleted channel widths are $\pm$10 percent, -20 percent and +15 percent of the nominal values. The calculations assume a 4 kilohm load and a very large coupling capacitor, C_L. Each transfer characteristic extends from near cut-off of Q_1 at large values of V_D^{Q1} to saturation of Q_1 at low values. With the nominal transistor parameters, for instance, the incremental voltage gain ranges from -115 at V_D^{Q1} = 6.5 volts to -252 between 4.8 and 2.3 volts, and it is back down to -132 between 2.3 and 1.0 volts.

This design accommodates the narrower channel widths without difficulty. The limitation for wider channels is saturation of transistor Q_2. With the channel width 15 percent above nominal, one can just achieve the 5 volt

output signal swing by placing the quiescent drain voltage of Q_1 at +6 volts.

The transfer characteristics plotted in Fig. 2.9 assume there are fixed supplies of +10 and -4 volts and that the chip substrate is tied to the -4 volt supply. The substrate can be operated, however, at any potential below the source potential of Q_2 and Q_3. If one is willing to accept a second negative supply potential, wider ranges of transistor parameters can be accommodated. Table 2.3 summarizes the currents furnished by each supply and the total quiescent power required by the postamplifier design. Also tabulated is the incremental voltage gain assuming the quiescent drain voltage for Q_1 is chosen at +6 volts.

Table 2.3 Calculated postamplifier performance with varying transistor parameters

Channel width	-20%	-10%	Nominal	+10%	+15%
Normalized V_p	0.64	0.81	1	1.21	1.32
Normalized I_{DSS}	0.512	0.73	1	1.33	1.52
Quiescent point values					
I^+ (mA)	0.507	0.492	0.490	0.530	0.510
I^- (mA)	0.390	0.435	0.487	0.542	0.573
Power dissipated in milliwatts	6.62	6.66	6.85	7.47	7.40
Voltage gain	-210	-124	-145	-140	-108

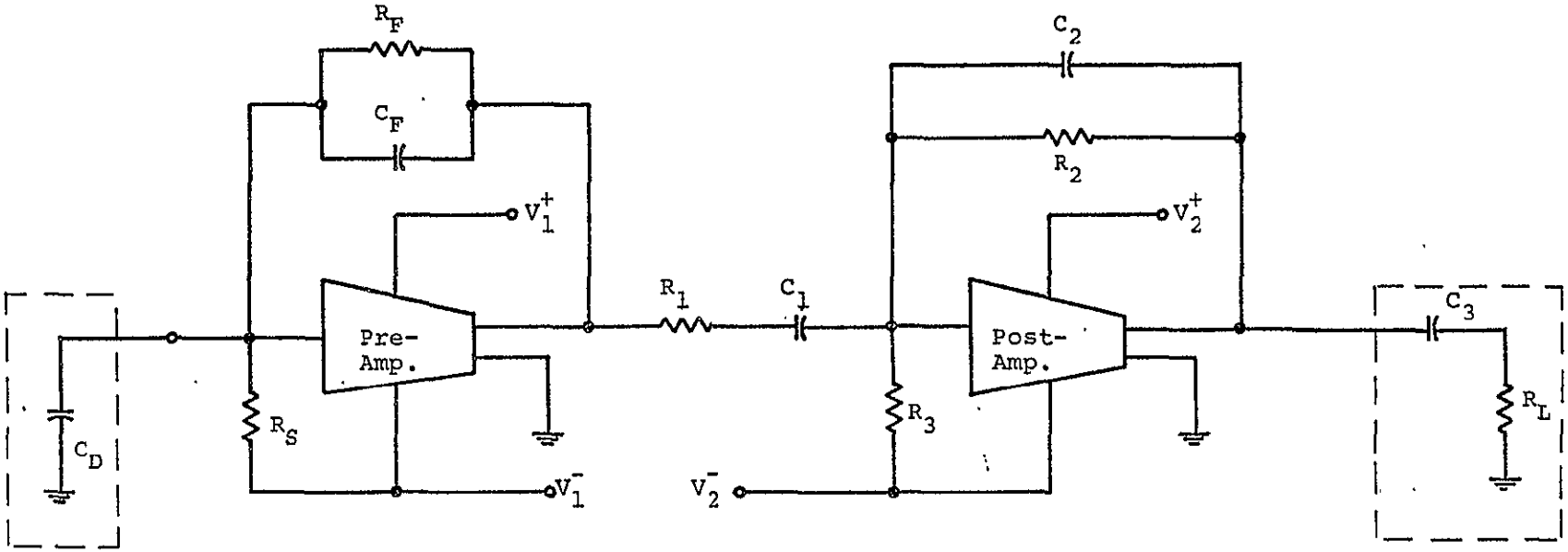


Fig. 2.1 Typical nuclear particle measurement system

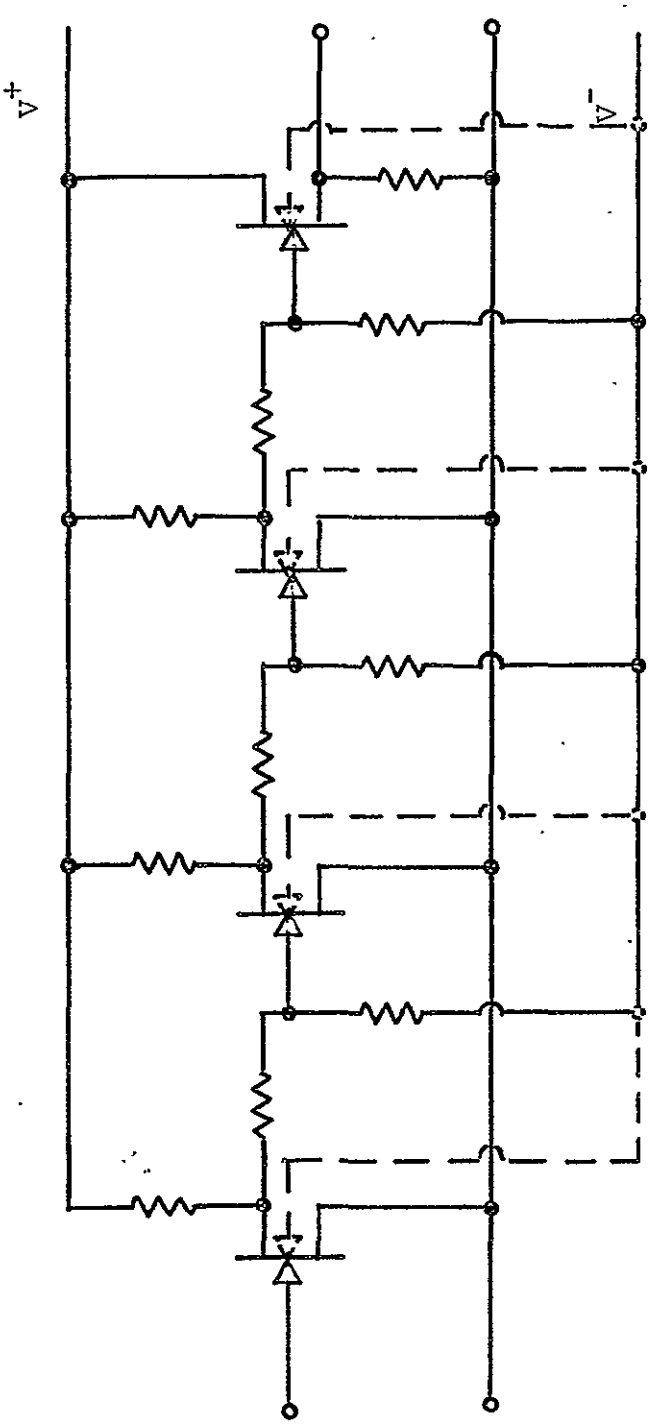


Fig. 2.2 Basic preamplifier circuit

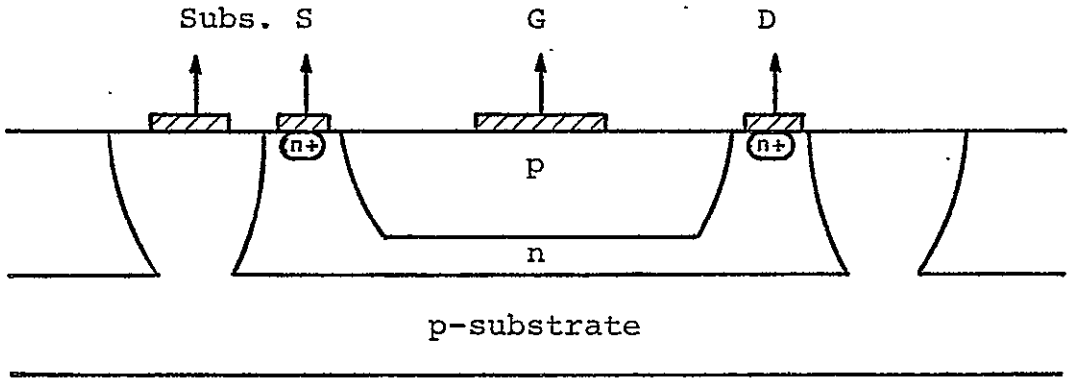
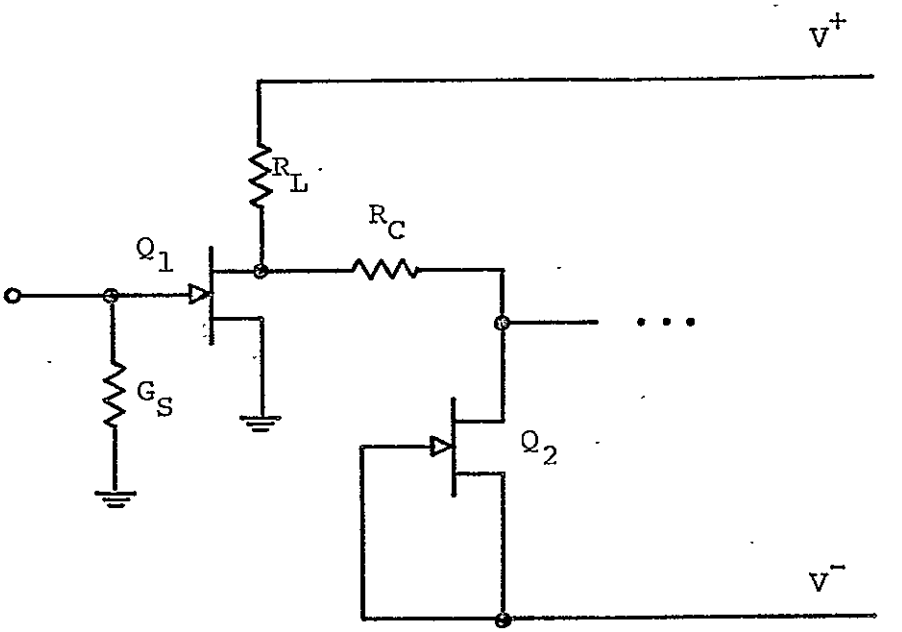
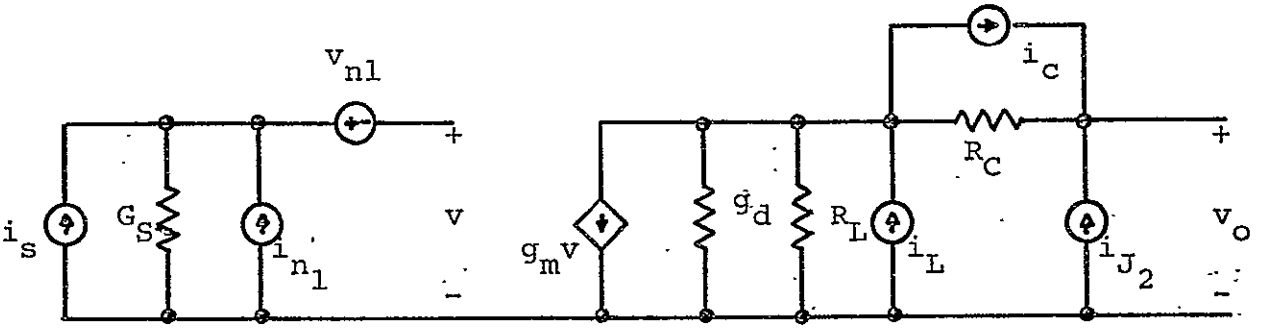


Fig. 2.3 Cross-section of a typical monolithic JFET



(a)



$1/R_L >> g_d$

$$\overline{v_{n_1}^2} = 4kTdf(K_1/g_{m_1}) = 4kTdfR_{nv}$$

$$\overline{i_L^2} = 4kTdf(1/R_L)$$

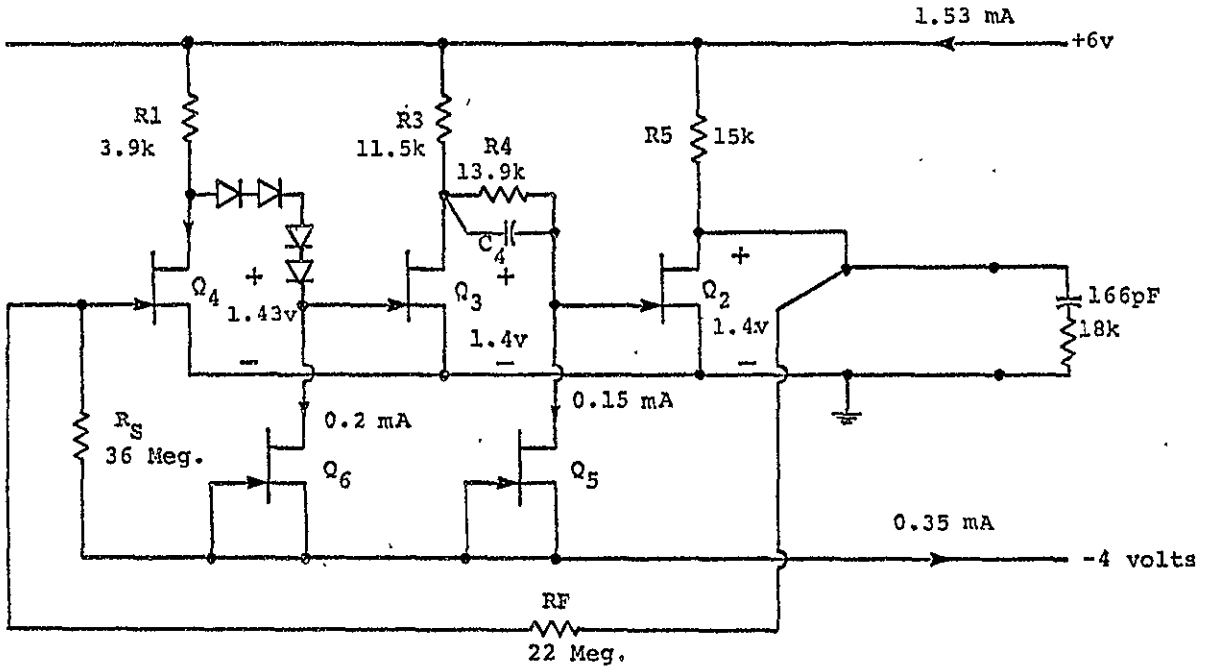
$$\overline{i_C^2} = 4kTdf(1/R_C)$$

$$\overline{i_{J_2}^2} = 4kTdfK_2 g_{m_2}$$

$$\overline{i_S^2} = 4kTdfG_S$$

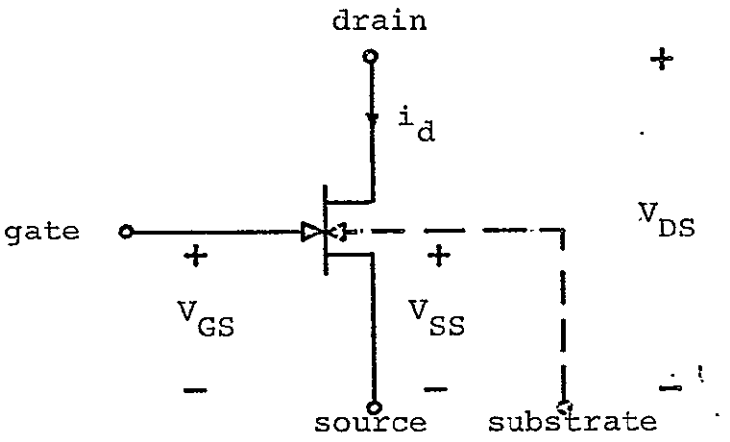
(b)

Fig. 2.4 (a) Preamplifier input circuits and
(b) Noise model of those circuits

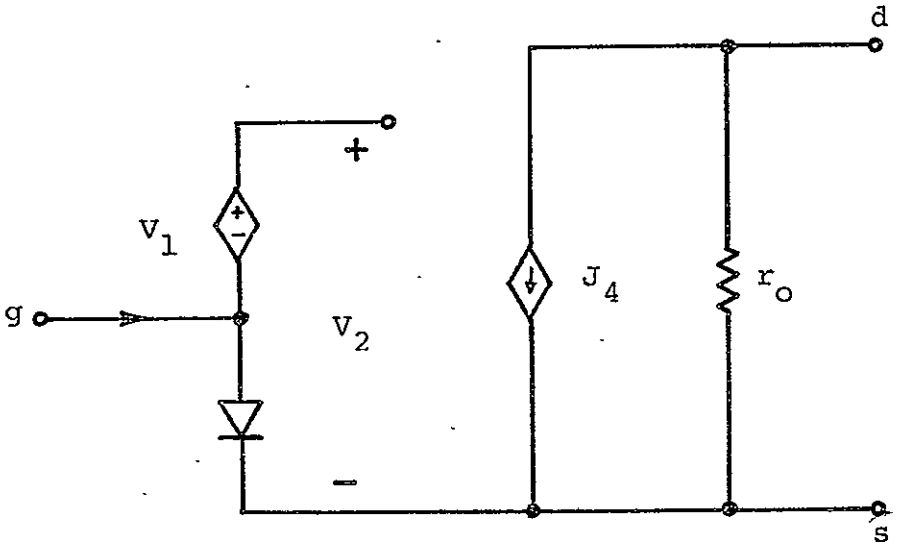


JFET No.	Q_2	Q_3	Q_4	Q_5	Q_6
I_{DSS} in mA	10.9	10.9	21.8	0.15	0.2
V_p in volts	-2.4	-2.4	-2.4	-2.4	-2.4
Quiescent i_D	0.307	0.25	0.97	0.15	0.20

Fig. 2.5 Monolithic JFET preamplifier design 4-B



(a)



(b)

$$V_1 = V_{SS}(V_{p_1}/V_{p_2})$$

$$J_4 = I_{DSS}\left(1 + \frac{V_2}{V_{p_1}}\right)^2 \quad ; \; V_{DS} \geq V_{p_1}+V_2$$

$$= I_{DSS}\left[2\left(1 + \frac{V_2}{V_{p_1}}\right)\frac{V_{DS}}{V_{p_1}} - \frac{V_{DS}^2}{V_{p_1}^2}\right]; \; V_{DS} < V_{p_1}+V_2$$

Fig. 2.6 (a) n-channel JFET with substrate gate
(b) dc analysis program model

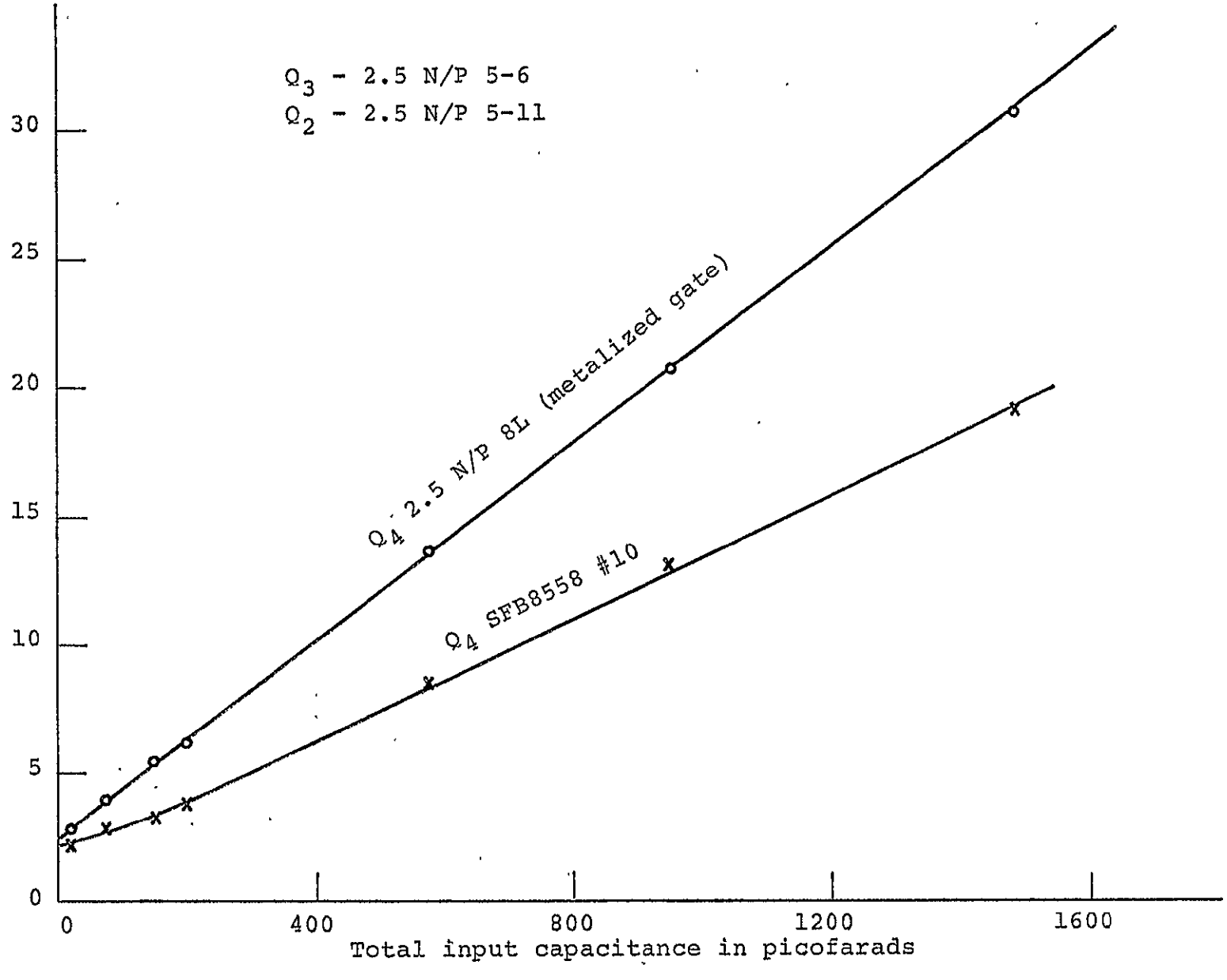
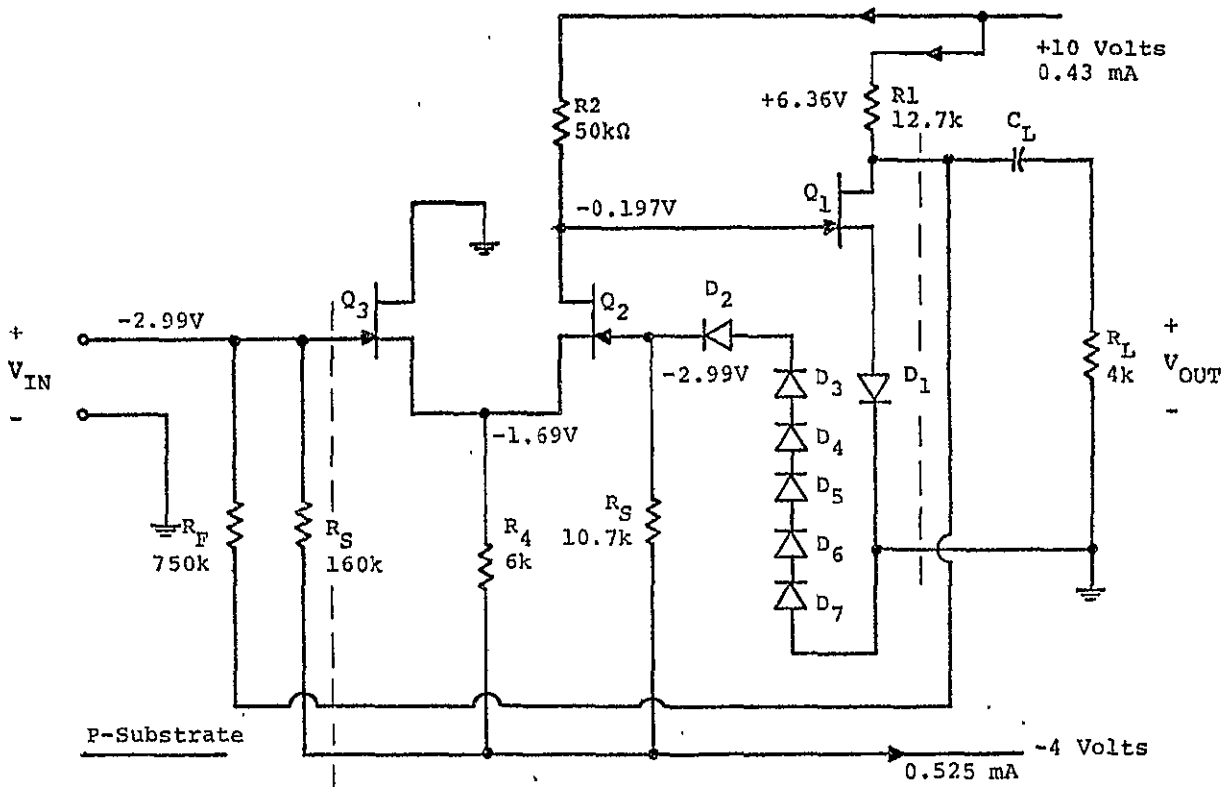


Fig. 2.7 Noise performance of preamplifier breadboard



JFET No.	Q_1	Q_2	Q_3	V_{SUBS}
I_{DSS1} in mA	21.8	10.9	10.9	0 V
V_{pl} in Volts	-2.4	-2.4	-2.4	0 V
i_D at Q point	0.23	0.2	0.2	-4 V

Fig. 2.8 Monolithic JFET postamplifier design 4

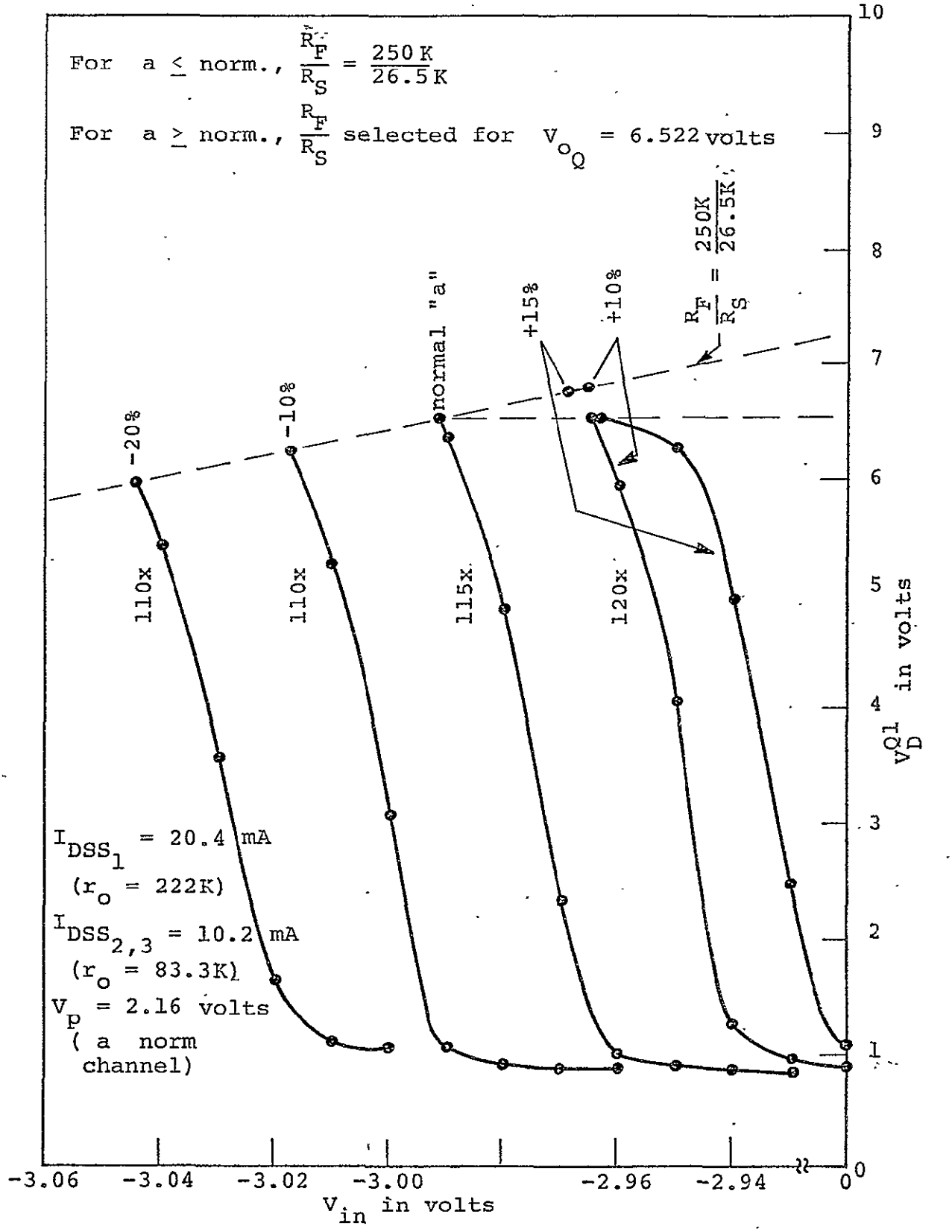


Fig. 2.9 Postamplifier; Q points and transfer characteristics (with 4 KΩ load)

III. EVALUATION OF FABRICATION PROCEDURE FOR NUCLEAR PARTICLE MEASUREMENT DC AMPLIFIER CIRCUIT

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Staff: W. W. Fisher

3.1 Introduction

The postamplifier and preamplifier circuits as designed for this program utilize JFET devices as the key active components in the circuits. Thus the entire fabrication procedure is centered around the requirements of the JFET structures. Two separate approaches are available for these circuits:

(a) A double-diffused technique in which the n-type diffusion is used to create the active source-drain channel region followed by a p^+ gate diffusion into the n-channel region. In this case the starting material is p/p^+ silicon.

(b) A single p-gate diffusion technique in which the starting wafer consists of an n-epitaxial layer on a p-substrate.

Both techniques have been utilized but the single-diffusion approach has been shown to be superior and thus was selected for the final fabrication procedure.

The initial investigations involved the fabrication and evaluation of discrete JFET structures in appropriate materials. The processing sequences were standardized to

yield devices with pinch-off voltages of ∿2 volts and I_{DSS} values of approximately 5-25 mA depending on the particular Z/L (gate width-to-length ratio) value for the individual JFET structures.

The effect of using a completely metallized diffused gate structure was also evaluated and found to be superior, in terms of noise performance, to the conventional unmetallized diffused-gate structure. The improved noise performance was a direct result of the lower series gate resistance of the metallized gate structure. However, the unmetallized gate structure was adequate for all of the JFET's except the preamplifier input transistor. Hence, for the two circuit designs, only the preamplifier input JFET structure made use of the metallized gate fabrication technique.

The postamplifier circuit was designed first, and an appropriate fabrication sequence was developed and used. During evaluation of the fabricated postamplifier circuits it became obvious that several of the processing steps could be improved despite the successful rf performance of the circuits. One of these modifications was incorporated into the final fabrication sequence for the preamplifier circuits.

3.2 Discussion of JFET Operation

An idealized JFET structure is illustrated in Fig. 3.1. This particular structure is symmetric with p-type gate regions on both sides of the conducting channel. Assuming the

doping concentration to be constant in the respective regions (i.e., a two-sided abrupt-junction structure) with N_d the channel doping concentration and N_A the gate doping concentration, the pinch-off voltage can be expressed as

$$V_p = -\frac{qa^2}{2\varepsilon_s} N_d\left(1 + \frac{N_d}{N_A}\right) + \frac{kT}{q} \ln \frac{N_d N_A}{n_i^2} \tag{3.1}$$

where $a \triangleq$ channel half-width,

$n_i \triangleq$ intrinsic carrier concentration in silicon at room temperature (1.45×10^{10} cm^{-3}),

$q \triangleq$ electron charge (1.6×10^{-19} coulombs),

and $\varepsilon_s \triangleq$ dielectric constant of silicon (1.04×10^{-12} f/cm).

When the voltage applied to the gate with respect to the source (i.e., the gate voltage, V_{Gs}) is equal to or more negative than V_p, the depletion region extends completely across the channel so that the conducting path disappears and the drain-source current I_D becomes zero. It should be noted that even with no gate voltage applied there is a finite depletion layer at the p^+-n interface as a result of the built-in potential difference between the p- and n-regions as given by

$$\psi_o = \frac{kT}{q} \ln \frac{N_d N_A}{n_i^2} \tag{3.2}$$

That is, even with no applied voltage the channel is at a potential of $+\psi_o$ with respect to the gate region.

The drain saturation current flow with $V_{GS} = 0$ is defined as I_{DSS} and can be written

$$I_{DSS} = \frac{q^2 \mu_n N_d^2 a^3}{3\epsilon_S} \frac{Z}{L}\left(1+\frac{N_d}{N_A}\right)\left[1-3\left|\frac{\psi_o}{W_o}\right| +2\left|\frac{\psi_o}{W_o}\right|\right]^{\frac{3}{2}} \qquad (3.3)$$

where $Z/L \triangleq$ width-to-length ratio of the gate region,

$\mu_n \triangleq$ electron mobility in the channel region,

and

$$W_o \triangleq V_p - \psi_o = - \frac{qa^2 N_d}{2\epsilon_S}\left(1+\frac{N_d}{N_A}\right)$$

In general, $N_d << N_A$ so that I_{DSS} tends to vary as $N_d^2 a^3$ while the pinch-off voltage V_p varies as $N_d a^2$. Thus for a given pinch-off voltage there is a fundamental limit on the product $N_d a^2$. This introduces a basic limit on I_{DSS} which can only be altered by changing the Z/L ratio. Hence the basic design procedure is to choose material with appropriate N_d and a values thus giving the desired pinch-off voltage. The necessary I_{DSS} value can then be obtained by choosing an appropriate Z/L factor; i.e., the device geometry is optimized.

It should be noted that the actual JFET structure as fabricated in monolithic form has the configuration illustrated in Fig. 3.2. For this case the n-channel region may be either the n-epitaxial layer of an n/p wafer or a diffused n-layer into a p/p^+ structure. Although both techniques were utilized during these investigations, the epitaxial channel

structure proved superior and hence the rest of these discussions will be confined to that configuration.

The isolation of each JFET from other components on the IC chip is achieved by first carrying out an isolation diffusion as illustrated in Fig. 3.2. This is followed by a p^+ gate diffusion and final n^+ contact diffusion to the source and drain regions. It should be noted that both the diffused p^+ gate and p-substrate serve as gates so that the channel can be pinched off from both directions. However, since the p-type doping concentration in the gate is much higher than that in the substrate, the upper diffused gate is much more effective in controlling the channel conductivity.

3.3 Investigation of Discrete JFET Structures

Several different JFET structures were evaluated during these investigations. For example, Fig. 3.3 illustrates a chip consisting of a simple JFET structure, an interdigitated JFET structure and a parallel JFET structure obtained by the single-gate diffusion technique. In addition there are several resistors formed during the p-gate diffusion step. Note that all of the resistors sit in a common n-epitaxial island while each of the JFET's are located in their own individual n-epitaxial islands. Note also that the JFET's have been fabricated as unmetallized gate structures in which gate contact is made to the gate region only at the gate contact pads.

The gates were formed by a p^+ diffusion into a thin n-type epitaxial layer with the epitaxial region serving as

the source, drain and channel regions. The starting material was n/p silicon with the n-type epitaxial layer being 2.5 μm thick and having a resistivity of 0.55 Ω-cm (i.e., $N_d \simeq 9 \times 10^{15}$ cm^{-3}). The devices were fabricated in a five-step masking operation as follows:

1. p-type isolation diffusion
2. p^+ gate diffusion
3. n^+ source and drain contact diffusion
4. contact opening
5. metal definition pattern

Devices fabricated from this mask set and silicon material have exhibited low junction leakage currents, good I-V characteristics and uniform V_p and I_{DSS} values across the entire wafer. Figure 3.4 illustrates the typical behavior of a reverse-biased parallel JFET gate-source junction. The low leakage current and sharp breakdown voltage indicate an excellent junction. Figure 3.5 illustrates the I-V drain characteristics of a typical parallel JFET structure. With the substrate grounded (i.e., at the same potential as the source), $V_p \simeq 2.4$ V and $I_{DSS} \simeq 23.5$ mA for these parallel devices which had Z/L ratios of 950.

Figure 3.6 illustrates the I-V drain characteristics of the interdigitated JFET structure again with the substrate grounded so that control of the channel conductance was influenced by the upper diffused gate only. The Z/L ratio for this structure was approximately 400 and $I_{DSS} \simeq 10.9$ mA.

The pinch-off voltage was consistent with those values which were typical for the parallel JFET structures described above.

After thorough evaluation of the various structures, it was decided to use the interdigitated JFET structure for the amplifier designs. The interdigitated structure is somewhat more efficient in the use of real estate thus requiring less chip area to obtain the same I_{DSS} value.

The final device design considered was that of a metallized-gate interdigitated JFET structure in which the entire gate was metallized (except for the source and drain cross-over regions). Although the unmetallized gate interdigitated structure was satisfactory for nearly all of the JFET's, the input JFET of the preamplifier required a metal gate to improve the noise performance. The unmetallized interdigitated JFET structure had an effective series gate resistance of about 6000 Ω . This created a problem for the preamplifier input JFET since the high gate resistance introduces a significant amount of thermal noise. Thus it was decided to design a metallized gate JFET structure and to evaluate its performance as compared with an identical unmetallized gate device.

Figure 3.7 illustrates the discrete device test chip for this evaluation. The chip contains other components (resistors and bipolar transistors) but the main interest focused

on the metallized-and unmetallized-gate JFET's as indicated. As expected, these JFET devices had similar V_p and I_{DSS} values and their I-V drain characteristics were essentially identical. However, the gate metallization resulted in a much lower series gate resistance; these devices, when used in a breadboarded preamplifier circuit, gave far superior noise performance when compared with the unmetallized structure. This improvement increased dramatically with current. For example, at a current of 0.35 mA, the unmetallized and metallized structures had equivalent noise values of 58 Kev and 41 Kev respectively when operated with a 1000 pF capacitor. When the current was increased to 0.95 mA, the corresponding figures became 54 Kev and 21 Kev, respectively. Hence, the gate metallization was demonstrated to be effective in allowing the stringent requirements of the preamplifier input transistor to be satisfied.

3.4 Postamplifier Fabrication

Figure 3.8 illustrates the circuit diagram for the final postamplifier design. The actual physical layout is illustrated in Fig. 3.9. (It should be noted that this layout, as well as the individual processing masks to be shown later, is the mirror image of the actual chip configuration. This is clearly seen by observing Fig. 3.10 which is a photograph of one of the fabricated postamplifier chips.) Each of the three JFET's is located in its own n-type epitaxial island. The resistors are all situated in a common epitaxial island

while the n-side of each diode is also isolated from every other circuit component.

Several processing sequences have been studied throughout the life of this contract. The final sequence selected involved a five-mask process allowing the simultaneous fabrication of single-diffusion n-channel JFET's, p-type diffused resistors and p-n diodes. The starting material was n/p epitaxial silicon with <111> orientation. This material has a 2.5 μm thick n-type epitaxial layer of ∿0.6 Ω-cm resistivity and a p-type substrate with a resistivity of 12-20 Ω-cm. The p-type isolation and gate resistor diffusions are carried out using a solid boron-nitride source wafer. The n^+ contact diffusion is accomplished with a liquid $POCl_3$ source bath through which N_2 and O_2 carrier gases are bubbled. The final complete processing sequence is as follows.

1. Preliminary wafer evaluation.
    a. The sheet resistance of the n-type epitaxial layer is measured using the 4-point probe system.
    b. Scribe the 2" wafers into smaller segments for processing.
    3. Measure the epitaxial layer thickness by angle-lapping and staining.
2. Wafer degreasing
    a. Boil wafers for 10 minutes in trichloroethylene.

b. Boil wafers for 10 minutes in acetone.

c. Boil wafers for 10 minutes in methanol.

3. Wafer cleaning.

a. Boil wafers for 10 minutes in 1:1 solution of H_2O_2 and H_2SO_4 .

b. Boil wafers for 10 minutes in 1:1 solution of H_2O_2 and NH_4OH.

c. Immerse wafers for 40 seconds in 20:1 solution of de-ionized water (DI-H_2O) and HF (deglaze step).

d. Blow wafers dry and place onto appropriate quartz boat for following furnace step.

4. Initial oxidation.

The oxidation furnace is set to a temperature of 1150° C and an O_2 flow rate of 125 cc/min is established. The temperature of the DI-water bubbler is set at 100° C.

a. Allow wafers to dry on boat at furnace mouth for 5 minutes.

b. Insert wafers into furnace for 10 minute initial dry oxidation.

c. Turn on bubbler and oxidize wafers in atmospheric steam for 10 minutes.

d. Turn off bubbler and continue to oxidize wafers in dry O_2 for 10 minutes.

e. Slowly pull wafers to furnace mouth and allow to cool for 5 minutes.

f. Remove wafers from quartz boat.

5. Photolithographic step to define pattern for isolation diffusion.

   a. Allow wafers to cool to room temperature under laminar flow hood.

   b. Spin-on 110 centistoke Kodak 747 negative photoresist for 30 seconds at 5000 rpm.

   c. Prebake the wafer in a covered petri dish for 12 minutes in the 60° C oven.

   d. Align wafer with isolation diffusion mask (Fig. 3.11(a)) and expose for ∿3 seconds to ultra-violet light.

   e. Develop for 30 seconds and rinse for 10 seconds.

   f. Postbake in covered petri dish for 15 minutes in 120° C oven.

   g. Coat wafer backs with photoresist and post-bake ∿5 additional minutes.

   h. Allow wafers to cool under laminar flow hood.

   i. Etch wafer oxide in buffer HF until windows are properly etched through the oxide.

   j. Remove photoresist by immersing wafers in hot J-100 resist stripper solution for ∿5 minutes.

   k. Rinse off J-100 in DI-water.

6. Isolation predeposition.

The boron predeposition furnace is set at 1050° C, and an N_2 flow rate of 1 lpm is established.

a. Clean wafers as in Step 3 and place on horizontal boron source boat.

b. Allow wafers to dry in furnace mouth for 5 minutes.

c. Insert wafers into furnace and diffuse for 15 minutes.

d. Slowly pull wafers to the furnace mouth and allow to cool for 5 minutes.

e. Immerse wafers into 10:1 (or stronger) solution of DI-H_2O and HF for 1 minute (or longer, if necessary) to remove boron nitrate layer.

f. Rinse wafers in DI-H_2O and blow dry with N_2.

g. Place wafers on boron drive-in boat.

7. Isolation drive-in and oxidation.

The boron drive-in furnace is set at 1150° C and an O_2 flow rate of 1 lpm is established. The DI-water bubbler is set at 100° C.

a. Allow the wafers to dry in the furnace mouth for 5 minutes.

b. Insert wafers in furnace for 10 minutes in dry O_2 flow.

c. Route O_2 gas flow through bubbler and continue diffusion for 10 minutes in atmospheric steam.

d. Re-route O_2 gas flow around bubbler and finish drive-in with 10 minutes in dry O_2 flow.

e. Turn off bubbler when no longer in use.

f. Slowly pull wafers to mouth of furnace and cool for 5 minutes.

g. Repeat photolithographic steps as in Step 5 above to define gate and resistor diffusion pattern (Fig. 3.11(b)).

8. Gate and resistor predeposition.

The boron predeposition furnace temperature is set at 1050° C, and an N_2 flow rate of 1 lpm is established.

a. Clean wafers as in Step 3 above and place on horizontal boron source boat.

b. Allow wafers to dry in furnace mouth for 5 minutes.

c. Insert wafers into furnace for 15 minutes.

d. Slowly return wafers to mouth of furnace and allow to cool for 5 minutes.

e. Deglaze wafers for 1 minute (or longer, if necessary) in a 20:1 solution of DI-H_2O and HF.

f. Rinse wafers in DI-H_2O and blow dry with N_2 .

g. Place wafers on boron drive-in boat.

9. Gate and resistor drive-in.

The boron drive-in furnace temperature is set at 1100°C with an O_2 flow rate of 1 lpm. The DI-water bubbler temperature is established at 100° C.

a. Allow wafers to dry in furnace mouth for 5 minutes.

b. Insert wafers in furnace for 5 minutes in dry O_2 .

c. Turn on bubbler and continue drive-in for 10 minutes in atmospheric steam.

d. Turn off bubbler and drive-in an additional 10 minutes in dry O_2 .

e. Slowly return wafers to furnace mouth and allow to cool for 5 minutes.

f. Photolithographically define n^+ contact diffusion pattern as in step 5 above (Fig. 3.11(c)).

10. N^+ contact diffusion predeposition.

The phosphorus predeposition temperature is set at 1050° C with 1 lpm of N_2 flowing. O_2 is to be added later. Ice is placed around the $POCl_3$ bubbler.

a. Clean wafers as in Step 3 and place on phosphorus predeposition boat.

b. Allow wafers to dry in furnace mouth for 5 minutes.

c. Insert wafers into furnace with 1 lpm of N_2 flowing.

d. After 1 minute, turn on 20 cc/min of O_2 and turn on $POCl_3$ bubbler.

e. Leave $POCl_3$ bubbler on for 5 minutes.

f. After 5 minutes turn off $POCl_3$ bubbler and turn off O_2 gas flow.

g. Continue predeposition for 10 minutes (a total of 15 minutes from time $POCl_3$ bubbler is turned on).

h. Slowly pull wafers to mouth of furnace and allow to cool for 5 minutes.

i. Deglaze wafers for 40 seconds (or longer, if necessary) in 20:1 solution of DI-H_2O and HF.

j. Rinse wafers in DI-H_2O and blow dry with N_2 .

k. Place wafers on phosphorus drive-in boat.

11. N^+ contact diffusion drive-in.

The phosphorus drive-in furnace is set at 1000° C with 1 lpm of O_2 flowing. The DI-water bubbler temperature is established at 100° C.

a. Allow wafers to dry in furnace mouth for 5 minutes.

b. Insert wafers into furnace for 5 minutes in dry O_2 .

c. Turn on bubbler and continue oxidation for 15 minutes in atmospheric steam.

d. Turn bubbler off and continue for 5 minutes in dry O_2 .

e. Slowly return wafers to furnace mouth and let cool for 5 minutes.

f. Photolithographically define the contact window pattern as in Step 5 (Fig. 3.11(d)).

12. Metallization

a. Clean wafers as in Steps 3 a-c.

b. Blow the wafers dry.

c. Metallize both sides of the wafers with a layer of Cr followed by a layer of Au.

d. Coat wafer backs with Shipley AZ-1350 photoresist.

e. Electroplate wafers in gold-plating solution until a plated-gold thickness of $\geq$ 1 μm is achieved. (The plating operation will typically require ∿15 minutes at a current of 1.5 mA in a 65° C plating-bath solution.

f. Remove photoresist in boiling acetone for 5 minutes.

g. Repeat the photolithographic pattern definition Steps 5 a-h using the metallization mask (Fig. 3.11(e)).

h. Immerse wafers in gold etch for 10-15 seconds as necessary to define gold pattern.

i. Rinse wafer in DI-water.

j. Remove photoresist in hot J-100 resist stripper solution for 5 minutes.

k. Immerse wafers for 60 seconds in warm chrome etch until unwanted chrome layer is removed.

l. Rinse wafers in DI-water and blow dry with N_2.

The above procedure has resulted in the successful fabrication of numerous postamplifier circuits. As discussed elsewhere in this report, the best of these postamplifiers have met the rf performance requirements quite satisfactorily. However, the operation of the units resulted in excessive supply current flow and power consumption. This was traced to several "weaknesses" in the fabrication processing sequence.

The first problem area was related to the way in which the resistors were formed. They are fabricated by using the same p-diffusion step as is used in creating the transistor gate regions. Thus the cross-sectional structures of resistors R_1 and R_2 are as illustrated in Fig. 3.12. Note that the voltage at one end of the resistor is at +10 V (along with the n-epitaxial island) while the p-substrate is at -4 V. Thus the 14 volt difference in potential may be sufficient to allow the depletion region around the resistor to extend down to the substrate and cause a punch-through condition in which the resistor latches-up directly to the substrate.

When this occurs at the power supply end of the resistor, the amplifier still operates as planned but there is an extra parasitic current flow from the positive supply to the negative supply. This problem can be overcome in the future by fabricating the resistors with a shallower p-type diffusion separate from the deeper p-type gate diffusion step. This punch-through condition can also be minimized or eliminated by reducing the power-supply voltages.

The second factor which contributes to the high current/power requirements of the postamplifier design is related to the manner in which the diodes are fabricated. As illustrated in Fig. 3.13, the diodes are formed by diffusing p-regions into isolated n-epitaxial regions. When the diodes are operating as planned with the p-n junctions forward biased, each diode also acts as a vertical pnp transistor in the active biasing mode. That is, the p-type substrate is reversed biased with respect to the n-epitaxial island which serves as the base. Thus current is injected from the forward-biased emitter (diffused p-type region) into the reversed-biased collector (substrate). As in the case of the resistor punch-through phenomena, the currents from diode D_2 , ..., D_7 do not have a direct effect on the amplifier's characteristics, but they do increase the bias current which must be delivered by the negative supply. This problem can be overcome by altering the fabrication sequence so that

n-p-n bipolar transistors are formed instead of p-n diodes This requires that the p-diode diffusion be followed by an n^+ emitter diffusion into the diffused p-region. A diode can then be formed by connecting the p-type base to the n-epitaxial collector thus forming one side of the diode, and using the n^+-side of the diode junction as the emitter region. A typical diode fabricated in this way would have the form illustrated in Fig. 3.14.

3.5 Preamplifier Fabrication

The schematic diagram for the preamplifier circuit is illustrated in Fig. 3.15 while the corresponding physical layout is shown in Fig. 3.16. Table 3.1 contains design and fabrication information relevant to the preamplifier. Since the supply voltages for this circuit are less than those for the postamplifier, the resistor punch-through problem should not occur. Hence these resistors are again formed simultaneously with the gate diffusion step.

The diode fabrication sequence, however, has been modified in accordance with the discussion above. The diodes are formed in the manner illustrated in Fig. 3.14. The fabrication sequence is identical with that of the postamplifier with the exception that the n^+ contact diffusion is also introduced into the center of the p-type diffused diode regions thus creating the bipolar n-p-n transistor structures which are connected as diodes by the metallization step.

Table 3.1 Design and fabrication information for the JFET preamplifier integrated circuit

Resistor	Nominal Value	Z/L
R_1	3900 Ω	68.7
R_3	11500 Ω	201.7
R_4	13900 Ω	243.9
R_5	15000 Ω	263.5

Used R_S=57Ω/

JFET	Z/L
Q_2	383
Q_3	377
Q_4	753.7
Q_5	5
Q_6	7

Isolation Region:
62.6 mils x 67.3 mils

Isolation and Bonding Pads:
69.9 mils x 67.3 mils

Region Inside Scribe Lanes:
71.8 mils x 71.1 mils

Step and Repeat Spacing:
75 mils x 75 mils

Note:
Put isolation region on both isolation and gate mask.

Figure 3.17 illustrates the series of masks used during the fabrication sequence. Again the process consists of five masking steps:

1. Isolation diffusion (p-type)
2. Gate/resistor/diode diffusion (p-type)
3. Contact/emitter diffusion (n-type)
4. Contact openings
5. Metal pattern definition

Several wafers were processed using the prescribed masks and fabrication schedule. A typical fabricated circuit is illustrated in Fig. 3.18.

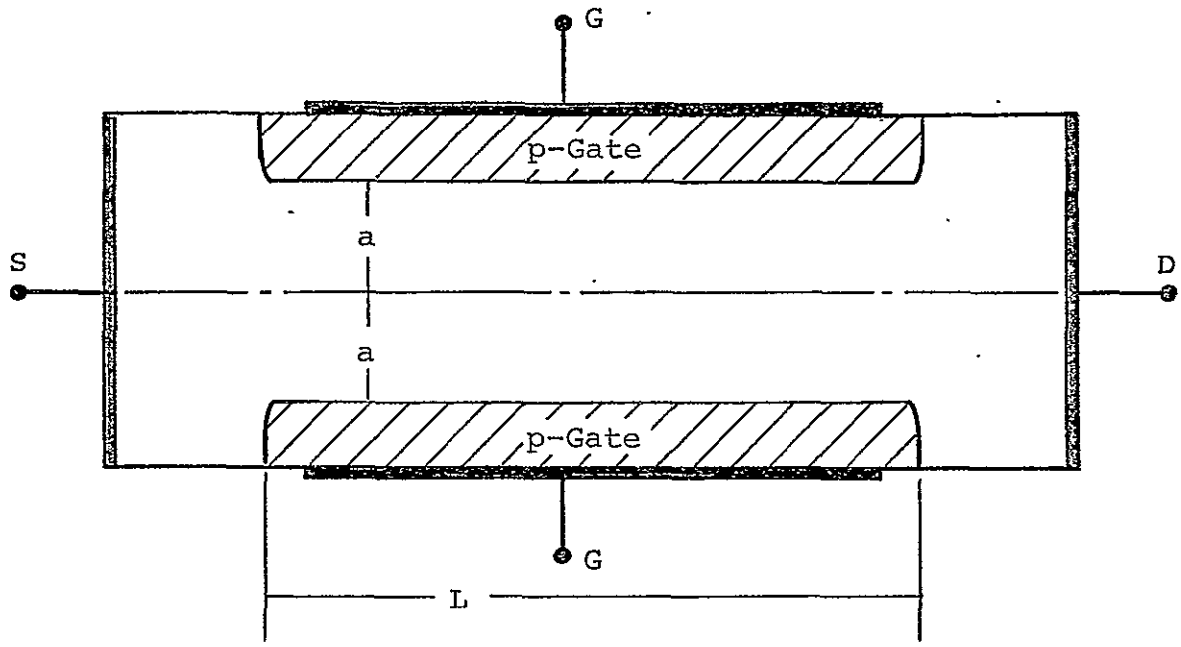


Fig. 3.1 Idealized two-gate n-channel JFET structure

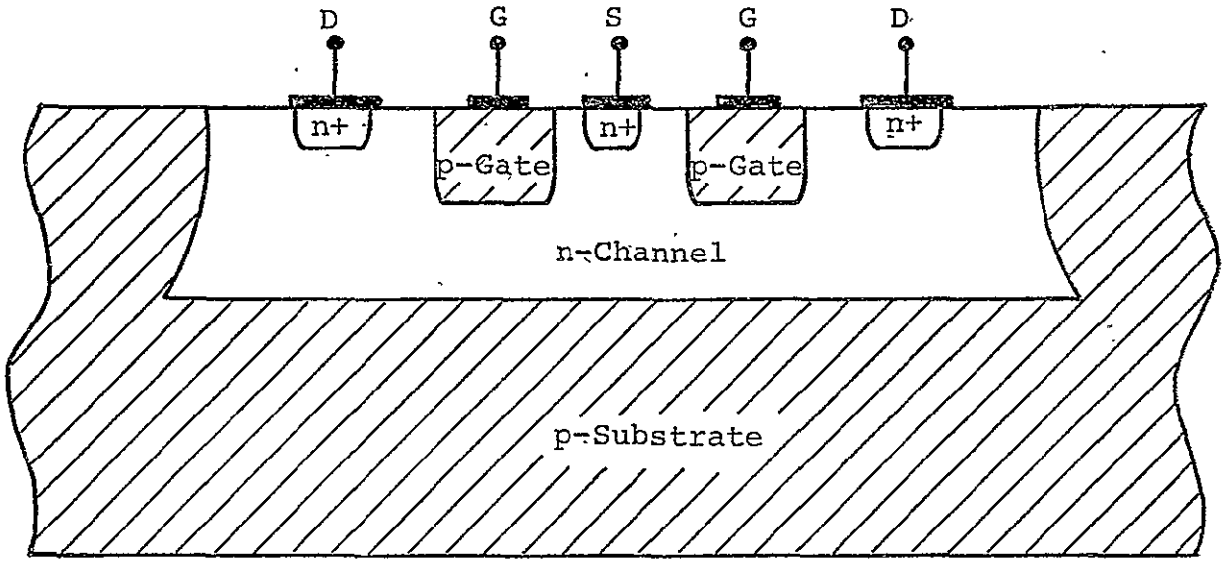


Fig. 3.2 Typical n-channel JFET configuration obtained by monolithic integrated-circuit fabrication

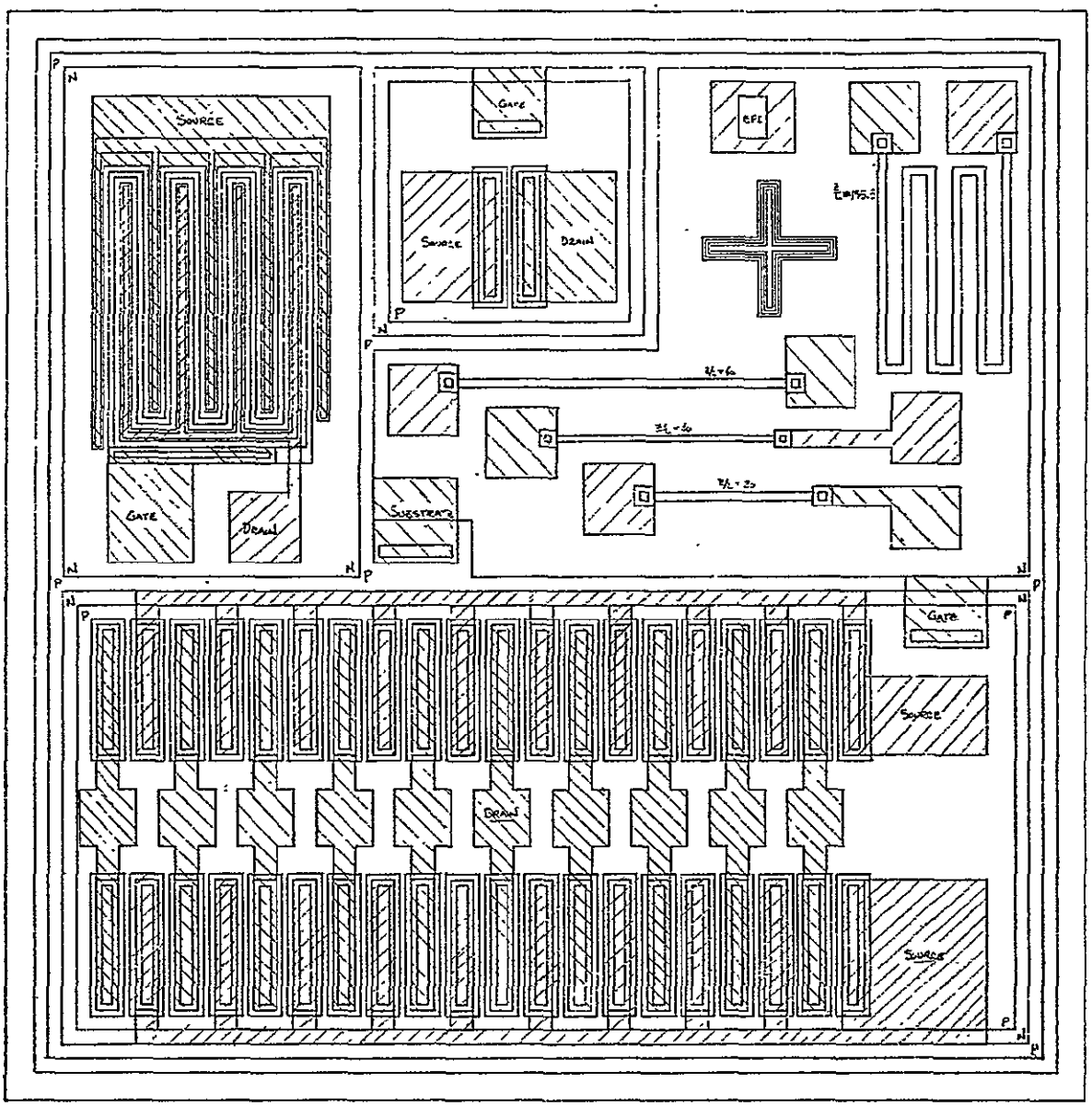


Fig. 3.3 Layout of experimental chip for single-diffusion JFET's and resistors; interdigital JFET and simple parallel JFET - top left; parallel JFET - bottom; and resistors - top right

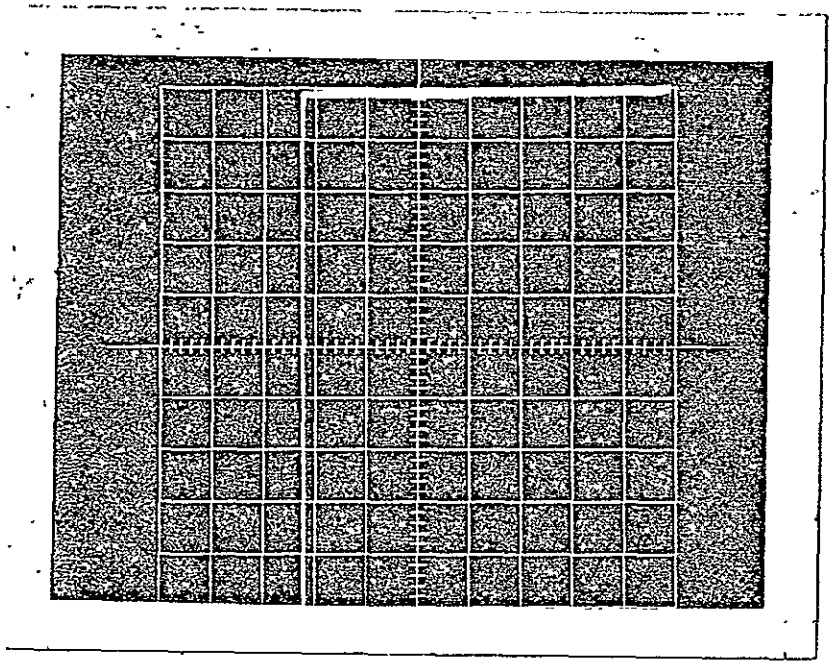


Fig. 3.4 I-V characteristics of the reverse-biased p-n junction between the gate and source region of a parallel JFET. (0.01 mA/DIV, 5 V/DIV)

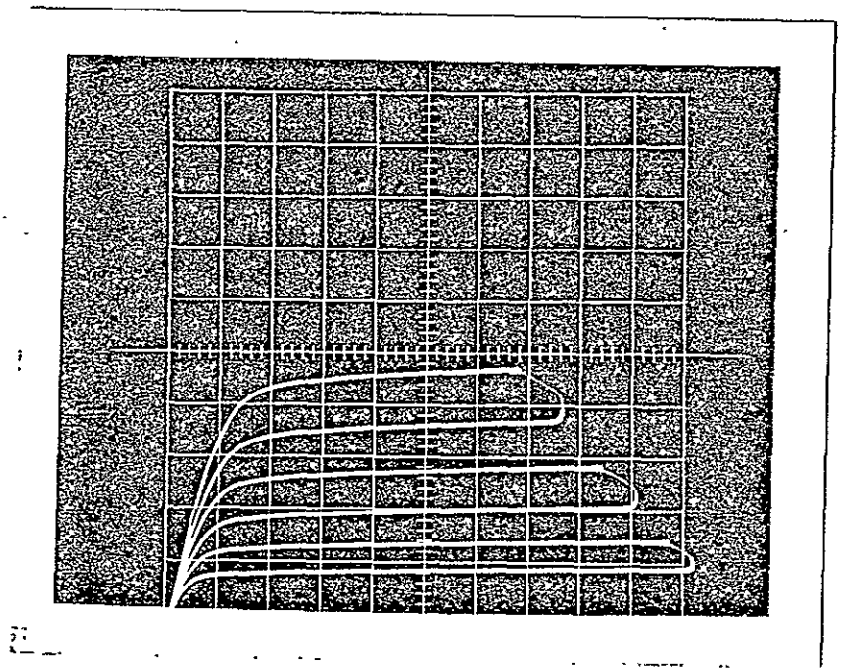


Fig. 3.5 I-V drain characteristics of a full parallel JFET with substrate and top gate connected. (5 mA/DIV, 1 V/DIV, 0.2 V/Step)

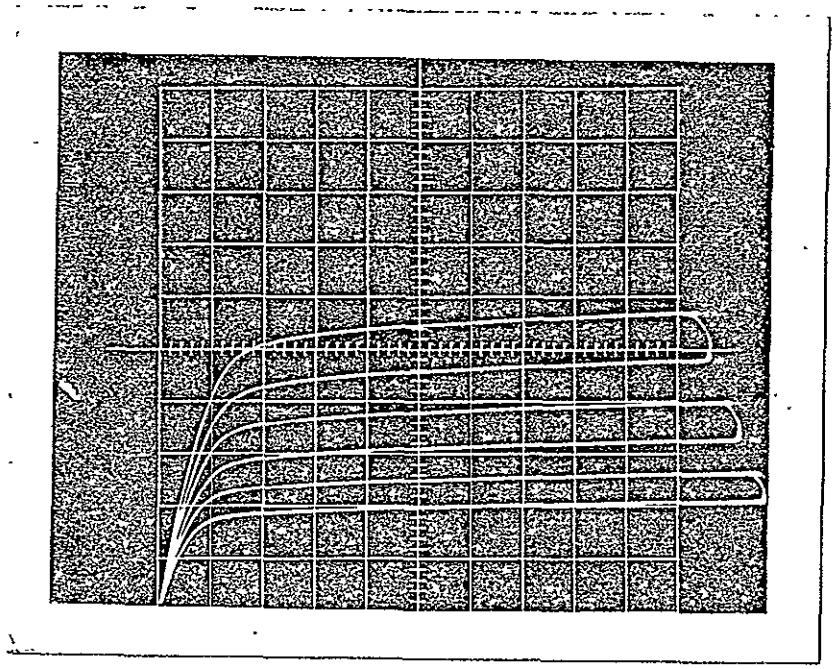


Fig. 3.6 I-V drain characteristics of an interdigitated JFET with grounded substrate. (2 mA/DIV, 1 V/DIV, 0.2 V/Step)

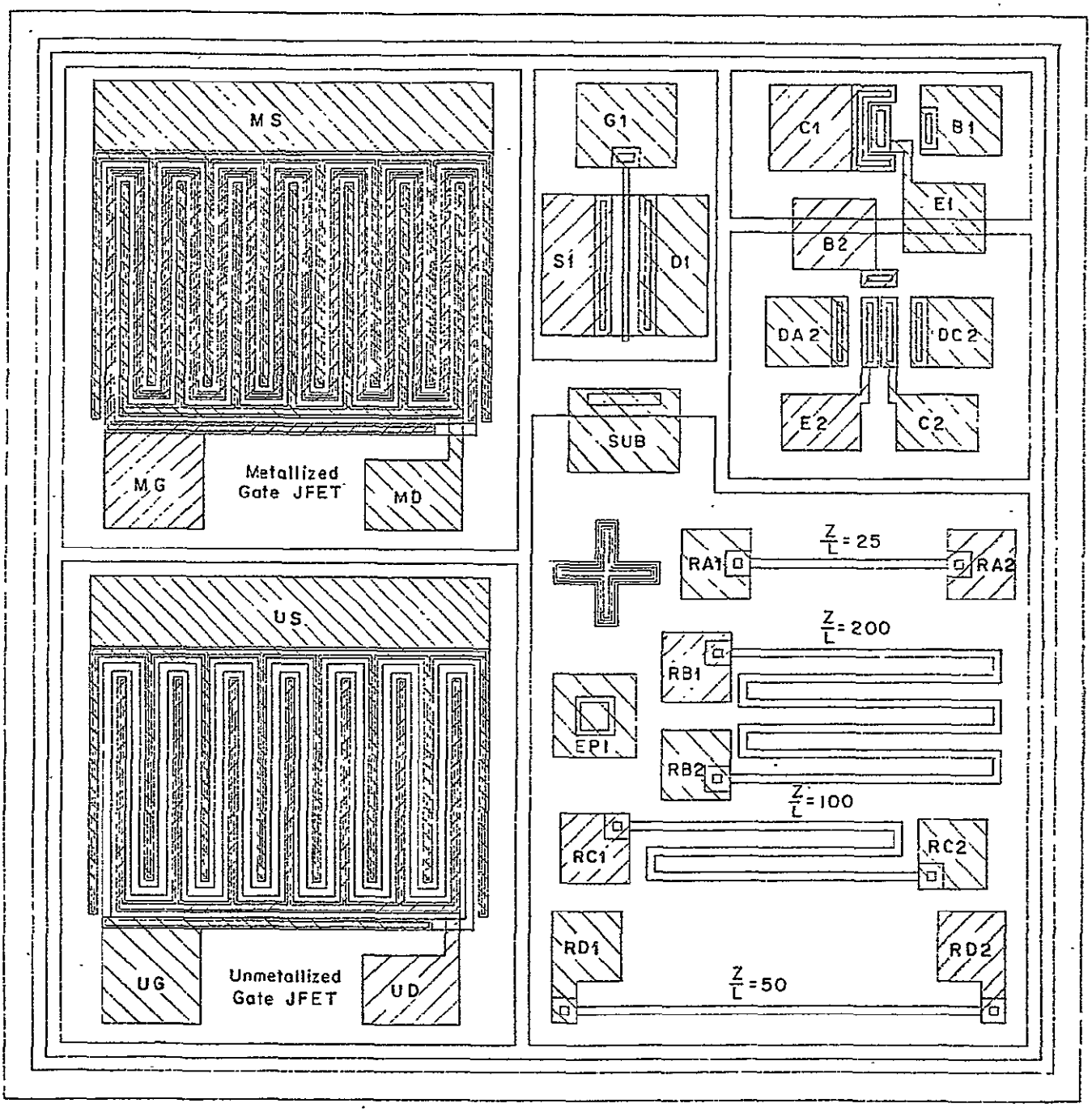
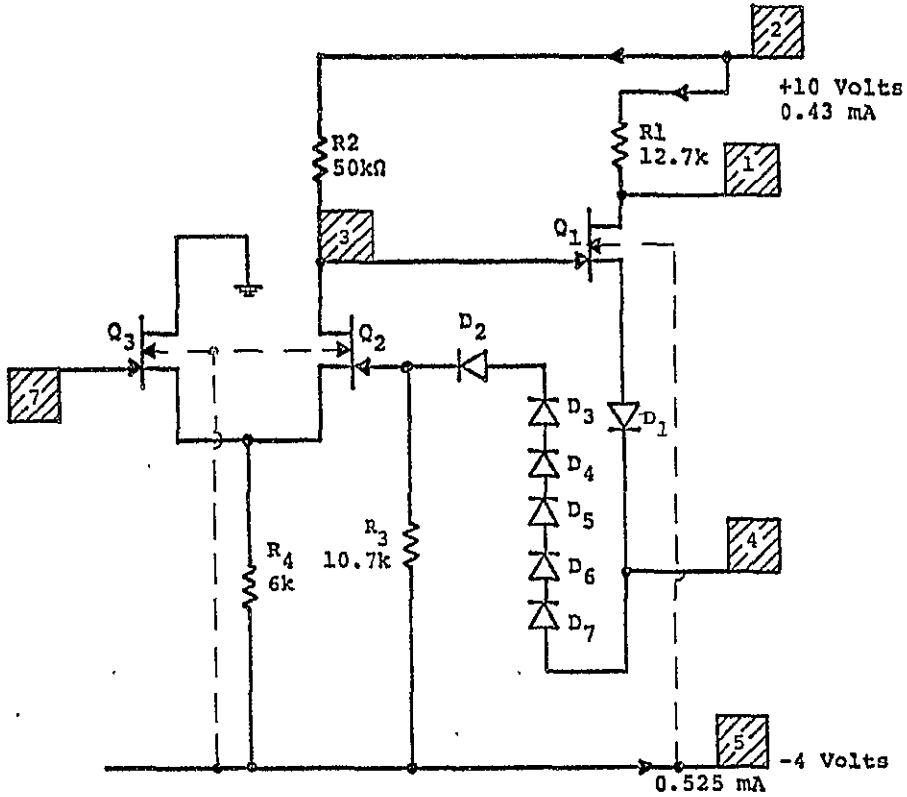


Fig. 3.7 IC chip fabrication for evaluation of completely metallized gate on JFET performance



JFET No.	Q_1	Q_2	Q_3	V_{SUBS}
I_{DSS1} in mA	21.8	10.9	10.9	0 V
V_{p1} in Volts	-2.4	-2.4	-2.4	0 V
i_D at Q point	0.23	0.2	0.2	-4 V

Fig. 3.8 Final circuit design for JFET postamplifier integrated circuit

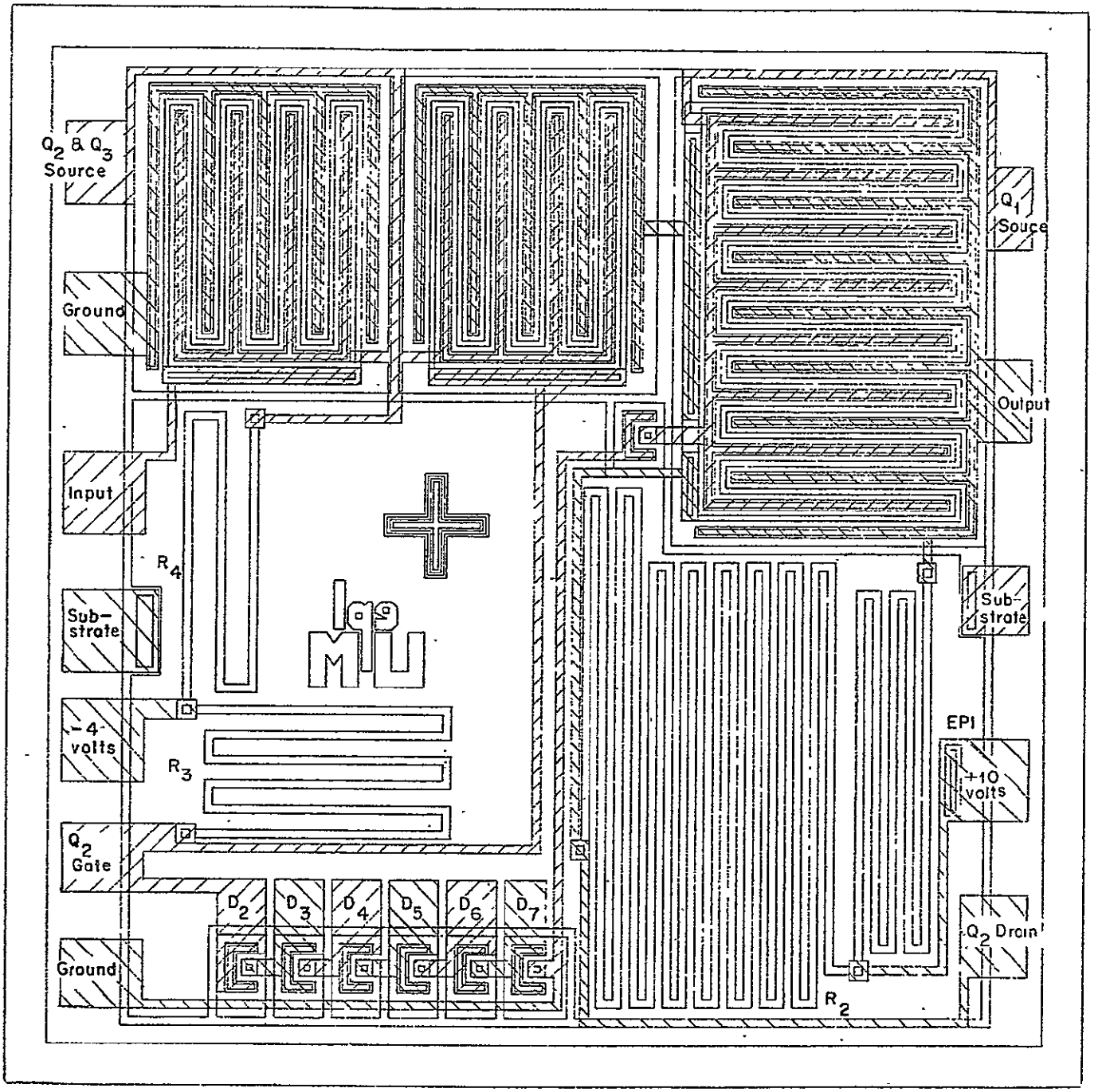


Fig. 3.9 Physical layout of the JFET postamplifier circuit

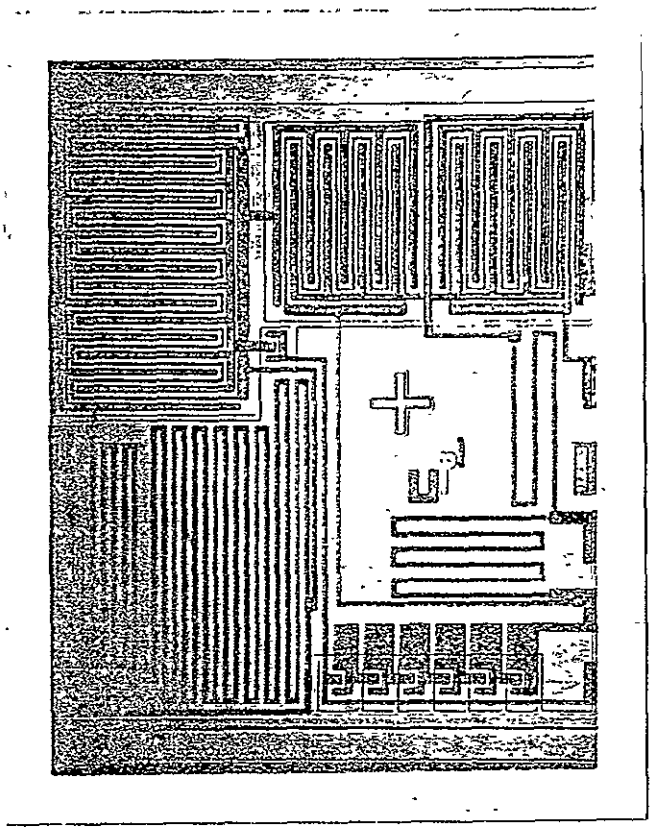
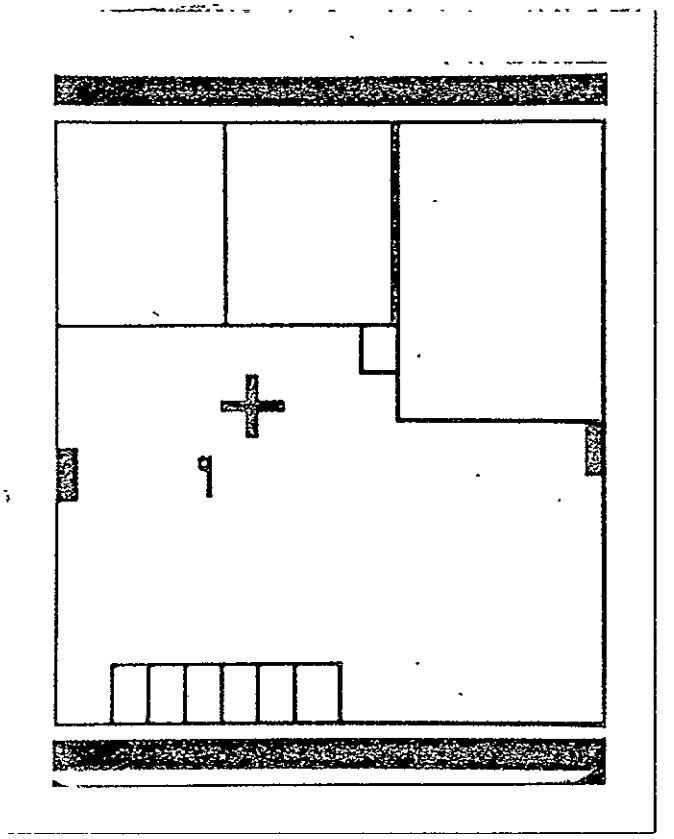
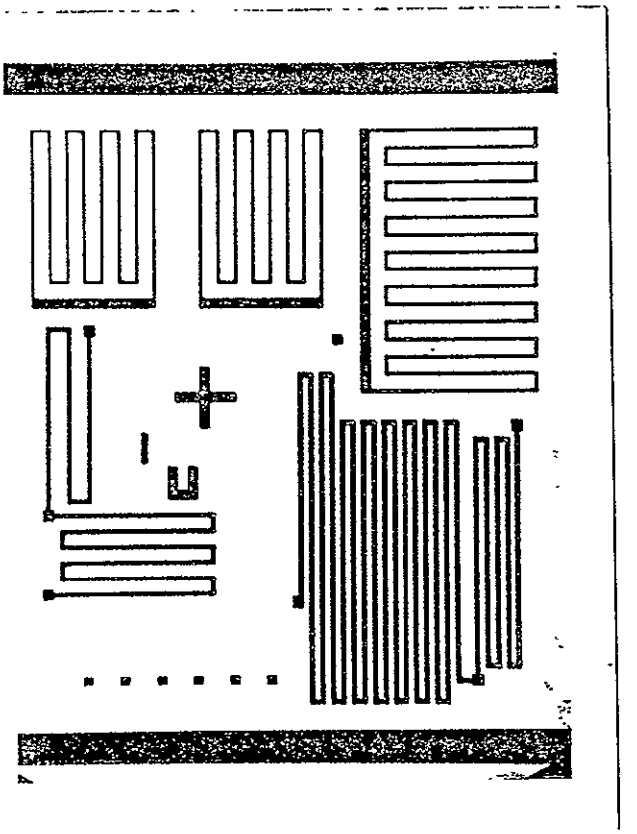


Fig. 3.10 Photograph of fabricated JFET postamplifier circuit

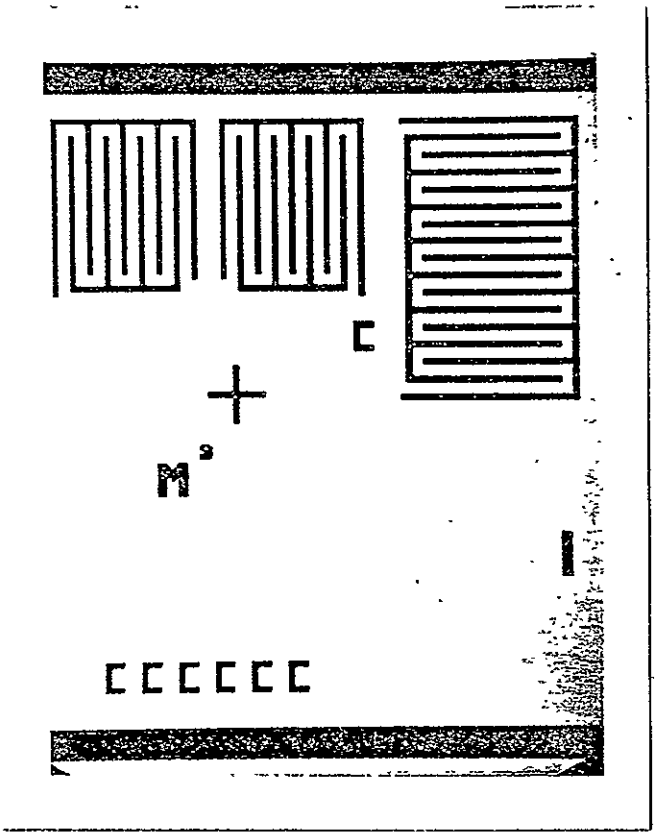


(a)

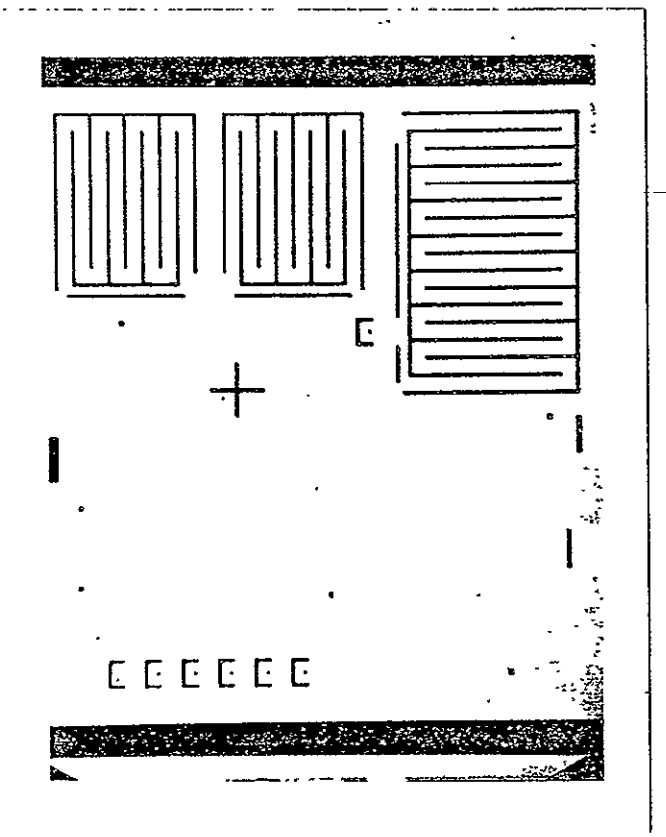


(b)

Fig. 3.11 Mask patterns used for the IC fabrication of the JFET postamplifier circuit
(a) Isolation diffusion mask
(b) Gate/resistor diffusion mask

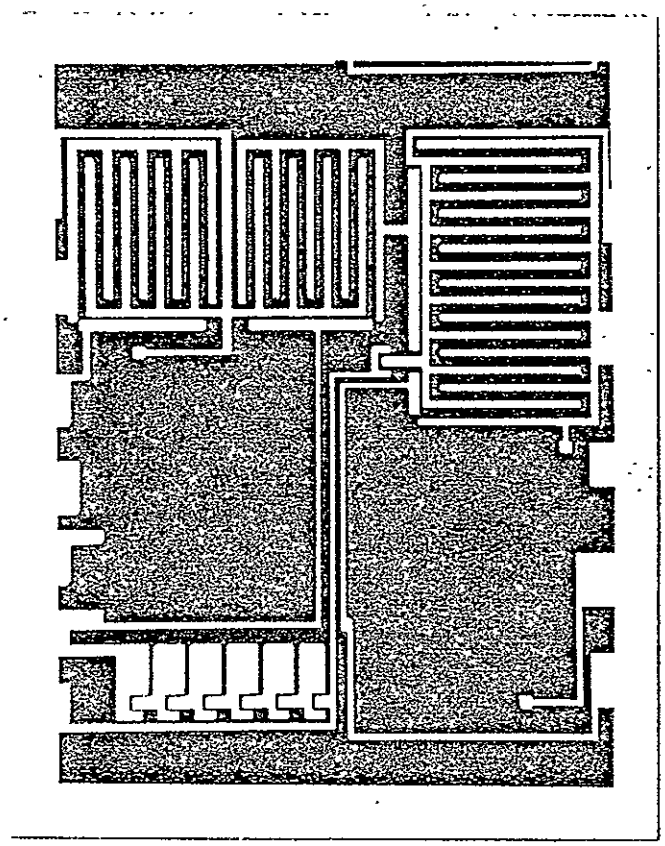


(c)



(d)

Fig. 3.11 (Cont.)
(c) n^+ contact diffusion mask
(d) Metal pattern mask



(e)

Fig. 3.11 (Cont.)
(e) Metal pattern mask

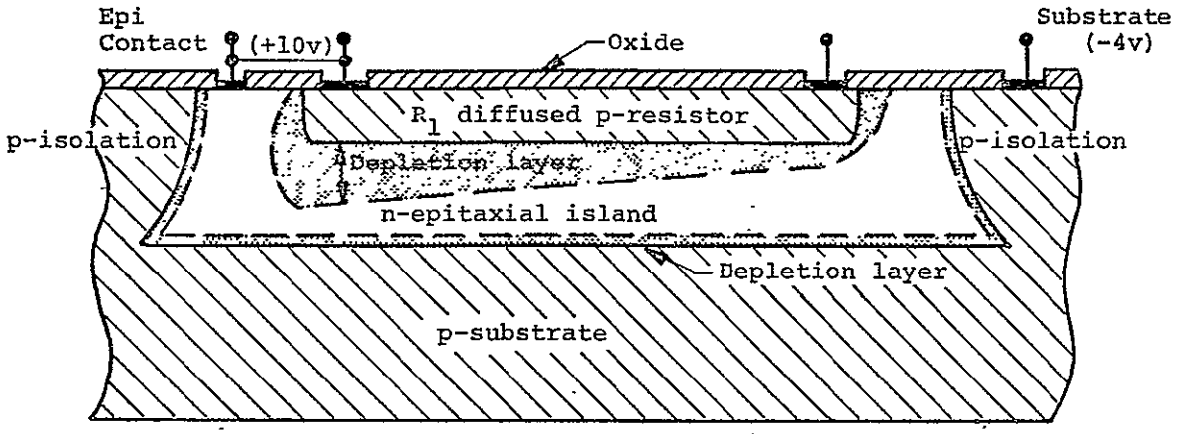


Fig. 3.12 Cross-sectional view of diffused resistor R_1 which has one terminal connected to the +10V potential of the n-epitaxial island

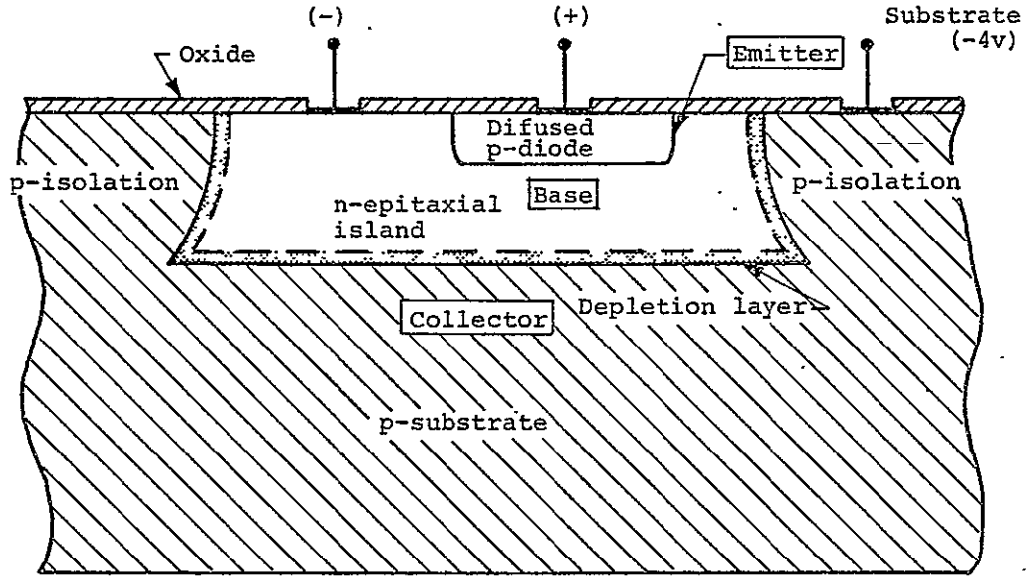


Fig. 3.13 Cross-sectional view of single diffused diode structure illustrating the vertical pnp structure when the diffused p-layer-n-epi junction is forward biased

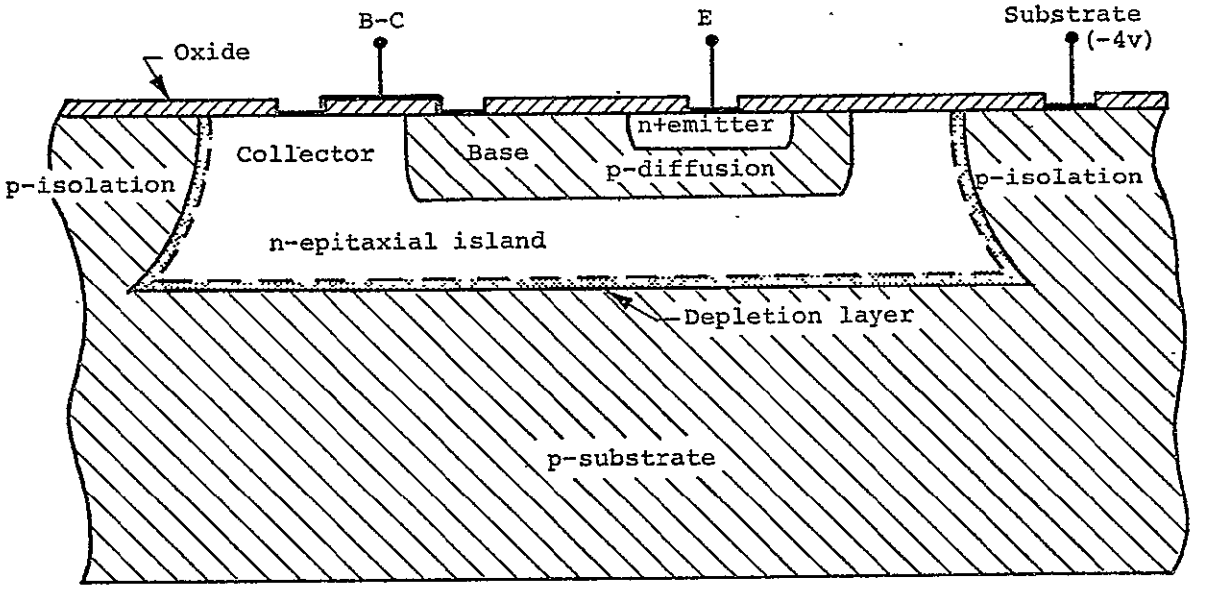
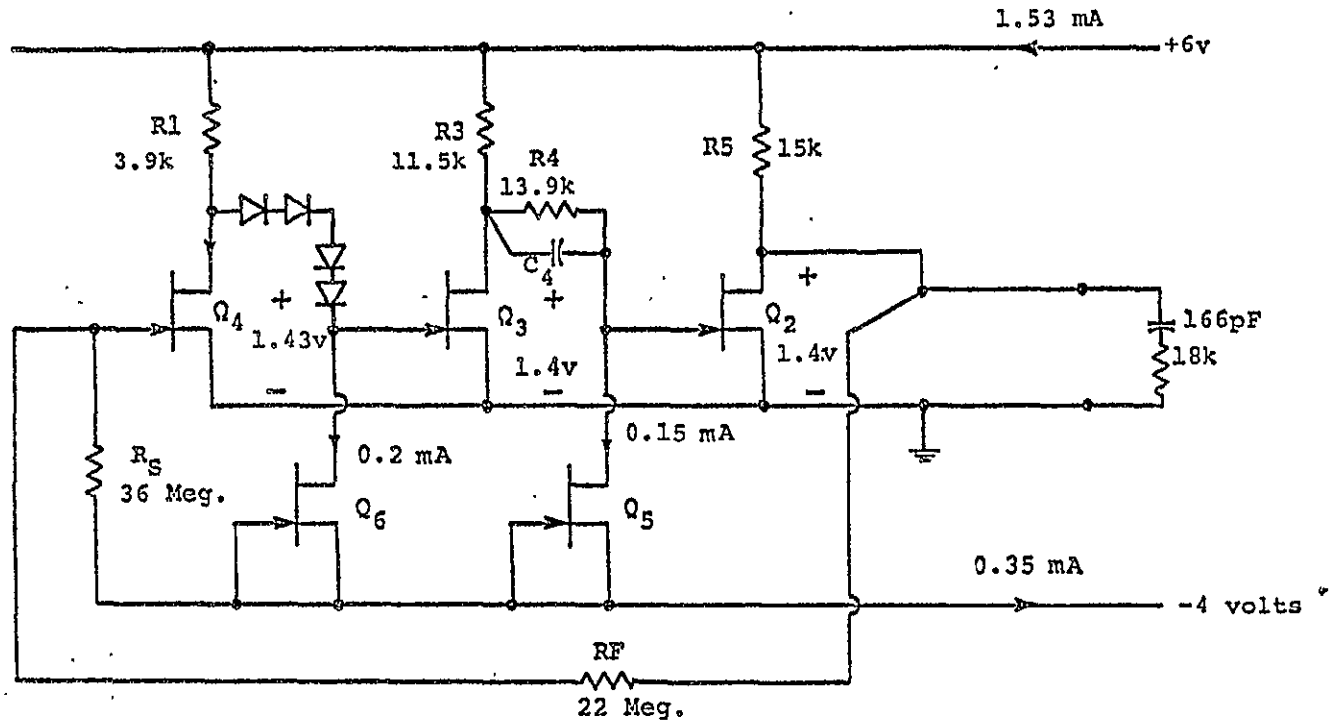


Fig. 3.14 Diode structure formed by shorting the collector and base regions of a conventional npn bipolar transistor



JFET No.	Q_2	Q_3	Q_4	Q_5	Q_6
I_{DSS} in mA	10.9	10.9	21.8	0.15	0.2
V_p in volts	-2.4	-2.4	-2.4	-2.4	-2.4
Quiescent i_D	0.307	0.25	0.97	0.15	0.20

Fig. 3.15 Final circuit design for JFET preamplifier integrated circuit

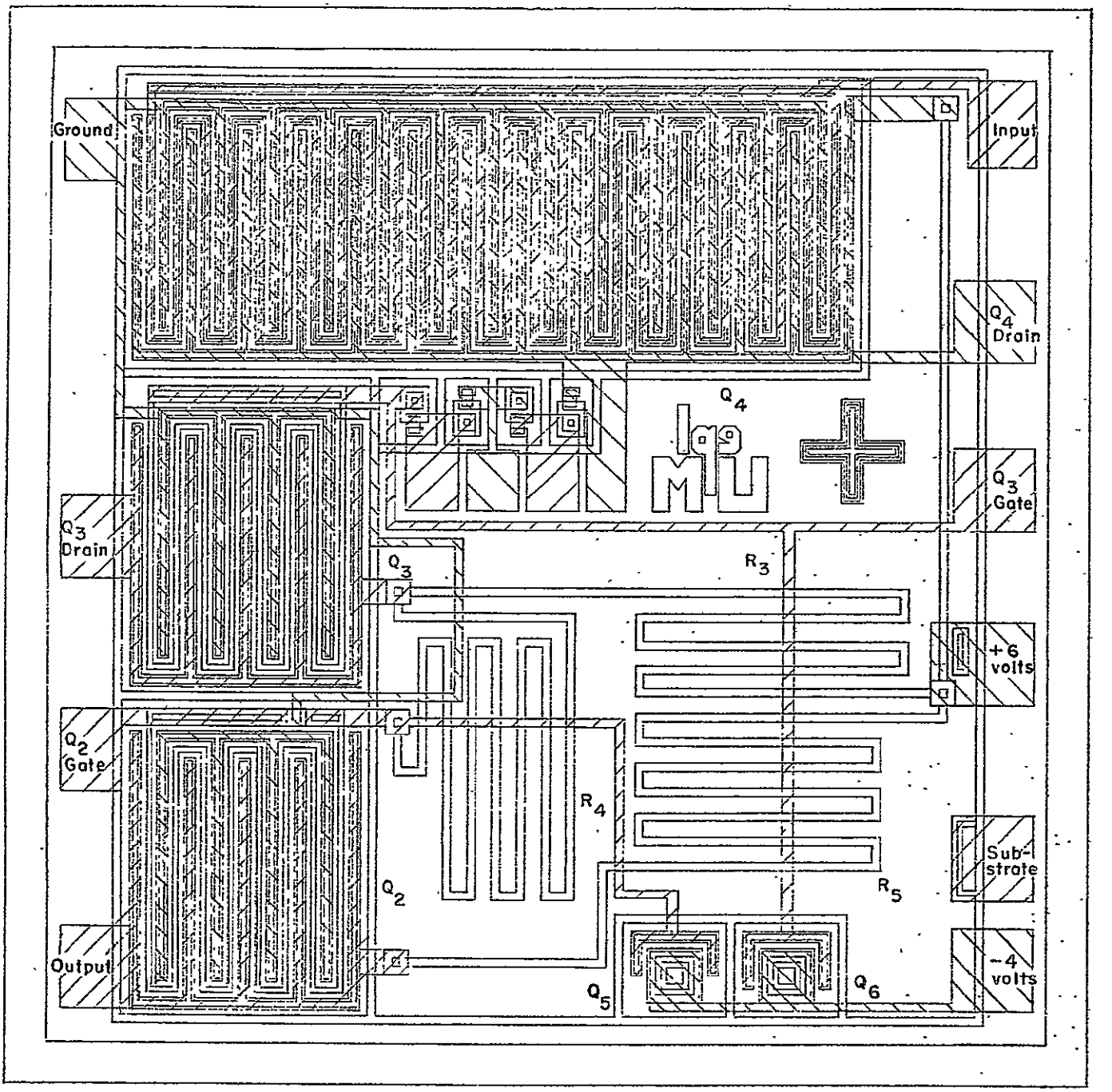
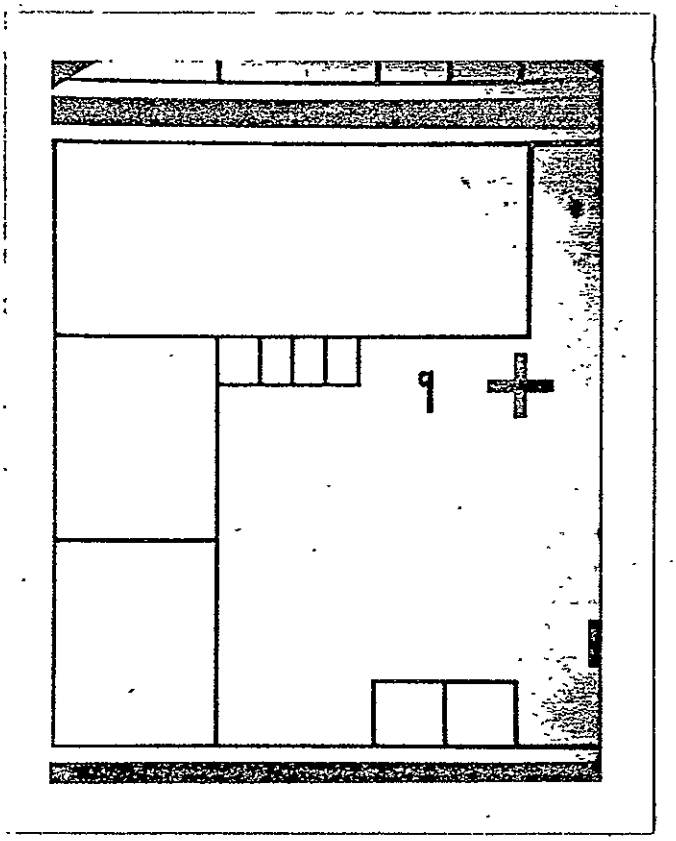
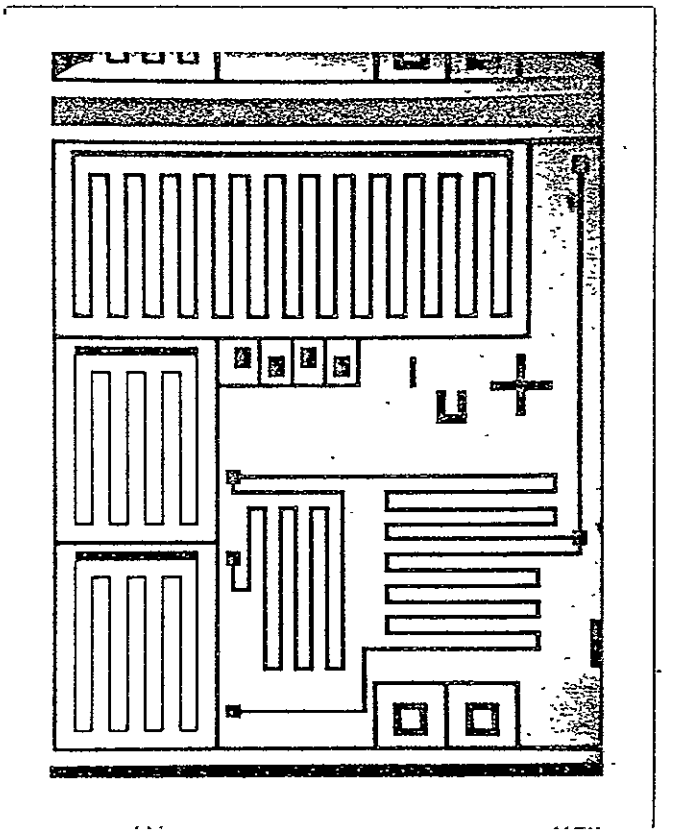


Fig. 3.16 Physical layout of the JFET preamplifier circuit

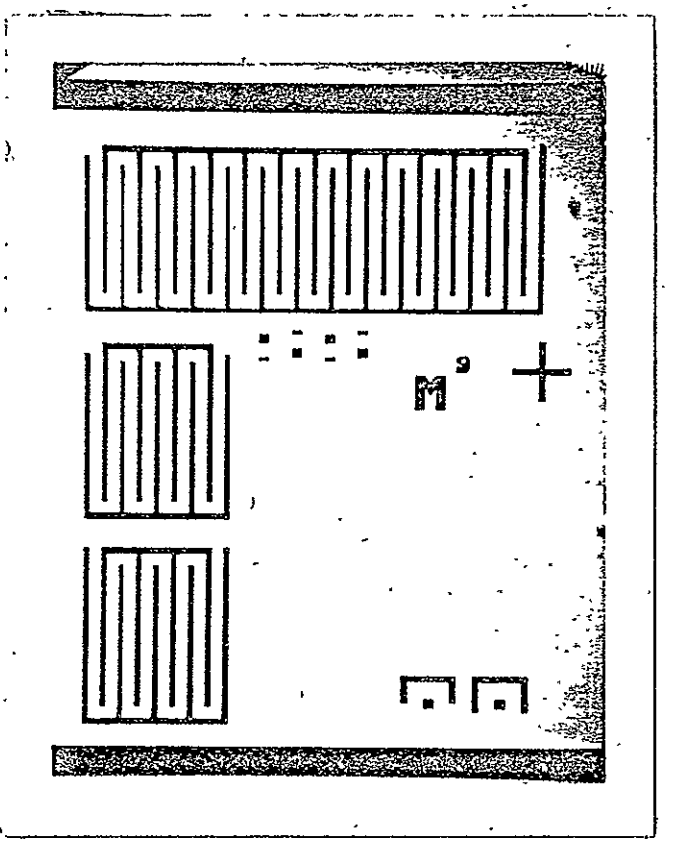


(a)

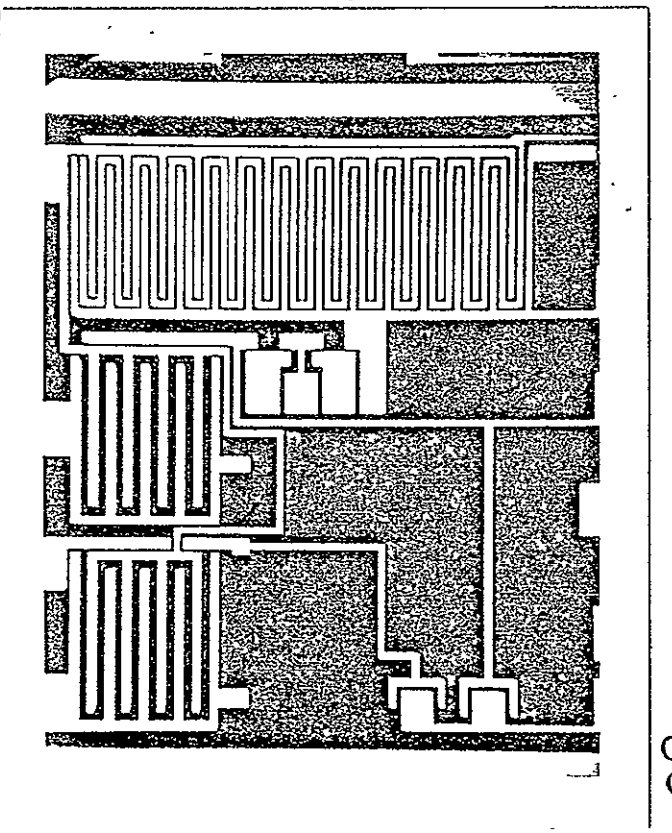


(b)

Fig. 3.17 Mask patterns used for the IC fabrication of the JFET preamplifier circuit
(a) Isolation diffusion mask
(b) Gate/resistor/base diffusion mask

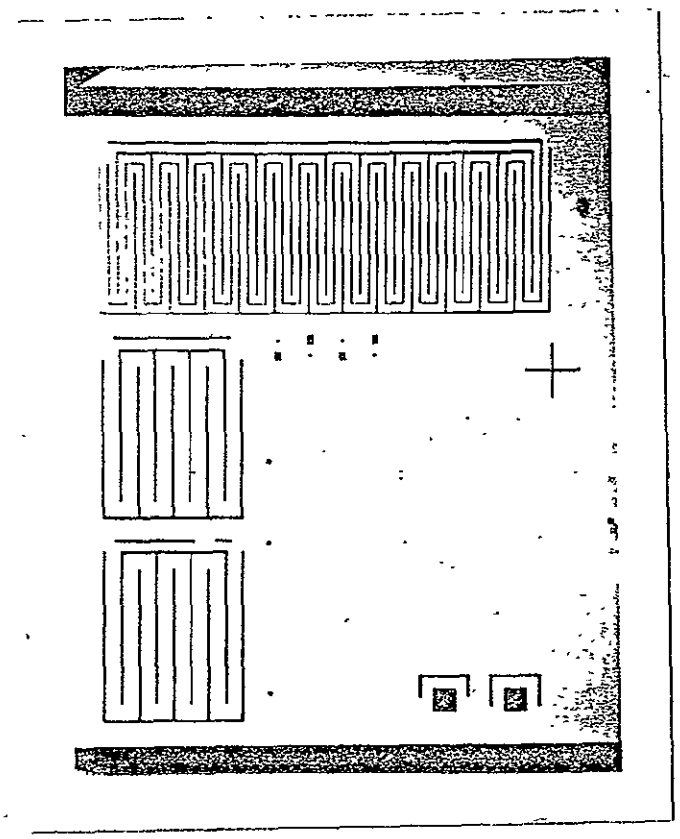


(c)



(d)

Fig. 3.17 (Cont.)
(c) n^+ contact/emitter diffusion mask
(d) Contact opening mask



(e)

Fig. 3.17 (Cont.)
(e) Metal pattern mask

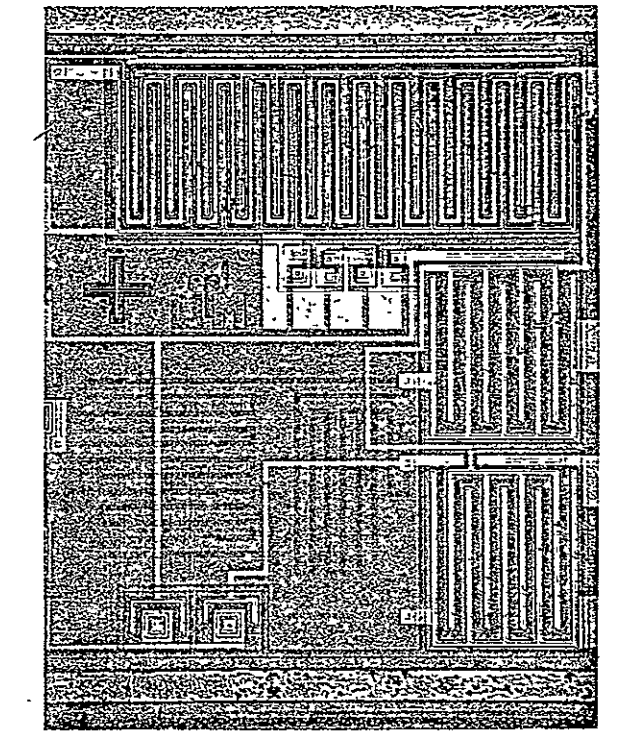


Fig. 3.18 Photograph of fabricated JFET preamplifier circuit

IV. AMPLIFIER TESTS

A. B. Macnee

4.1 Introduction

The pre- and post-amplifier designs are described in Section II, and their fabrication in monolithic form is described in Section III. In this section the results of tests made on fabricated samples are reported. Two postamplifier fabrication runs produced useable amplifiers. The best of these achieve the design goals for this unit. The postamplifier was fabricated first because it is somewhat less complex than the preamplifier. The postamplifier gain is less than that of the preamplifier, and it does not require a low noise input JFET (which requires a tight tolerance metallization step).

Within the time span of this contract we did not succeed in fabricating preamplifier samples which achieve the design specifications. Two fabrication runs were carried out. The second of these produced amplifier units which could be tested, but the component values were too far from the design values to give useful preamplifiers.

The tests reported here confirm the feasibility of the monolithic pre- and post-amplifier designs even where the test units failed to achieve the design performance. The observed deviations from the expected performance are correlated with device parameter deviations which in turn

can be controlled by systematic adjustment of the processing steps.

4.2 Preamplifier Tests

4.2.1 Test Fixtures. The preamplifier circuit design is presented in Section 2.3, and its layout and fabrication are described in Section 3.5. Figure 4.1 shows the printed circuit test fixture for the preamplifier samples. The four small capacitors (50, 100, 500, and 1000 pF) can be switched in parallel with the input singly, or in pairs to simulate a range of detector capacitances between 11 and 1511 pF. Ten microfarad electrolytic bypasses mounted at the socket terminals assure low power supply impedances at the higher frequencies. C_F is the feedback capacitor, and the 10 pF capacitor between pins 10 and 11 is for high frequency stabilization.

4.2.2 Preamplifier Sample Tests. Two preamplifier fabrication runs were made. The first run was not successful because the boron p-impurity source was not completely reactivated after a shut-down of the p-diffusion furnace. This resulted in JFET's with channel widths much greater than planned which gave excessively large values for I_{DSS} and V_p. The second run produced undepleted channel widths narrower than planned. Measurements of individual JFET's on the Electron Physics Laboratory Probe Station showed that the I_{DSS} values running 13 percent of nominal and

the pinch-off voltages at 33 percent of nominal. These values are consistent with an undepleted channel width approximately one half the desired width. The circuit is designed to tolerate a $\pm$ 20 percent variation of this width, so these samples are far outside of this range.

Since lack of time (in the period of this contract) precluded additional fabrication runs to bring the JFET parameters closer to the design values, a few (5) chips from the second fabrication run were mounted up on TO5, 14 pin, headers. The header connections used for these samples are given in Fig. 4.2. It will be noted that leads 7-10 were not used, but the ordering of the leads coincides with that given in Fig. 4.1 so that the pre-amplifiers can be plugged into the test board without difficulty.

The mounted amplifiers were designated A, ..., E . The individual JFET's of all five units were examined on the transistor curve tracer, and it was rapidly evident that in three cases the metallized JFET, Q_2 in Fig. 4.2, was short-circuited. These three samples (A, B, and D were not tested further). The measured values for I_{DSS} and V_p of transistors Q_2 , Q_3 , and Q_4 in the two remaining units are tabulated in Table 4.1. Assuming that the I_{DSS} values vary as the cube of the undepleted channel width, and the V_p values vary as the square, these

data suggest that the channel widths are 55 percent and 45 percent of nominal for amplifiers C and E respectively. The reduced I_{DSS} and V_p values prevent achievement of the design quiescent points with the resistors and diodes which also are fabricated into the circuit.

Table 4.1. Measured JFET parameters for two preamplifier samples

Parameter		Amplifier	
(See Fig. 4.2)	Design value	Sample C	Sample E
Q_4 I_{DSS} (mA)	21.8	3.6	2.1
Q_4 V_p (volts)	-2.4	-1.0	-0.7
Q_3 I_{DSS} (mA)	10.9	1.75	0.9
Q_3 V_p (volts)	-2.4	-0.8	-0.55
Q_2 I_{DSS} (mA)	10.9	1.5	1.0
Q_2 V_p (volts)	-2.4	-0.84	-0.8

An even more serious consequence of the deeper than planned p-diffusion is the resulting very narrow separation between the resistors and the p-substrate. The resistor isolation island depletion layer can punch through destroying the resistor isoloation from the substrate, at the design circuit potentials.[1] The resulting uncontrolled feedback,

[1]This is explained in Section 3.4.

via the resistive substrate, changes the amplifier performance in unpredictable ways. Measurements on amplifiers C and E indicate that punch through occurs at substrate to epitaxial layer reverse biases of the order of 3 volts. This prevented testing of these units without punch through.

The "C" amplifier sample was tested in the test circuit board of Fig. 4.1. By operating with a reduced negative supply, it was possible to get some amplification from this unit, but the gain was far below the design value. Because of the unpredictable interaction via the substrate (caused by resistor isolation punch through), there did not appear to be much to be gained by extensive experimentation. Using a pair of external series connected diodes from the drain of Q_4 to the gate of Q_3, these two transistors could be operated at close to the nominal Q point. The overall voltage gain in this case was -16.6. The gain of the Q_3 stage in this case was close to nominal (approximately -10), but the input and output stage gains were low. Even when Q_3's gain was removed from the circuit by connecting 100 μF from the Q_3 gate to source, there was still an overall gain of 1.52! In this instance the signal apparently was getting from Q_4 to Q_1 via a substrate punch-through path. At $V^+ = +7.0$ volts and $V^- = -1.35$ volts, the measured supply current were $I^+ = 2.14$ mA and $I^- = 1.085$ mA. The substrate potential in this instance settled at

V_{sub} = -0.555 volts corresponding to a substrate current (which should be zero) of 54.8 microamperes. This shows that the currents flowing through Q_5 and Q_6 (the "current source" JFET's) are excessive. The measured interstage loss between Q_3 and Q_2 also suggests that incrementally Q_5 is acting more like a resistance of 12 kilohms than a current source. Bypassing the R_4 resistor with a large (0.1 μF) capacitor raised the overall gain to -25.

The gain of -25 is so low that any noise measurements with this sample would have no significance, and therefore none were made. Based on our noise measurements on the preamplifier breadboard (Section 2.3, Fig. 2.7), however, we believe that, with additional fabrication development, satisfactory noise and gain performance can be obtained.

4.3 Postamplifier Tests

4.3.1 Test Fixtures. The postamplifier circuit design is presented in Section 2.4, and its layout and fabrication as a monolithic integrated circuit are described in Section 3.4. Two fabrication runs produced useable amplifier samples and four chips from each run were successfully mounted up on T05 headers for testing. The samples from the first run (designated P01, ..., P04) were mounted on 8-pin headers. The amplifier chip has a total of 12 nodes which can be brought out to external connections, as shown in Fig. 3.9.

Figure 4.3 shows the points selected for external connections to the first run amplifier samples and the pin numbers on the T05 headers. To test these first run amplifiers, the circuit shown in Fig. 4.4 was fabricated on a printed circuit board with an 8-pin T05 socket for the postamplifier samples.

The positive and negative supply lines have RC filtering to reduce noise that might enter the amplifier from the supply leads. The feedback and series input RC circuits are selected for a time constant of 3 microseconds, and a 3.9-kilohm load resistor is wired permanently on the board. The series diode string and the 27-kilohm resistor from the negative supply line to ground allowed us to return the substrate to potentials less negative than V^- during testing.

Our measurements on the first run amplifier samples gave unexpected results, and it rapidly became evident that it would be very helpful to have access to all twelve of the connection tabs fabricated on the amplifier chip. When the second amplifier fabrication run was completed (Run #14), the new chips were mounted on 12-pin T05 headers. The basing of these second run samples is given in Fig. 4.5. To test these new samples a second test board was assembled. The components on this board were the same as those in Fig. 4.4; the only difference being in the pin designations.

4.3.2 Component Parameters. To establish the parameters of the components in the samples, curve tracer measure-

ments were made at the available terminals. While our initial measurements were made with diode D_1, in the source lead of transistor Q_1, it soon became apparent that this diode was not needed in the circuit. It was removed from the circuit by bonding a jumper between the Q_1 source tab and the ground tab (see Fig. 3.9). This modification shorts out D_1 in Fig. 4.3, and makes it possible to observe the drain-source characteristics of Q_1 directly. Figure 4.6 shows drain-source characteristics of the input and output transistors Q_3 and Q_1 in amplifier P02. These are typical of the characteristics observed for all the four amplifiers P01, ... , P04. From characteristics such as these the values of I_{DSS} and V_p for these transistors were determined for each amplifier. Table 4.2 summarizes this measured data for the four, first run amplifier samples. Looking over this table it is apparent that all the transistors which could be measured from the external amplifier terminals have values of I_{DSS} about 45 percent of the nominal (design) values given in Fig. 4.3. The pinch-off voltages are also low. If we assume that the two larger values are anomalies, the average pinch-off voltage is 75 percent of the nominal value. Although these values do not follow exactly the variation predicted for varying undepleted channel width, they are certainly of the correct order of magnitude. Except for the pinch-off voltages of the output transistors for P01 and P04, the measured parameters are all relatively uniform. The resistor values are about 6 percent above their nominal values.

Table 4.2 Measured parameters of first run amplifier components

Amplifier No.	P01	P02	P03	P04	Aver.
Input transistor					
I_{DSS}^{Q3} (mA)	4.1	4.7	4.8	4.8	4.76
V_p^{Q3} (volts)	-1.74	-1.8	1.85	-1.8	-1.80
Output transistor					
I_{DSS}^{Q1} (mA)	9.6	10.3	11.0	10.3	10.3
V_p^{Q1} (volts)	-2.75	-1.8	*	-2.6	-2.38
R_{2-1}	14.7 KΩ	13.3 KΩ	12.9 KΩ	13.2 KΩ	13.5
R_{8-5}	5.81 KΩ	6.02 KΩ	6.67 KΩ	6.94 KΩ	6.4

*Could not be measured because of broken lead to tab #3.

Since the I_{DSS} and V_p values achieved in the first fabrication run were below nominal, a second batch of amplifiers was fabricated with the processing altered to increase the undepleted channel widths. Four samples from this run were mounted on 12-pin T05 headers for testing. One of these units was damaged in the lead bonding process; three units

Table 4.3 Measured parameters of second run amplifier components

Amplifier No.	14B	14E	14H	Average
Input transistors				
I_{DSS}^{Q3} (mA)	9.55	9.25	7.5	8.77
V_p^{Q3} (volts)	-2.73	-2.56	-2.15	-2.48
Output transistors				
I_{DSS}^{Q1} (mA)	17.3	16.3	12.4	15.3
V_p^{Q1} (volts)	-2.78	-2.78	-2.12	2.56
R_1 (KΩ)	16.7	18.2	19.2	18.0
R_2 (KΩ)	207.0	99.3	83.5	130.0
R_4 (KΩ)	8.18	8.33	8.93	8.48

designated 14B, 14E, and 14H were thoroughly tested. Table 4.3 summarizes the component parameters measured on these second run samples. As expected the I_{DSS} and V_p values are closer to the nominal values in these units. Two samples, 14B and E, have almost identical characteristics except for the value of the resistor R_2. Since the resistors are created by the same p-diffusion which produces the transistor gates, the increased V_p and I_{DSS} values

are accompanied by increases in the resistor values. The value of R_2 cannot be measured directly; it is inferred from measurements of R_1 alone and R_1 and R_2 in parallel; as a result this measurement is subject to greater error than the others. The average values of R_1 and R_4 are both 41 percent above nominal.

4.3.3 Amplifier Performance. When the postamplifier samples were first inserted in the test circuit board with a 250 kilohm variable resistor between the gate of Q_3 and the -4 volt supply (Fig. 4.3), it was observed that (a) the supply currents were much higher than expected and (b) the quiescent drain potential of Q_1 could not be adjusted to the desired 6-8 volts in 3 of the 4 units. It was also found that the incremental voltage gains were of the order of 15 to 25. After the second run samples, with their addition measurement points, were obtained, it was established that these initial results were produced by interactions via the amplifier substrate.[1] As fabricated, each diode in Figs. 4.3 and 4.5 forms a vertical pnp transistor with the substrate which forms a common, resistive layer under the entire circuit. The resulting circuit including these vertical transistors is given in Fig. 4.7. The resistive substrate layer is represented by an R ladder in this circuit. In normal operation all the diodes in this figure are forward biased, the string $D_2, \ldots, D_7$ by the resistor R_3 and the -4 volt suppy, and

[1] See Section 3.4.

D_1 by the source current of Q_1. The forward beta of a typical vertical pnp transistor was measured to be 100. As a result, these vertical transistors are normally all saturated, and there is a low impedance path from each emitter (diode anode) through the resistive substrate to the negative supply. Since the transistors associated with diodes D_1 and D_2 act as short-circuits to the substrate, there is a resistive pad connecting the source of Q_1 to the gate of Q_2! The resulting signal feedback is negative, and it produced the low voltage gains observed initially. As soon as diode D_1 was removed from the circuit (by short circuiting), the best of the incremental gains jumped to the expected values.

With diode D_1 shorted, the vertical transistors associated with diodes $D_2, \ldots, D_7$ do not affect the signal characteristics of the amplifiers, but they do require a much larger current from the -4 volt supply. If we assume the resistance through each saturated transistor to the -4 volt supply is about the same, the added current is

$$\frac{1.5}{R} + \frac{2.0}{R} + \frac{2.5}{R} + \frac{3.0}{R} + \frac{3.5}{R} + \frac{4}{R} = \frac{16.5}{R}$$

Our measured -4 volt supply currents ran about 7 milliamperes above the expected 0.5 milliamperes which implies $R = 2360$ ohms. This is reasonable for the 12-20 Ω-cm p-substrate on which these amplifiers are fabricated. To experimentally

verify that the extra current was indeed produced by these vertical transistors, an external diode string was connected from the base of Q_2 (Tab 7 in Fig. 4.5) to ground (Tab 6 in Fig. 4.5) in one of the second run units. With 4 diodes in the external string the potential of the Q_2 gate was raised to -2 volts and the substrate current dropped to 0.43 milliamperes.

Initially it was observed that the current taken from the positive supply was also one or two milliamperes above the expected value on some samples. Experimentation showed that this extra current was produced by punch-through of the resistor to the substrate when the difference between the substrate potential and the island potential "pinched off" the thin n layer. The reverse bias necessary to deplete the n-epitaxial layer beneath the resistors is the substrate gate pinch-off potential of the amplifier JFET's since the p-resistors and the p JFET gates are created by the same diffusion steps.[1] This potential is in the range 10-14 volts. By reducing the positive supply potential to +8 volts, the excess current from the positive supply was made negligible in most units as indicated below.

Table 4.4 summarizes the measured small signal gains of the amplifiers at various supply voltages. The gains are measured at 1 kHz which is well below the upper half power frequencies of these amplifiers. The voltage gains range from a low of 22.5 to a high of 112. The first run amplifiers,

[1] See Section 3.4.

Table 4.4 Measured quiescent point dc parameters and signal gains of postamplifier samples

Amplifier Number	V^+ volts	V^- volts	$V_{substrate}$ volts	I^+ mA	I^- mA	V^Q_{out} volts	$V^Q_{8,12}$ volts	$\frac{AV_{out}}{AV_{in}}$ (at 1 kHz)
P01	+8.0	-4.0	-1.89	0.553	0.950	+4.08	-1.293	-24.5
P02	+8.0	-4.0	-1.87	0.295	0.580	+4.02	-1.537	-22.5
P03	+8.0	-4.0	-1.77	0.386	0.800	+4.02	-1.154	-54.5
P04	+8.0	-4.0	-1.87	0.414	0.530	+4.09	-1.349	-104.0
14B	+8.0	-4.0	-3.0	0.96	2.80	+2.00	-1.582	-65.7
14E	+8.0	-4.0	-3.96	0.89	5.08	+4.00	-2.09	-111.7
14E	+8.0	-4.0	-3.0	0.51	2.51	+4.13	-1.678	-97.2
14E	+8.0	-4.0	-2.5	0.44	1.16	+4.0	-1.398	-48.3
14H	+8.0	-4.0	-2.0	0.70	0.717	+4.05	-1.337	-91.5
14H	+8.0	-4.0	-3.0	1.51	2.93	+4.00	-1.84	-112.0

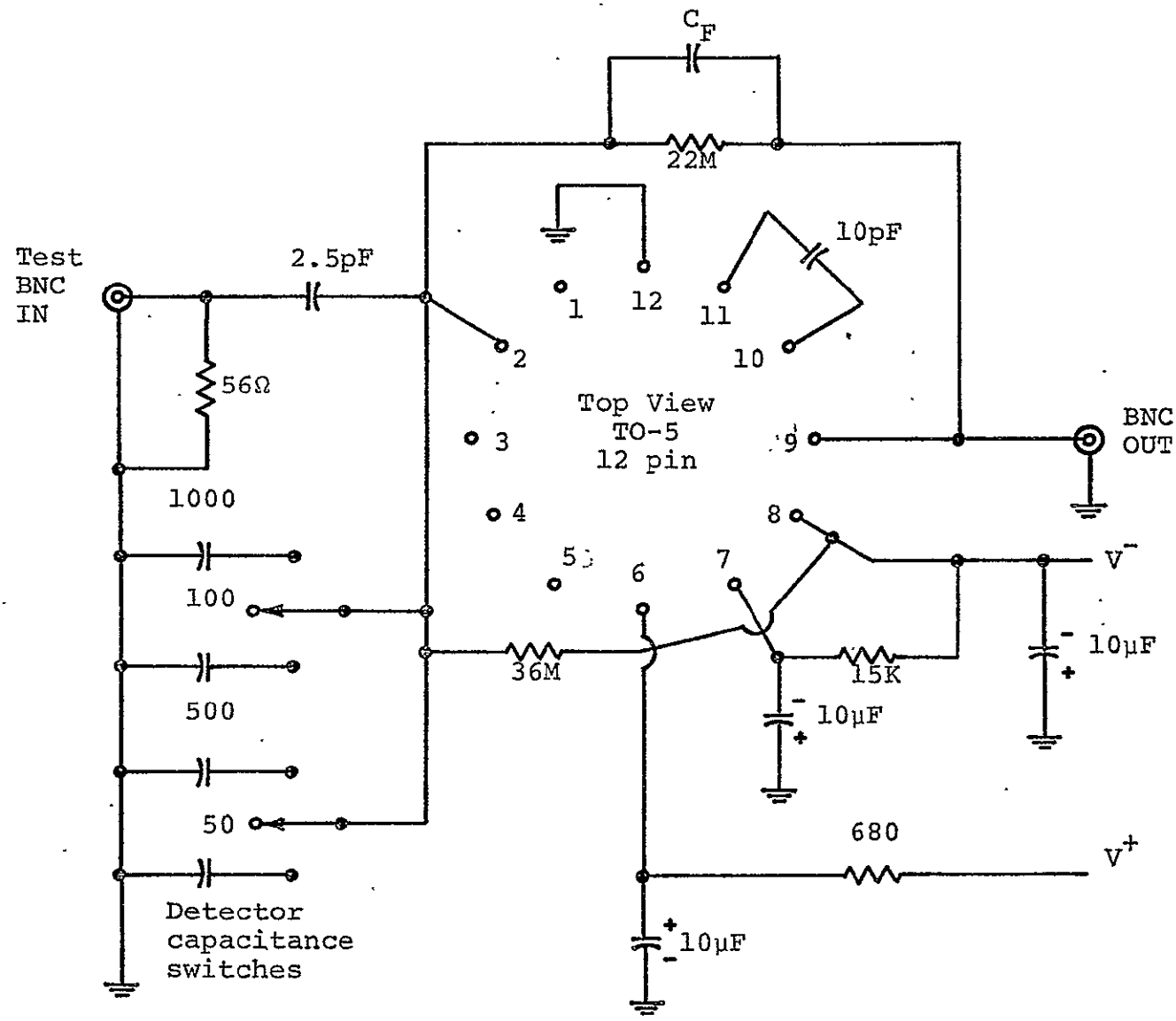
P01, ..., P04, used an external 4 diode-resistor string to set the substrate potential as shown in Fig. 4.4. The measured changes in this potential reflect varying currents taken by the substrate of these samples. Operating at the less negative substrate potential reduced the currents flowing in the vertical pnp transistors described above and compensated for the lower values of V_p and I_{DSS} of the JFET's in the first run amplifiers. The second run pre-amplifiers, 14B, E, and H, were tested with three independent supplies. The data on 14E and 14H show clearly the rapid increase in the negative supply current with more negative substrate voltages because of the vertical pnp transistors created by the D_2, ..., D_7 diode strings. The current I^- in this table is the total negative supply current (to leads 8 and 9 in Fig. 4.5).

Except for the substrate current required, amplifiers P04, 14E, and 14H are operating in close agreement with our design calculations and breadboard measurements. Frequency response and measurements on two normal gain units, P04 and 14E, and one low gain unit P01 are presented in Fig. 4.6. The open loop voltage gains were measured between the gate of Q_3, the input transistor, and the 3.9 kilohm ac coupled external load. The closed loop gains are between the input and output in Fig. 4.4 with a 3.9 kilohm external load. The open loop upper half power frequencies of P04 and 14E are 58 kHz and 68 kHz respectively, while for the low gain P01 unit it is 144 kHz. The dominant time constant in the

postamplifier design is due to the interstage between Q_2 and Q_3. The voltage gain-bandwidth products of these three amplifiers are tabulated below along with the gains and bandwidths.

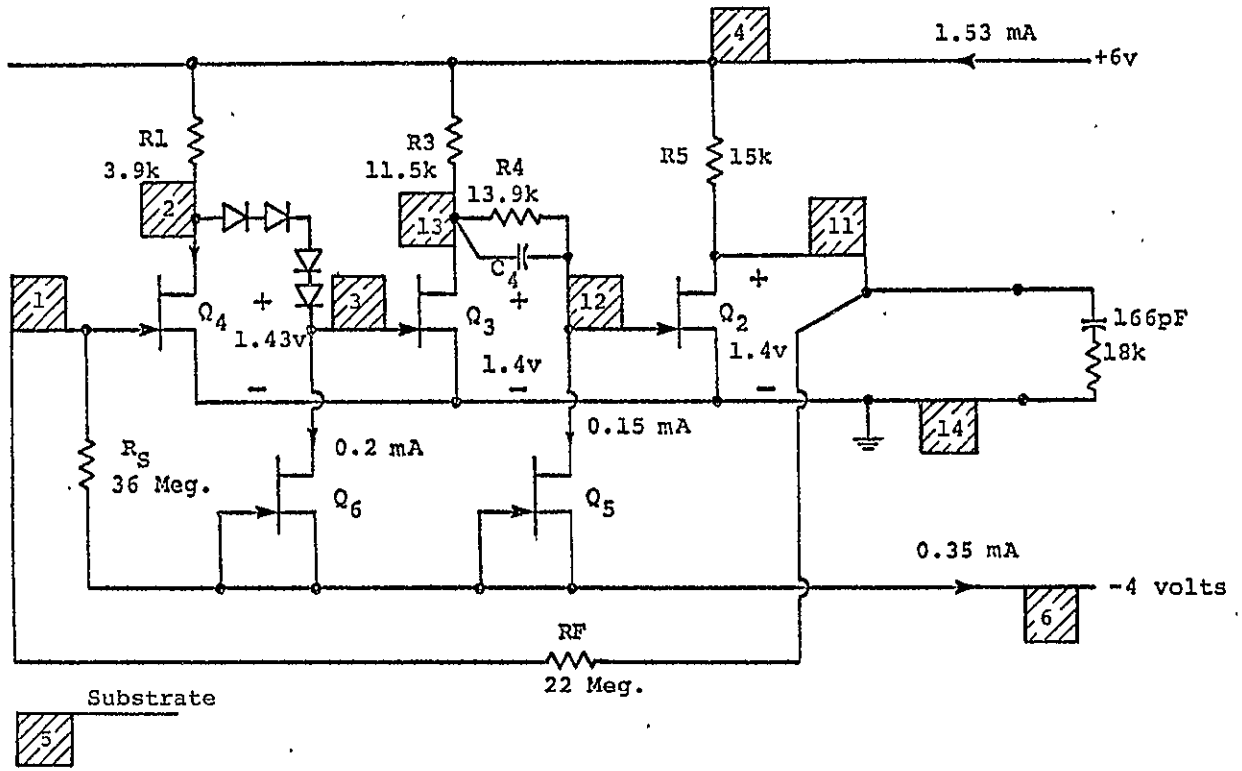
Amplifier	V.G.	f_3dB	(V.G.)xf_3dB
P04	116	58 kHz	6.73 MHz
14E	93	60 kHz	6.32 MHz
P01	26	144 kHz	3.74 MHz

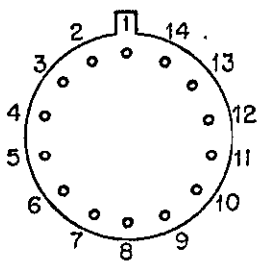
Although the gain of P01 is only 22 percent that of P04, its gain-bandwidth product is only down 56 percent. This suggests that the low gain of P01 probably is due to a reduced value for R_2. This could be caused by the resistor isolation region punch-through discussed earlier if the punch-through point is somewhere along the resistor's length (as opposed to the positive end).



Pin # 1	Blank
Pin # 2	Input (Q_4 gate)
Pin # 3	Blank
Pin # 4	Q_4 drain
Pin # 5	Q_3 gate
Pin # 6	Positive Supply
Pin # 7	Substrate
Pin # 8	Negative Supply
Pin # 9	Output (Q_2 drain)
Pin #10	Q_2 gate
Pin #11	Q_3 drain
Pin #12	Ground

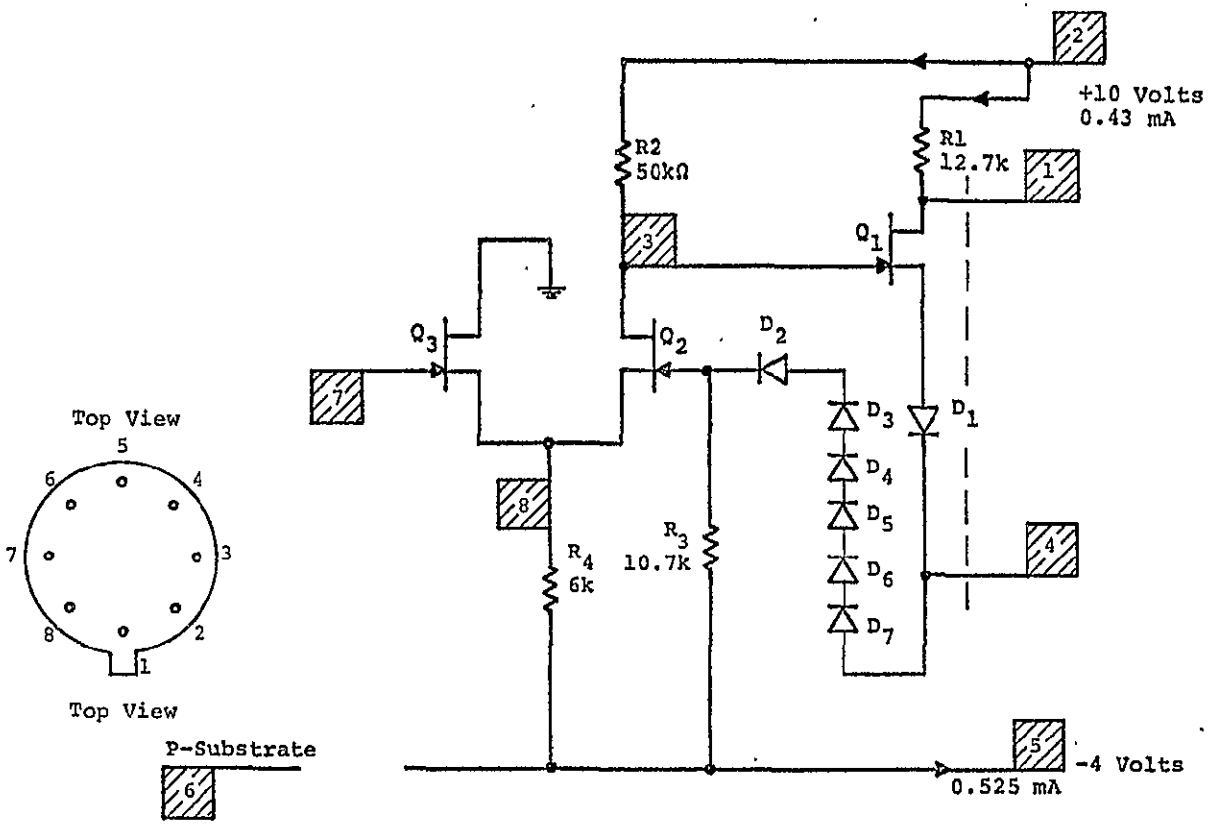
Fig. 4.1 Test circuit board for preamplifier samples





JFET No.	Q_2	Q_3	Q_4	Q_5	Q_6
I_{DSS} in mA	10.9	10.9	21.8	0.15	0.2
V_p in volts	-2.4	-2.4	-2.4	-2.4	-2.4
Quiescent i_D	0.307	0.25	0.97	0.15	0.20

Fig. 4.2 Basing of preamplifier samples



JFET No.	Q_1	Q_2	Q_3	V_{SUBS}
I_{DSS1} in mA	21.8	10.9	10.9	0 V
V_{p1} in Volts	-2.4	-2.4	-2.4	0 V
i_D at Q point	0.23	0.2	0.2	-4 V

Fig. 4.3 Basing of first run postamplifier samples

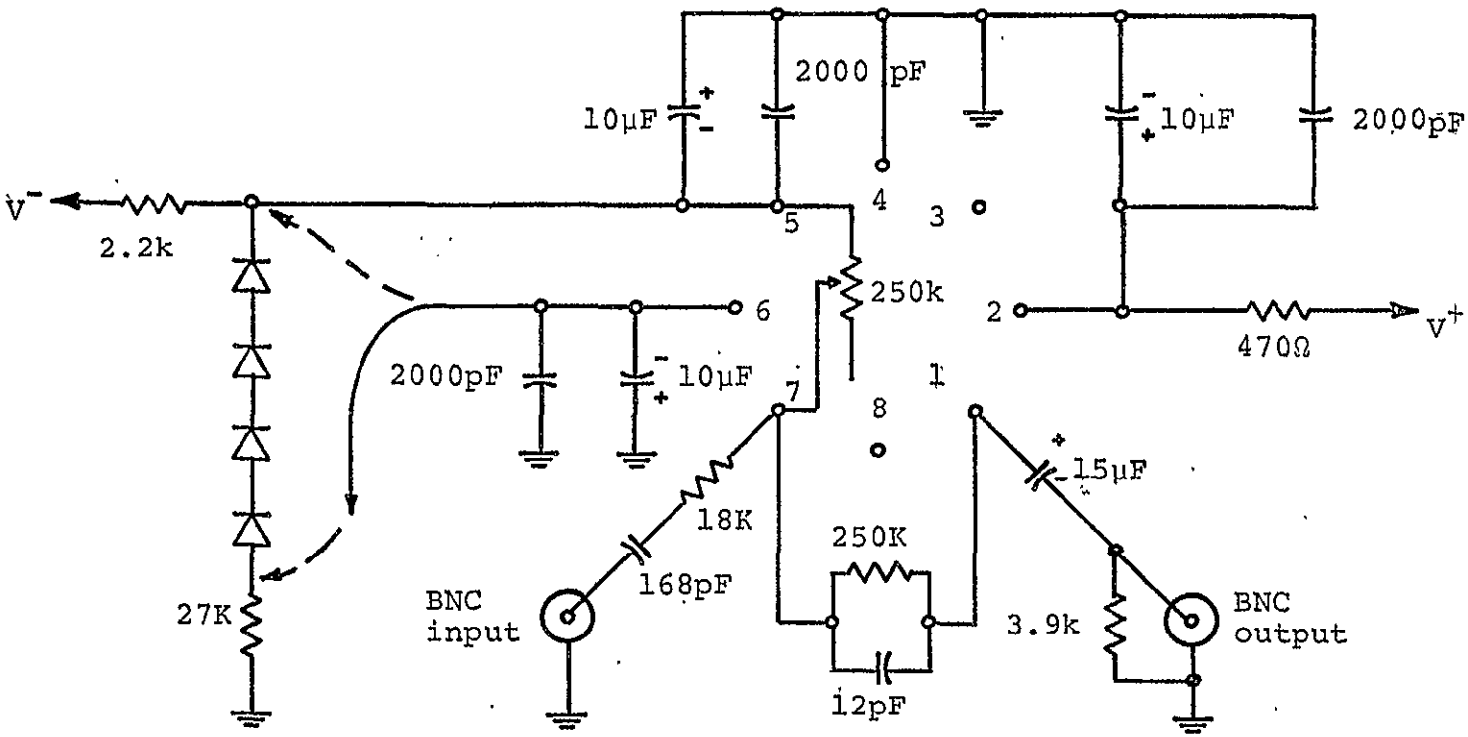
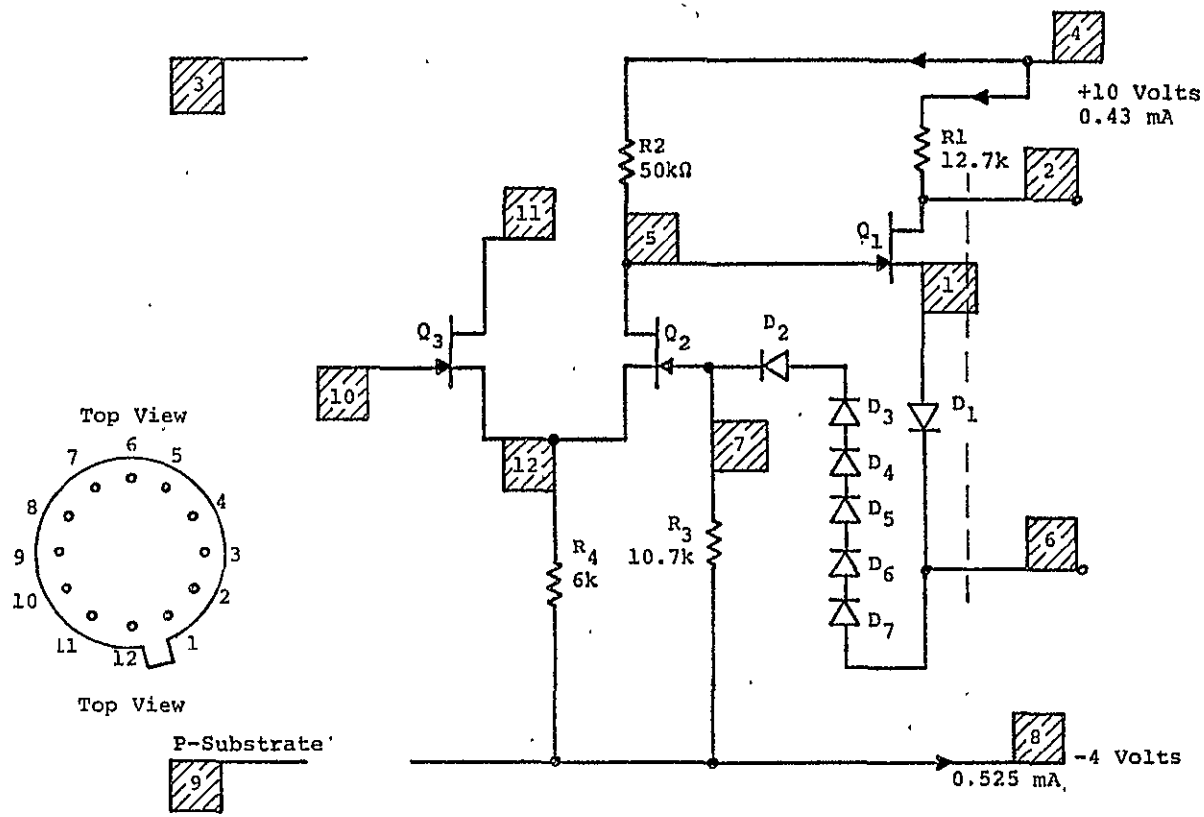
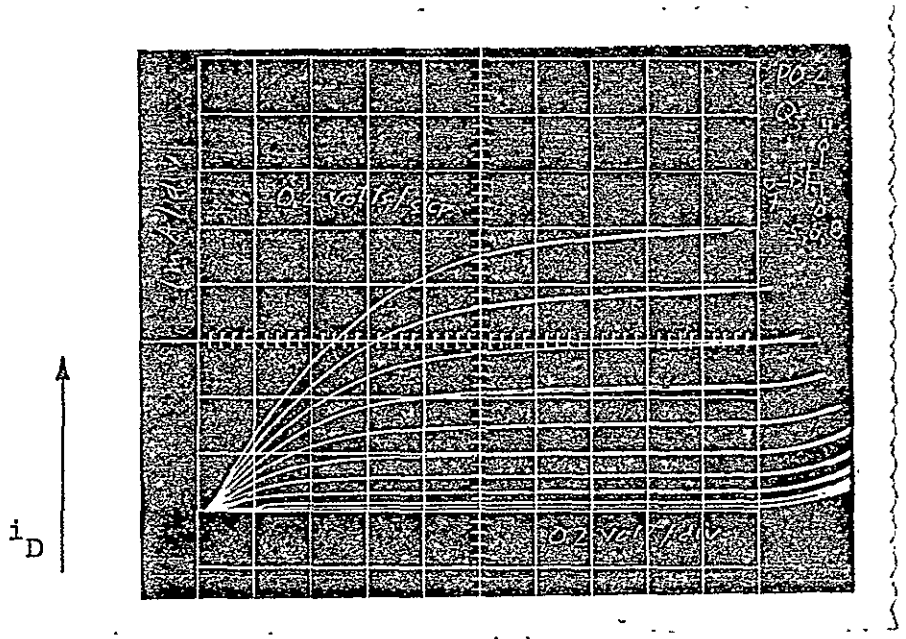


Fig. 4.4 Test board circuit for preamplifier run #1 samples



JFET No.	Q_1	Q_2	Q_3	V_{SUBS}
I_{DSS1} in mA	21.8	10.9	10.9	0 V
V_{p1} in Volts	-2.4	-2.4	-2.4	0 V
i_D at Q point	0.23	0.2	0.2	-4 V

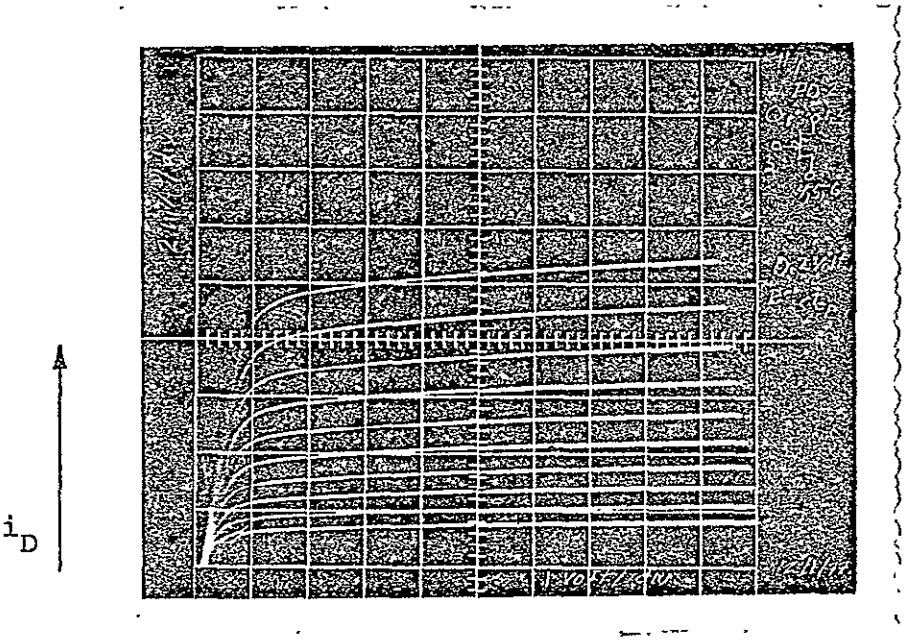
Fig. 4.5 Basing of second run postamplifier samples



(a)

1 mA/div., 0.2 volt/div., 0.2 volt/step

V_{DS}



(b)

2 mA/div., 1 volt/div., 0.2 volt/step

Fig. 4.6 Drain-source characteristics of (a) input and (b) output transistors of amplifier P02

C-2

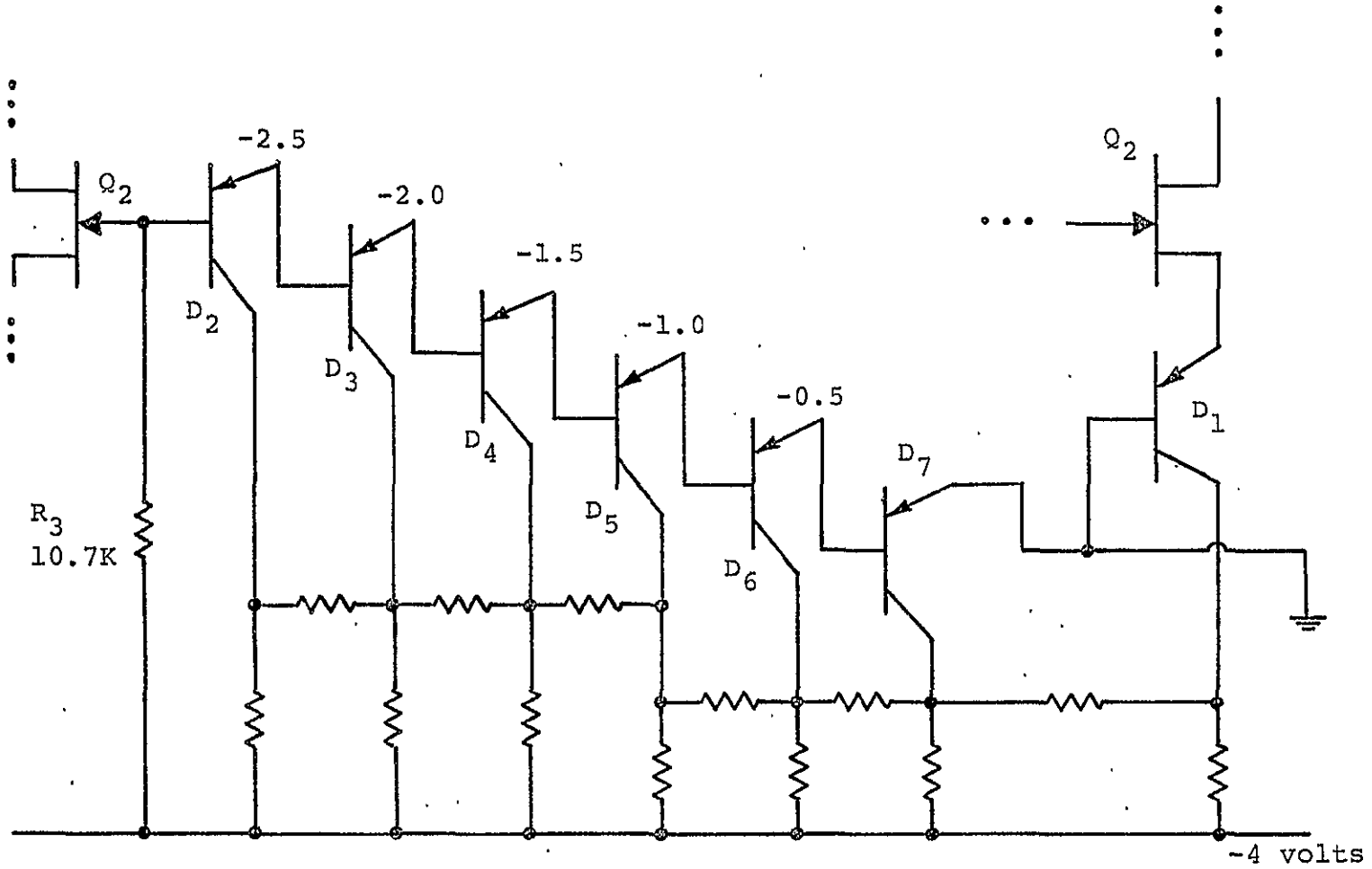


Fig. 4.7 Parasitic vertical PNP transistors associated with the diodes in Figs. 4.1 and 4.3

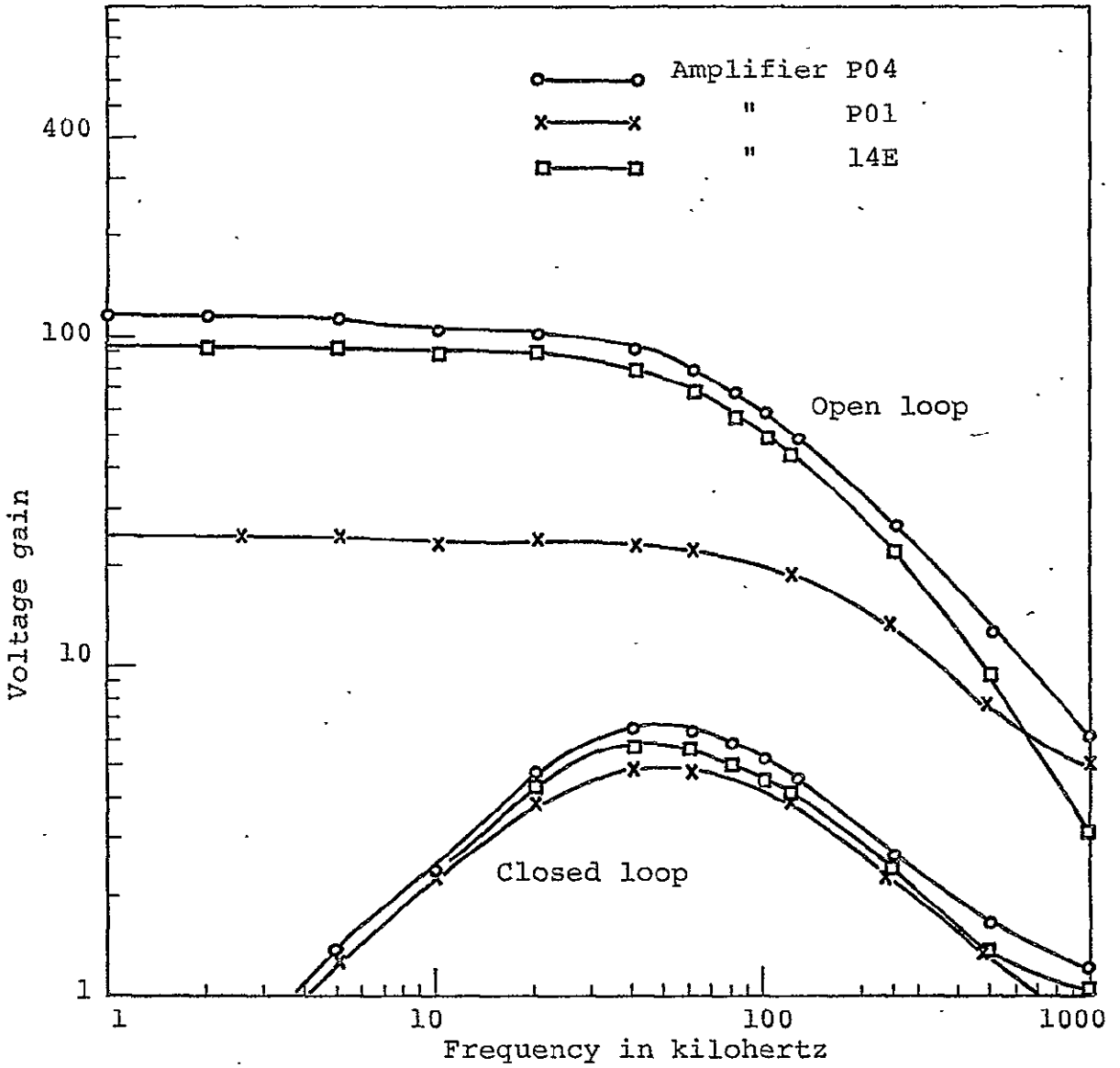


Fig. 4.8 Measured postamplifier open and closed loop frequency responses

V. SUMMARY AND SUGGESTIONS FOR FURTHER WORK

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5.1 Summary of Results

The objective of this project was to design and develop a fully integrated-circuit version of the preamp/postamps used with solid state detectors on MJS. A second step in the development program was to match the performance of existing discrete designs in integrated form and to proceed to a pilot production of sample chips to verify performance. Section II of this report summarizes the circuit designs for a preamplifier-postamplifier combination suitable for integrated circuit fabrication using junction-FET technology. Section III describes the fabrication technology required to fabricate these amplifiers in monolithic form, and Section IV reports on tests of samples taken from pilot production of these units.

The circuit designs presented in Section II evolved through the duration of this project in response to our experiences with the fabrication of JFET's in a planar form suitable for integration into a complete amplifier. A major circuit constraint, imposed by the JFET fabrication technology, is the presence of a substrate gate. All the JFET's have two gates: one which is "free" to be connected by the surface metallization and a second which is connected

to the chip substrate and is common to all transistors. To prevent undesired feedback the substrate must be held at a fixed potential, and therefore circuit configurations which require both the transistor gate and source potentials to vary (such as source followers and positive current source circuits) are not practical in most cases. Both the preamplifier and the postamplifier circuits have been breadboarded and tested extensively using sample JFET's produced by the fabrication processes which were developed in our laboratory. These breadboarded, all JFET, circuits match the electrical performance of a pre/postamplifier circuit used previously to test the performance of SFB8558 JFET's under NASA contract NAS5-23267. The details of those discrete circuits which utilize PNP and NPN bipolar transistors with a single JFET at the preamplifier input, and the measurement techniques used, are described in the Interim Report on that earlier contract.[1]

The technology developed to fabricate the JFET integrate pre/postamplifier circuits is described in Section III. Initially, almost a year was spent trying to develop a double diffusion technology for the JFET fabrication.[2] This effort

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[1]Interim Report for June 20, 1973 to June 20, 1974, Contract No. NAS5-23267, "Circuits for Nuclear Particle Measurement Systems," Part I: Charge Sensitive Preamplifiers with Large Detector Capacitance; February 1975.

[2]Quarterly Reports 014393-1, 014393-2, 014393-3, and 014393-4.

was unsuccessful, and eventually was abandoned for the single diffusion process described in Section III.[1] In retrospect, this change should have been made earlier. As soon as the single diffusion process was introduced, JFET's with suitable characteristics (I_{DSS} and V_p) were produced.

The first of these transistors exhibited more noise than comparable commercial discrete devices. The source of the extra noise was traced to series resistance in the gate lead of the first samples. This resistance was greatly reduced by the addition of a gate metallization step, and tests on the metallized gate, single diffusion JFET's show them to be comparable with the best discrete commercial JFET's we have available. (See Fig. 2.7.)

Based on our experiences in fabricating singly diffused JFET's and resistors, complete preamplifier and postamplifier chips were laid out. Mask sets were fabricated, and several fabrication runs were carried out as described in Section III. These pilot fabrication runs confirmed the suitability of the JFET designs, but they also revealed two unanticipated parasitic effects. A punch through from the resistor isolation island to the substrate and a vertical pnp transistor associated with offset diodes used in the circuits. Both of these effects can be eliminated by a modified fabrication process as described in Section III.[2] The end of the contract period prevented our carrying out and verifying

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[1] Also in Quarterly Reports 014393-5 and 014393-6

[2] Section 3.4

those modifications. Lack of time also prevented a completion of the pilot development of the monolithic preamplifiers.

In retrospect, we underestimated the time needed to develop and control the JFET fabrication procedures in the environment of our laboratories. Faulty air conditioning, very short furnace heater life, and the random flow of students all contributed to delays. The critical steps in the JFET fabrication are the p-diffusion and drive-in which determine the width of the undepleted channel. As long as the furnace and p-type diffusion used for this step are not disturbed, we can establish by trials the times and temperatures required. This is a time-consuming process, however, since each trial fabrication takes a week to ten days, minimum. The preamplifier pilot fabrications were begun using a new p-type impurity source, and time ran out before the necessary trial sequence could be completed.

Tests of the pilot fabrication samples are reported in Section IV. Except for excessive power consumption associated with the parasitic vertical pnp transistors, the best postamplifer samples performed as planned. Their performance is summarized in Table 4.4, Section 4.3.3. Two of the postamplifiers, P04 and 14E, have accumulated about 150 hours of operation in bench test setups without any measureable change in their characteristics despite the fact that the sample amplifiers are all mounted on T05 headers (with varying numbers of leads) and covered by metal caps which

are merely held in place with scotch tape. Time did not permit any temperature or radiation exposure tests. The 14E unit was also operated for two weeks in a noise measurement setup in conjunction with the preamplifier breadboard. The overall noise performance of this combination is the plotted data in Fig. 2.7, Section 2.3.

Time limitations ended the iteration of the preamplifier fabrication processes before the device parameters could be brought into the desired ranges. The limited measurements made on two sample amplifiers did not reveal any unexpected weaknesses in the circuit design.

5.2 Suggestions for Further Work

Since the pilot fabrication runs of the preamplifier and postamplifier chips fell short of matching the performance of existing discrete designs, there obviously is a need for further development of the integrated amplifiers and for the testing of the results of those developments.

A first step in this development would be simply to complete the necessary fabrication runs to bring the preamplifier JFET and resistor parameters to within ± 10 percent of the nominal values. Apart from some uncertainty concerning the current source JFET's (Q_5 and Q_6 in Fig. 4.2), it appears that only adjustments of the gate diffusion and drive-in steps are needed to produce operable preamplifiers.

A second step would be to modify the processing sequence to eliminate the resistor isolation island punch through problem. This requires that the resistors be fabricated with a separate p diffusion which would give a shallower p-layer than the p-gate diffusion. (Presently, the resistors and JFET gate regions are formed simultaneously by a single p-diffusion.) This modified fabrication would require one additional mask and etch step; the shallower p-resistors should lead to a larger ohms per square, and would probably require somewhat less area for the resistors in Figs. 3.10 and 3.16.

The diodes in the preamplifier layout (Fig. 3.10) were fabricated as n-p-n transistors with collector-base shorts to overcome the vertical p-n-p transistor effect encountered with the diodes of the postamplifier pilot fabrications. When the separate resistor fabrication step is introduced, the postamplifier diodes (D_2 ,..., D_7 in Fig. 4.3) should be redesigned in the same manner. The question of whether diode D_1 should be retained (in which case it would also be modified) should also be answered. Its presence reduces the postamplifier's nominal gain, but it may have some value in terms of rendering the design less sensitive to variations of component parameter values.

Beyond the completion of the fabrication developments, a natural next step is to evaluate the monolithic pre/postamplifier combinations with respect to environmental

conditions anticipated in space applications. The most obvious of these are temperature and radiation. At this point one might also turn some attention to the question of mounting and encapsulation of the pilot run samples.