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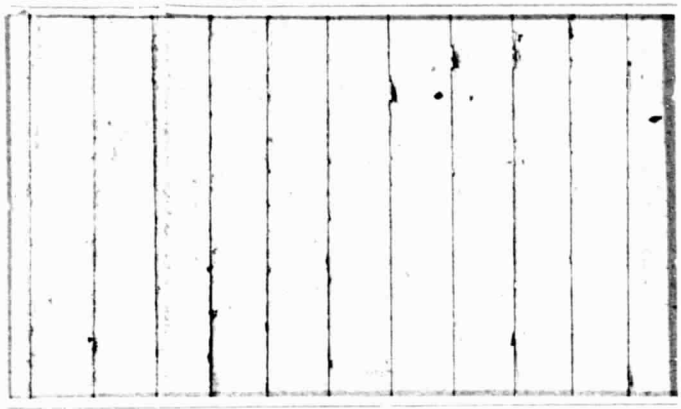

TEXAS INSTRUMENTS
INCORPORATED

FINAL REPORT
FOR THE
DESIGN AND DEMONSTRATION OF
AN ADVANCED DATA COLLECTION/POSITION
LOCATION SYSTEM

Prepared for

NASA-GODDARD
SPACE FLIGHT CENTER

Prepared by
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01-879210-F
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FOREWARD

The work described in this report was performed by the Space Systems Department, Equipment Group, Texas Instruments Incorporated, Dallas, Texas, under NASA Contract NAS 5-23599 for Goddard Space Flight Center. The reporting period is from August 1976 to July 1977. The technical director of this investigative program was James L. Coates. He was assisted by John F. DuBose Jr., James D. Quarfoot, and Joffrey K. Majors of the Space Systems Department and William L. Eversole of the Central Research Laboratory of Texas Instruments. Acknowledgement and appreciation are also due Earle Painter of GSFC for his constructive critiscism and suggestions throughout the course of the program.

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DESIGN AND DEMONSTRATION OF AN ADVANCED DATA COLLECTION/POSITION LOCATION SYSTEM

Final Report
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SECTION I
INTRODUCTION AND SUMMARY

A. INTRODUCTION

This report is the final report on a breadboard evaluation and demonstration program concerning the applicability of MSK modulation and chirp-z transformer technology in Advanced Data Collection/Position Location (ADC/PL) systems. The program effort consisted of three phases - design, testing, and evaluation. Section II describes the breadboard hardware built during the design phase of the program, Section III describes the tests conducted on the breadboard and the results of the tests, and Section IV presents a brief analysis and summary of the findings of the breadboard tests and developes a sample ADC/PL system which incorporates both MSK modulation and a chirp-z transformer.

B. BREADBOARD DESCRIPTION

The ADC/PL breadboard consists of four major hardware units or simulators - an MSK Transmitter Simulator, a Communications Link Simulator, a Search Subsystem Simulator, and a Receive Channel Simulator. The purpose of the breadboard is to collect experimental data to characterize MSK modulation and chirp-z transformer techniques and to demonstrate the applicability of

these technologies to ADC/PL type systems. To accomplish these tasks the breadboard was designed to be quite versatile so that parameters such as data encoding techniques, message formats, frequency deviation ratio, signal-to-noise ratio, etc. could be easily manipulated by switches. No attempt was made in the breadboard effort to finalize a satellite receiver configuration or a platform transmitter design, although efforts were made in the design of the breadboard to determine suitable implementation techniques for a final hardware design. Most of the test equipment required to evaluate the MSK and chirp-z transformer technologies were built into the breadboard hardware to provide a complete and customized test bed for evaluating the two technologies.

The MSK Transmitter Simulator contains a data generator, a data checker, and a coherent MSK modulator. The data generator can output either a selectable number of burst messages or a continuous stream of pseudo random data, and the format of the data in either case can be either NRZ or Manchester encoded. The data checker provides a means of comparing the data recovered by the Receive Channel Simulator against that transmitted by the data generator. Either burst messages or the continuous data stream can be monitored by the data checker. In the case of continuous data, the data checker outputs the number of bit errors detected for bit error type measurements, and in the case of burst messages the data checker outputs the number of correct messages received for probability of success type measurements. The coherent MSK modulator - were coherent implies the carrier is synchronous with the data clock - is a digital type MSK modulator based on the digital oscillator technique developed on the Random Access Measurement (RAMS) instrument. The carrier of the modulated output is at a baseband frequency of 20 kHz.

The Communications Link Simulator serves two functions - it simulates an r-f communications link and it houses two different hardware designs for implementing MSK modulation at an r-f frequency. The r-f communications link simulation is accomplished at an i-f of 10.7 MHz, which is a common i-f frequency that can be readily up-converted to an r-f frequency for transmission if so required at a later date. The input and output of the simulator are at baseband, and two separate oscillators are used for the up-conversion to 10.7 MHz and the subsequent down-converstion to baseband. This arrangement of separate translation oscillators allows the output of the simulator to be adjusted in baseband frequency from 10 to 40 kHz. Provisions are also included in the 10.7 MHz i-f of the simulator for summing wide-band, narrow-band, or CW interference in with

the signal to simulate unwanted signal and noise - like interference associated with r-f links. A hard limiter is also included in the 10.7 MHz i-f strip to simulate class C type processing of the MSK modulated signal.

The two MSK modulators housed in the Communications Link Simulator provide a means of evaluating the properties of MSK modulation when generated at an r-f frequency. The two types of modulators provided are a VCXO type modulator and a varactor phase shift modulator. The two modulators are non-coherent in that the 10.7 MHz carrier and the data clock are not synchronously related. These two modulators then, along with the coherent digital MSK modulator in the MSK Transmitter Simulator, provide a means of evaluating the differences between coherent and non-coherent generation of MSK modulation.

The Search Subsystem Simulator consists of a chirp-z transformer search unit coupled with threshold detection logic and receive channel assignment logic. Circuitry is also provided to measure the probability of detection and false alarm rate parameters of the search unit. Two different types of charge-coupled devices are alternately used in the chirp-z transformer circuitry - an apodized chip specifically designed to minimize the sidelobes or spectral spreading resulting from strong signals and a standard non-apodized chip. The assignment circuitry, upon receiving a signal detected indication from the threshold detector, generates a local mixing frequency which is used to place the detected signal in the center of the i-f band of the receive channel. The output of the simulator is the incoming MSK modulated baseband signal translated to an i-f of 180 kHz, which is the center frequency of the receive channel.

The Receive Channel Simulator consists of a non-coherent MSK demodulator and data detector for demodulating and recovering the NRZ data stream and a frequency measurement circuit for performing the frequency measurements. Three different types of non-coherent demodulators were built and tested. The last two demodulators to be built and tested were built in an attempt to improve the E/N_o performance measured on the first demodulator. The last two demodulators are not included in the hardware description of Section II, but are described in Section III under MSK non-coherent demodulator test results. The frequency measurement circuitry, in conjunction with the implementation of the phase lock loop in the non-coherent demodulator, is designed to provide an 0.1 Hz measurement resolution.

Although the ADC/PL breadboard was configured to interface with either a coherent or non-coherent demodulator, time did not allow construction of the coherent demodulator (which theoretically can demodulate MSK modulation and recover the NRZ data with an E/N_o performance equivalent to that obtainable with coherent PSK demodulation circuits).

C. DESCRIPTION OF TESTS

The tests conducted on the ADC/PL breadboard are divided into four categories - chirp-z transformer tests, MSK demodulator/data detector tests, frequency measurement tests, and system throughput tests - with the majority of the testing devoted to characterizing the chirp-z transformer and the non-coherent MSK demodulator/data detector. The tests conducted on the chirp-z transformer include

- Dynamic range tests
- Bin spreading tests (mutual interference)
- Probability of detection tests for different false alarm rates
- Coefficient utilization tests (using only real vs. real and imaginary spectral coefficients in the signal detection process)

All of the tests listed above were conducted using both apodized and non-apodized charge-coupled device transversal filters in the chirp-z transformer. Although tests were not specifically conducted, discussions are also included in Section III concerning the temperature characteristics of charge-coupled devices and the search times and channel reassignment times achievable with a chirp-z transformer implemented search unit.

The tests conducted on the Receive Channel Simulator include

- Bit error rate vs. E/N_o tests for both types of non-coherent MSK demodulators
- Frequency measurement accuracy vs. signal-to-noise ratio tests
- Tests comparing linear and class-C transmission of MSK signals in terms of spectral spreading of the MSK signal and the E/N_o performance of the non-coherent demodulator/data detector.
- Tests comparing coherent and non-coherent generation of MSK modulation in terms of E/N_o performance of the non-coherent demodulator/data detector.
- Bit error rate vs. E/N_o for different frequency deviation ratios

The primary non-coherent demodulator/data detector used in the Receive Channel

Simulator tests was a carrier tracking phase lock loop demodulator with the phase lock loop phase detector followed by a differentiator providing the demodulation of the MSK signal. Tests were conducted on the different components of this demodulator/data detector to itemize the contributions the different components made to the total loss in E/N_o performance as compared to that theoretically obtainable.

The final set of tests conducted on the ADC/PL breadboard are throughput tests utilizing all the equipment in the breadboard as an integrated system. The throughput test is conducted by having the MSK Transmitter Simulator generate an MSK signal which is routed through the Communications Link Simulator, detected and assigned to the receive channel in the Search Subsystem Simulator, demodulated and detected in the Receive Channel Simulator, and verified for proper reception in the error checker housed in the MSK Transmitter Simulator. The purpose of the test is to demonstrate the applicability of MSK modulation and chirp-z transformers to ADC/PL systems and to verify that the overall throughput test results agree with the test findings of the individual chirp-z transformer and MSK demodulator/data detector tests. To demonstrate compatibility between the MSK and chirp-z transformer technologies, the measured results of the throughput tests are compared against calculated results based on data taken from the individual chirp-z transformer and MSK demodulator/data detector tests.

D. CONCLUSION

Data collection/position location systems implemented using low polar orbiting satellites are characterized as time-limited, band-limited systems. As a result, the key to improving the serviceability of such a system, or the number of users that can be accommodated by such a system, is to improve the efficiency in which the system uses the time and bandwidth available. The choice of MSK modulation and chirp-z transformers is directly aimed at improving these two key parameters. MSK modulation is shown to possess an extremely efficient utilization of bandwidth in that 99% of the spectral energy is contained within a double-sided bandwidth of 2.3 times the data rate. A chirp-z transformer implemented search unit is found to search the designated system bandwidth for the presence of signals in a time span equal to the analyzing bandwidth of the search unit - thus providing a very efficient utilization of time.

The chirp-z transformer implemented search unit was found to be superior to the RAMS search unit in every aspect. The probability of detection curves were superior to those obtained on RAMS, a dynamic range of 30 dB was found to be acceptable, bin spreading in the presence of signals separated in power by up to 30 dB was less than that experienced on RAMS for a 10 dB range of signals, and, most importantly, the search time for the same system bandwidth was reduced over an order of magnitude over the search time required in the RAMS instrument. The MSK modulation format did exhibit excellent spectral characteristics. The mutual interference band for signals as great as 30 dB apart in signal power was calculated to be approximately 3.5 times the data rate of the modulated signal, as compared to eight times the data rate for $\pm 60^{o}$ PSK signals - as measured on the RAMS instrument. The non-coherent MSK demodulator/data detector did not perform as well in terms of E/N_o performance, being 2.5 dB worse in performance than the PSK demodulator used in the RAMS instrument. The coherent MSK demodulator should show a significant improvement in E/N_o performance over that obtained with the non-coherent demodulator, since MSK modulation can theoretically be treated as a PSK modulation format with equivalent E/N_o performance if coherently demodulated. Unfortunately, time did not allow the implementation of the coherent demodulator.

Had MSK modulation and a chirp-z transformer been used on the RAMS instrument - with all parameters constant except the length of the CW preamble and the transmitted power - the number of serviceable platforms in the field of view could have been increased from the goal of 200 to over 800. For an ADC/PL system with a 100 kHz bandwidth and ten watt transmitters in the user platforms, a user community of approximately 2500 could be accommodated in the satellite field of view.

In conclusion, the findings of this breadboard program definitely show that MSK modulation and chirp-z transformers are vital technologies for maximizing the serviceability of future data collection/position location system.

SECTION II

HARDWARE DESCRIPTION

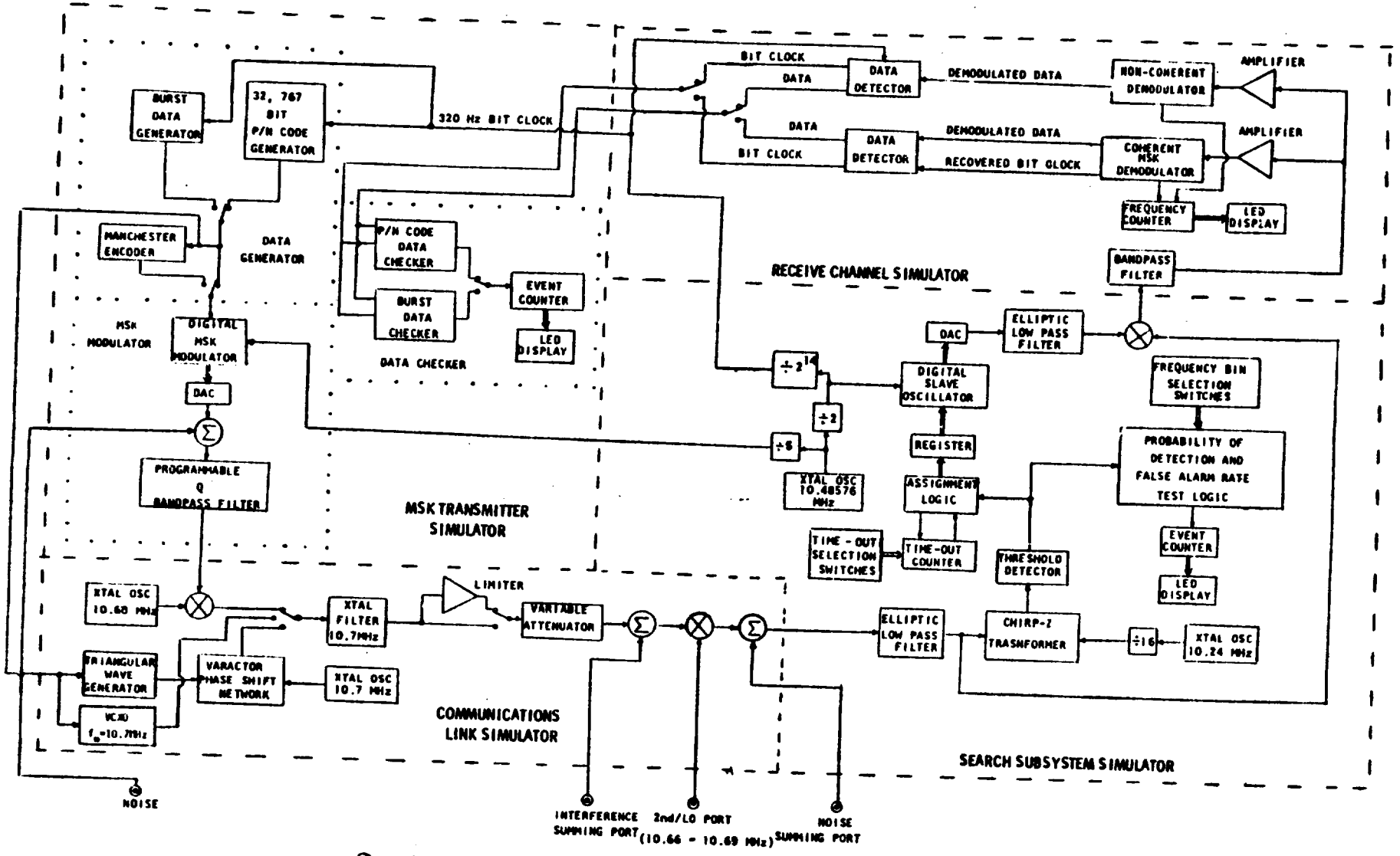
A. INTRODUCTION

This section describes the special-purpose hardware specifically designed to demonstrate an Advanced Data Collection/Position Location (ADC/PL) system. Figure 2-1 shows the breadboard configuration for the ADC/PL system and, as shown, the system consists of four major hardware units or simulators - an MSK Transmitter Simulator, a Communications Link Simulator, a Search Subsystem Simulator, and two different implementations of a Receive Channel Simulator. The implementation of each of these four major units is presented to a detailed block diagram level following a brief discussion of the features incorporated into each of the four simulators and the frequency plan adopted for the breadboard system.

B. BREADBOARD SYSTEM FEATURES

The utilization of the breadboard system is twofold. The first objective is to collect experimental data to characterize MSK modulation and chirp-z transform techniques and verify the applicability of these technologies to data collection and position location requirements. The second objective is to demonstrate the usage of the two technologies in data collection type systems by conducting simulated throughput tests. It is evident from these objectives that the hardware must be flexible in design to accommodate the various tests and parameter characterization studies required.

Before listing the features and programmable options incorporated into each simulator, the function of each simulator will be briefly described. The MSK Transmitter Simulator provides an MSK modulated data stream and also contains error detection facilities for verifying the



MSK/CHIRP-Z TRANSFORMER BREADBOARD CONFIGURATION

Figure 2-1

proper recovery of the modulated signal in the Receive Channel Simulator. The Communications Link Simulator serves not only to simulate a communications link by allowing interferring tones and front end receiver type noise to contaminate the received signal, but also contains MSK modulation circuitry to determine the feasibility of implementing the MSK modulation format at the final RF stage. The Search Subsystem Simulator contains a chirp-z transformer - implemented with charge coupled devices and associated logic - to implement a search and detect technique for locating incoming MSK modulated transmissions and assigning a receiver/demodulator channel to the detected signal. The two Receive Channel Simulators provide a means of characterizing both coherent and non-coherent demodulation techniques and weighing the E/N_o performance of each technique against hardware complexity and platform transmission time.

The following lists, which show the capabilities and options available within each major hardware unit, indicate substantial versatility and programmability is provided to accommodate the required characterization and throughput tests.

1. MSK Transmitter Simulator Features

   a. Modulation Format - the modulation format is selectable between either MSK modulation or FSK modulation. In the case of FSK modulation, the deviation ratio can be varied from 0.1 to 10.0 in steps of 0.1.

   b. Encoding Format - The format of the digital data stream prior to modulation can be selected to be either non-return-to-zero (NRZ) or Manchester (split-phase).

c. Message Format - A message can consist of either a 32,767 bit P/N code or a burst of selectable data of programmable length. For the case of burst data type messages, the following programmability features are provided:

(1) CW Preamble - The CW preamble is programmable in length from 0 to 99 bits in one bit increments.

(2) Bit Synchronization Code - The bit synchronization code can be varied in length from 0 to 99 bits in one bit increments. The bit pattern of the code is also programmable in that logic ones and zeroes can be chosen to be alternated in bit groups of one, two, three, four, five, six, eight, ten, twelve, or fifteen.

(3) Frame Synchronization Code - The frame synchronization code can be varied between 0 to 15 bits in length. In addition, the content or bit pattern of the code is programmable.

(4) Sensor Data - The data portion of the burst message can be varied in length from 0-255 bits. The bit pattern of the sensor data can be uniquely programmed for up to sixteen bits of sensor data. For sensor data formats longer than 16 bits in length, the unique 16-bit pattern selected will repeat.

(5) Number of Messages Transmitted. The number of messages transmitted can be varied between 0 and 999. A 255 bit period is fixed between successive burst message transmissions, and during this fixed "dead" time the MSK modulator is disabled. Also, at the conclusion of the selected number of transmissions, the MSK modulator is disabled.

d. Output Signal-to-Noise Adjustments - A separate noise input port for the summation of modulated signal and noise, in conjunction with the presence of a bandpass filter of adjustable noise bandwidth located at the final output stage of the MSK Transmitter Simulator, allows precise and adjustable settings of output modulated signal-to-noise ratios to be derived.

e. Modulation Center Frequency - The center frequency of the output modulated signal is set to the center frequency of the bandpass filter-which is 20.016 KHz.

f. Mark/Space Frequency Check - A switch is provided to allow the operator to continuously output either the mark frequency or the space frequency for frequency verification purposes and checkout of the coherent demodulator in the Receive Channel Simulator.

g. Data Checker - Circuitry is provided in the MSK Transmitter Simulator to accept bit clock and data from either the coherent or non-coherent Receive Channel Simulator and compare the data pattern recovered against the data pattern transmitted. Features of the data checking circuitry are:

(1) Either polarity of the recovered bit clock and digital data can be accommodated.

(2) Adjustable delay lines in the data checker allow accommodation of data recovery circuitry delays up to a maximum of three bit periods.

(3) For the continuous transmission of the 32,767 bit P/N code, a counter - the contents of which are displayed - records the number of bit errors

detected. This error count continues until the MSK Transmitter Simulator is reset.

(4) For the burst message format the data checker is configured to display the number of correctly received messages.

2. COMMUNICATIONS LINK SIMULATOR FEATURES

a. Input Requirements - The filtering in the Communications Link Simulator restricts the centering of the modulated input signal to 20KHz $\pm$ 6.5KHz.

b. Output Signal - The output of the Communications Link Simulator consists of the modulated input plus an interference tone, if desired. The output carrier frequency may be adjusted over the range of 25KHz $\pm$15KHz.

c. IF Throughput Frequency - The input is up-converted to a working IF frequency of 10.7MHz. The choice of 10.7MHz allows the use of commercial off-the-shelf equipment to achieve a final r-f output.

d. Linearity - All amplification and translation processes are linear class A type processes. Provision is made, however, to insert by switch selection a hard-limiter at the output of the final 10.7 MHz stage prior to down-conversion. This feature is included to examine what spectral spreading of the MSK signal, if any, will result from using non-linear class C type power amplifiers in an r-f transmitter. Another question that will be addressed by this feature is the amount of degradation, if any, that occurs in the MSK demodulation process as a result of non-linear processing of the transmitted signal.

e. External Inputs - In addition to the MSK modulated baseband signal input port, three other input ports are provided. One input is the down-conversion local oscillator port which can be driven from a commercial type frequency synthesizer. Another input provides a means of summing noise or interference with the modulated tone at the final IF frequency of 10.7 MHz. The third port is for inputting a serial digital data stream to be used in implementing the MSK modulation format at the 10.7 MHz IF frequency.

f. IF Implementation of MSK Modulation Format - Capability is provided to implement the MSK modulation format at the IF working frequency of 10.7 MHz. Two implementation techniques are provided - a varactor type phase shift network driven by a ramp generator controlled by the digital data stream and a VCXO whose gain is adjusted to provide the mark and space frequencies when driven by the serial digital data stream. These modulation techniques are provided to evaluate the feasibility of accomplishing the MSK modulation format at the final RF stage - thereby eliminating any up-conversion processes.

3. Search Subsystem Simulator Features

a. Chirp-z Transformer Parameters - the chirp-z transformer is a 500 point transform yielding 250 real frequency coefficients and 250 imaginary frequency coefficients. The critical parameters of the transformer are:

(1) Analyzing Bandwidth - 160 Hz

(2) Search Band - 0 to 40 KHz

(3) Search Time - 6.25 milliseconds

b. Assignment Logic Parameters

(1) Selection is provided to assign the Receive Channel

Simulator upon threshold detection either during the outputing of real frequency coefficients from the chirp-z transformer or during the outputting of both real and imaginary frequency coefficients. This feature allows data to be taken to determine if processing the imaginary spectral coefficients as well as the positive coefficients results in any improvement in the ratio of probability of detection to false alarm rate.

(2) Time-out logic is provided to inhibit the assignment of the Receive Channel Simulator to any threshold occurrence once an assignment is made. The duration of the time-out window can be adjusted from 0 to 1.0 second in increments of 1.0 millisecond.

(3) The activation of the assignment logic can be restricted, by switch selection; to only that time period when an actual message is being transmitted by the MSK Simulator. The selection of this capability reduces the probability of burst type messages being missed because the Receive Channel Simulator has been assigned to a noise occurrence. The restriction effectively simulates a complex time-out assignment sequence whereby the Receive Channel Simulator is interrogated for an in-lock condition, the proper reception the frame synchronization code, etc.

(4) The format of the channel assignment as output by the assignment logic is a sinusoidal signal of proper frequency such that the incoming signal, when up-converted by the sinusoid, will be centered at 180KHz.

c. Assignment Logic Self Test Functions - Several test features are incorporated into the assignment logic to provide a ready means of characterizing the chirp-z transformer. The two major test configurations implemented are:

(1) Probability of Assignment Test Mode - In this test mode the output of the threshold detector following the chirp-z transformer is interrogated for an event at a selectable frequency bin. If a detection is present, a counter is updated. The counter will continue to be updated until a selectable number of spectral sweeps have been completed, at which time the test is terminated. A seven segment LED display is included in the Simulator to display the counter's content.

(2) False Alarm Test Mode - This test mode is identical to the probability of assignment test mode except that the output of the threshold detector is interrogated at every frequency bin rather than just one particular frequency bin.

4. Receive Channel Simulator Features

(a) Coherent Demodulator

(1) A coherent demodulator utilizing two phase lock loops is provided to coherently recover the bit

clock and the NRZ digital data stream from the incoming MSK modulated signal.

(2) Another function of the coherent demodulator is to display by means of a seven segment LED display the frequency of the incoming modulated signal. A counter drives the LED display. The counter counts the zero crossings of an oscillator which is phase locked to the mark frequency of the incoming MSK modulated data, and thus records the mark (upper) frequency of the received signal. The accuracy of the frequency measurement is $\pm$ 0.1 Hz.

(b) Non-Coherent Demodulator

(1) A non-coherent technique for demodulating the MSK signal is accomplished using an FM discriminator type demodulation technique. A phase lock loop is utilized to track the modulation carrier, with the data discrimination accomplished by differentiating the output of the phase lock loop's phase detector.

(2) Data recovery is accomplished by using a bit sync clock as supplied by the MSK Transmitter Simulator to drive a data detector located at the output of the demodulator.

(3) The frequency measurement circuitry is that circuitry utilized in the coherent demodulator.

C. Breadboard Frequency Plan

A diagram showing the allocation or assignment of frequencies is shown in Figure 2-2. The key frequency assignments are:

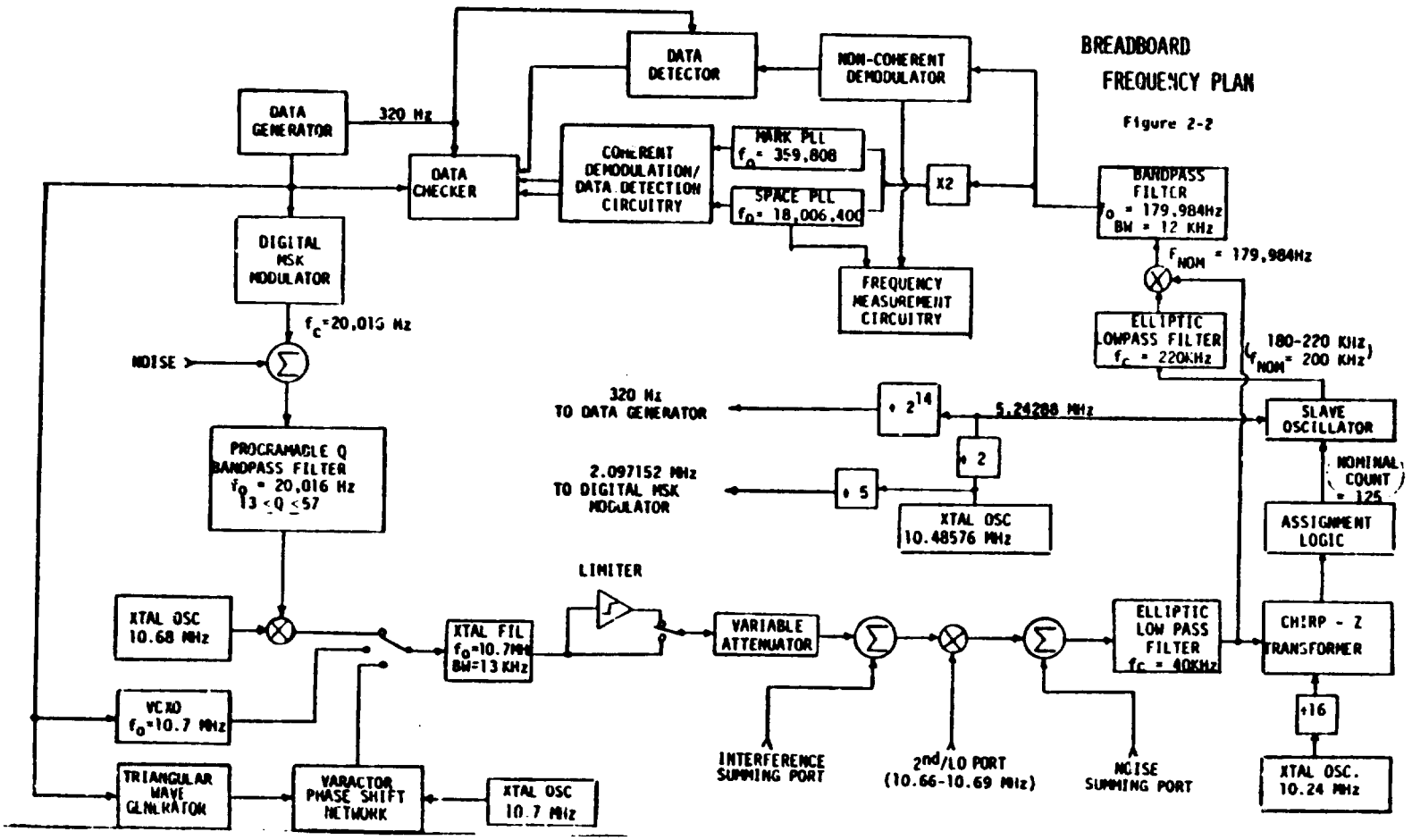
Digital Data Bit Rate	-	320 Hz
Digital MSK Modulator Carrier	-	20,016 Hz
Final I-F throughput Frequency	-	10.7 MHz
Chirp-z Transformer Search Band	-	0-40 KHz
Receive Channel Input Frequency	-	180 KHz

The criteria used to select the above frequencies was not one of optimization in terms of minimizing the number of serviceable mobil and fixed platforms for a given frequency band allocation, but rather to simplify the breadboard hardware and use where possible existing designs or commercial equipment. While simplifying hardware and hardware design tasks, the frequencies selected also provide the opportunity to examine and demonstrate all pertinent properties of both MSK modulation/demodulation techniques and the chirp-z transformer as a search system.

The principle driving force in selecting the above frequencies was the existence of a proven design for a 500-point chirp-z transformer capable of running at a basic clock rate no greater than 750 KHz. The chirp-z transformer utilizes a four phase CCD chip, with the four phases being derived by dividing down the basic input clock by a divide-by-eight countdown circuit. The effective maximum rate in which the CCD cells can be clocked then is 93.75 KHz -- which results in a total of 5.33 milliseconds being required to clock a given sample through all 500 cells. A maximum throughput rate of 5.33 milliseconds equates to a maximum analyzing bandwidth of 187.5Hz and a maximum search band of 46.875KHz. With these limitations, it was decided to implement a search system which covered the same frequency search band as did the Random Access Measurement instrument for ease in comparing the performance of the two systems.

BREADBOARD
FREQUENCY PLAN

Figure 2-2



A basic clock rate of 640KHz yields such a system by creating a frequency search range of 0-40 KHz. The analyzing bandwidth which results is 160Hz.

The next assignment made was the carrier frequency of the baseband digital MSK modulator. Here the decision was made to place the carrier near the center of the chirp-z transformer search band to allow maximum flexibility of carrier adjustment via the frequency translation processes contained in the Communications Link Simulator. The exact carrier frequency chosen-20,016 Hz- was picked as it falls as near to the center of the frequency search band of the chirp-z transformer as is possible to achieve-considering the 32 Hz frequency resolution limitation of the digital MSK modulator.

The frequency resolution of the digital MSK modulator-32Hz-directly defines the digital data rate or bit clock frequency. The modulation format of the digital MSK modulator is one of continuous phase FSK modulation with the modulation index variable from 0.1 to 10.0 in steps of 0.1. A modulation index of 0.5 defines MSK modulation - which is but a special case of continuous phase FSK modulation. With a frequency resolution of 32 Hz in the digital MSK modulator and a modulation index resolution requirement of 0.1, the data rate is uniquely defined to be 320 Hz. The only question then is why a resolution limitation of 32 Hz in the digital MSK modulator. A finer frequency resolution would require a basic clock higher than the 2.097152 MHz clock used; and although a higher clock rate is feasible, the added expense and complications associated with a higher clock rate cannot be justified in terms of the objectives of the breadboard hardware. The choice of a basic clock frequency as high as 2.097152 MHz is necessary, however, to minimize the effects of the discrete nature of the digital MSK modulator by sampling the carrier frequency at a rate one hundred times faster than the carrier frequency itself. With a basic clock requirement as high as 2.097152 MHz, the 32 Hz resolution limitation is chosen as it divides into 2.097152 MHz by a power of two (2^{16}) - which is a requirement

for the digital technique implemented - and it can be easily achieved by using only four 4-bit arithmetic stages in the digital oscillator portion of the digital modulator.

The Communications Link Simulator uses an i-f throughput frequency of 10.7 MHz - which is a standard i-f frequency frequently used as an intermediate frequency in r-f equipment. The choice of a standard i-f such as 10.7 MHz allows the use of standard off-the-shelf hardware, such as crystal filters, in implementing the Communications Link Simulator. Also, the 10.7 MHz i-f can be readily used to both drive a commerical off-the-shelf r-f translator/ transmitter and serve as the final i-f output frequency of a commerical receiver should it ever become necessary to expand the ADC/PL breadboard to have r-f transmission/reception capability.

The last key frequency assignment required is that of the center or receive frequency of the Receive Channel Simulator. The Search Subsystem Simulator, upon detecting the presence of a signal, assigns the detected signal to the Receive Channel Simulator by outputting a sinusoid of proper frequency such that the incomin signal, when mixed with the sinusoid will fall within the receive channel bandwidth of the Receive Channel Simulator. The selection of the receive frequency, or the frequency range of the sinusoid output by the Search Subsystem Simulator, is influenced by two conflicting requirements. The coherent demodulation technique requires quite stable crystal controlled VCXO's, which are readily available only at the higher frequencies, to provide acquisition discrimination in the two phase lock loops between the mark and space frequencies. On the other hand the implementation of the sinusoid output by the Search Subsystem Simulator and the bandwidth or Q limitations of the bandpass filter which follows the mixing of the incoming signal with the sinusoid place a limitation on how high the Receive Channel Simulator center frequency can be. The choice of the nominal center

frequency of 179,984 Hz is a compromise between the two conflicting requirements.

The VCXO center frequencies for the two phase lock loops in the coherent MSK demodulator are a direct fallout of the center frequency selection in the Receive Channel Simulator. For a nominal center frequency of 179,984Hz, the MSK modulation format yields a space or logic zero frequency of 180,064 Hz and a mark or logic one frequency of 179,904 Hz. Allowing for the frequency doubler, the phase lock loop assigned to the mark frequency will have a VCXO center frequency of 359,808 Hz. The center or rest frequency of the VCXO in the space frequency phase lock loop is complicated by the requirement that the VCXO also provide the clock input for implementing the frequency measurement. To transmit a nominal data message of 64 bits requires 200 milliseconds in time for a 320 bps data rate. To accomplish a 0.1 Hz measurement accuracy in 200 milliseconds requires the measured clock or VCXO output to be fifty times the actual frequency to be measured. The space VCXO must then be followed by a divide-by-fifty counter so that the VCXO itself can run at a frequency fifty times the incoming space frequency. This results in a VCXO rest frequency for the space phase lock loop of 18,006,400 Hz.

D. MSK Transmitter Simulator

The MSK Transmitter Simulator consists of three major subunits - a digital data generator, a data checker, and an MSK modulator. The digital data generator can operate in one of two modes. It can output a 320 bps data stream of random data bits as generated by a 32,767 bit P/N code generator or it can output structured bursts of data with each data burst consisting of a CW preamble, a bit synchronization code, a frame synchronization code, and data. The structure of each transmission is fully programmable in that the CW preamble, bit synchronization code, frame synchronization code, and data may all be varied in length and all but the CW preamble may be programmed in terms of data or code content. In the case of the burst message mode, each message is separated in time from the previous message by 800 milliseconds and a provision is also incorporated in the hardware implementation to transmit a selectable number of transmissions and then halt all transmissions. This feature allows message reception statistics to be easily measured. The digital data output by the data generator can be selected to be either Manchester (split-phase) or NRZ encoded data.

The data checker provides a means of comparing the data received by the Receive Channel Simulator with the data output by the data generator. Because of the two data modes available in the data generator, the data checker must contain two data checking facilities - one for handling the P/N code data and one for handling the burst messages. The P/N code data mode is used primarily to facilitate bit error measurements, and as such the output of the data checker in the P/N data mode will be a displayed count showing the time accumulated number of bit errors detected. By accumulating an error count for a pre-determined period of time, bit error rate measurements for various signal-to-noise ratios can be easily made. The burst data mode is

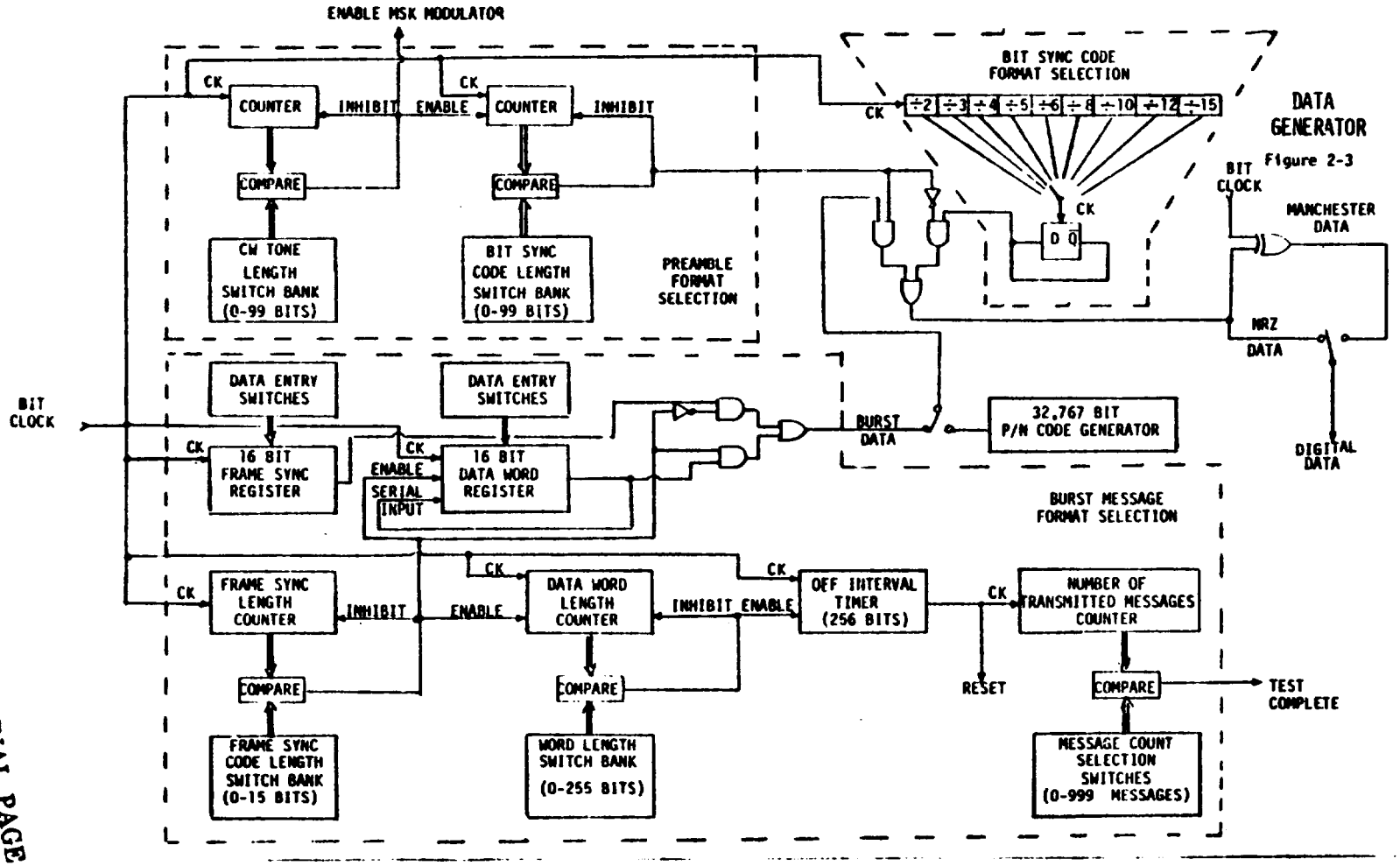
used primarily to test the dynamics of the overall ADC/PL breadboard system. In this mode the interest is primarily concerned with questions such as can bit synchronization be established within the code length assigned to the bit synchronization code, can the search system detect the presence of signal and assign the Receive Channel Simulator within the time allocated to the CW code preamble, etc. The output of the data checker in the burst data mode then is a count display showing the number of correct messages received. If, for example, the data generator were programmed to transmit 500 burst messages, and at the conclusion of 500 transmissions the data checker displayed a count of 495, the probability of successfully receiving each transmission is 99.0 %. The count displayed then effectively represents the probability of success, and critical parameters governing the successful detection and reception of messages can be easily plotted as a function of the probability of success, with the signal-to-noise ratio serving as an independent parameter to create a family of curves.

The ADC/PL breadboard system contains three MSK modulators. The MSK modulator housed in the MSK Transmitter Simulator is an adaption of the digital oscillator technique developed for the Random Access Measurement System. The effective carrier of the modulated output is at 20.016 KHz. Although a higher carrier could be implemented, the technique does impose frequency restrictions which inhibit implementing the modulation at the final r-f carrier. The use of the digital oscillator technique to achieve the MSK modulation format will thus require up-conversion circuitry to translate the modulation carrier to the final r-f frequency. For this reason two additional MSK modulators are implemented in the Communications Link Simulator to test techniques for implementing MSK modulation at the final r-f carrier frequency.

The primary reason for having the digital oscillator type MSK modulator is that it is a very low risk technique of obtaining the proper MSK modulation format. In addition, the digital implementation provides a ready means of implementing coherent FSK modulation. The digital oscillator modulation technique is designed so that the deviation (ΔF/data rate) ratio can be varied from 0.1 to 10.0 in steps of 0.1 - where MSK modulation is but a special case of coherent FSK utilizing a deviation ratio of 0.5. The ability to vary the deviation ratio allows MSK modulation to be compared against other coherent FSK deviation ratios using the non-coherent demodulator in the Receive Channel Simulator. The digital MSK modulator also contains a programmable Q bandpass filter which is used to ascertain the effect of transmission bandwidth on the bit error performance of the coherent MSK demodulator, as well as the non-coherent MSK demodulator, in the Receive Channel Simulator.

D.1 Data Generator

A detailed block diagram of the data generator is presented in Figure 2-3. Upon initiating a transmission, a CW tone length counter in the preamble format selection circuitry begins counting data clocks. When the count in the counter equals the count selected in the CW tone length switch bank, the counter is disabled and a bit sync code length counter is enabled to count data clocks. During the time the CW tone length counter is active an inhibit signal is output to instruct the MSK modulator to transmit carrier only - i.e., no modulation. Upon activating the bit sync code length counter, the data generator begins outputting the bit synchronization code. The format of the code is selectable and may consist of an alternating one-zero data pattern or alternating groupings of ones and zerors - with the groupings consisting of two, three, four, five, six, eight, ten, twelve, or fifteen bits of logic ones followed by the same number of logic zeroes. The provision



to select the format of the bit synchronization code was incorporated into the data generator to allow different bit synchronization codes to be evaluated in characterizing the acquisition properties of the coherent MSK demodulator. When the count in the bit synchronization code length counter equals the count selected in the bit sync code length switch bank, the counter is deactivated and the data generator begins outputting the 32,767 bit P/N code or the frame synchronization code portion of a burst message. Both the CW preamble and the bit synchronization code may be individually adjusted in length between 0 and 99 bit periods in increments of one bit period. It is also noted that regardless of whether the P/N code or burst message data mode is selected, the initial part of the message consists of a CW preamble followed by a bit synchronization code. This preamble occurs for every burst message transmitted, but only occurs once for the continuously transmitted P/N code - unless a reset button is pushed to re-initiate the data generator.

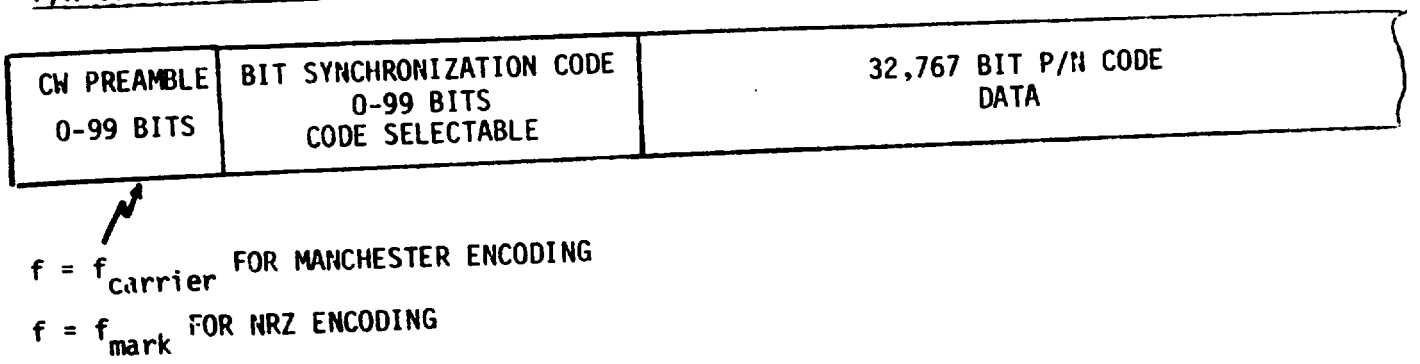
The burst message format selection circuitry structures the data portion of a burst message transmission. At the completion of the bit synchronization code, a frame sync code length counter is enabled and begins counting data clocks. At the same time, a frame sync register, which has been previously loaded with the frame synchronization code as selected by the frame sync data entry switches, begins serially shifting out the frame synchronization code. The length of the frame synchronization code is adjustable between 0 and 15 bits in one bit increments and is determined by the setting of the frame sync code length switch bank. When the count in the frame sync code length counter equals the count selected in the switch banks, both the frame sync counter and register are disabled and a data work length counter and a data word register are enabled. The data word content and length are selected in exactly the same manner as the frame synchronization code, except that the data content may be uniquely defined

for only sixteen bits while the word length may be varied from 0 to 255 bits in increments of one bit. As the data is serially shifted out of the data word register, it is routed at the same time back to the serial input of the register. For data word lengths greater than 16 bits, the 16-bit message selected by the data word data entry switches is repeatedly transmitted, as a whole or a portion thereof, until the count in the data word length counter equals the count selected in the word length switch bank. At this time both the counter and register are disabled and the time-out or interval timer is activated. At this same time an inhibit signal is activated to disable the MSK modulator.

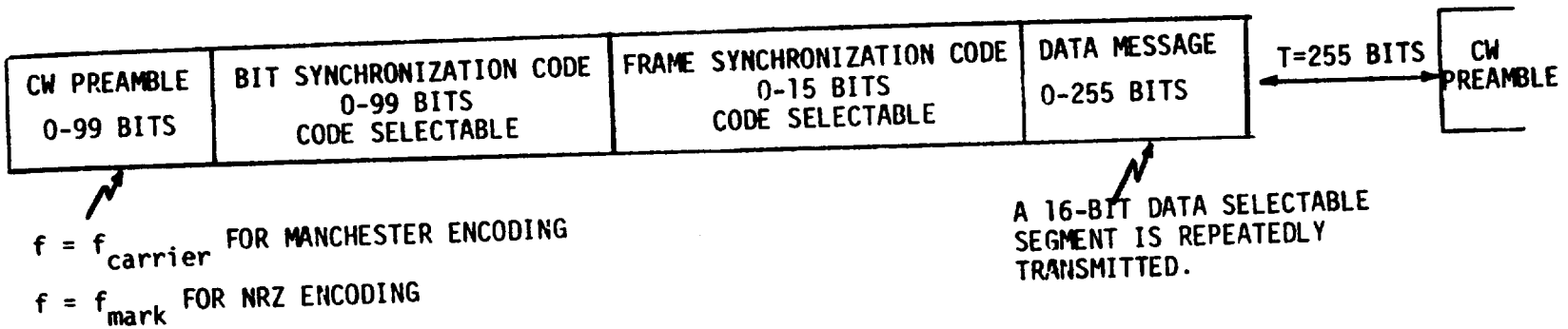
The interval timer in the burst message format selection circuitry counts data clocks for a fixed interval of 256 bit periods - which is 800 milliseconds for a 320 Hz data clock. At the conclusion of the time-out interval the MSK modulator inhibit signal is deactivated, a reset pulse is generated to instruct the data generator to begin a new transmission by activating the CW tone length counter, and a transmitted message counter is updated by one count. The purpose of the transmitted message counter is to allow the number of burst messages transmitted to be selectable. When the count in the transmitted message counter equals the count selected in the message count selection switches - which can range from 0 to 999 in increments of one, the automatic generation of the reset pulse at the conclusion of a time-out interval is disabled. The data generator is then deactivated and may be re-activated only by manually depressing the reset push button switch.

The formats of the messages as assembled by the data generator are shown in Figure 2-4. It is noted that for both the P/N code data selection and the burst message data selection, the beginning of the transmission consists of a CW preamble followed by a bit synchronization code. For the P/N code format, the pseudo-random data follows the bit

P/N CODE DATA FORMAT



BURST MESSAGE DATA FORMAT



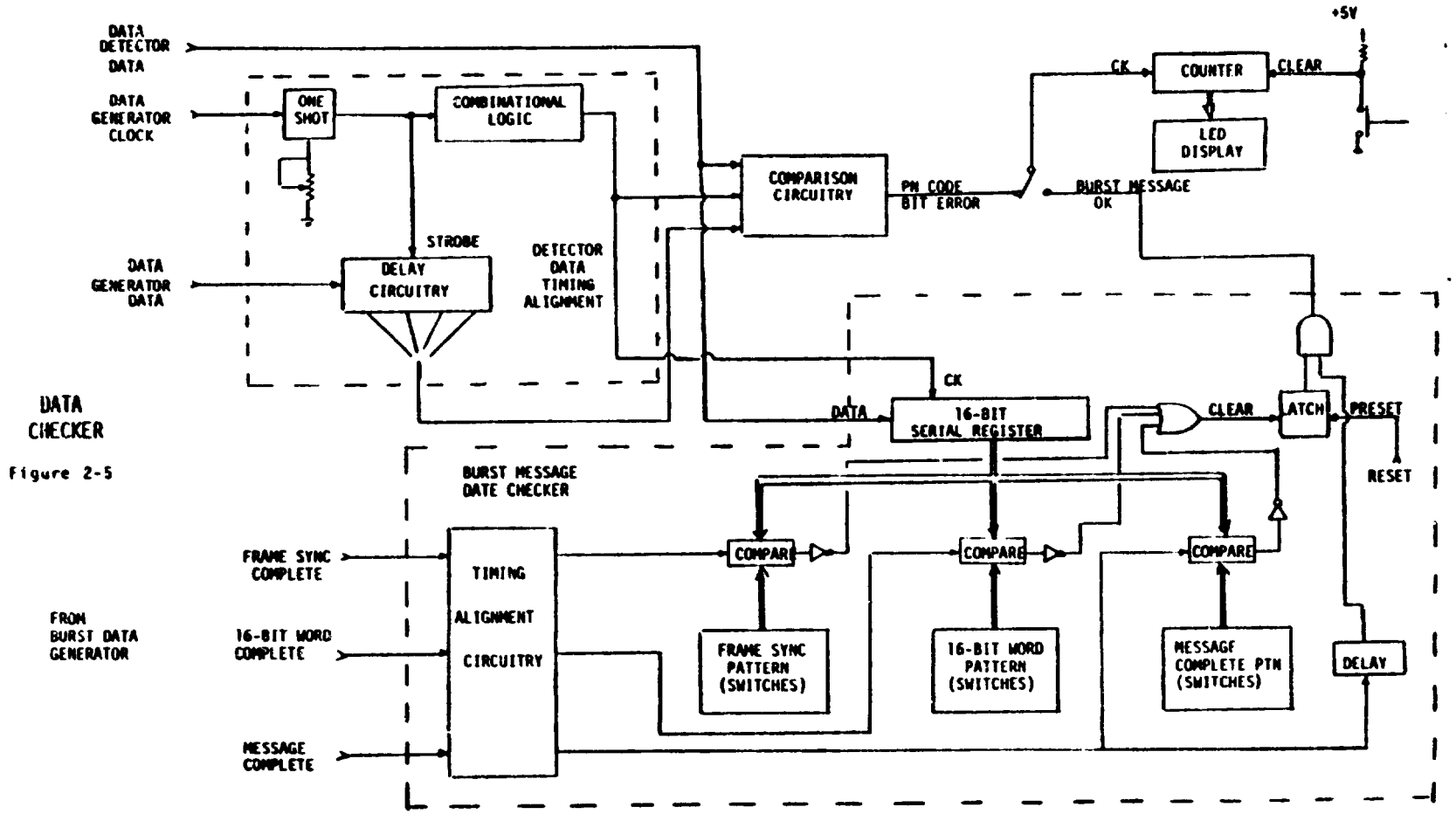
DATA GENERATOR MESSAGE FORMATS

Figure 2-4

synchronization code, while for the burst message format the frame synchronization code and data follow the bit synchronization code. The frequency generated by the MSK modulator during the CW preamble depends on whether the serial data stream output by the data generator is NRZ or Manchester (split-phase) encoded. The use of two different frequency values during the CW preamble is due to the preference of different frequency preambles by the coherent and non-coherent demodulators in the Receive Channel Simulator. For the coherent demodulator, which is capable of recovering NRZ encoded data, the mark frequency is transmitted during the CW preamble as it falls in the center of a frequency bin in the Search System Simulator. In order that the two phase lock loops in the coherent demodulator uniquely lock to the mark and space frequencies, the pull-in range of the two loops must be less than the frequency separation of the mark and space frequencies. This requirement disallows any uncertainity in the assignment pattern of the Search System Simulator and for this reason the frequency transmitted during the CW preamble resides at the center of a frequency bin. It should be noted however that this is not a "real" problem since it can be readily resolved by simply making the analyzing bandwidth of the Search System Simulator less than half the bit rate clock of the transmitted message. For the breadboard system, however, this was not practical with the chirp-z transformer design utilized. For non-coherent demodulation, the demodulator implemented in the Receive Channel Simulator requires a component of carrier to always be present. For this reason then Manchester encoding is always used when non-coherent demodulation tests are being conducted. To allow the non-coherent demodulator to initially acquire the carrier, the CW preamble frequency for Manchester encoding is set at the carrier frequency.

D.2. Data Checker

A detailed block diagram of the data checker is shown in Figure 2-5. The data checker consists of detector data timing alignment circuitry, burst message data checker circuitry, and comparison and event counter circuitry. The demodulation and data recovery circuitry in the Receive Channel Simulator recovers the transmitted data, but the recovered data will not be in phase with the data output by the data generator due to delays encountered in the circuitry. To compare the data received against the data transmitted, the phase error must be removed. The detector data timing alignment circuitry delays the bit clock and data generator data by an adjustable amount so that it will match the phase of the data output by the Receive Channel Simulator. The alignment is accomplished by adjusting the phase of the data generator data clock by an adjustable one-shot until the leading edge of the clock coincides with the leading edge of the recovered bit clock. The delayed clock is then used to load the data generator data serially into a four stage shift register. The data as it resides in the shift register is then in phase with the data recovered in the Receive Channel Simulator. To accommodate more than 360° or one bit interval of delay, a switch is provided to select the data from the shift register to be compared against the data output by the Receive Channel Simulator from any one of the four stages of the shift register. The data from the Receive Channel Simulator is also loaded into a single stage shift register, so that selecting data from the first stage of the four stage register accommodates phase shift discrepancies from 0° to 360°, the second stage shifts from 360° to 720°, etc. Additional circuitry is also provided to accomodate either phase of bit clock or data from the Receive Channel Simulator.



DATA CHECKER

Figure 2-5

For the P/N code data mode, the delayed data generator data and the data from the Receive Channel Simulator are compared one data bit at a time. If an agreement is not found on any one data bit, an error pulse is output which updates the event counter by one count. Over an interval of time then, the count in the counter displays the number of data bit errors that have occurred in the time interval.

For the burst data transmission mode, the question is not how many data bit errors have occurred but rather how many recovered messages had one or more bit errors. The burst message data checker circuitry is implemented to inspect an entire message and output a count pulse if and only if the recovered message has no errors in it. This results in the event counter displaying the number of messages correctly received. The data from the Receive Channel Simulator is input into a 16-bit shift register whose contents are compared against three banks of switches-a frame sync. pattern switch bank, a data word pattern switch bank, and a message complete switch bank. However, the recovered data will be appropriately aligned in the shift register to allow comparing against one of the switch banks only at specific points in time. These points in time are provided by compare enable signals output by the burst data format selection circuitry in the data generator. A frame sync complete signal signifies that the frame synchronization code has just been transmitted, a 16-bit word complete signal becomes true each time the programmable 16-bit word in the data word portion of the message has been transmitted in its entirety, and a message complete signal signifies that the last bit of the burst message has just been transmitted. This last signal is necessary as the data word length may not consist of an integer number of 16-bit words. When one of the three signals occurs, it enables a comparison to be made between the contents of the 16-bit shift register and the appropriate switch bank.

At the beginning of a message transmission a latch is preset to a logic one. If a comparison is not found when one of the three compare enable signals occurs, the latch is cleared. If the latch remains set through the entire period of transmission then, no errors were found. The latch output is gated with a delayed version of the message complete signal to generate an event pulse to update the event counter counting the number of correct messages received, and thus the latch must remain set if a received message is to be counted as an error free message reception. It is also noted that the three compare enable signals output by the burst data format selection circuitry must be delayed in the same manner as the data generator data clock so that the comparisons will be made at the proper points in time.

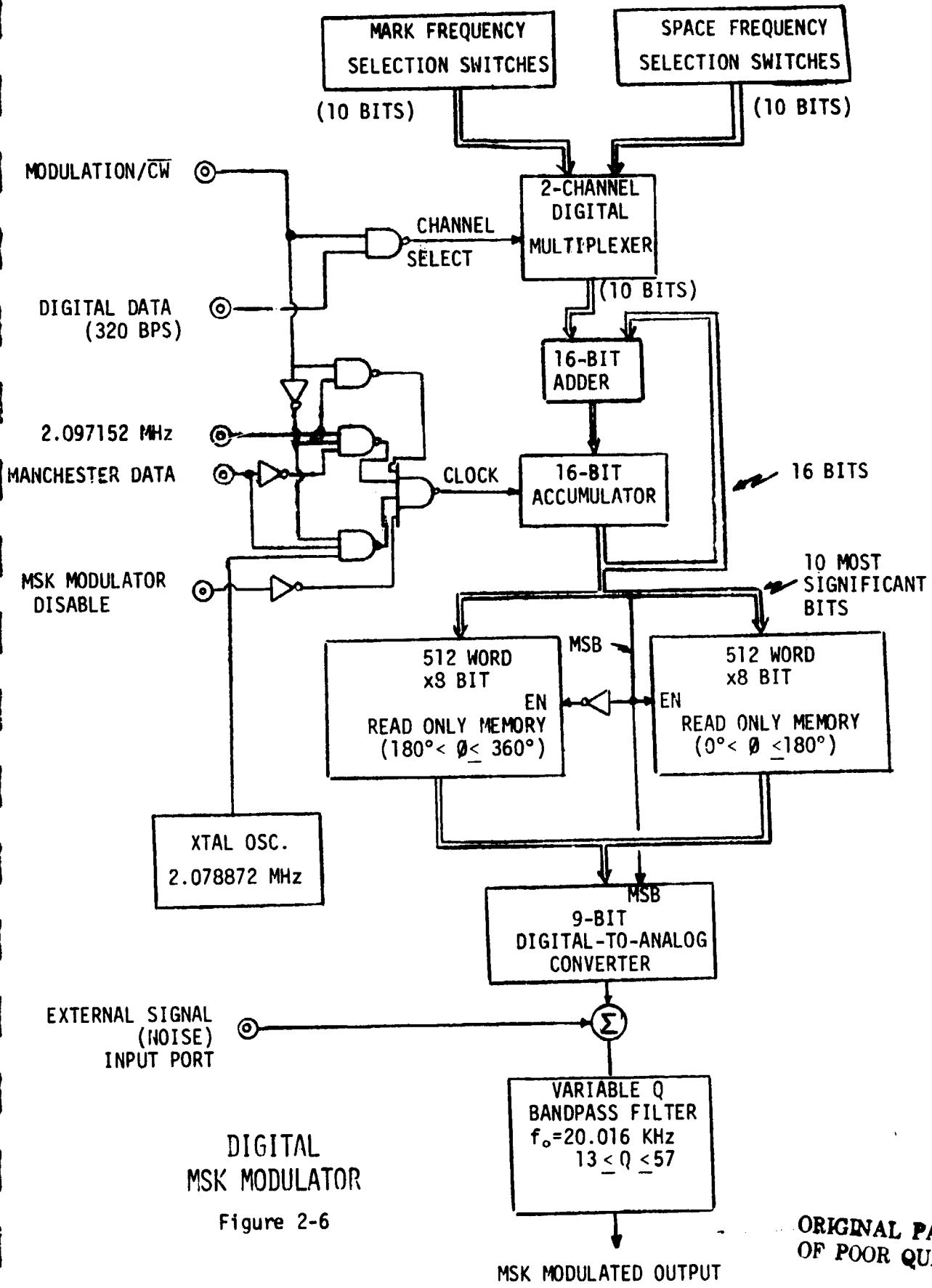
D.3 MSK Modulator

The MSK modulator housed in the MSK Transmitter Simulator is a digitally implemented modulator based on the digital oscillator technique developed on the Random Access Measurement System (RAMS) program. Two analog MSK modulator techniques are housed in the Communications Link Simulator, but the digital implementation offers two advantages not found in the analog implementations. The digital technique provides a more precise formulation of MSK modulation in that the deviation ratio (which is 0.5 by definition for MSK modulation) is precisely 0.5 for the digital technique while only approximated in the analog technique. The availability of both modulation schemes allows data to be taken on the effect of the "purity" of the MSK modulation on the performance of both coherent and non-coherent demodulation techniques. Also, the digital implementation technique provides a low frequency modulation carrier- 20.016 KHz

that can be directly input into the Search Subsystem Simulator and the Receive Channel Simulator. This direct interface capability allows data to be taken to determine the effect, if any, on the demodulation processes from non-coherently up-converting and down-converting the MSK modulated signal via the Communications Link Simulator.

A detailed block diagram of the MSK modulator is shown in Figure 2-6. The digital oscillator used to implement the MSK modulation format is a non-recursive digital oscillator that uses a stored quantized phase plane as the quantizing element. The frequency output by the oscillator is determined by the rate in which a digital sampler cycles through the quantized phase plane. A binary number serves as a digital representation of the frequency to be generated and controls the cyclic rate of the sampler. The digital number is input into a full adder whose output is strobed into a holding register. The output of the holding register serves as the other input to the full adder. The holding register thus serves as an accumulator, and the accumulated count at any one time represents where in the discrete phase plane the output frequency resides. The accumulator is updated at the reference clock rate of 2.097152 MHz, and on each clock pulse the accumulated count is increased by an amount equal to the digital number input into the adder. Thus the digital number determines the rate in which the discrete phase points in the phase plane are addressed and cycled through and hence controls the frequency output.

If the digital number which controls the output frequency is one, the 16-bit accumulator register will take 2^{16} or 65,536 clocks to cycle the accumulated count from 0 to 65,535 and then overflow back to 0. For the accumulator reference clock of 2.097152 MHz, the time required to complete one cycle through the phase plane is:



DIGITAL
MSK MODULATOR

Figure 2-6

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$$\text{time} = \frac{2^{16}}{2.097152\ \text{MHz}} = 31.25\ \text{milliseconds}$$

The presentation of 2π radians in 31.25 milliseconds describes a frequency of 32 Hz. If the digital number is changed to two, the presentation of 2π radians is accomplished in 15.625 milliseconds, describing a frequency 64 Hz. It is clear then that the digital number, when multiplied by 32, equals the frequency output by the digital oscillator.

The discrete phase plane is stored in a read-only memory (ROM) which is addressed by the contents of the accumulator. The accumulator content represents where in phase the output frequency is at some point in time, and as a function of time describes a sawtooth waveform with a repetition rate equal to the output frequency. The purpose of the ROM is to convert the sawtooth waveform into a sine wave function, with one period of the sine wave function described during a single cycle of the accumulator. The ROM physically consists of two separate ROMS, with one ROM containing the phase points for the first half of the accumulator count and the other the phase points for the second half of the accumulator count. The ten most significant bits of the accumulator address the ROM networks with the most significant bit of the accumulator used to steer the activation of the appropriate ROM. The ROM outputs are tri-state so that corresponding outputs from each ROM can be tied together in a wired-or configuration. The wired-or output from the two ROM networks is a quantized or digital version of the desired sine wave and thus a digital to analog converter (DAC) is used to obtain the final output. The most significant bit of the accumulator is also applied to the DAC to obtain a bi-polar output which is the final MSK modulated output.

The MSK modulation is implemented using the digital oscillator concept by simply changing the digital number being input into the adder. Assume, for instance, that the digital number is suddenly changed to a larger numerical value. Initially no change in the digital oscillator output will take place, but on the next 2.097152 MHz clock pulse the accumulator will be updated by the new value of the digital number. Since the new value of the digital number is larger in value, the accumulator accumulates count, overflows, and begins a new accumulation cycle at a faster rate. It is important to note that the switch to the new digital number causes no abrupt jump in the phase of the signal output by the DAC since there is no abrupt jump in the accumulator count. The frequency of the signal output by the DAC jumps to the frequency dictated by the new value of the digital number, but there is no phase discontinuity. If the digital number is suddenly lowered to the original value , again no discontinuity in phase will occur and the accumulator will accumulate count, overflow, and begin a new cycle at a slower rate - thereby lowering the output frequency. Raising or lowering the value of the digital number thus serves to immediately change the frequency of the signal output while maintaining phase continuity.

MSK modulation has just been described if the two digital numbers are of the proper value to create two signals separated in frequency by half the data clock. Two switch banks are used to implement the two digital numbers. The outputs of the two switch banks are routed to a 2-channel multiplexer which is steered by the polarity of the digital data. With this choice of implementation, any modulation index can be generated by properly selecting the outputs from the two switch banks. The modulator then generates continuous phase FSK of selectable modulation index - with MSK modulation being but a special case with a modulation index of 0.5. The steering logic controlling the multiplexer

receives the data from the data generator and steers the multiplexer accordingly. The steering logic is also implemented to allow only one switch bank output to be utilized during the CW portion of the message transmission. This is done to assure that the modulator outputs only a continuous tone during the CW preamble.

The DAC output is input into a summing network where the modulated signal is summed with an external signal or noise. This summation port is provided chiefly to implement known signal to noise ratios for testing the demodulation techniques in the Receive Channel Simulator. The output of the summing network is input into a variable Q bandpass filter. This bandpass filter, which is implemented with a Burr-Brown universal active filter, can be varied in Q from 13 to 57, which represents a bandwidth of 1.1 f_b to 2.3 f_b (where f_b is the digital data rate) for both NRZ and Manchester encoded data. The purpose of this filter is to measure the performance of the demodulation techniques in the Receive Channel Simulator as a function of band-limiting the MSK mdoulated signal. This can be a very crutial set of data points in terms of optimizing the mutual interference statistics in future data collection systems utilizing MSK modulation.

The reference clock of 2.097152 MHz is used as the reference clock to the accumulator to generate the phase coherent FSK modulation. However, with the particular digital oscillator implementation used there is no means of generating the carrier frequency (20.016 KHz) during the CW preamble portion of a message. The non-coherent demodulator requires a front-end CW preamble at the carrier frequency to effectively center the discrimination process. It is also imparative that some percentage of carrier frequency remain present during the transmission of data - which necessitates Manchester encoding. For the non-coherent demodulation process then, which is synonymous with the transmission of

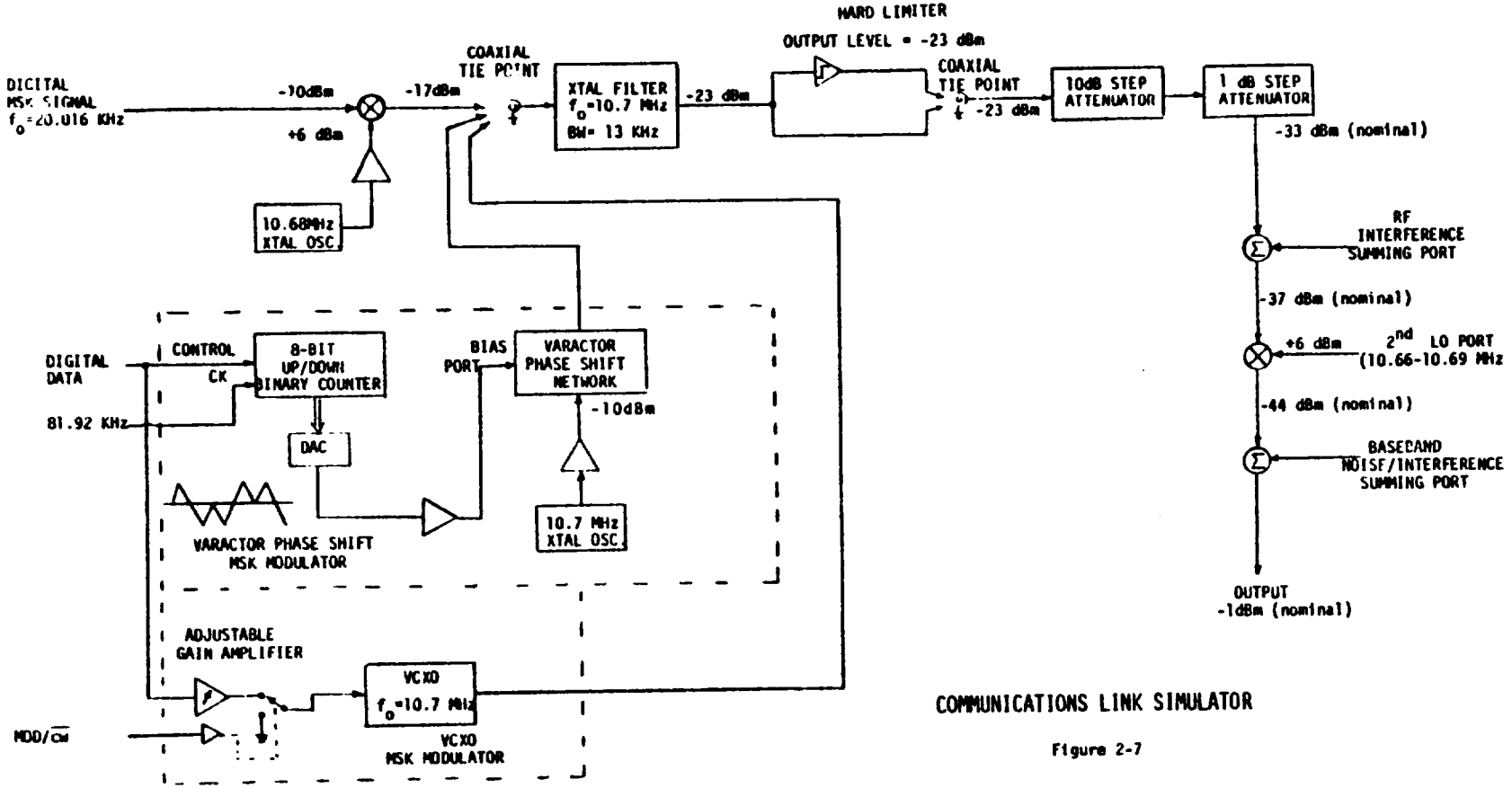
Manchester encoded data, the MSK modulator is implemented to output the carrier frequency during the CW preamble. For straight NRZ data, the mark frequency of 20.096 KHz is transmitted during the CW preamble rather than the carrier frequency. The mark frequency is used with NRZ data because it falls in the center of a frequency bin in the chirp-z transformer search system, resulting in no ambiguity in the frequency bin assigned to the Receive Channel Simulator. This removal of bin assignment ambiguity is important to the operation of the coherent demodulator. The mark and space phase lock loops must be narrow enough to avoid tracking each other, and if the loops had to acquire over a frequency range equivalent to a bin ambiguity, the acquisition range requirement and adjacent signal rejection criteria would conflict. This problem can be overcome in a final hardware design by simply stipulating that the resolution of the search unit be much less than the mark and space frequency separation if coherent demodulation is to be used.

To implement the carrier frequency during the CW preamble, a separate reference clock set at 2.0788 MHz is used to clock the accumulator in the digital oscillator. This reference clock value in conjunction with the setting of that switch bank output by the multiplexer during the CW preamble - which with the normal referency frequency of 2.097152 MHz would generate the mark frequency - generates a tone at exactly the carrier frequency of 20.016 KHz. The selection logic which selects which reference clock is to be applied to the accumulator is designed to output the 2.097152 MHz reference except during the CW preamble portion of a Manchester encoded message transmission or during the absence of any transmission at all. In the latter case no clock at all is applied to the accumulator and the modulator is completely disabled.

E. COMMUNICATIONS LINK SIMULATOR

The Communications Link Simulator provides two functions - it simulates an r-f communications link and it houses two different hardware designs for implementing MSK modulation. The r-f communications link simulation is accomplished at an i-f of 10.7 MHz, which is a common i-f frequency that can be readily up-converted to an r-f frequency for transmission if so required at a later date. At the 10.7 MHz i-f, the MSK modulated signal, which is obtained by either up-converting the 20.016 KHz digital MSK modulator carrier or utilizing one of the two MSK modulators housed in the Communications Link Simulator, is either linearly processed and then down-converted to a baseband signal centered between 10 to 40 KHz, or it is routed through a hard limiter prior to down-converting. This feature allows comparisons to be made in terms of data recovery performance, both for the coherent and non-coherent demodulators, between MSK signals which have been linearly processed and transmitted and MSK signals which have been passed through non-linear devices - such as class C power stages - prior to transmission. Also, interference can be inserted at the 10.7 MHz i-f frequency via an interference summing port to simulate either broadband or narrow band type r-f interference. The down-conversion LO port is designed to be driven by an external synthesizer which, when varied in frequency between 10.66 and 10.69 MHz, effects a baseband signal between 10 to 40 KHz. A summing port is also provided at baseband for inserting noise or another interfering tone.

The two MSK modulators housed in the Communications Link Simulator provide a means of evaluating the properties of MSK modulation when generated at an r-f frequency. The two types of modulators provided are a VCXO type modulator and a varactor phase shift modulator. The center or rest frequency of the VCXO modulator is tuned to 10.7 MHz, and the gain of the VCXO is adjusted to provide the mark and space frequencies when driven by the serial digital data stream. For the varactor phase shift modulator, the incoming digital data stream drives a ramp generator - which is a digitized version of an integrator. The



COMMUNICATIONS LINK SIMULATOR

Figure 2-7

ramp generator, in turn, outputs positive or negative sloped ramps which, when used to drive the bias port of the varactor phase shift network, create linear phase ramp excursions of the 10.7 MHz signal. The phase shift network has a linear phase range of approximately 360 degrees. When utilizing this modulator then it is necessary that the digital data driving the modulator be encoded to ensure that data transitions are present so that the linear phase range of the modulator is not exceeded. Manchester encoding is the encoding scheme utilized. The VCXO type modulator does not have the encoding requirement and may be driven by NRZ data.

Both modulators do have a common property, however, which distinquishes them from the digital MSK modulator housed in the MSK Transmitter Simulator. In the digital MSK modulator the 20.016 KHz carrier and the 320 bps data rate are synchronous since both carrier and data clock are generated from a common crystal oscillator. For the two modulators housed in the Communications Link Simulator, however, synchronism between the 320 bps data and the 10.7 MHz carrier is not maintained. The question of synchronism between the carrier and the data is one of the main properties of MSK modulation to be addressed. The value of synchronism will be judged by comparing the data recovery performance for both the coherent and non-coherent demodulators for both synchronous and asynchronous data clock and carrier relationships. The synchronous relationship between carrier and data clock is a prime reason for building the digital MSK modulator.

Figure 2-7 is a block diagram of the Communications Link Simulator. The digital MSK signal is input into the simulator at a -10 dBm signal level and up-converted to 10.7 MHz. The up-conversion is accomplished by a mixer driven by a 10.68 MHz crystal oscillator. The mixer output is tied to a coaxial tie point along with the outputs from the VCXO and varactor phase shift MSK modulator The purpose of the coaxial tie point is to allow the selection between the three sources of MSK modulation to be made by attaching a short coaxial cable between

the desired MSK output and the common junction into the bandpass filter. The bandpass filter which follows the coaxial tie point is a crystal filter centered at 10.7 MHz with a double-sided bandwidth of 13 KHz. The purpose of this filter is to remove the unwanted mixing products from the up-converted digital MSK modulator signal and reject any extraneous frequency components from the varactor phase shift or VCXO type MSK modulators. The filter output, which sets at approximately - 23 dBm, drives both a hard-limiter and a second coaxial tie point. The hard-limiter output is also tied to the second coaxial tie point. A selection can then be made between a hard-limited or linear version of the selected MSK modulation, and allows tests to be conducted to determine the effect or degradation resulting from using non-linear hardware - such as class C power amplifiers - in generating the MSK signal. Two attenuators follow the second coaxial tie point and allow the signal to be varied in power over a wide dynamic range in 1 dB steps. The input into the attenuator bank is approximately - 23 dBm, and the output is nominally set at - 33 dBm.

Following the attenuator bank, the signal is input into a summing amplifier. A second input port into this amplifier allows r-f interference - either wideband or narrow band - to be summed with the signal to simulate unwanted signals and noise-like interference associates with typical r-f links. The output of this amplifier, which is nominally set to -37 dBm, concludes the 10.7 MHz i-f signal processing in the Communications Link Simulator. The amplifier output drives a second mixer which serves to down-convert the 10.7 MHz signal to base-band. The down-conversion is accomplished by inputting a second LO from an external synthesizer into the reference port of the mixer. The external synthe-sizer may be varied in frequency from 10.66 MHz to 10.69 MHz, which places the signal at baseband between 10 and 40 KHz. The baseband signal is then routed through yet another summation amplifier to allow Gaussian noise or additional interfering signals to be combined with the signal. The summing amplifier also provides approximately 43 dB of gain. The output of the Communications Link

Simulator is then a -1 dBm baseband signal ranging in frequency between 10 and 40 KHz.

The varactor phase shift MSK modulator and the VCXO MSK modulator are also shown in Figure 2-7. For the varactor modulator, the incoming digital data steers or controls the count mode of an 8-bit up/down binary counter. If the incoming data is a logic one, the counter is commanded to "count-up", and if the data bit is a logic zero, the counter is commanded to "count down". The counter output is sent to an 8-bit digital-to-analog converter to convert the counter content to voltage ramps as shown in Figure 2-7. As previously noted, Manchester encoding is required when using this modulator to ensure that the linear phase range of the varactor phase shift network, which is but 360 degrees, is not exceeded. For 320 bps Manchester encoded data, the maximum duration of a logic one or zero is 3.125 milliseconds. To achieve a count of 2^8 in 3.125 milliseconds requires a clock rate of

$$f_{clock} = \frac{2^8}{3.125.10^{-3}} = 81.92 \text{ KHz}$$

This clock is derived from the 10.48576 MHz oscillator housed in the Search Subsystem Simulator. The triangular ramp waveform is then converted to a proper drive level by an amplifier and input into the bias port of a Merrimac Model PSE-4 phase shift network. The drive voltage serves to alter the bias on a varactor diode which in turn alters the capacitance of the diode and varies the tuning of the network. The net result is to linearly vary the phase of the 10.7 MH crystal oscillator generated reference frequency in $\pm$ 90^o ramps - which is the phase characteristic of MSK modulation as referenced at the carrier frequency.

The VCXO MSK modulator consists of a VCXO whose center or rest frequency is tuned to the carrier frequency (10.7 MHz) of the MSK modulated signal. The incoming digital data stream is passed through an adjustable gain amplifier which serves to remove the dc bias, or convert the 0 to 4 volt logic signal to a signal centered about zero volts. The gain of the amplifier is also adjustable so that the proper drive levels can be obtained to slew the VCXO to the mark or space frequency - depending on whether the incoming data bit is a logic one or a logic zero respectively. Circuitry is also provided to ground the input to the VCXO during the CW preamble so that the carrier frequency is output during the preamble - a necessary requirement for the phase lock loop type non-coherent demodulator used in the Receive Channel Simulator.

F. SEARCH SUBSYSTEM SIMULATOR

The Search Subsystem Simulator detects the presence of signal transmissions, assigns a receive channel to the detected signal, and generates a reference tone to translate the detected signal to the center of the Receive Channel Simulator's i-f bandpass filter. The simulator also contains built-in test circuitry for conducting probability of detection tests and false alarm tests.

The heart of the simulator is the chirp-z transformer, which performs a discrete Fourier transform on the incoming baseband signal. The output of the chirp-z transformer is a set of spectral coefficients representing the spectral content of the incoming signal. The magnitude of the coefficients output is examined by a threshold detector. Any tone or coherent signal in the baseband input which exceeds a minimal signal-to-noise ratio will cause the coefficient presenting the spectral content about the frequency of the incoming tone to exceed all other coefficients in magnitude. This means the threshold level can be set above the coefficient levels output on noise alone and yet below the coefficient levels resulting from the presence of signals in the baseband input. The threshold detector then will ideally be triggered only on incoming signals. The spectral coefficients generated by the chirp-z transformer are output serially. This allows the detection process to be accomplished with a single threshold detector. The outputting of the coefficients is also time/frequency ordered, so that noting the time of detection as referenced to the start of a transformation gives the location of the detected signal in frequency. This information allows a reference tone to be generated at the proper frequency to place the detected signal in the center of the i-f receive channel.

The following sections will first describe the theory of operation and the hardware implementation of the chirp-z transformer, and then the overall implementation of the Search Subsystem Simulator.

F.1. Chirp-Z Transformer

a. Theory of Operation

The chirp-z transform is a mathematical algorithm for implementing the discrete Fourier transform. The transform was originally conceived as an algorithm for implementing a discrete Fourier transform on a digital computer, but never gained wide acceptance as it offered no clearcut advantage over the popular Cooley-Tukey algorithm. However, the algorithm does lend itself to a natural implementation of the discrete Fourier transform using charged-coupled-device (CCD) transversal filters. To show this harmony between the chirp-z transform algorithm and the implementation of the algorithm with CCD transversal

filters, the mathematical development of the algorithm will be briefly developed

The discrete Fourier transform is given by

$$F_k = \sum_{n=0}^{N-1} f_n e^{-i2\pi kn/N}$$

where F_k = K^{th} spectral component of f(t), where

$f_k = k\ f_s/N$ (f_s being the sampling frequency)

N = number of samples taken on incoming signal f(t)

f_n = n^{th}/sample in time of f(t)

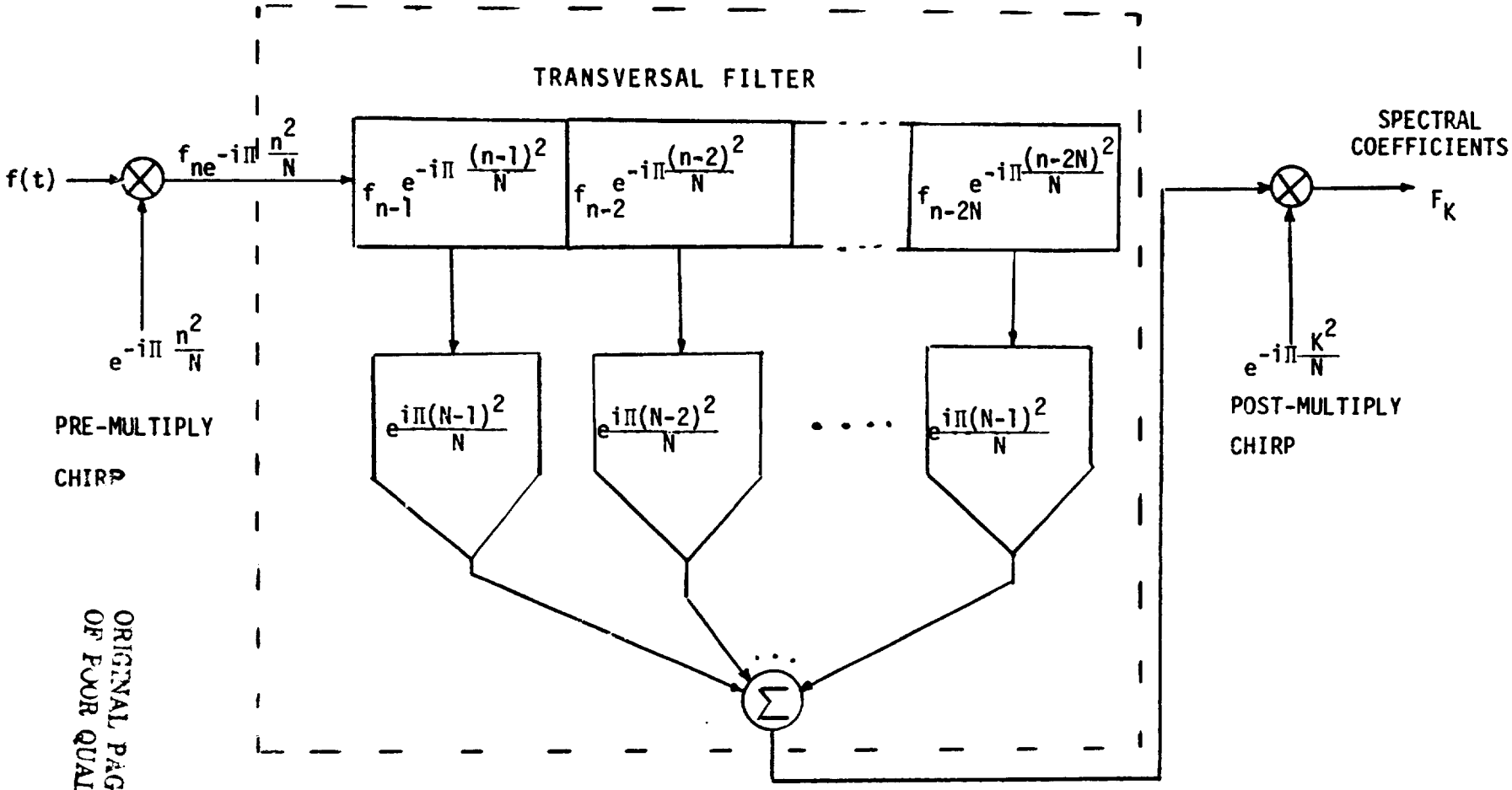
Using the substitution $2nk = n^2+k^2-(n-k)^2$ gives

$$F_k = \underbrace{e^{-i\pi\ k^2/N}}_{\text{Chirp Post-Multiply}} \sum_{n=0}^{N-1} \underbrace{(f_n\ e^{-i\pi\ n^2/N})}_{\text{Chirp Pre-Multiply}}\ \underbrace{e^{i\pi(k-n)^2/N}}_{\text{Tap Weights}}$$

Transversal Filter

As can be seen, the equation has been factored into three mathematical operations which are illustrated in Figure 2-8. The incoming signal f(t) is applied to a mixer where it is multiplied by a chirp (linear FM) waveform. The result of this initial mixing process, labeled the pre-multiply chirp operation, is then input into a CCD transversal filter where a convolution process is implemented. The CCD filter consists of a discrete number of cells with each cell containing a sample of the incoming data as modified by the pre-multiply chirp. The implementati then is a sampled data system with each sample in the CCD filter representing the analog value of the incoming chirp-weighted signal at the transition of the chirp bin or sample clock. The stored samples within the CCD filter are individually weighted (or multiplied) by coefficients or tap weights. The products are then summed and output to another mixer where a second chirp multiply, labeled the chirp post-multiply, is performed.

The actual derivation of the Fourier coefficients utilizing the chirp-z transformer as implemented with CCD's is a strict time-ordered process. Initially all of the storage cells in the CCD filter contain zero charge and the sampled signal f_n, after mixing with the complex chirp signal, is input into the CCD transversal filter. After N clock times, N samples of the incoming signal as modulated by the FM chirp are stored in the first N cells of the CCD. At this time the data is aligned so that when multiplied by the tap weights associated with each cell, the products summed, and the sum mixed with a second complex



CHIRP-Z TRANSFORMER OPERATION

Figure 2-8

FM chirp, the first spectral coefficient F_o results. After the next clock, in which the stored data samples are shifted down one cell with the input blanked so that zero charge is stored in the first or input cell, the data is aligned so that the second spectral component F_1 results. This serial step by step process continues until all N spectral components are calculated. At this time the 2N-1 cell CCD transversal filter contains the FM chirp modulated data samples in the top most N cells and zeroes in the first or input side N-1 cells.

The operation described has a major drawback in that the simultaneous inputting of new data samples and outputting of spectral coefficients is not allowed. The sampled data must first be loaded into the CCD filter while the output is blanked, and then the input must be blanked while the spectral coefficients are output. This gives only a 50% duty cycle in that a coefficient is effectively output only on every other chirp bin or sample clock. Unfortunately this is necessary if true Fourier coefficients are required, i.e., accurate both in phase and magnitude. However, when just the spectral density or magnitude of each coefficient is required, the implementation of the chirp-z transform can be greatly simplified.

To demonstrate the simplification that results when only magnitude data is required, it will be assumed that the blanking functions described above are disabled. Having made this assumption, it will then be shown that the resultant expression is the same as the strict DFT definition if only magnitude is considered. The omission of blanking means that a coefficient is output every clock period. The omission of blanking further implies that each successive coefficient is calculated from those data points used to calculate the previous coefficient, plus a newly sampled data point, and minus the oldest sample point. Furthermore, the data used in the previous calculation is now shifted one bit to the right. In other words, the data is indexed each time a spectral coefficient is calculated. The expression for the k^{th} coefficient then is simply.

$$F_k = \sum_{n=k}^{N+k-1} f_n \, e^{-i2\pi \, kn/N}$$

where the N sample points available for the calculation of the k^{th} coefficient lie in the time window of $k \leq n \leq n+k-1$. Now let $n-k=m$

$$F_k = \sum_{m=0}^{N-1} f_{m+k}\, e^{-i2\pi\, k(k+m)/N}$$

$$F_k = e^{-i2\pi\, k^2/N} \sum_{m=0}^{N-1} f_{m+k}\, e^{-i2\pi\, km/N}$$

It is noted that the above expression is identical to the strict definition of the DFT except for the phase modifier preceeding the summation sign. The magnitude of each coefficient is then unchanged by the sliding of the sampled data points. Making the same substitution as previously made for the chirp-z transform derivation yields.

$$F_k = e^{-i2\pi\, k^2/N}\, e^{-i\pi\, k^2/N} \sum_{m=0}^{N-1} f_{m+k}\, e^{-i\pi\, m^2/N}\, e^{-i\pi(k-m)^2/N}$$

Taking the magnitude squared of the above expression yields

$$|F_k|^2 = \Big|\sum_{m=0}^{N-1} \underbrace{\underbrace{(f_{m+k}\, e^{-i\pi\, m^2/N})}_{\text{Chirp Pre-Multiply}}\, \underbrace{e^{i\pi(k-m)^2/N}}_{\text{Tap Weights}}}_{\text{Transversal Filter}}\Big|^2$$

A very important simplification has taken place. The requirement for only magnitude has eliminated the need for post chirp multiplication. The above expression is called the "sliding" chirp-z transform algorithm.

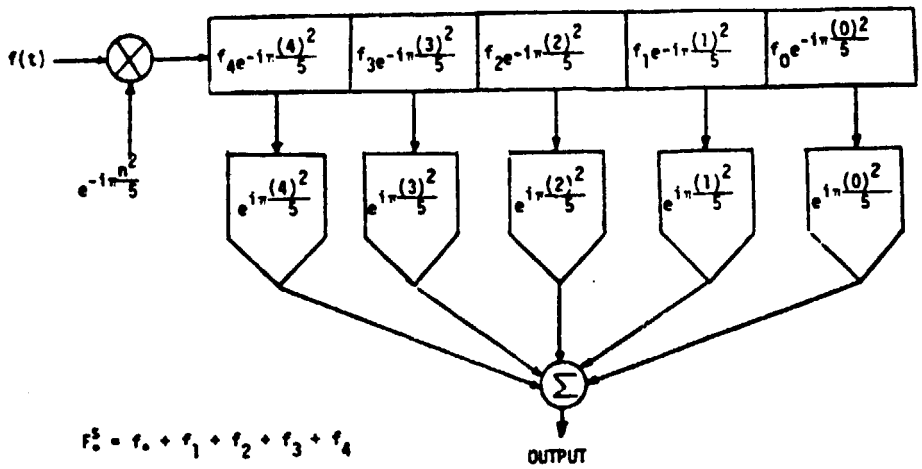
The CCD implementation of the sliding chirp-z transform is pictorially shown in Figure 2-9. As noted in the above equation, the sampled data points are indexed with each coefficient calculation, as are the tap weights. This latter observation is most disturbing because the tap weights in a realizable CCD filter are fixed, and using a fixed set of tap weights does not yield the product summation given in the above definitive equation. However, as indicated in Figure 2-9, a multiplier of constant magnitude (one), which remains fixed for a given coefficient calculation, can be applied to the answer output by the actual CCD implementation to give the proper answer. This required trick to obtain the product summation in the proper format simply signifies again that the sliding chirp-z transform does not preserve phase information. The output from the CCD transversal filter agrees with the definition of the sliding chirp-z transform in magnitude but not in phase.

EXAMPLES OF SLIDING CHIRP-Z

TRANSFORMER COEFFICIENT FORMULATION

Figure 2-9

F_0^s CALCULATION

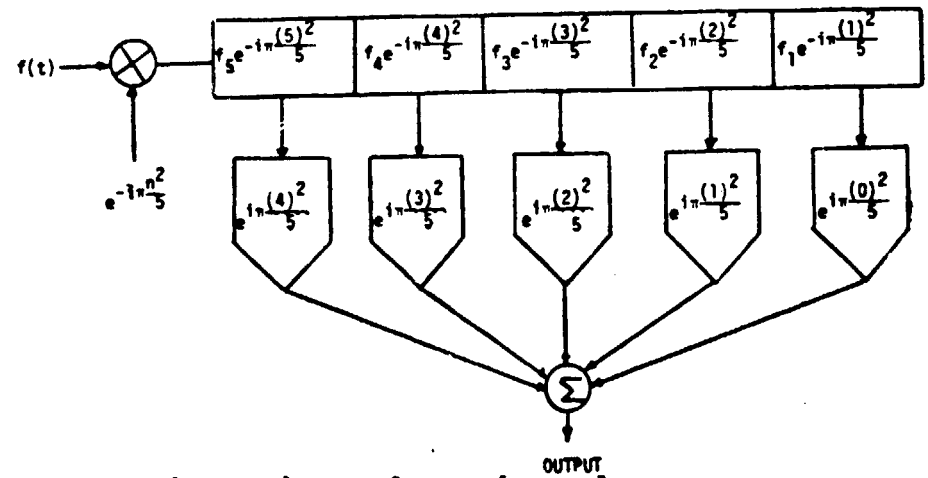


$F_0^s = f_0 + f_1 + f_2 + f_3 + f_4$

OUTPUT = F_0^s

$\therefore |F_0^s| = |\text{OUTPUT}$

F_1^s CALCULATION

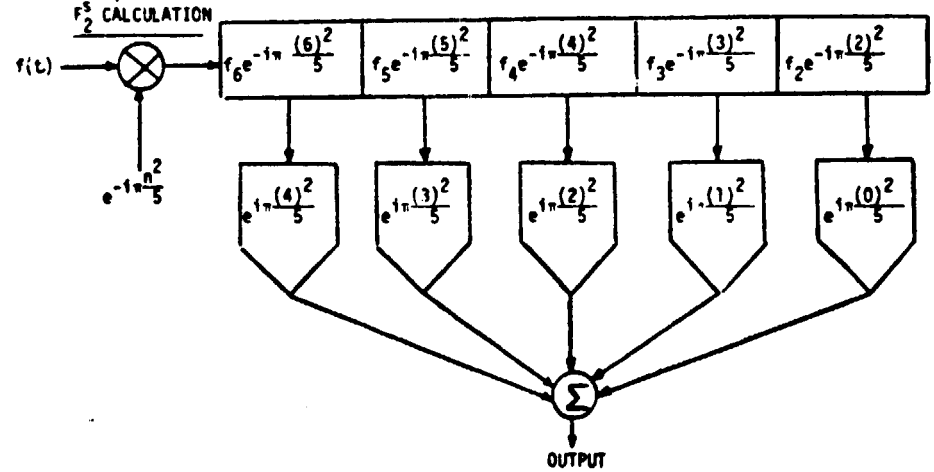


$F_1^s = f_1e^{i\pi\frac{1}{5}} + f_2e^{-i\pi\frac{1}{5}} + f_3e^{-i\pi\frac{3}{5}} + f_4e^{-i\pi\frac{5}{5}} + f_5e^{-i\pi\frac{7}{5}}$

OUTPUT = $F_1^s\, e^{-i\pi\frac{2}{5}}$

$\therefore |F_1^s| = |\text{OUTPUT}$

F_2^s CALCULATION



$F_2^s = f_2e^{i\pi\frac{4}{5}} + f_3 + f_4e^{-i\pi\frac{4}{5}} + f_5e^{-i\pi\frac{8}{5}} + f_6e^{-i\pi\frac{12}{5}}$

OUTPUT = $(F_2^s)(e^{-i\pi\frac{8}{5}})$

$\therefore |F_2^s| = |\text{OUTPUT}$

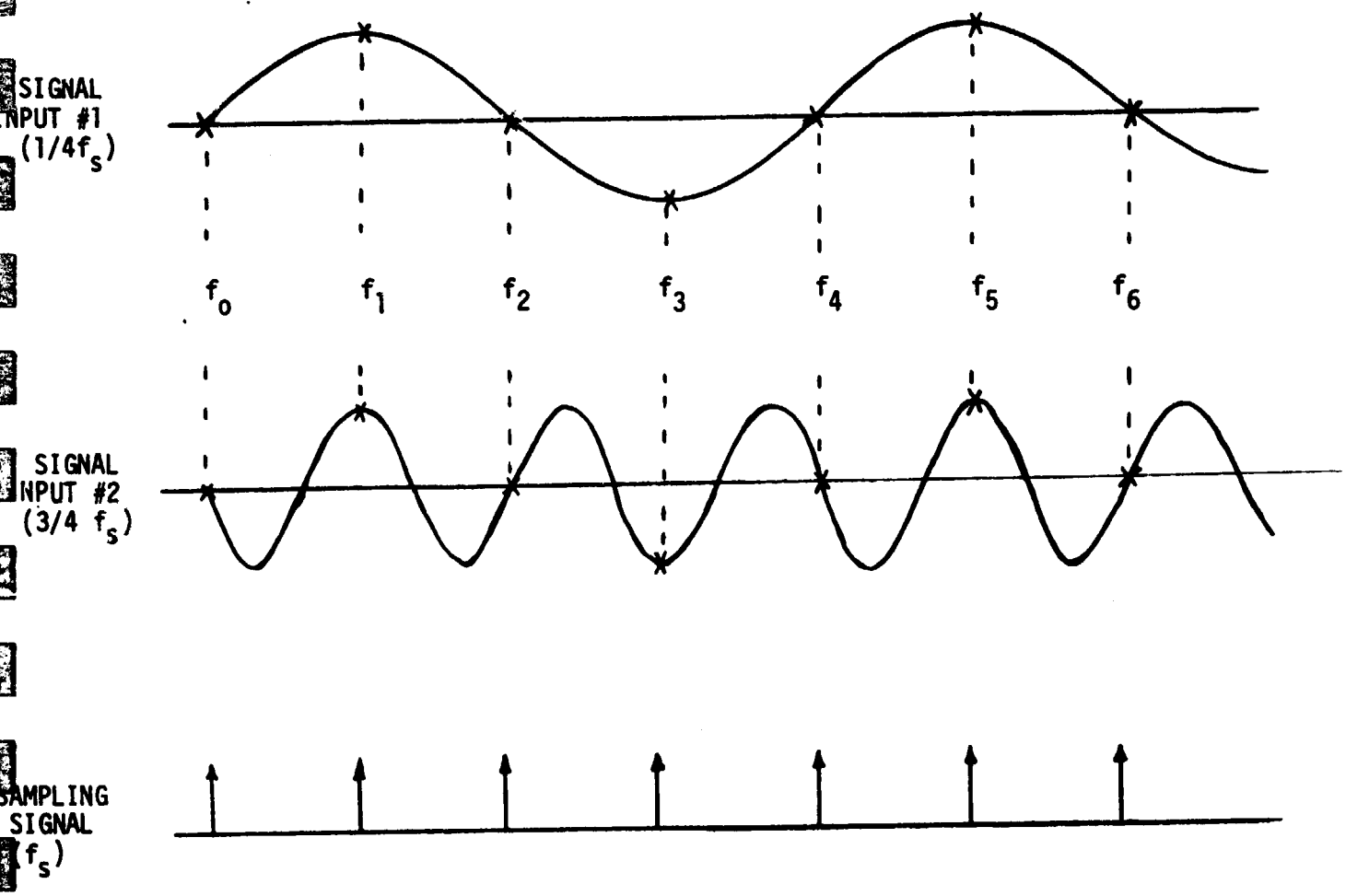
A property of the chirp-z transformer is the presence of what have been termed in this report "real" and "imaginary" coefficients. The discrete Fourier transform is defined only for periodic time functions. For N sampled data points, from which a discrete Fourier transform is to be derived via the chirp-z transform algorithm or any other appropriate algorithm, the time required to collect the N sample points (N/f_s) defines the period of the time domain signal. By definition, the discrete Fourier transform assumes that the sampled signal repeats its pattern every period. The output of the discrete Fourier transform is a set of N points or coefficients, with each coefficient representing a frequency band equivalent to the reciprocal of the time period. This frequency band is often termed the analyzing bandwidth of the discrete Fourier transform. An important observation can now be made. If N frequency points are output, with each frequency point separated in frequency from its adjacent neighbors by the analyzing bandwidth, then the highest frequency point represents the frequency spectrum in the neighborhood of the sampling frequency f_s. The equivalent period in the frequency domain as measured on a continuous frequency scale is then f_s. However, the discrete Fourier transform over the first half of the frequency period is related to the transform over the second half. The maximum unambiguous frequency range then is $f_s/2$, which is the familiar foldover frequency f_o. Discrete Fourier transform theory further tells us that regardless of the makeup of the input time signal (real, imaginary, complex), the last N/2 frequency points are but a mirror image of the first N/2 frequency points in magnitude. It can also be shown that the behavior of the frequency points in the range from N/2 to N is identical to the behavior from - N/2 to 0. Thus the interval from N/2 to N is often referred to as a negative time or frequency range interval. This is an important point in the actual implementation of the chirp-z transformer used in the ADC/PL breadboard system.

The result of all this is that a single frequency tone at the input will appear twice in the set of coefficients or frequency points output by the transform process. Another perhaps less confusing way to explain the dual frequency coefficients output during a given transform for each single frequency tone input is to consider the sampling theorem and its implications in the transform process. Assume the sample points are gathered at a sampling rate of f_s and further assume that there are N sample points used to perform the transform. For N sample points into the transform, N frequency points will be output and will cover a frequency range of 0 to f_s Hz. These are clear and straightforward results from the definitive equations governing the discrete Fourier transform. The sampling theorem states, however, that for proper reproduction of the sampled signal at least two samples per cycle must be taken. For an f_s sampl

rate, signals above $f_s/2$ in frequency will have less then two samples per cycle represented in the N sample points and will fold back about the $f_s/2$ frequency point and appear as lower-valued frequencies. By the same argument, it is noted that frequency inputs lower than $f_s/2$ can fold across the $f_s/2$ frequency point and appear as higher-valued frequency points. These two examples are illustrated in Figure 2-10. Two signals are shown, one at a frequency of 1/4 the sampling rate and one at a frequency of 3/4 the sampling rate. It is noted that both signals give the same sample values at the sampling points, so if presented just the sample points it would be impossible to tell from which signal the sample points came. This is precisely the reason why a given spectral tone which is below the foldover frequency of $f_s/2$ will appear twice in the set of spectral coefficients output from the transform process. One coefficient will represent the true frequency of the signal input (real coefficient) and one coefficient will represent the signal folded over (imaginary coefficient). In the example shown in Figure 2-10, a signal at 1/4 f_s will result in coefficients being output at both 1/4 f_s (real coefficient) and 3/4 f_s (imaginary coefficient).

It was stated earlier that the behavior of the frequency points in the range from N/2 to N is identical to the behavior of the frequency points in the range from -N/2 to 0. The chirp-z transform makes use of this equality by sweeping the input through zero frequency to create a spectral search band from $-f_s/2$ to $f_s/2$, which again is the same as a spectral band from 0 to f_s. This really is no more than an implementation technique to halve the maximum frequency required in the fm chirp. Also, visualizing the spectral search band this way clearly differentiates between the imaginary (negative frequency) and real (positive frequency) coefficients. The key reason for dwelling on the dual frequency coefficient phenomena is that a part of the chirp-z transformer evaluation is the processing gain (or loss) to be obtained by utilizing both the real and imaginary coefficients in constructing the probability of detection curves -- as opposed to just the real coefficients.

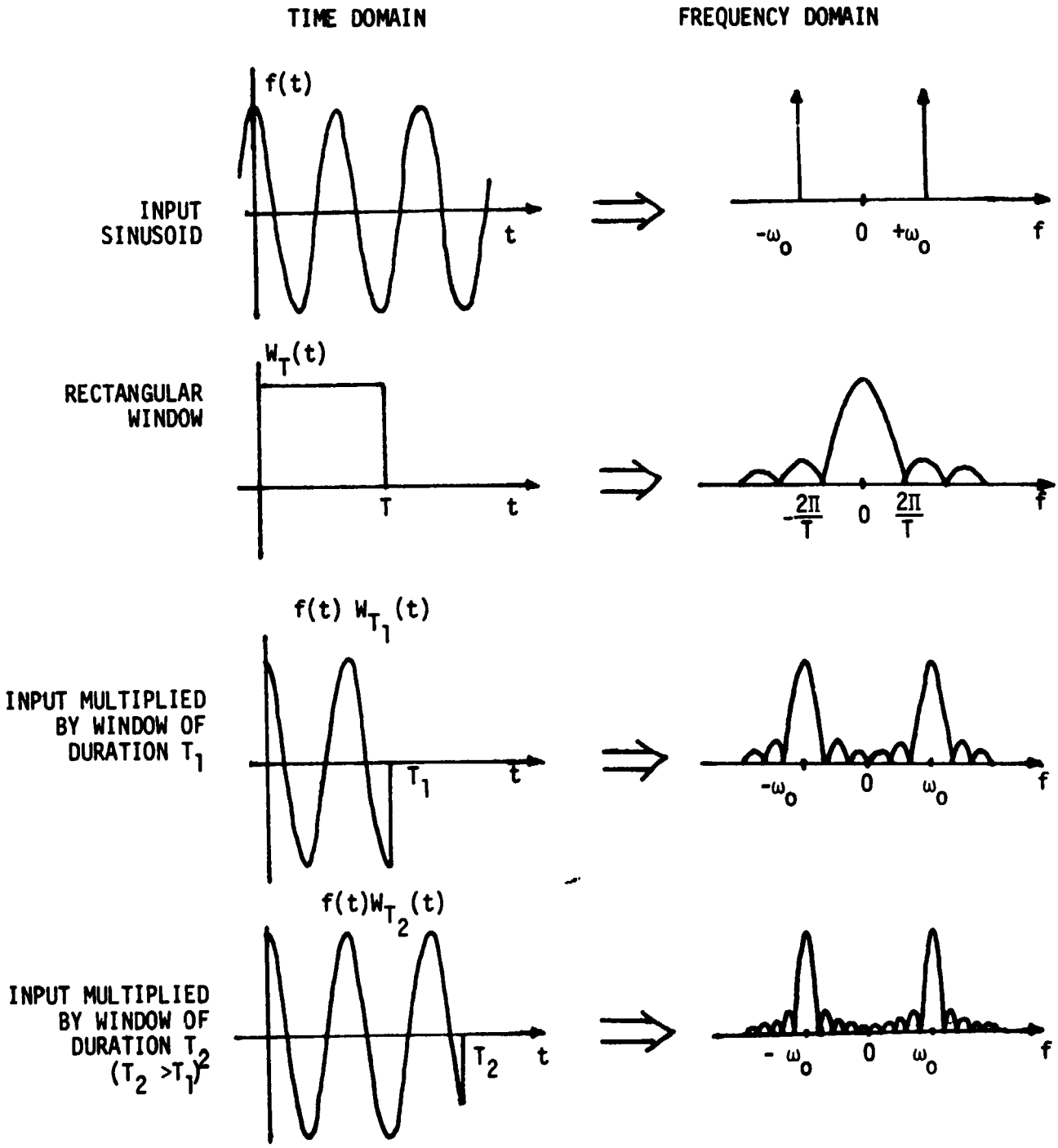
Another property of the chirp-z transformer is the weighting or sampling of the sampling window, by appropriately adjusting the tap weights, to minimize the effects of spectral spreading. The shaping of the sampling window to minimize spectral spreading is commonly referred to as apodization. Figure 2-11 depicts the need for apodization. As shown, a sine wave transforms into the frequency domain as two impulse functions located at the positive and negative frequency



FREQUENCY FOLDOVER

EXAMPLE

Figure 2-10



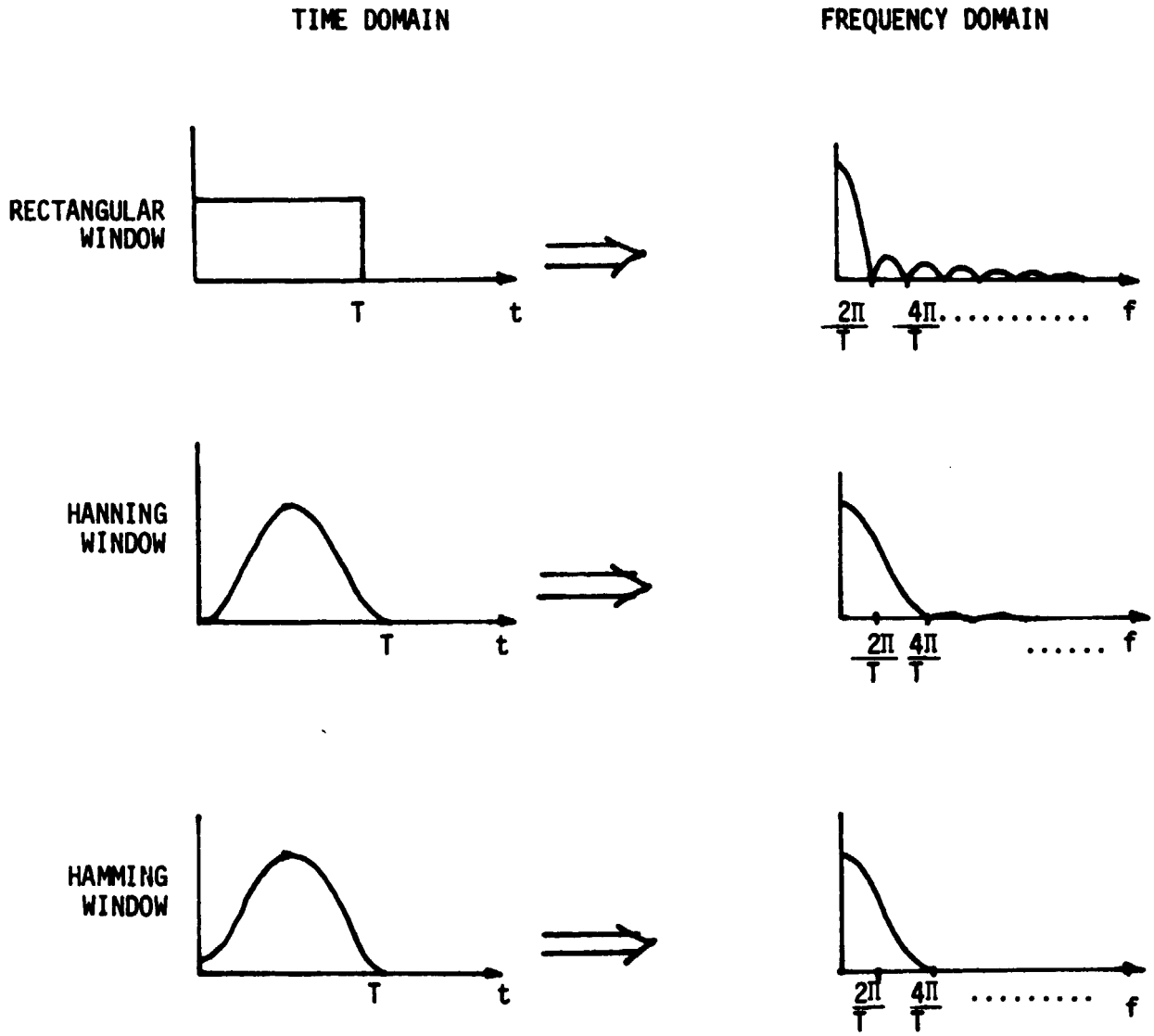
THE NEED FOR APODIZATION
Figure 2-11

points. A finite pulse however, which represents an unweighted or rectangular sampling window, transforms into the frequency domain as a sin x/x function centered at zero frequency or dc. The spectral function resulting from sampling the sinusoid over a finite duration can be found by convolving the sinusoid spectrum with the pulse spectrum. The result, shown in Figure 2-11, is two sin x/x functions centered at the positive and negative frequency points of the sinusoid. Also, as shown in Figure 2-11, increasing the length of the sample time narrows the two main spectral lobes as well as the sidelobes.

The presence of the sidelobes or leakage terms can create problems if the detector monitoring the coefficients output by the chirp-z transformer must operate over a large dynamic range. If the detector is adjusted to detect the presence of weak signals, then the leakage components of strong signals will also be detected and result in a high false alarm rate. To overcome this problem, the rectangular sampling function can be shaped to lower the sidelobes. Figure 2-12 depicts sampling windows of different shape factors and their Fourier transforms. As can be seen both the Hanning and Hamming windows transform into the frequency domain with wider main lobes but much lower sidelobes. The lower sidelobes will give a greater dynamic range capability in the detection process; however, a question arises as to whether or not the widening of the main lobes degrades the probability of detection for a given signal-to-noise ratio. To address this question two different chirp-z transformer chips are utilized. One chip has a straight rectangular shaped sampling window while the other utilizes a Hamming window. The Hamming weighting is accomplished by altering the tap weights of each CCD cell. Comparisons will be made between the two transformers both in terms of probability of detection versus signal-to-noise ratio and dynamic range or bin spreading.

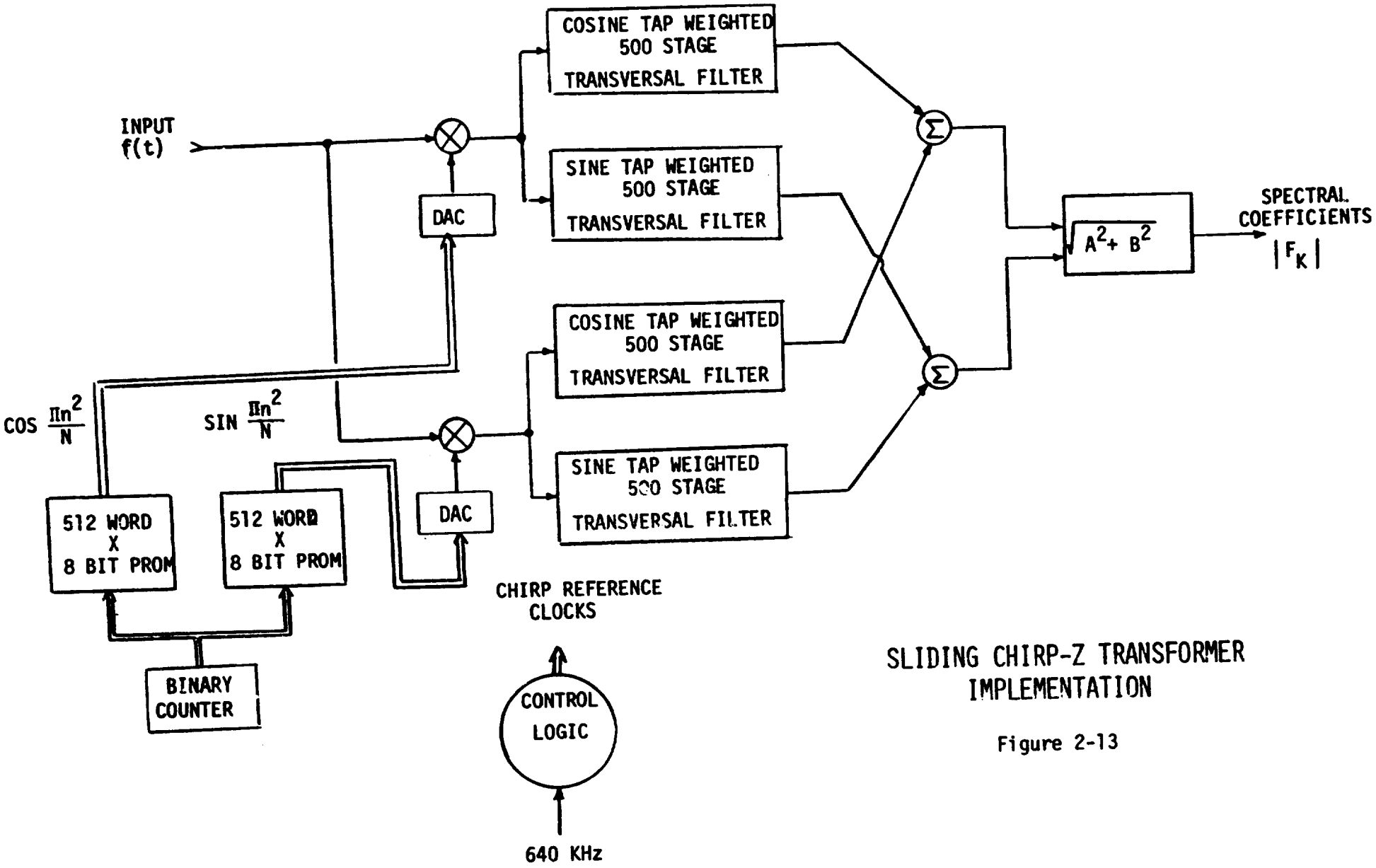
b. Hardware Implementation

Figure 2-13 is a block diagram of the sliding chirp-z transformer implementation. The CCD chip itself consists of four 500 cell transversal filters with sine or cosine tap weighting. Additional sine and cosine processing is included outside the chip itself to implement the chirp-z transformation. The configuration shown in Figure 2-13 can best be explained by examining the definitive equation for the sliding chirp-z transform previously developed.



DIFFERENT SAMPLING WINDOWS
AND THEIR SPECTRA

Figure 2-12



SLIDING CHIRP-Z TRANSFORMER
IMPLEMENTATION

Figure 2-13

$$F_k = \sum_{m=0}^{N-1} (f_{m+k}\, e^{-i\pi\, m^2/N}) e^{i\pi(k-m)^2/N}$$

$$F_k = \sum_{m=0}^{N-1} f_{m+k} \cos\pi\, m^2/N \cos\pi\, (k-m)^2/N + \sum_{m=0}^{N-1} f_{m+k} \sin\pi\, m^2/N \sin\pi\, (k-m)^2/N$$

$$+i\sum_{m=0}^{N-1} f_{m+k} \cos\pi\, m^2/N \sin\pi\, (k-m)^2/N - i\sum_{m=0}^{N-1} f_{m+k} \sin\pi\, m^2/N \cos\pi (k-m)^2/N$$

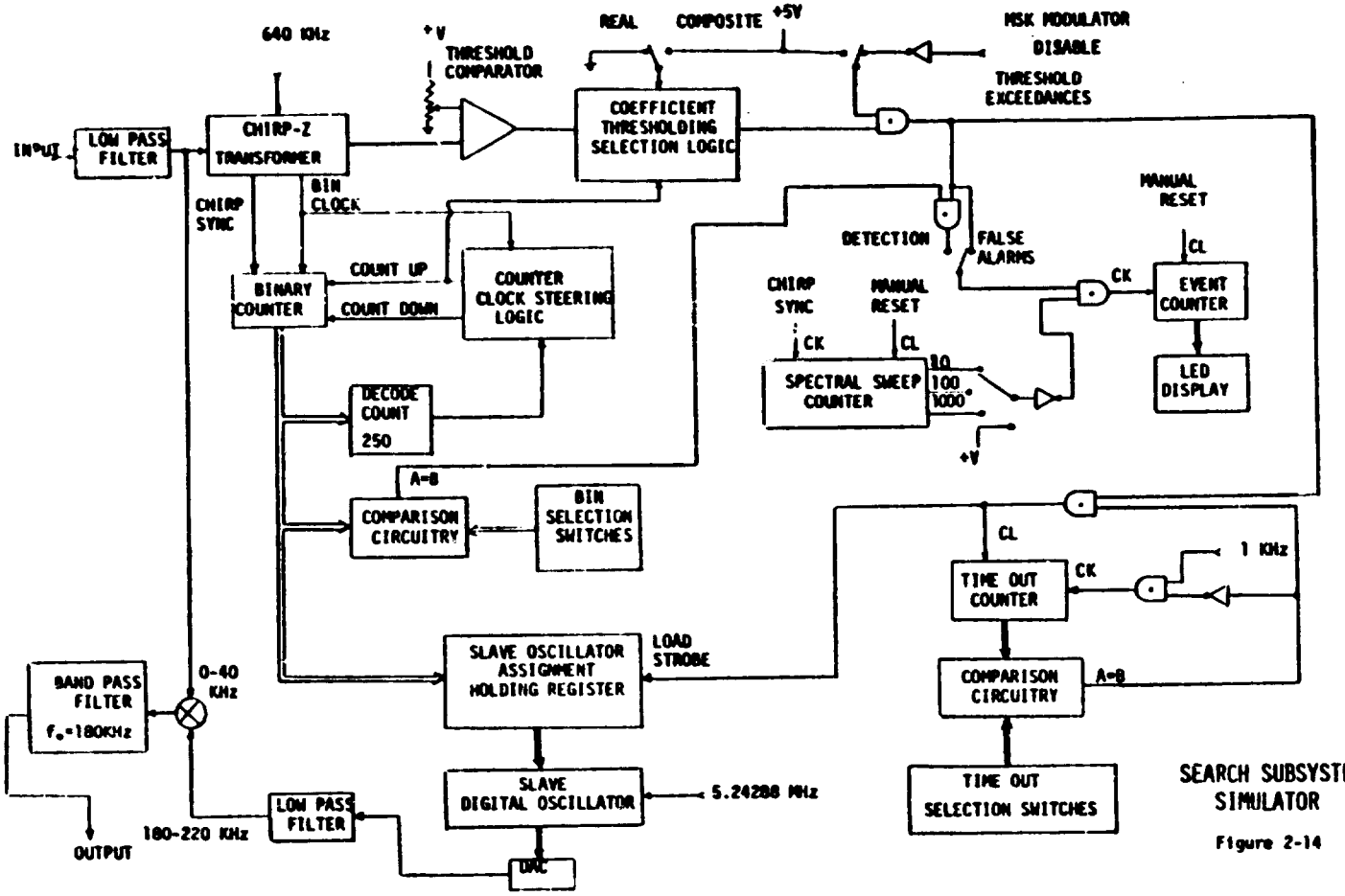
The above equation contains four summation terms involving the products of the sine and cosine components of the pre-multiply chirp multiplied by the sine and cosine components of the transversal filter. The four separate summation terms are developed in the four separate transversal filters shown in Figure 2-13. The two real summation terms are then added together and the two imaginary summation terms are added together by two summation amplifiers. The resulting real and imagina terms are then squared, summed, and the square root is taken to obtain the final magnitude term.

The pre-multiply sine and cosine chirp components are generated by using read-only memory look-up tables. Two 512 word by 8 bit PROMS (programmable read-only memories) provide the look-up table. An 8-bit binary counter is used to step through the look-up table and generate the chirp components. Two digital to analog converters are used to convert the digital PROM words to analog format. The two analog chirp components are then mixed with the incoming signal and input into the transversal filters.

Texas Instruments is presently developing a fully integrated 500 cell chirp-z transformer which will include all of the components shown in Figure 2-13 on the CC chip itself, except for the two PROMS. This level of integration should improve the performance of the chirp-z transformer by reducing stray capacitances and pick-up problems and will certainly make the chirp-z transformer attractive in terms of packaging requirements.

F.2 Simulator Implementation

Figure 2-14 is a block diagram of the Search Subsystem Simulator with the chirp-z transformer represented as a single block. The incoming signal is passed through a 5 pole low pass elliptic filter prior to the chirp-z transformer to remove any unwanted high frequency terms and to establish a well-defined noise bandwidth for implementing signal-to-noise measurements. The low pass filter has a cutoff



SEARCH SUBSYSTEM SIMULATOR

Figure 2-14

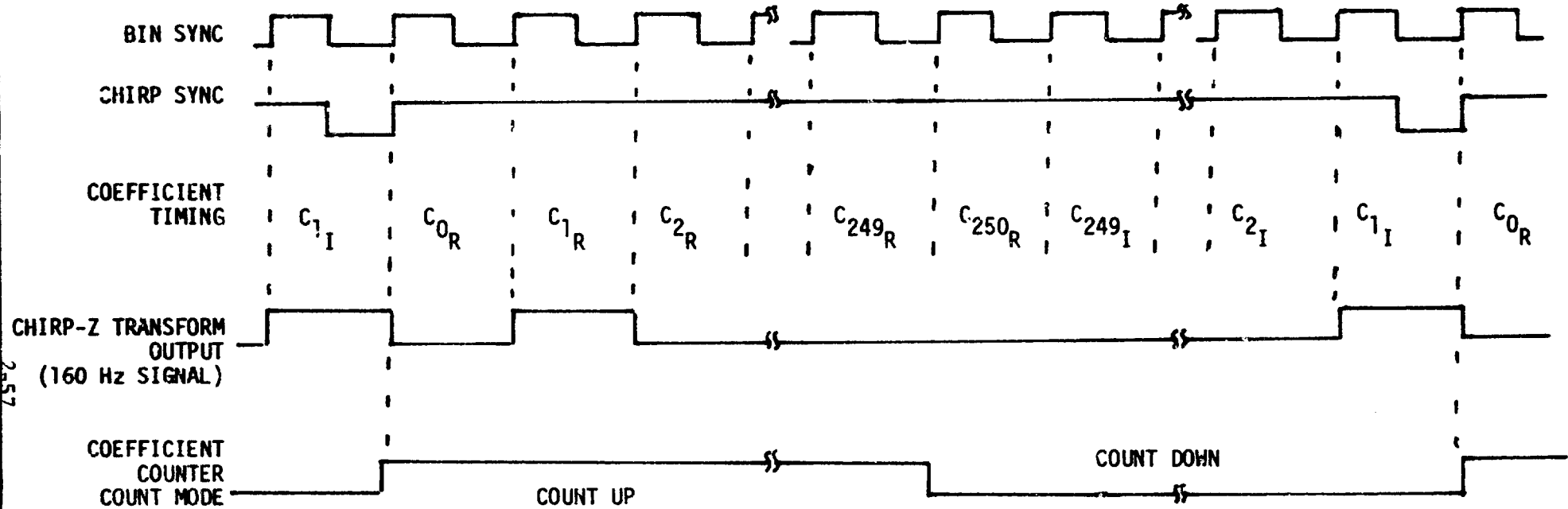
frequency of 40 kHz. The chirp-z transformer divides this 40 kHz frequency band into 250 frequency cells. Each cell then represents 160 Hz in frequency. A coefficient is output for each cell, and the magnitude of the coefficient reflects the spectral energy present in the 160 Hz bin assigned to the coefficient. The output of the chirp-z transformer is a serial train of coefficients which are input into a threshold comparator. The threshold level on the comparator is adjustable to allow different false alarm rates to be selected by monitoring the rate of threshhold exceedances on noise alone. The output of the threshold comparator is input into coefficient thresholding selection logic where the choice is made to output only threshold exceedances resulting from "real" coefficients or threshold exceedances resulting from either "real" or "imaginary" coefficients. The choice is made by a switch located on the front panel of the simulator. The output from the coefficient thresholding selection logic is routed through a gate which can disallow outputting threshold exceedances if a signal is not being output by the MSK Transmitter Simulator. No mechanism is provided in the Receive Channel Simulator to verify that an assignment received from the Search Subsystem Simulator is being properly attended - phase lock has been established, the frame sync code has been detected, etc. Once an assignment is made then, it remains throughout the time required to transmit a message. Any assignments based on false alarms will then tie the Receive Channel Simulator up for a significant period of time and in all probability will result in the actual message being missed. The gate is provided to reduce the probability of assigning the Receive Channel Simulator to a false alarm by not allowing any threshold exceedance to be output unless the MSK Transmitter Simulator is actually transmitting a signal. The gate can also be deactivated to allow threshold exceedances to be continually output. The control of the gate mode is accomplished by a switch located on the front panel of the simulator.

The resulting threshold exceedance signal, termed the threshold event signal, serves to clear or re-initialize a time-out counter and load the count defining which coefficient caused the exceedance into a holding register--the slave oscillator assignment holding register. The time-out counter is the mechanism which, once an assignment is made, allows no other assignments to be made, even though additional threshold event signals occur. The time-out duration is determined by thumbwheel time-out selection switches located on the front panel of the simulator. The resolution of the time-out signal duration is one millisecond and the length can be varied from 1 to 999 milliseconds. The time-out signal duration is normally set to the length of the message duration so that the search unit will be ready to detect a new transmission and make a new assignment at the end of a previously assigned signal transmission. When the count in the time-out counter agrees with the thumbwheel switch setting, the counter is deactivated and a gate

is activated to allow the next threshold event signal to re-initialize the counter and make a new assignment by loading a new count value into the slave oscillator holding register.

The chirp-z transformer outputs 500 coefficients, 250 real coefficients and 250 imaginary coefficients, in 6.25 milliseconds. The search time of 6.25 milliseconds is the reciprocal of the cell size or analyzing bandwidth of 160 Hz. The serial output rate of the coefficients is then 80 kHz, which in 6.25 milliseconds gives 500 coefficient samples. Figure 2-15 depicts the time-ordered sequence in which the coefficients are output. A synchronizing pulse output by the chirp-z transformer, the chirp sync pulse, denotes the beginning of a new transformation; and the bin sync clock signal, also output by the chirp-z transformer, is the 80 kHz coefficient rate clock. Following the chirp sync pulse, the first coefficient output is the real coefficient C_{0_R}, which represents the spectral energy from -80 Hz to +80 Hz. The next coefficient output is $C1_R$, which represents the spectral energy from +80 Hz to +240 Hz. This sequence continues until the last real coefficient, $C250_R$, is output representing the spectral energy from 39,920 Hz to 40,080 Hz. The next coefficient output is the imaginary coefficient $C249_I$, which represents the spectral energy from -39,920 Hz to -39,760 Hz. The next coefficient output, $C248_I$, represents the spectral energy from -39,760 Hz to -39,600 Hz. The outputting of imaginary coefficients continues until the last imaginary coefficient $C1_I$ is output representing the spectral energy from -240 Hz to -80 Hz. The cycle then repeats with coefficient $C0_R$ being output next.

To keep track of which coefficient is being output at any one point in time, an up/down binary counter, which is clocked by the bin sync clock, is used. The chirp sync pulse initially clears the binary counter and places the counter in a count-up mode. When a count of 250 is detected, the count mode is changed to a count-down mode and the counter begins counting down at the bin sync clock rate. The mode or selection of count direction then defines whether the coefficient being output is real or imaginary, and the mode selection is used to steer the coefficient thresholding selection logic. Also, the count residing in the binary counter upon receiving a threshold event signal represents where, to within 160 Hz, the detected signal lies. Transferring this count to the slave oscillator assignment holding register allows a reference tone to be generated to place the detected signal within the i-f bandwidth of the Receive Channel Simulator. The slave oscillator is the same type digital oscillator described in the MSK Transmitt Simulator. The frequency range of the slave oscillator is 180 kHz to 220 kHz and the resolution is 160 Hz. The output of the slave oscillator is mixed with the incoming baseband signal out of the 5 pole elliptic low pass filter, and the lower



CHIRP-Z TRANSFORMER
SPECTRAL COEFFICIENT TIMING

Figure 2-15

sideband is routed through a bandpass filter centered at 180 kHz with a double-sided bandwidth of 12 kHz.

The threshold event signal is also used to conduct probability of detection tests and false alarm rate tests. Probability of detection tests are conducted by examining how many times the threshold event signal occurs at a given bin or frequency cell over a given number of attempts for a given input signal of known frequency. A set of thumbwheel bin selection switches located on the front panel of the simulator select which frequency cell is to be examined for threshold events. The switch setting is compared against the count in the binary counter keeping track of the coefficient order. A comparison signifies that the coefficient presently being output to the threshold detector represents the spectral content of the frequency bin of interest. This comparison signal is gated with the threshold event signal line, and the output is the threshold event signal for the frequency bin to be examined. The gate output is routed to a threshold event counter where the number of gated events is recorded.

To determine the probability of detection, it is necessary to know how many detections were made over a period of time and how many detections could have been made if a 100 percent probability of detection were available. If only real coefficients are utilized, only one coefficient will be output per transformation; whereas using both real and imaginary coefficients result in two coefficients being output during each transformation for the frequency bin of interest. A spectral sweep counter is provided to count the number of transformations or spectral sweep cycles. Upon manually resetting the counter, the counter begins counting chirp sync pulses. When a selected number of sync pulses have been counted, the counter halts. A gate is provided prior to the threshold event counter which allows the gated threshold events to update the event counter only while the spectral sweep counter is active. In this way, the number of events in the event counter represent the number of events detected over a given number of spectral sweeps. The number of spectral sweeps can be selected to be 10, 100, 1000, or infinite - the latter case being used in false alarm testing. Assume for example, that the 1000 spectral sweep case were chosen, real coefficients only were selected, and the resulting count in the event counter were 973. The probability of detection then would simply be 97.3%.

False alarms are defined to be those threshold event signals which are triggered by noise rather than signal energy. To determine the false alarm rate it is necessary to remove all signals, input just Gaussian type noise, and count the total number of threshold events across the entire spectral search band. This means that all coefficients contribute to the false alarm rate. When making false alarm rate measurements then, the gate which allows the event counter to count only those threshold events for a selected frequency bin is bypassed to allow any threshold event signal at any frequency bin to update the event counter. However, the selection between real only or real and imaginary coefficients is still viable. The number of spectral sweeps is generally chosen to be infinite, since the false alarm rate of 10^{-6}, for example, for both real and imaginary coefficients would give on the average one threshold event per 10^{6} coefficients output - or one threshold event per 2000 spectral sweeps for a 500 point transform. The false alarm rate is adjusted by adjusting the reference level to the threshold comparator.

G. RECEIVE CHANNEL SIMULATOR

The Receive Channel Simulator consists of a non-coherent MSK demodulator, a coherent MSK demodulator, and a frequency measurement circuit. The non-coherent demodulator is a discriminator type demodulator utilizing a phase lock loop to center the carrier of the incoming signal at the center of the discriminator. The phase lock loop also provides a mechanism for implementing a frequency measurement of the received carrier. The use of a phase lock loop does require the presence of a carrier component and thus some form of data encoding is required to ensure the presence of a carrier. Manchester encoding is chosen mainly for ease in recovering the data clock - although circuitry is not provided in the breadboard for recovering the data clock. The coherent demodulator is the type discussed most often in the literature, and consists of two phase lock loops - one to recover the mark frequency and one to recover the space frequency. The outputs of the two phase lock loops are routed through sum and difference networks and then mixed with the incoming signal in such a way as to recover the in-phase and quadrature components of the incoming MSK signal. The phase lock loop outputs, when mixed with each other, also provide the data clock. The data clock is used to alternately sample the output of two matched filter networks - one operating on the in-phase component and the other the quadrature component - to recover the NRZ data stream. Unlike the non-coherent MSK demodulator, the coherent MSK demodulator does not require encoding of the data, and the recovery of the data clock is easily obtained from the signals formed in the demodulation process.

The frequency measurement circuit can operate with either demodulation unit. The circuit consists of a binary coded decimal counter which counts the zero crossings of the incoming VCXO signal from the appropriate demodulator for a fixed time period of 100 milliseconds. In the non-coherent demodulator the VCXO in the phase lock loop runs at 100 times the frequency of the incoming carrier. In 100 milliseconds then the counter will give a frequency resolution of 0.1 Hz as referenced to the incoming carrier. In the coherent demodulator, the VCXO in the phase lock loop assigned to the space frequency of the incoming signal runs at fifty times the frequency of the incoming space frequency. In the same 100 milliseconds window, the counter will give an 0.2 Hz resolution as referenced to the incoming space frequency. The frequency measurement circuit also contains hardware for generating the 100 millisecond measurement window and the acquisition/track bandwidth selection signal to the phase lock loops in the demodulators.

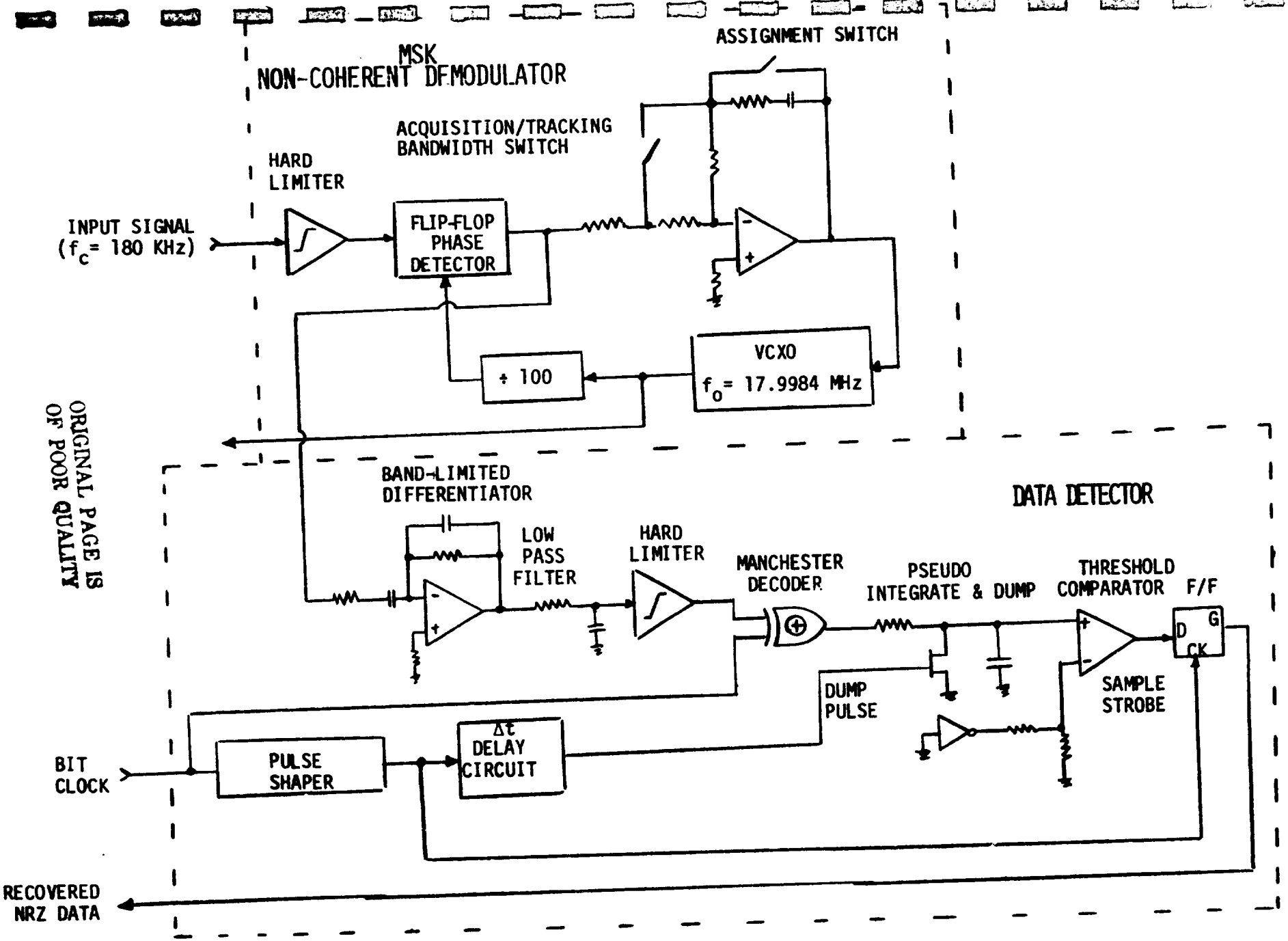
The following sections detail the hardware comprising the coherent and non-coherent demodulators and the frequency measurement circuit.

G.1 Non-Coherent MSK Demodulator

A block diagram of the non-coherent MSK demodulator is shown in Figure 2-16. The incoming signal, which is set to a carrier frequency of approximately 180 kHz by the Search Subsystem Simulator, is received by a second order phase lock loop. The phase lock loop locks to and tracks the carrier of the incoming modulated signal and provides a vehicle for performing doppler frequency measurements. The MSK modulation format is a coherent FSK modulation technique, and the positive (mark) and negative (space) steps in frequency with respect to the carrier constitute - since no phase discontinuties occur during frequency transitions - phase error ramps from the phase detector. The phase ramps are differentiated to give bi-polar voltage steps which are a noise contaminated version of the transmitted Manchester encoded digital data steam. The phase lock loop then serves as a discriminator type demodulator with the phase lock mechanism providing a means of automatically setting the null point or center frequency of the discriminator to the frequency of the carrier during the transmission of data. The NRZ data stream must be Manchester encoded to guarantee the presence of carrier during data modulation.

The voltage steps from the discriminator are then submitted to a data detector which employs an exclusive-or circuit to remove the Manchester encoding followed by a pseudo integrate and dump circuit and decision circuit to recover the NRZ data stream. The bit clock is not recovered from the Manchester encoded data stream but rather is hard-wired from the MSK Transmitter Simulator.

The loop parameters for the phase lock loop are determined by the incoming data rate, the Search Subsystem Simulator analyzing bandwidth, the minimum available signal-to-noise ratio, and the duration of the CW preamble - which determines how quickly the loop must acquire the signal. The initial frequency uncertainity over which the phase lock loop must acquire is $\pm$ 1.5 times the Search Subsystem Simulator analyzing bandwidth, or 240 Hz. The multiplicative factor of 1.5 was adopted to allow the assignment logic to be off by $\pm$ 1 bin should bin spreading occur in the search system in the presence of strong signals. A loop lock-in range (signal acquisition without cycle slipping) of $\pm$ 240 Hz equates to a loop noise bandwidth of 565 Hz assuming a .707 damping factor. This noise bandwidth provides adequate signal-to-noise for acquisition if it is assumed that the data detection process following the



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OF POOR QUALITY

NON-COHERENT MSK DEMODULATOR
AND DATA DETECTOR
Figure 2-16

phase lock loop achieves a minimum bit error rate performance of 10^{-4}. For an ideal coherent PSK data detection process, an E/N_o of 8 dB is required, which equates to a signal-to-noise ratio of 8 dB in 320 Hz or 5.5 dB in 565 Hz. Adding margin to account for the fact that the non-coherent process is not ideal results in a more than adequate acquisition threshold in the 565 Hz acquisition noise bandwidth.

It was also determined from breadboard studies conducted during the initial phases of the Random Access Measurement System (RAMS) program that the tracking bandwidth of the loop should be no more than 0.185 times the data rate to keep the droop in the demodulated output due to the loop attempting to track the data excursions from becoming excessive. The lower bound on the tracking loop bandwidth is determined by the maximum amount of doppler that must be accommodated by the loop. For a transmission time of one second or less, and using an integrator in the implementation of the loop filter, the phase error in the phase lock loop can be approximated by

$$\phi_e = \frac{\Delta\dot{\omega}}{\omega_n^2}$$

The tracking noise bandwidth was chosen to be 19.8 Hz which, for a maximum doppler rate of 80 Hz/sec, results in a phase error no greater than 0.4 radians. The 0.4 radians of phase error, when added with the data phase ramp of $\pm \pi/2$ radians, leaves a phase error margin of approximately 1.2 radians to accommodate phase noise.

It is clear that the loop will have to contain a switching mechanism to switch between acquisition and tracking bandwidths. The switching between loop bandwidths is physically accomplished in the same manner as was done in the RAMS instrument - by switching resistors to change the time constants in the active loop filter circuit. Since there is no loop in-lock indication incorporated into the phase lock loop, the command to switch bandwidths is issued after a fixed time period has elapsed since the assignment was made by the Search Subsystem Simulator. The lock-up transient for the acquisition bandwidth is approximately one millisecond, assuming the incoming signal falls within the loop bandwidth or lock-in range. A selectable interval of one to four milliseconds is generated by utilizing the initial "assignment store" pulse and a 1 millisecond time mark from the time-out interval timer in the Search Subsystem Simulator. During this selectable "assignment" interval the phase lock loop is in the acquisition bandwidth to acquire the incoming signal. At the conclusion of the one to four millisecond assignment interval

it is assumed that the phase lock loop has acquired the signal and the loop is switched to the tracking bandwidth. Although this scheme is utilized in the breadboard system to avoid building additional in-lock indication hardware, the scheme is a viable alternative for a final hardware design. The only disadvantage to the scheme is the inability to recognize the failure to lock to the signal and thereby release the loop for another assignment. With the automatic loop switching scheme as implemented in the breadboard, the first indication that the signal is not being properly received is the failure to receive the frame synchronization code. This is truly a disadvantage in that a loop is occupied for a large period of time on false alarms output by the Search Subsystem Simulator and as a consequence the probability of having a loop or receive channel available to assign to a detected signal is degraded.

A final consideration in the implementation of the phase lock loop is the hardware implementation of the frequency measurement circuitry. To measure the frequency of a signal to an 0.1 Hz resolution requires a measurement window of 10 seconds. However, if the signal to be measured is multiplied by N, then the multiplied signal need only be measured to an accuracy of N X 0.1 Hz, which requires a measurement window on 10/N seconds, to obtain the same 0.1 Hz measurement resolution in frequency of the original signal. This principle is utilized in the phase lock loop to reduce the measurement time required to obtain an 0.1 Hz resolution. The VCXO output is divided by 100 before it is applied to the phase detector, and thus runs at a frequency one hundred times the incoming signal frequency. The frequency measurement is made on the frequency directly output from the VCXO. To obtain an 0.1 Hz measurement resolution of the incoming frequency thus requires a 10 Hz measurement resolution at the VCXO, which can be accomplished in a measurement window of only 0.1 seconds. The VCXO rest frequency is then one hundred times the nominal frequency input into the Receive Channel Simulator - or 17.9984 MHz.

The critical design parameters for the phase lock loop are summarized in Table 2-1. The preceeding discussions have highlighted the tradeoffs and system considerations weighed in reaching the parameters listed in Table 2-1. Every effort has been made to make the phase lock loop design compatible with a design which would be used in implementing an actual ADC/PL system, so that the demodulation characteristics exhibited by the phase lock loop would be indicative of that obtainable in an actual system.

The data detector used to recover the demodulated data stream is also shown in Figure 2-16. It is noted that no hardware is provided to recover the bit clock from the Manchester encoded data stream output by the phase lock

Table 2-1

Phase Lock Loop Parameters

Nominal Input Frequency	179,984 Hz
Frequency Acquisition Range	±240 Hz
VCXO Rest Frequency	17.9984 MHz
Frequency Measurement Accuracy	±0.1 Hz
Frequency Measurement Window	100 Milliseconds
Nominal Acquisition Lock-up Time	1.0 Millisecond

		ACQUISITION	TRACK
Loop Natural Frequency	(ω_n)	1066 rad/sec	35 rad/sec
Damping Factor	(ζ)	.707	.3
Loop Noise Bandwidth	(B_L)	565 Hz	19.8 Hz

loop. Both a phase lock loop bit synchronizer and an open loop ringing circuit bit synchronizer were developed on the RAMS program for recovering the bit clock from a stream of Manchester encoded data, and the E/N_o performance of both schemes were well documented. To repeat these efforts on the ADC/PL breadboard would not provide any new significant performance data to justify the time and hardware expenditure that would be required. The bit clock is thus provided by the data generator housed in the MSK Transmitter Simulator.

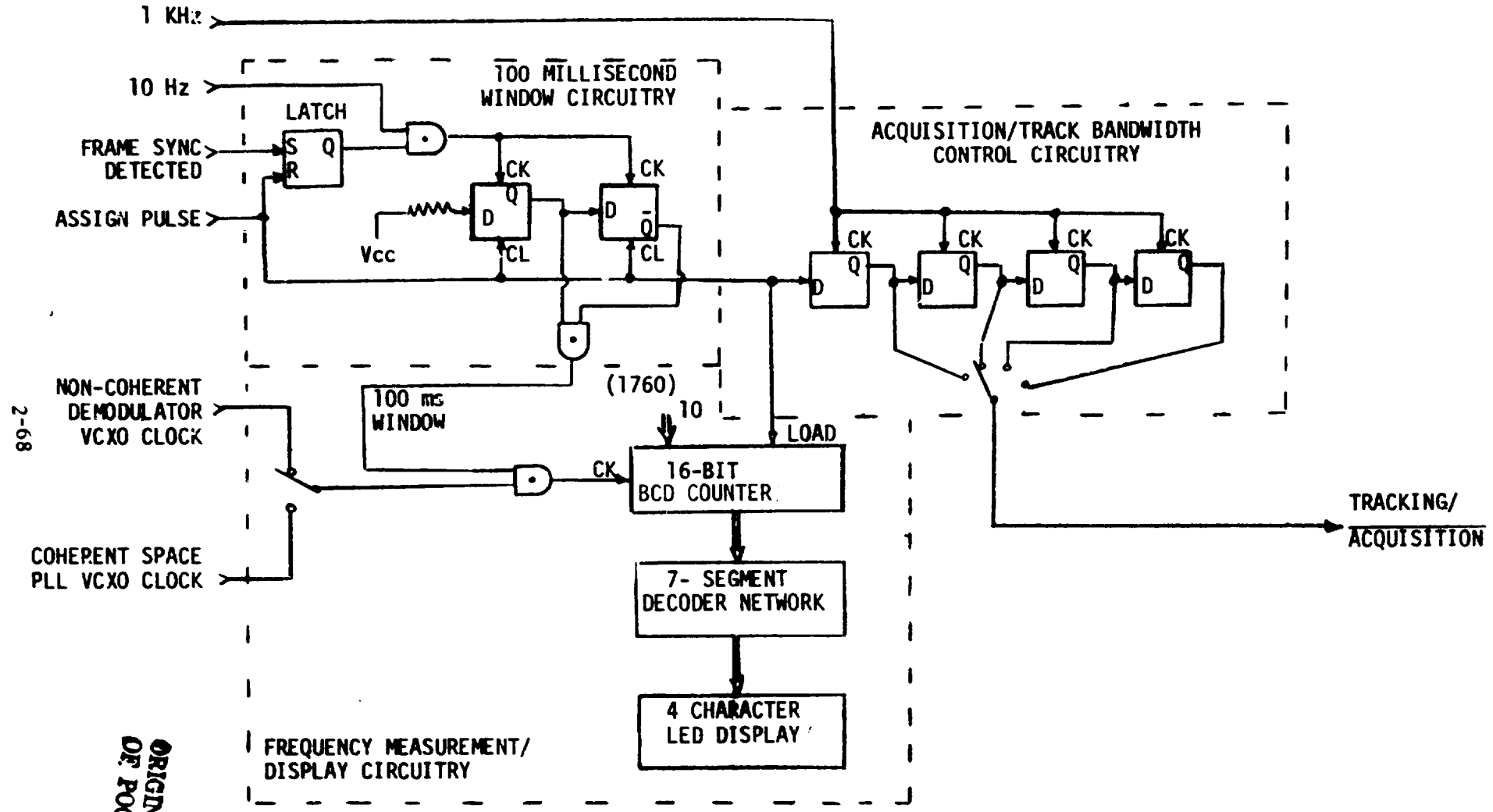
The demodulated data stream from the output of the differentiator following the phase lock loop phase detector is applied to a low pass filter to remove any residual carrier component. The low pass filter is a single pole RC filter with a 3 dB point at 1920 Hz or six times the bit rate of 320 bps. This bandwidth selection will give approximately 55 dB of rejection of the 180 kHz i-f and yet pass approximately 96% (from calculations conducted on the RAMS program) of the data energy. The output of the low pass filter is input to a hard limiter whose output drives one part of an exclusive - or circuit. The input into the other port of the exclusive - or circuit is the bit clock from the data generator. The exclusive - or circuit removes the Manchester encoding from the data stream and outputs an NRZ data stream. The data detector is a pseudo integrate and dump circuit utilizing an RC time constant and a FET transistor to dump the charge accumulated in the capacitor. At the start of a bit period the RC time constant begins integrating the output of the exclusive - or circuit. At the conclusion of the bit period, a differentiator circuit, which is triggered by a positive transition of the bit clock, creates a clock pulse which serves to strobe the output of the threshold comparator into a holding flipflop. The threshold comparator reference level is set by a resistor divide - down network driven by a logic "one" from a T^2L 5404 inverter network. The values of the resistor network are an exact duplicate of the values chosen on the RAMS program for the same function and are chosen to optimize the "one - zero" selection process for the data detector implementation used. The sample or strobe clock is delayed to generate a dump pulse to dump the charge accumulated in the capacitor during the previous bit period. The dumping mechanism assures that each bit decision is independent of the previous bit received. The output of the flipflop is the recovered data stream which is sent to the data checker for validation.

G.2 Frequency Measurement Circuit

A block diagram of the frequency measurement circuit is shown in Figure 2-17. The circuit provides three major functions - it generates a 100 millisecond window to serve as the time base for the frequency measurement, it provides the control circuitry for switching the phase lock loop bandwidths in either demodulator from a wide band acquisition bandwidth to a narrow band tracking bandwidth, and it contains a binary coded decimal counter and LED display for implementing and displaying the frequency measurement. The 100 millisecond window is initiated on the first 10 Hz clock edge that follows the reception of the frame synchronization code as detected in the data checker. On the next 10 Hz clock edge the window is disabled. The accuracy of the 100 millisecond window is thus directly dependent on the accuracy of the 10 Hz clock - which is derived from the 10.24 MHz crystal oscillator in the Search Subsystem Simulator. It is also noted that the 100 millisecond window occurs during the transmission of data, and thus it is not necessary that the preamble portion of the message be extended to accommodate the frequency measurement.

The bandwidth control function controls the switching between wide band acquisition and narrow band tracking bandwidths in the demodulator phase lock loops. Before detecting the presence of a signal in the Search Subsystem Simulator, the loops are set to the wide band acquisition bandwidth. When the assign pulse occurs, indicating a signal has been detected, a flipflop is set to a logic one on the next 1 KHz clock edge. Since the 1 KHz clock and the assign pulse are synchronous, the flipflop will follow the transition of the assign pulse one millisecond after the occurrence of the pulse, and thus constitutes a one millisecond delay. Three other flipflops follow this first flipflop to implement an additional three milliseconds of delay. The bandwidth control signal can be taken from any one of the four flipflop outputs. In this way, the dwell time in the wide band acquisition bandwidth following the assignment of the phase lock loop to a detected signal can be varied from one to four milliseconds in one millisecond steps. When the bandwidth control signal becomes true, the loop bandwidth is switched to the narrow band tracking bandwidth.

The assign pulse serves two other functions in the frequency measurement circuit. It clears a latch in the 100 millisecond window circuitry to initialize the circuitry for the generation of a new 100 millisecond window and it loads a count of 1760_{10} into the frequency measurement counter. The presetting of the counter prior to making the frequency measurement biases the resulting count so that the output directly displays the difference between the frequency measured



FREQUENCY MEASUREMENT CIRCUIT

Figure 2-17

and a reference frequency. For the non-coherent demodulator, the incoming carrier will be at 180,064 Hz ± 240 Hz. The frequency uncertainty of ± 240 Hz allows an assignment uncertainty of ± 1.5 frequency bins in the Search Subsystem Simulator. The VCXO frequency will then be 18,006,400 Hz ± 24,000 Hz. For a VCXO frequency of 17,982,400 Hz, the counter will read

$$\text{FRACTIONAL PART OF} \left| \frac{17{,}982{,}400 \times 0.1 + 1760}{10^4} \right| = 0$$

(100 Millisecond Window; Incoming Frequency; Preset Number; Count Range)

During the 100 millisecond window, the counter will overflow many times. Taking the fractional part of the above expression gives the count that resides in the counter at the conclusion of the 100 millisecond window. For a VCXO frequency of 18,030,400 the counter will read

$$\text{FRACTIONAL PART OF} \left| \frac{18{,}030{,}400 \times 0.1 + 1760}{10^4} \right| = 4800$$

The resulting count of 4800 is interpreted as 480.0 Hz above the reference frequency of 179,824 Hz. The display then displays the number of cycles, to the nearest tenth of a cycle, the measured frequency is above 179,824 Hz .

G.3 Coherent MSK Demodulator

Although not specifically required on the ADC/PL breadboard effort, every effort was made to include a coherent MSK demodulator in the Receive Channel Simulator so that a comparison could be made between the performance characteristics of the coherent and non-coherent demodulators. Although the entire ADC/PL breadboard was constructed to accommodate either a coherent or non-coherent demodulator, time did not allow the coherent MSK demodulator to be constructed. For this reason, no descriptions concerning the theory, implementation, or performance characteristics of the coherent demodulator will be presented in this final report.

SECTION III

BREADBOARD TEST RESULTS

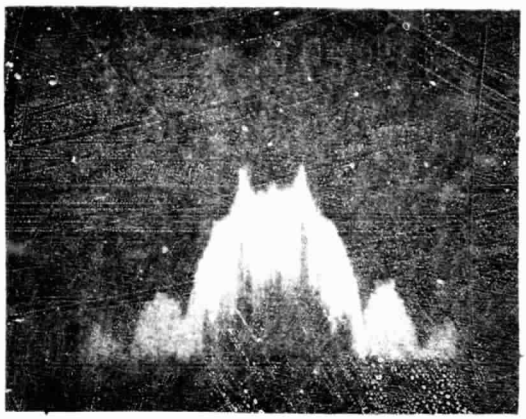
A. INTRODUCTION

This section describes the results of the tests conducted on the ADC/PL breadboard unit described in Section II. The test hierarchy can be divided into four major categories - chirp-z transformer tests, MSK demodulator tests, frequency measurement tests, and system throughput tests. The majority of testing is concerned with the performance of the chirp-z transformer and the MSK demodulator since these two subsystems profoundly effect the traffic flow and operational characteristics achievable in an ADC/PL system. In any data collection system which is restricted both in usable bandwidth and view time, two parameters are of utmost importance - spectral transmission efficiency and temporal transmission efficiency. Spectral efficiency of the transmission consists of two properties of the spectral signature of the transmitted signal. The first property is the amount of bandwidth required to transmit a certain percentage of the total signal energy as normalized to the bit rate. For MSK modulation it can be shown that 99 percent of the transmitted power is contained within a double-sided bandwidth of 2.3 times the data rate. The second property is the behavior of the spectral signature outside the 99% signal power bandwidth - i.e., the presence or absence of significant sidebands or leakage components. The MSK modulation technique was found to be free of any significant sidelobe terms apart from those present in the incoming data stream itself. Figure 3-1 shows the spectral signature of MSK modulation both for NRZ and Manchester encoded data taken from the ADC/PL breadboard. These pictures summarize the spectral properties just discussed and show that MSK is indeed an attractive modulation format from the standpoint of spectral transmission efficiency. The question to be addressed in this section is whether or not the use of MSK modulation results in penalities in either E/N_o performance or receiver complexity.

Temporal transmission efficiency is a measure of the use made of the time available in the orbiting satellite view time. The most efficient use of time would simply be to transmit data only - with no preamble preceeding the transmission of data for detecting the presence of the signal, assigning a receive channel to the signal, and acquiring the signal. The bit rate can also be increased to lower the transmission time for a given message, but this results in a larger spectral occupancy and thus does not yield any benefits in terms of a band-limited, time-limited system. Temporal efficiency then is defined to be the amount of message transmission time that must be allotted

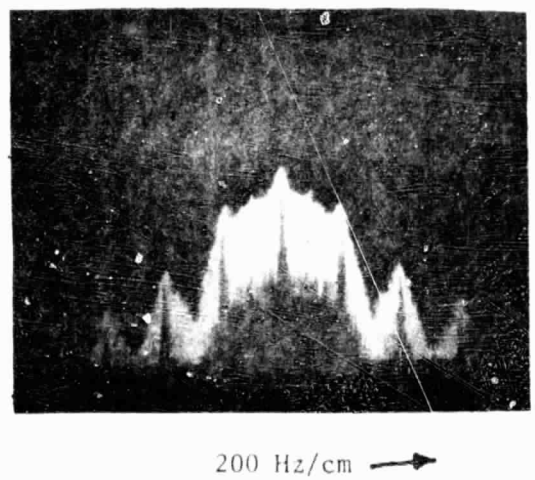
SPECTRA OF MSK MODULATION
AS PROCESSED BY HP141T SPECTRUM ANALYZER

FIGURE 3-1



320 BPS MSK MODULATED NRZ DATA
FROM 32,767 BIT PN CODE GENERATOR

30 HZ ANALYZING BANDWIDTH



320 BPS MSK MODULATED MANCHESTER
ENCODED DATA FROM 32,767
BIT PN CODE GENERATOR

30 HZ ANALYZING BANDWIDTH

to the set-up time in the satellite receive system. The chirp-z transformer is a signal search mechanism which will optimize the temporal transmission efficiency in that the search time for the chirp-z transformer is the inverse of the analyzing bandwidth used in the search process. Specifying a nominal transmit power for the data collection platforms, and calculating the communication link parameters yields a minimum expected signal power into the receiver unit aboard the satellite. For a given false alarm rate and a desired probability of detection, the analyzing bandwidth in the search subsystem is defined. The minimum time to search the entire spectral band using the required analyzing bandwidth would be to use a bank of filters with each filter having a bandwidth equal to the analyzing bandwidth and separated in center frequency from the two adjacent filters by the same analyzing bandwidth. The chirp-z transformer in effect implements just such a filter bank and thus requires the minimum amount of analyzing time for the signal power received. The question to be addressed in this section is the performance of the chirp-z transformer in terms of parameters such as probability of detection vs. signal-to-noise ratio, dynamic range, bin spreading, etc.

The frequency measurement circuitry counts the zero crossings of the demodulator's phase lock loop VCXO output for a fixed period of time. The circuitry is designed to provide an 0.1 Hz measurement resolution. The frequency measurement tests are designed to verify the scheme utilized to obtain the 0.1 Hz resolution and to measure the deviation in the measurements, if any, as a function of the signal-to-noise ratio.

The final set of tests are the system throughput tests where an NRZ or Manchester encoded data stream is MSK modulated in the MSK Transmitter Simulator, routed through the Communications Link Simulator, and detected and assigned to the Receive Channel Simulator in the Search Subsystem Simulator. The signal is demodulated and the digital data stream recovered in the Receive Channel Simulator and the recovered data is verified against what was transmitted in the data checker housed in the MSK Transmitter Simulator. The purpose of the test is to verify that the MSK and chirp-z transformer technologies can be utilized together in an ADC/PL application and that the individual performance parameters associated with each technology, when combined into overall system performance parameters, agree with those system parameters found in the throughput tests. The throughput tests then serve as summarizing tests to validate the findings on the individual components comprising the ADC/PL breadboard.

B. CHIRP-Z TRANSFORMER TEST RESULTS

B.1 General

The specific parameters to be tested in the chirp-z transformer are

(a) Probability of detection vs. signal-to-noise ratio for different probability of false alarm settings

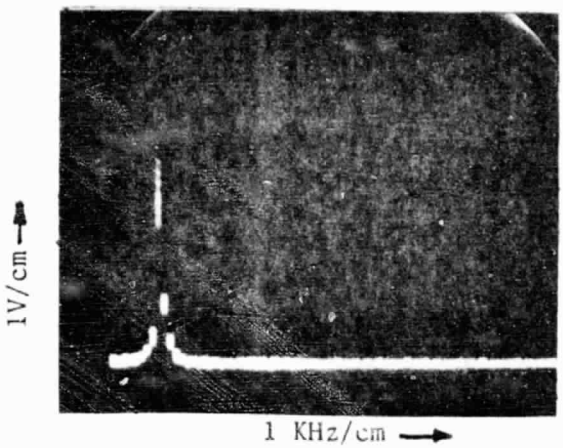
(b) Dynamic range (bin spreading)

Two other parameters - the time required to detect the presence of a signal and assign a phase lock loop and the time required to recycle a channel assignment after a false alarm - are also very important parameters in a search subsystem to be utilized in an ADC/PL system. These parameters will also be presented in this section, although, as will be discussed, no specific testing is required to validate the characteristics associated with these parameters. A final consideration is the temperature characteristics of CCD devices. No specific testing has been conducted on the ADC/PL breadboard concerning the temperature characteristics of CCD devices. However, a discussion is presented in this section to highlight which parameters of CCD devices are temperature dependent and to present temperature data on these temperature dependent parameters. The temperature data was taken on a previous program.

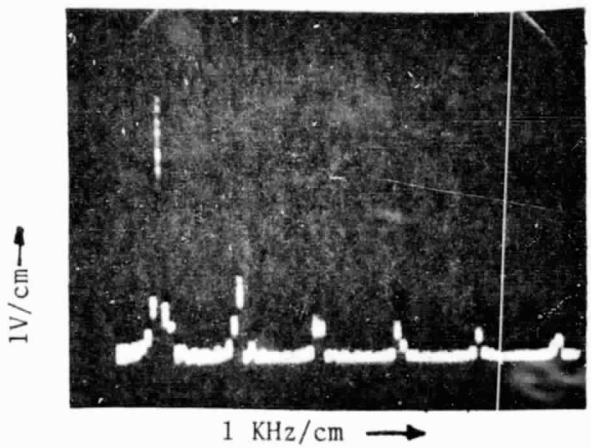
To provide an intuitive understanding of the output format of the chirp-z transformer, several photographs were taken of oscilloscope traces of the actual transformer output. As described in Section II. F.1.a, the chirp-z transformer outputs a serial train of coefficients, with each coefficient representing the spectral energy present in a 160 Hz frequency cell. A total of 500 coefficients are output representing a frequency band from approximately -40 KHz to +40 KHz. Figure 3-2 depicts the serial coefficient train that results from a 1.1 KHz sine wave, square wave, triangular wave, and sawtooth waveform. Only the real coefficients are shown in Figure 3-2. It is obvious from Figure 3-2 that the coefficients, when lined up side by side as on an oscilloscope trace, give a discrete representation of the Fourier transformation of the incoming signal. Another informative set of photographs is presented in Figure 3-3, with again only the real or positive coefficients displayed for the chirp-z transformer derived spectra. Here the spectrum of MSK modulation, both with and without Manchester encoding, is compared against the coefficient pattern output by the chirp-z transformer upon receiving the same MSK modulated signal. The similarity between the two resulting spectra for both NRZ and Manchester encoded data is obvious. Figures 3-2 and 3-3 also show that the chirp-z transformer not only outputs coefficients for those frequency bins which possess spectral

SPECTRA OF DIFFERENT SIGNAL WAVEFORMS
PROCESSED BY THE CHIRP-Z TRANSFORMER
FIGURE 3-2

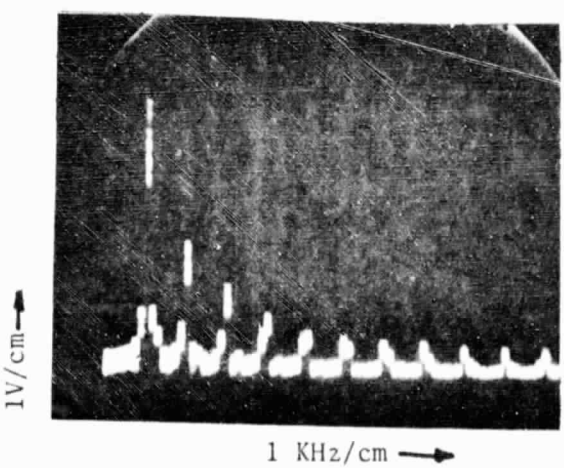
ANALYZING BANDWIDTH = 160 Hz



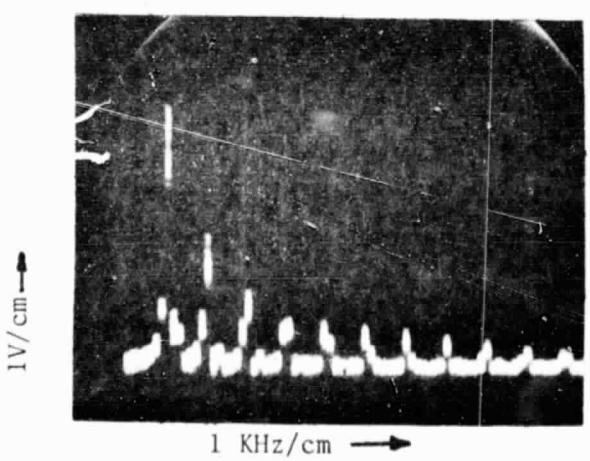
1.1 KHZ SINE WAVE SPECTRUM



1.1 KHZ SQUARE WAVE SPECTRUM



1.1 KHZ TRIANGULAR WAVE SPECTRUM

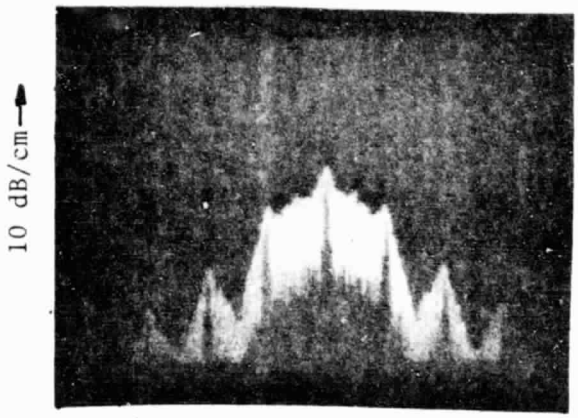


1.1 KHZ SAWTOOTH WAVE SPECTRUM

SPECTRA OF MSK MODULATION

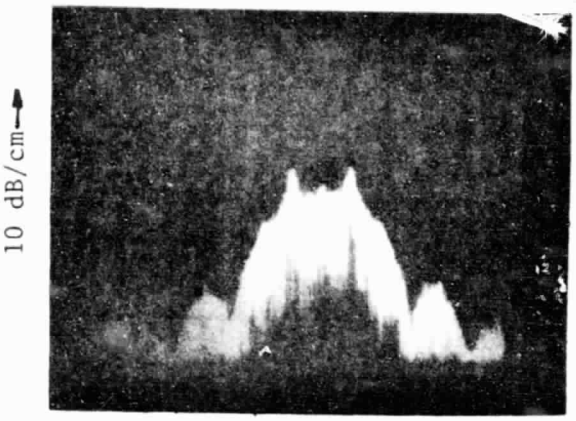
FIGURE 3-3

SPECTRA AS PROCESSED BY AN HP 141T SPECTRUM ANALYZER



320 BPS MANCHESTER ENCODED DATA

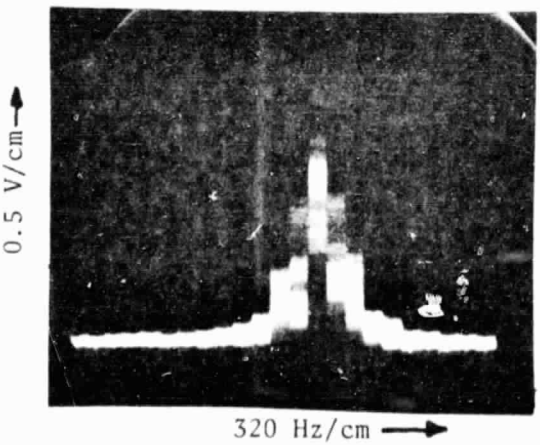
30 HZ ANALYZING BANDWIDTH



320 BPS NRZ DATA

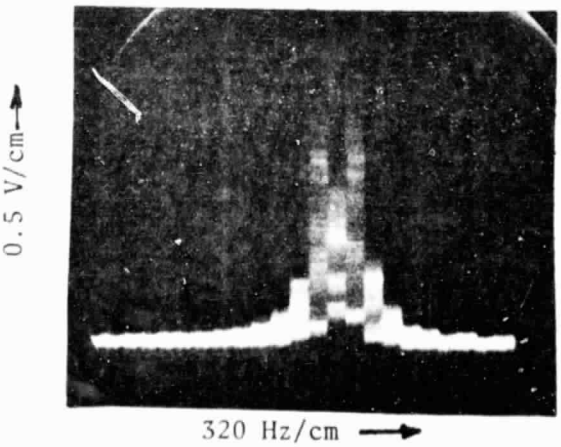
30 HZ ANALYZING BANDWIDTH

SPECTRA AS PROCESSED BY THE CHIRP-Z TRANSFORMER



320 BPS MANCHESTER ENCODED DATA

160 HZ ANALYZING BANDWIDTH



320 BPS NRZ DATA

160 Hz ANALYZING BANDWIDTH

energy, but the magnitude of the coefficients directly reflects the amount of spectral energy present in the frequency bin. This property is key to the implementation of a detection/false alarm circuit following the chirp-z transformer.

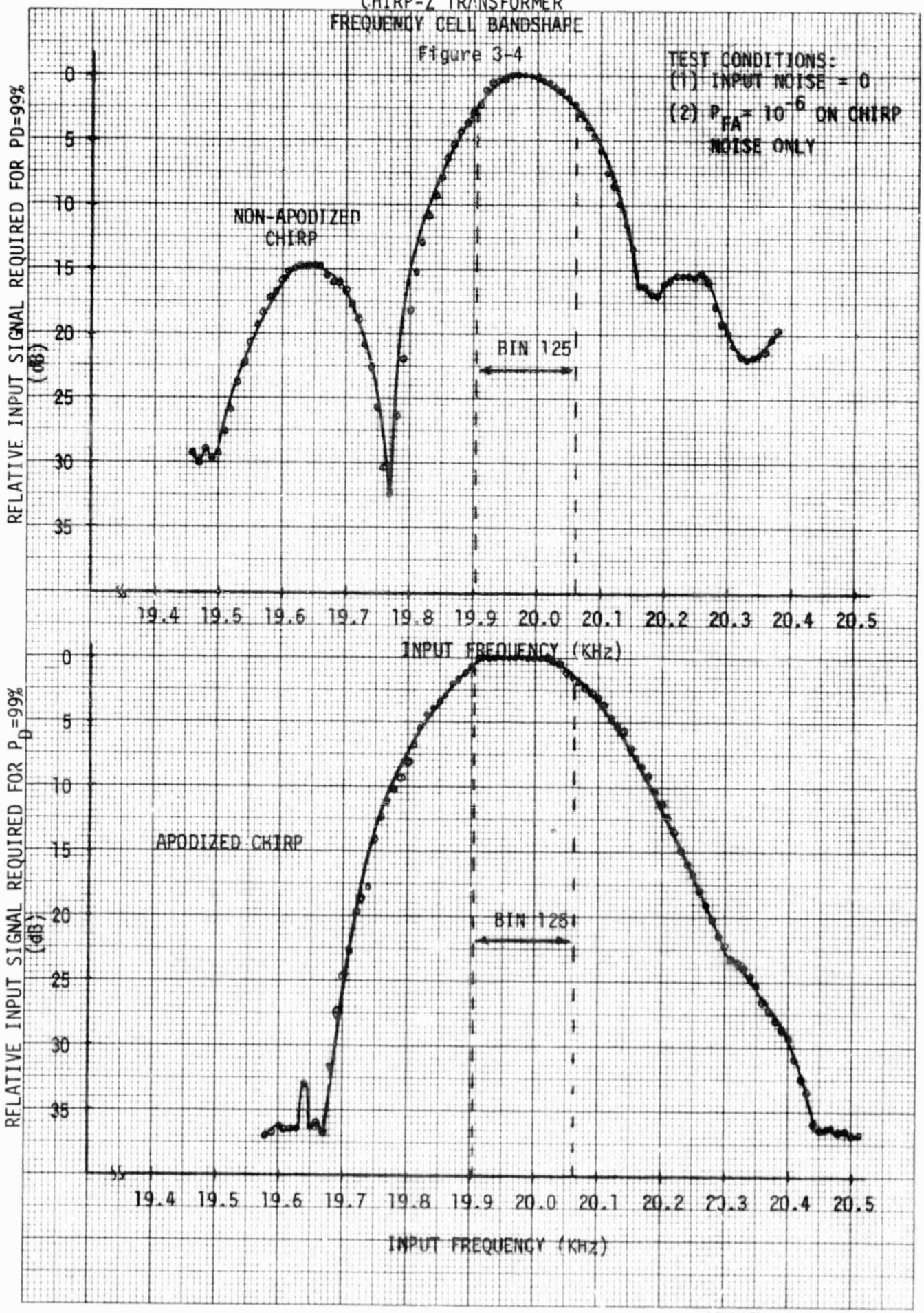
B.2 Probability of Detection/False Alarm Rate Measurements

The probability of detection tests were conducted with the express purpose of evaluating the performance of the chirp-z transformer as a search mechanism. In particular, the tests were configured to evaluate or compare the performance of non-apodized and apodized transformers and the use of only real or real and imaginary (composite) coefficients in the detection process. The evaluation of apodized vs. non-apodized transformers involves using two different chirp-z transformer chips - with one chip having its tap weights adjusted so as to effect a weighted window function to reduce sidelobes or spectral leakage components. In terms of dynamic range and bin spreading, the apodized transformer is definitely preferable. However, the question to be addressed is whether or not the apodized chip effects a penalty in terms of probability of detection as a function of signal-to-noise ratio.

The answer to the question of whether it is better to use only real or both real and imaginary coefficients in the detection process initially appears to be obvious - the composite coefficients are preferable since using both sets of coefficients provides two tries at detecting the presence of a signal in a single sweep of the search band. However, this is not necessarily true if a constant false alarm rate is to be maintained since using imaginary as well as real coefficients effectively doubles the number of coefficients to be processed in the threshold detection circuitry and will therefore increase by some factor the number of false alarms encountered in a single sweep of the search band. Thus only if the false alarm rate in the threshold circuitry is adjusted to be equivalent for both real and composite coefficients can a comparison be made between using only real or both real and imaginary coefficients. The test results presented in this section comparing only real versus both real and imaginary coefficients were measured using equal false alarm rates.

Comparison data is also provided concerning the performance of the chirp-z transformer when a signal lies at the edge of two adjacent frequency bins as opposed to lying in the center of a given frequency bin. Figure 3-4 shows the bin shape for both apodized and non-apodized chirp-z transformer chips.

CHIRP-Z TRANSFORMER
FREQUENCY CELL BANDSHAPE
Figure 3-4



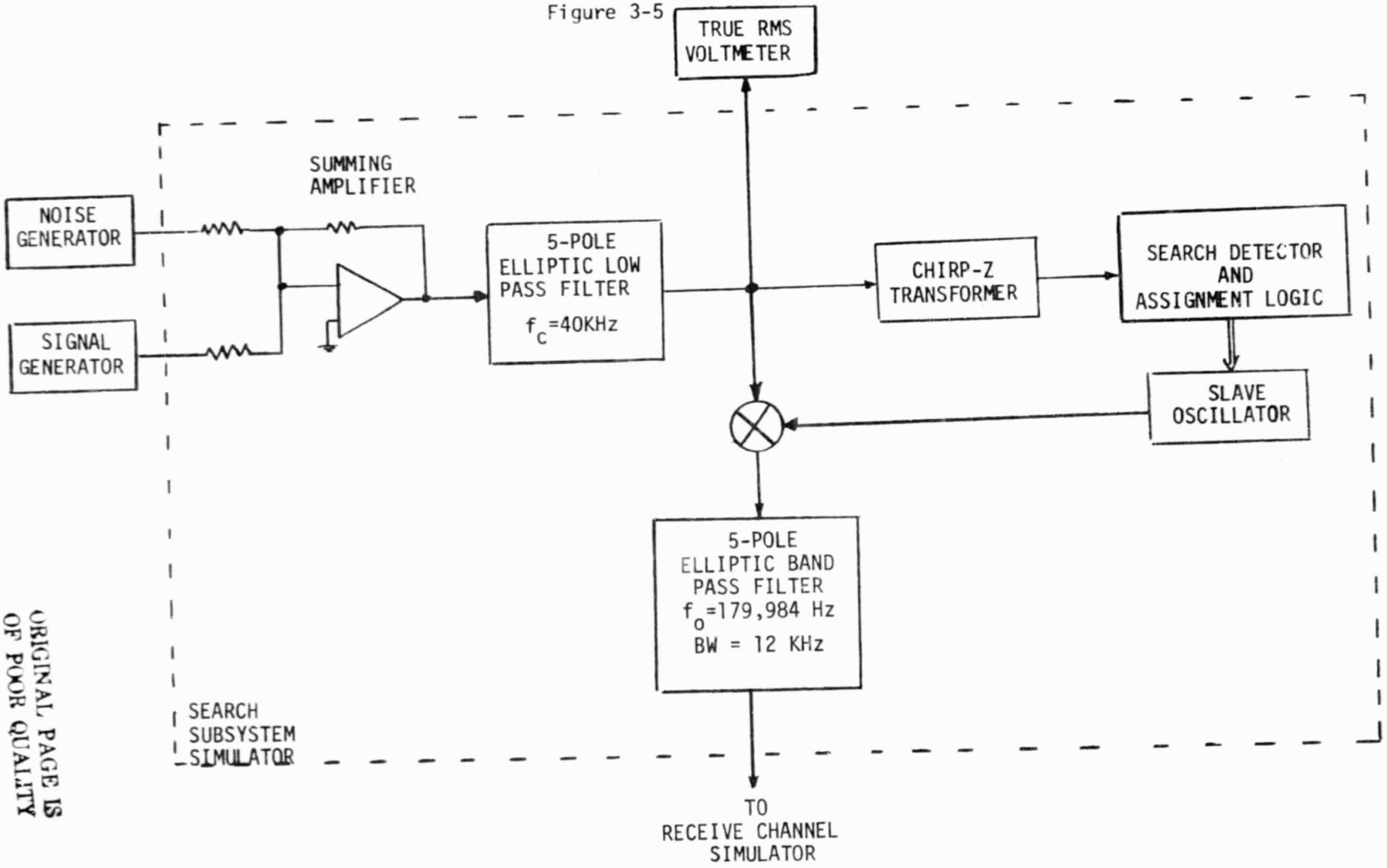
The curves were obtained by measuring the amount of signal power required to maintain a constant probability of detection at a given frequency bin, as normalized to the amount of power required when the signal resides exactly in the center of the given frequency bin, as a function of frequency offset from the center of the frequency bin. Bin 125, the center of which is 20 kHz, was the particular frequency bin used. Two conclusions are readily drawn in examining Figure 3-4. The non-apodized chip has a much narrower main lobe than the apodized chip, but the sidelobes of the apodized chip are almost nonexistent as compared to the non-apodized chip. Also, the non-apodized chip exhibits about a 3-dB roll-off at the edge of bin 125, while the apodized chip exhibits hardly any roll-off at all at the bin edges. It would be expected then that the apodized chip would show little preference in terms of probability of detection performance as to whether the signal occurred at the center or the edge of a bin. However, as the data in this section will show, a degradation in the probability of detection was found in the case of the apodized chip when the signal moved to the edge of a bin.

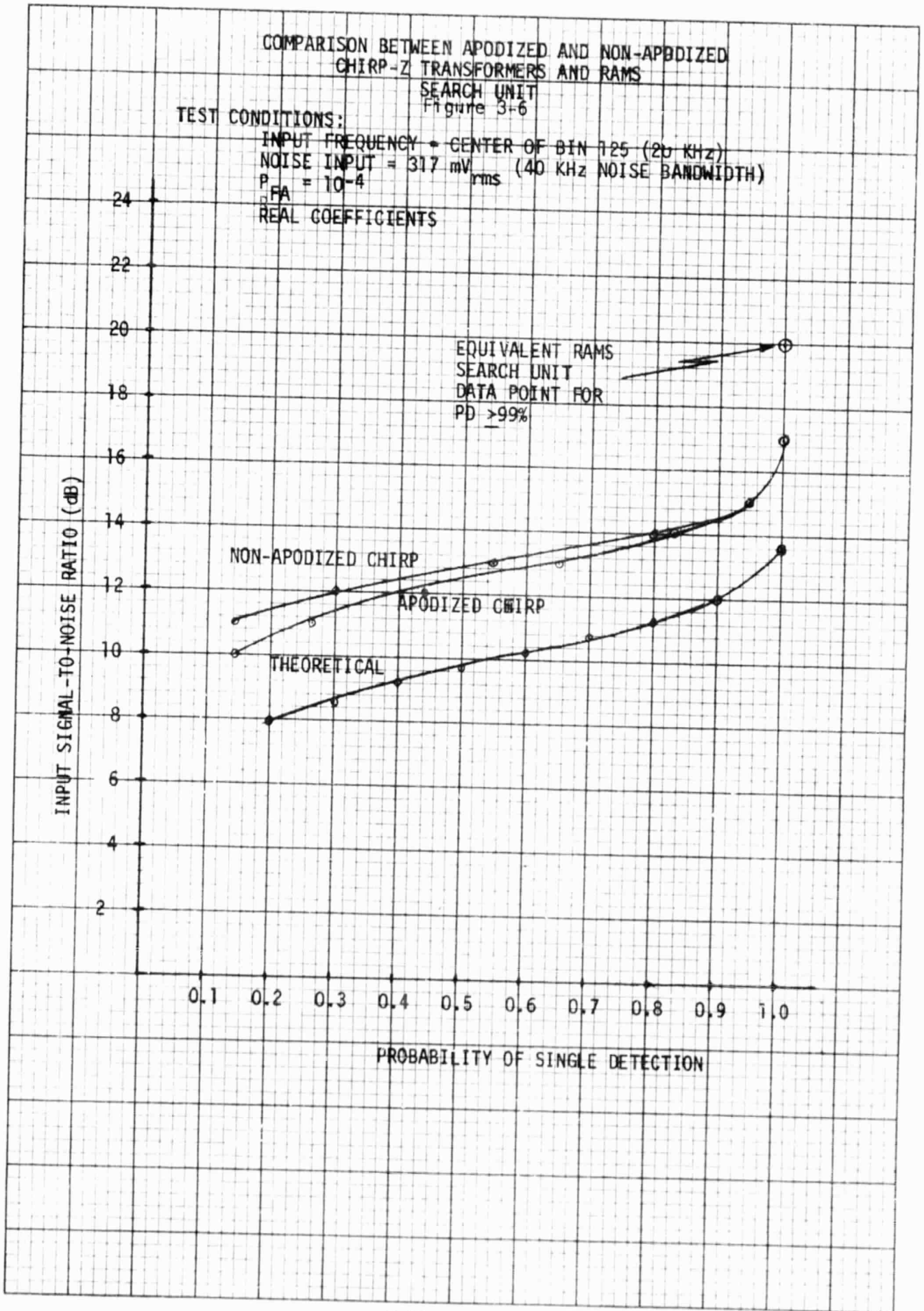
The test setup used for all probability of detection tests is shown in Figure 3-5. The input consists of a sinusoid or MSK modulated signal summed with noise. The 5-pole low pass elliptic filter serves to define a noise bandwidth of 40 kHz for determining the signal to noise ratio into both the chirp-z transformer and the Receive Channel Simulator. By measuring the noise power at the output of the filter, and assuming the noise is Gaussian and evenly distributed across the 0 -40 kHz band, the noise power density can be obtained. Having the noise power density and measuring the signal power at the output of the elliptic filter provides the data required to calculate the signal-to-noise ratio in either the analyzing bandwidth of the chirp-z transformer or the demodulation bandwidth of the Receive Channel Simulator.

All probability of detection testing is done using a pre-determined false alarm rate. The false alarm rate is set to the desired value by inputting Gaussian noise at the level desired, since AGC is not included in the ADC/PL breadboard, and adjusting the threshold level of the threshold detector until the false alarm rate desired is obtained. The noise input level and threshold setting then remain fixed, and the different signal-to-noise ratios required to plot the probability of detection curves are obtained by varying the level of the incoming signal. Figure 3-6 is a probability of detection plot comparing the apodized and non-apodized chirp-z transformer chips and the RAMS instrument. To make the comparisons valid, the false alarm rate was set to 10^{-4}, which was the setting used on the RAMS instrument. A theoretical probability of detection

TEST CONFIGURATION
CHIRP-Z TRANSFORMER & MSK DEMODULATOR

Figure 3-5

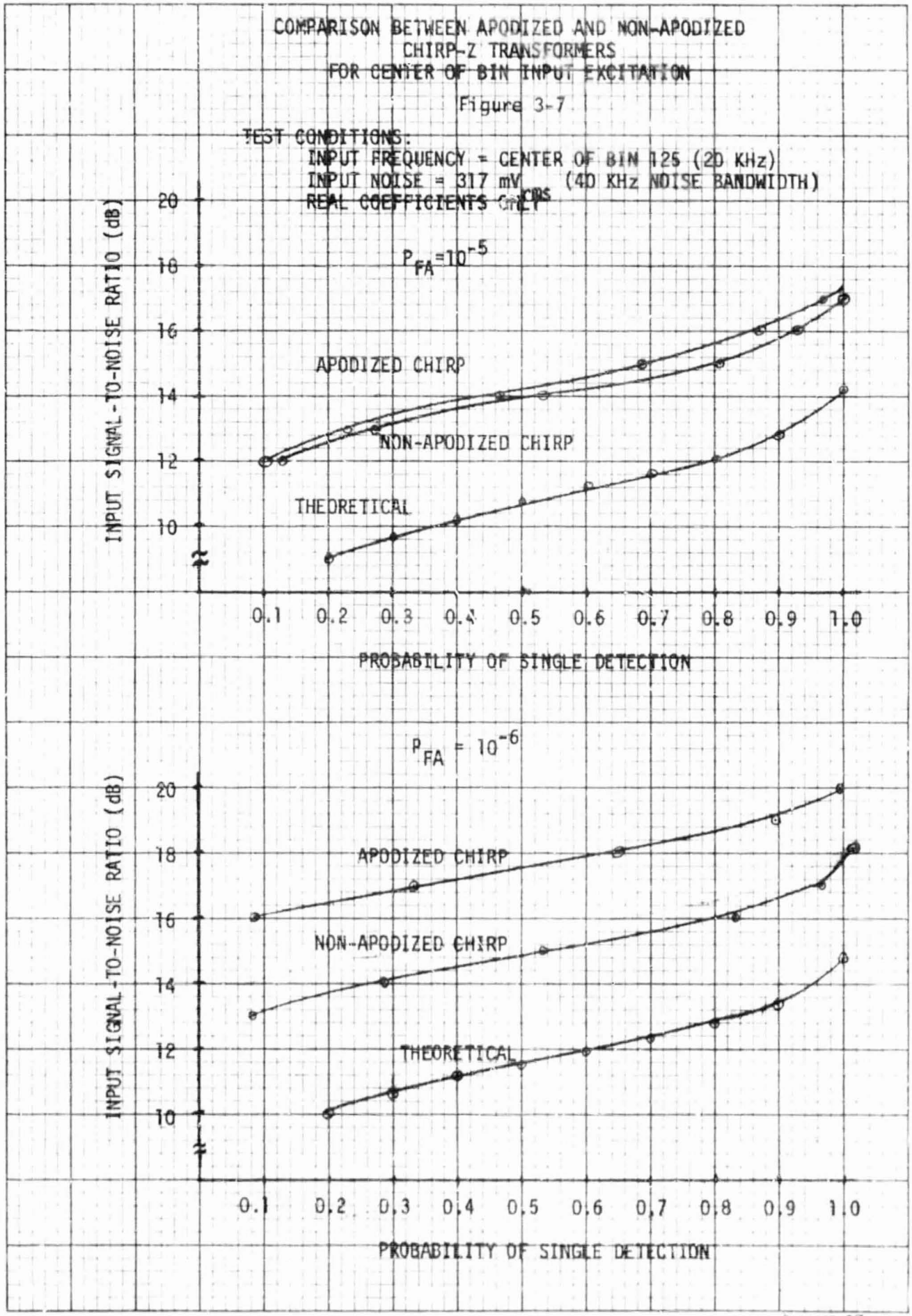


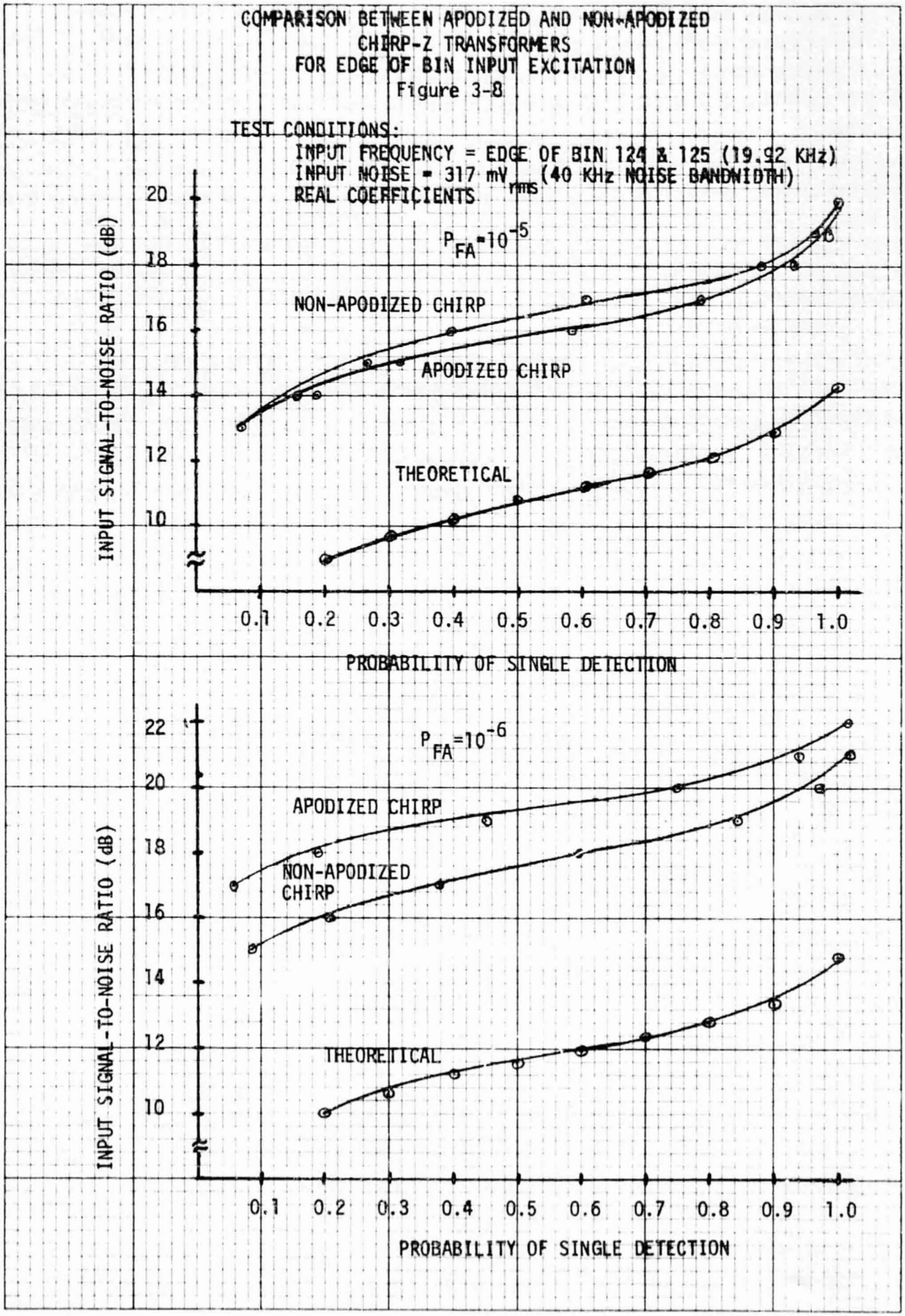


plot showing the theoretical limitation in performance is also included as a benchmark. Two encouraging observations are made from Figure 3-6 - there is little difference in performance between the apodized and non-apodized chips, and the probability of detection curves for either chirp-z transformer is only 2.5 dB above the theoretical curve, as compared to 6.5 dB for the RAMS search unit.

Figures 3-7 and 3-8 are also probability of detection plots comparing the apodized and non-apodized chirp-z transformer chips for false alarm rates of 10^{-5} and 10^{-6}. Figure 3-7 shows the probability of detection plots for a signal located at the center of one of the transformer's frequency bins and Figure 3-8 shows the same plots for a signal located exactly at the edge of two adjacent frequency bins. Both figures show that for a false alarm rate of 10^{-5}, the apodized and non-apodized chips are practically equal in performance, as was the case for the 10^{-4} false alarm rate depicted in Figure 3-6. For a false alarm rate of 10^{-6}, the non-apodized chip shows about a 2 dB improvement over the non-apodized chip. For the 10^{-5} false alarm rate, both curves are about 5 dB above the theoretical curve, and for the 10^{-6} false alarm rate the non-apodized chip is approximately 6 dB above the theoretical curve. The performance appears to degrade then as a function of false alarm rate with the apodized chip appearing to degrade at a more rapid rate than the non-apodized chip, but no conclusions were reached as to the exact cause of the degradation. If the two figures are overlaid, a degradation of about 2 dB is noted in the curves for the case of a signal occurring at the edge of a bin as opposed to the center of a bin. This degradation was expected for the non-apodized chip from the plot presented in Figure 3-4, however the apodized chip was not expected to exhibit quite as much degradation. Again, no final conclusions were reached as to the apparent discrepancy between the plot of Figure 3-4 for the apodized chip and the 2 dB difference in detection performance for the same chip between center and bin edge signal placement.

Figures 3-6, 3-7 and 3-8 were all taken with an input noise level of 317 mV_{rms} as measured at the output of the 40 kHz 5-pole elliptic low pass filter. A question to be asked is how does the noise floor of the chirp-z transformer itself compare with the incoming noise level. If the noise floor is comparable, then the resulting probability of detection plots will be degraded since they are based on signal-to-noise ratios obtained from measuring the incoming noise power only. Figures 3-9 and 3-10 are probability of detection curves comparing the detection performance for input noise levels of 317 mV_{rms}

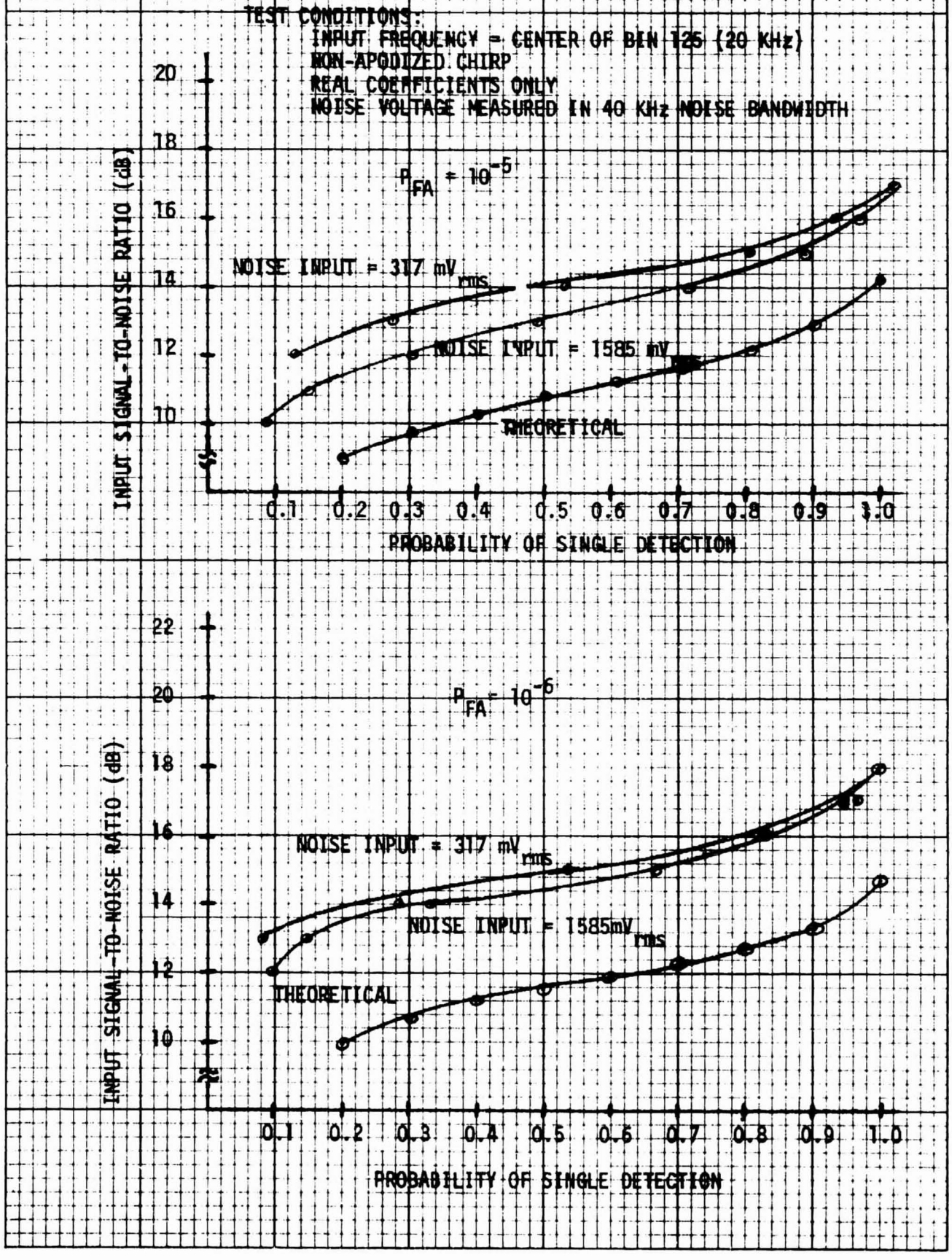


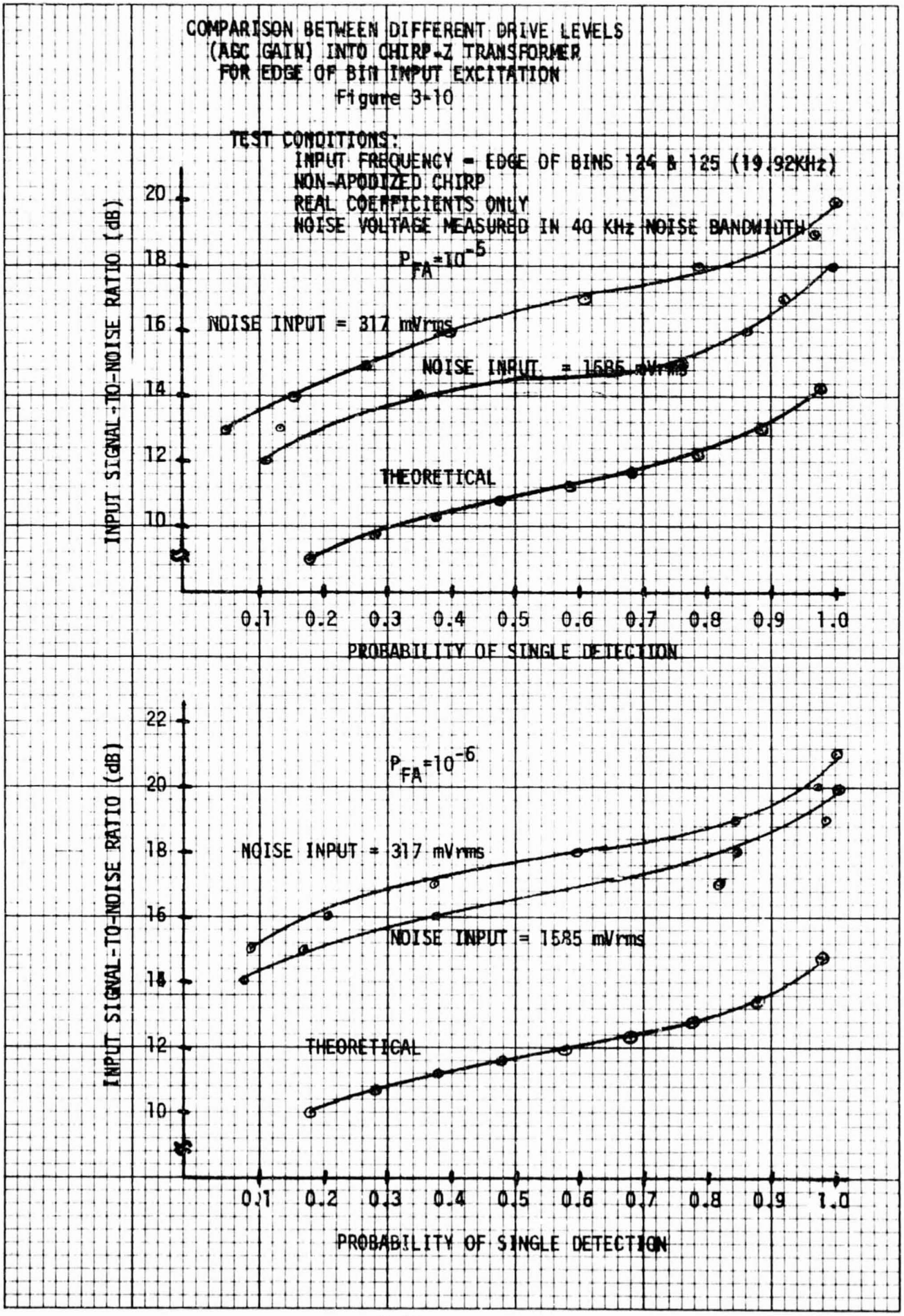

COMPARISON BETWEEN APODIZED AND NON-APODIZED
CHIRP-Z TRANSFORMERS
FOR EDGE OF BIN INPUT EXCITATION
Figure 3-8
TEST CONDITIONS:
INPUT FREQUENCY = EDGE OF BIN 124 & 125 (19.92 KHz)
INPUT NOISE = 317 mV rms (40 KHz NOISE BANDWIDTH)
REAL COEFFICIENTS
$P_{FA}=10^{-5}$
NON-APODIZED CHIRP
APODIZED CHIRP
THEORETICAL
INPUT SIGNAL-TO-NOISE RATIO (dB)
20
18
16
14
12
10
0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0
PROBABILITY OF SINGLE DETECTION
$P_{FA}=10^{-6}$
APODIZED CHIRP
NON-APODIZED CHIRP
THEORETICAL
INPUT SIGNAL-TO-NOISE RATIO (dB)
22
20
18
16
14
12
10
0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0
PROBABILITY OF SINGLE DETECTION

C-2

COMPARISON BETWEEN DIFFERENT DRIVE LEVELS
(AGC GAIN) INTO CHIRP-Z TRANSFORMER
FOR CENTER OF BIN EXCITATION

Figure 3-9




COMPARISON BETWEEN DIFFERENT DRIVE LEVELS
(AGC GAIN) INTO CHIRP-Z TRANSFORMER
FOR EDGE OF BIN INPUT EXCITATION
Figure 3-10
TEST CONDITIONS:
INPUT FREQUENCY = EDGE OF BINS 124 & 125 (19.92KHz)
NON-APODIZED CHIRP
REAL COEFFICIENTS ONLY
NOISE VOLTAGE MEASURED IN 40 KHz NOISE BANDWIDTH
$P_{FA}=10^{-5}$
NOISE INPUT = 317 mVrms
NOISE INPUT = 1585 mVrms
THEORETICAL
INPUT SIGNAL-TO-NOISE RATIO (dB)
20
18
16
14
12
10
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
PROBABILITY OF SINGLE DETECTION
$P_{FA}=10^{-6}$
NOISE INPUT = 317 mVrms
NOISE INPUT = 1585 mVrms
THEORETICAL
INPUT SIGNAL-TO-NOISE RATIO (dB)
22
20
18
16
14
12
10
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
PROBABILITY OF SINGLE DETECTION

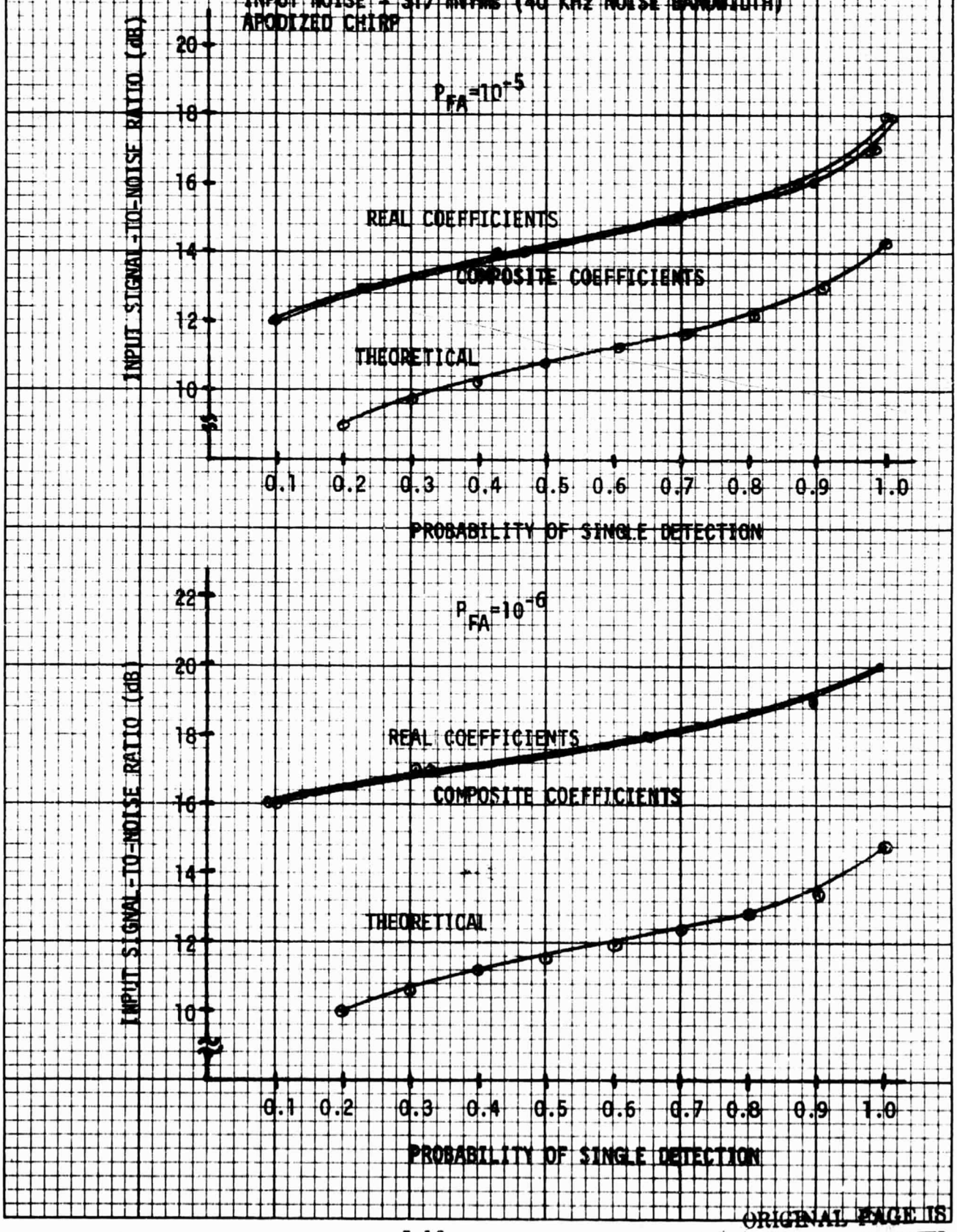
and 1585 mV_{rms} as measured in 40 kHz. Figure 3-9 shows the probability of detection plots for a signal located at the center of one of the transformer's frequency bins and Figure 3-10 shows the same plots for a signal located exactly at the edge of two adjacent frequency bins. To maintain a false alarm rate of 10^{-5} or 10^{-6} when switching between the two noise levels, it is necessary to re-adjust the threshold setting on the threshold detector. Figures 3-9 and 3-10 show approximately a 1 to 2 dB improvement in performance when the noise level is increased to the higher level, indicating that the noise floor of the chirp-z transformer would measure between 165 mV_{rms} and 250 mV_{rms} in a 40 kHz noise bandwidth. This finding is not too surprising since the breadboard ADC/PL layout was far from ideal from the standpoint of low noise packaging. With a noise level of 1585 mV_{rms}, which in effect swamps out the noise floor of the chirp-z transformer, and centering the incoming signal at the midpoint of a frequency bin, the difference between theoretical and measured performance is only 2 dB for a false alarm rate of 10^{-5} and 3 dB for a false alarm rate of 10^{-6} Under the exact same conditions, except with the signal at the edge of two adjacent frequency bins, the difference between theoretical and measured performance is about 4 dB for a false alarm rate of 10^{-5} and 5 dB for a false alarm rate of 10^{-6} - again with the placement of a signal at the edge of a frequency bin exhibiting a 2 dB degradation over the placement of a signal in the center of a frequency bin. It is also noted that the change in noise level from 317 mV_{rms} to 1585 mV_{rms} represents a dynamic range of 14 dB.

Figure 3-4 and 3-6 through 3-10 have all been probability of detection plots based on using or processing only the real spectral coefficients in the detection process. Figures 3-11 and 3-12 are probability of detection plots comparing the difference in detection performance between utilizing only the real coefficients and using both real and imaginary coefficients in the detection process. Figure 3-11 shows the probability of detection plots for an incoming signal located in frequency at the center of one of the frequency bins of the chirp-z transformer and Figure 3-12 shows the same plots for an incoming signal located on the edge of two adjacent frequency bins. To maintain a constant false alarm rate of 10^{-5} or 10^{-6} it was necessary to adjust the threshold level of the threshold detector when switching between processing only real coefficients and processing both real and imaginary coefficients. When processing only real coefficients, each spectral sweep or spectral transformation in the chirp-z transformer results in 250 spectral coefficients being processed in the search detector. However, when processing both real and imaginary coefficients a total of 500 coefficients are processed by the search detector

COMPARISON BETEEN REAL AND COMPOSITE CHIRP-Z TRANSFORMER COEFFICIENTS FOR CENTER OF BIN EXCITATION

Figure 3-11

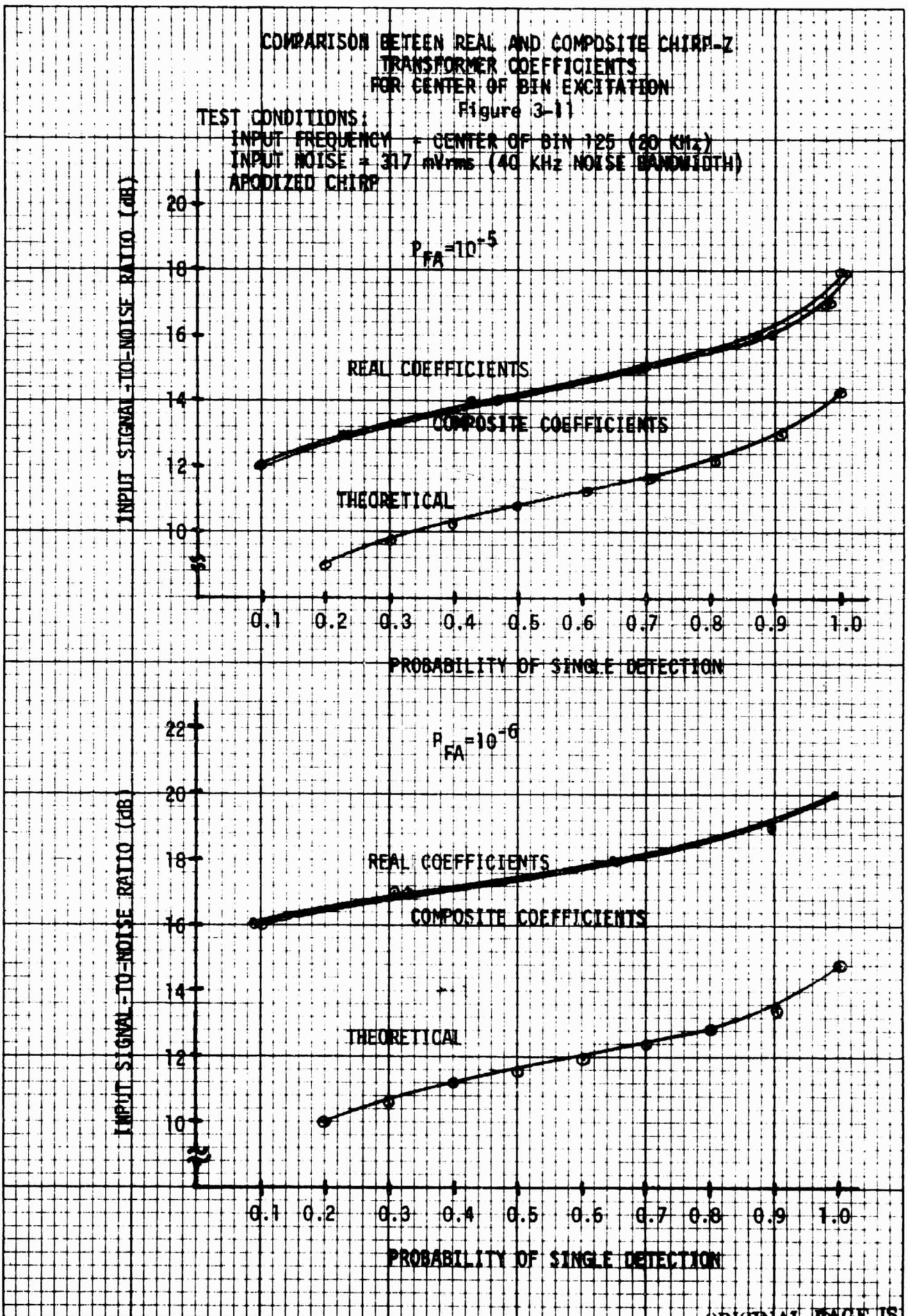
TEST CONDITIONS:
INPUT FREQUENCY = CENTER OF BIN 125 (20 KHz)
INPUT NOISE = 317 mVrms (40 KHz NOISE BANDWIDTH)
APODIZED CHIRP

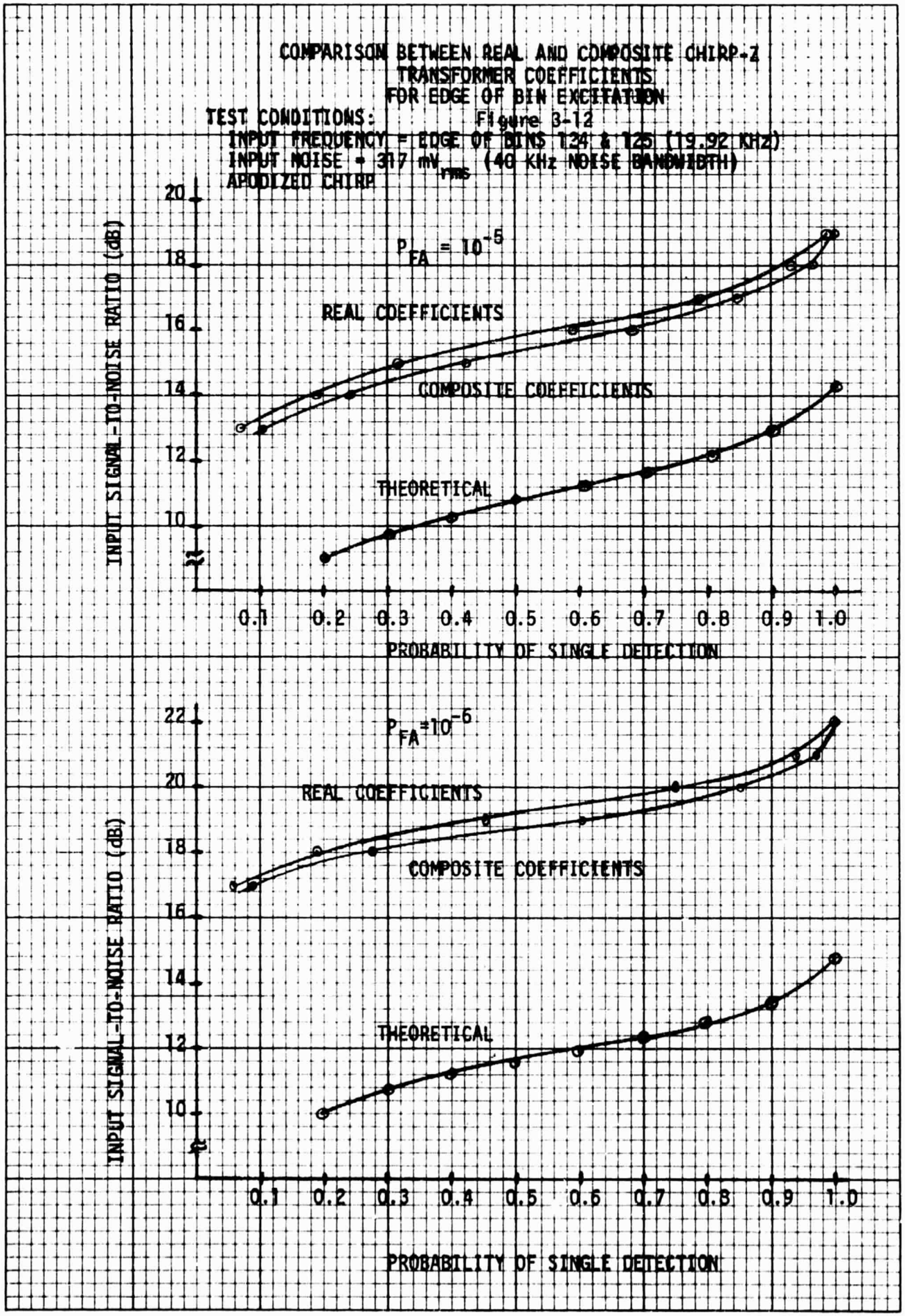


COMPARISON BETEEN REAL AND COMPOSITE CHIRP-Z TRANSFORMER COEFFICIENTS FOR CENTER OF BIN EXCITATION

Figure 3-11

TEST CONDITIONS:
INPUT FREQUENCY = CENTER OF BIN 125 (20 KHz)
INPUT NOISE = 317 mVrms (40 KHz NOISE BANDWIDTH)
APODIZED CHIRP




COMPARISON BETWEEN REAL AND COMPOSITE CHIRP-Z
TRANSFORMER COEFFICIENTS
FOR EDGE OF BIN EXCITATION
TEST CONDITIONS:
Figure 3-12
INPUT FREQUENCY = EDGE OF BINS 124 & 125 (19.92 KHz)
INPUT NOISE = 317 mV rms (40 KHz NOISE BANDWIDTH)
APODIZED CHIRP
$P_{FA} = 10^{-5}$
REAL COEFFICIENTS
COMPOSITE COEFFICIENTS
THEORETICAL
INPUT SIGNAL-TO-NOISE RATIO (dB)
PROBABILITY OF SINGLE DETECTION
$P_{FA}=10^{-6}$
REAL COEFFICIENTS
COMPOSITE COEFFICIENTS
THEORETICAL
INPUT SIGNAL-TO-NOISE RATIO (dB)
PROBABILITY OF SINGLE DETECTION

during each spectral sweep. It is expected then that the false alarm rate would increase upon switching from real only to both real and imaginary coefficients - and the test results showed that the false alarm rate approximately doubled. It was necessary then to adjust the threshold level upon switching coefficient processing modes. Another consideration in plotting probability of detection curves for the case of utilizing both the real and imaginary coefficients is that a given input signal will result in two coefficients exceeding threshold - an imaginary coefficient and a real coefficient. For a probability of detection of 100%, observing threshold exceedances for 1000 spectral sweeps while utilizing both coefficients would result in 2000 detections or threshold exceedances whereas using only the real coefficients would result in only 1000 threshold exceedances. The probability of detection when using both real and imaginary coefficients is determined then by dividing the number of threshold exceedances by twice the number of spectral sweeps.

Figures 3-11 and 3-12 show hardly any discernable difference between using only real or both real and imaginary coefficients in the detection process. This is a very key finding since it effectively indicates that the real and imaginary coefficients are statistically independent - which is not totally surprising since the sliding chirp-z transform implementation involves inputting a new data point for each coefficient output. This means that for each spectral sweep the search detector has two tries at detecting the presence of an incoming signal. The probability of detecting the signal then in one spectral sweep is, assuming the real and imaginary coefficients to be statistically independent.

$$P_{D_T} = 1 - (1-P_D)(1-P_D)$$

Probability of Missing Imaginary Coefficient

Probability of Missing Real Coefficient

$$P_{D_T} = 2P_D - P_D^2$$

where P_{D_T} = probability of detecting the presence of a signal in one spectral sweep

P_D = probability of detecting the presence of a signal for a given coefficient - real or imaginary

Figure 3-13 compares, for a signal positioned in the center of a frequency bin, the probability of detection for real coefficients only and the probability of detection for both real and imaginary coefficients using the above equation. In comparing Figures 3-11 and 3-13 it is noted that the use of both coefficients results in approximately a 1 dB improvement in detection per spectral sweep over that obtained using only the real coefficients.

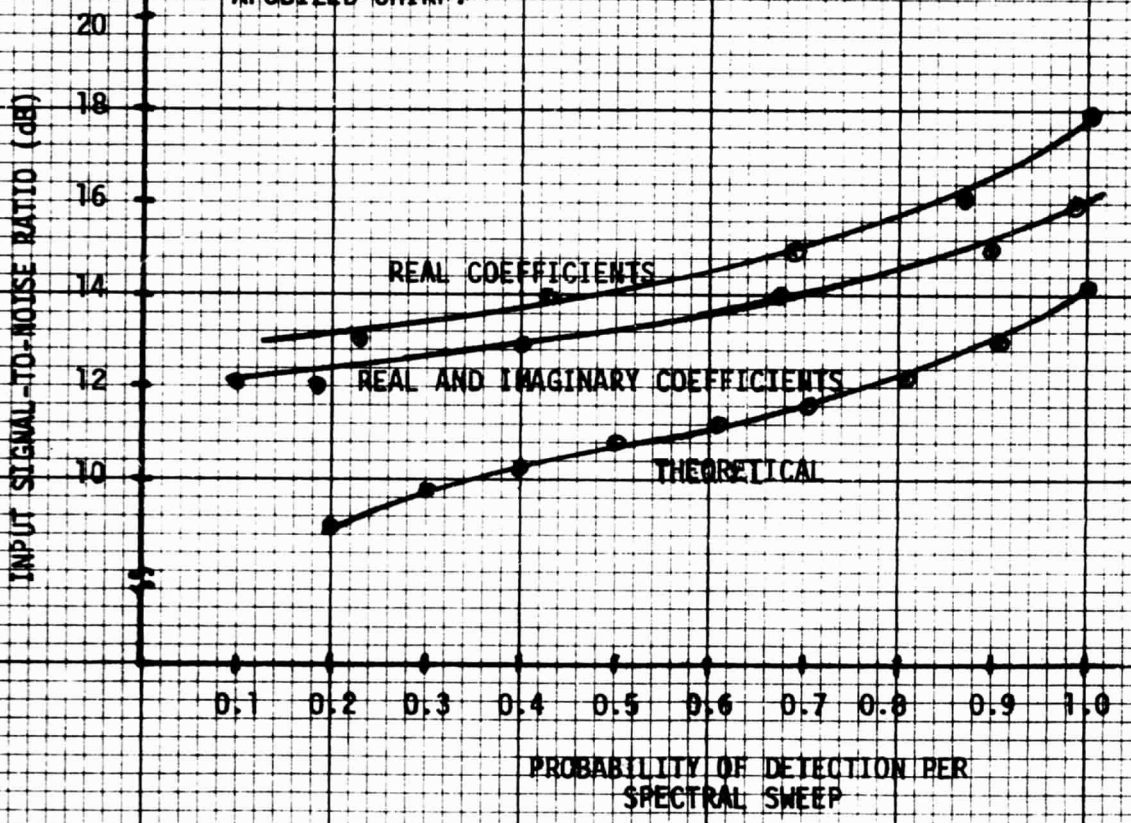
Figure 3-14 shows the performance of the chirp-z transformer, as compared to the RAMS search unit, across a 10-40 kHz search band. The test was conducted for both types of search units by setting the incoming signal power level to that level required to give a probability of detection of approximately 80%. The frequency of the incoming signal was set to 10kHz for the initial signal power adjustment. The choice of an 80 percent probability of detection was made to sensitize the plot to changes in the effective incoming signal power as the signal is varied in frequency across a 10-40 kHz search band. By sensitizing the probability of detection plot, any degradation or problem spots in the detection process as a function of frequency can be easily found. It is noted that the RAMS search unit displayed a degradation in detection performance as the signal increased in frequency above 32 kHz. This phenomena was traced to the delta modulator which does display increasing quantization noise as the incoming signal increases in frequency. The chirp-z transformer, by comparison, displays a relatively flat probability of detection characteristic as a function of signal frequency. The chirp-z transformer does show a drop in performance at the upper edge of the 10-40 kHz search band due to the rolloff of the 5-pole elliptic low pass filter.

A problem was noted in taking the probability of detection data, both for the apodized and non-apodized chips, in that the threshold point did not appear to be a hard threshold. That is, if a strong signal is input into the chirp-z transformer of sufficient signal strength to be well above the noise floor, and the threshold level is set well above the noise floor, the threshold exceedance point should be well defined. As the signal level is increased there should be a threshold point such that just below the threshold point no exceedances are observed and just above the threshold point a 100% probability of detection is observed. However, the chirp-z transformer did not exhibit a solid threshold point, but rather appeared to wander or "warble" about an approximate 3 dB range in threshold. Figure 3-15 shows a plot of the warbling effect. The plot is developed by inputting a strong signal, setting the threshold level well above the noise floor, and plotting the probability of detection

COMPARISON IN THE PROBABILITY OF DETECTION PER SPECTRAL SWEEP REALIZABLE USING ONLY REAL OR BOTH REAL AND IMAGINARY CHIRP-Z SPECTRAL COEFFICIENTS

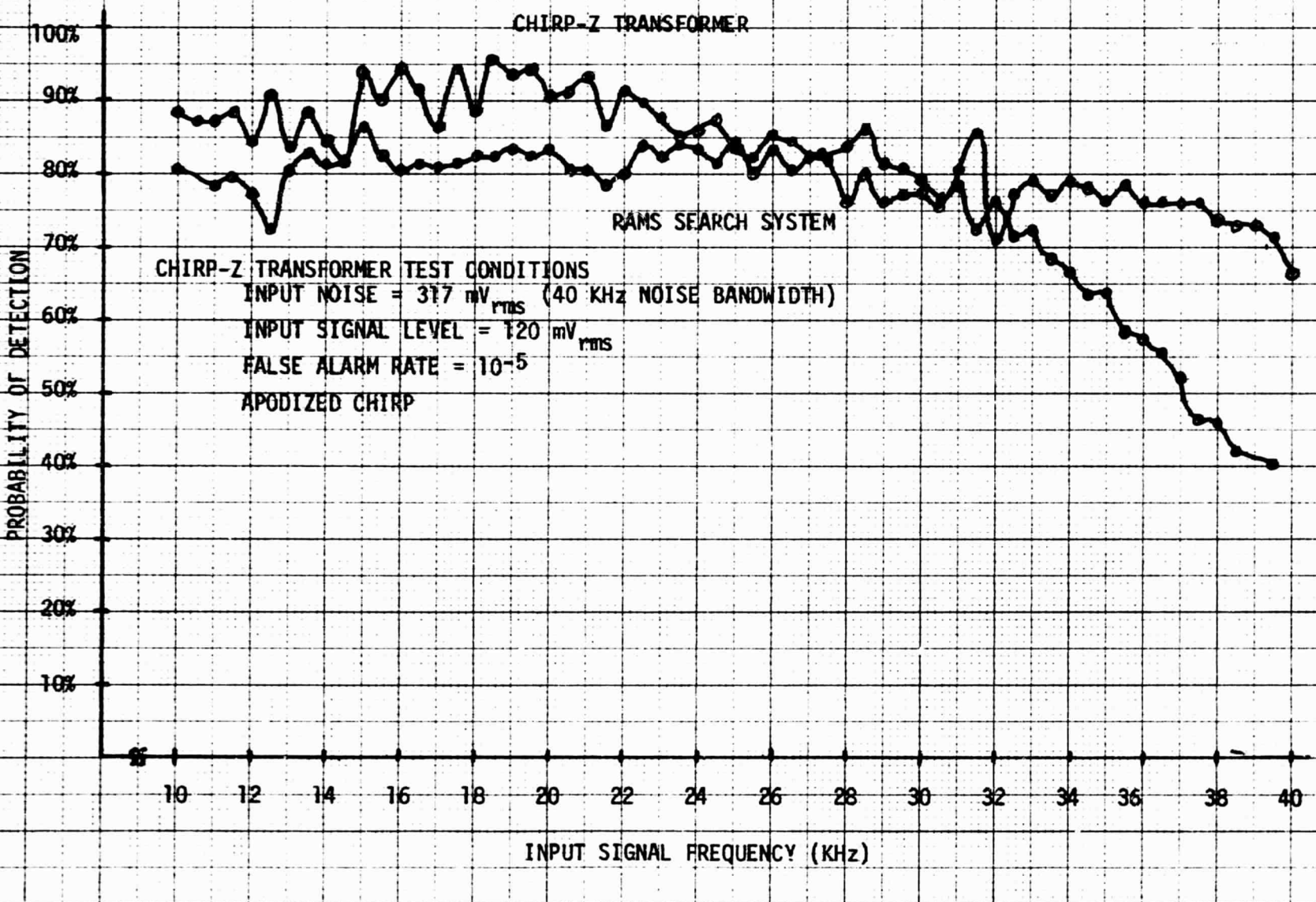
Figure 3-13

TEST CONDITIONS:
INPUT FREQUENCY = CENTER OF BIN 125 (20 KHz)
INPUT NOISE = 317 mV_{rms} (40 KHz NOISE BANDWIDTH)
APODIZED CHIRP.



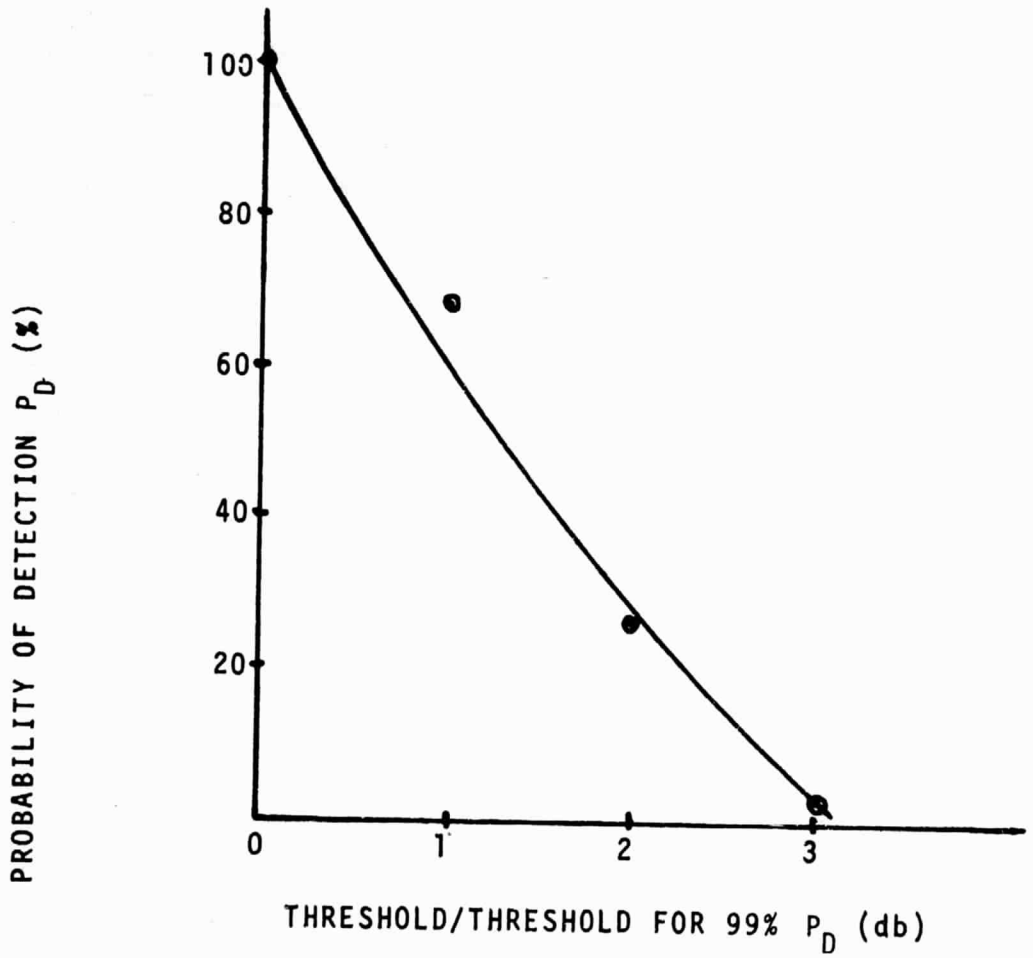
PROBABILITY OF DETECTION
VS
INPUT FREQUENCY

Figure 3-14



SOFT THRESHOLD PHENOMENON (WARBLING)
IN CHIRP-Z TRANSFORMER

Figure 3-15



as a function of the threshold setting as normalized to the threshold setting for a 100% probability of detection. As the threshold is adjusted below the setting required for a 100% probability of detection, the probability of detection should rapidly drop to zero. However, the plot in Figure 3-15 shows a graceful degradation in the probability of detection as the threshold is adjusted below the 100% probability of detection threshold point.

The exact cause of this warbling effect is thought to be in the peripheral circuitry supporting the CCD chip. Filtering is accomplished utilizing CCD technology by partitioning the sampled charge packet in each cell via split electrodes (tap weight multiplication) and then summing the partitioned charges from all cells. The summation of the partitioned charges is accomplished by a differential current integrator. If the two differential current integrator ports are unbalanced with respect to each other, the magnitude of the coefficients output will vary as the phase of the input signal varies with respect to the start of a new chirp sweep. If the phase, as measured at the start of a chirp sweep, changes from transformation to transformation, the weighting between the charge packet summed at the positive port of the differential current integrator and the charge packet summed at the negative port of the integrator will change. These changes will change the magnitude of the coefficients output. This phenomenon was quite noticeable during the probability of detection tests in that the incoming signal frequency could be adjusted in frequency to maximize the warbling rate, or the rate in which the magnitude changes, or to totally remove any warbling effect at all. The changing of the incoming signal alters the rate of the phase change at the start of a chirp sweep, and signal frequencies could be found where the phase of the signal at the start of the chirp sweep remained constant thereby eliminating the warbling effect.

Present CCD efforts in the Central Research Laboratory at Texas Instruments include housing the differential current integrator on the CCD chip to allow tighter balancing between the differential lines to be achieved.

B.3 Dynamic Range Measurements

A major concern in evaluating the performance of a search system for an ADC/PL type application is the amount of bin spreading encountered over the incoming signal dynamic range. If the bin spreading becomes severe, causing many frequency bins to exceed threshold when a strong signal is present, it can seriously degrade the overall performance of the ADC/PL system. Bin spreading will reduce the resolution of the search system or the ability of the search system to recognize the presence of two different signals closely spaced in frequency. If, for example, a strong signal can result in

up to ten frequency bins distributed about the center frequency bin to exceed threshold, then a neighboring incoming signal must be at least six frequency bins (960 Hz for the 160 Hz frequency bin size in the breadboard ADC/PL) removed from the strong signal if it is to be distinguished from the strong signal. If the neighboring signal is also a strong signal then the frequency separation must be even greater to prevent the threshold exceedances from the two signals overlapping in frequency. This need to spread apart adjacent signals for unique detection capability severely degrades the number of platforms that can be serviced since the spectral efficiency of the system is seriously degraded.

Bin spreading also increases the uncertainity in the frequency assignment to the assigned receive channel, which in turn means that the phase lock loop in the receive channel must have a wider acquisition bandwidth in order to pull over to and acquire the signal over the frequency uncertainity band. The wider acquisition bandwidth means the minimum signal strength allowable must be increased to accommodate the enlarged acquisition bandwidth of the receive channel, which means either the transmit power of the data collection platforms must be increased or the field of view that can be accommodated by the receiving equipment must be reduced in size.

Two different phenomina can cause bin spreading - the incoming signal to be detected can be quite broad in its spectral content or the search system itself can cause the bin spreading. Only the latter case will be considered here since the incoming signal is assumed to be a CW tone during the acquisition phase of the signal transmission - which is the preamble portion of the signal message format. In addition, the MSK modulation spectrum will be shown in the following section to be free of any significant sidebands which could cause bin spreading. Section II.F.1.a discusses the principles behind spectral spreading caused by the search system and the use of apodization to minimize the spreading effect. The purpose of this section is to present the bin spreading measured both for the apodized and non-apodized chips.

The photographs in Figure 3-16 depict the nature of the bin spreading phenomina by showing the changes that occur in the levels of the coefficients output by the non-apodized chirp-z transformer as the input signal varies in amplitude from 50 mV_{rms} to 1.5 V_{rms} - representing a dynamic range of 29.5 dB. Assume for instance that the threshold level is set so that a 100% probability of detection is obtained for a signal input of 50 mV_{rms}. It is noted that this signal level results in only that coefficient representing the frequency band containing the signal standing above the noise floor. No noise is input, so the only noise seen by the chirp-z transformer is the noise floor of the

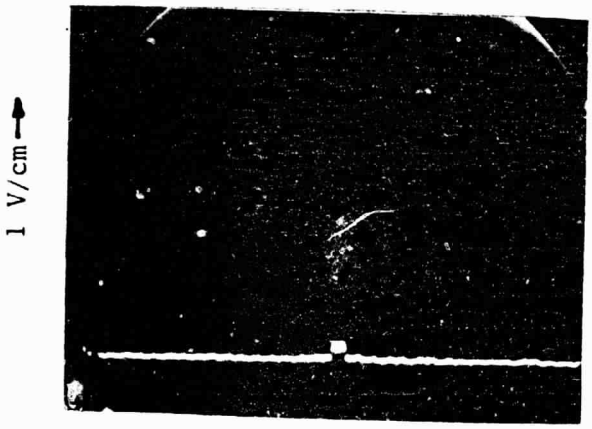
PHOTOGRAPHIC DISPLAY OF BIN SPREADING

vs. SIGNAL STRENGTH

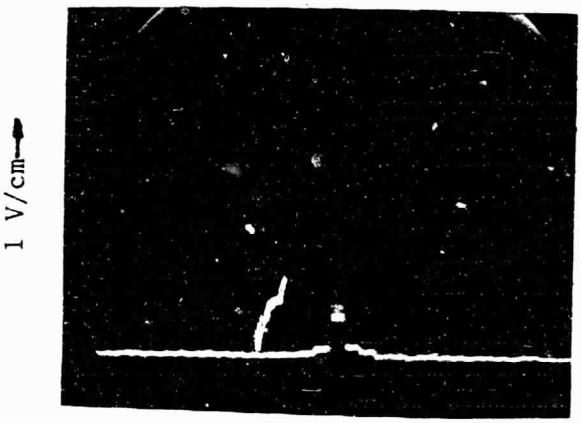
NON-APODIZED CHIRP-Z TRANSFORMER

INPUT FREQUENCY = 19.8 KHz

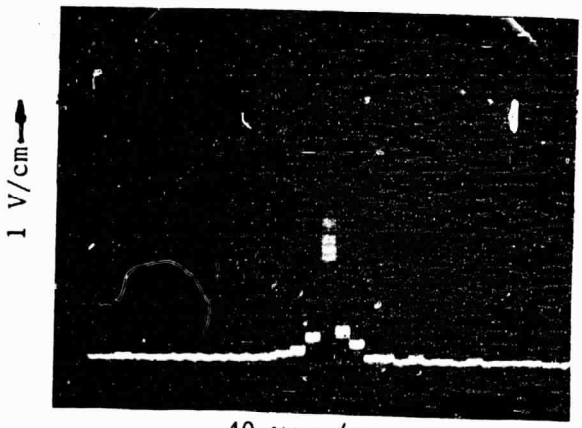
FIGURE 3-16



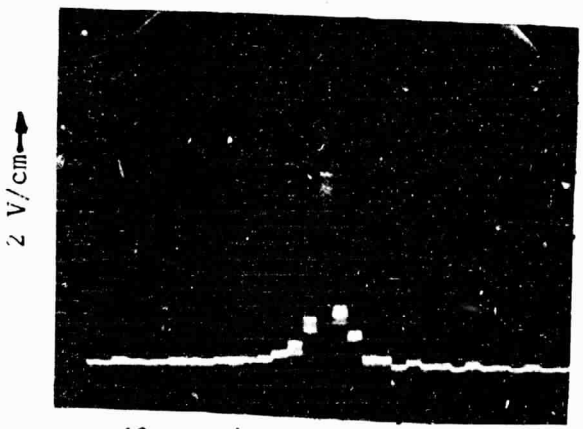
50 mV_{rms} INPUT LEVEL



150 mV_{rms} INPUT LEVEL



500 mV_{rms} INPUT LEVEL



1.5 V_{rms} INPUT LEVEL

transformer itself. When the signal is increased to 150 mV_{rms}, it is noticed that the two adjacent frequency bins on either side of the center frequency bin have grown. These adjacent bins, while not strong enough to give a 100% probability of detection, will result in some threshold exceedances occurring. When the signal level is increased to 500 mV_{rms}, the two adjacent frequency bins on either side of the center frequency bin have grown in magnitude such that they will now show a 100% probability of detection. It is also noted that frequency bins beyond these will begin to show a finite number of threshold exceedances. Finally, when the signal level is increased to 1.5 V_{rms}, the bin spreading becomes quite noticeable. Remembering that the threshold level is adjusted to give a 100% probability of detection for the 50 mV_{rms} signal level, it is quite easy to visualize at least four frequency bins on either side of the center frequency bin giving a 100% probability of detection. It is also obvious that frequency bins as far away as ten bins from the center bin will show finite probability of detection readings.

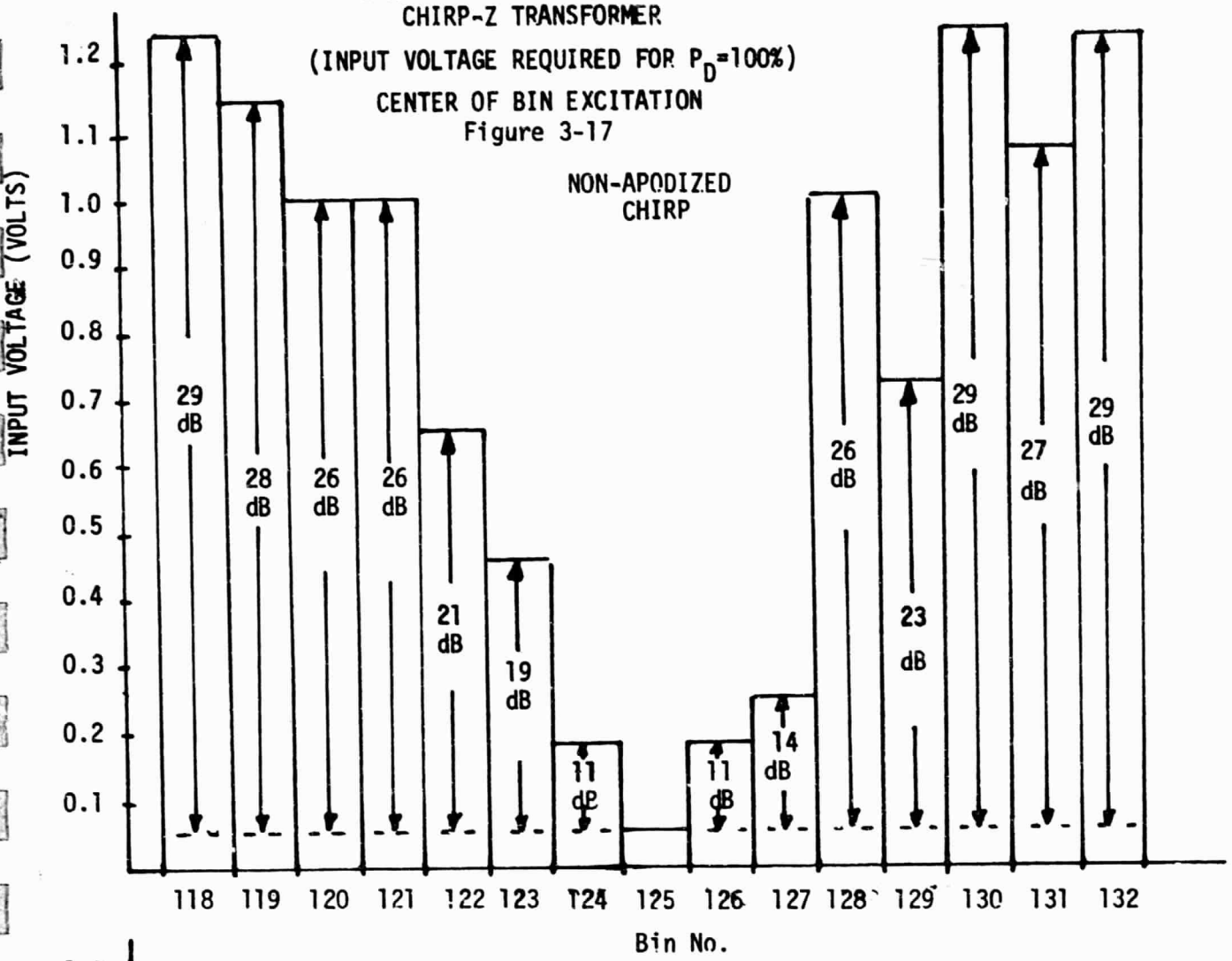
Figures 3-17 and 3-18 show the bin spreading characteristics in bar chart format of both the apodized and non-apodized chips for both bin center (Figure 3-17) and bin edge (Figure 3-18) signal excitation. The method used to take the measurements is the exact technique described above. No noise is input and the threshold level is adjusted to give a false alarm rate of approximately 10^{-6} on internal chirp-z transformer noise. The input signal, located in frequency either at the center or the edge of a frequency bin, is then adjusted in signal level until a 100% probability of detection is just reached either in the center bin or the two adjacent bins. This input signal level is established as the reference level and represents in effect the minimum level signal that can be reliably detected. The signal level is then increased until a 100% probability of detection is reached in one of the adjacent bins. This signal level marks the height of the bar in Figures 3-17 and 3-18 for that adjacent bin which has reached the 100% probability of detection mark. For center bin signal excitation Figure 3-17 shows that for the non-apodized chip, a 30 dB dynamic range will result in up to fifteen frequency bins containing enough spectral energy to give a 100% probability of detection. For the apodized chip, the same 30 dB dynamic range will result in only four frequency bins containing enough spectral energy to give a 100% probability of detection. For the edge of bin signal excitation, the 30 dB dynamic range results in thirteen frequency bins showing a 100% probability of detection for the non-apodized chip while still only four bins for the apodized chip.

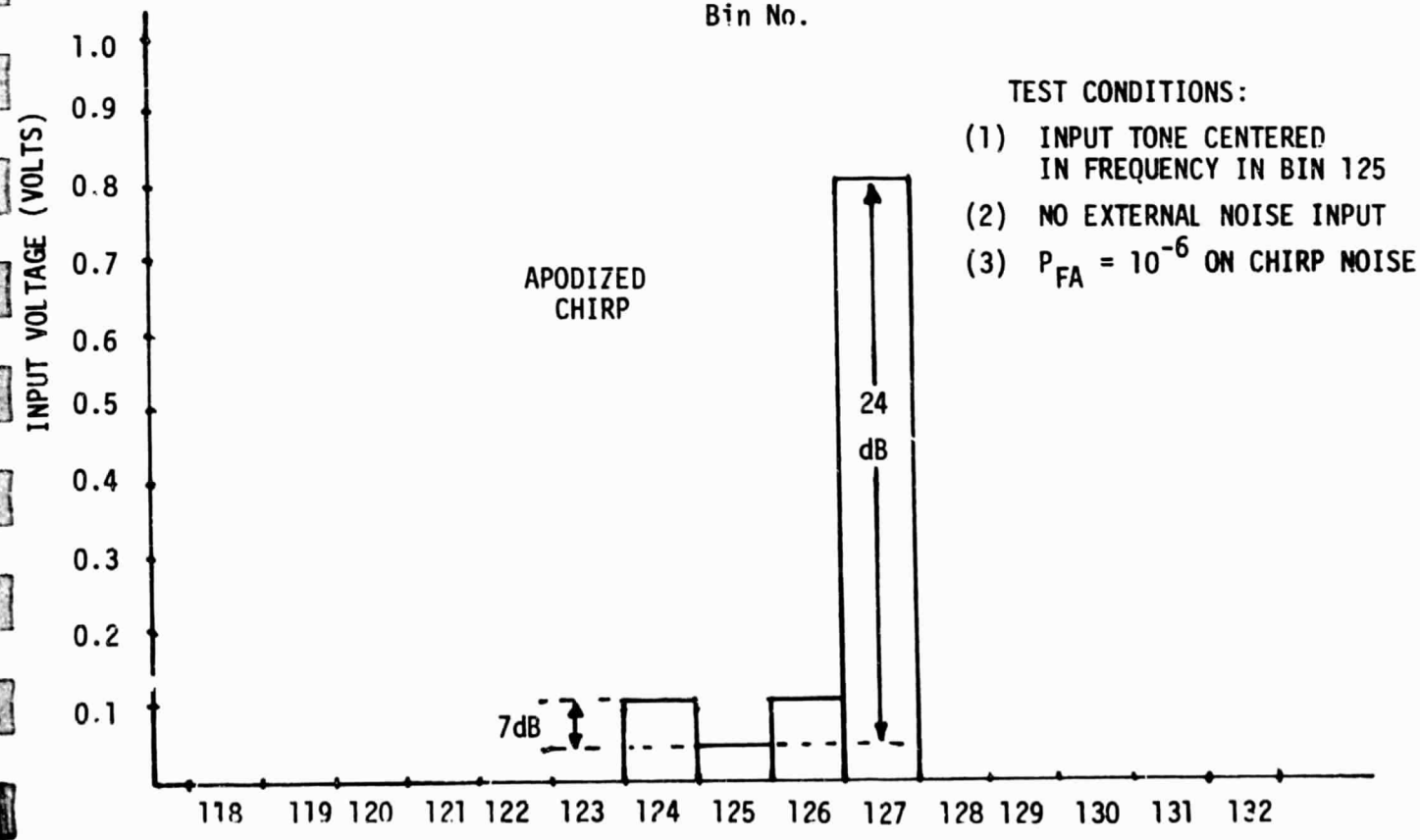
BIN SPREADING CHARACTERISTICS
CHIRP-Z TRANSFORMER

(INPUT VOLTAGE REQUIRED FOR P_D=100%)

CENTER OF BIN EXCITATION

Figure 3-17





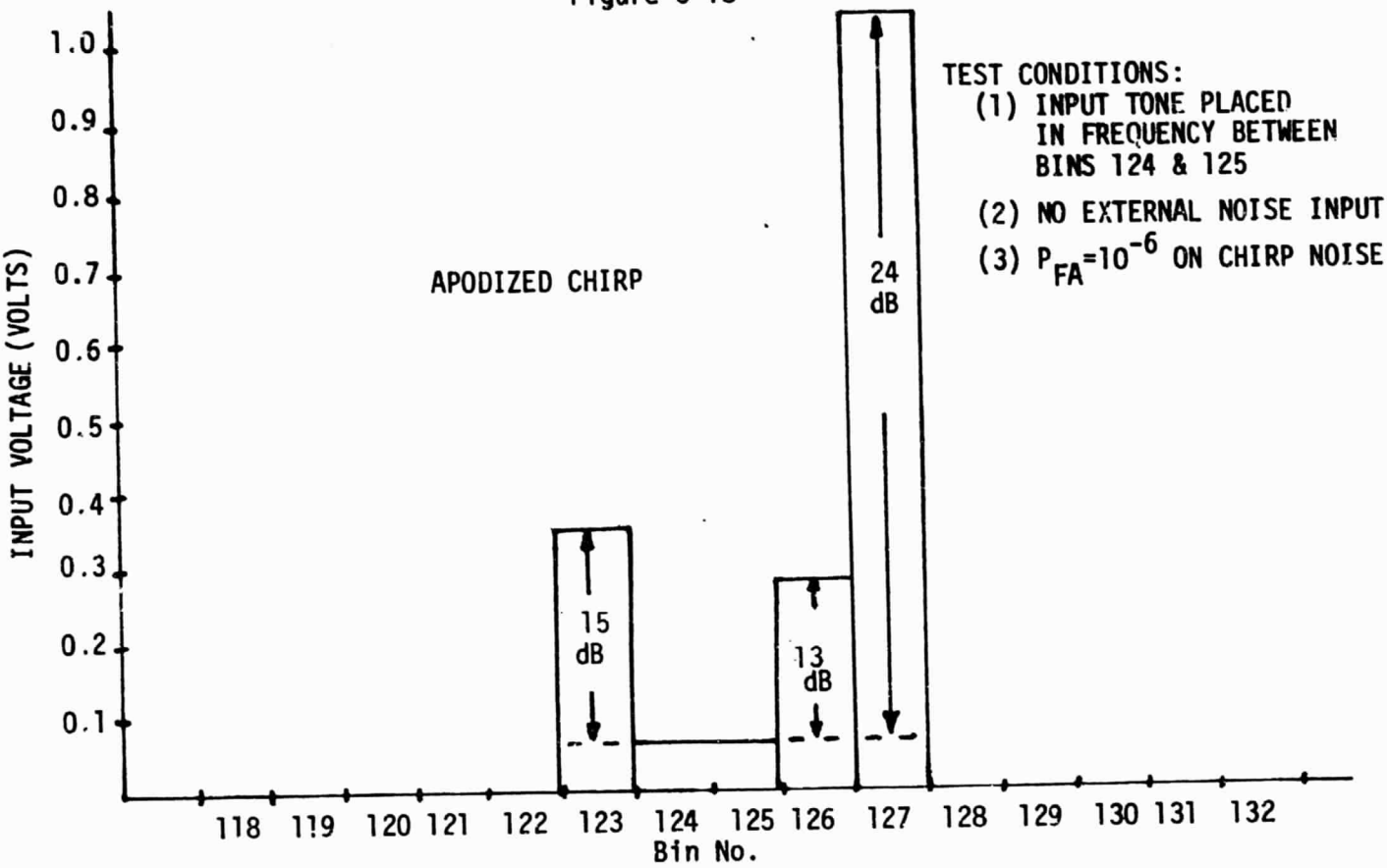
TEST CONDITIONS:

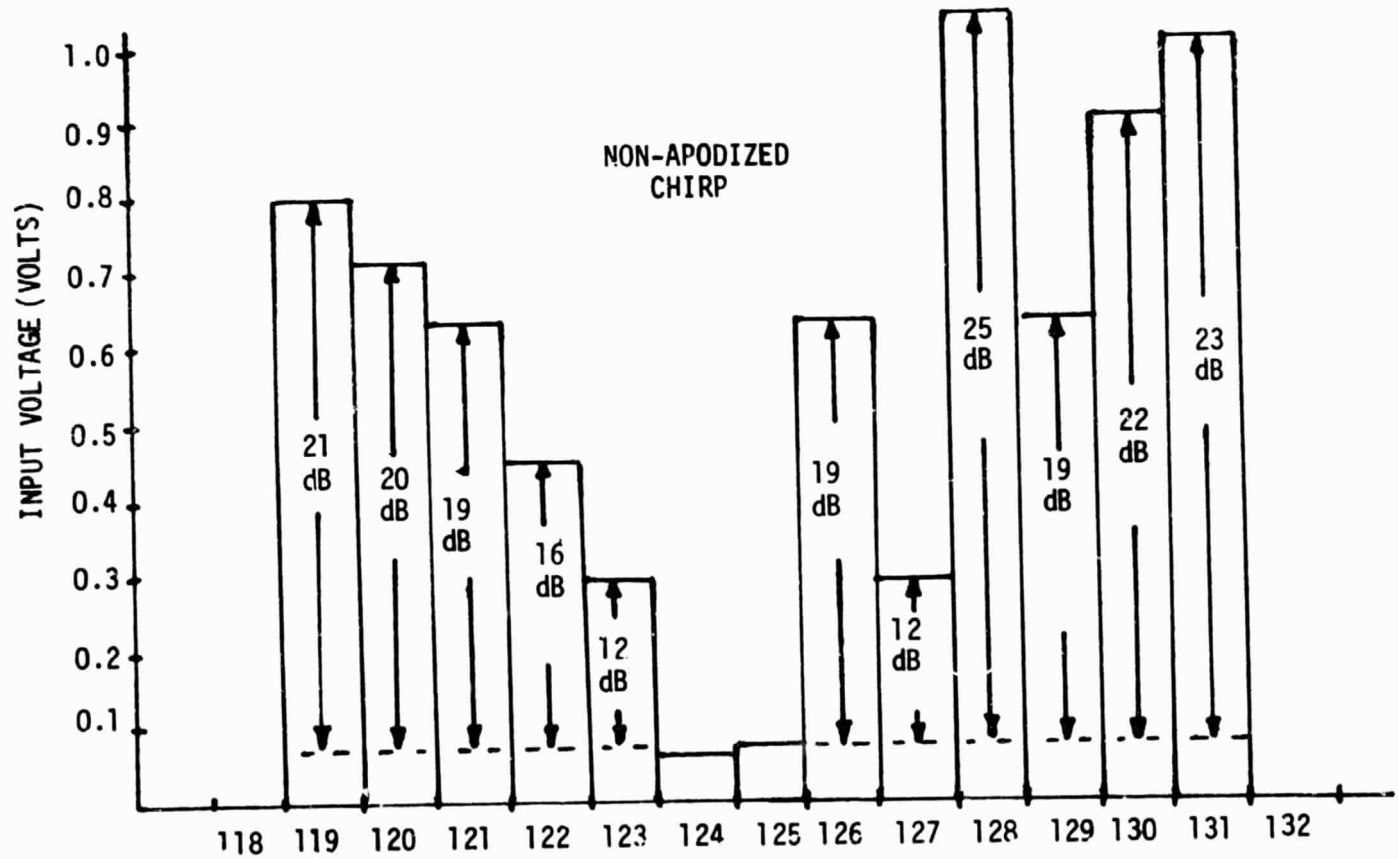
(1) INPUT TONE CENTERED IN FREQUENCY IN BIN 125

(2) NO EXTERNAL NOISE INPUT

(3) $P_{FA} = 10^{-6}$ ON CHIRP NOISE

BIN SPREADING CHARACTERISTICS
CHIRP-Z TRANSFORMER
(INPUT VOLTAGE REQUIRED FOR P_D=100%)
Figure 3-18





It is clear that the apodized chip is superior. In fact, the bin spreading is so severe in the case of the non-apodized chip as to render it unusable for dynamic range levels above ten to twelve dB - which was the range experienced in the RAMS TWERLE Experiment. Fortunately, the apodized chip exhibits acceptable bin spreading parameters for up to 30 dB dynamic range excursions, and the previous section has shown that little or no penalty is paid in detection performance in using the apodized chip.

B.4 Search Time and Channel Reassignment Time

The search time, or the time required to detect the presence of a signal and assign a receive channel, and the recycle time, or the time required to recycle a receive channel assignment after an assignment to a false alarm, are two additional search unit parameters quite important in assessing the overall performance of the search unit. The spectral search time of the chirp-z transformer is fixed at the reciprocal of the analyzing bandwidth - and is 6.25 milliseconds for the ADC/PL chirp-z transformer. The time required to detect the presence of a signal is then simply the reciprocal of the analyzing bandwidth, assuming the incoming signal strength is adequate to give a high probability of detection. If the signal strength is not adequate to provide a high probability of detection, the time required to detect the presence of a signal becomes a question of probabilities - if the signal is not detected in one spectral search period, what is the probability that the signal will be detected in two spectral search periods, or three, or four, etc. The time to detect then becomes a direct function of the probability of detection for low level or weak signals, and can be obtained by applying probabilistic equations to the probability of detection test results.

The time required to recycle a channel assignment after a false alarm is a direct function of the complexity of the channel assignment logic following the search unit rather than the search technique itself. Two natural checkpoints are available for determining whether or not the assignment made by the search unit is being properly carried out. Very shortly after making an assignment, a check can be made as to whether or not the assigned receive channel has locked to or acquired the incoming signal. The time that must be allocated between assigning the phase lock loop and determining whether or not the loop has acquired lock is a function of the time required for the loop to acquire lock and the time required for the lock condition to be recognized. Generally the latter time is much longer than the former loop acquisition time. The lock indication is generally implemented with a quadrature or auxiliary phase detector

followed by a smoothing filter to minimize false lock indications due to noise. In the Random Access Measurement System (RAMS), it was determined that the bandwidth of the smoothing filter should be approximately one half the acquisition noise bandwidth of the loop to give an effective tradeoff between time to detect lock and noise induced false lock indications. The time delay t_D between assigning a receive channel to a detected signal and testing the assigned channel for a lock condition is

$$t_D \cong \frac{1}{W_n} + \frac{2.2}{W_{3dB}}$$

where W_n = loop acquisition bandwidth natural frequency

f_{3dB} = smoothing filter bandwidth = $\frac{W_n}{2}$

$$T_D \cong \frac{5.4}{W_n}$$

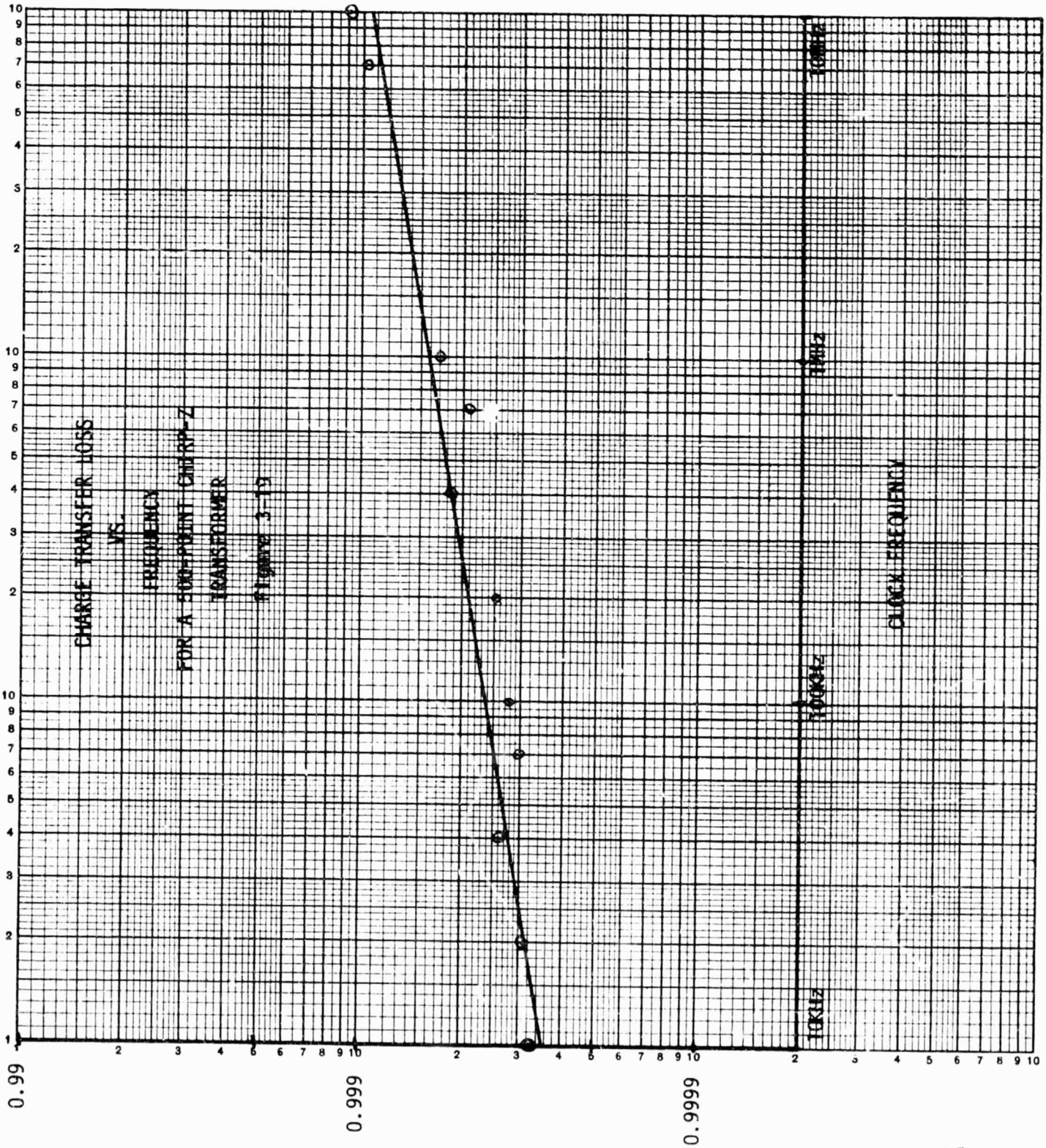
The minimum recycle time then is approximately $5/W_n$. Another checkpoint for determining whether or not the receive channel is demodulating a valid data collection transmission is whether or not the frame synchronization code, which is common to all data collection transmissions, has been received. The time delay required between the assignment of a channel and the verification of frame sync reception depends on the message format and the data rate. Experience on the RAMS system showed that most false alarms were caught by the "in-lock" check, with the bit synchronization code check serving to reject signals to weak in signal strength to provide adequate demodulation. The average recycle time then for false alarms is approximately $5/W_n$.

B.5 Temperature Considerations of CCD Devices

A major concern in considering the use of a chirp-z transformer search system in an ADC/PL system is whether or not the chirp-z transformer can be qualified to space flight specifications. Specifically, the question is whether or not the charge-coupled device, which is the heart of the chirp-z transformer, can meet the rigid requirements for space usage. Charge-coupled devices, strictly speaking, are no more than MOS devices which store charge packets in the depletion regions formed under biased electrodes. These charge packets can be transferred between successive electrode locations by applying the proper clocking waveforms to the electrodes. Since the quantity of charge which can be stored under an electrode can vary between a few hundred to a few million electrons, the devices are truly sampled-data devices.

There are two major parameters to be monitored in characterizing a charge-coupled-device - the charge transfer efficiency and the dark current or leakage current. In charge-coupled-devices, the charge or signal transfer mechanism is the successive formation of potential wells or depletion regions down the device channel. Via appropriate clocking of the CCD electrodes, the input signal is sampled and moved down the channel from well to well in the form of charge packets proportional to the input signal at each time-sampled point. Unfortunately, the charge is not completely transferred from well to well due to the presence of surface states at the boundaries of the silicon substrate and the gating electrodes. These surface states trap a portion of the signal charge during a transfer process which results in a charge transfer inefficiency as the signal charge packets are clocked along the CCD channel. The dark current phenomenon is a result of the wells attempting to reach an equilibrium condition. In an attempt to reach an equilibrium condition (full potential well), minority carriers are generated in the depletion regions and the potential wells tend to fill with those minority carriers as well as the signal charge packets. The signal charge packets are thus degraded by the minority carriers which "leak" into the wells, and this degrading mechanism is referred to as dark or leakage current.

Charge transfer efficiency is highly dependent on the geometry utilized to construct the CCD channel and the frequency of the transfer clocks. In fact, tests have shown that geometry and clock frequency are virtually the only viable parameters as temperature and other environmental tests have altered little the charge transfer efficiency as measured at room temperature. The effect of charge transfer loss upon transversal filter operation is principally one of broadening the correlation peak and slightly degrading the amplitude of the correlation peak. The 500 stage CCD filter used on the ADC/PL breadboard is of a particularly sensitive geometry as regards charge transfer efficiency since in order to get the length of 500 onto the substrate it was necessary to "turn corners" to establish filter rows upon the substrate. Tests have shown that the major degradation in the charge transfer efficiency is in the inefficiency incurred at the "corner-turning" diffusions. On straight serial type CCD diffusions the charge transfer efficiency typically ranges from .9995 to .9999, whereas on the CCD devices requiring "corner-turning" diffusions the transfer efficiency typically runs from .9995 to .9990. Figure 3-19 shows a plot of the frequency dependence of a 500 point chirp-z transformer as measured on a device identical to that utilized on the ADC/PL breadboard. The ADC/PL breadboard chirp-z transformer was clocked at a rate of 640 kHz, which, as noted



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OF POOR QUALITY

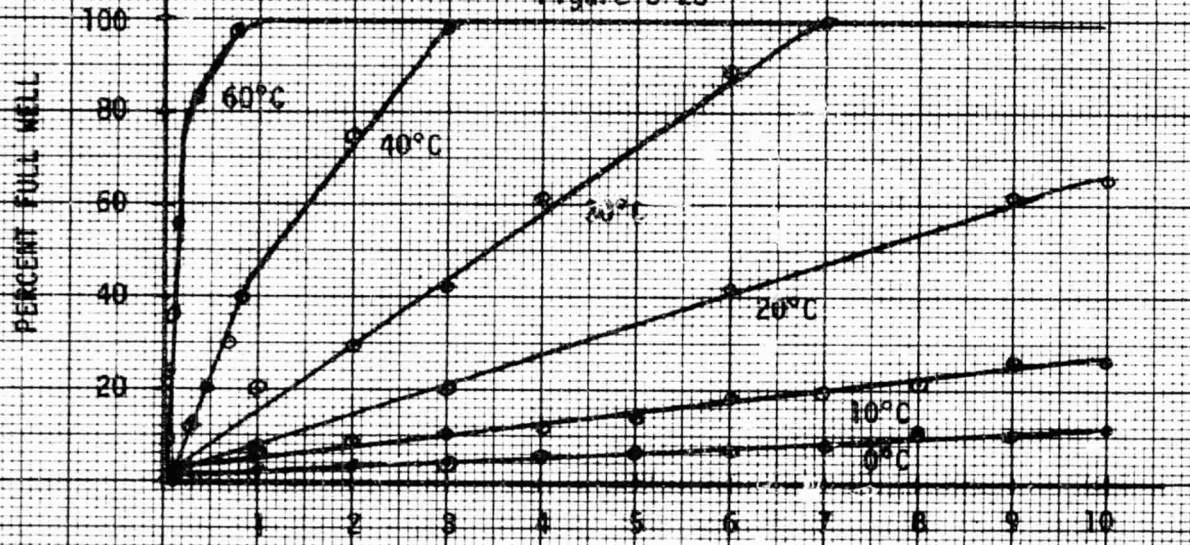
in Figure 3-19, should yield a charge transfer efficiency of approximately 0.9992.

The temperature dependent parameter of the chirp-z transformer is the leakage or dark current. Figure 3-20 shows the integrated leakage current as a function of storage time for a 500 element chirp-z transformer identical to to that used on the ADC/PL breadboard. It can be seen that as the ambient temperature of the chirp-z transformer increases, the leakage current dramatically increases. The effects of leakage current on the performance of the chirp-z transformer is that it raises the noise floor and degrades the performance of the transformer in the presence of low level signals. This also reduces the dynamic range of the device since there is an upper limit on the allowable signal strength because of the limit on the maximum amount of charge that can be stored in the depletion regions of the device. For example, if the total integrated leakage current resulted in a 25-percent full well contribution at the output of the transversal filter, and the input is biased at the 50-percent full well level (which is the common operating point), the filter could only accommodate a 25-percent full well output signal peak swing. This reduces the maximum signal swing by 50-percent, or approximately 6 dB.

Unfortunately, the data presented in Figure 3-20 is not too applicable to the chirp-z transformer used in the ADC/PL breadboard. The ADC/PL breadboard transformer uses a 320 Hz analyzing bandwidth, which requires an integration time of 3.125 milliseconds. It is not clear from Figure 3-20 what percent level of leakage current could be expected at, say, 60^{o}C for a storage time of 3.125 milliseconds - except that it should be well below the 10-percent full well level. Also, it is not clear from Figure 3-20 how to extrapolate what percent level of leakage current could be expected at ambient temperature conditions higher than 60^{o}C. Data more suited to the parameters of the ADC/PL application, and higher temperature data as well, are simply not available at the present time. It is clear from Figure 3-20 that analyzing bandwidths much narrower than 100 Hz could be severely limited by dark current restrictions.

Means are continually being sought at Texas Instruments to reduce the leakage or dark current. Driving factors other than potential improvements in transversal filter operation serve to stimulate the search to reduce the dark current in CCD devices. One very important such factor is the large scale dynamic MOS digital memory market where refresh cycle requirements (which are controlled by the amount of dark current encountered) are highly competitive. Although no single program has been identified which will provide the data

INTEGRATED LEAKAGE CURRENT
VS.
STORAGE TIME
500-CELL TRANSVERSAL FILTER
Figure 3-20



required to demonstrate the ability to qualify the chirp-z transformer for space flight use, the amount of manpower and effort being presently expended on dark current reduction will yield the data required in the near future.

C. MSK NON-COHERENT DEMODULATOR TEST RESULTS

The specific parameters to be tested in the non-coherent MSK demodulator are:

(a) Bit error rate vs. E/N_o for MSK modulation

(b) Bit error rate vs. E/N_o for phase coherent FSK modulation

(c) Performance comparison of three different MSK modulators - digital modulator, varactor phase shift modulator, and VCXO modulator

(d) Performance comparison between linear and non-linear transmission of MSK modulation

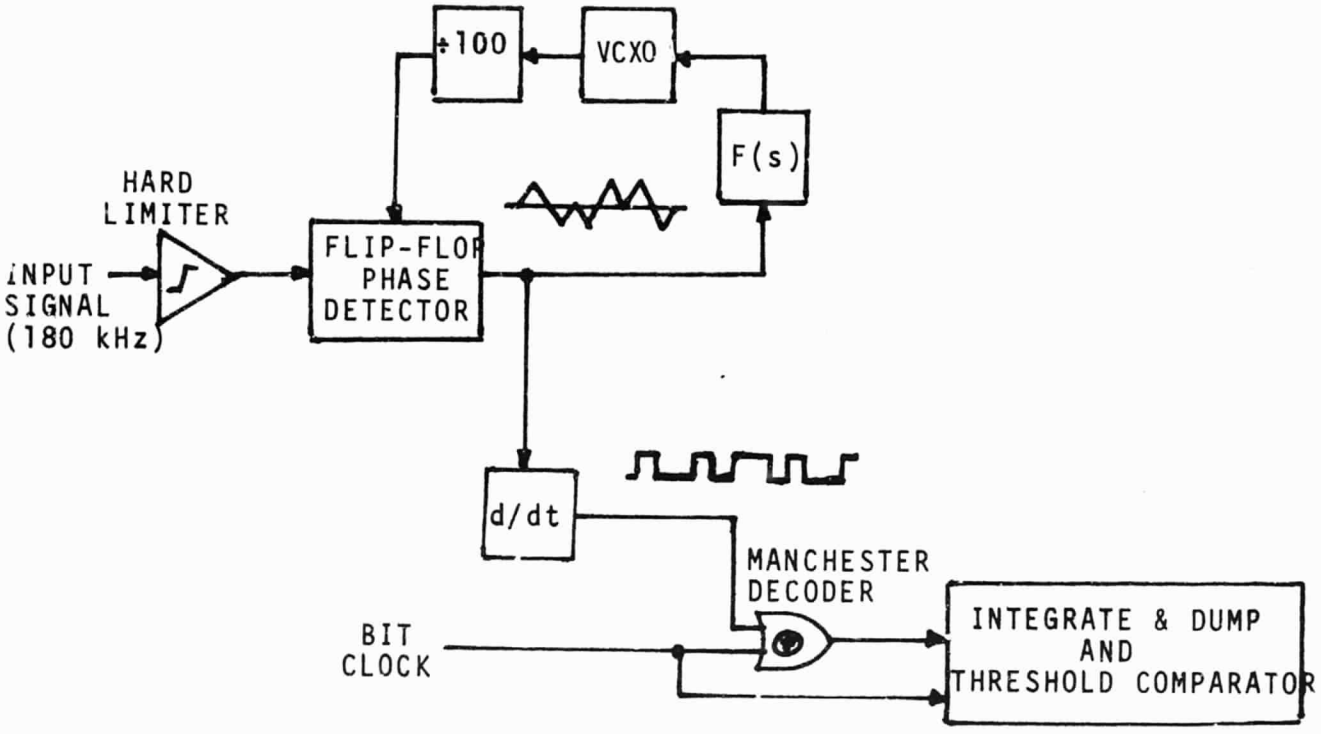
Since the non-coherent demodulator utilizes a phase lock loop to center the demodulator at the frequency of the incoming carrier, frequency offset in the non-coherent demodulator has no effect on the demodulation process - as long as the phase lock loop has enough pull-in range to acquire the signal and enough dc gain to minimize the phase offset out of the phase detector. Another vital parameter not listed above is the effect of interference on the performance of the demodulator. Unfortunately, long delivery times did not allow a suitable i-f filter to be purchased to allow meaningful interference tests to be conducted. The phase lock loop constructed in the non-coherent demodulator utilizes a flip-flop phase detector. This type phase detector provides a $\pm 180^{o}$ linear phase range, which, as will be shown later, is necessary for demodulation of the incoming MSK signal in the presence of noise. However, the phase detector does exhibit the unfortunate property of being captured by the strongest incoming signal, which means the filtering action of the phase lock loop itself provides no aid in rejecting an incoming interferer. The rejection of an incoming interferer is then solely dependent on the i-f filter characteristics. The i-f filter utilized is a 5-pole elliptic bandpass filter comprised of discrete LC components and exhibits a double-sided bandwidth of approximately 12 kHz. Interference tests were run and it was found that any interfering tone which fell inside the 12 kHz bandwidth and was of comparable strength to the signal itself resulted in a total loss of data. These results are certainly not indicative of the type of interference rejection capabilities achievable with MSK modulation utilizing the proper i-f filter.

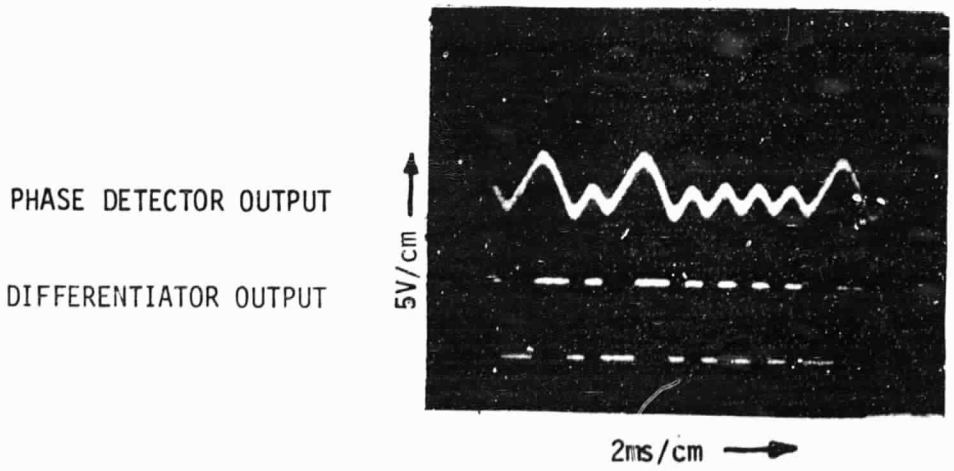
The test setup used to derive the E/N_o settings for the test measurements is shown in Figure 3-5, and is the same exact setup used to test the chirp-z transformer. A simplified block diagram of the non-coherent demodulator is shown in Figure 3-21, and typical waveforms at different points in the demodulator are also shown. The photograph showing the phase detector and differentiator outputs was obtained from the ADC/PL breadboard. MSK modulation is but a special case of phase coherent FSK modulation which utilizes a deviation ratio of 0.5. For a bit rate of 320 bps then, the total frequency deviation from mark to space frequencies is 160 Hz. However, the data format of the modulated data stream into the non-coherent demodulator is Manchester encoded to provide a carrier component for the phase lock loop to acquire and track. With Manchester encoding, the effective transition rate of the incoming signal can be as high as 640 Hz - depending on the content of the data being encoded. To maintain an MSK format with the Manchester encoding, the frequency separation between mark and space frequencies was set to 320 Hz. The initial portion of each transmission consists of just a carrier component centered halfway between the mark and space frequencies, and it is this carrier component which the phase lock loop acquires. When the first data bit is transmitted, the incoming frequency jumps to either the mark or space frequency - depending on the polarity of the first bit to be transmitted. This step in frequency is viewed by the phase lock loop as a ramp in phase, with the polarity of the slope depending on whether a mark or space frequency is being received. The output of the phase detector then is a series of positive and negative ramps in voltage. The Manchester encoding assures that the phase transitions are bounded between $+90^{o}$ and -90^{o}, and since the flip-flop phase detector has a linear range of $\pm 180^{o}$, a margin of $\pm 90^{o}$ is available for handling additional phase excursions due to noise.

The data polarity can be determined from the phase detector output by examining the polarity of the slope of the voltage output. The differentiator which follows the phase detector does just such an examination by converting the positive and negative voltage ramps into positive and negative steps in voltage. This is shown in Figure 3-21. These steps in voltage are a noise contaminated version of the Manchester data stream transmitted. The output from the differentiator is input into an exclusive - or circuit where the recovered data stream is mixed with a bit clock provided by the MSK Transmitter Simulator to remove the Manchester encoding. The output from the exclusive - or gate is a noise - contaminated version of the original NRZ data stream. The pseudo integrate and dump circuit and the threshold comparator which

NON-COHERENT MSK DEMODULATOR
BLOCK DIAGRAM AND KEY WAVEFORMS

Figure 3-21





follow the exclusive - or gate provide a near optimum method for recovering the NRZ data from the noise.

Figure 3-22 shows the E/N_o performance of the non-coherent MSK demodulator and data detector as compared to the E/N_o performance obtained in recovering the $\pm 60^o$ PSK data in the RAMS instrument. The E/N_o points were determined from the signal-to-noise readings by

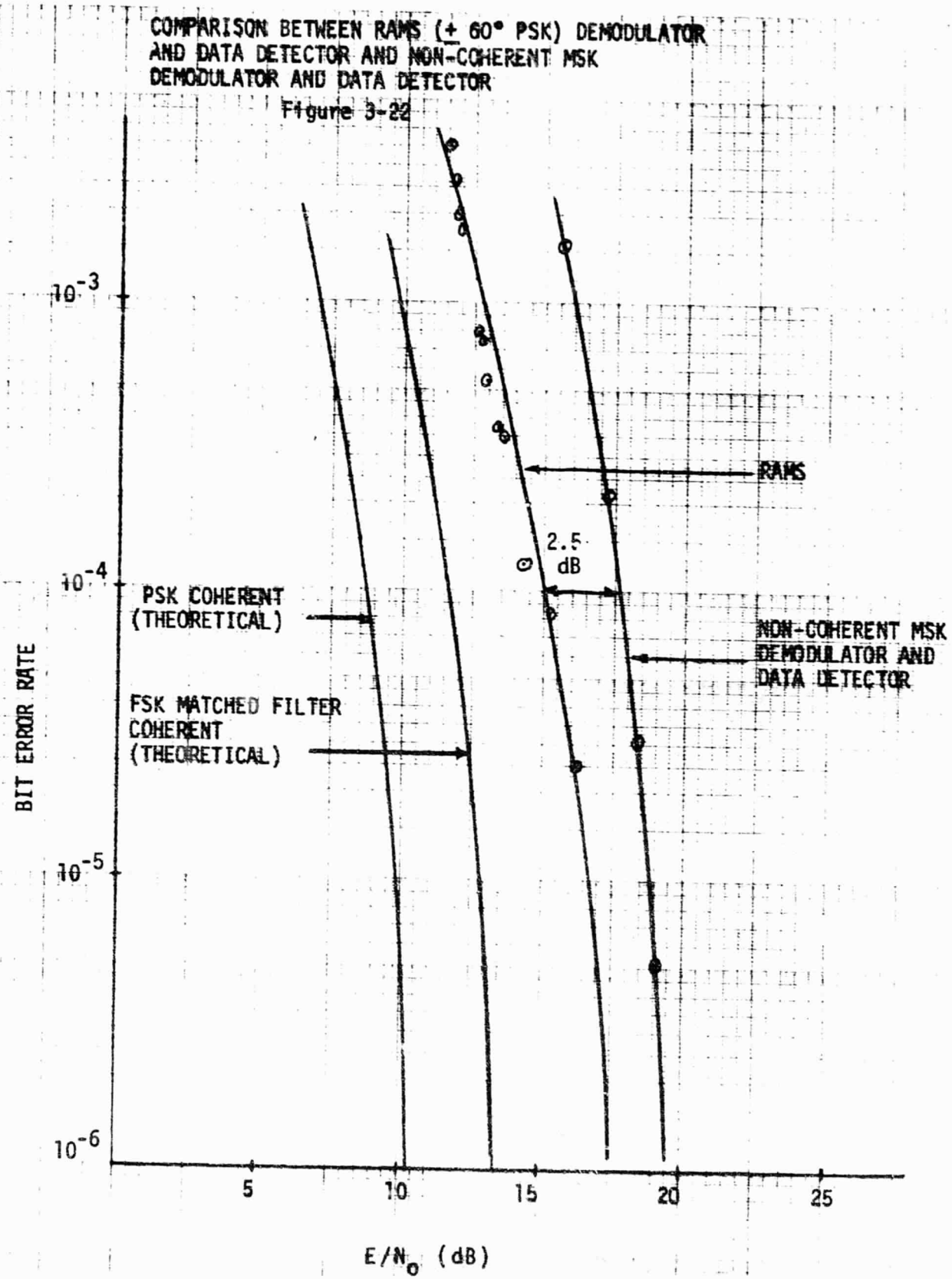
$$E/N_o = \frac{\text{Signal Power}}{\text{Noise Power}} \times \frac{\text{Noise Bandwidth}}{\text{Bit Rate}}$$

where the noise bandwidth is that bandwidth used to measure the noise power. The bit rate was taken to be 320 Hz, which is the bit rate of the NRZ data before Manchester encoding. If the maximum Manchester encoded data transition rate of 640 Hz were used for the bit rate, the E/N_o plot would improve by 3 dB. Figure 3-22 shows the non-coherent MSK demodulation process to be about 2.5 dB worse in performance than the RAMS instrument. However, three important points need to be made in making this comparison. First, the non-coherent MSK curve is the result of a non-optimum non-coherent demodulation process with the MSK modulation format being treated as an FSK modulation format. As shown in Figure 3-22, the optimum theoretical curve for demodulating an FSK signal is 3 dB worse in performance than the optimum theoretical curve for PSK modulation. Second, the RAMS curve is somewhat mislabeled in that it includes only the bit synchronizer and data detector and not the phase lock loop demodulator. Finally, the MSK curve, while including the phase lock loop demodulator and the data detector, does not include any losses that would be incurred in the bit synchronization process. It is hard than to draw any specific comparisons between the two systems, but it is obvious from examining Figure 3-22 that the non-coherent technique used in the ADC/PL breadboard for demodulating and recovering the NRZ data is inferior in E/N_o performance to that obtained in the RAMS instruments. It is also clear from Figure 3-22 that to minimize additional losses due to the bit synchronization process it would be advisable to use a phase lock loop bit synchronizer (which was experimentally developed and tested on the RAMS instrument) rather than a ringing circuit type bit synchronizer such as finally used on the RAMS instrument.

The results shown in Figure 3-22 are somewhat disappointing, and as a result tests were conducted to determine to what degree the different components of the non-coherent demodulator and data detector contributed to the total loss measured. Figure 3-23 shows the test configurations used to test the different components of the demodulator. The first step was to test just the data detector. As shown in Figure 3-23, this was accomplished by simply

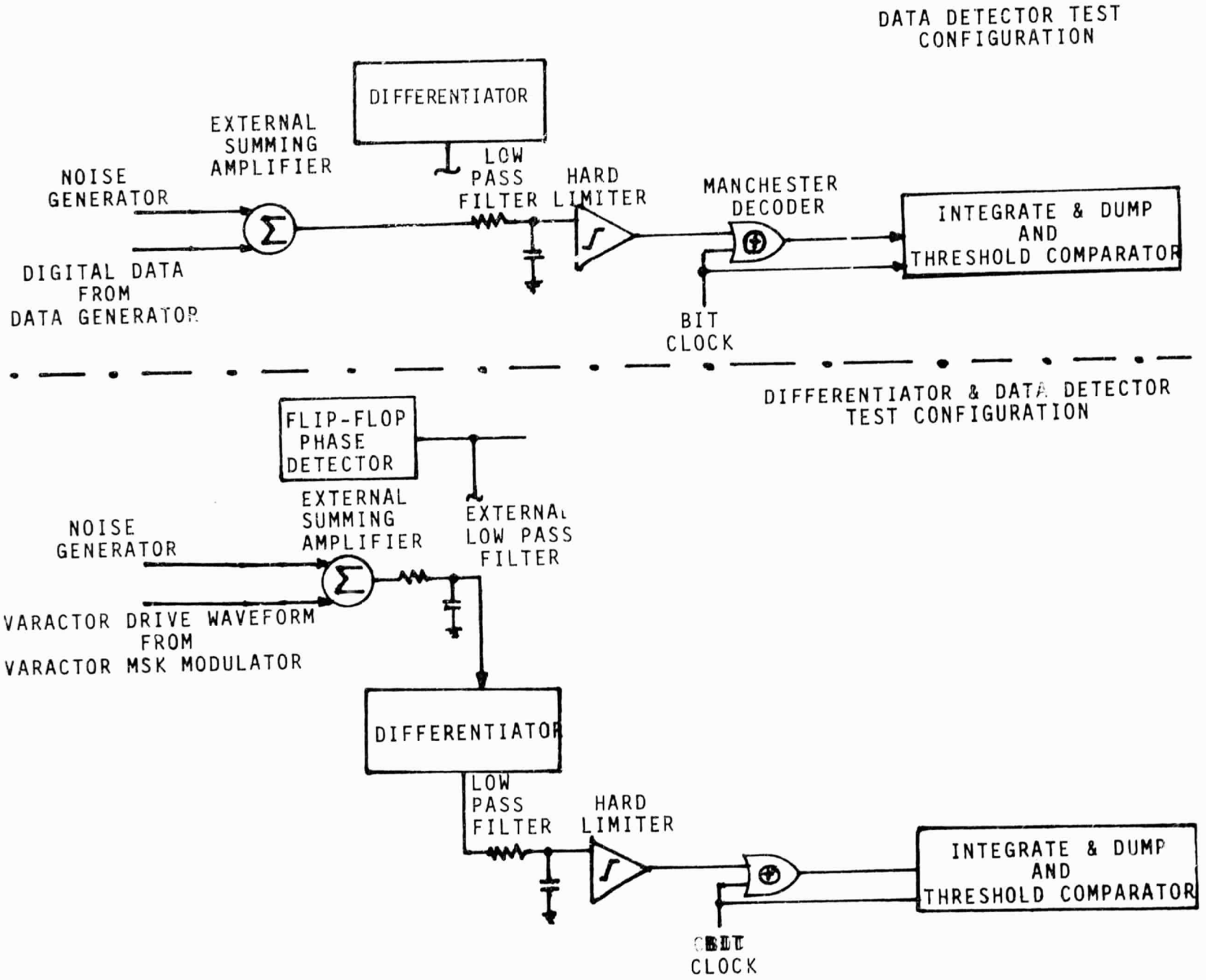
COMPARISON BETWEEN RAMS (± 60° PSK) DEMODULATOR AND DATA DETECTOR AND NON-COHERENT MSK DEMODULATOR AND DATA DETECTOR

Figure 3-22



TEST CONFIGURATIONS FOR ANALYZING COMPONENT PARTS OF NON-COHERENT MSK DEMODULATOR

Figure 3-23

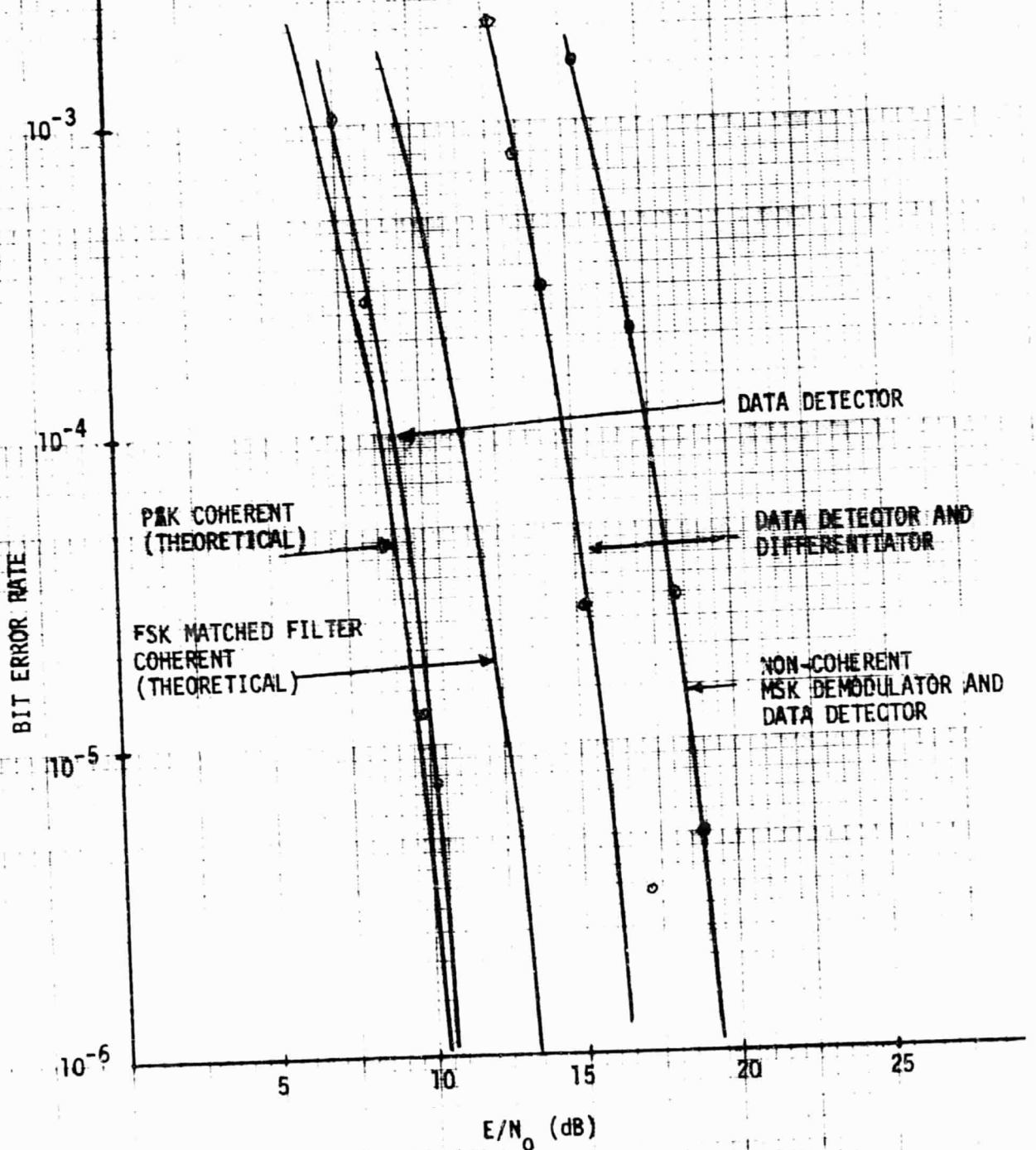


inserting the Manchester encoded data stream from the data generator in the MSK Transmitter Simulator and the output of a noise generator into a summing amplifier and routing the output of the summing amplifier to the low pass filter which is normally attached to the output of the differentiator. The low pass filter is part of the non-coherent demodulation circuitry and its bandwidth served as the noise bandwidth for determining the E/N_o points. The results of the test are shown in Figure 3-24. As can be seen from Figure 3-24, the data detector curve lies 0.5 dB from the theoretical curve. The data detector configuration used is an exact copy of the data detector used on the RAMS instrument and the bit error rate vs. E/N_o curve is an exact copy of the data detector performance measured on the RAMS instrument.

The next step is to include the differentiator in the test configuration. The input into the differentiator, which is normally provided by the output of the flip-flop phase detector, is a series of voltage ramps whose slope depends on the polarity of the incoming data bit. Fortunately, just such a noise-free drive waveform is available from the Communications Link Simulator, as the same exact waveform output by the flip-flop phase detector is also required to drive the varactor phase shift network in the varactor phase shift MSK modulator (refer to Figure 2-7). The varactor drive waveform and the output from a noise generator are summed together in an external summing amplifier and the output of the amplifier is routed through an external low pass filter prior to inputting into the differentiator. The low pass filter is used to define the noise bandwidth for converting the measured signal-to-noise ratio readings to E/N_o readings. The results are shown in Figure 3-24 and it is noted that the differentiator contributes 5.5 dB degradation in performance. This is a significant portion of the total loss measured in the non-coherent demodulator and data detector, and every effort was made to minimize this loss. The differentiator is not a simple differentiator but rather is a band-limited differentiator with low pass filtering provided to minimize the noise output by the differentiator. A transfer function of the differentiator and the low pass filter which follows the differentiator is shown in Figure 3-25. A simple differentiator contains only a zero located at the origin, with the gain ever increasing as a function of frequency. Figure 3-25, however, shows that three additional poles have been included to eliminate the high frequency noise components from the differentiation process. The first pole is at approximately 530 Hz and the other two poles - one being the pole provided by the low pass filter which follows the differentiator - are both at approximately 588 Hz. It was found experimentally in the ADC/PL breadboard that this configuration

PERFORMANCE OF COMPONENT PARTS COMPRISING
NON-COHERENT MSK DEMODULATOR AND DATA DETECTOR

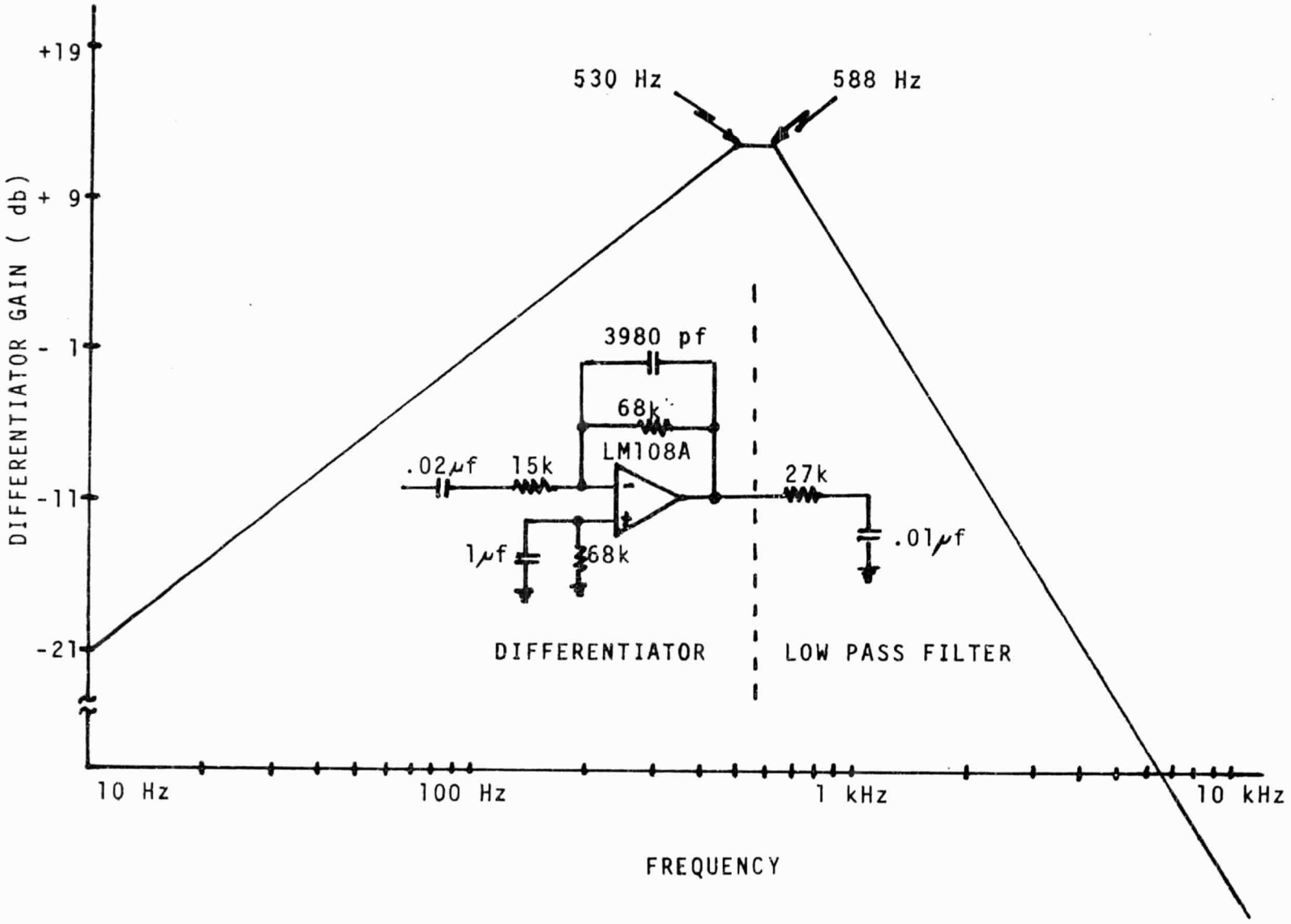
Figure 3-24



DATA DETECTOR = 0.5 dB loss
DIFFERENTIATOR = 5.5 dB loss
PHASE LOCK LOOP AND FRONT END LIMITER = 2.75 dB loss

FREQUENCY RESPONSE OF DIFFERENTIATOR
AND LOW PASS FILTER

Figure 3-25



of the differentiator provided the best E/N_o results.

The non-coherent MSK demodulator and data detector E/N_o curve is offset from the theoretical PSK curve by approximately 8.75 dB. Since the component tests showed that the data detector contributed 0.5 dB of loss and the differentiator contributed 5.5 dB of loss, the phase lock loop and front end limiter are left with a 2.75 dB loss contribution. The signal-to-noise ratio into the limiter is set by the 13 kHz bandpass filter preceeding the limiter and is in the range of - 5dB to +4dB. For these levels of input signal-to-noise ratio, the limiter will account for approximately 1 dB of the 2.75 dB of loss, which leaves the phase lock loop itself with approximately 1.75 dB of loss. A definite contributor to this 1.75 dB of loss will be the flip-flop phase detector. The flip-flop type of phase detector was chosen because it displays a $\pm 180^{o}$ linear phase range. However, this type of phase detector is admittedly a poor choice for low signal-to-noise ratio environments. Figure 3-26 presents a comparison in the overall performance of the non-coherent demodulator between using a flip-flop type phase detector and an exclusive-or type phase detector. It is seen that the exclusive-or type phase detector provides approximately 0.5 dB improvement in performance. However, it was necessary to reduce the deviation ratio to 0.25 - from the 0.5 ratio used for MSK - to keep the phase lock loop from slipping cycles when the exclusive - or type phase detector was used. The exclusive - or type phase detector exhibits only a $\pm 90^{o}$ linear phase range, and since the MSK modulation format results in linear phase ramps between $\pm 90^{o}$, there is no margin left to accommodate phase excursions due to noise. Thus the improvement provided by the exclusive - or phase detector is strictly of academic interest only since it could not be used with MSK modulation. From the standpoint of optimum signal-to-noise performance, the optimum phase detector configuration would be a sinusoidal type phase detector with no limiter preceeding the detector. Unfortunately, this type of phase detector exhibits even less of a linear phase range than does the exclusive - or gate and thus would be unusable for the demodulation of MSK.

Table 3-1 tabularizes the losses of the component parts comprising the non-coherent demodulator. Again, the total loss or deviation from the theoretical PSK demodulation curve was 8.75 dB, with more than half the loss accounted for in the differentiator.

COMPARISON BETWEEN FLIP-FLOP PHASE DETECTORS AND EXCLUSIVE-OR GATE (MIXER) PHASE DETECTORS IN NON-COHERENT MSK DEMODULATOR AND DATA DETECTOR

Figure 3-26

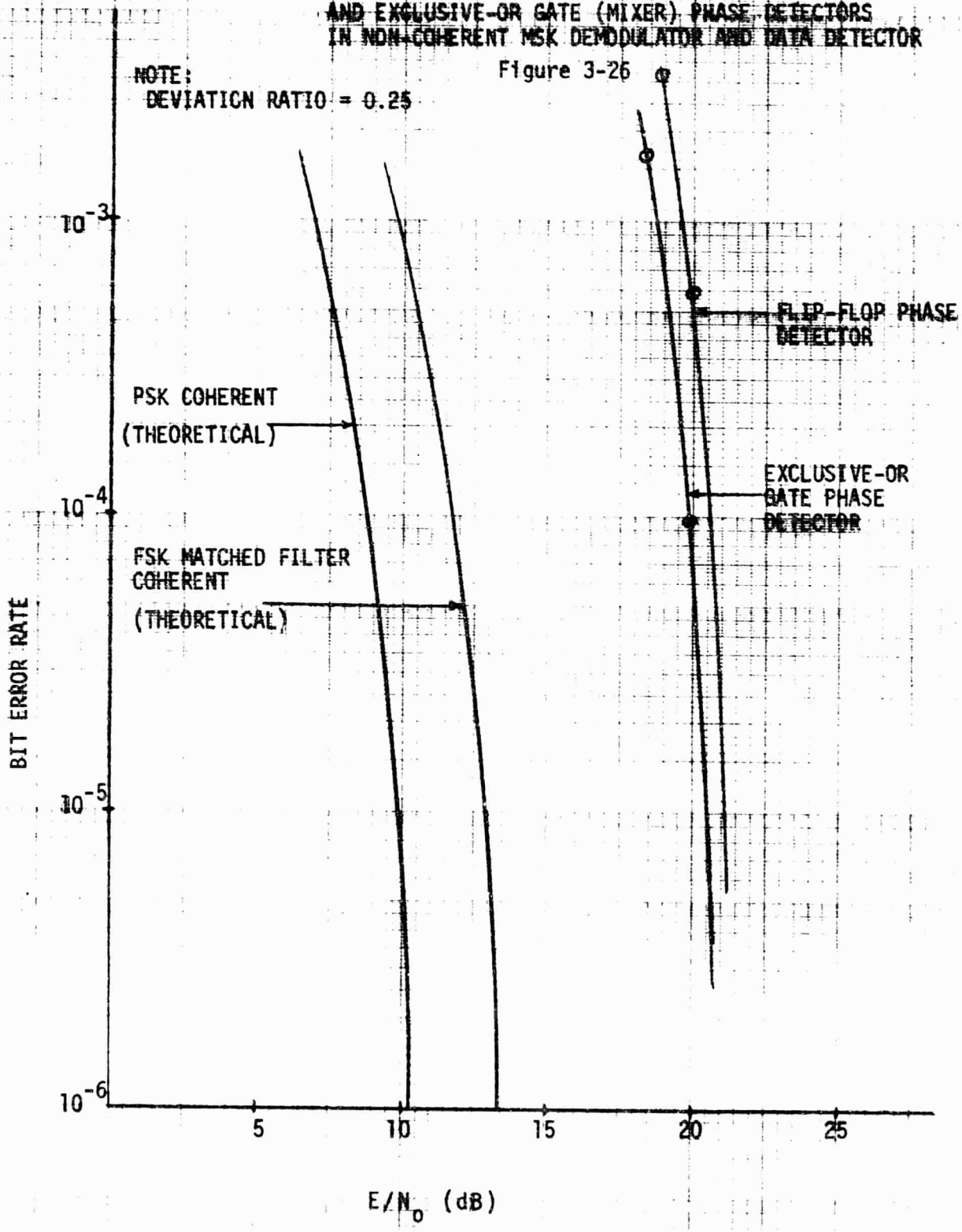


Table 3-1

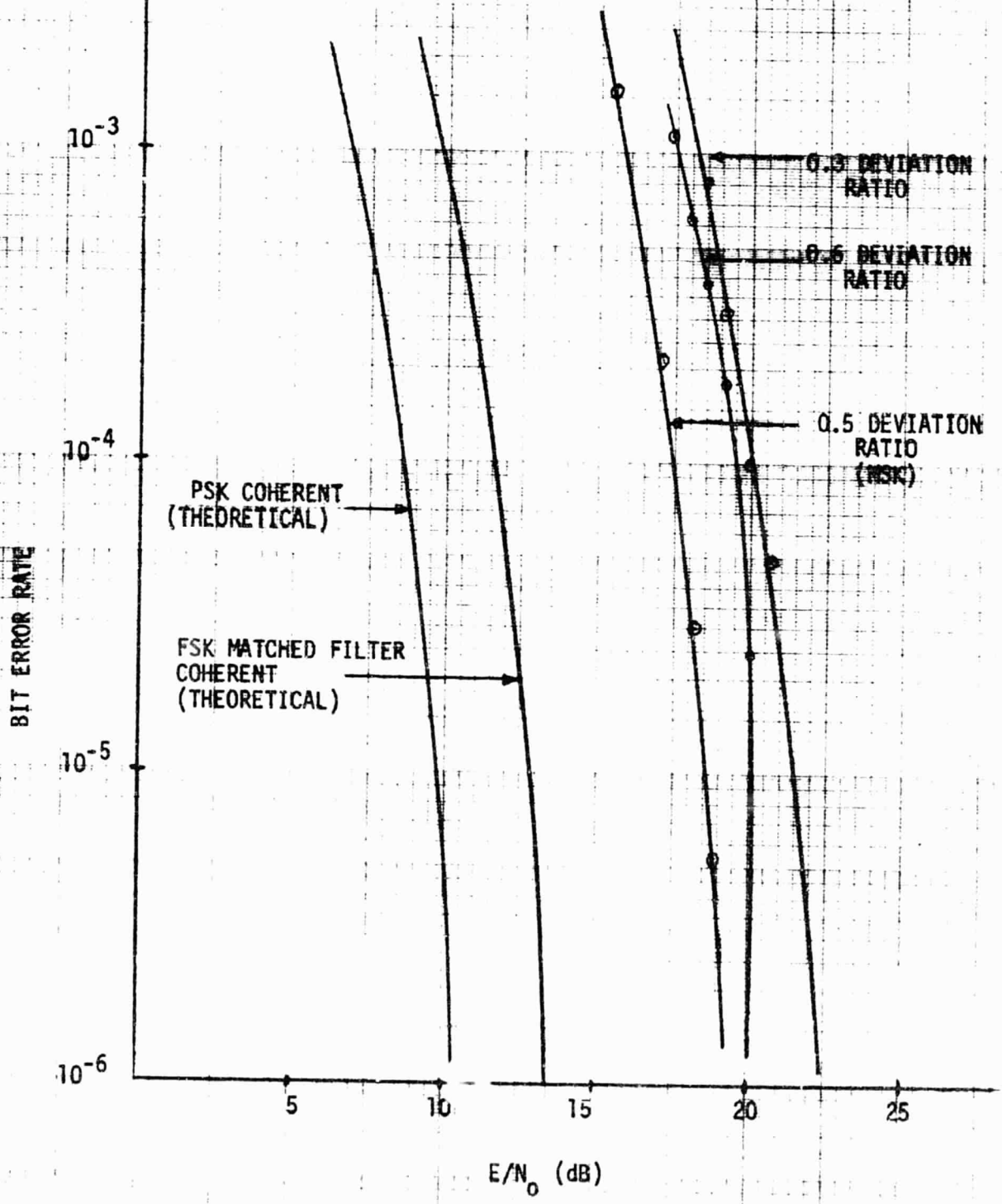
Itemization of Losses in Non-Coherent

MSK Demodulator

COMPONENT	LOSS
Front End Limiter	1.0 dB
Flip-Flop Phase Detector	0.5 dB
Other PLL Losses	1.25 dB
Differentiator	5.5 dB
Data Detector	0.5 dB
TOTAL	8.75 dB

Having measured the performance of the non-coherent demodulator and data detector, these were then used as a vehicle for measuring other data dependent parameters. A set of measurements were taken to determine how the non-coherent demodulator and data detector behave in the presence of deviation ratios other than the deviation ratio of 0.5 for MSK modulation. The noncoherent demodulator and data detector do not utilize the unique in-phase and quadrature components that comprise MSK modulation and which can be shown to give MSK modulation the capability of being demodulated as a coherent PSK signal, but rather treats MSK as coherent FSK. The deviation ratio is not vital then in the non-coherent demodulation scheme. Figure 3-27 shows the bit error rate as a function of E/N_o for three different deviation ratios - 0.3, 0.5, and 0.6. Manchester encoding of the data was utilized for all three deviation ratios to provide a carrier component for the phase lock loop to acquire and track. As seen from Figure 3-27, the deviation ratio of 0.5 gives the best results, which is somewhat contrary to that expected since the higher deviation ratios should result in more power in the data sidebands. The discrepancy is due to the limited phase excursions of $\pm 180^{o}$ that can be handled by the flip-flop phase detector. A deviation ratio of 0.6 yields phase excursions of $\pm 108^{o}$, or 18^{o} more than that encountered with the 0.5 (MSK) deviation ratio. This means the deviation ratio of 0.6 removes 18^{o} of phase margin that can be allotted to phase noise excursions. It is this loss of 18^{o} of phase margin that causes the 0.6 deviation ratio bit error rate curve to lie outside the 0.5 deviation ratio bit error rate curve - the phase lock loop slips cycles due to phase noise excursions more often in the 0.6 deviation ratio case. It is noted in Figure 3-27 that as the E/N_o ratio increases, the 0.6 deviation ratio curve improves in bit error rate performance at a much faster rate than do the 0.5 or 0.3 deviation ratio curves. This phenomenon is expected since as the E/N_o ratio improves, the phase noise excursions diminish and the phase detector remains in its linear range, allowing the increased signal power in the data sidebands for the 0.6 deviation ratio to improve the bit error rate performance obtained. In conclusion, it appears that with the non-coherent MSK demodulator configuration utilized, a deviation ratio of 0.5 provides the best bit error rate results.

PERFORMANCE OF NON-COHERENT MSK
DEMODULATOR FOR DIFFERENT DEVIATION RATIOS
Figure 3-27



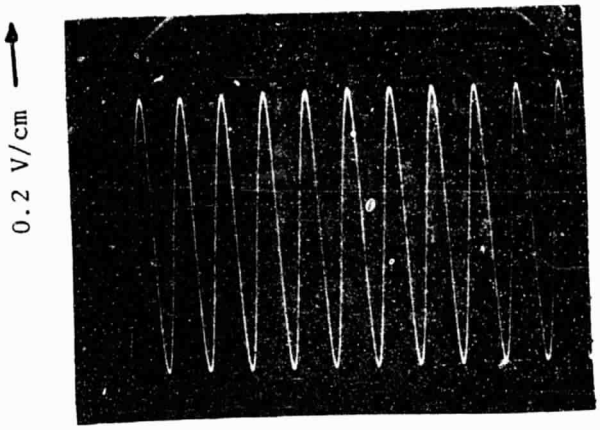
A set of measurements were also made to determine the effect, if any, that non-linear processing of the MSK modulation in the transmitter - such as class C rf power amplifiers - would have on the demodulation performance. Since there are no phase discontinuities in an MSK modulated signal there should be no change in the spectral content of the modulation due to non-linear processing, except to add harmonic spectral bands about the harmonics of the carrier. Figure 3-28 shows both time domain and frequency domain representations of both linear and non-linear MSK modulated signals. The varactor phase shift MSK modulator in the Communications Link Simulator was used as the source of MSK modulation, and a hard limiter, inserted at the 10.7 MHz i-f, was used to simulate the non-linear effects of class-C type power amplifiers. The voltage swings in the two time domain photographs have no significance when compared to each other as they were taken from different points in the circuitry. The spectral photographs display the spectral content about the 10.7 MHz i-f, and as can be seen, there is very little, if any, difference in the spectral pattern resulting from linear or non-linear transmission of MSK modulation. This is a very key finding since it means that expensive linear r-f stages in the transmitter are not required to prevent spectral splatter. This also means that coherent MSK modulation (data rate and carrier coherently related) is not necessary to retain the spectral properties key to MSK. These are very key advantages that MSK offers for an ADC/PL application.

Figure 3-29 presents a comparison in MSK demodulation performance for linear and class-C transmission of MSK modulated signals. For all practical purposes there is no difference, again illustrating that MSK modulation is not affected by non-linear operations in the transmission process.

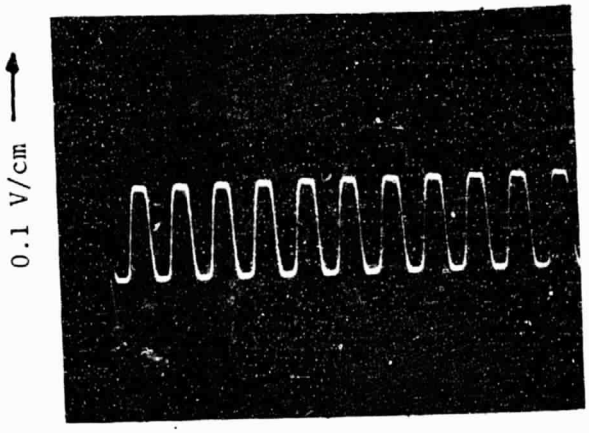
The last test conducted on the non-coherent MSK demodulator was to examine the differences, if any, in the bit error rate performance obtained in the non-coherent demodulator utilizing different types of MSK modulators. Three types of MSK modulators were used - the coherent digital MSK modulator housed in the MSK Transmitter Simulator and the non-coherent varactor phase shift and VCXO MSK modulators housed in the Communications Link Simulator. The results are shown in Figure 3-30, and as can be seen, there is little difference in performance between the three types of modulators. The digital

SPECTRAL COMPARISON BETWEEN LINEAR
AND CLASS C TRANSMISSION OF MSK
MODULATION

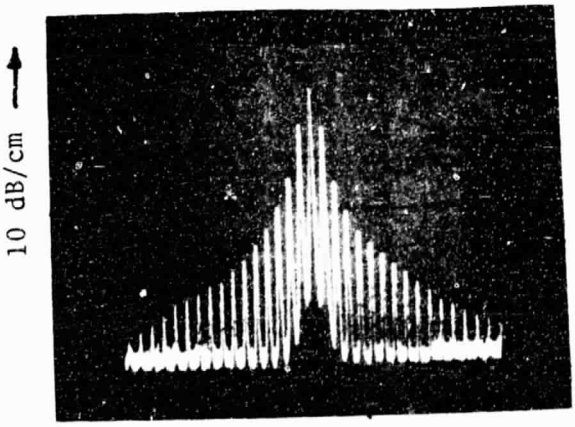
FIGURE 3-28



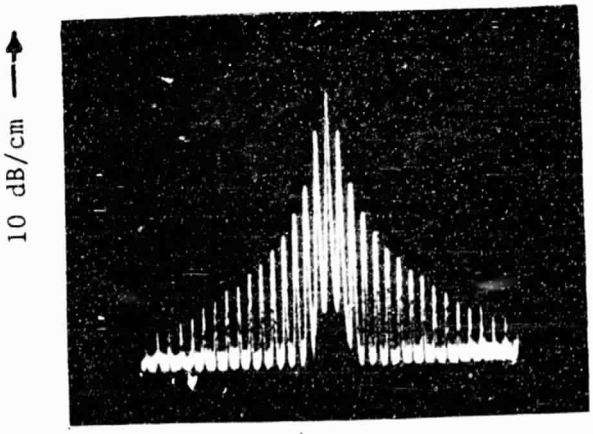
LINEAR TRANSMISSION OF
MSK MODULATION



CLASS C TRANSMISSION OF
MSK MODULATION



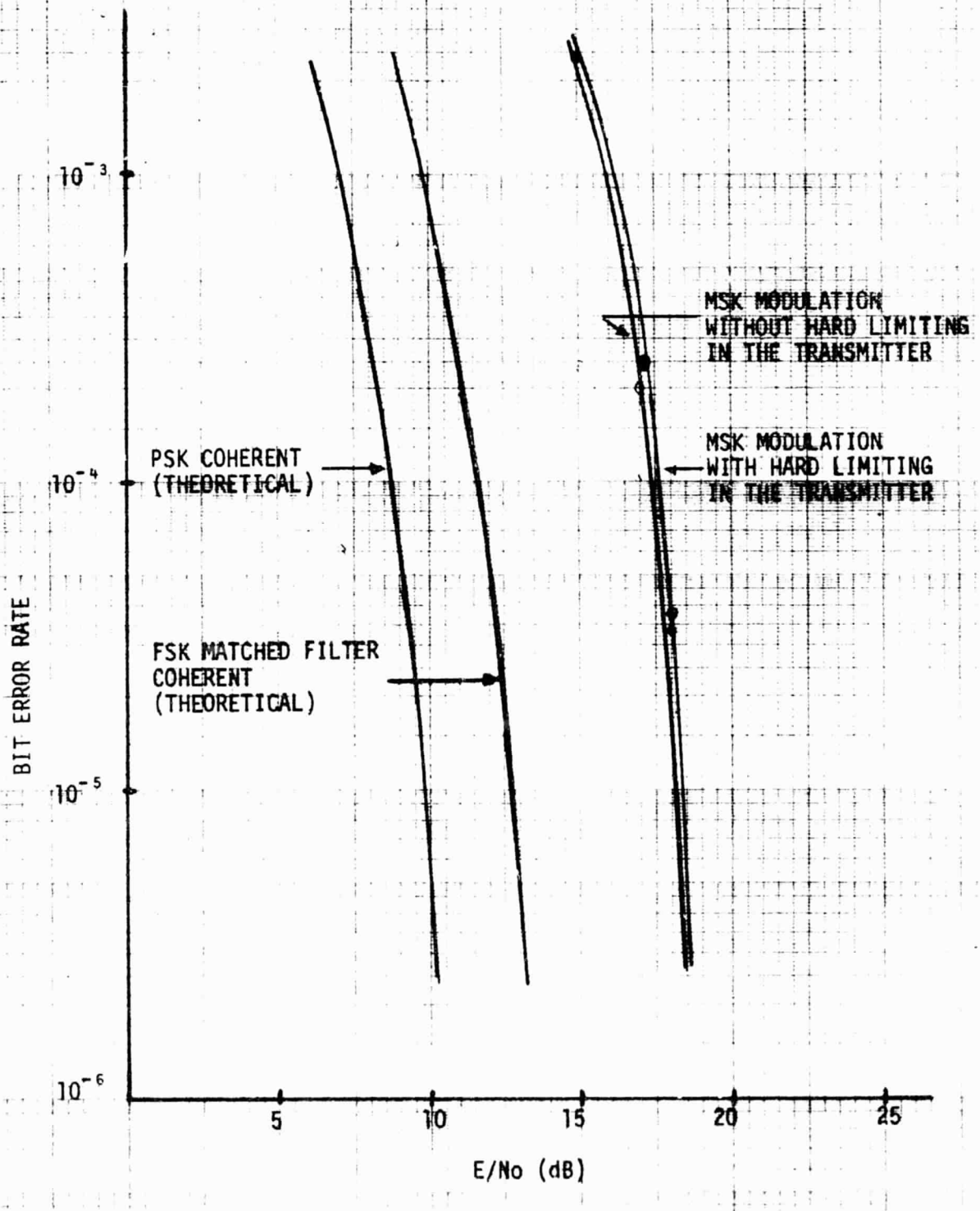
SPECTRAL CONTENT OF
LINEAR TRANSMISSION OF MSK
MODULATION
CENTER FREQUENCY = 10.7 MHz



SPECTRAL CONTENT OF
CLASS C TRANSMISSION OF MSK
MODULATION
CENTER FREQUENCY = 10.7 MHz

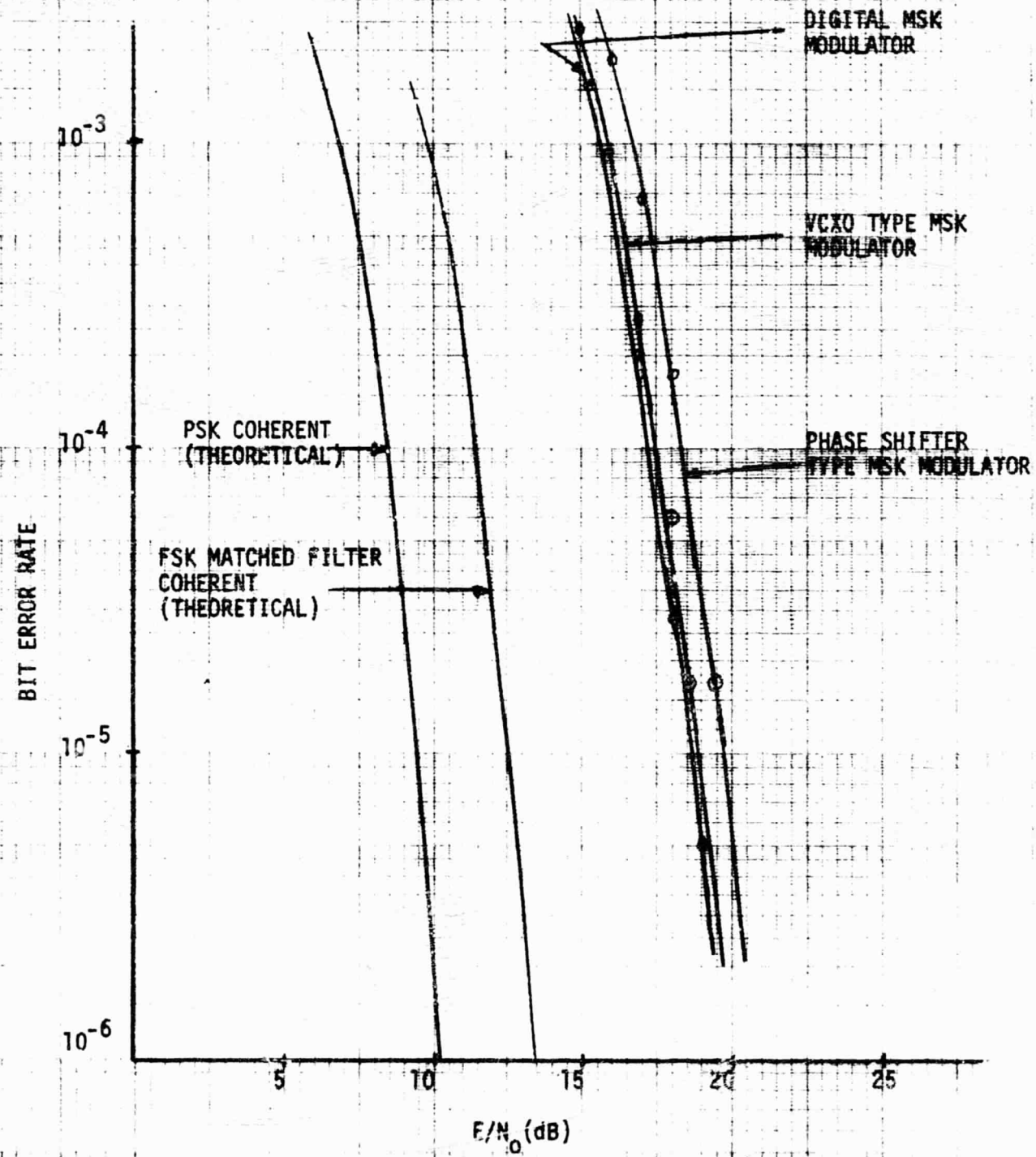
COMPARISON IN MSK DEMODULATION PERFORMANCE
FOR LINEAR AND CLASS C TRANSMISSION
OF MSK MODULATED SIGNALS

Figure 3-29



COMPARISON OF DIFFERENT TYPES OF MSK MODULATORS

Figure 3-30



MSK modulator does show the best bit error rate vs. E/N_o performance while the varactor phase shift MSK modulator shows the worst performance. However, the separation in the two curves is under 1.0 dB - which falls within measurement accuracy tolerances.

D. ALTERNATIVE NON-COHERENT DEMODULATION SCHEMES AND TEST RESULTS

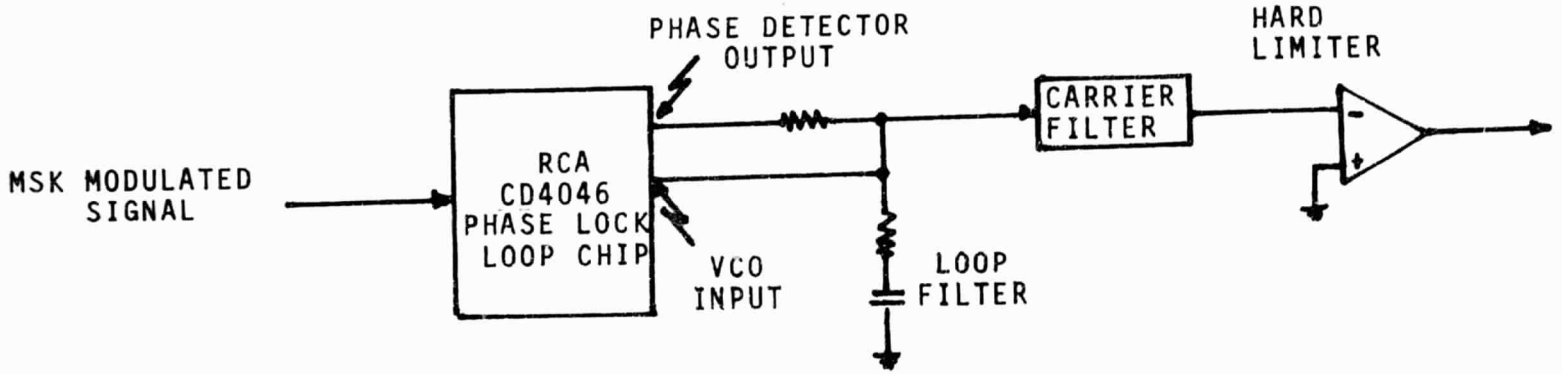
A key feature of the non-coherent demodulator presented in the previous section is that it provides a mechanism for performing a precise frequency measurement as well as demodulating the incoming signal. In fact, the frequency measurement requirement was a key consideration in arriving at the final non-coherent demodulator configuration used. However, as seen in Table 3-1, the bit error rate performance was not as good as hoped, and the key element in the degradation of the bit error rate was the differentiator. Attempts were thus made to come up with different schemes which would not require the use of a differentiator, which is not an attractive element to be utilizing in noisy environments.

The first scheme devised was to use a separate phase lock loop for the demodulation process and use the carrier tracking loop in the previously described non-coherent demodulator simply for frequency measurements. The separate phase lock loop has a much wider loop tracking bandwidth and tracks the frequency steps of the MSK modulation format. In essence, the phase lock loop serves as a discriminator with the output of the loop filter, or input into the VCO, being the demodulated output. Initially the loop is locked to the carrier. When the first bit is transmitted, the loop slews to the mark or space frequency being received, which requires a positive or negative step in voltage into the VCO - depending on whether the mark or space frequency is being received. When the polarity of the data changes, the loop slews to the new frequency (mark or space). The input into the VCO then is a replica of the Manchester encoded data train transmitted and serves as the demodulated output.

Figure 3-31 is a block diagram of the separate phase lock loop non-coherent demodulation scheme. The scheme would not be viable if the addition of a second phase lock loop for demodulation required doubling the complexity of the overall receive hardware. Fortunately as Figure 3-31 shows, the wide bandwidth requirements on the demodulation loop allows a standard phase lock loop chip (RCA CD 4046) to be utilized. The RC components defining the loop filter are external to the chip, and a carrier filter is inserted at the output of the loop to further reduce the carrier component. A hard limiter follows

PHASE LOCK LOOP FM DISCRIMINATOR
NON-COHERENT MSK DEMODULATOR

Figure 3-31



the carrier filter to provide a logic compatible signal for driving the exclusive - or Manchester decoder in the data detector. Gardner[1] has shown that for small deviation ratios or modulation indices, the loop noise bandwidth should be equal to the r-f bandwidth occupied by the incoming modulated signal and heavy damping should be used. The noise bandwidth then was chosen to be 350 Hz - which is approximately 1.15 times the bit rate of 320 Hz - and a damping factor of 1 was used. A double-sided bandwidth of 2.3 times the bit rate contains 99% of the power of the MSK modulated signal, and thus the factor of 1.15 times the bit rate for the noise bandwidth gives a setting equal to the effective single-sided bandwidth occupied by MSK modulation.

The bit error rate vs. E/N_o obtained in the separate phase lock loop FM discriminator type demodulator is compared in Figure 3-32 to that obtained with the narrow-band carrier tracking non-coherent demodulator utilizing the differentiator. As can be seen, the separate phase lock loop FM discriminator type demodulator shows an improvement of approximately 0.5 dB over the carrier tracking/differentiator type non-coherent MSK demodulator discussed in the previous section. Although an improvement is shown, the improvement is so slight that it hardly warrants the additional hardware required.

The second demodulation scheme devised involves using just the carrier tracking loop. A simplified block diagram and pertinent waveforms are shown in Figure 3-33. The output of the flip-flop phase detector, which, as shown, is a series of voltage ramps, is passed through a low pass filter and input into a threshold comparator. The threshold comparator output is input into a flip-flop, and the flip-flop samples the input at the midpoint of a bit period. The sampling is done at the midpoint of the bit period since it is at this point that the voltage ramps output by the phase detector reach their peak values. The resulting output from the sampling flip-flop is the recovered NRZ data stream. As was the case in the other non-coherent demodulation schemes presented, Figures 3-33 includes no provisions for recovering the bit clock.

Obviously, the scheme is far from ideal in that it is essentially an open-loop demodulation/detection process. However, the circuitry being replaced - the differentiator and data detector - represents 6 dB of loss in E/N_o performance. If this technique can even duplicate a loss performance of 6 dB, it holds a distinct advantage over the differentiation/data detection

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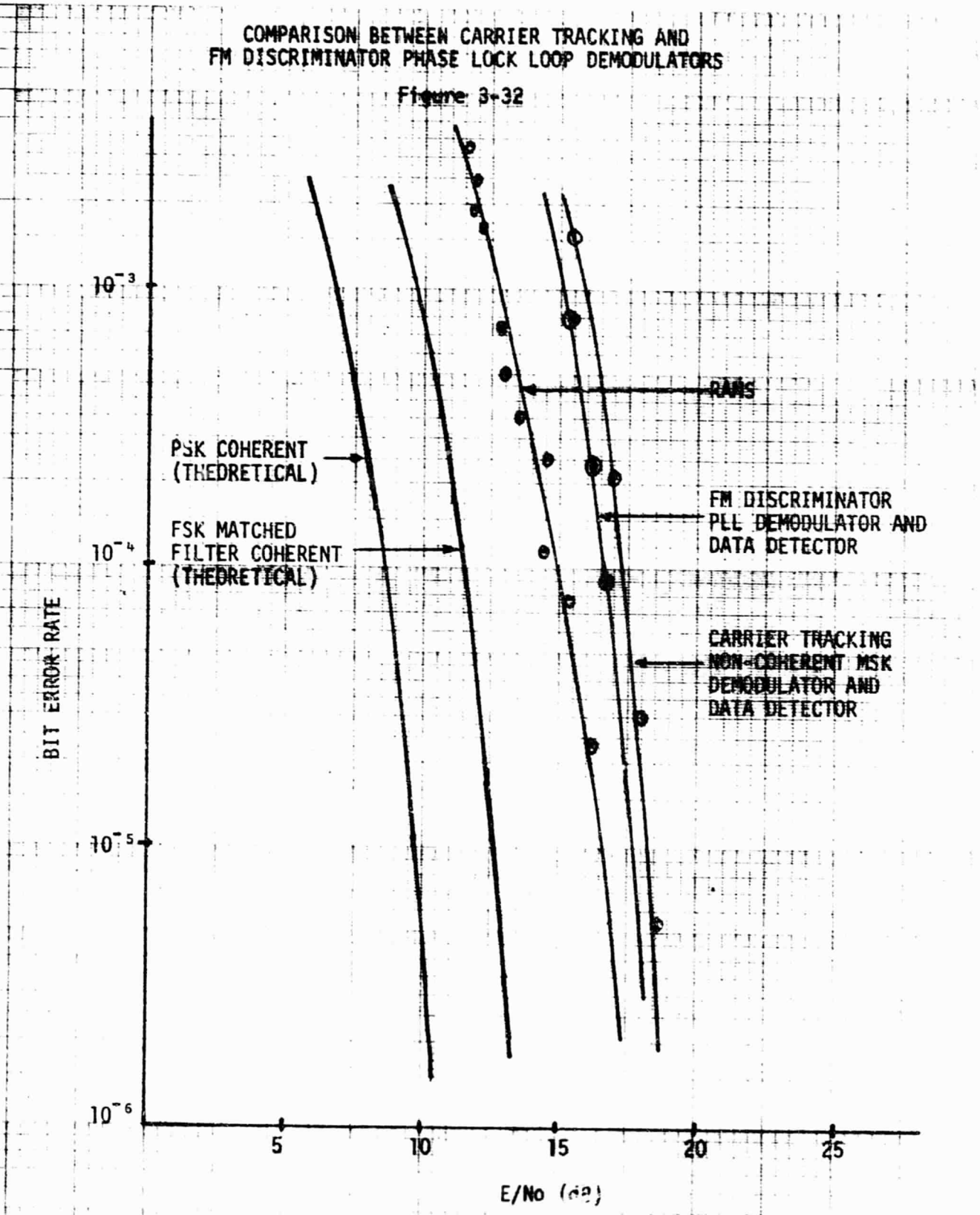
[1] Gardner, F.M., "Phaselock Techniques", pg 114, Wiley, New York, 1966

COMPARISON BETWEEN CARRIER TRACKING AND
FM DISCRIMINATOR PHASE LOCK LOOP DEMODULATORS

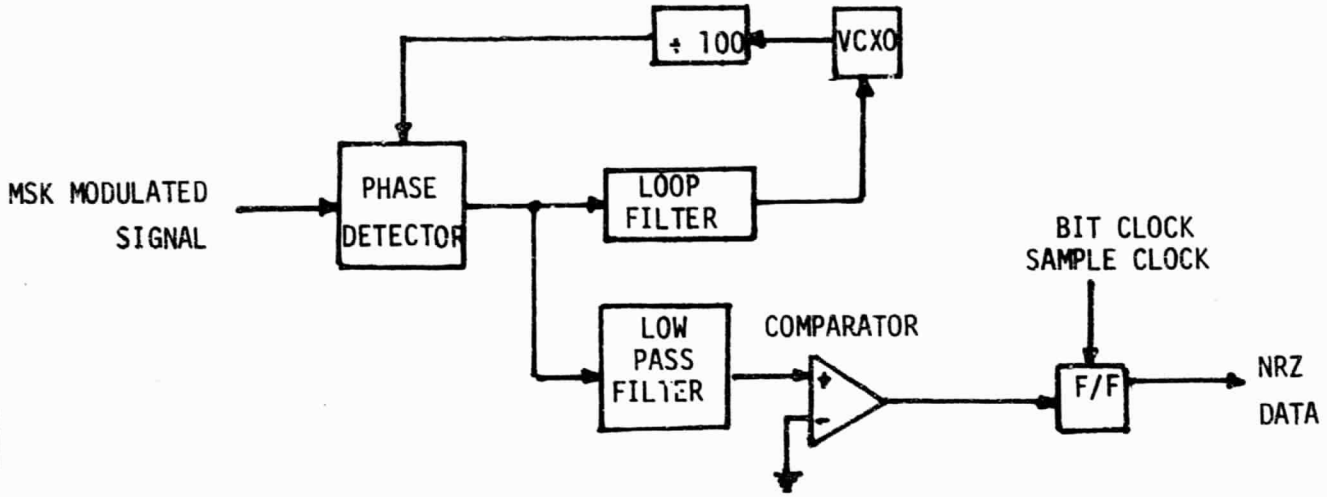
Figure 3-32

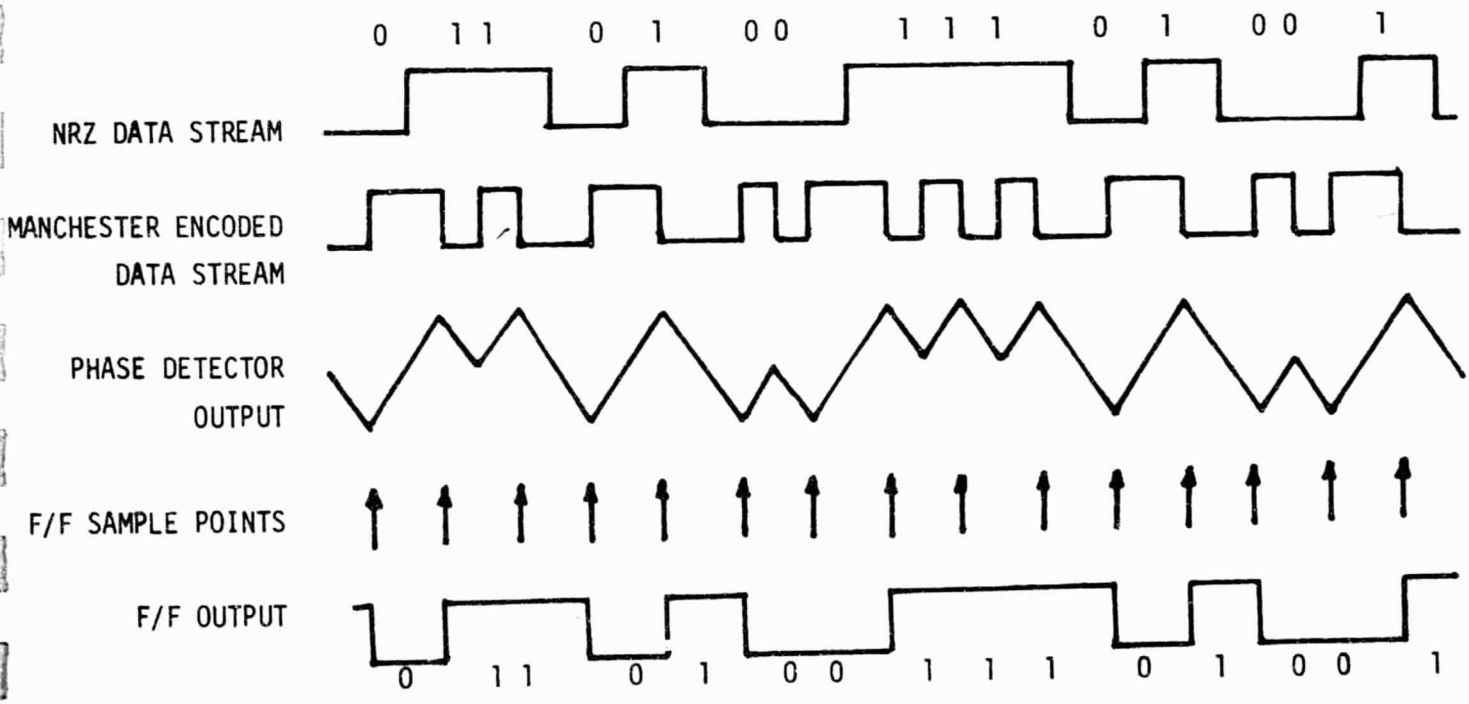


CARRIER TRACKING PHASE LOCK LOOP

DEMODULATOR

Figure 3-33





technique in that it requires much less hardware to implement.

The results of the E/N_o tests conducted on the alternate carrier tracking loop demodulation scheme are shown in Figure 3-33A. The other two MSK demodulators are also depicted for ease in comparing results. As can be seen, the alternate demodulation scheme is approximately 1dB worse in E/N_o performance than the demodulation scheme employing the differentiator and about 1.5 dB worse than the separate phase lock loop discriminator demodulator.

E. FREQUENCY MEASUREMENT TEST RESULTS

A simplified block diagram of the frequency measurement circuitry is shown in Figure 3-34. The circuitry is quite simple, consisting of only count control logic and a BCD counter. The frequency to be measured is taken from the VCXO in the carrier tracking phase lock loop. The resolution required is 0.1 Hz, which means the incoming carrier frequency must be measured to a 0.1 Hz accuracy or a multiple of 0.1 Hz in accuracy. A multiplicative factor of 100 is used. The VCXO output is divided by 100 before it is input into the reference port of the phase detector, which means the VCXO runs at 100 times the incoming carrier in frequency. A 0.1 Hz measurement resolution of the incoming carrier then requires measuring the VCXO frequency to a resolution of 10 Hz - which can be accomplished in a measurement window of 100 milliseconds. The measurement is initiated by the reception of the frame synchronization code in the data checker housed in the MSK Transmitter Simulator. A 10 Hz clock from the Search Subsystem provides the 100 millisecond measurement window.

It would initially appear that the frequency measurement circuit, if properly working, requires little characterization - either the phase lock loop is locked to the incoming carrier, in which case the proper measurement will be made, or the loop did not acquire the signal. The frequency measurements showed, however, that the resolution obtainable is highly dependent on the signal-to-noise ratio within the phase lock loop, even if the loop is locked and tracking the carrier. The presence of the noise will result in the phase detector outputting jitter which, in turn, will cause phase fluctuations in the VCXO. Gardner[1] has shown that the mean square output phase jitter from the VCXO is:

$$\overline{\phi^2_{no}} = \frac{1}{2(SNR)_L}$$

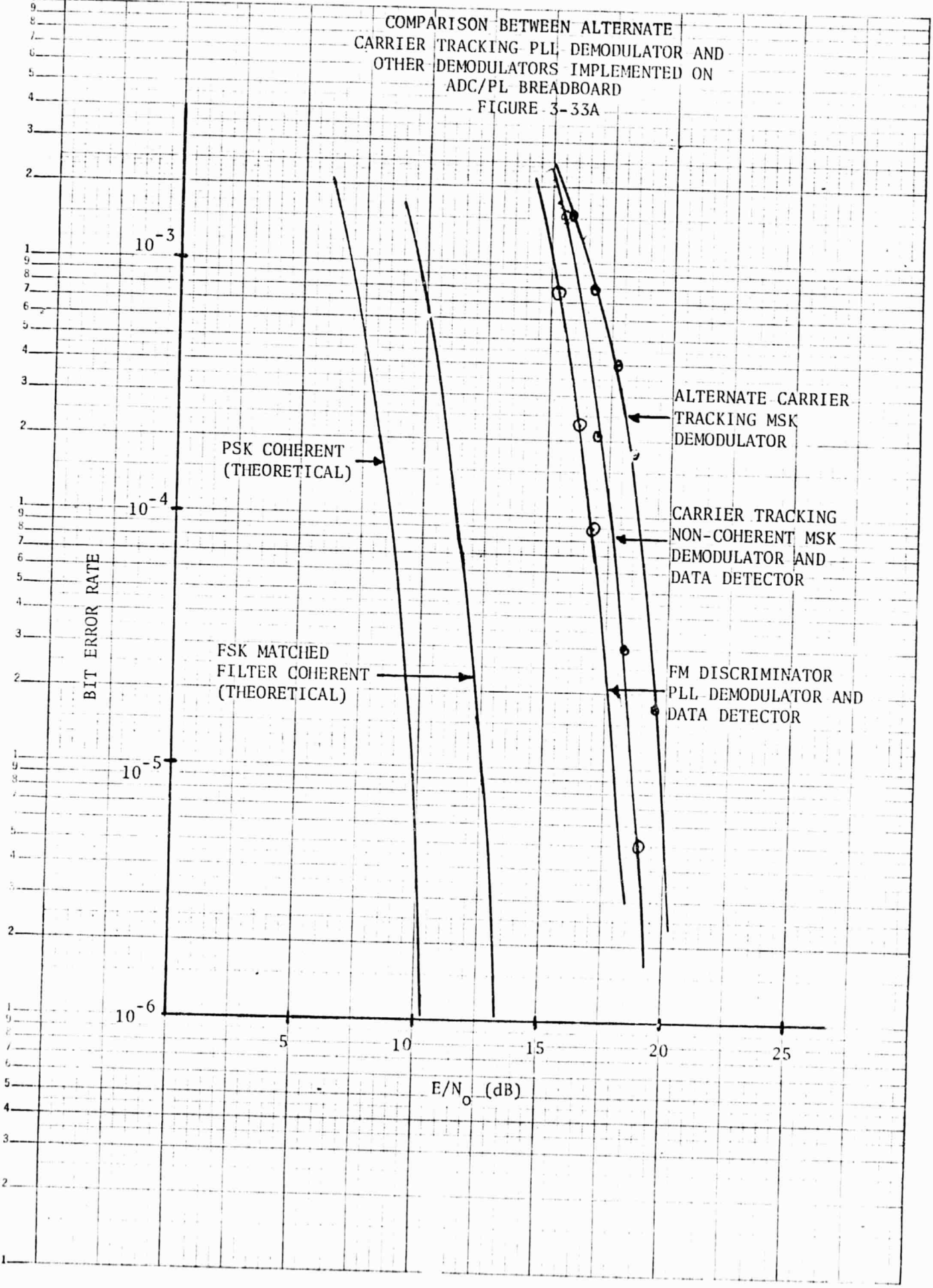
where $\overline{\phi^2_{no}}$ = VCXO mean square output phase jitter seen at the reference port of the phase detector.

$(SNR)_L$ = Signal-to-noise ratio in the tracking noise bandwidth of the carrier tracking phase lock loop.

(1) Gardner, F.M., "Phaselock Techniques", pg 21, Wiley, New York, 1966

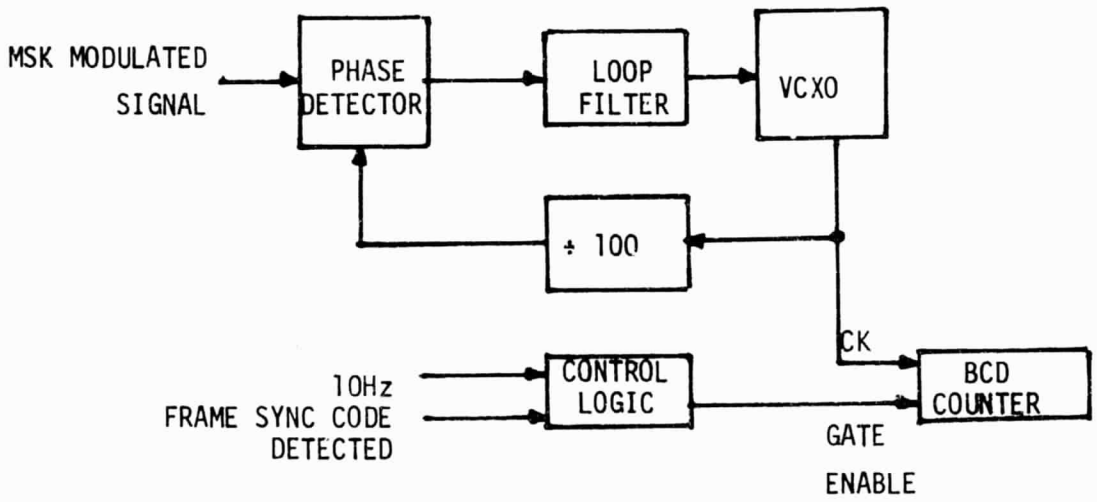
COMPARISON BETWEEN ALTERNATE CARRIER TRACKING PLL DEMODULATOR AND OTHER DEMODULATORS IMPLEMENTED ON ADC/PL BREADBOARD

FIGURE 3-33A



BLOCK DIAGRAM
FREQUENCY MEASUREMENT TECHNIQUE

Figure 3-34



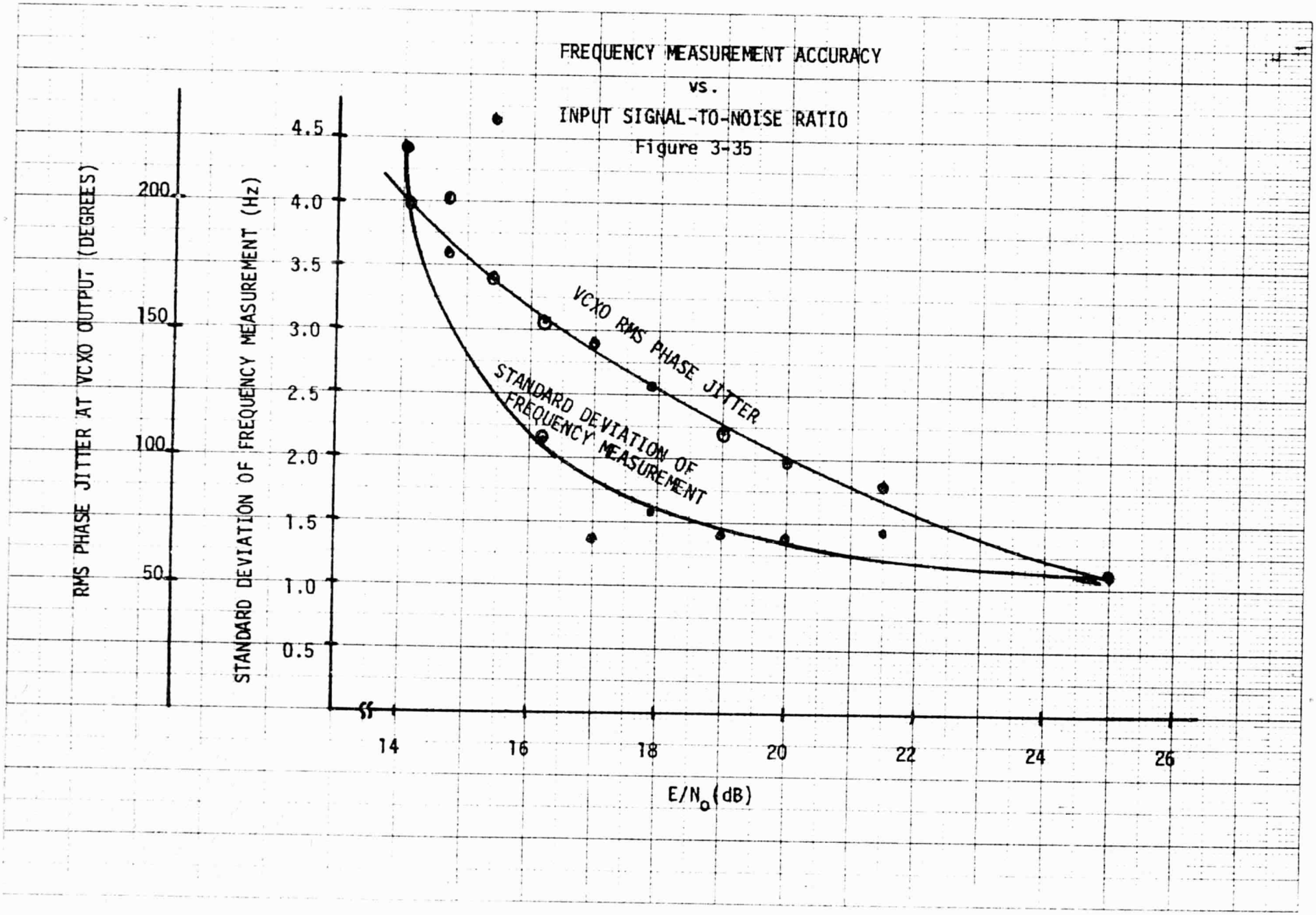
The root mean square or rms phase jitter at the VCXO output, because of the divider network, is 100 times the rms phase jitter seen at the phase detector reference point, or

$$\phi_{rms_{VCXO}} = \sqrt{\frac{100}{2(SNR)L}}$$

The accuracy obtainable with the frequency measurement circuit is controlled by the amount of phase jitter present at the VCXO output since phase excursions exceeding $\pm 360^{o}$ result in the BCD counter incrementing or decrementing one count from the true or proper count. This, in turn, means the frequency measurement is controlled by the signal-to-noise ratio in the noise bandwidth of the phase lock loop.

Figure 3-35 depicts the dependency of the frequency measurement accuracy on the signal-to-noise ratio. Two curves are plotted in Figure 3-35. One curve plots the calculated rms phase jitter at the output of the VCXO, using the above equation, and the other curve plots the measured standard deviation of the frequency measurement. Both curves are plotted as a function of the incoming E/N_o ratio, which is no more than the incoming signal-to-noise ratio as measured in a noise bandwidth equal to the bit rate of 320 Hz. The use of the E/N_o ratio in plotting the curves is simply to allow the data to be easily compared with the bit error rate curves to provide a means of analyzing the overall performance of the phase lock loop. It is noted that the two curves track one another, as expected, at the higher E/N_o readings. But for E/N_o ratios below approximately 16 dB, the standard deviation in the frequency measurement begins exponentially increasing. It is also noted that the frequency measurement accuracy never approaches the design goal of 0.1 Hz. In fact, with no noise input at all, the standard deviation of the frequency measurement was found to be 0.15 Hz. The standard deviation readings were calculated from 100 data points for each E/N_o setting, and although not an overly large sample, the 100 points do provide an adequate base for deriving statistical data such as the standard deviation of the frequency measurements.

The results of the frequency measurement test are admittedly disappointing. In fact, it appears that with E/N_o settings below about 16 dB, the measurement accuracy approaches that obtained on the RAMS instrument - $\pm$ 1Hz. The test was run at baseband - using the digital MSK modulator and bypassing the Communications Link Simulator - to avoid frequency drift problems incurred at the higher frequencies. The problem appears to be one of excessive phase


FREQUENCY MEASUREMENT ACCURACY
vs.
INPUT SIGNAL-TO-NOISE RATIO
Figure 3-35
RMS PHASE JITTER AT VCXO OUTPUT (DEGREES)
200
150
100
50
STANDARD DEVIATION OF FREQUENCY MEASUREMENT (Hz)
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
VCXO RMS PHASE JITTER
STANDARD DEVIATION OF FREQUENCY MEASUREMENT
14
16
18
20
22
24
26
E/N0 (dB)

excursions at the output of the VCXO. As an example suppose that the presence of a given data bit - and all frequency measurements were conducted in the presence of data modulation - resulted in a droop of 10^{o} due to the phase lock loop trying to pull from the carrier to the mark or space frequency. Because of the divide - by - 100 network, the VCXO would show a phase excursion of 1000^{o} - or several cycles of frequency pull. This phenomenon will average out to some degree since the next transition in the data will result in a phase excursion or frequency pull in the opposite direction. Also, the rms phase jitter due to noise is extremely high at the output of the VCXO - again due to the divide - by - 100 network. At an E/N_o of 16 dB, for example, the calculated rms phase jitter at the VCXO is 160^{o}. This is clearly excessive in light of the fact that a phase excursion of $\pm 2\pi$ results in a measurement error of 0.1 Hz. If the noise is truly unbiased, the phase noise excursions will, on the average, have zero mean. Nevertheless, errors can certainly be anticipated with this level of noise.

In conclusion, it is evident that a multiplicative ratio of 100 is excessive if a 0.1 Hz frequency resolution is required over reasonable settings of E/N_o. The only solution is to reduce the multiplicative ratio and measure the frequency for a longer time - which will degrade the temporal efficiency of the system unless the added time is also required to complete the transmission of data. The key finding in this test is that the measurement accuracy is not a simple fallout of the circuit implementation, but is highly dependent on the incoming signal-to-noise ratio. The implementation of the frequency measurement circuitry and the resulting accuracy to be expected must then be based not only on the maximum times allowable for the measurement but on the signal strength expected as well.

F. THROUGHPUT TEST RESULTS

The throughput tests served to summarize the results of the tests conducted on the chirp-z transformer and non-coherent demodulator/data detector. The test involved all components of the ADC/PL breadboard and served to show the overall level of performance achievable with a chirp-z transformer search unit and a non-coherent demodulator/data detector. The digital MSK modulator in the MSK Transmitter Simulator was used to generate the MSK modulated signal. The signal was then routed through the Communications Link Simulator, detected and assigned to the Receive Channel Simulator in the Search Subsystem Simulator, demodulated and detected by the non-coherent demodulator/data detector in the Receive Channel Simulator, and verified for proper data reception in the data

checker housed in the MSK Transmitter Simulator.

Figure 3-36 shows the probability of successfully receiving a message as a function of E/N_o, where a successful message reception is defined to be one which was detected by the Search Subsystem Simulator and demodulated and detected without bit errors in the Receive Channel Simulator. Each data point on the curve is comprised of 1000 message transmissions. The message format used in the throughput tests is shown in Figure 3-37. It is of interest to compare the test results to the results expected using the performance data from the individual chirp-z transformer and non-coherent demodulator/data detector tests. The probability of success is defined to be the probability that a message is detected by the chirp-z transformer times the probability that the message is demodulated and detected without bit error by the non-coherent demodulator/data detector, or

$$P_s = P_D^T(1-P_E^T)$$

where P_s = probability of successfully receiving a message
P_D^T = probability of detecting the presence of the transmission during the CW preamble
P_E^T = probability of error in one or more of the data bits for a given message

The probability of detecting the presence of a transmission during the CW preamble P_D^T is a function of the length of the CW preamble, since the length governs how many attempts can be made at detecting the transmission. The CW preamble length was set to 73 bit periods, or 228 milliseconds. Since each spectral sweep in the chirp-z transformer requires only 6.25 milliseconds, a total of 36 attempts are available during the 228 millisecond preamble. P_D^T may then be expressed as

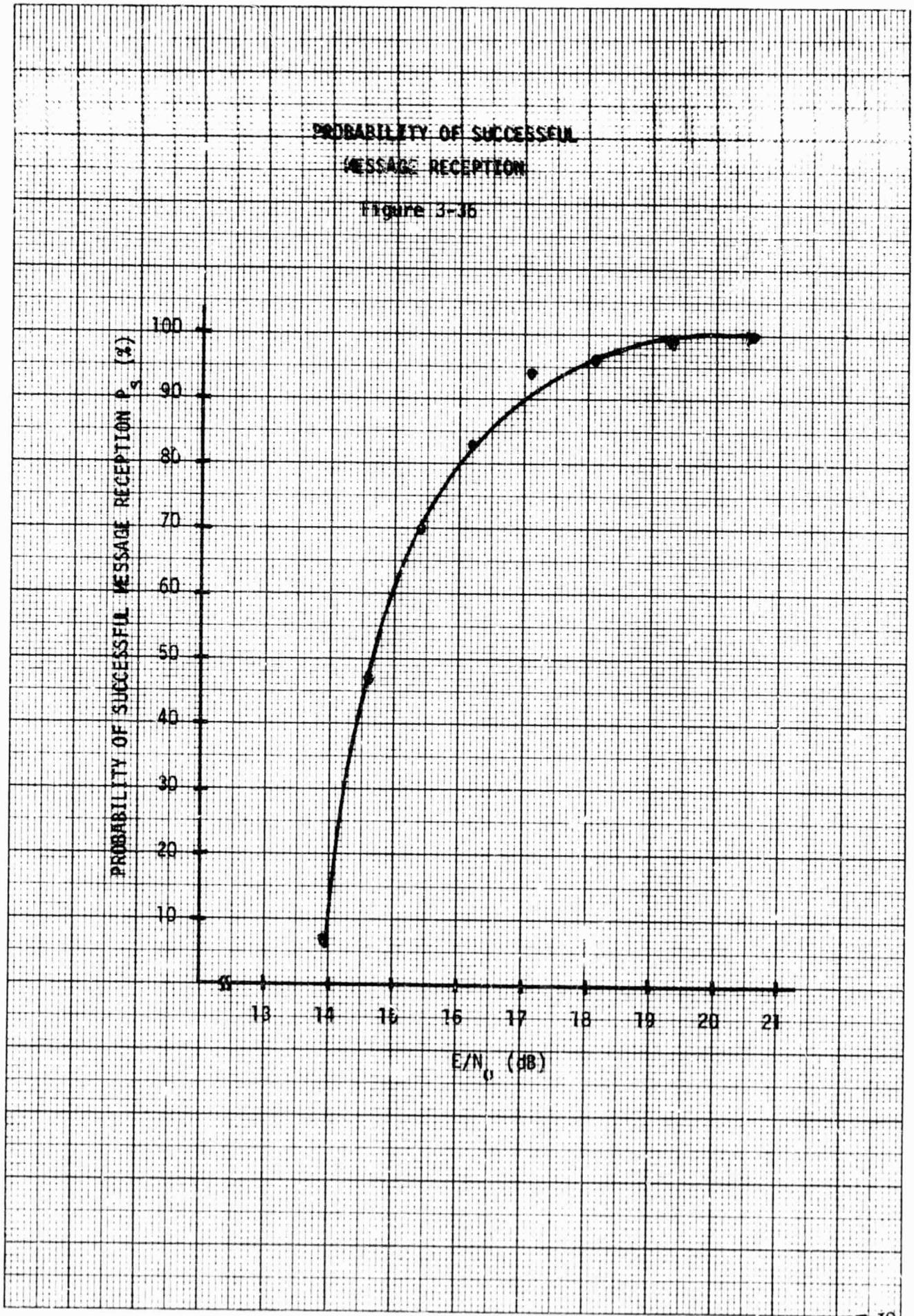
$$P_D^T = 1 - (1-P_D)^{36}$$

where P_D = probability of detecting the presence of a transmission during a given spectral search.

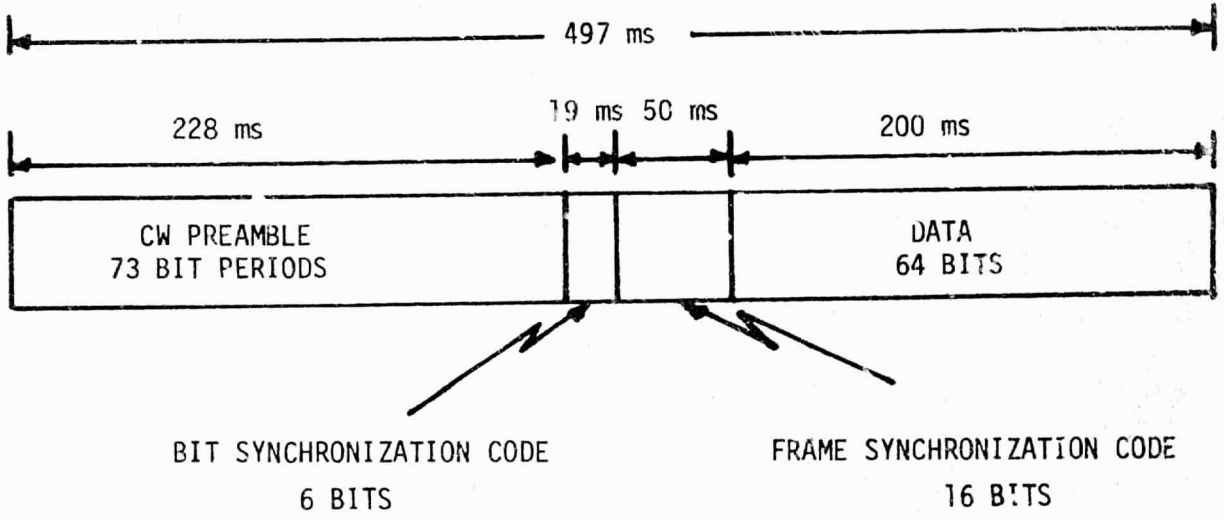
The probability of error in one or more of the data bits recovered P_E^T may be expressed as

PROBABILITY OF SUCCESSFUL
MESSAGE RECEPTION

Figure 3-36



MESSAGE FORMAT FOR ADC/PL BREADBOARD
THROUGHPUT TEST
Figure 3-37



$$P_E^T = 1 - (1-P_E)^N$$

where P_E = bit error rate

N = total number of data bits contained in a message

From Figure 3-37 it is seen that including the 16 bit synchronization code there are a total of 80 bits transmitted each message.

The probability of successfully receiving a message then is

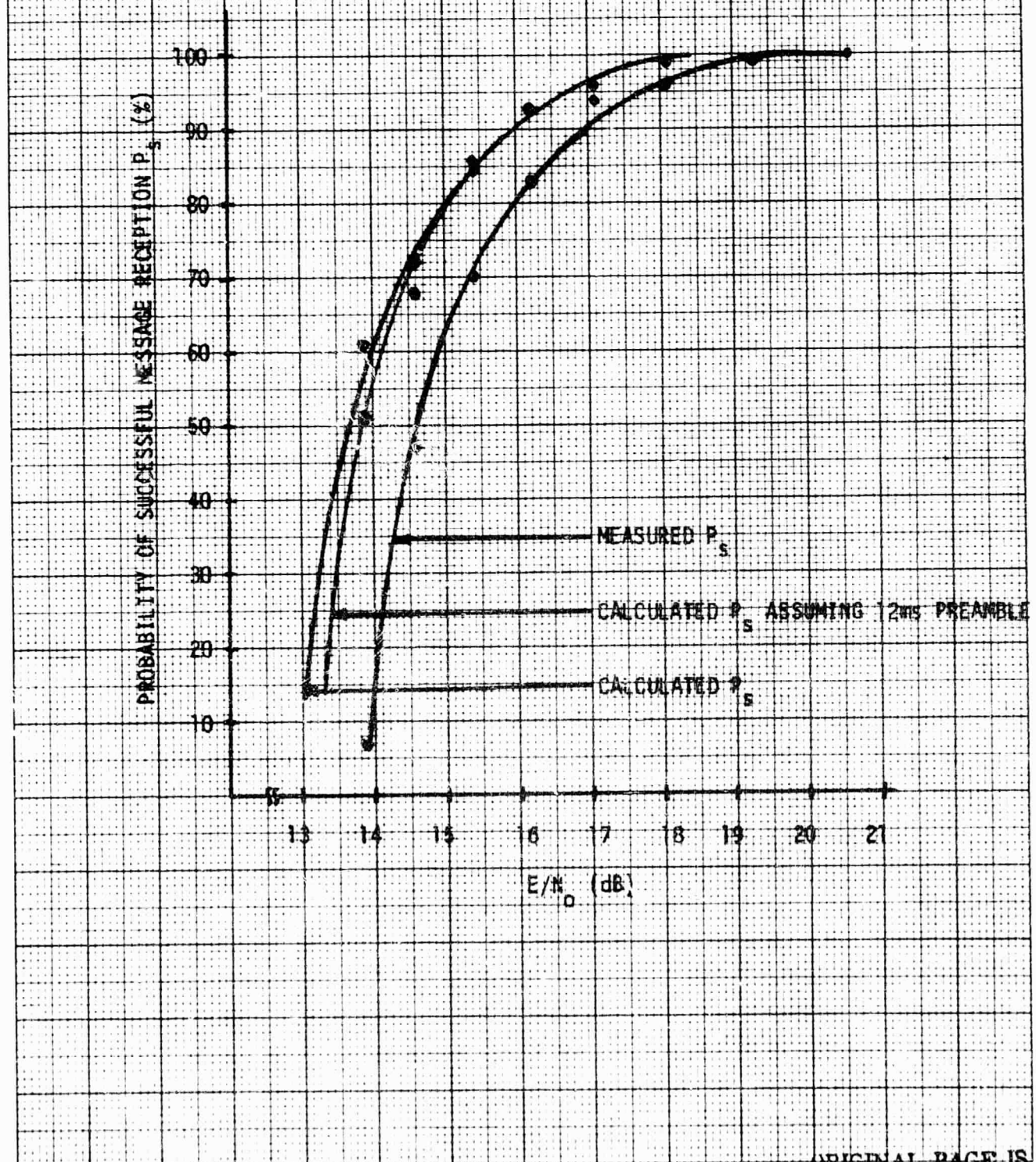
$$P_s = [1 - (1-P_D)^{36}][(1-P_E)^{80}]$$

Note that the above equation expresses the overall probability of success in terms of just the chirp-z transformer probability of detection and the bit error rate of the non-coherent demodulator/data detector.

Figure 3-38 shows a comparison between the measured probability of successful message reception, which is a repeat of the curve shown in Figure 3-36, and the calculated probability of successful message reception using the above equation. Because of the excessive length of the preamble, the calculated probability of success is totally controlled by the bit error rate of the non-coherent demodulator/data detector. A third curve is also plotted in which the calculations assume a preamble length of only 12.5 milliseconds, or four bit periods. For this preamble length the chirp-z transformer has only two tries available to detect the presence of a transmission. As can be seen, the curve is effected very little by shortening the length of the preamble, meaning the overall probability of successfully receiving a message is still governed by the bit error rate performance of the non-coherent demodulator/data detector.

COMPARISON BETWEEN MEASURED AND CALCULATED CURVES OF THE PROBABILITY OF SUCCESSFUL MESSAGE RECEPTION

Figure 3-38



SECTION IV

ANALYSIS OF RESULTS

A. INTRODUCTION

This section summarizes the findings of the breadboard tests described in Section III, develops a sample ADC/PL system from these summarizations, and discusses the feasibility of conducting throughput tests using the Landsat II satellite. The findings of the breadboard tests are summarized in terms of the impact MSK modulation and chirp-z transformers would have on future data collection/ position location systems. The thrust of both MSK modulation and chirp-z transformers is to improve the temporal and spectral efficiency of a data collection system. The tests on the ADC/PL breadboard were conducted to both confirm the predicted improvements in time and bandwidth that these two technologies would provide and to characterize other pertinent parameters such as signal-to-noise performance. Two subsections are presented to summarize the impact each technology brings to ADC/PL systems - one subsection for the impact of MSK modulation and one subsection for the impact of chirp-z transformers.

The sample system is developed in two parts. First the Random Access Measurement System (RAMS) is analyzed from the standpoint of what user population could the instrument have accommodated had MSK modulation and the chirp-z transformer been used - holding all parameters constant except for transmitter output power and the length of the CW preamble. An ADC/PL system is then developed in which all parameters are adjusted to yield a system which can handle a large user population in the field of view of the satellite. A total of 2500 platforms in the field of view of the satellite is obtained with the sample system using MSK modulation, a chirp-z transformer implemented search unit, 10 watt platform transmitters, and a 100 KHz frequency band.

The addition of r-f equipment to the ADC/PL breadboard to implement throughput demonstration tests using the Landsat II Satellite is next discussed. Although the down-link from Landsat II presents problems which are not resolved in this report, a typical up-link, using the Landsat II up-link receive frequency of 401.55 MHz as an example, is presented in detail.

B. IMPACT OF THE CHIRP-Z TRANSFORMER ON ADC/PL SYSTEMS

Fundamentally, there is no need at all for a unique search unit in an ADC/PL receiving unit since the receive channels themselves can serve to

search the receive band for the presence of signals. A search unit is used then only because it can provide improvements in the overall characteristics of the ADC/PL system, and the key improvement to be made is in the search time required to locate a transmission. Reducing the required search time reduces the length of the CW preamble required on each transmission and thus improves the temporal efficiency of the transmissions. If a separate search unit can be used to reduce the required search time, it is important that other parameters such as probability of detection vs. signal-to-noise ratio, bin spreading vs. dynamic range, false alarm rate, etc. be investigated to assure that penalities such as increasing the transmit power, increasing the number of receive channels to handle the false alarm load, etc. do not result from using the separate search unit. Table 4-1 summarizes the findings of the tests conducted on the chirp-z transformer search unit housed in the ADC/PL breadboard.

Table 4-1 is divided into two sections - implementation investigations and parameter investigations. Several implementation type questions arose during the development of the ADC/PL breadboard - such as whether or not apodization is desirable, whether the use of the imaginary as well as the real coefficients in the threshold detection process provides any improvements, what the implementation limits are on the size of the analyzing bandwidth, etc. These type questions are answered in the implementation investigation section of Table 4-1. Apodization was found to be not only desirable but necessary in systems which require dynamic range capabilities in excess of 16 dB to limit the amount of bin spreading that occurs on strong signals. The use of both real and imaginary coefficients was found to provide approximately 2 dB improvement in the probability of detection per spectral scan over that obtainable using only real coefficients. The false alarm rate for the chirp-z transformer was found to be adjustable over a range of 10^{-4} to 10^{-6} without degrading the shape of the probability of detection plots.

The limitations on the size of the frequency cell or analyzing bandwidth in the chirp-z transformer are mainly in the manufacturing process rather than any theoretical limits. The chirp-z transformer used on the ADC/PL breadboard is a 500 cell transversal filter and represents the limit that CCD technology has reached in terms of the number of cells that can be placed on a substrate for high dynamic range analog type applications. The problem in creating longer cell lengths is the degradation in the charge transfer efficiency incurred due to the need to "bend" the cell pattern into rows in order to fit onto the substrate. It is at the corners or "bends" in the cell pattern that

Table 4-1

SUMMARY OF TESTS INVESTIGATING THE USE OF
CHIRP-Z TRANSFORMERS IN ADC/PL APPLICATIONS

IMPLEMENTATION INVESTIGATIONS

REAL vs. COMPOSITE COEFFICIENTS-------	Composite coefficients provide approximately 2dB improvement in detection performance
APODIZATION vs. NON-APODIZATION ------	Apodization greatly improves bin spreading without sacrificing detection performance
FALSE ALARM RATE ----------	Detection performance well behaved for false alarm rate range between 10^{-4} and 10^{-6}.
ANALYZING BANDWIDTH ----------	Present state of technology limits analyzing bandwidth to no less than 0.4% of search band.

PARAMETER INVESTIGATIONS

PROBABILITY OF DETECTION ----------	$\geq$ 99% for SNR $\geq$18dB
DYNAMIC RANGE ----------	30 dB
BIN SPREADING FOR 30 dB DYNAMIC RANGE-	$\leq$5 frequency bins
SEARCH TIME----------	(Analyzing bandwidth)$^{-1}$
MUTUAL INTERFERENCE FREQUENCY BAND----	3 frequency bins for 30 dB dynamic range 2 frequency bins for 10 to 20 dB dynamic range

NOTE: The above parameters assume an apodized chip, the use of composite coefficients, and a false alarm rate of 10^{-5}

the degradation occurs. The use of 500 cells in the transversal filter means the search band will be divided into 250 frequency bins. The analyzing bandwidth then can be no smaller than 0.4 % of the total search band.

The parametric data taken on the chirp-z transformer is summarized in the second half of Table 4-1. A probability of detection greater than 99% was observed for signal-to-noise ratios in the analyzing bandwidth equal to or exceeding 18 dB. The transformer was well behaved over a 30 dB range of signal input, and signals at the upper end of the 30 dB range resulted in no more than five frequency bins exceeding threshold. The frequency separation between adjacent signals required to prevent bin spreading from masking one of the incoming signals depends on the dynamic range or power separation between the two signals. The minimum frequency separation allowable for a 30 dB dynamic range system is three frequency bins, while for a 10 to 20 dB dynamic range system the minimum allowable separation is two frequency bins.

Table 4-2 shows an instructive comparison between the parameters of the RAMS search subsystem and the performance parameters that would have been obtained had a chirp-z transformer been used. The chirp-z transformer configuration assumed in Table 4-2 is a 500-cell apodized transformer with both real and imaginary coefficients used in the detection process. As can be seen, the chirp-z transformer excels in every viable parameter. The most drastic improvement is in the search time required to detect the presence of a signal. The chirp-z transformer also offers a 3 dB improvement in the minimum detectable signal level. For the 10 dB dynamic range of the RAMS system, the chirp-z transformer also offers an improvement in the mutual interference bandwidth, or that frequency separation required to distinguish the presence of two time overlapping signals.

C. IMPACT OF MSK MODULATION ON ADC/PL SYSTEMS

The attraction of MSK modulation with regard to ADC/PL type applications is the extremely efficient use of bandwidth the modulation format displays while providing a bit error rate demodulation/detection performance equivalent to PSK modulation. To obtain a bit error rate equivalent to PSK, it is necessary to use a rather elaborate coherent receiver. However, if loss in demodulation and detection performance can be accommodated, a simpler non-coherent demodulation/detection scheme can be utilized whereby the MSK signal is treated as an FSK signal. Time permitted only the design and implementation of the simpler non-coherent technique for the ADC/PL breadboard.

Table 4-2

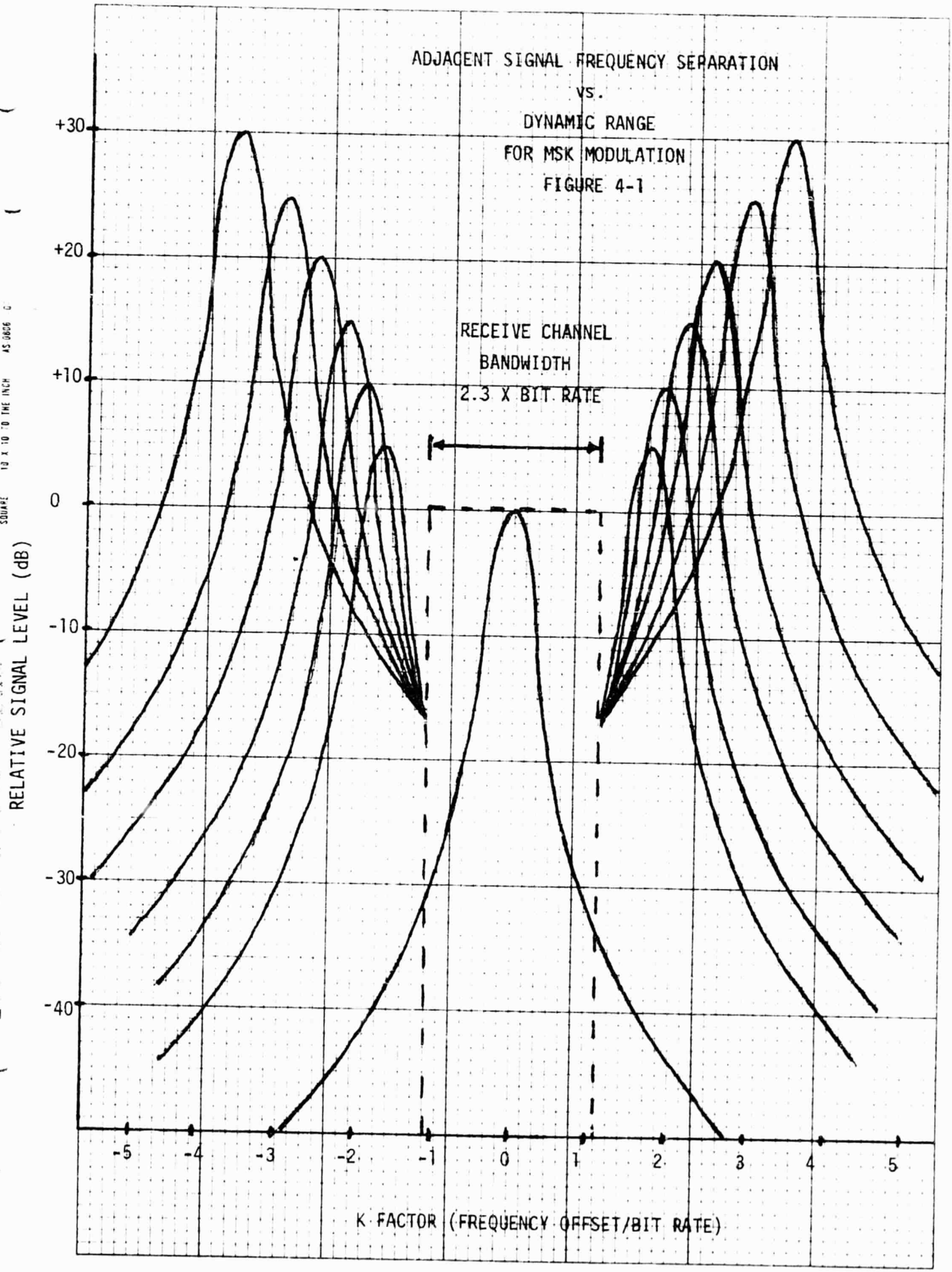
COMPARISON BETWEEN RAMS SEARCH UNIT
AND EQUIVALENT CHIRP-Z TRANSFORMER SEARCH UNIT

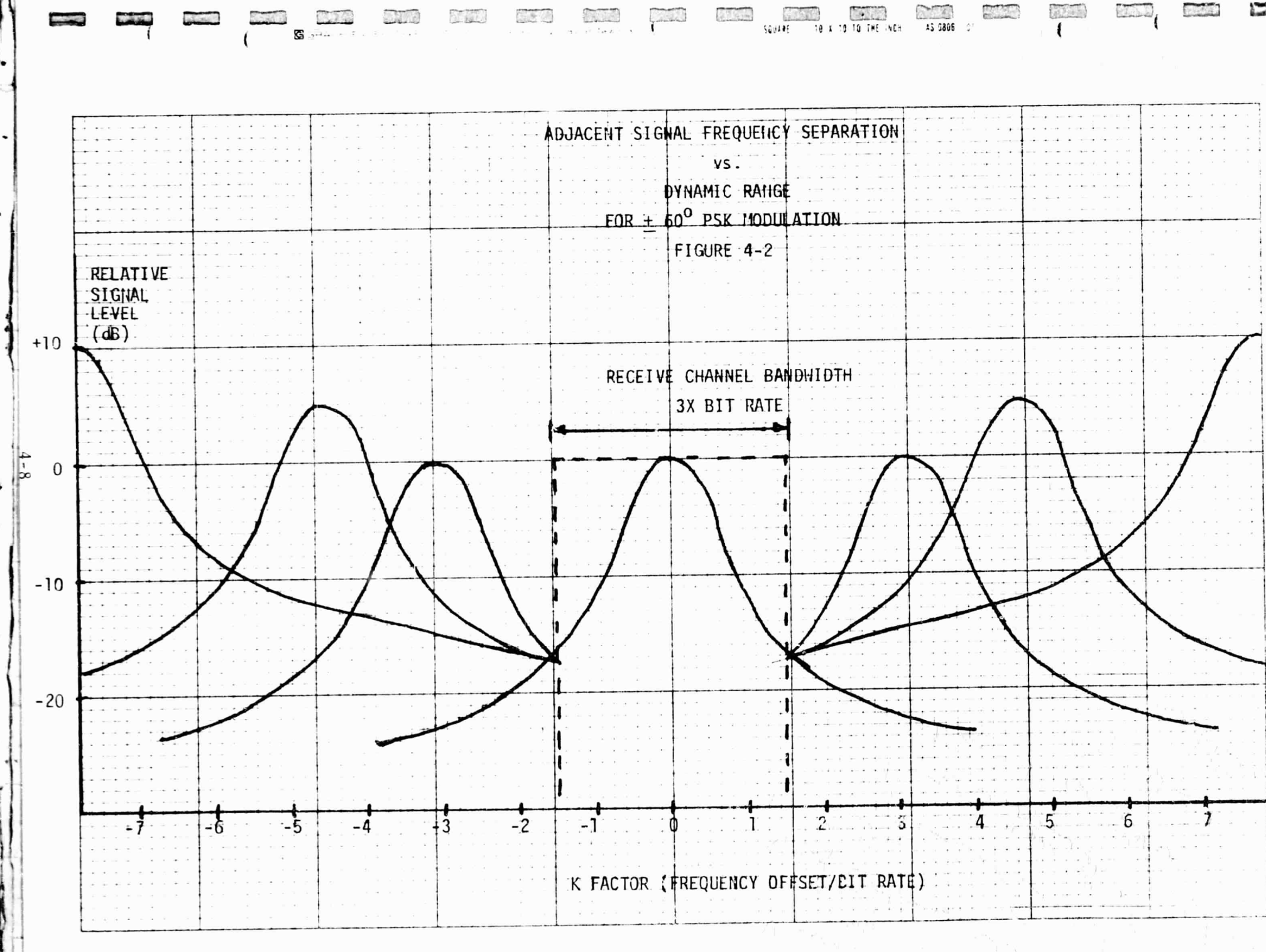
PARAMETER	RAMS	CHIRP-Z TRANSFORMER
Search Band	30 kHz	30 kHz
Analyzing Bandwidth	100 Hz	120 Hz
Search Time	132 ms	8.33 ms
Minimum Detectable Transmit Power for RAMS communication Link ($P_D \geq 99\%$)	600 mW	300 mW
Mutual Interference Band-Single-Sided (10 dB Dynamic Range)	300 Hz	240 Hz
False Alarm Rate	10^{-4}	10^{-4}

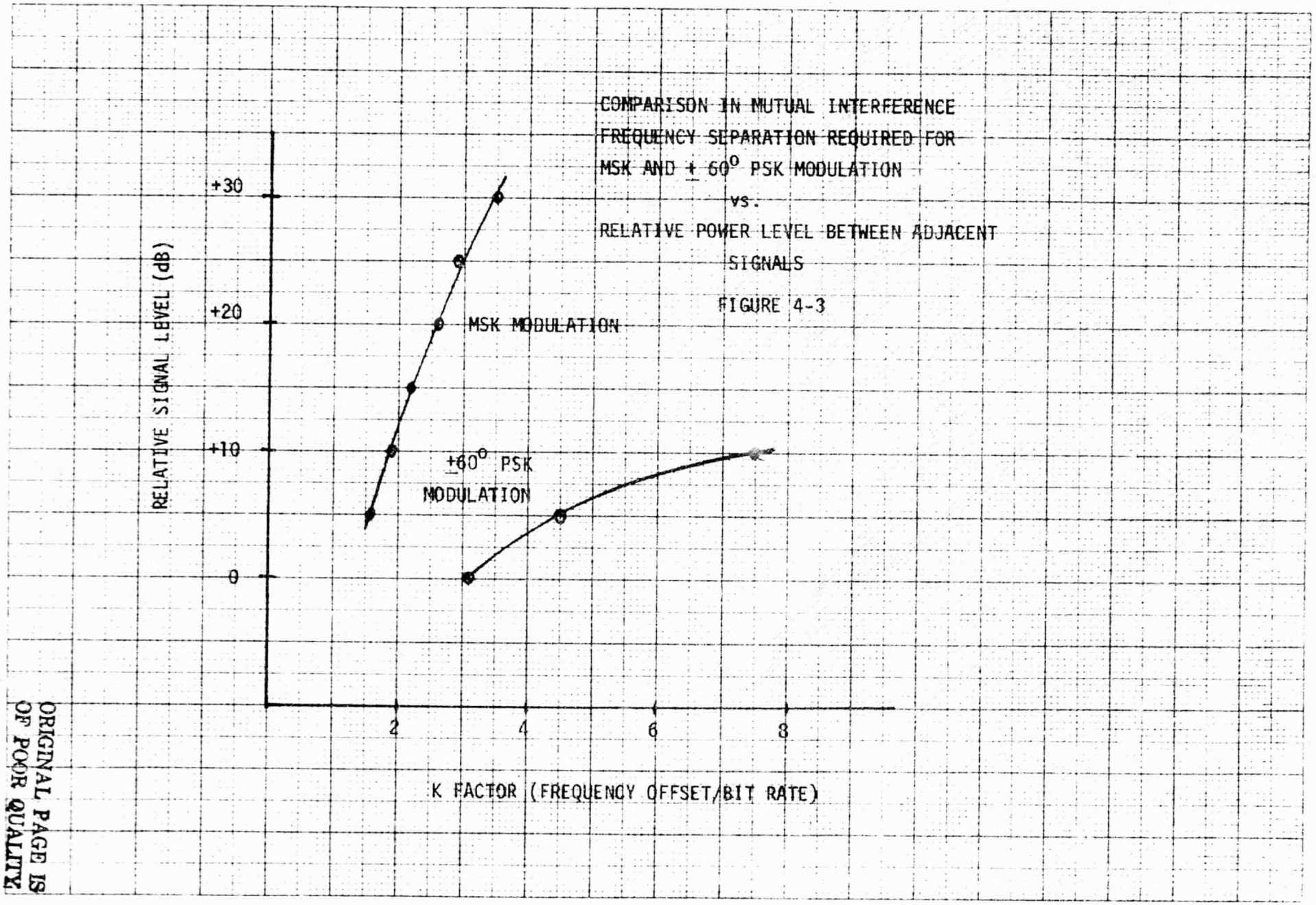
The spectral efficiency of the MSK modulation format is shown in Figure 3-28 both for linear and non-linear transmission of MSK modulated Manchester encoded data. Figure 4-1 depicts the overlap of mutually transmitting MSK modulated Manchester encoded signals as a function of relative signal level and offset in frequency. The diagram is constructed to display the offset in frequency required - which is plotted using the K factor, where K is the ratio of the frequency offset to the data bit rate of the modulated signal - to prevent mutual interference between adjacent signals. The definition of mutual interference is obtained by considering adjacent signals as sources of noise. For a bit error rate of 10^{-4}, the non-coherent MSK demodulator/data detector requires an E/N_o of 17.5 dB. Adjacent signals must then be displaced in frequency so that the amount of spectral energy that leaks into the passband of a receive channel is 17.5 dB below the power of the signal being received. An ideal brick-wall filter of double-sided bandwidth 2.3 times the data rate is placed about the MSK signal being received, and adjacent signals are then positioned in frequency so that their spectral skirts fall at least 17.5 dB below the peak of the signal spectra being received. The received signal is assumed to be at the lowest expected receive signal level. The spectral shape of the MSK modulation is taken as the envelope of the spectrum shown in Figure 3-28.

The very same set of curves are plotted in Figure 4-2 for $\pm 60^{o}$ PSK modulated Manchester encoded data rather than MSK modulated Manchester encoded data. Here an ideal brick-wall filter of double-sided bandwidth three times the data rate is assumed, which will pass approximately 92 percent of the PSK signal energy - as opposed to the brick-wall filter of 2.3 times the data rate for MSK modulation which passed over 99% of the signal energy. Again, the received signal is assumed to be at the lowest expected receive signal level and the adjacent PSK modulated signals are positioned in frequency so that their spectral skirts fall at least 17.5 dB below the peak of the signal being received.

Figure 4-3 summarizes the frequency separation plots of Figures 4-1 and and 4-2 by plotting the mutual frequency interference band as a function of dynamic range both for $\pm 60^{o}$ PSK and MSK modulation. Again the K factor, which is the frequency offset divided by the bit rate or data rate clock, is used to remove the dependency of the curves on the bit rate. In examining Figure 4-3 it is seen that MSK is clearly superior in terms of spectral efficiency. For a dynamic signal range of 10 dB, the K factor is approximately




ADJACENT SIGNAL FREQUENCY SEPARATION
vs.
DYNAMIC RANGE
FOR ± 60° PSK MODULATION
FIGURE 4-2
RELATIVE SIGNAL LEVEL (dB)
+10
0
-10
-20
RECEIVE CHANNEL BANDWIDTH
3X BIT RATE
-7
-6
-5
-4
-3
-2
-1
0
1
2
3
4
5
6
7
K FACTOR (FREQUENCY OFFSET/BIT RATE)



2 for MSK modulation and approximately 7.5 for $\pm 60^{o}$ PSK. In the RAMS instrument, it was found that two signals 10 dB apart in signal level had to be separated at least 800 Hz to prevent mutual interference, which agrees with the plot shown in Figure 4-3. For a dynamic range of 30 dB, MSK requires but a K factor separation of 3.5, which is still less then half that required for $\pm 60^{o}$ PSK for a 10 dB dynamic range.

Table 4-3 summarizes the findings of the investigations conducted on MSK modulation. The non-coherent MSK demodulator/data detector demonstrated an E/N_o performance approximately 2.5 dB worse than that obtained on the RAMS instrument. In all other aspects, however, the MSK modulation format was clearly superior. The frequency separation required to prevent mutual interference between adjacent signals is clearly superior to the $\pm 60^{o}$ PSK format used on RAMS. MSK modulation is also very tolerant of transmitter designs for transmitting the modulation. Linear r-f amplifier and power stages are not required to preserve the spectral properties of MSK modulation. In fact, as shown in Figure 3-28, there is little if any discernable difference in the spectrum of MSK modulation output from a hard limiter as compared to the MSK modulation spectrum prior to limiting. It was also found that non-linear processing of MSK modulation resulted in no marked difference in performance of the non-coherent MSK demodulator/data detector.

D. SAMPLE SYSTEM

The purpose of this section is to derive a sample ADC/PL system utilizing MSK modulation and a chirp-z transformer search unit to illustrate the benefits derived from these technologies. The primary thrust in considering the use of MSK modulation and a chirp-z transformer search unit is to increase both the spectral and temporal efficiency of ADC/PL type systems. ADC/PL systems are typically limited both in time and bandwidth, and these two restrictions limit the population serviceable by the ADC/PL system. Any increase in the efficiency with which time and bandwidth are utilized will result in a larger serviceable population. Future ADC/PL system such as search and rescue networks, off-shore ship monitoring, etc. stress the need for larger and larger

Table 4-3

SUMMARY OF TESTS INVESTIGATING THE USE OF
MSK MODULATION IN ADC/PL APPLICATIONS

COHERENT DEMODULATOR E/N_o PERFORMANCE	Coherent demodulator was not implemented
NON-COHERENT DEMODULATOR/DATA DETECTOR E/N_o PERFORMANCE	BER $\leq 10^{-4}$ for $E/N_o \geq 17.5$ dB
MUTUAL INTERFERENCE FREQUENCY SEPARATION	1.9 X bit rate for 10 dB dynamic range 2.6 X bit rate for 20 dB dynamic range 3.5 X bit rate for 30 dB dynamic range
SPECTRAL OCCUPANCY	99% of spectrum contained within double-sided bandwidth of 2.3 times the data rate.
TRANSMITTER REQUIREMENTS	Class C amplifiers may be used without degrading spectral efficiency of the signal or degrading the demodulation performance of the non-coherent demodulator. Also, non-coherent generation of MSK at an r-f frequency does not degrade the demodulation performance of the non-coherent demodulator.

user populations - even at the cost of degrading other parameters within the system, such as transmit power required, if necessary. The tests conducted on the ADC/PL breadboard showed that with the exception of the E/N_o performance of the non-coherent MSK demodulator, all vital parameters defining an ADC/PL system are improved with the MSK modulation and chirp-z transformer technologies.

To begin, the RAMS system will be briefly examined to demonstrate the impact on the serviceable population the use of a chirp-z transformer search unit and MSK modulation would have had - holding all parameters constant except for transmit power and the length of the CW preamble in the transmitted message. It was shown in a paper[1] concerning the statistical performance of RAMS that a probability of success of 58 percent on a given message was adequate to meet the requirements of the TWERLE Experiment. The probability of success was derived as

$$P_s = (1-P_I)\ P_{EQP}.$$

where P_I = probability of mutual interference in frequency and time

P_{EQP} = composite probability of a RAMS processing error. (data bit error, failure to detect the signal in the search unit, etc.)

To simplify the discussion, it will be assumed that the composite probability of a RAMS processing error is kept constant. This will necessitate increasing the transmitting power of the balloon platforms because of the loss in E/N_o performance exhibited by the non-coherent demodulator/data detector as compared to the $\pm 60^o$ PSK demodulator/data detector. The composite probability of a RAMS processing error was shown[1] to be 72.3 percent, which yields

$$P_s = .50 = .723\ (1-P_I)$$

which in turns yields, for P_I

$$P_I = .198$$

The expression for P_I was shown[1] to be

$$P_I = 1 - (1- 2\tau_1/T\ \ 2\Delta f/F)^{N-1}$$

(1) J.L. Coates, "The NIMBUS F Random Access Measurement System", IEEE Trans. on Geoscience Electronics, Vol GE-13, Jan 1975, pp 18-27

where

N = number of platforms in satellite field-of-view

F = platform dispersion band = 30 kHz

T = time between successive transmissions for i^{th}/ platform = 60 seconds

Δf = frequency band of mutual interference

τ_1 = platform transmission time = 640 milliseconds + CW preamble

For the RAMS instrument as constructed, a 320 millisecond preamble was required to provide enough time for detecting the signal in the search unit - which sets τ_1 to 960 milliseconds. Also Δf, for a 10 dB dynamic range in received signal power as specified for RAMS, was 800 Hz. To keep P_I at .198, N can be no greater than 129. If a frequency band of mutual interference of 500 Hz is selected, which was the specified but not achieved interference band for RAMS, N increases to the TWERLE goal of 200.

If the chirp-z transformer were used in RAMS, however, the CW preamble could be reduced to 8.33 milliseconds, which reduces τ_1 to 648.33 milliseconds. Also, if MSK modulation were used, the band of mutual interference could be reduced to 190 Hz, which is a K factor of 1.9. With these changes in τ_1 and Δf, N can be as large as 800 without exceeding 0.198 for the probability of mutual interference. The number of serviceable platforms has been increased by a factor of over six.

Although interesting, the application of MSK modulation and the chirp-z transformer to the RAMS instrument without altering any parameters other than the length of the CW preamble or the transmitted power does not maximize the number of platforms such a system could service if structured differently. Table 4-4 depicts an ADC/PL system which has been structured to yield a high number of serviceable platforms in the field of view. A system bandwidth of 100 KHz is assumed, and it is further assumed that the platform population is evenly distributed throughput the band by doppler, crystal drift, different crystal center frequencies, etc. An MSK modulation format is used, a communications link equivalent to the worst case RAMS TWERLE link is assumed, and a dynamic range of 20 dB is specified as the maximum separation in signal levels as received at the satellite. The platform transmit power is specified at 10 watts.

Table 4-4

ADC/PL Sample System

System Bandwidth	100 kHz
Platform Transmit Power	10 Watts
Platform Modulation Format	MSK (Manchester Encoded)
Link Losses for Low Polar Orbiting Satellite (Including Antennas and Receiver Noise Figure)	160 dB_{max}
Dynamic Range (Including Antenna Misorientations)	20 dB
Search Unit Implementation	Chirp-Z Transformer
Search Unit Analyzing Bandwidth	400 Hz
Search Unit Search Time	2.5 ms
Minimum Signal-to-Noise Ratio In Search Unit Analyzing Bandwidth	24.7 dB
Minimum Probability of Detection in Search Unit	100%
Bit Rate	1.3 KBps
Minimum E/N_o	19.5 dB
Demodulator Implementation	Non-Coherent
Maximum Bit Error Rate	10^{-5}
Message Length (64 data bits, 16 bit bit sync, 16 bit frame sync, 2.5 ms CW preamble)	76.3 ms
Mutual Interference Band	
Search Unit (2X Analyzing Bandwidth = 800 Hz)	3.4 kHz
Demodulator (2.6 X Bit Rate = 3.4 kHz)	
Satellite View Time ($\geq 30^{o}$ Latitude, 35^{o} field of view)	8 minutes min
Number of Receptions Required Per Orbit	3
Time Between Successive Transmissions of i^{th} Platform	53.33 sec.
Probability of Receiver Properly Processing Message (no bit errors, signal detected, receive channel available, etc.)	.95
Probability of Mutual Interference	.389
Number of Platforms Serviceable	2500
Probability of Successfully Receiving a Message	.58
Probability of Successfully Receiving 3 Messages Per Orbit	.95

A 500 point chirp-z transformer search unit is used in the satellite to divide the 100 KHz band into two hundred fifty 400-Hz frequency bins. For a 10 watt transmit power and the communications link assumed, a signal-to-noise ratio of 24.7 dB is available in the analyzing bandwidth of the chirp-z transformer, which gives a probability of detection of 100% with about 6.7 dB of margin. The 100 KHz band search time is the reciprocal of the analyzing bandwidth of 400 Hz - or 2.5 milliseconds. The bit rate of 1.3 KBps was selected to yield an E/N_o of 19.5 dB, which, for the non-coherent MSK demodulator/data detector, results in a bit error rate of approximately 10^{-5}. The message consists of a 16 bit synchronization code, a 16 bit frame synchronization code, 64 data bits, and a 2.5 millisecond CW preamble - for a total transmission time of 76.3 milliseconds. The mutual interference band, or the minimum allowable frequency separation between adjacent signals before mutual interference due to spectral overlap occurs, is governed by the spectrum of the MSK modulation. The MSK modulation rather than the chirp-z transformer sets the mutual interference band because of the high bit rate (1.3 KBps) as compared to the analyzing bandwidth (400 Hz) of the chirp-z transformer. For a 20 dB dynamic range, two time overlapping transmissions must be at least 3.4 kHz, or 2.6 times the bit clock, apart in frequency. The mutual interference band then is 3.4 kHz.

For position location determination it is assumed that a minimum of three message receptions per orbit for two successive orbits is marginally adequate. It is further assumed that the minimum satellite view time is 8 minutes for a latitude equal to or greater than 30°. A satellite view time of 8 minutes for a latitude of 30° or more can be shown[1] to equate to a 35° field-of-view. A low polar orbiting satellite requires in the neighborhood of 100 to 110 minutes to complete an orbit, and in this time the earth will have rotated approximately 23° in longitude. As can be seen from Figure 4-4, a 35° field-of-view will leave approximately an 11° gap in longitude within which a platform would not be seen for a period of 8 minutes or more on each of two successive orbits. This does not imply that the platform would not be seen at all, but simply that it would not be seen for an 8 minute period or more on each of two successive orbits. If the time between transmissions is low enough - less than 1 second - then two or three messages will be re-

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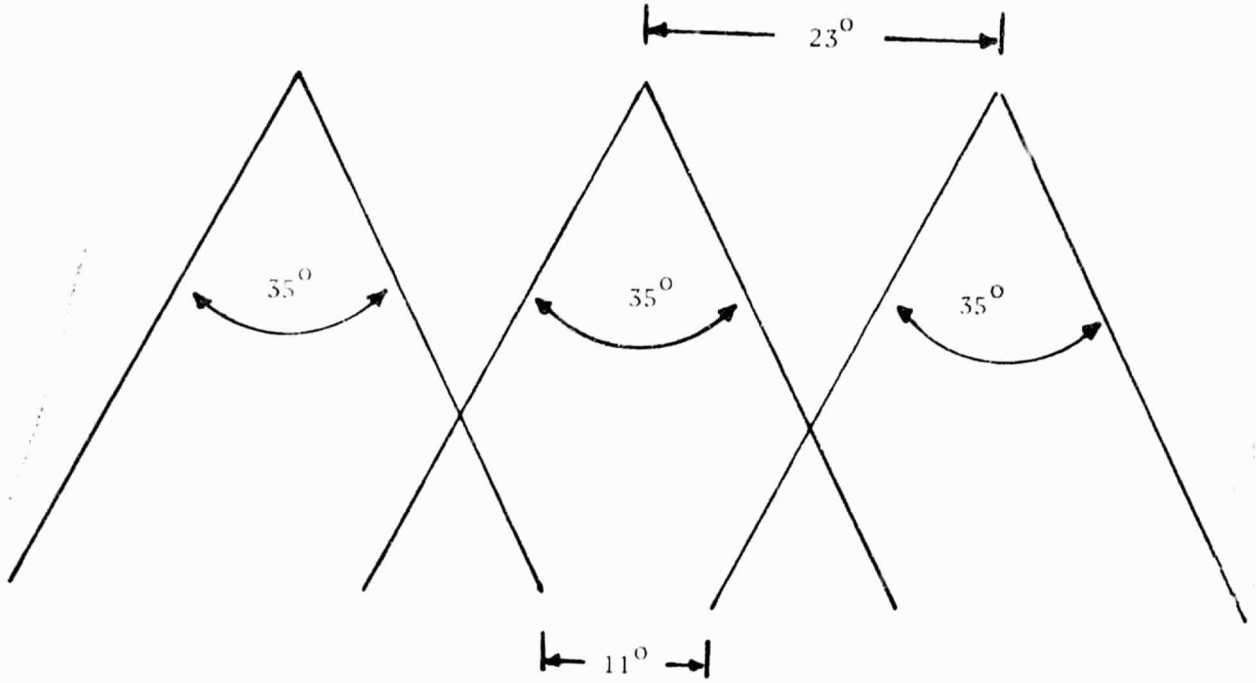
J.L. Langston, "Final Report for a Study of Satellite Emergency Locator Systems", prepared for NASA-GSFC, report U1-879110-F, May, 1977

SATELLITE COVERAGE FOR
ADC/PL SAMPLE SYSTEM
FIGURE 4-4



SINGLE ORBIT
COVERAGE AREA

ceived from a platform within the 11^{o} longitudinal gap, and the question becomes whether or not these messages were interferred with or were received with errors.

The probability of successfully receiving three or more transmissions per orbit per platform is set to 0.95. For a transmit repetition rate of 53.33 seconds, a total of 9 transmissions will be received in the 8 minute satellite view time. If the probability that three or more of these messages are successfully received is 0.95, and if it is assumed that the reception of a given message from a given platform is statistically independent from all other attempts to receive messages from the same platform, the probability of successfully receiving any one given transmission need only be 0.58 since

$$P_T = \sum_{i=3}^{9} \binom{9}{i} P_s^i (1-P_s)^{9-i}$$

where P_T = probability of receiving three or more transmissions
P_s = probability of successfully receiving any one given transmission

The probability of successfully receiving a transmission (P_s) is comprised of the probability that the message is properly processed by the receiver (detecting the signal in the search unit, having a receive channel available, recovering the data without bit errors, etc.) times the probability that the message is not mutually interferred with. The probability of properly processing the signal is set to 0.95, which is reasonable considering the high signal-to-noise ratio available in the search unit and the bit error rate of 10^{-5} in the receive channel. This then leaves the probability of no mutual interference at 0.61, or a probability of mutual interference of 0.39.

The parameters needed for deriving the number of users searviceable within the satellite field-of-view are now available. The probability of mutual interference has been previously given as

$$P_I = 1 - (1 - 2\tau_1/T \quad 2\Delta f/F)^{N-1}$$

Using the values for τ_1, T, Δf, F, and P_I presented above and listed in Table 4-4 yields a value of N of 2500.

Two key parameters, each controlled by one of the two technologies addressed in the ADC/PL breadboard - MSK modulation and chirp-z transformers, were instrumental in obtaining the large user population of 2500 within the satellite field-of-view. The chirp-z transformer implemented search unit provides a spectral search time of only 2.5 milliseconds. This extremely short search time requires an equally short CW preamble in the transmitted message format, and thus allows the message bit rate to be increased to reduce the message transmit time below 100 milliseconds. This is important in that it lowers the overall duty cycle of the platform and allows the transmit power to be increased without substantially increasing the overall power drain in the platform. The use of MSK modulation reduces the frequency band of mutual interference to only 2.6 times the data rate for no more than 20 dB separation in signal power between received signals, and thus provides a much more efficient use of the frequency band available than does PSK type modulation. It is also noted that the data rate is higher than the analyzing bandwidth of the chirp-z transformer. Although providing excessive signal-to-noise ratio, the smaller analyzing bandwidth provides a higher resolution in frequency. This is important because it reduces the frequency uncertainity of the signal location, which in turn allows the i-f bandwidth of the channel to be reduced to provide as much rejection of adjacent signals as possible. For example, it can easily be seen from Figure 4-1 that if the receive channel bandwidth is increased, the frequency separation between adjacent signals must also be increased to prevent mutual interference.

The ADC/PL sample system is intended to simply display the growth in the serviceable user population obtainable using MSK modulation and chirp-z transformers. The sample system is not intended to reflect the requirements for an actual ADC/PL system, as many other parameters pertinent to the particular problem to be addressed by the ADC/PL system would have to be examined to finalize any system.

E. RF EQUIPMENT FOR LANDSAT II COMPATIBILITY

The original intent of the Landsat II tests was to conduct throughput demonstration tests using Landsat II and its gound processing stations. Unfortunately, the data format developed for the ADC/PL breadboard, which, to a large degree, was dictated by the choice to use a previously developed chirp-z transformer, prohibits the use of the Landsat II ground receiving stations. The Landsat II gound equipment has provisions for demodulating and recovering FSK modulated (1.0 deviation ratio) 5KBps (Manchester encoded) data streams, and the ADC/PL breadboard format of a 0.5 modulation deviation

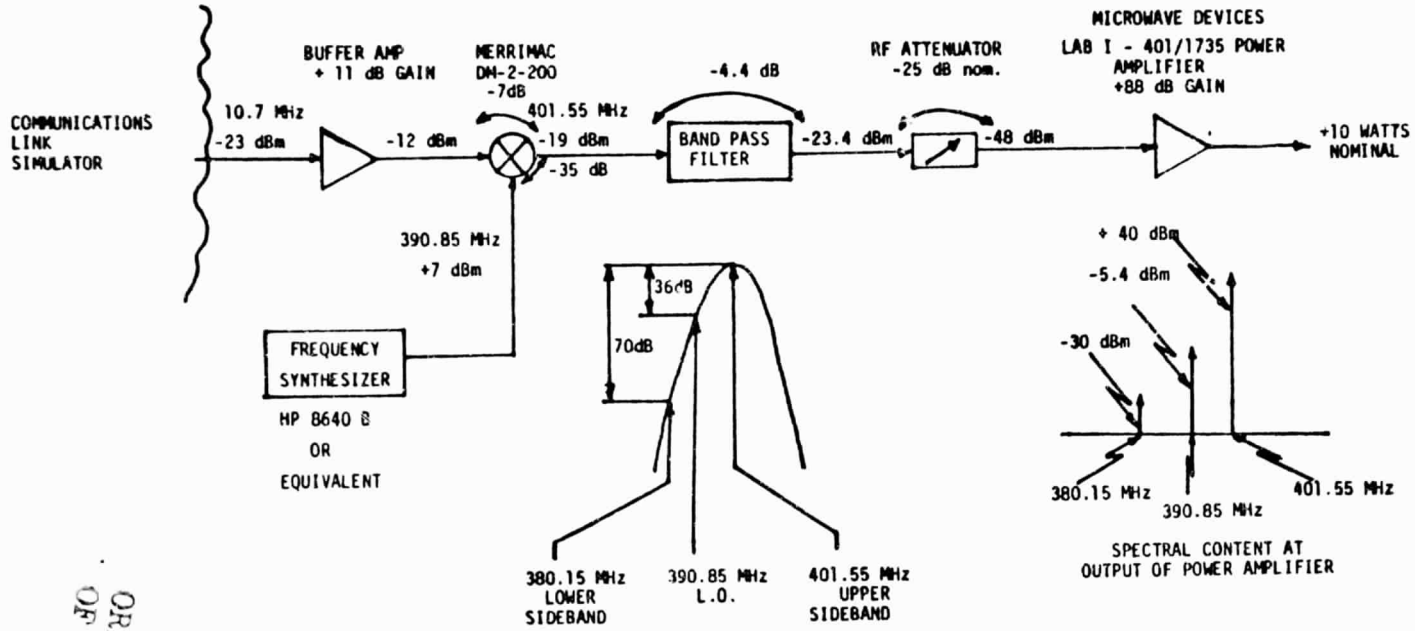
ratio and a 320 Bps data rate would not be compatible with the Landsat II format. The alternative for the down-link would be to build a separate receive subsystem whose i-f output was compatible with the ADC/PL breadboard. Even this approach, however, is not without problems since the absence of a coherent demodulator in the ADC/PL breadboard leaves no means of recovering the bit clock. A bit synchronization circuit, as well as a receive subsystem would thus be required.

The alternate approach of a separate receiver subsystem and bit synchronizer for the down-link would require considerable engineering effort to properly define and is beyond the scope of this report. The up-link, however, is relatively simple to implement. A typical up-link for the ADC/PL breadboard is described below using the Landsat II receive frequency of 401.55 MHz as a model.

A block diagram for an up-conversion link for the ADC/PL breadboard is shown in Figure 4-5. The output of the 10.7 MHz crystal filter in the Communications Link Simulator, which nominally sets at -23 dBm, is routed into a simple discrete buffer amplifier to provide approximately 11 dB of gain. Although not presently included in the ADC/PL breadboard hardware, the buffer amplifier can be easily installed in the Communications Link Simulator. The output of the buffer amplifier, which sets at approximately -12 dBm, is input into the signal port of a Merrimac DM-2-200, or equivalent, doubly balanced mixer. The input into the reference port of the mixer is a 390.85 MHz local oscillator (L.O.) set at +7 dBm. The mixer provides approximately 35 dB of L.O. rejection at the output and has an insertion loss of 7 dB. The output of the mixer then will be upper and lower sidebands at approximately -19 dBm and L.O. component at approximately -28 dBm. Additional filtering is thus required to lower the L.O. component in the output and to remove the unwanted lower sideband. A six section Telonic type TBC-401-8-6-AA tubular bandpass filter of 8 MHz double-sided bandwidth centered at 401.55 MHz is used to provide the additional filtering required. As shown in Figure 4-5, the filter provides an additional 36 dB of L.O. rejection and over 70 dB of suppression of the lower sideband. The output of the filter, which nominally sets at -23.4 dBm, is routed through a variable attenuator to adjust the drive level into the final power amplifier to approximately -48 dBm. The final output stage is a Microwave Devices LABI-401/1735 power amplifier purchased on the RAMS program, and provides approximately 88 dB of gain. For a -48 dBm input drive level, the amplifier will output approximately 10 watts of r-f power. Also shown in Figure 4-5 are the relationships at the final output of the L.O. and lower sideband with respect to the 10 watt upper sideband

R-F UP-CONVERSION / TRANSMIT HARDWARE
FOR LANDSAT II COMPATIBILITY

Figure 4-5



at 401.55 MHz. It is seen that the L.O. component is 45 dB below the upper sideband and that the lower sideband is 70 dB below the upper sideband - which is adequate rejection of the unwanted components.

The L.O. is shown to be derived by an HP8640B, or equivalent, frequency synthesizer. Another approach for the generation of the L.O. would be to use a crystal oscillator and supporting hardware. Two such crystal oscillator circuits for generating the 390.85 MHz L.O. are shown in Figure 4-6. The oscillator/multiplier circuit shown is a widely used approach whereby a crystal oscillator output is multiplied up in frequency by a circuit tuned to a harmonic of the crystal oscillator. The reason for setting the crystal oscillator frequency below the final L.O. frequency required is the difficulty in obtaining crystals at the higher L.O. frequency. The phase lock loop L.O. generator uses the same principle by slaving a VCO power oscillator to the crystal oscillator. A divide-by-four network between the output of the VCO and the reference port of the phase detector serves to implement the times four multiplication. The advantage of this circuit over the multiplying technique is the absence of narrow-band bandpass filtering; the disadvantage is the possible increase in phase noise in the output as compared to the phase noise output in the multiplying technique.

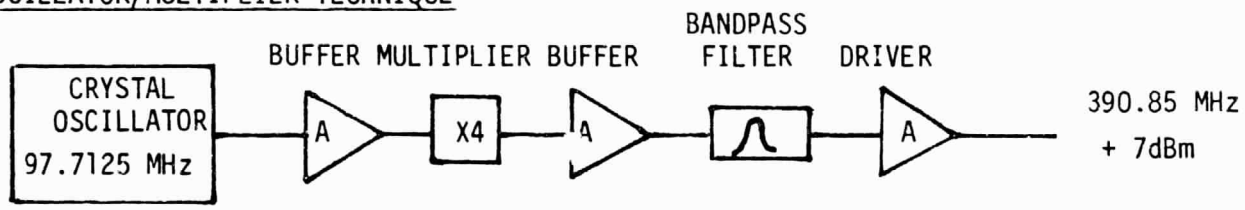
The frequency synthesizer is the recommended approach for the ADC/PL breadboard since it requires no engineering design or checkout efforts.

LOCAL OSCILLATOR GENERATION

EXAMPLES

Figure 4-6.

OSCILLATOR/MULTIPLIER TECHNIQUE



PHASE LOCK LOOP TECHNIQUE