SPECTROLAB

DOE/JPL 954853-78/1
Distribution Category UC-63

ARRAY AUTOMATED ASSEMBLY

PHASE 2

Quarterly Report

William E. Taylor

February 1978

SPECTROLAB, INC.
12500 Gladstone Avenue
Sylmar, California 91342

The JPL Low-Cost Silicon Solar Array Project is sponsored by the U. S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DoE.

ABSTRACT

An analysis was made of cost trade-offs for shaping modified square wafers from cylindrical crystals. For reasonably expectable silicon and sheet costs, the optimum shape will be nearer a circle than a square. This will result in significant incremental costs arising from a combination of the shaping costs and module cost of non-productive areas.

Tests were conducted of the effectiveness of texture etching for removal of surface damage on sawed wafers. A single step texturing etch appears adequate for removal of surface damage on wafers cut with multiple blade reciprocating slurry saws.

Four glass systems have survived preliminary screening tests for use as edge masking dielectrics. These include beta-spodumen, $MgO-Al_2O_3$ borosilicate, baria and titania glasses. Two polymeric phosphorus diffusion sources are being investigated, at least one of which appears suitable. Cofiring of the aluminum back during diffusion has been found to be incompatible and will require a separate firing step.

Aluminum contact metallization does not appear promising, and six silver screen printing inks have been selected for detailed investigation.

Screening tests are underway for the selection of adhesive and coating materials for the superstrate fabrication. Three adhesive candidate materials have been identified for detailed investigation.

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1.0 SUMMARY

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Screening tests are underway for the selection of adhesive and coating materials for the superstrate fabrication. Three adhesive candidate materials have been identified for detailed investigation.

2.0 INTRODUCTION

This is the first quarterly report for an investigation of technology readiness of a selected process sequence for the low cost fabrication of photovoltaic modules as a part of Phase 2 of the Array Automated Assembly Task, Low Cost Silicon Solar Array Project. It covers the Quarter ending December 31, 1977.

2.1 TECHNICAL OVERVIEW OF CELL DESIGN AND PROCESS SEQUENCE

The cell design and selected process sequence are outlined in Table 2-1. Discussion of the module design and process sequence is presented in a subsequent section. In order to make clear what is being proposed, operations which would be performed on one piece of automated equipment and regarded as one process have been subdivided. Thus printing a pattern and firing it have been indicated as separate steps.

The design includes shaped cells in order to achieve the goal of 12-13% module efficiency. Spectrolab's plan includes the use of texturized surfaces, conforming with the conclusions of the Phase 1 studies that this is advantageous. Texturizing is already well developed for (100) oriented single crystal material. Sheet or ribbon input materials may have a different orientation, however, and for these it will be necessary to develop a suitable texturizing process.

The cell design includes a p+ back field obtained from a printed aluminum source. The n+ diffusion will be obtained from a phosphorus doped polymer source. An innovative approach to the junction formation process has been included: namely, the use of a prefired masking dielectric on the edge of the cell. This

Table 2-1

CELL DESIGN AND PROCESS SEQUENCE

1. Design:

   Shaped, size 25-100 cm^2 (4-16 in^2)
   Texturized surface
   n+ junction diffusion
   p+ back surface field
   Printed contact metallization
   Wraparound contacts
   η_c = 15% (28°C, 100 mW/cm^2)

2. Process Sequence:

   1) Texture Etch
   2) Print edge masking dielectric
   3) Fire edge masking dielectric
   4) Print back aluminum
   5) Apply front polymer dopant
   6) Fire junction and back surface field sources
   7) Print back isolation dielectric
   8) Fire back isolation dielectric
   9) Print contact pads
   10) Print front grid pattern and wraparound conductors
   11) Fire contact pads, grid pattern and wraparound conductors
   12) Test cells

is intended to permit the codiffusion of the n+ and p+ regions without the need for an edge etch. As a further innovation, the diffusion oxide will not be removed, but will be retained to serve as an antireflection coating. The process sequence proposed here thus is intended to eliminate the following process operations: Separate p and n diffusions, edge and/or back etching, diffusion oxide removal and a separate AR coating step.

A further use for the edge masking dielectric will be as an insulation layer for wraparound contacts. At this point an additional printing and firing operation is introduced to locate dielectric pads for the wraparound contacts on the back aluminum. The solderable contacting pads on the aluminum back will be printed next. The front metallization grids and wraparound conductors are then printed. For this we propose using thick film paste which has been formulated for adherence and contact through the diffusion oxide. Attention will be given to minimizing the junction depth, and line width, and optimizing collector grid spacings. Finally, the front contact grids and solderable contacts on the back side will be cofired to complete the cell fabrication.

2.2 TECHNICAL OVERVIEW OF MODULE DESIGN AND PROCESS SEQUENCE

The module design and selected process sequence are shown in Table 2-2. The module design is comprised of a 24 by 48 inch (60 x 120 cm) tempered glass superstrate. Square shaped cells will be used in order to achieve the 12% module efficiency goal.

The module structure uses a thin bond line adhesive to attach the solar cells to the glass superstrate. Since silicone adhesives are known to be technically feasible, and the thin bond

Table 2-2

MODULE DESIGN AND PROCESS SEQUENCE

1. Design

   Size 60 x 120 cm (2 x 4 ft)
   Tempered glass superstrate
   Cells attached by polymeric adhesive
   Preformed circuit interconnects
   3 mil polymeric conformal coating
   Aluminum extrusion frame
   η_m = 13%

2. Process Sequence*

   13. AR Treat Superstrate Glass
   14. Mount Cells on Superstrate
   15. Cure Adhesive
   16. Apply Interconnects
   17. Apply Conformal Coat
   18. Cure Conformal Coat
   19. Mount in Frame
   20. Test Module

*Process sequence numbers continue from the cell area (Table 2-1)

line minimizes costs, they have been included in the preliminary design. However, alternative adhesives will be evaluated in a search for greater cost effectiveness. Interconnect conductors will be in the form of thin copper foil or ribbons. A simple automatic reflow soldering operation is permitted by the wrap-around techniques used to position both contacts on the back sides of the cells. A conformal coating will be used as the encapsulant and rear surface. The module assembly will be completed by mounting the superstrate in an aluminum extrusion frame.

3.0 TECHNICAL DISCUSSION

3.1 OPTIMUM SQUARE WAFER SHAPING FROM CYLINDRICAL CRYSTALS

An analysis has been made of the optimum shaping of squared wafers from cylindrical Czochralski crystals as a function of the relative costs of silicon material and photovoltaic module and system related costs. For the purposes of this analysis it was assumed that the shaping would be accomplished by slabbing off four sides of the crystal to form a square section with truncated corners. This procedure eliminates the cell processing costs which would be associated with the discarded silicon if the cells were shaped after processing. It also provides the maximum salvage value for the discarded silicon.

The module geometry associated with one cell is shown in Figure 1. The circular segments, A_s, outside of the square correspond to the areas of discarded silicon. The corners of the square, A_I, which are truncated by the circle, correspond to interstitial areas which incur module and system related costs, but which do not generate any power.

The total cost per watt will be

$$C_W = C_W^o = S_W^o A_S' + M_W^o A_I' \qquad (1)$$

where C_W^o = Cost per watt assuming perfect nesting without shaping

S_W^o = Cost per watt of silicon

A_S' = Fractional area of silicon discarded

M_W^o = Module and system associated cost per watt

A_I^1 = Fractional area of module not occupied

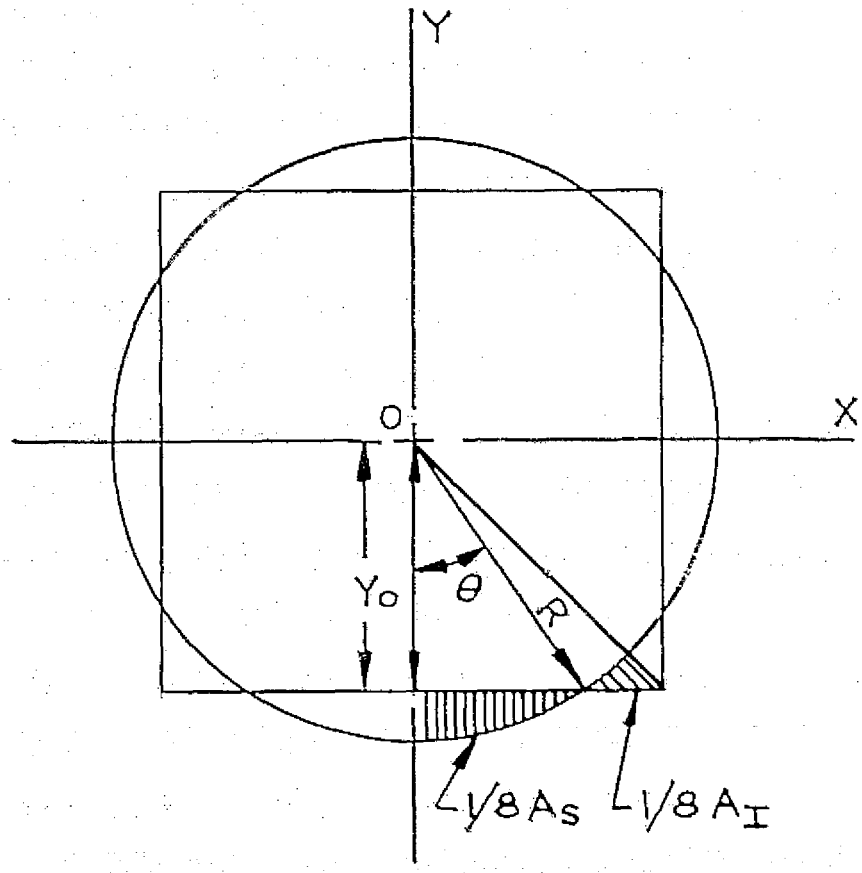

Figure 1. MODULE GEOMETRY OF UNIT CELL

and where the superscript o indicates costs assuming perfect nesting without shaping.

It can be shown that

$$A_S' = \frac{4}{\pi}(\theta - \text{Sin}\theta\text{Cos}\theta) \tag{2}$$

$$\text{and} \quad A_I' = \frac{(\text{Cos}^2\theta - \text{Sin}\theta\text{Cos}\theta - \frac{\pi}{4} + \theta)}{\text{Cos}^2\theta} \tag{3}$$

where θ is defined in Figure 1.

The incremental costs associated with shaping will be

$$\frac{\Delta C_W}{S_W^o} = A_S' + \beta A_I' \tag{4}$$

$$\text{Where} \quad \beta = M_W^o/S_W^o \tag{5}$$

Substitution of equations (2) and (3) into (4) gives

$$\frac{\Delta C_W}{S_W^o} = \frac{4}{\pi}(\theta - \text{Sin}\theta\text{Cos}\theta) + \frac{\beta}{\text{Cos}^2}(\text{Cos}^2\theta - \text{Sin}\theta\text{Cos}\theta - \frac{\pi}{4} + \theta) \tag{6}$$

Shaping will be favored if the silicon cost is small compared to the module associated costs (i.e., large β). However cost projections suggest that it is unlikely β will ever be larger then 1. For example one estimate of the cost allocation required to meet the 1986 goal of \$50/kW allots \$25 to silicon sheet and \$10 to module assembly and encapsulation[1].

For interpretive purposes it is convenient to use a ratio of the size of the circle to that of the square rather than the angle θ:

$$\alpha = \frac{R}{Y_o} = \frac{1}{Ccs\theta} \tag{7}$$

The incremental cost normalized to silicon costs (equation 4) is plotted against the ratio α in Figure 2 for $\beta = 0.5$ and $\beta = 1.0$.

The minimum in incremental cost will occur when

$$\frac{d}{d\theta}\left(\frac{C_W}{S_W^o}\right) = \frac{dA_S'}{d\theta} + \beta\frac{dA_I'}{d\theta} = 0$$

or

$$\beta = -\frac{\frac{dA_S'}{d\theta}}{\frac{dA_I'}{d\theta}} \tag{8}$$

From equations (2) and (3) it can be shown that

$$\frac{dA_S'}{d\theta} = \frac{8}{\pi}Sin^2\theta \tag{9}$$

and

$$\frac{dA_I'}{d\theta} = -\frac{2(\frac{\pi}{4} - \theta)Sin\theta}{Cos^3\theta} \tag{10}$$

from which it follows that the condition for the minimum is

$$\beta = \frac{\frac{4}{\pi}Sin\theta Cos^3\theta}{\frac{\pi}{4} - \theta}. \tag{11}$$

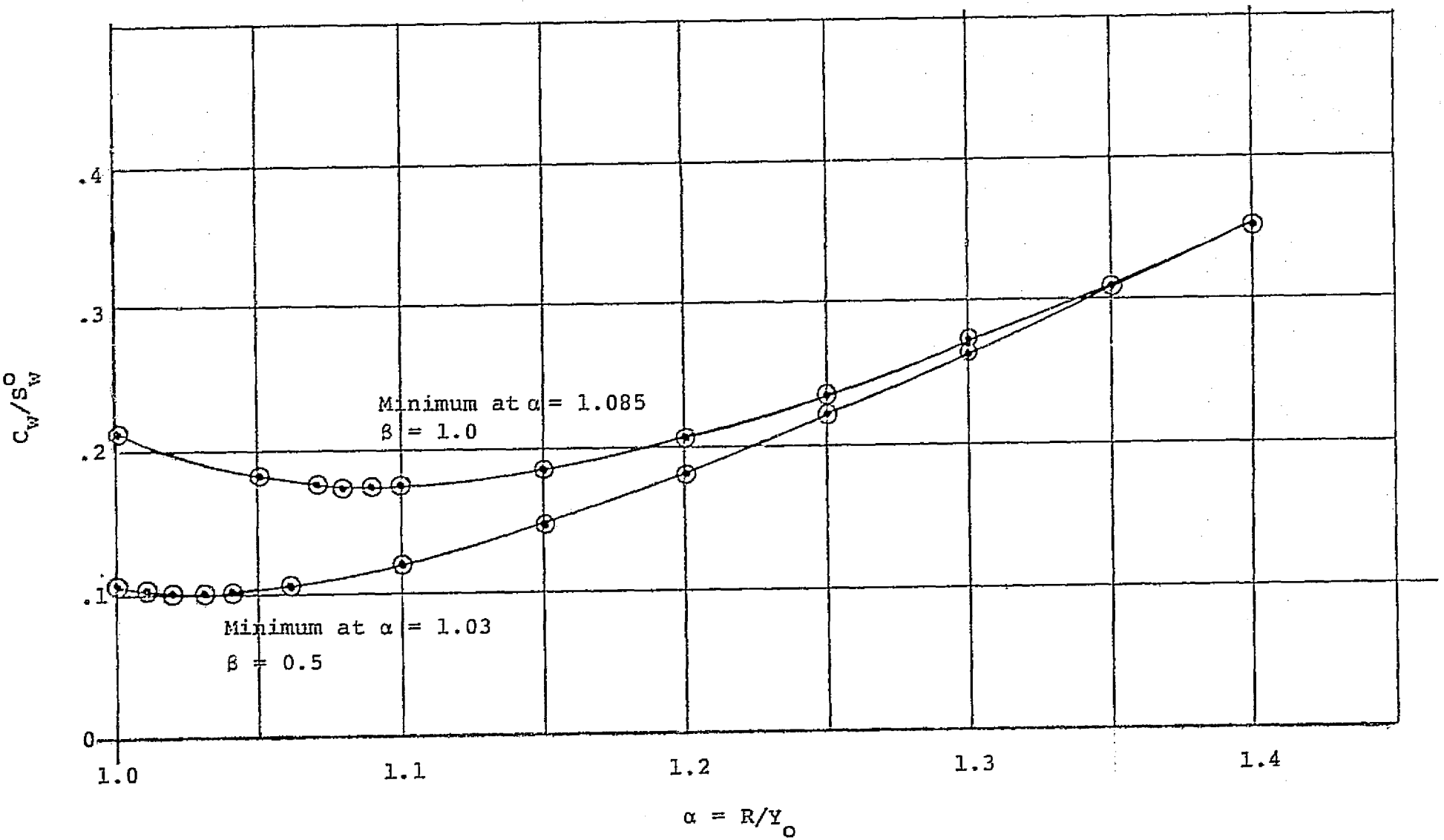

Figure 2. INCREMENTAL COSTS ASSOCIATED WITH SHAPING MODIFIED SQUARES FROM CIRCULAR CRYSTALS

The relation between β and the corresponding size ratio, α, for the cost minimum is shown in Figure 3 as derived from equations (11) and (7). The region of most probable interest is defined by the box.

From Figures 2 and 3 it will be seen that the optimum shape will be nearer to a circle than a square. This implies that there will be significant incremental costs. Incremental costs for a number of assumptions regarding interim silicon and module costs are summarized in Table 3-1. Similar results have been obtained for shaping modified hexagons from circular discs.[2]

3.2 SURFACE PREPARATION

Silicon wafers, which had been sliced using slurry-fed gang cutting methods, were etched in sodium hydroxide for varying times to determine the minimum quantity of material removal necessary for damage elimination. The 1-0-0 orientation, one ohm-cm material used in this study was then diffused and fabricated into solar cells using standard controlled aerospace processes. 2 cm by 2 cm cells were cut from the processed round wafers and tested without AR coating. Since a distorted layer of silicon has a low minority carrier diffusion length, the output of a cell is adversely affected by any residual cutting damage. In addition the high leakage current manifested by abraded silicon cells also results in curve shape degradation. Current at the 500 mv load point was used as a measure of residual surface damage.

Four surface preparation procedures were examined:

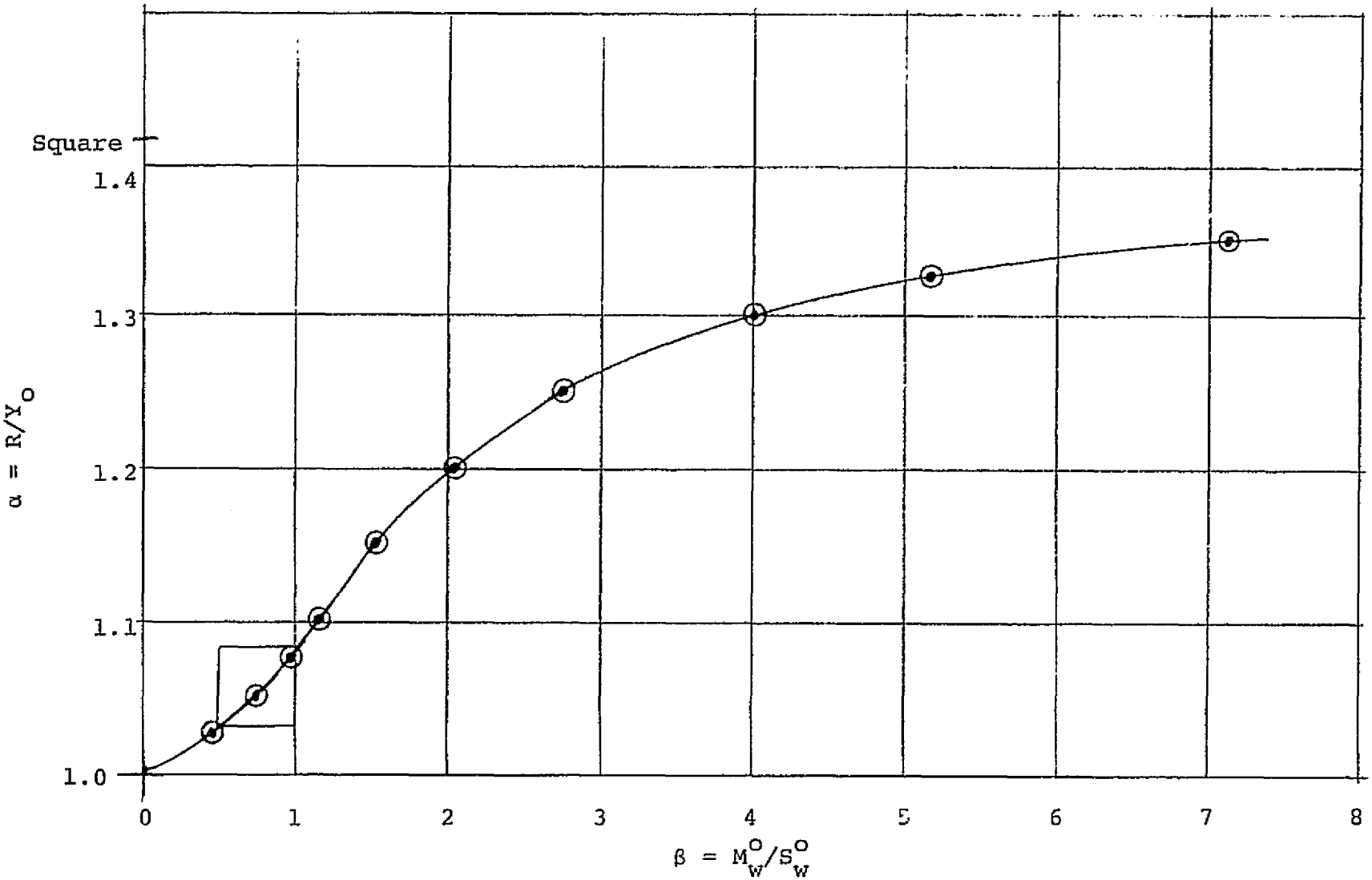

Figure 3. α LOCATION OF THE MINIMUM INCREMENTAL COST FOR SHAPING MODIFIED SQUARES FROM CIRCULAR CRYSTALS AS A FUNCTION OF THE RATIO OF MODULE TO SILICON COSTS.

Table 3-1

INCREMENTAL COSTS ASSOCIATED WITH SHAPING
MODIFIED SQUARES FROM CIRCULAR CRYSTALS

Silicon Cost $/Watt	Cost Ratio $\beta = M_w^o/S_w^o$	Size Ratio at Cost Min. $\alpha = R/Y_o$	Minimum Incremental Cost
2.00	0.5	1.0287	$0.200
2.00	1.0	1.0851	0.351
2.00	2.0	1.1966	0.515
1.00	0.5	1.0287	$0.100
1.00	1.0	1.0851	0.176
1.00	2.0	1.1966	0.257
0.20	0.5	1.0287	$0.020
0.20	1.0	1.0851	0.035
0.20	2.0	1.1966	0.051

Group	Pre-Etch Boiling 30% NaOH	Texturizing Etch 80°C 2% NaOH*	Material Removed per Side	Sample
1	0	55 Min.	0.0009 inch	29 cells
2	90 Sec.	55 Min.	0.002 inch	26 cells
3	180 Sec.	55 Min.	0.003 inch	30 cells
4	270 Sec.	55 Min.	0.004 inch	28 cells

*20% by volume Isopropyl alcohol.

Open circuit voltage, short circuit current and current at 500 mv were measured under AM1 Xenon source illumination. The data obtained are reported in Table 3-2, together with calculated values of the mean and standard deviation and coefficients of kurtosis and skewness.

These data (Table 3-2) suggest that the power at load is as large with a one-step texture etch as it is with a multi-stage etching process (groups 2, 3, 4). Moreover, there appears to be the advantage of a narrower distribution of output power and possibly fewer units lost in the form of outliers. The latter would undoubtedly be rejects in a manufacturing operation.

We tentatively attribute the larger variance of I_{500} for the more heavily etched samples to an increased probability of surface damage occurring between the junction diffusion and front collector metallization steps. Visual observation of the textured surface reveals that the parts treated by the one-step process have a somewhat coarser and more irregular structure. The greater number of smaller and more uniformly sized tetrahedral peaks formed in a multi-stage sequence will be more susceptible to damage in subsequent processing. Such damage would result in varying degrees of junction shunting, depending on the nature of the damage and its location. Such shunting would also have adverse effects on open circuit voltage and could account for the greater bariance of that parameter for Groups 2, 3 and 4.

Table 3-2

ETCH TEST DATA

Group 1. (No Pre-Etch)

V_{oc} mV	I_{sc} mA	I_{500} mA
612	140	135
609	139	134
612	139	134
606	139	134
605	139	133
607	138	133
610	137	133
612	138	133
610	137	132
608	138	132
603	139	132
612	135	131
610	136	131
608	136	131
608	140	131
609	137	131
610	137	131
608	135	130
604	136	130
607	139	130
608	138	129
604	138	129
604	139	128
607	139	127
604	133	126
605	132	126
604	140	125
587	140	99*
540	139	35*
$\bar{x}$ 607.6	137.5	130.8
σ 2.78	2.01	2.60
Kurtosis 1.85	3.64	1.28
Skewness 0.02	-1.06	-0.58

*Cells treated as outliers, data not included in calculated statistical parameters.

Table 3-2 (cont.)

ETCH TEST DATA

Group 2 (90 Sec. Pre-Etch)

	V_{oc} mV	I_{sc} mA	I_{500} mA
	611	146	139
	611	144	139
	612	145	139
	611	145	138
	611	144	138
	609	143	136
	607	144	135
	603	143	134
	611	141	134
	607	139	133
	606	143	132
	608	146	132
	600	145	128
	611	144	128
	606	137	127
	605	145	124
	602	145	124
	604	141	122
	603	143	122
	601	145	119
	602	146	117
	604	138	115
	593	142	109
	596	144	108
	597	137	107
	541	144	37*
$\bar{x}$	605.2	143	127.2
σ	5.12	2.67	9.93
Kurtosis	2.59	3.04	2.26
Skewness	-0.58	-1.06	-0.62

*Cells treated as outliers, data not included in calculated statistical parameters.

Table 3-2 (cont.)

ETCH TEST DATA

Group 3 (180 Sec. Pre-Etch)

	V_{oc} mV	I_{sc} mA	I_{500} mW
	612	143	136
	606	141	131
	609	140	131
	609	135	128
	607	142	128
	605	141	127
	601	139	126
	605	139	126
	610	133	125
	608	139	125
	607	133	124
	609	140	124
	603	136	123
	604	141	122
	603	142	122
	601	141	120
	602	140	118
	605	139	117
	603	139	113
	600	140	113
	595	141	109
	597	140	107
	596	139	105
	592	141	97.3
	588	136	92.7
	573	141	71.7*
	551	141	38.2*
	486	140	2*
	419	140	2*
	324	140	2*
$\bar{x}$	603.1	139.2	119.6
σ	5.76	2.59	10.45
Kurtosis	3.21	3.43	3.30
Skewness	-0.84	-1.10	-0.96

*Cells treated as outliers, data not included in calculated statistical parameters.

Table 3-2 (cont.)

ETCH TEST DATA

Group 4 (270 Sec. Pre-Etch)

	V_{oc} mV	I_{sc} mA	I_{500} mA
	613	145	140
	614	143	138
	610	145	138
	613	142	138
	607	143	137
	604	144	136
	612	140	136
	604	146	135
	610	139	134
	605	145	134
	611	142	134
	605	141	132
	612	139	132
	606	143	131
	608	142	130
	603	144	127
	604	142	127
	605	143	124
	598	144	119
	605	139	116
	599	144	114
	602	144	114
	605	129	123*
	584	146	82.4*
	571	142	71.2*
	574	144	67.3*
	550	144	46.8*
	530	143	25.9*
$\bar{x}$	606.6	142.7	130.3
σ	4.54	2.01	7.91
Kurtosis	1.98	2.33	2.61
Skewness	-0.01	-0.50	-0.92

*Cells treated as outliers, data not included in calculated statistical parameters.

Another effect of pre-etching is the development of a rocky or pillowed structure, with local square shaped areas which are in some cases recessed and in others standing in relief. This structuring is barely noticeable for Group 2 in contrast to Groups 3 and 4, where it is quite pronounced. It may be that the elevated blocks are susceptible to more severe damage during subsequent processing, which could account for the increased incidence of outliers in Groups 3 and 4.

The more perfectly texturized surfaces of Groups 2, 3 and 4 would be expected to trap incident radiation more efficiently and hence to have higher short circuit current than Group 1. There is some evidence of this, but it is not sufficient to offset a degradation in curve shape for the pre-etched cells. This tendency toward curve shape degradation is probably attributable to the damage effects which have been discussed in the previous paragraphs.

3.3 JUNCTION FORMATION

3.3.1 Edge Masking Dielectric

Work is underway on the formulation of the dielectric paste to be used on the cell edge as a diffusion mask and subsequently as the isolation dielectric for the wraparound contact. The following criteria have been selected for guiding this phase of the development effort:

1. Maturation (firing) temperature $\simeq 900^{o}$C.
2. Barrier to phosphorus migration.
3. Thermal coefficient of linear expansion, 3.5 to 4.5 x 10^{-6} per ^{o}C.
4. Good melting properties.
5. Stability with respect to water.

6. Stability with respect to silicon at the maturation temperature.
7. Structural and chemical stability with respect to thermal cycling in subsequent processing.

The low expansion coefficient of silicon (3.9 to 4.6 x $10^{-6}/^{o}C$) dictates the use of glasses whose compositions can be modified to obtain expansion values below 4 x $10^{-6}/^{o}C$. The glasses must mature within the selected temperature ranges and exhibit the required physical characteristics when applied to silicon. In general, the expansion coefficients of glasses are inversely proportional to the maturation temperature. Low expansion glasses usually have high maturation temperatures.

The glass systems to be investigated were selected on the following considerations:

1. Those with low expansion coefficients which would mature within the required temperature limits; and

2. Coating systems with acceptable maturation temperatures and composition which can be altered to reduce the expansion coefficient and not affect the firing characterists.

Four glass systems have been selected for evaluation as Edge Dielectric Materials:

Series 1 - Beta-Spodumene Systems

The glasses have very low expansion characteristics and have the general (molar equivalent) formulation

$$0.811\ Li_2O \quad \bullet \quad 0.189\ MgO \qquad \bullet \qquad 0.282\ Al_2O_3 \quad \bullet \quad 0.340\ P_2O_5 \qquad \bullet \qquad 3.023\ SiO_2$$

These glasses devitrify when fired at low temperatures (900 to 1000°C) to form precipitated refractory second phase.

Series 2 - $MgO \cdot Al_2O_3$ Borosilicate Glasses

These glasses have calculated expansion coefficients approximating that of silicon. The general formulation as shown below has a maturation temperature of 1050°C.

$$0.125\ CaO \quad \bullet \quad 0.875\ MgO \qquad \bullet \qquad 0.330\ Al_2O_3 \quad \bullet \quad 1.382\ B_2O_3 \qquad \bullet \qquad 2.334\ SiO_2$$

Series 3 - Baria Glasses

This family of glasses has a calculated lower expansion coefficient than silicon and maturation temperatures between 950 and 1000°C. The general compositions are:

$$0.133\ BaO,\ 0.041\ ZnO,\ 0.043\ CaO,\ 0.783\ MgO \qquad \bullet \qquad 0.175\ B_2O_3 \qquad \bullet \qquad 0.016\ SiO_2$$

Series 4 - Titania Glasses

These glasses precipitate dissolved titania at about 650°C during a slow cooling process. Maturation

temperatures are about 815°C. Expansion coefficient are between 9.0 and 9.9 x 10^{-6}/°C. General compositions are as follows:

$$\begin{matrix} 0.505\ Na_2O \\ 0.211\ K_2O \\ 0.080\ CaO \\ 0.149\ Li_2O \\ 0.055\ ZnO \end{matrix} \quad \bullet \quad 0.644\ B_2O_3 \quad \bullet \quad \begin{matrix} 1.178\ TiO_2 \\ 2.669\ SiO_2 \end{matrix}$$

The Mayer and Havas[3] factors shown in Table 3-3 were used as the basis for estimating the expansion coefficients of the selected compositions. Materials which contribute to low expansion are SiO_2, MgO and B_2O_3, whereas the high expansion materials are Na_2O and K_2O. Since B_2O_3 is a glass former, with low fusion temperature, it is an excellent addition to reduce both expansion and maturation temperature. However, excessive additions of B_2O_3, contribute towards high water solubility. Expansion characteristics can be reduced by additions of MgO and SiO_2. However, these materials contribute towards increasing viscosity and tend to increase maturation temperature. Silica is an excellent addition to increase resistance to water solubility. Additions of K_2O and Na_2O will reduce the maturation temperature, but will also increase expansion coefficients.

The following experiments have been carried out:

Series 1 - Beta-Spodumene Glasses

This series of glasses was originally compounded for application to slip-cast-fused silica, which has an expansion coefficient of 0.3 x 10^{-6}/°C. Maturation temperature is about 1150°C. These glasses, upon maturation devitrify to form keatite ($Li_2O \cdot Al_2O_3 \cdot 5SiO_2$) and spodumene ($Li_2O \cdot Al_2O_3 \cdot 4SiO_2$).

Table 3-3

MAYER AND HAVAS EXPANSION FACTORS*[3]

Oxide	Factor ($\times 10^{-7}/^{o}C$)
B_2O_3	0.1
MgO	0.8
SiO_2	2.0
SnO_2	2.0
P_2O_5	2.1
ZnO	3.0
BaO	4.1
TiO_2	5.0
CaO	5.0
Al_2O_3	8.5
K_2O	10.0
Na_2O	

*Based on weight percent.

The original formulation 1E1 (Table 3-4) was modified to increase expansion, promote devitrification and reduce maturation temperature. Composition 1E6 did not form a melt after smelting at 1360°C for 30 minutes. Compositions 1E-7 formed a melt at 1360°C, but was highly viscous. A low viscosity melt was obtained with Composition 1E8.

The latter composition was overfired at 900°C when fired an silicon for either 7 minutes or one minute. Maturation (firing) temperature was reduced until a vitrified surface was obtained at 700°C. This glass at 700°C exhibits a possible two phase system. However, surface tension is high and the glass tends to form beads.

Series 2 - $MgO\text{-}Al_2O_3$ Borosilicate Glasses

The composition of this series was based on a Ferro Corporation glaze which had a calculated coefficient of expansion of $3.9 \times 10^{-6}/°C$ (2E1, Table 3-5). The glass did not form a melt at a smelting temperature of 1400°C. Subsequent additions of B_2O_3 (2E2), and decrease of MgO (2E3) to reduce the maturation temperature resulted in a low viscosity melt. The Series 2E3 exhibited a partially vitrified surface when fired on silicon at 900°C for 7 minutes.

Series 3 - Baria Glasses

The composition of these glasses is based on a eutectic at 850°C of $BaO\text{-}3.58SiO_2$. Compositions were modified to increase expansion and increase fluidity as shown in Table 3-6. At 900°C the glasses exhibit a low amount of vitrification when applied to silicon.

Table 3-4

COMPOSITION (mol %) OF BETA-SPODUMENE GLASSES

	Series Number			
Oxide	1E1	1E6	1E7	1E8
Li_2O	17.46	15.29	24.25	19.22
MgO	4.07	3.56	5.64	4.47
Na_2O	--	4.71	7.47	5.92
Al_2O_3	6.07	5.33	8.45	6.69
P_2O_5	7.32	13.20	20.93	37.32
SiO_2	65.08	56.97	31.76	25.18
SnO_2	--	0.94	1.49	1.18

Table 3-5

COMPOSITIONS (Mol %) OF $MgO \cdot Al_2O_3$ BOROSILICATE GLASSES

	Series Number		
Oxide	2E-1	2E-2	2E-3
CaO	2.48	2.07	2.25
MgO	17.34	14.47	7.18
Al_2O_3	6.54	5.46	5.93
B_2O_3	27.39	39.40	42.73
SiO_2	46.25	38.60	41.90

Table 3-6

COMPOSITIONS (mol %) OF BARIA GLASSES

	Basic		
Oxide	3E-1	3E-2	3E-3
BaO	3.52	4.44	5.33
ZnO	1.09	1.38	1.66
CaO	1.14	1.44	0.94
MgO	20.79	--	--
B_2O_3	46.51	58.71	70.39
SiO_2	26.96	34.03	21.68

Series 4 - Titania Glasses

These compositions are based on titania enamels which devitrify when air quenched through the temperature range of 650 and 700°C. The expansion coefficient of the original formulation (5E-1, Table 3-7) is about 9.9 x 10^{-6}/°C whereas the compositon represented by 5E-3 is approximately 7.0 x 10^{-6}/°C.

Composition 5E3 formed a low viscosity clear melt at a smelting temperature of 1360°C. Maturation on silicon with precipitation of titania was obtained at 600°C through 900°C.

The commercial inks shown in Table 3-8 have been screened on silicon and general observations made after firing at 500 and 880°C for 7 minutes.

Based on the work conducted thus far in the program, the most viable glasses for the edge dielectric material system are the titania and beta-spodumene systems. These glasses form a secondary refractory phase during firing, and thus should be able to withstand repeated processing at lower temperatures without deterioration.

3.3.2 N+ Diffusion

Preliminary tests have been made with two phosphorus sources as alternatives to gaseous sources. Emulsitone Emitter Source N-250 (Emulsitone Co., Whippany, New Jersey) yielded cells with properties similar to those obtained with our aerospace process gaseous PH_3 source. The second alternative source was a Transene 1020N Phosphorus Diffusant Preform (Transene Co., Inc. Rowley, Massachusetts) which gave results somewhat inferior to those obtained with the spin-on and gaseous sources.

Table 3-7

COMPOSITIONS (mol %) OF TITANIA GLASSES

	Series Number		
Oxide	5E-1	5E-2	5E-3
Na_2O	9.20	5.87	6.23
K_2O	3.84	1.95	2.07
CaO	1.46	1.57	1.66
Li_2O	2.71	1.95	2.07
ZnO	1.00	1.08	1.15
B_2O_3	11.73	19.59	20.79
TiO_2	21.45	15.68	10.56
SiO_2	48.61	52.29	55.47

Table 3-8

COMMERCIAL DIELECTRIC INKS

(Firing Time - 7 Min.)

Ink	Temp °C	Observations
Plessey I-90255	880	Matte Surface
Owens Illinois H110	880	Matte Surface
ESL 4608	880	Matte Surface
EMCA 2828B	880	Matte Surface
ESL 4901	880	Matte Surface
Transene 57724	880	Clear, Some Cracks
Owens Illinois 61229	880	Opaque, Bubbles
Transene 780	880	Overfired
Transene 980	880	Overfired
DuPont 9137	880	Overfired
ESL 4771B	880	Overfired

The Emulsitone N-250 source was applied to texturized round (2 inch) and square (2 cm) wafers at a spin rate of 3000 RPM. The wafers were cut from 2-3 ohm-cm boron doped crystals. The coated wafers were baked for 10 minutes at 125°C and then diffused for 30 minutes at 850°C in a flowing Nitrogen-oxygen gas mixture (500 cc/min N_2, 20 cc/min O_2). The other cell processing steps consisted of standard controlled aerospace solar cell processing methods, without AR coating. Measurements of open circuit voltage, short circuit current and current at 300 mv were made using AM1 Xenon illumination. Results obtained with the square cells are reported in Table 3-9.

The Transene 1020N Phosphorus Diffusant Preform is comprised of a thin (2.5 mils) disc impregnated with a phosphorus compound. A sample of cells was prepared with these preforms using the same diffusion conditions, cell processing and measurement techniques as were used with the Emulsitone source. Results are reported in Table 3-10.

A small control sample was prepared using the PH_3 source used in our normal aerospace cell processing. In this case the diffusion cycle consists of 5 minutes pre-heat, 20 minutes deposition and 10 minutes of further drive-in all at 850°C. Gas flow conditions are the same as in the experimental runs, as are the other cell processing and measurement techniques. Results are reported in Table 3-11 where the standard deviation is replaced by its unbiased estimate, S.

Examination of cells processed with the Transene 1020N source showed that the tetrahedral peaks and edges had been rounded by a corrosive or dissolution process and that residual stains, which could not be removed with hydrofluoric acid, appeared erratically on the cell surfaces. Both of these processes would have a negative impact on short circuit and load point current.

Table 3-9

DIFFUSION DATA

Emulsitone N-250 Spin-On Source

2 cm Square Wafer

	V_{oc} mV	I_{sc} mA	I_{300}
	580	137	136
	581	138	136
	584	137	136
	584	136	136
	587	136	135
	579	136	135
	593	136	135
	579	136	134
	586	134	134
	584	134	134
	583	135	134
	589	135	134
	582	135	134
	587	134	133
	586	134	133
	584	134	133
	583	134	133
	586	132	132
	593	132	131
	576	132	131
	586	132	131
	584	134	131
	585	128	127
	558	137	137*
$\bar{x}$	584.0	134.4	133.4
σ	3.91	2.14	2.12
Kurtosis	3.65	4.33	4.31
Skewness	0.53	-0.94	-1.06

*Cells treated as outliers, data not included in calculated statistical parameters.

Table 3-10

DIFFUSION DATA

Transene 1020N Phosphorus Diffusant Preform

2 cm Square Wafer

V_{oc} mV	I_{sc} mA	I_{300} mA
588	140	140
590	140	140
589	138	138
590	137	136
585	137	136
586	134	134
590	133	133
589	133	132
584	134	132
586	133	131
585	131	130
586	129	129
584	129	128
587	129	128
587	126	122
582	121	121
589	121	120
578	119	119
587	117	117
583	116	116
585	116	116
590	112	111
288	001	001*
$\bar{x}$ 586.4	128.4	127.7
σ 2.98	8.40	8.39
Kurtosis 3.62	1.91	1.93
Skewness -0.84	-0.42	-0.31

*Cells treated as outliers, data not included in calcualted statistical parameters.

Table 3-11

DIFFUSION DATA
Phosphine (Control Sample)
2 cm Square Wafer

V_{oc} mV	I_{sc} mA	I_{300} mA
592	140	136
589	140	136
590	137	135
593	138	135
594	136	135
590	139	135
594	137	134
591	139	134
$\bar{x}$ 591.6	138.2	135.0
S_x* 1.92	1.49	0.76

*Unbiased estimate of standard deviation.

3.3.3 P+ Back Contact Metallization

The back contact metallization utilizes a proprietary screen-printed aluminum paste which is tolerant of a wide variety of firing time periods (15 seconds to 3 minutes) and temperatures (750°C to 900°C). Previous experience[4] has shown that this treatment produces a back surface field which results in open circuit voltages averaging 610 mV (at 20°C) for bulk resistivities between 2 and 800 ohm-cm and thicknesses greater than 0.0015 inch. The process also causes a short circuit current enhancement for cells of five mil thickness or greater. The magnitude of enhancement decreases as the thickness increases. This current and voltage improvement caused by the paste back surface field has been verified using both 1-0-0 and 1-1-1 materia.

In attempting to fire the aluminum during the diffusion cycle, we have discovered that the longer time at 850°C causes excess dissolution of silicon into the aluminum. This effect will preclude firing the aluminum during the diffusion step as had been originally planned. In order to retain a process sequence which does not involve back etching we have investigated the possibility of firing the aluminum on phosphorus diffused surfaces. If the aluminum attacks the silicon sufficiently uniformly and penetrates beyond the junction, back-field contact to the p-type region can be accomplished without back etching. The requirement for an edge diffusion mask would be unchanged from the requirement of the originally planned process sequence.

In order to test this possibility, aluminum paste was printed and fired at 850°C for 30 seconds on one surface of a round, 2 ohm-cm wafer which had been diffused on both sides using a PH_3 gaseous source. In order to provide an adequate test, the junction depth was 0.35 mm, well beyond the depth which will be

encountered in actual solar cell fabrication. After dicing into 2 cm squares, cells were completed using standard controlled aerospace cell fabrication processes. AR coating was omitted. Measurements of V_{oc}, I_{sc} and I_{500} were made using AM1 xenon illumination. The results are reported in Table 3-12.

The observed characteristics are substantially those one would expect of a normal p+ back field cell on this type of material, indicating that the junction was eliminated over substantially all of the back surface. This is particularly evident in the open circuit voltage ($\bar{x}$ = 612 mW) which would be about 600 mV for this material in the absence of a back field. There is no evidence of a badly degraded curve shape; however, further detailed comparison against a control standard is required to be sure that the curve shape is completely unaffected.

3.4 FRONT CONTACT METALLIZATION

The firing of a fritted metallization contact paste on a silicon solar cell surface is accompanied by a number of complex interactions. As an example, the possibility of deleterious contamination in the vicinity of the shallow junction is always a matter of concern. The assessment of this possibility is complicated by such considerations as whether paste borne contaminants are available, migrate into the silicon given the time and temperature conditions available.

On the basis of our experience with fritted paste contact metallization we believe that while likely sources of problems such as contamination and contact resistance may be significant, the situation is usually dominated by oxidative attack of the silicon by the frit. Contact adherence of a paste formulation is primarily achieved by oxide formation and solution processes at the silicon

Table 3-12

PROPERTIES OF SOLAR CELLS WITH ALUMINUM PASTE BACK-FIELD
NO BACK ETCH

V_{oc} mV	I_{sc} mA	I_{500} mA
616	142	137
609	141	135
617	140	135
612	139	134
613	139	134
613	139	134
615	139	134
610	140	134
618	139	133
612	138	133
611	141	133
608	139	133
615	137	133
612	139	133
615	139	132
610	140	132
612	139	132
615	138	132
616	138	131
616	137	131
612	139	131
612	137	131
612	141	131
612	137	131
613	138	130
613	139	130
613	137	129
614	135	129
616	136	129
615	136	128
614	134	128
609	136	127
618	140	127
612	133	127
613	136	127
606	136	127
613	140	126
614	134	126
613	138	125
612	136	125
608	138	124
610	137	124
610	137	124
613	139	124
607	140	122
611	139	122
609	138	114*
612	136	113*
603	138	92.6*
610	142	92.4*
604	137	57.6*
$\bar{x}$	612.6	138.1	129.8
σ	2.71	1.96	3.79
Kurtosis	2.82	2.89	2.10
Skewness	-0.22	-0.47	-0.33

*Cells treated as outliers, data not included in calculated statistical parameters.

surfaces. Thus the firing step is commonly carried out in an oxidizing atmosphere. The SiO_2 layer which acts as a rate limiting membrane on the silicon surface is unable to perform this function under the metallization paste because it is disolved by the frit. Oxidation and solution can proceed rapidly, with shunting of the junction or even complete shorting, depending on the depth of the junction and extent of the attack.

Preliminary screening tests have been run on a number of commercially available silver metallization pastes (Table 3-13). These tests consisted of fabricating solar cells using the firing time and temperature matrix given in Table 3-14. A shallower than normal junction depth (.18 - .2μm) was used in order to increase sensitivity of the test to the oxidation attack described above. This also tended to make the results somewhat more erratic. Paste firing was carried out in a flowing gas atmosphere consisting of 1500 cc/min. N_2 and 1500 cc/min. O_2 to further increase the sensitivity.

Curves obtained on cells fabricated with two different pastes with 650°firing temperatures are shown in Figures 4 and 5. Cell output, insensitivity of curve shape to location in the matrix of Table 3-14 and adhesion were used as criteria of merit. On this basis the pastes listed in Table 3-15 were selected for further evaluation. The observed current at 400 mV load point for these pastes are reported in Tables 3-16 through 3-21.

Aluminum front contact metallization does not appear to be promising. We have so far been unable to obtain contacts which do not show very large shunting and series resistance.

Table 3-13

COMMERCIAL SILVER PASTES
EVALUATED FOR USE AS COLLECTOR METALLIZATION

Cermalloy 4450
DuPont 7095
Electro-Science Laboratories 590
Englehard A2735
Englehard A2921 (Mod. 025)
Englehard A3233
Englehard E439A
Englehard E439B
Englehard E439C
Plessey L15-1260-T1
Thick Film Systems A-250
Thick Film Systems A-256
Thick Film Systems A-268
Thick Film Systems 3330

Table 3-14

TIME-TEMPERATURE MATRIX
USED FOR PASTE EVALUATION

	650°C	700°C	750°C
15 Sec.	void	X	X
30 Sec.	X	X	X
45 Sec.	X	X	X
60 Sec.	X	X	X
75 Sec.	void	X	X
90 Sec.	X	X	X
120 Sec.	X	void	void
180 Sec.	X	void	void

Table 3-15

PASTE RETAINED FOR FURTHER EVALUATION

DuPont 7095
Electro-Science Laboratories 590
Englehard A2921 Mod. 025
Englehard E439B
Thick Film Systems A250
Thick Film Systems A256

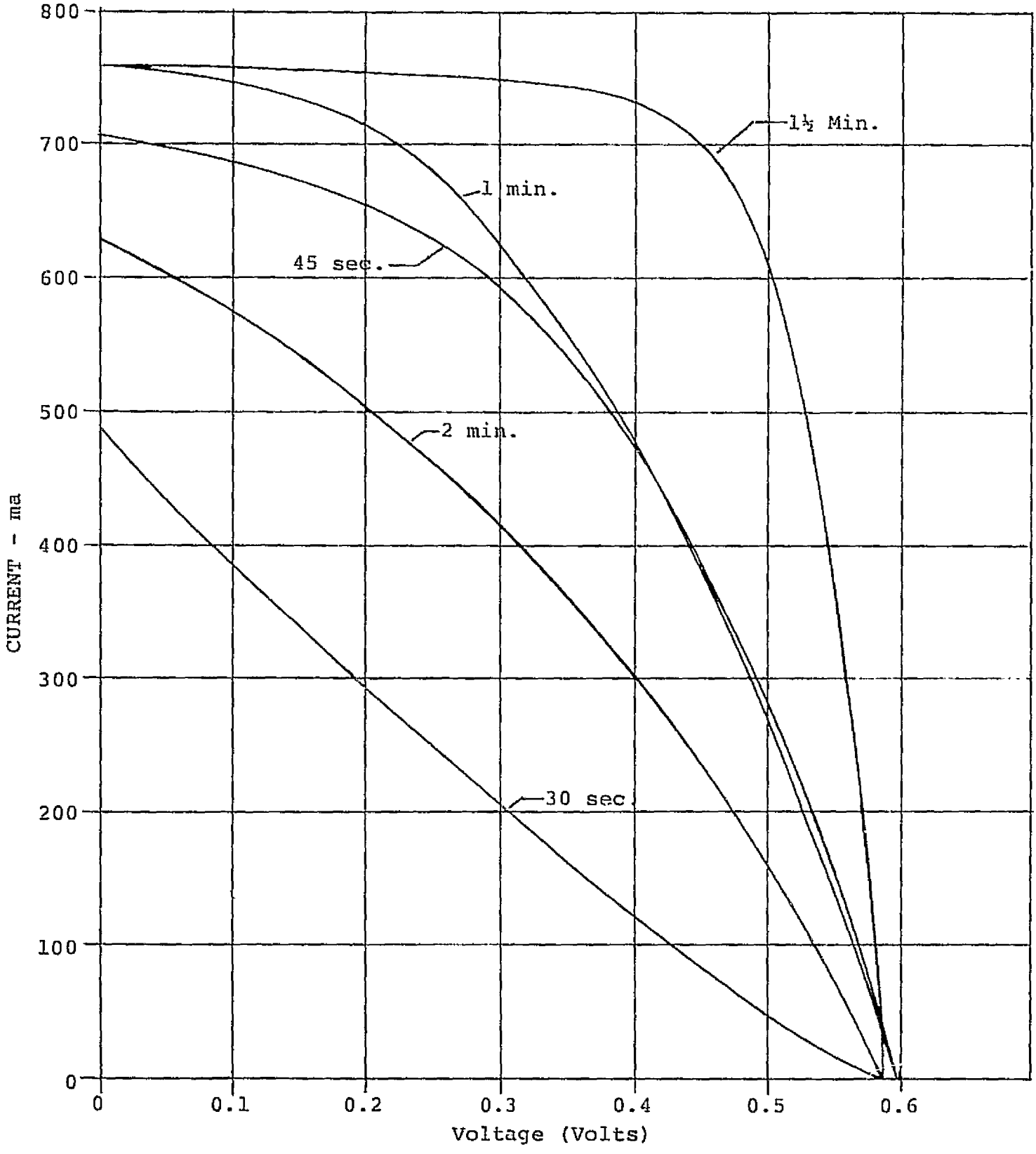

Figure 4. EFFECT OF FIRING TIME AT 650°C ON CURVE SHAPE, PASTE A

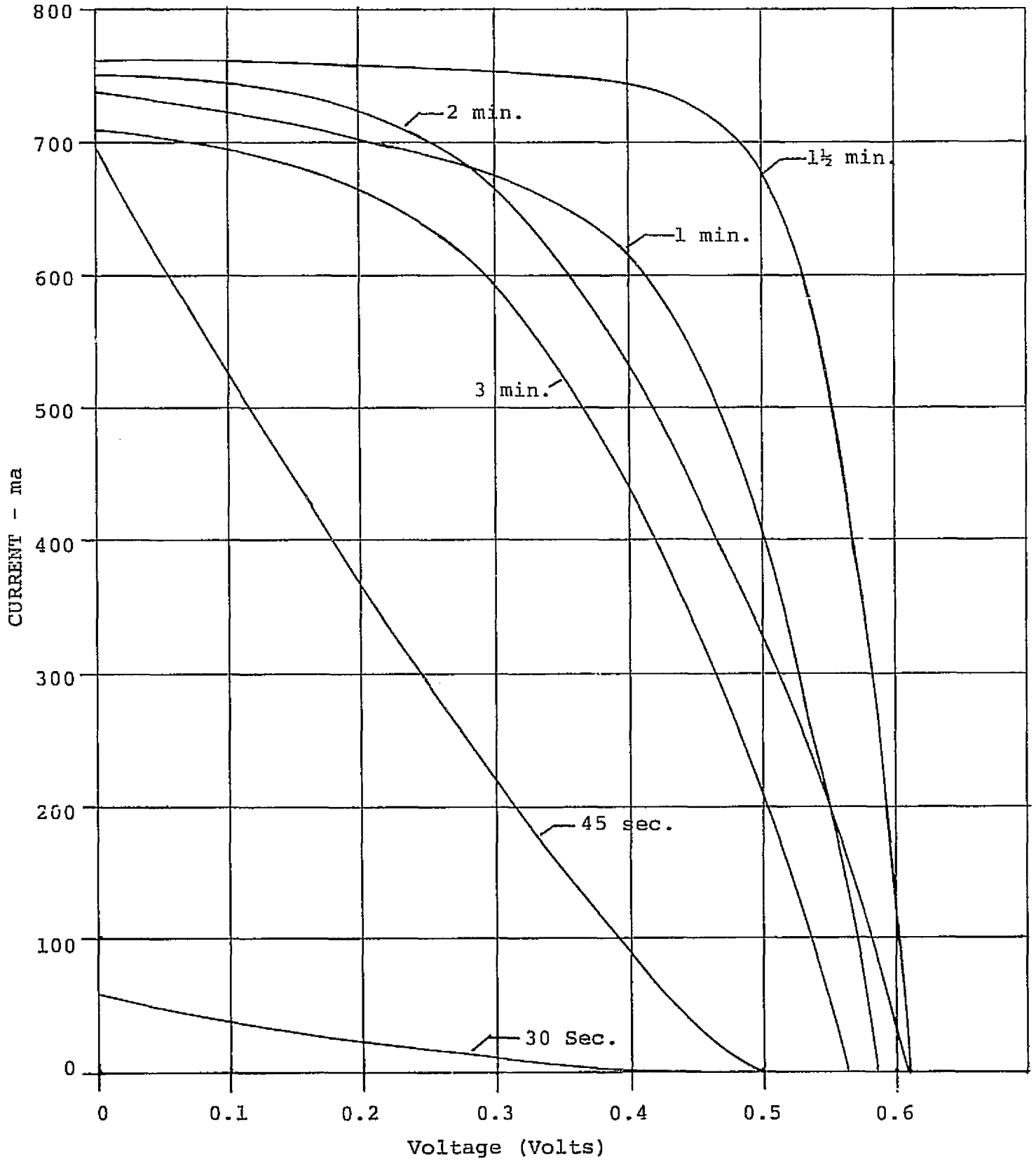

Figure 5. EFFECT OF FIRING TIME AT 650°C ON CURVE SHAPE, PASTE B

Table 3-16

EVALUATION MATRIX, FRONT CONTACT METALLIZATION
Paste: DuPont 7095

I_{400} - ma

	650°C	700°C	750°C
15 Sec.		662	447
30 Sec.	578	405	530
45 Sec.	630	380	447
60 Sec.	622	380	220
75 Sec.		390	295
90 Sec.	570	412	275
180 Sec.	340		
270 Sec.	455		

Table 3-17

EVALUATION MATRIX, FRONT CONTACT METALLIZATION
Paste: Electro-Science Laboratories 590

I_{400} - ma

	650°C	700°C	750°C
15 Sec.		718	680
30 Sec.	700	714	636
45 Sec.	693	684	550
60 Sec.	660	660	415
75 Sec.		665	390
90 Sec.	700	590	310
180 Sec.	670		
270 Sec.	655		

Table 3-18

I_{400} EVALUATION MATRIX, FRONT CONTACT METALLIZATION
Paste: Englehard A2921 (Modification 025)

	I_{400} - ma					
	650°C		700°C		750°C	
15 Sec.			660 673	628 440	710 590	610 540
30 Sec.	593 650	480 550	710 619	592 530	694 303	584
45 Sec.	650 670	503 465	684 554	560 440	609 538	448 125
60 Sec.	597 645	228 504	624 487	500 403	538 0	430
75 Sec.			475 380	368 378	485 0	420
90 Sec.	465 613	348 542	500 470	355 382	468 325	448 0
180 Sec.	390 391	381 580				
270 Sec.	270 252	274				

Table 3-19

I_{400} EVALUATION MATRIX, FRONT CONTACT METALLIZATION
Paste: Thick Film Systems A250

I_{400} - ma

	650°C		700°C		750°C	
15 Sec.			395	544	530	665
30 Sec.	330	690	468	648	530	375
45 Sec.	425	685	485	700	520	678
60 Sec.	365	670	528	668	397	620
75 Sec.			485	705	568	571
90 Sec.	318	718	523	671	230	625
180 Sec.	348	583				
270 Sec.	518	583				

Table 3-20

I_{400} EVALUATION MATRIX, FRONT CONTACT METALLIZATION
Paste: Englehard E439B

I_{400} - ma

	650°C	700°C	750°C
15 Sec.		738	687
30 Sec.	675	655	650
45 Sec.	647	690	600
60 Sec.	706	695	562
75 Sec.		615	485
90 Sec.	684	520	338
180 Sec.	661		
270 Sec.	541		

Table 3-21

I_{400} EVALUATION MATRIX, FRONT CONTACT METALLIZATION
Paste: Thick Film Systems A256

	I_{400} - ma		
	650°C	700°C	750°C
15 Sec.		474	630
30 Sec.	692	670	584
45 Sec.	632	580	460
60 Sec.	692	610	310
75 Sec.		--	--
90 Sec.	634	--	--
180 Sec.	--		
270 Sec.	--		

3.5 SUPERSTRATE ASSEMBLY

A variety of coating-encapsulant and adhesive type materials has been considered both for cell bonding and module backside protective coating applications. Products which were procured for screening are listed in Table 3-22.

Table 3-22

COATING/ENCAPSULANT MATERIALS

1.	RTV 615 Silicone Primers 4126 and 4155	G.E.
2.	Sylgard 184 Silicone	Dow Corning
3.	R-4-3117 Silicone Coating	Dow Corning
4.	3140 RTV Silicone Coating	Dow Corning
5.	Q1-2577 Silicone Coating	Dow Corning
6.	Q1-2577 Impregnated Mica	Dow Corning
7.	Densil Double Backed Tape	Dennison
8.	Versilock 510 Acrylic Adhesive	Hughson Chemicals
9.	Rexite IMR Acrylic Adhesive	Franklin Chamical
10.	EA9446 A/B Acrylic Adhesive	Hysol
11.	LO-524/525 Acrylic Adhesive	Loctite Corporation
12.	DA-560-4 U.V. Curable	Ciba Geigy
13.	Loctite 353 U.V. Curable	Loctite Corporation
14.	Acryloid B-7 Acrylic Adhesive	Rohm and Haas
15.	Epon 828/Versamid 125	Shell Chemical/ General Mills
16.	QR-568/Desmodure N-75	Rohm and Haas/ Mobay Chemical

A part of the screening function involved consideration of the various properties necessary and/or desirable in materials for these applications. Tables 3-23 and 3-24 give criteria used for adhesive materials and coating materials respectively. Many of the same individual properties appear in both tables, but priorities can differ significantly. The order of listing reflects

tentative judgment of relative importance in the corresponding applications. This is necessarily a rather approximate type of ranking and cannot be considered firm in detail because of complicating factors such as interrelationships between different properties and the range of impact of different properties on system performance. In general, improvement of performance is directly related to improvements in properties. However, some properties have a threshold requirement equivalent to a "go no-go" level, but might then provide little benefit from further involvement. Properties in these tables judged to be in this category are indicated by an asterisk.

Preliminary cell bonding experiments showed some problem areas in this operation. These included relative displacement between cells and superstrate because of sliding at the glue line before the adhesive set, creeping of adhesive around the edge of cells onto unbonded back surfaces, and bubble entrapment in the glue line.

The cell-glass displacement problem reflects the difficulty in holding individual cells in place during assembly and cure operations. This is expected to be less of a problem in an automated system which could be designed with individual cell holding devices.

Adhesive creeping around onto cell back surfaces appeared to be mainly the result of capillary action. The use of a flat pressure plate to hold the cells down against the glass resulted in the two surfaces, glass and pressure plate, so close together that any adhesive squeezed from the glass-cell bond line filled the space around the cell periphery and was drawn into the cell-pressure plate interface by capillary action. Therefore, assembly procedures providing greater glass to pressure plate separation appear desirable.

Table 3-23

ADHESIVE CRITERIA

1. Cost/Watt
2. Light Transmission
*3. Ultraviolet Radiation Resistance
*4. Thermal and Thermal Cycling Resistance
*5. Low Elastic Modulus
*6. Thermal Expansion Compatibility
7. Viscosity, Compatibility with Assembly Process
8. Long Pot Life
9. Short Cure Time
*10. Environmental Stability
*11. Cost/Pound
*12. Bond Strength
*13. Uniform Bubble Free Bond Line

*Properties having a threshold requirement character.

Table 3-24

BACK COATING CRITERIA

1. Cost/Watt
2. Permeability, Liquids and Vapors
*3. Weatherability
*4. Thermal and Thermal Cycling Resistance
*5. Bond Strength
6. Uniform Void Free Coating
7. Cost/Pound
*8. Low Elastic Modulus
*9. Mechanical Strength
*10. Thermal Expansion Compatibility
11. Long Pot Life
12. Short Cure Time
*13. Ultra Violet Radiation Resistance
14. Viscosity, Compatibility with Application Method
15. Light Transmission

*Properties having a threshold requirement character.

The light transmission specimens consisted of a capillary film of test material cured between glass microscope cover slips. Acceptance was based on specimen transmission as tested above 95%. Some judgment considerations realtive to shape of spectral curve were also involved.

The cell bonding experiments provided criteria for evaluation of processability. "Spreading" or "Running" failure is indicative of too high and too low viscosities respectively. Bubbles are mainly a processing variable but also can be related to materials properties such as residual solvent or tackiness in film type adhesives. Cure time acceptability was set at 15 minutes. Shorter times would clearly be desirable, and this limit may be lowered if feasible.

Table 3-26 shows results of bond strength tests. Bond strength evaluation for screening purposes consisted of testing lap shear specimens in which the test material was used to bond cell front surfaces to glass. Specimens consisted of appropriate sized cell fragments prebonded to a backing plate and then bonded with the test material to a microscope slide. The microscope slide provides a convenient 1" wide glass member and the bond can be made with a measured overlap in the configuration of a standard lap shear specimen. Most materials also required a metal backing bonded to the glass in order to provide strength enough to insure fracture at the test joint. In fact the bending moment at the joint was such that stronger adhesives caused the brittle glass and cell material to crack in a fragmented pattern which tended to reduce apparent bond strength by reducing effective areas of bond.

The bubble problem apparently resulted primarily from air entrapment when two precoated surfaces were joined. Therefore, testing was directed toward development of an assembly procedure in which precoating is not used, and the adhesive is applied so that it spreads over the bonding surfaces as they are brought together. This minimizes bubbles by driving air out ahead of the advancing glue line.

In connection with these cell bonding experiments, attention was also directed toward the need for methods which have potential for development into automated procedures. The most promising to date involves laying the cells out in the prescribed array then bonding by placing the superstrate on top of this array.

This procedure uses a cell support fixture which consists of an array of pedestals of a flexible material. These pedestals, about 1/8" smaller than the cells, are positioned on a flat surface in a pattern corresponding to the module cell layout. The cells positioned on these supports are then bonded by applying a measured amount of adhesive to the face of each cell, positioning the glass superstrate over the array and lowering it into place.

The individual flexible supports provide essentially equal pressure between each cell and the superstrate. The total pressure required is a function of minimum adhesive viscosity during cure. The individual supports also provide a friction holding force which tends to prevent lateral cell displacement. Therefore, a single set of stops to hold the superstrate is all that is needed to prevent displacement during cure.

Results of adhesive materials screening tests which have eliminated some of the candidate materals are shown in Table 3-25. Entries in the first column, Light Transmission, were based on spectrophotometric tests. The rest of the chart is based on cell bonding experiments.

Table 3-25

LIGHT TRANSMISSION AND CELL BONDING TESTS

	Light Trans	Cure Time	Spreading	Running	Bubbles
Densil	FAIL	OK	OK	OK	FAIL
RTV 615	OK	OK	OK	OK	OK
Q1-2577 (B Stage)	FAIL	OK	OK	OK	OK
Versilock 506	FAIL	OK	FAIL	OK	OK
DA-560-4	OK	OK	OK	OK	OK
Loctite 373	OK	OK	OK	OK	OK
Rexite	OK	OK	FAIL	OK	OK
EA 9446	FAIL	OK	OK	OK	OK
Acryloid B-7	OK	OK	NA	NA	FAIL
Epon 828/Versamid	OK	OK	OK	OK	OK

Table 3-26

LAP SHEAR TESTS

	Primer	Cure	Bond Strength*
RTV 615		24 hrs R.T.	23 psi
RTV 615	4120	24 hrs R.T.	31
RTV 615	4155	24 hrs R.T.	30
RTV 615		72 hrs R.T.	36
RTV 615	4120	72 hrs R.T.	58
RTV 615	4155	72 hrs R.T.	53
RTV 615		1 hr 100°C	108
RTV 615	4120	1 hr 100°C	127
RTV 615	4155	1 hr 100°C	95
Q1-2577-Mica		1 hr 80°C 12 psi	100
Q1-2577-Mica	1204	1 hr 80°C 12 psi	80
Versilock		72 hrs R.T.	375
Loctite 353		72 hrs R.T.	355
DA-560-4		72 hrs R.T.	255

*Average of two measurements.

Some of the candidate materials have been eliminated by these screening tests. The Densil tape and Acryloid B-7 showed bubbles or unbonded areas. The Versilock 506, Rexite IMR, EA9446 and LO-524/525 showed relatively poor light transmission, and probably will be eliminated. However the better of these materials may still warrant some consideration because the bonding mechanism could be very attractive for an automated system. This consists of application of resin and accelerator to separate surface which are then pressed together to bond. The cure is at room temperature and requires only a few minutes.

The silicones as a group have poor bond strength, but it may be adequate because initial system stresses are very low. Also, silicones have been widely used because their low modulus is desirable for resistance to thermal stresses.

Silicones, Locktite 353 and Epon 828/Versamid 125 have been selected for more detailed investigation.

3.6 AUTOMATION CONCEPTS

3.6.1 Edge Masking Dielectric

A design concept has been worked out for coating wafer edges with masking dielectric by a roll transfer shown schematically in Figure 6. Cells entering from the left are transferred by a walking beam mechanism to pedestals on a moving belt which passes through the firing furnace. Before entering the furnace, the cells are picked up by articulated arms and the edges applied to a roll which transfers dielectric paste from a reservoir to the cell edges in a controlled fashion. After coating, the cells are returned to their pedestals and the beld advanced to position the next row of cells for pick-up. We have estimated the throughput of such an equipment to be 8540 4" cells per hour (5 second cycle time). Twelve coating

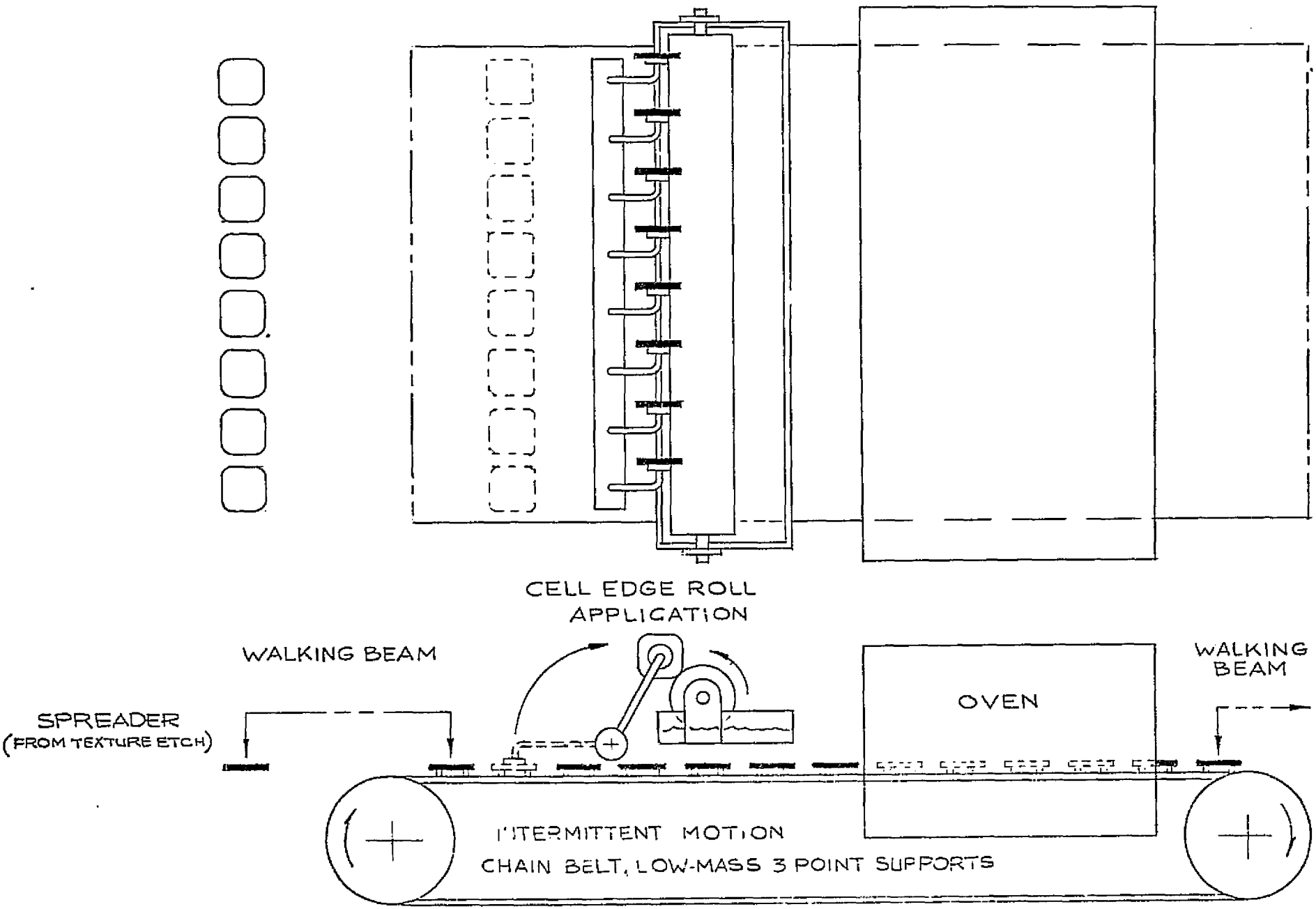

Figure 6. CONCEPTUAL DESIGN OF AUTOMATED FACILITY FOR COATING WAFER EDGES

stations would be required for 500 megawatts per year production capacity. We believe that equipment of this type will be suitable for round or partially shaped cells but would encounter some difficulties with perfect squares and may not be adaptable to rectangular shapes.

The projected cycle time results in a belt speed of 4 feet per minute, suggesting furnace size problems for firing times which might be as long as 15 minutes (60 feet of furnace profile), plus heating and cooling gradients.

3.6.2 Superstrate Assembly

A design concept for the superstrate assembly is shown in Figure 7. At the adhesive application station, the cells for an entire superstrate are accurately located in a grid array. Cells are presented face up for automatic application of adhesive by mechanized dispensing heads. By applying a controlled amount of adhesive at the centers of the cells, bubble free adhesive joints will be obtained when the superstrate glass is lowered onto the adhesive mounds which then spread due to the weight of the glass.

After adhesive application, the grid of cells is advanced to the glassing station. At this station the superstrated glass is transferred by vacuum pick-up arms and accurately positioned on the cell array. The assembly is then moved to another station where time is provided for the adhesive to flow to the edges of the cell. After inspection, the assembly advances into an oven where the adhesive is cured.

The superstrate is then inverted to display the back sides of the cells for interconnection. This is projected to be an automatic reflow soldering process using copper braid interconnect conductors.

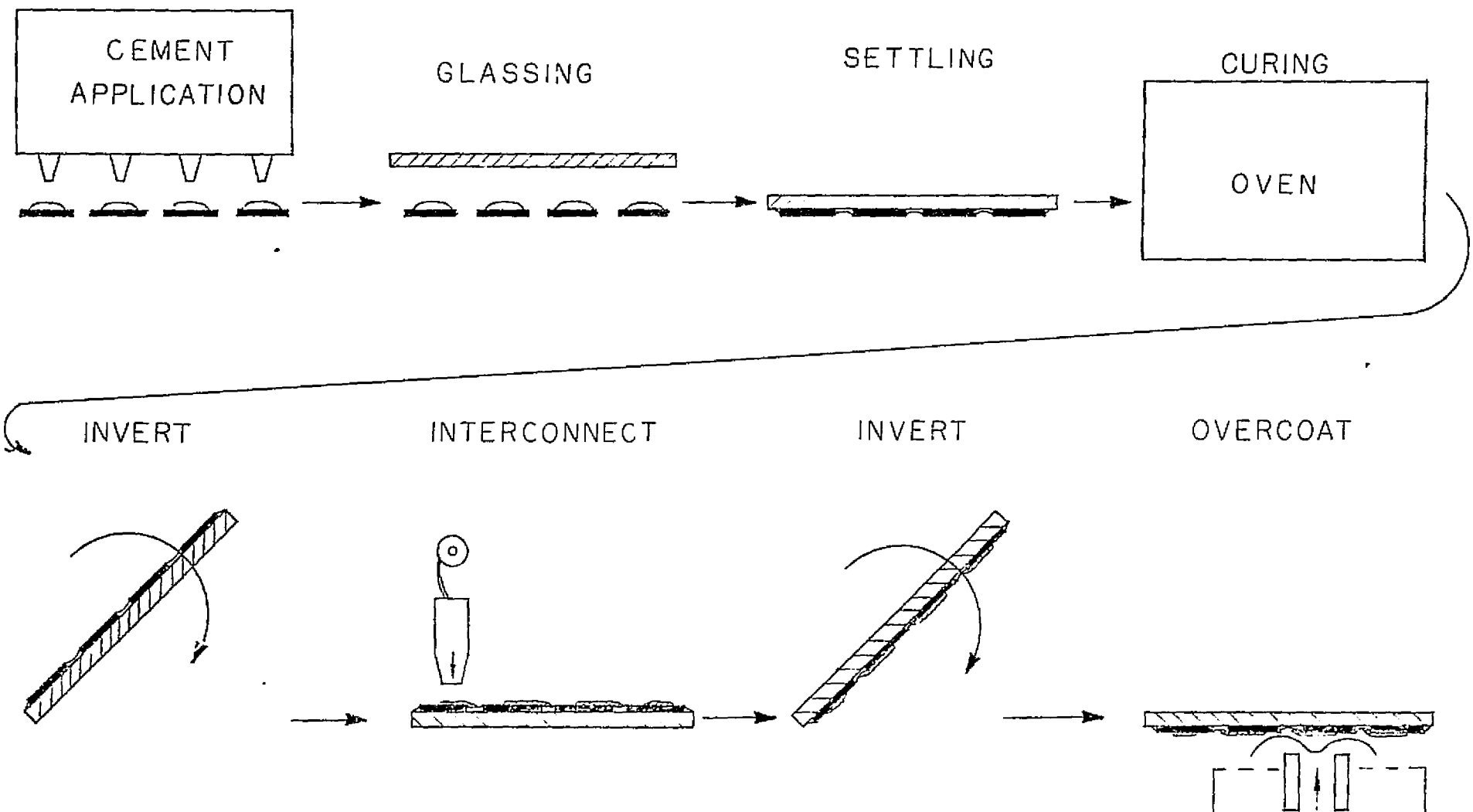

Figure 7. CONCEPTUAL DESIGN OF AUTOMATED SUPERSTRATE ASSEMBLY

A second inversion presents the interconnected solar cell circuit on the lower side of the glass. In this position, the superstrate moves continuously through a solvent spray flux removal tank and through an overcoating station. This might be a wave coating process as shown or alternatively could be a spray coating, curtain coating or other suitable process.

4.0 CONCLUSIONS

The following conclusions are drawn on the basis of the work reported:

1. Use of sheet material from Czochralski crystals will encounter significant incremental costs for nesting inefficiencies and shaping.

2. A single step texture etching process is suitable for wafers cut by multiple blade slurry saws. This is probably also true for wafers shaped by other methods, but should be verified before adopting.

3. Cofiring aluminum paste back contacts during the diffusion process is not feasible, but the aluminum can be fired through a diffused n type layer without back etching.

5.0 RECOMMENDATIONS

There are no recommendations.

6.0 NEW TECHNOLOGY

There was no new technology reported during the quarter.

7.0 REFERENCES

1. B. Carbajal, Automated Array Assembly Task, Phase I, (Dallas Texas: Texas Instruments, Inc.) JPL Contract 954405, Annual Report (March, 1977), ERDA/JPL-954405-77/4.

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