NASA TECHNICAL MEMORANDUM

NASA TM-78900

NASA TM-78900

MEDIUM POWER VOLTAGE MULTIPLIERS WITH A LARGE NUMBER OF STAGES

by W. T. Harrigill and I. T. Myers
Lewis Research Center
Cleveland, Ohio 44135

TECHNICAL PAPER to be presented at the
Power Electronics Specialists Conference
sponsored by the Institute of Electrical and Electronics Engineers
Syracuse, New York, June 13-15, 1978

MEDIUM POWER VOLTAGE MULTIPLIERS WITH A LARGE NUMBER OF STAGES

W. T. Harrigill and I. T. Myers

National Aeronautics and Space Administration
Lewis Research Center
Cleveland, Ohio 44135

ABSTRACT

Voltage multiplier techniques were extended at medium power levels to larger multiplication ratios. A series of DC-DC converters were built, with from 20 to 45 stages and with power levels up to 100 watts. Maximum output voltages were about 10,000 volts.

E-9636

INTRODUCTUION

Previous work (1-5) has proven that capacitor diode voltage multiplier (CDVM) DC-DC conversion with efficiencies up to 96 percent and at power levels up to 1 kW is possible. The multiplication factor, or ratio of DC output to DC input voltage in this previous work was about 8 or 10. This paper discusses the extension of this multiplication ratio for medium power multipliers, and explares large multiplication ratios in terms of efficiency, weight, and operating characteristics. Multipliers with twenty to forty-five stages were examined both analytically and experimentally. Emphasis was placed on high efficiency and light weight. Some large multiplication ratio work has already been reported in the literature (6-11). However, the converters were of low power and efficiency was not of primary concern.

EQUATIONS FOR LOAD VOLTAGE DROOP, OUTPUT RIPPLE, AND LOSSES

The voltage multiplier used was of the type shown in figure 1. The multiplication ratio, at low power, is approximately equal to the number of stages. Each stage includes 2 capacitors and 2 diodes. Descriptions of the transistor drive and control circuits have previously been reported (1-4) and will not be repeated here.

The output voltage was determined using techniques previously described by Harrigill and Myers (1-4), Brugler (12), and Borneman (13). The average value of the load voltage, V_L, is:

$$V_L = sV_i - \frac{i_L(s)(s+1)(2s/3 + 1/12)}{fC} \qquad (1)$$

where

- s number of multiplier stages
- i_L load current
- f chopping frequency
- C individual capacitor values
- V_i imput voltage

For large values of s, the average output voltage, within a few percent, can be written as:

$$V_L = sV_i - \frac{2i_L s^3}{3fC} \qquad (2)$$

The first term, sV, is the no load voltage and may be considered analogous to the internal voltage of a generator. The second term, $2i_L s^3/3fC$, is the load voltage droop due to capacitor charging losses in the voltage multiplier.

This series voltage drop in the voltage multiplier gives rise to a power loss of $2s^3 i_L^2/3fC$. In addition to the DC output voltage V_L, a ripple voltage V_R with a frequency of f is superimposed on the output. This ripple voltage has a peak to peak value of

$$V_R = \frac{i_L(s)(s+1)}{2fC} \qquad (3)$$

For large multiplication ratios, the droop voltage, which is a function of s^3, is much larger than the ripple voltage, which is a function of s^2.

In addition to the capacitor charging loss, there are other losses. See reference (2) and tables I and II. Note that one loss is proportional to i_L^2, several are proportional to i_L, and some are independent of i_L. This suggests that a maximum efficiency exists at some load current. In order to determine this point of maximum efficiency, an expression for efficiency in terms of i_L was formulated and its derviative with respect to load current set equal to zero. The efficiency η is equal to

STAR Category 20

$$\eta = \frac{P_{input} - P_{losses}}{P_{input}} \tag{4}$$

$$P_{input} = I_{input} V_{input} \tag{5}$$

For a well designed voltage multiplier, the input current is very nearly equal to the number of stages s times the load current.

Thus

$$\eta = \frac{i_L sV - k_1 sV - k_2 sVi_L - k_3 sVi_L^2}{i_L sV} \tag{6}$$

where k_1, k_2 and k_3 are constants defined by:

$$k_1 = 2C_{DR}Vf + 2C_{TR}Vf + 4i_{DR} + \frac{2i_{T,off}}{s} \tag{7}$$

$$k_2 = \frac{2V_{DF}}{V} + \frac{2V_{TF}}{V} + \frac{2V_d}{V\beta} + \frac{2\pi^2}{3}\left(\frac{\tau_T}{\tau_{IT}}\right)^2 + \frac{\pi^2}{3}\left(\frac{\tau_D}{\tau_{ID}}\right)^2 \tag{8}$$

$$k_3 = \frac{(s+1)(2s/3 + 1/12)}{fCV} \simeq \frac{2s^2}{3fCV} \tag{9}$$

where the symbols have been previously defined.

The losses given by sVk_1 are independent of load current, the losses given by the k_2 term (sVk_2i_L) are proportional to load current, and the k_3 term losses ($2s^3i_L^2/3fC$) are proportional to the square of the load current. The efficiency η can then be written in terms of k_1, k_2, k_3 and i_L as

$$\eta = 1 - \frac{k_1}{i_L} - k_2 \quad k_3 i_L \tag{10}$$

Setting $d\eta/di_L = 0$ gives

$$i_L(\text{max efficiency}) = \sqrt{\frac{k_1}{k_3}} \tag{11}$$

and

$$\eta_{max} = 1 - 2\sqrt{k_1 k_3} - k_2 \tag{12}$$

The trend in the efficiency versus load current curve, and the variation in efficiency with the number of stages s, is shown in the experimental results section.

OPTIMIZING THE NUMBER OF STAGES FOR A GIVEN OUTPUT VOLTAGE

It is desirable to select the minimum size (and weight) multiplier for a given application. The output voltage for a voltage multiplier of the type shown in figure 1 was given in equation (1) as

$$V_L = sV - \frac{s(s+1)(2s/3 + 1/12)i_L}{fC}$$

The value of capacitance C required for each position in the multiplier is:

$$C = \frac{s(s+1)(2s/3 + 1/12)i_L}{f(sV - V_L)} \tag{13}$$

Normally, i_L and V_L are fixed by the load. The frequency f is also fixed or limited by stray inductances or losses. The number of stages s, however, may be varied.

The total capacitance C_T is

$$C_T = 2sC, \text{ or} \tag{14}$$

$$C_T = \frac{2s^2(s+1)(2s/3 + 1/12)i_L}{f(SV - V_L)} \tag{15}$$

One can now determine the optimum s by differentiation of C_T with respect to s, and setting the resultant expression equal to zero. From a strict mathematical standpoint this is not possible, since s occurs in discrete, integral values. For this treatment, however, s will be considered continuous, and the nearest integral value taken.

$$\frac{dC_T}{ds} =$$

$$= i_L(sV - V_L)\frac{(s+1)\left(\frac{2s}{3}+\frac{1}{12}\right)+s\left(\frac{2s}{3}+\frac{1}{12}\right)+s(s+1)\left(\frac{2}{3}\right)}{f(SV - V_L)^2}$$

$$- \frac{i_L s(s+1)\left(\frac{2s}{3}+\frac{1}{12}\right)V}{f(SV - V_L)} = 0 \tag{16}$$

If we take the case with large s

$$(sV - V_L)2s^2 = \frac{2s^3}{3}V, \text{ or } s = \frac{3}{2}\frac{V_L}{V} \tag{17}$$

Substituting into the expression for C_T, again for the case of large s, gives:

$$C_T = \frac{27V_L^3 i_L}{2fV^4} \tag{18}$$

and the capacitance per unit stage is

$$C = \frac{C_T}{2s} = \frac{9}{2}\frac{V_L^2 i_L}{fV^3} \tag{19}$$

Since the efficiency of the converter is $i_L V_L / i_{in} V$, and the input current is very closely equal to si_L, for the minimum total capacitance case the efficiency η_M is

$$\eta_M = \frac{V_L}{sV} = \frac{2}{3} \qquad (20)$$

EXPERIMENTAL RESULTS

A series of large multiplication ratio voltage multipliers were built using 10 microfarad polyvinylidene fluoride capacitors and fast switching diodes. The input was 255 V dc. Switching was provided by npn transistors driven by small pulse transformers. The operational parameters of the multiplier are given in table III.

Alternate circuit approaches could have been taken. For example, a bridge circuit could have been used for the switching transistors, providing double the voltage output with the same number of stages. However, this would require 4 transistors instead of two. No regulator was used, although one could have been incorporated. (See ref. 3). The purpose of this work was to develop the technology of large multiplication ratio voltage multiplier power supplies for high power rf tubes; regulation, ripple, dynamics response and other requirements will depend upon the particular application involved.

Figure 2 gives the voltage change with load for different multiplications. (25 stages means 25 times multiplication) Calculated load voltages are given by the solid lines. Agreement between calculated and experimental results are seen to be reasonably good. Figure 3 shows the efficiency as a function of load with the number of multiplier stages as a parameter. As expected, the efficiency decreases with increasing number of stages, but still remains in the middle and high 80 percent range for reasonable capacitor sizes. As can be seen from figure 3, 100 watts was near the peak in the efficiency curve. For applications where somewhat lower efficiencies could be tolerated, it would be possible to operate the multiplier at higher power with the same capacitors. In general, the ripple was small, of the order of one percent, due to the self filtering action of the multiplier capacitors.

CONCLUSIONS

Medium power, high multiplication ratio voltage multiplier DC-DC converters were investigated. The following results and conclusions were obtained.

1. A series of capacitor diode voltage multipliers with 20 to 45 stages were built and evaluated. A multiplier with 45 stages and 10,000 volts output demonstrated 83 percent efficiency at 100 watts output power.

2. Experimental measurements plus analysis indicates the efficiency of a given configuration of voltage multiplier increases with power output, goes through a maximum, and decreases at higher power.

3. The power level corresponding to the point of maximum efficiency may be varied by varying the amount of capacitance in the multiplier.

4. The efficiency decreases with increasing number of multiplier stages.

5. No fundamental limits to higher multiplications were found.

6. Large power high multiplication ratio voltage multipliers can be built, within component limitations.

7. Theoretical predictions of efficiency and voltage output agree reasonably well with measured values.

REFERENCES

(1) W. T. Harrigill, Jr. and I. T. Myers, "High Performance DC-DC Conversion with Voltage Multipliers," NASA TM X-71566, presented at IEEE Power Electronics Specialists Conference, June 10-12, 1974.

(2) W. T. Harrigill, Jr. and I. T. Myers, "Efficiency and Weight of Voltage Multiplier Type Ultra Lightweight DC-DC Converters," NASA TM X-71735, presented at IEEE Power Electronics Specialists Conference, June 9-11, 1975.

(3) W. T. Harrigill, Jr. and I. T. Myers, "Regulation of a Lightweight High Efficiency Capacitor Diode Voltage Multiplier DC-DC Converter," NASA TM X-73427, presented at the IEEE Power Electronics Specialists Conference, June 8-10, 1976.

(4) J. J. Kisch and R. M. Martinelli, "High Frequency Capacitor Diode Voltage Multiplier DC-DC Converter Development," NASA CR-135309, Sep. 1977.

(5) R. M. Martinelli, "Extended Performance Solar Electric Propulsion Thrust System Study, Volume V: Capacitor Diode Voltage Multiplier, Technology Evaluation," NASA CR-135281, Sep. 1977.

(6) E. Greinacher, "Über eine Methode, Wechselstrom Mittels Elektrischen Ventile und Kondensatorem in Hochgespannten Gleichstrom Umzuwandelen," Z. Phys. vol. 4, pp. 195-205, 1921.

(7) P. Lorrain, "On the Design of a Radiofrequency Cocheroft-Walton Accelerator," Rev. Sci. Instrum. vol. 20, pp. 216-217, 1949.

(8) E. Everhart and P. Lorrain, "The Cockcroft-Walton Voltage Multiplying Circuit," Rev. Sci. Instrum. vol. 24, pp. 221-226, 1953.

(9) T. P. Nowalk and G. D. Hajek, "High Voltage Solar Array Segment," Air Force Aero Propulsion Lab. TR-68-1, 1968.

(10) M. Spector, "Diode Technology is Key To Battlefield Intensifier," EDN Feb. 1, pp. 55-56, 1969.

(11) J. F. Sutton and J. E. Stern, "Spacecraft High Voltage Power Supply Construction," NASA TN D-7948, 1975.

(12) J. S. Brugler, "Theoretical Performance of Voltage Multiplier Circuits," IEEE J. Solid-State Circuits, vol. 6, pp. 132-135, 1971.

(13) E. H. Borneman, "Boost High-Voltage DC Outputs," Electronic Design, vol. 26, no. 7, pp. 72-74, 1978.

TABLE I. - DEFINITION OF SYMBOLS

C_{DR}	reverse junction capacitance of diode, F
C_{TR}	transistor "off" junction capacitance, F
C	unit CDVM capacitance, F
f	frequency, Hz
i_{DR}	reverse leakage current of diodes, A
i_L	load current, A
$i_{T,off}$	transistor "off" dc leakage current, A
s	number of stages
V_{DF}	diode conduction drop, V
V_d	transistor drive voltage, V
V_i	input voltage, V
V_{TF}	transistor average forward conduction drop, V
β	chopper transistor current gain
τ_D	diode switching time, sec
τ_{ID}	period of diode current, sec
τ_{IT}	period of transistor input current, sec
τ_T	transistor turn on time, sec

TABLE II. - LOSSES IN VOLTAGE MULTIPLIER

Loss type	Formula for loss
Capacitor charging loss	$2i_L^2 s^3/3fC$
Diode reverse junction charging loss	$2sC_{DR}V_i^2 f$
Transistor reverse junction charging loss	$2C_{TR}V_i^2 f$
Diode forward conduction losses	$2sV_{DF}i_L$
Transistor forward conduction losses	$2V_{TF}si_L$
Diode reverse bias dc leakage losses	$4V_i i_{DR}s$
Transistor "off" dc leakage losses	$2V_i i_{T,off}$
Transistor base drive loss	$2i_L V_d s/\beta$
Transistor switching losses	$(2\pi^2 V_i i_L s/3)(\tau_T/\tau_{IT})^2$
Diode switching losses	$(\pi^2 V_i i_L s/3)(\tau_D/\tau_{ID})^2$

TABLE III. - EXPERIMENTAL PARAMETERS

Input voltage	255 V dc
Output voltages	5000-11,000 V dc
Output power	30-120 W
Switching frequency	50 kHz

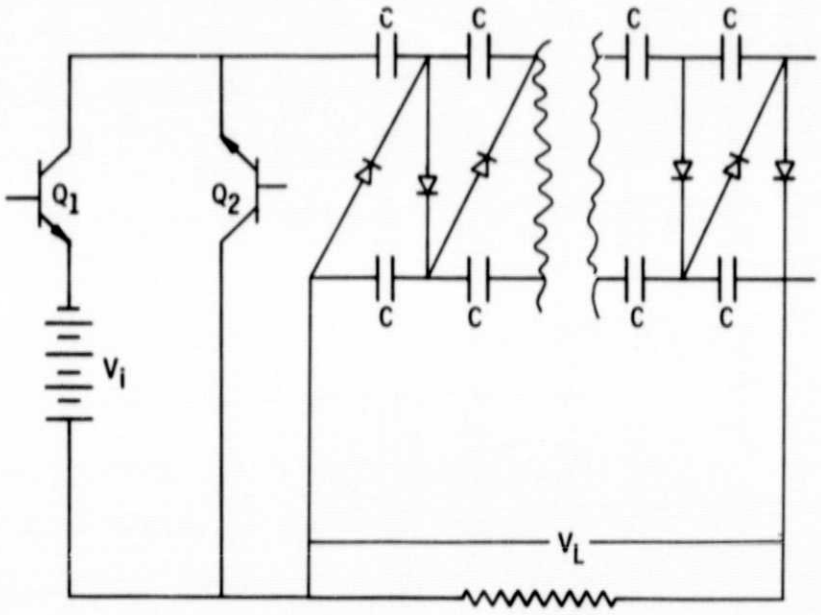

Figure 1. - Capacitor diode voltage multiplier.

E-3636

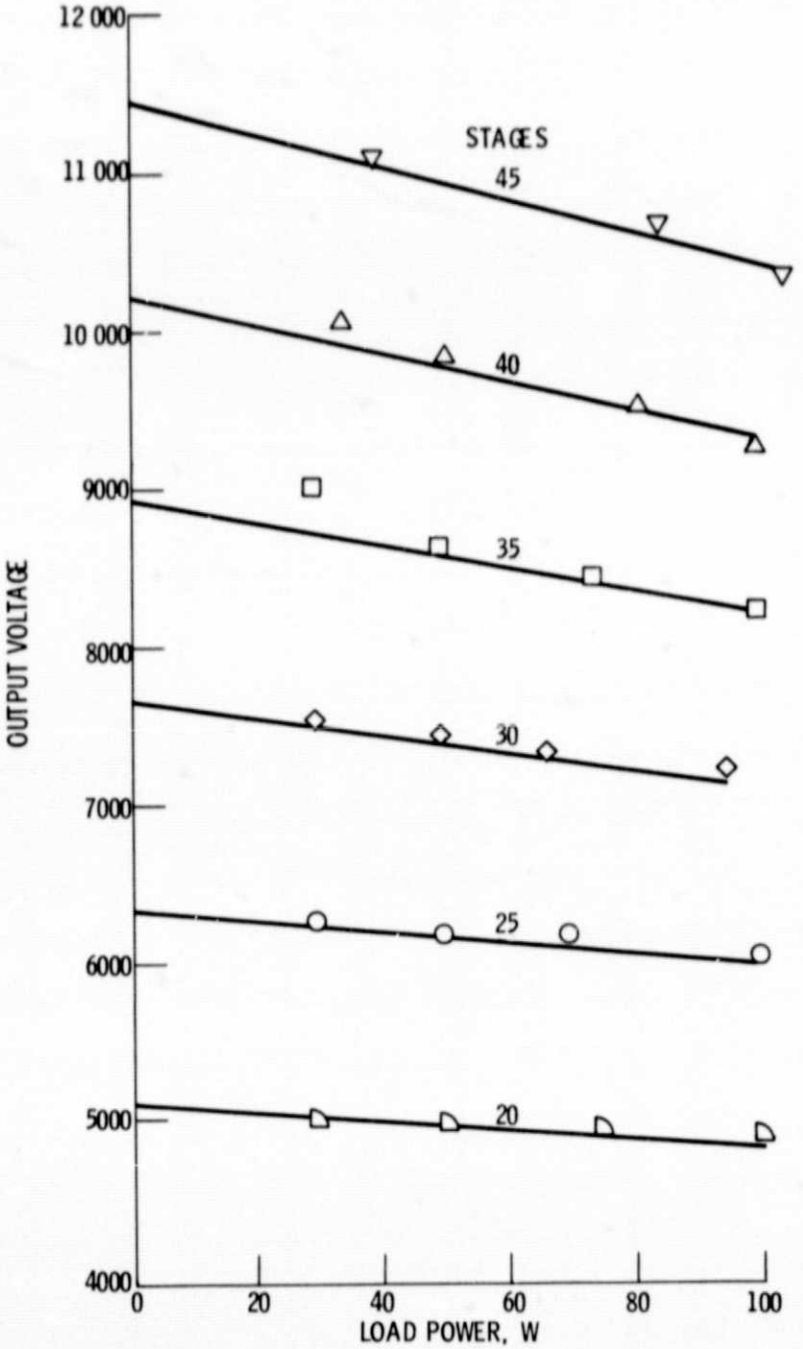

Figure 2. - Open loop voltage regulation of high multiplication voltage multipliers.

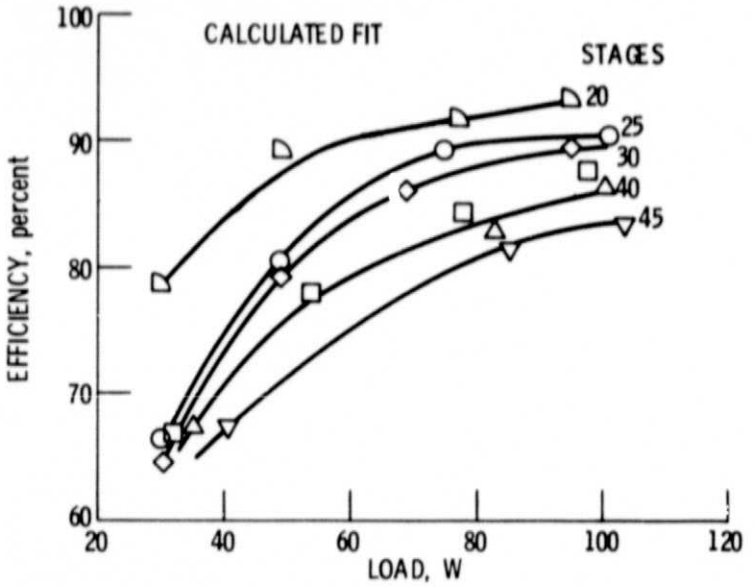

Figure 3. - Efficiency of high multiplication voltage multipliers.