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# AN INVERTER/CONTROLLER SUBSYSTEM OPTIMIZED FOR PHOTOVOLTAIC APPLICATIONS

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# AN INVERTER/CONTROLLER SUBSYSTEM OPTIMIZED FOR PHOTOVOLTAIC APPLICATIONS

Roy L. Pickrell, NASA Lewis Research Center, Cleveland, Ohio; George O'Sullivan, Abacus Controls Inc., New Jersey; and Walter C. Merrill, NASA Lewis Research Center, Cleveland, Ohio




## ABSTRACT

Conversion of solar array dc power to ac power stimulated the specification, design, and simulation testing of an inverter/controller subsystem tailored to the photovoltaic power source characteristics. This paper discusses the optimization of the inverter/controller design as part of an overall Photovoltaic Power System (PPS) designed for maximum energy extraction from the solar array. The special design requirements for the inverter/controller include: (1) a power system controller (PSC) to control continuously the solar array operating point at the maximum power level based on variable solar insolation and cell temperatures; and (2) an inverter designed for high efficiency at rated load and low losses at light loadings to conserve energy. It must be capable of operating connected to the utility line at a level set by an external controller (PSC). This paper is presented in three sections: (1) the overall PPS and PSC design (Utility Mode); (2) the inverter design and test results; and (3) a PPS analysis and simulation testing, conducted at LeRC to verify the design control concepts and fix design parameters.


## OVERALL PPS AND PSC DESIGN (UTILITY MODE)

In order to optimize the potential for photovoltaic energy to supplement or replace other energy sources, as much as possible of the solar array power capability should be extracted. The power available from the solar array is dependent upon the solar cell temperatures and the insolation level. This power may be used locally, stored, or transferred to the utility bus. In the utility mode operation of the subject PPS, the excess energy produced by the array over that demanded by the load is transferred to the utility bus, where it replaces conventionally generated power. If the solar array cannot fully supply the load demand, then the deficit is provided from the utility bus.

An examination of the current-voltage (IV) data in Fig. 1 shows the performance characteristics of a typical solar array (SA). For a specific temperature and solar insolation, there exists an IV point at which the power extracted from the SA is at its maximum. The maximum power (MP) points of Fig. 1 are shown connected by a dashed line. These MP points occur at approximately 0.8 of the open circuit SA voltage.

The ratio of the array voltage at which maximum power is extracted, to the open circuit voltage ($V_{MP}/V_{OC}$), suggested possible use of this relation as a control parameter to operate the solar array at its maximum power point. Test data were obtained to investigate the variation of the $V_{MP}/V_{OC}$ ratio with cell temperature and insolation. Results of these tests are shown graphically in Fig. 2. Analysis of the data show that for most of the operating range, the ratio will not deviate more than about ±2% from an arbitrary fixed value. Other data show that the array power is reasonably flat for up to ±5% voltage variation around the maximum power point. Therefore controlling the array voltage, by loading, to a level consistent with a fixed $V_{MP}/V_{OC}$ ratio (say 0.8) would not incur significant loss of power capability.

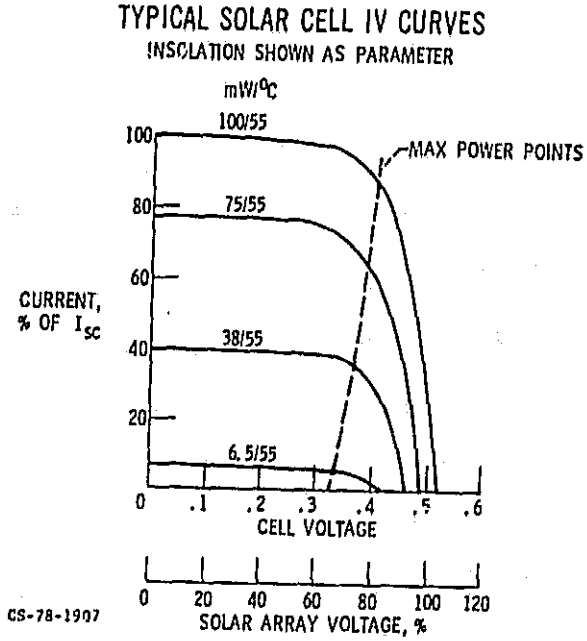



Figure 1.

The basic system concept shown in Fig. 3 was selected for a 10 kW (peak) solar power experiment. In this concept, the power system controller (PSC) derives the array target voltage level from an open circuited pilot cell array. By control of the magnitude of power (current) transferred to the utility bus, the PSC regulates the

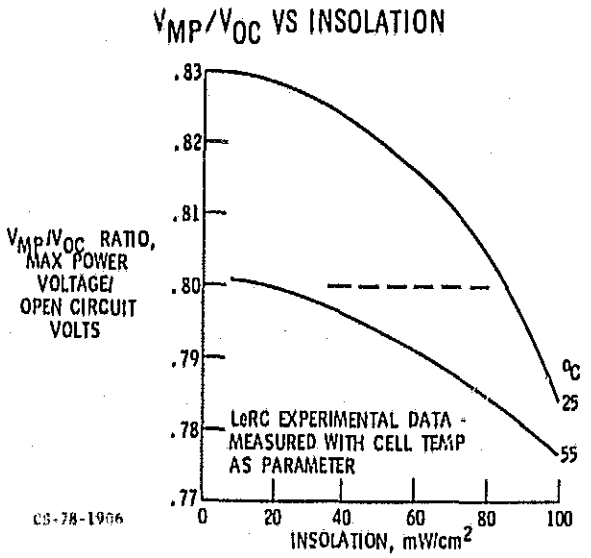



Figure 2.

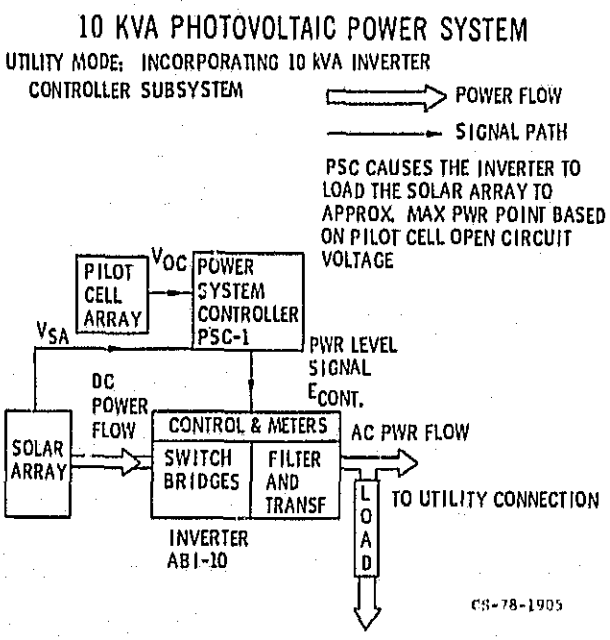



Figure 3.

output voltage of the solar array. Thus the array is regulated to a voltage level consistent with its maximum power capability, based on a reference level derived from the open circuit pilot cells. These pilot cells are located in the same environment as the array, and the pilot cell array output voltage reflects changes in both the solar array insolation level and cell temperature.

This system concept requires an inverter which can respond to signals from the PSC to load the solar array. In this PPS, the inverter must be capable of operation connected to a utility bus. The inverter design and tests are discussed in the following section.

## INVERTER DESIGN AND TESTS

Special inverter requirements, in addition to the challenge of operating connected to the utility line, include operation at 90% efficiency at full load, with no load losses of not more than 2.5% of rated power, and stable control response to varying power level commands from the power system controller (PSC).

The transition from dc power to ac sine wave power is implemented by dual transistorized power bridges. The bridges are switched in accordance with a pulse pattern (stored in a PROM) which approximates a sine wave with only high order harmonic content. Power losses in the bridge are minimized by providing just enough base drive to the power stages to satisfy the collector current requirements. A low loss output filter removes the high frequency harmonics.

Unique to the inverter design is a digital controller which simultaneously regulates two control loops in the utility mode: output current amplitude and output current phase.

The inverter is designed for a nominal dc input voltage of 200 volts and the output is single phase 240 V ac. The rated power output is 10 kW. The inverter is capable of operating in a stand alone mode. However, this mode is not analyzed in this paper.

### Utility Tie In

Figure 4 depicts the functional arrangement of the inverter when it interfaces with the utility. The digital controller, which simulta-

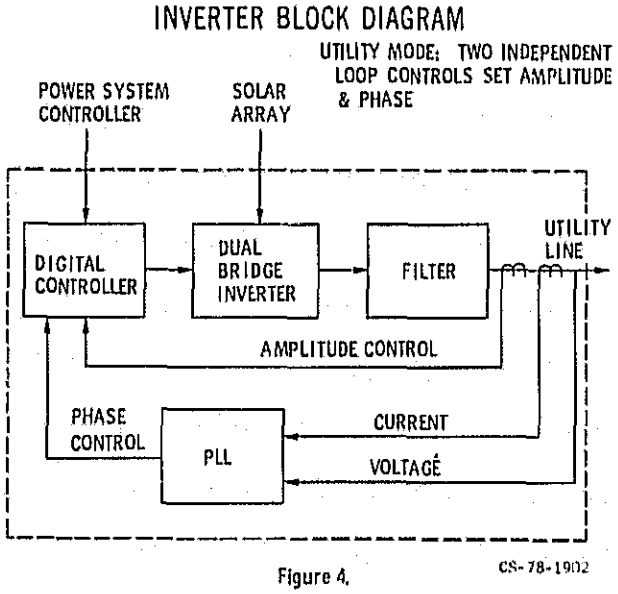



Figure 4.

neously controls the inverter amplitude and phase, establishes amplitude control by regulating the inverter output current as a function of the PSC command. The output current is held in phase with the utility voltage by means of a phase locked loop (PLL) (1). Output of the PLL, a bi-directional dc signal proportional to the phase error between the utility voltage and the inverter current, is applied to a voltage controlled oscillator (VCO) in the digital controller.

The VCO is the main clock in the digital controller, and after being divided through several stages of counters, establishes the 60 Hz frequency of the inverter. The counter outputs are connected to a PROM, which is programmed for four pulse pattern outputs that, when combined in the output, form a simulated wave over 360 electrical degrees. The phase of the simulated wave is adjusted by the PLL to the position relative to the line voltage to assure that the output current is in phase with the line voltage.

When operated connected to the utility line, the inverter receives an amplitude control signal from the PSC, which sets the power level of the inverter. The control signal from the PSC is compared with the inverter output current. The difference becomes the control error signal to the amplitude control loop. Since the output current is held in phase with the line voltage (held constant by the utility), the injected current is directly proportional to the output power. Thus the inverter amplitude control loop in the utility mode is a direct control of the power being delivered to the utility.

## Harmonic Distortion

The pulse pattern applied to the dual bridge switches was selected to eliminate all significant harmonics less than the 19th (2). Mathematical analysis of the harmonic content in the output wave form indicates a distribution of harmonics as shown in Fig. 5. The frequencies shown are multiples of the fundamental 60 Hz present in the pulse pattern output for a typical 80% power level. The harmonic content varies somewhat with the amplitude, which establishes a "dwell at zero voltage" at several places in the pulse pattern.

In the utility mode of operation, the inverter harmonic currents are injected into the utility line which has essentially zero impedance to the injected current. The output transformer is coupled to the utility via a series inductor which limits the harmonic current injected.

For stand alone operation two parallel filter branches are connected which, with the series inductor make up a low pass filter with characteristics shown in Fig. 5. The first parallel branch is a capacitor; the second branch is a series tuned LC section with a damping resistor bypassing the inductor. The series resonance is set for the 23rd harmonic. The effective pass band of the combined output filter is cut off at the 12th harmonic.

## Efficiency

Low power loss and high efficiency are critical design requirements for inverters intended for photovoltaic applications. Inverter losses are

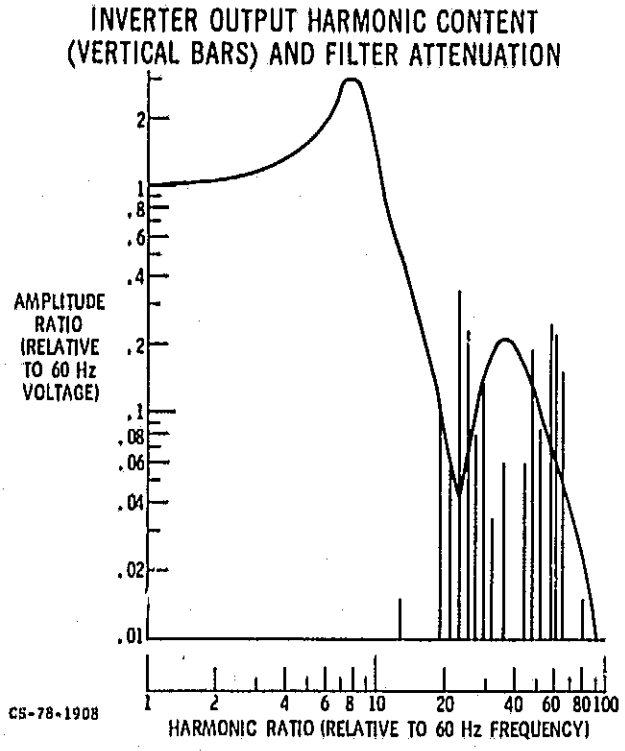



Figure 5.

primarily in the power bridges, the output transformers and the series filter inductor. The output transformers were designed for operation at a maximum flux density of 10 kg in grain oriented silicon steel to minimize no load losses. The reactive volt-amperes in the output filter have been set to less than 5% of the rated VA to minimize no load losses.

Transistors were selected as the power switches in the dual bridge inverter over SCR's because of the low loss requirement at no load. The power transistors are driven in a Darlington arrangement so that the base drive automatically adapts to the collector current demand; the power transistors are operated nonsaturated, that is, they remain in the Class A amplifier mode with the real collector voltage always in excess of the base voltage. To augment efficiency at high powers and guarantee reliable transistor operation, snubber circuits were included for both safe operating area turn-on and turn-off (3,4). Figure 6 shows plots of power loss and efficiency versus rated load (at unity power factor).

The inverter is fan cooled. To minimize the cooling fan losses, thermal switches turn the fans on when the power transistors reach a case temperature of 105° C. This occurs at a loading of approximately 40% to 60% of rated load subject to environmental conditions.

## Controlled Turn On

In addition to steady state design considerations, several transient phenomena must be accounted for when an inverter is connected to utility lines. The most important factor with photo-

INVERTER EFFICIENCY AND POWER LOSS

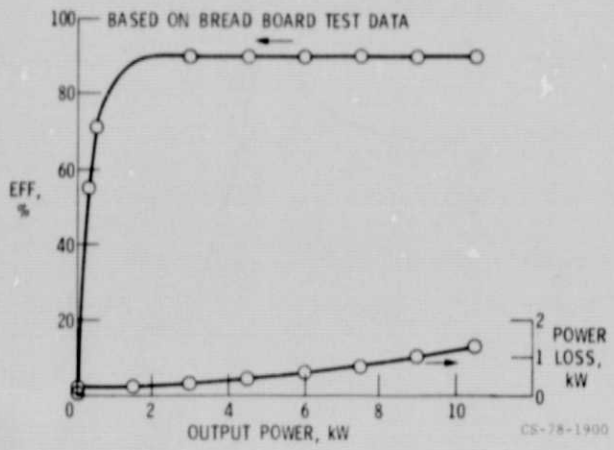



Figure 6.

INVERTER CONTROLLED TURN ON LOAD ASSUMPTION

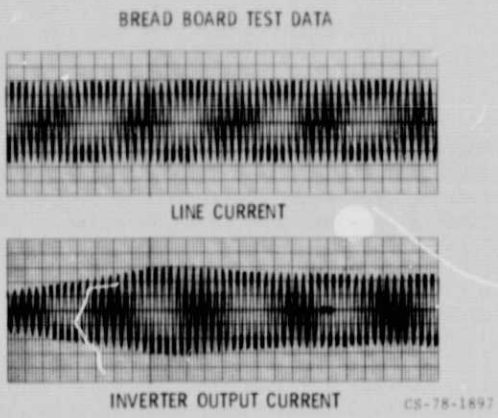



Figure 7.

voltaic cells, with their inherent high dc source resistance, is a "soft start" when utility tie-in takes place. Figure 7 is an oscillograph recording of the controlled assumption of load current by the inverter digital controller.

Connection to the utility line is made through an ac contactor/controller with independent safety features which guarantee system integrity. Connecting a solid state inverter of 10 kV A capacity must be done with "control and care." The "control" is incorporated into the soft start provisions. The "care" is engineered into the safety circuits which require eight conditions to be present for the inverter to remain tied to the utility.

Initial connection requirements are:

(1) The photovoltaic cell voltage exceeds $V_{min}$ = 160 V dc.

(2) The photovoltaic cell voltage is less than $V_{max}$ = 240 V dc.

(3) The sunrise-sunset signal from the PSC is GO.

(4) The PSC error detector is GO.

(5) The utility line voltage exceeds $V_{min}$ = 204 V ac.

(6) The utility voltage is less than $V_{max}$ = 264 V ac.

To remain connected, requirements are all the above plus:

(7) The inverter current remains in phase with the utility voltage.

(8) The inverter current does not exceed a safe maximum limit.

If any of the above conditions are not met, the inverter will automatically disconnect from the utility.

## SIMULATION TESTS AT LeRC

Hybrid analog-digital computer simulation tests were conducted at LeRC in order to confirm the basic stability of the Photovoltaic Power System (PPS) and to fix the values of critical control parameters in both the PSC and the inverter circuitry (5). System stability, system transient performance, and power conversion efficiencies were investigated. Highlights of the simulation tests are presented here.

### PPS System Model

For the subject simulation and analysis, the PPS is defined in block diagram form in Fig. 8. Dynamically, the important elements are (1) the solar array, (2) the power system controller, (3) the power inverter with its input and output filters, (4) the inverter phase controller, and (5) the reference utility line voltage. In this equivalent circuit, the pilot sensor array function ($E_{REF}$) is obtained from the solar array open circuit voltage model.

### Component Models

The solar array consists of several hundred solar cells interconnected in a series/parallel combination to achieve the desired power rating a

PHOTOVOLTAIC POWER SYSTEM INFORMATION FLOW DIAGRAM

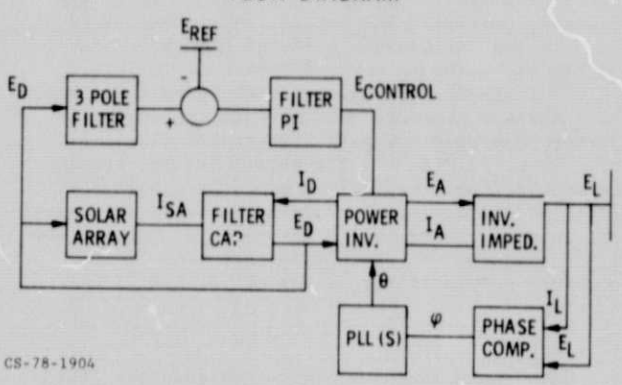



Figure 8.

and output voltage. The array characteristics can be obtained by simple scaling of the typical individual cell characteristic shown in Fig. 1. Each curve is normalized in terms of open circuit voltage and short circuit current to yield a single curve which can be varied by the temperature and insolation influence parameters. In the simulation tests the normalized solar array characteristics were simulated by a diode function generator.

The PSC model is shown in Fig. 9. The feedback voltage ($E_D$) is filtered by a 3 pole, 40 Hz butterworth filter to remove the 120 Hz ripple and compared to a reference voltage ($E_{REF} = 0.8\ E_D, f$). For a steady state operating point $E_D, f - E_{REF} = 0$. The error signal is filtered to remove the high frequency noise and the output drives a proportional-integral control to generate the inverter control voltage.

The inverter can be considered conceptually to be an ideal power conversion device, that is, losses are shown downstream of the dc to ac conversion. In this concept the dc power in equals the ac power out. In Fig. 10, the power inverter is shown as a four terminal device, together with the input filter, the output filter, and the utility interface. In this diagram $E_D$ is the solar array terminal voltage, $E_{CONTR}$ is from the PSC, $E_A$ the internally generated inverter voltage, $\theta$ is the internal phase control, and $E_L$ is the utility line voltage reference.

Relationships between the inverter voltage, the utility line voltage, and the filter impedance is shown in Fig. 11. From a controls view, the major parameters at any point in time are considered to be in an electrical steady state condition point in a control loop transient. In Fig. 11, the line voltage $E_{LM}$ is made the reference vector of an infinite bus (not effected by load perturbations), $E_{AM}$ is the internally generated inverter voltage, and $E_{XM}$ is the voltage drop across the filter reactor ($E_A \approx E_I$). The filter reactor is treated as an ideal reactance (i.e., no resistance).

The phasor diagram in 11(a) depicts a steady state relationship, wherein the injected line current is in phase with the utility voltage. The magnitude of the current is set by the angle $\theta$ (torque angle referred to in conventional alternator/utility bus analyses) and the value of the filter reactance X. The phasor diagram 11(b) shows a snapshot of relations during a transient control state resulting from an increase in line voltage. $I_{LM}$ is shown at an angle $\varphi$ with the utility voltage at a value required to satisfy the phasor diagram requirements.

Inverter control is accomplished by dual functions. Initially the E control begins to adjust the magnitude of the voltage vector $E_{AM}$ ($E_{LM}$) to obtain the desired current. The phase control continuously positions the vector by varying $\theta$ to bring the line current in phase with the line voltage. The controls stabilize at an operating point where the current requirement is met and that current is in phase with the line voltage.

## POWER SYSTEM CONTROLLER BLOCK DIAGRAM

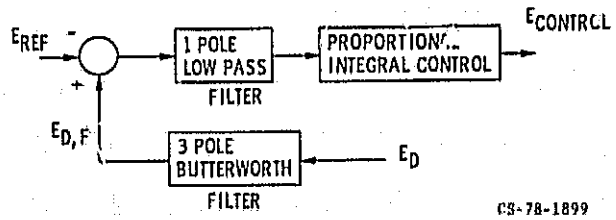



Figure 9.

## INVERTER MODEL

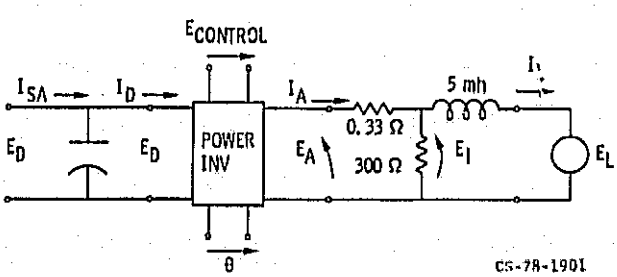
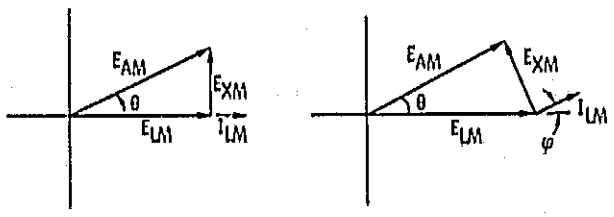



Figure 10.

## INVERTER/UTILITY INTERFACE VOLTAGE PHASOR RELATIONS




STEADY STATE CONDITION

TRANSIENT CONDITION

Figure 11.

### Linear Analysis

Initially, a linear analysis was conducted to investigate the basic stability of the system. Results of the Bode Analysis indicated marginal stability at high power levels and potential instability at low power levels, with open loop gains which appear probable. Further analysis of the impact of system nonlinearities was deemed desirable.

### Nonlinear Analysis

Several experiments were simulated on the hybrid analog computer to evaluate:

(1) System stability at different power levels
(2) Transient performance
(3) System efficiencies

Steady State Stability

To examine the system stability at different insolation levels and to simulate system operations, a worst case cloud cover transient experiment was conducted. System parameters were set at $E_{LM}$ = 340 V (peak), $E_{REF}$ = 0.8 $E_{OC}$, PSC gain of 5, and a PI setting of IV/V-SEC.

Insolation levels were decreased at a constant rate from the 100 to 6.5 mW/cm$^2$ in 5 seconds; held at 6.5 for 6 seconds, then increased at constant rate to 100 mW/cm$^2$. The locus of operating points obtained from tests incorporating initial simple nonlinear models are shown in Fig. 12.

Tests were subsequently conducted using the more complex inverter model, incorporating both the phase lock loop (PLL) and the current amplitude control circuitry.

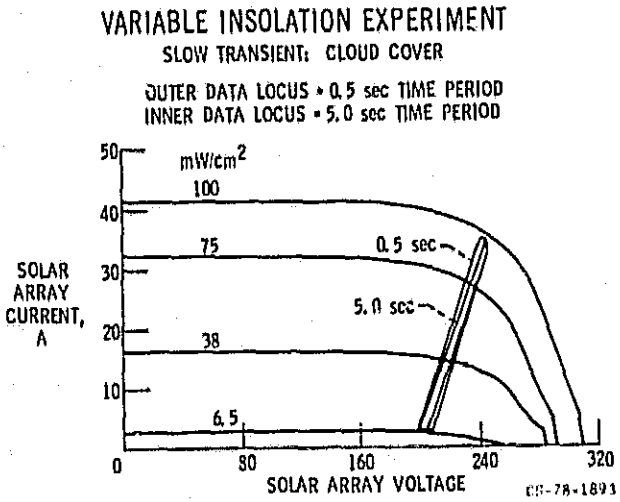



Figure 12.

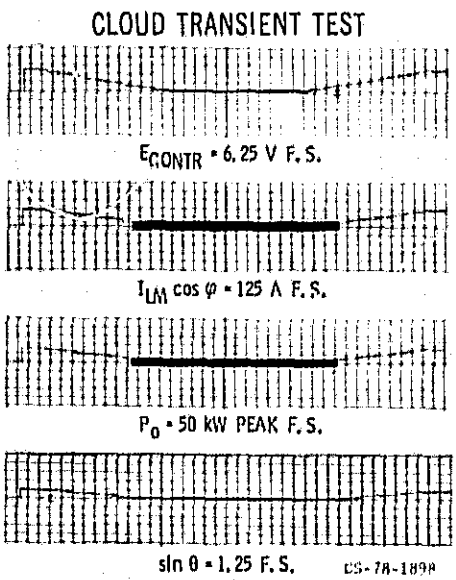



Figure 13.

Time records are shown for selected parameters in Fig. 13. Overall system operation is stable for almost the entire transient. A limit cycle is observed in the inverter phase control at the lower insolation levels (less than 20 mW/cm$^2$).

The onset of limit cycling is associated with the relative values of the two voltage phasors, $E_A$ and $E_L$. From Fig. 11(a), in the simulation model of the utility/impedance interface, $E_{LM}$ ($=E_{IM}$) must always be larger than $E_{LM}$ for a valid steady state $I_L$ calculation. From calculated values of $E_A$ and $E_L$ for the 20 mW/cm$^2$ insolation level, the difference between the two phasors is 0.72 volts. This is a difference of only 0.18%. Practically, the hardware used to implement the nonlinear simulation cannot resolve this difference.

Conceptually, this can be modeled as a dead-zone nonlinearity in the system. Therefore, ability to set injected power is impaired, a power imbalance is incurred, and localized limit cycling results. Similar results may be encountered in actual system operations, although via a different route. In the actual system phase lock is maintained through resolution of the phase differences between the line current and the line voltage. When the line current approaches zero, the phase comparator output can respond to line noise rather than valid signals. It is anticipated that this condition may be encountered at power levels of about 5%.

Transient Response Stability

The transient response of the PPS to changes in the commanded reference point and to changes in the utility line voltage were simulated. Response to reference point step changes define dynamic response times of the system. System response to utility line voltage fluctuations is particularly important since this is typically the most severe operating constraint on utility mode operation subsequent to the initial assumption of power when connected to the utility.

Tests were conducted to determine system response to changes of ±10% in $E_{REF}$ for insolation levels of 100, 33, 14, and 6.5 mW/cm$^2$. Selected data from the 100 mW/cm$^2$ test are shown in Fig. 14. As the result of a +10% change in $E_{REF}$, $E_{CONTR}$ shown a negative step followed by damped oscillations at approximately a 2 Hz rate. The inverter input current $I_D$ shows a decreased value. The solar array output voltage $E_D$ rises to meet the new target value commanded by $E_{REF}$.

Selected data from the 6.5 mW/cm$^2$ test are shown in Fig. 15. As a result of a +10% change in $E_{REF}$, $E_{CONTR}$ again takes a negative step, followed by damped oscillations. $I_D$ is already at a very low value, and is in a condition of limit cycling due to aforementioned model limitations. Even so, $I_D$ does decrease, bringing about an increase in $E_D$ as commanded by the $E_{REF}$.

Tests were conducted to determine system response to changes of utility line voltages of ±10%. These were done as in the above tests for the insolations ranges of 100 mW/cm$^2$ to 6.5 mW/cm$^2$.

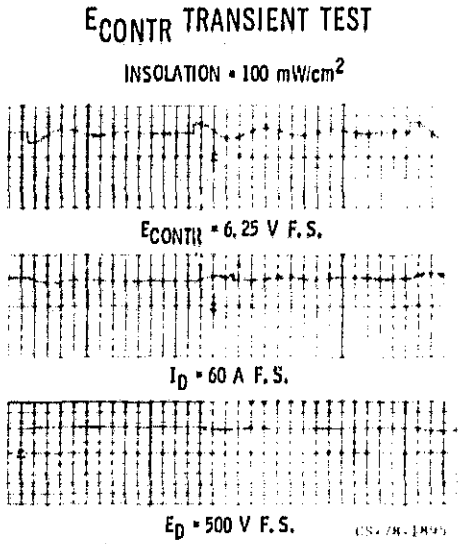



Figure 14.

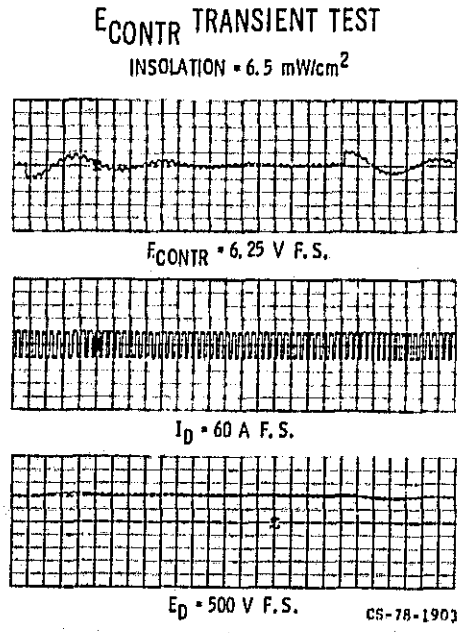



Figure 15.

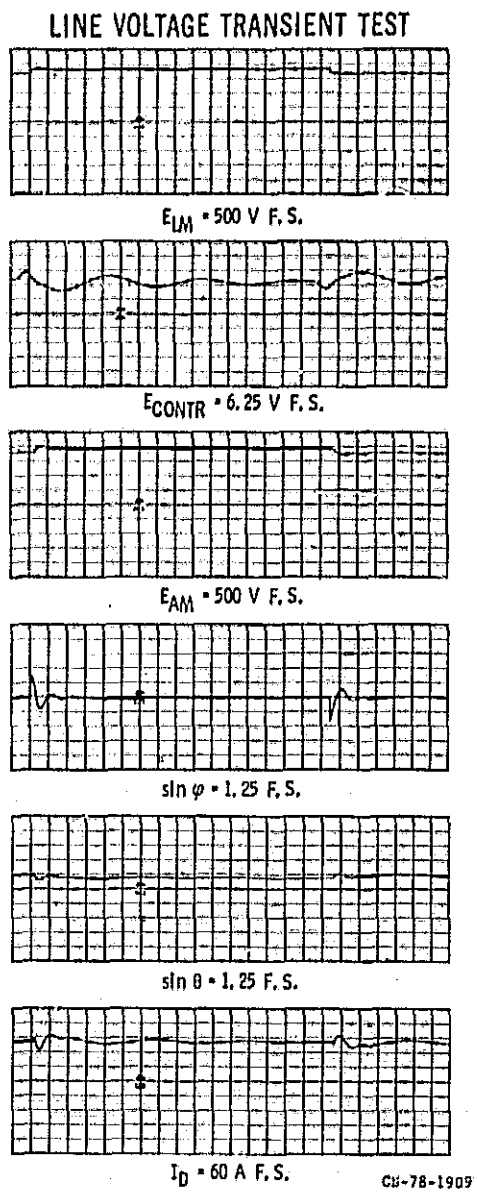



Figure 16.

Selected data from the 100 mW/cm$^2$ tests are shown in Fig. 16.

When the line voltage is stepped up 10%, the line current immediately jumps to a lead angle to fulfill the phasor requirements shown in Fig. 11(b) The change in angle $\varphi$ is reflected in the sin $\varphi$ perturbation shown in Fig. 16(d). The inverter phase control immediately tries to bring the current back to zero reactive by rotating the vector $E_A$ back toward $E_L$, as indicated by the change in sin $\theta$ function. $I_D$ show a momentary rise (supplied by the input capacitor) and then decreases in response to the smaller load current set by the decreased torque angle $\theta$. Ultimately, the inverter internal voltage $E_A$ increases to restore steady state conditions with the injected line current at zero phase angle.

Similar tests were conducted at the lower insolation levels with stable results. However as before, at the low insolation levels the system exhibited limit cycles due to the model limitations.

## SUMMARY

The simulation tests confirmed the basic system stability. Good immunity to transients in both the utility line and the target reference voltages was demonstrated. However, oscillations in the injected utility line power and solar array voltage were encountered at low insolation levels. In the simulation the limit cycling was attributed to model limitations. However, similar cycling may be encountered in the actual system as the result of similar hardware limitations.

Results show that the inverter/controller design will enable the PPS to be operated at the maximum power capability of the solar array. The gain parameters in both the inverter and the PSC were determined and these values specified in the hardware being manufactured.

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15. Supplementary Notes
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16. Abstract

Conversion of solar array dc power to ac power stimulated the specification, design, and simulation testing of an inverter/controller subsystem tailored to the photovoltaic power source characteristics. This paper discusses the optimization of the inverter/controller design as part of an overall Photovoltaic Power System (PPS) designed for maximum energy extraction from the solar array. The special design requirements for the inverter/controller include: (1) a power system controller (PSC) to control continuously the solar array operating point at the maximum power level based on variable solar insolation and cell temperatures; and (2) an inverter designed for high efficiency at rated load and low losses at light loadings to conserve energy. It must be capable of operating connected to the utility line at a level set by an external controller (PSC). This paper is presented in three sections: (1) the overall PPS and PSC design (Utility Mode); (2) the inverter design and test results; and (3) a PPS analysis and simulation testing, conducted at LeRC to verify the design control concepts and fix design parameters.

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