CUSTOM LARGE SCALE INTEGRATED CIRCUITS FOR SPACEBORNE SAR PROCESSORS *

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SUMMARY

Future space missions are expected to require real-time on-board SAR processors. Large scale integrated (LSI) circuit devices will play an important role in enabling development of SAR processors which meet the severe weight and power constraints associated with on-board processing applications. This paper discusses the application of modern LSI technology to the development of a time-domain azimuth correlator for SAR processing.

General design requirements for azimuth correlators for missions such as SEASAT-A, Venus Orbital Imaging Radar (VOIR), and Shuttle Imaging Radar (SIR) are summarized. Several azimuth correlator architectures that are suitable for implementation using custom LSI devices are described. Technical factors pertaining to selection of appropriate LSI technologies are discussed, and the maturity of alternative technologies for spacecraft application are discussed in the context of the expected space mission launch dates. Finally, the paper describes the preliminary design of a custom LSI time-domain azimuth correlator device (ACD) being developed for use in future SAR processors. Over 1000 of these ACD's are planned to be used in a laboratory model SAR processor to be built in 1979.

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1.0 INTRODUCTION

The first space mission to use a SAR instrument is SEASAT-A which will be launched early in 1978. In this earth orbiting spacecraft the raw SAR instrument data will be sent to the ground where it will be processed into images. The primary goals of the SEASAT-A mission are adequately satisfied by using earth based processing. Non-real-time SAR processing is planned for this mission primarily because the cost of development of a real-time SAR processor would not fit within the SEASAT budget. Since SEASAT-A is primarily a research tool in a feasability study and it was not intended to be used for operational radar observations, it was deemed acceptable to require several hours to process data which are collected in a few minutes.

In the future, SAR data from orbiting satellites must be processed to images in real time in order to avoid an ever increasing back-log of unprocessed data. Even ground based real-time processing is not without formidable problems. The spacecraft unprocessed SAR data rates for some identified SAR instrumented missions range from 5×10^6 bits per second to 120×10^6 bits per second with higher rates likely for more advanced SAR instruments. There are substantial functional and economic benefits associated with real-time on-board processing of SAR data. It is therefore likely that on-board spacecraft SAR processing will play an increasing role in future SAR spacemissions.

On-board SAR processing has the advantage that the down link data rate is reduced by at least the number of looks. In addition, since the processed SAR data is in the form of images it is possible to do on-board image feature extraction similar to the type planned for LANDSAT images and further reduce the down link data rate and volume. However, these benefits are not easily attained. A on-board SAR processor must be designed within the severe weight, volume and power restrictions of a spacecraft. A way (perhaps the only way) to implement high-performance on-board SAR processors is through the use of custom large scale integrated (LSI) circuits for major portions of the SAR processing circuitry.

The portions of the SAR processor that will most benefit from custom LSI are the range correlator and the azimuth correlator. Custom LSI devices have been used to perform the range correlation for several years in aircraft SAR

processors. Range correlation devices have been constructed using analog charge coupled devices (CCD) and surface wave devices (SWD). Both of these devices depend upon the stable range chirp parameters to permit the use of fixed tap weights in the correlator devices. If the correlation coefficients must be adjustable, as is required in the azimuth correlator, conventional CCD and SWD devices cannot be used. The remainder of this paper will briefly describe a few different azimuth correlator architectures that permit variable coefficients, and will discuss the detail specification of a custom LSI device for one of these architectures.

2.0 TYPICAL SPACEBORNE SAR INSTRUMENTS

A summary of some typical spaceborne SAR instrument characteristics is given in table 1. They represent a fairly broad range of resolutions and radar frequencies and provide a baseline for the range of azimuth correlator complexity. The radar center frequencies range from L-band to X-band. Swath width varies from 12.5 km to 100 km and resolution varies from 20 m to 200 m. The requirements specified for VOIR and SIR are preliminary and may change as their respective mission goals are defined more fully. The requirements for SEASAT-A, however, are well defined and are discussed in considerable detail in a companion paper [1]. The experimental electronic SAR processor described in [1] is being designed to produce 20 km swath 25 m resolution, four look, SAR imagry.

3.0 AZIMUTH CORRELATOR ARCHITECTURE AND LSI TECHNOLOGY

Since the laboratory SAR processor is required to perform real-time processing of SEASAT-A data, the selection of an azimuth correlator architecture was heavily influenced by SEASAT-A requirements. "Simple" frequency domain azimuth processors have been devised which use an FFT to obtain the intensity of image elements along isodoppler lines on the surface of the earth. However, these "simple" frequency domain processors exhibit substantial geometric distortion requiring complex processing to solve registration problems associated with formation of multilook images. The use of custom LSI circuits to implement FFT function have been described in other papers [2] [3] and will not be discussed any further in this paper. The primary thrust of the remainder of this paper will be to discuss a few

candidate time-domain azimuth correlator architectures that are implementable in custom LSI circuits reasonable chip size.

TABLE 1

SAR PROCESSOR FUNCTIONAL REQUIREMENTS

	SEASAT-A	SIR-B		VOIR
	L-BAND	C-BAND	X-BAND	L-BAND
GROUND RANGE RESOLUTION (M)	25	70,25,20	70,25,20	200, 25
AZIMUTH RESOLUTION (M)	25	70,25,20	70,25,20	200, 25
NUMBER OF LOOKS	4	15, 5, 5	15, 5, 5	30, 4
SWATH WIDTH (KM)	100	50,25,55	50,25,55	100, 12.5
PIXELS PRODUCED ACROSS SWATH	5760	1039,1604 3755	1039,1604 3755	770, 1115
BEAM CENTER SLANT RANGE (KM)	870	230,335 480	230,335 480	550
RANGE TIME-BANDWIDTH PRODUCT	646	339	10	42.3, 338
AZIMUTH SAMPLES PER LOOK	1020	28, 122 176	16,64,92	60, 475
RANGE WALK ACROSS BEAM (BINS)	128	10	10	2, 10
STALO FREQUENCY (MHz)	91.06	91.06	91.06	91.06
RADAR CENTER FREQUENCY (GHz)	1.275	4.75	9.1	1.275
RADAR PRF (MAX.) (Hz)	1645	2218	2218	1304
PULSE DURATION (μSEC)	33.8	33.9	1	33.8
PULSE CODING	CHIRP	PN	PN	PN
BANDWIDTH	10	10	10	10, 1.5(3)
SAMPLING FREQUENCY (I,Q)(MHz)	22.76	11.38	11.38	11.38, 1.42
ANTENNA DIMENSION (AZ.) (M)	10.5	8	8	12
ANTENNA LOOK ANGLE (DEG)	20	15,49,64	15,49,64	49
NOMINAL RADAR ALTITUDE	795	225	225	375
NOMINAL RADAR SPEED (M/SEC)	7450	7700	7700	7150

3.1 TWO AZIMUTH CORRELATOR ARCHITECTURES

In selecting a suitable time-domain azimuth correlator architecture implementable in custom LSI, one of the first characteristics to look for is a high degree of regularity in the arithmetic and memory hardware requirements. One of the first architectures considered was a pipeline processor shown in figure 1. It has the property that both the data and the partial sums, leading to image pixels, flow through the processor in nice regular ("laminar") manner. It also is nicely modular in which each LSI device would contain the range line memory, coefficient storage, multiplier, adder, and etc., as shown enclosed in the dashed lines. It has the advantage that it uses a minimum number of bits of on-chip storage which is a significant factor in minimizing chip size. Small chip size has a very close relationship to the chip yield in fabrication. Chip yield reduces dramatically as chip size increases. A disadvantage of this architecture is that it is not possible to include anything more than the simplest range interpolation without greatly increasing the complexity and size of the chip. Since it was considered important to have the option of using multipoint range interpolation for the SEASAT-A laboratory processor, this correlator architecture was not adopted for the experimental processor.

Another azimuth correlator architecture was considered that permitted parallel image line processing for all looks. Figure 2 is a block diagram of this azimuth correlator architecture. It is modular, as indicated by the dashed lines, and allows range interpolation to be done centrally, eliminating the necessity for interpolation logic on the chip. A disadvantage is that there is a larger amount of memory required on the chip because the complex image line is accumulated on the chip rather than accumulated over the array of chips as in figure 1. However, since multipoint range interpolation was considered to be an important option for the SEASAT-A laboratory processor, this second azimuth correlator architecture was preferred. A deciding factor in confirming this architecture choice is the availability of a suitable LSI technology which can implement the additional memory required without a significant power penalty.

3.2 SELECTION OF APPROPRIATE LSI TECHNOLOGIES

In order to implement an LSI device of the complexity required for one of the above azimuth correlators, one needs to consider only technologies that exhibit minimum area per gate properties. Also, for spacecraft application, the amount power required to operate the chips must be minimum. Fortunately minimum power and minimum area per gate are compatible requirements. Table 2 is a comparative summary of the area, power, and speed of several common LSI technologies. These are: Complementary-Metal-Oxide-Semiconductor-Silicon-on-Sapphire (CMOS-SOS), Integrated Injection Logic (I^2L), N-channel Metal-Oxide-Semiconductor (NMOS), and Digital Charge Coupled Device (DCCD). They are representative of the most common high speed, low power and small area devices available. The areas for a logic gate and a data storage element (shift register) are useful in assessing the amount of circuitry that can be placed upon a chip of moderate size ($3X10^7$ square micrometers). Speed-power product is a figure of merit used to indicate the amount of energy required to change the state of a typical logic element. As can be seen under the shift register power per bit column, the speed power product is not an absolute indicator of the relative power required to operate these LSI circuits. Topological factors can override the apparent speed-power product ratios as can be seen by comparing CMOS-SOS and NMOS. The speed-power product ratio of NMOS to CMOS-SOS is 2 but the ratio of power per bit for the shift register is 3.

All of the values in Table 2 assume that the minimum on-chip conductor widths are 5 micrometers, which is currently a standard photolithographic capability within the integrated circuit industry. In the next five to ten years, the minimum line widths can be expected to reduce to one-tenth of today's limits which will allow proportional scaling of the figures in Table 2.

Selection of an LSI technology for a spacecraft application requires careful assessment of the proposed application. In applications requiring high chip complexity, it is clear from Table 2 that DCCD has a significant advantage. DCCD, however, has less radiation resistance that either I^2L or CMOS-SOS. If the spacecraft must spend a large amount of time in trapped radiation fields, it would be necessary to shield the DCCD processor circuits. Also,

DCCD technology can only be used in pipe-line processor architectures [4]. A high spacecraft radiation environment would probably require the higher radiation tolerance of either CMOS-SOS or I^2L. The larger logic element dimensions of these technologies may require a multiple custom LSI implementation in azimuth correlators of high complexity. NMOS has about the same radiation restistance as DCCD.

It is not practical to discuss all possible tradeoffs involved in selecting a custom LSI technology in this paper. The above discussion is a brief outline of some of the factors that must be considered in technology selection. The next section of this paper will describe an example azimuth correlator architecture and will discuss an LSI technology selection. This will illustrate some of the practical problems encountered in using custom LSI for SAR processors.

TABLE 2

HIGH DENSITY LSI TECHNOLOGIES

DIGITAL (5 μm GEOMETRY)

	LOGIC GATE		SHIFT REGISTER	
	AREA	SPEED-POWER	POWER/BIT 1 MHZ	AREA/BIT
CMOS SOS	12903 μm^2	5 pJ	100 μW	49387 μm^2
I^2L	6452 μm^2	2 pJ	50 μW	19455 μm^2
NMOS	9677 μm^2	10 pJ	300 μW	41935 μm^2
DCCD	645 μm^2	0.2 pJ	0.3 μW	129 μm^2

NOTE: A MODERATE SIZE LSI CHIP AREA IS: $3 \times 10^7 \mu m^2$

4.0 EXAMPLE AZIMUTH CORRELATOR LSI DEVICE

JPL is presently involved in the development of an experimental electronic SAR processor [1] which will use a custom LSI device to implement the azimuth correlator. This processor, called the Developmental Model SAR Processor (DMSP), will be used to demonstrate real-time, time domain processing of SAR data from the SEASAT-A spacecraft. Unprocessed data from the spacecraft will

be sent to the DMSP which will produce a 20 km swath image at 25 m resolution at the real-time rate. Data given in Table 1 are the baseline requirements for this processor. The azimuth correlator uses the architecture described in Figure 2 and is implemented with a set of identical custom LSI devices specified for use in this azimuth correlator. This LSI device is called the azimuth correlator device (ACD).

4.1 GENERAL REQUIREMENTS FOR THE ACD

The DMSP functional block diagram, Figure 3, shows the relationship of the azimuth correlator to the other elements of the DMSP. The DMSP requires an array of 1020 ACD's to perform a 20 km swath azimuth correlation with 4 looks. The relationship of the ACD's to the complete SAR processor is shown in Figure 4 and 5 which are, respectively, a block diagram of the complete azimuth correlator and a block diagram of a single-look azimuth correlator module. The ACD receives data from the range correlator via the ACD input sample bus as a contiguous sequence of "range-lines". Each range-line comprises 5120 complex data samples accompanied by several sync signals. The basic operation performed by the ACD during a range-line processing cycle is to select the appropriate set of 1152 complex data samples from each range-line, multiply each data sample by the appropriate complex azimuth reference function (ARF) coefficients, and to add this product to the appropriate cell in the accumulator register. (New sets of reference function coefficients are needed for each new set of range-line date samples input to the ACD during an image-line processing cycle.) In the DMSP, an image-line processing cycle will involve 1020 range-lines. The final value of the complex image-line sample stored in the j^{th} accumulator cell takes on the value

$$P_j = \sum_{i=0}^{1019} C_{im} S_{ij} \qquad \text{for } j = 0,1151 \qquad (1)$$

where

C_{im} = complex reference function coefficient (where $m = [j/16]$, the integer portion of $j/16$) for the j^{th} data sample from the i^{th} range-line in the image-line processing cycle.

S_{ij} = the j^{th} complex data sample from the i^{th} range-line in the image-line processing cycle.

At the end of an image-line processing cycle, the output of the complex adder is switched to the output driver and the 1152 complex image-line samples are read out. The image-line memory is filled with zero levels during the image-line read out process. An ACD functional block diagram is shown in Figure 6. The functional characteristics of each element of the ACD is described in the following subsections.

4.1.1 Data sample format. The ACD input sample bus will supply data in word-serial (8-bits-per-word) fashion at word rates in the range from 400 kHz to 14.0 MHz. These data samples will be organized into sets of 5120 samples corresponding to individual SAR range-lines, and these range-line sample sets are subdivided into contiguous subsets of four interpolated samples each. Each data sample is a complex quantity. The first four bits of each sample report the sign and magnitude of the real part of the input sample, and the last four bits report the sign and magnitude of the imaginary part.

4.1.2 Coefficient formats. The following set of coefficients is provided to process the data samples corresponding to one range-line:

Coefficient Type	No. Coefficient Per Set	No. Bits Per Coefficient
RMC - Coarse	1	10
RMC - Fine	72	2
ARF	72	8

The first three bits of the Range Migration Compensation (RMC)-coarse coefficients have no effect on the processing. For convenience, the RMC-fine coefficient is appended to the end of the ARF coefficient to form a ten-bit composite coefficient. A coefficient bus sync is provided which controls and synchronizes the transfer of coefficients from ACD-to-ACD. (See Figure 5).

4.1.3 Coefficient buffers. Two levels of on-chip coefficient buffering are provided within the ACD. The first level provides for a set of 288 composite coefficients plus four RMC-coarse coefficients sufficient to process a set of four range-lines. The second level of buffering provides an eight word first-in-first-out (FIFO) buffer for the composite coefficients and a single word buffer register for the RMC-coarse coefficients. The organization of these buffers is described in Figure 6. The input coefficient mx switch routes the coefficient bit stream to the appropriate storage register. The internal mx switches enable the buffers to be operated in either a full-capacity mode or a one-quarter capacity mode which is useful in some applications. The output coefficient mx switch causes the normal coefficient bit stream to be re-formed from the output of the first level buffers so these coefficients can be passed on to another ACD in an azimuth correlator module (see Figure 5). The passage of coefficients from ACD-to-ACD occurs under the control of timing signals common to all of the ACDs in the azimuth correlator. The second level of buffering holds coefficients to be used in delayed range-line processing. This delay in processing is due to the action of the RMC-coarse coefficient which causes up to 127 sample subset periods of delay (realtive to coefficient transfer timing) is range line processing within an ACD. Each RMC-coarse coefficient is used once at the start of the corresponding range-line processing cycle. Each composite coefficient will be used with 16 consecutive range-line data sample subsets.

4.1.4 Input control. The input control (see Figure 6) selects an appropriate group of 1152 data samples from each range-line sample set. The applicable RMC-coarse coefficient determines how many of the input sample subsets (four samples each) of the range-line sample sets shall be passed-over before beginning selection of the data samples to be processed. The number of subsets passed-over can be any value from zero to 127. The four samples of each subsequent subset shall be stored in a sample buffer memory. The value of the appropriate RMC-fine coefficient will determine which on of the four samples to select for input to the complex multiplier element. (An RMC-fine coefficient value of zero shall cause the selection of the first sample of the subset, etc.)

4.1.5 Complex multiplier. The complex multiplier performs the following computation:

$$P = X \cdot Y; \qquad (2)$$

where

$$X = a + ib \text{ and } Y = c + id$$

This product (P) can also be expressed as $P = (ac - bd) + i(ad + bc)$. The quantities a and b are, respectively, the real and imaginary parts of the ARF coefficients. Quantities c and d are respectively the real and imaginary parts of the ACD input data samples. The real and imaginary parts of P each have a dynamic range of 8 bits.

4.1.6 Image line accumulator. The image-line accumulator comprises the functional equivalent of a complex adder and a recirculating image-line memory (Figure 6). The complex adder accepts the output of the complex multiplier (8 bit real component and 8 bit imaginary component) and the corresponding accumulator sample (16 bits I and 16 bits Q). The sum is passed through a multiplexer which will either route the complex sum to the image-line memory or to output driver circuits. This multiplexer, when in the output mode, shall enter zero levels into the image-line memory. The recirculating image-line memory is a shift register with a total capacity of 1152 complex image-line samples.

4.1.7 Control and timing. The control and timing circuitry provided on the ACD, accepts control and timing signals from the control processor and provides all of the necessary control and timing to all of the rest of the circuitry on the chip. Some of the functions to be provided by the control and timing circuitry are:

a. Clock signals to all elements of the ACD
b. Controls data input and sample selection
c. Controls coefficient buffer capacity and coefficient routing to and from internel coefficient buffers
d. Controls output of image-line pixels.
e. Controls selection of the 11 most significant or 11 least significant portion of the complex image-line sample magnitude at the

accumulator output.

4.2 ACD LSI TECHNOLOGY SELECTION

Taking an inventory of the circuitry required for the ACD, we observe the following:

a) There is a memory requirement of the order of 40,000 bits. Fortunately all of it is sequential (shift register) memory.

b) A 4 bit x 4 bit complex multiplier is required, which is comprised of four multipliers and two adders.

c) A complex adder is required which consists of two 16 bit adders.

d) Some random logic circuits for on-chip control and timing.

Assuming the chip size is to be kept within the 6mm x 6mm size category and that the total operating power for the chip must be kept under 0.5 watt, the LSI technology choice must be DCCD. The other three technologies would only be viable if the conductor widths were reduced to about 1.7 microns. Fortunately the radiation environment for a SEASAT-A type spacecraft is in the order of 10^5 rad (Si) per year, which is within the radiation tolerance range of DCCD with some shielding.

5. CONCLUSIONS

It has been concluded from the above that a custom LSI device is practical for a system as complex as the DMSP. Certainly SAR processing systems less complex than the DMSP could also benefit from LSI technology [5]. In the case of SEASAT-A type spacecraft, custom LSI is an enabling technology for spaceborn SAR processors.

REFERENCES

1. Wu, C., Electronic SAR Processors For Space Missions, Proceedings of The Synthetic Aperture Radar Technology Conference, New Mexico State University, New Mexico, 1978.

2. Atkinson, L. W. and Lumsford, J. A., A CMOS/SOS Pipeline FFT Processor - Construction, Performance and Application, NAECON Convention Record, 1977.

3. Wu, C., A-Digital Approach To Produce Imagry From SAR Data, AIAA System Design Driven By Sensor Conference, October 1976.

4. Zimmermann, T. A., The Digital Approach To Charge Coupled Device Signal Processing, IEEE International Symposium on Systems and Circuits, 1975.

5. Arens, W. E., Real-Time SAR Image Processing Onboard a Venus Orbiting Spacecraft, Proceedings of The Synthetic Aperture Radar Technology Conference, New Mexico State University, New Mexico, 1978.

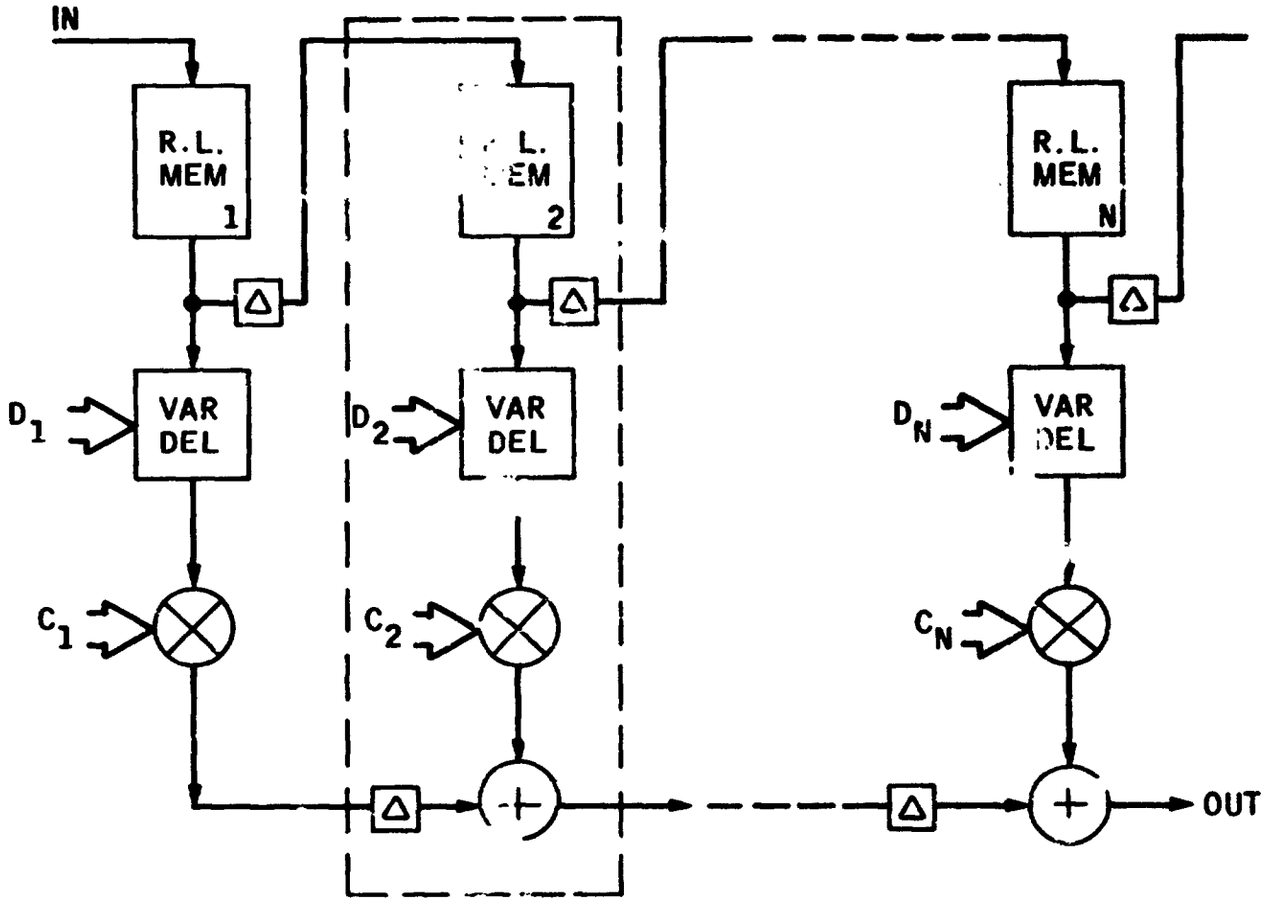

Figure 1. Time Domain Azimuth Correlator Architecture A

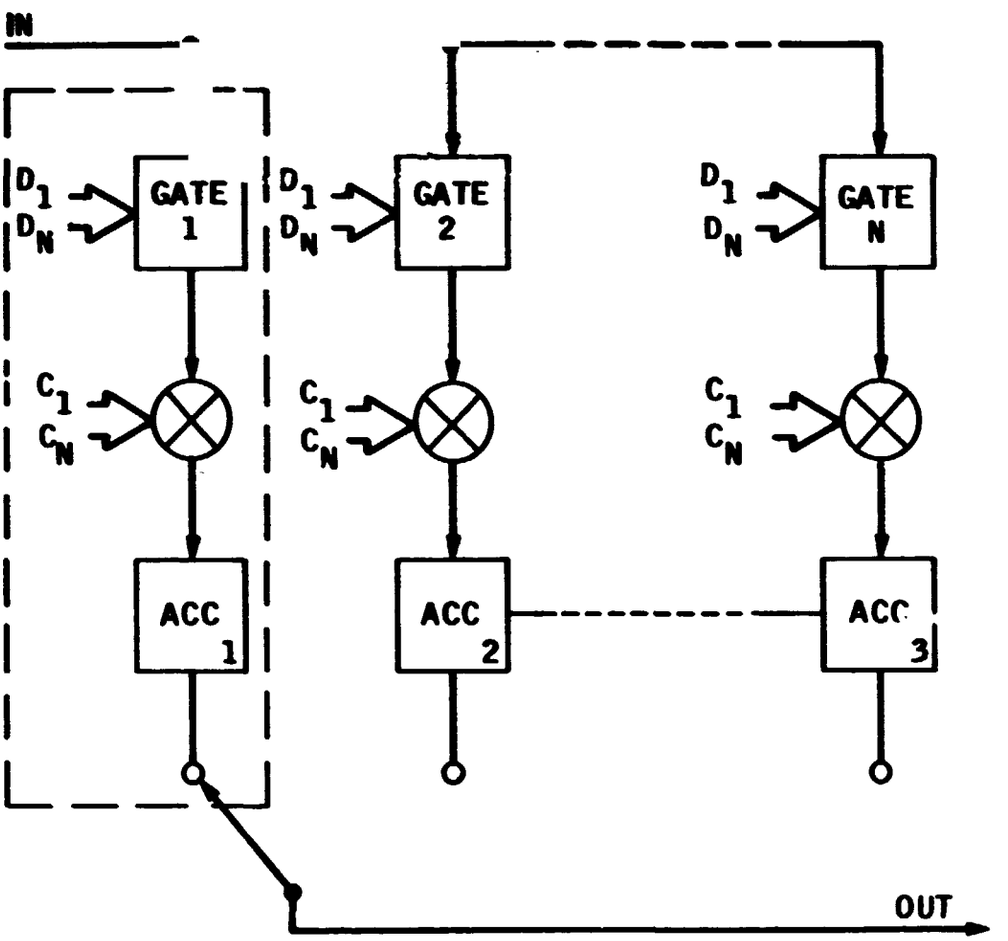

Figure 2. Time Domain Azimuth Correlator Architecture B

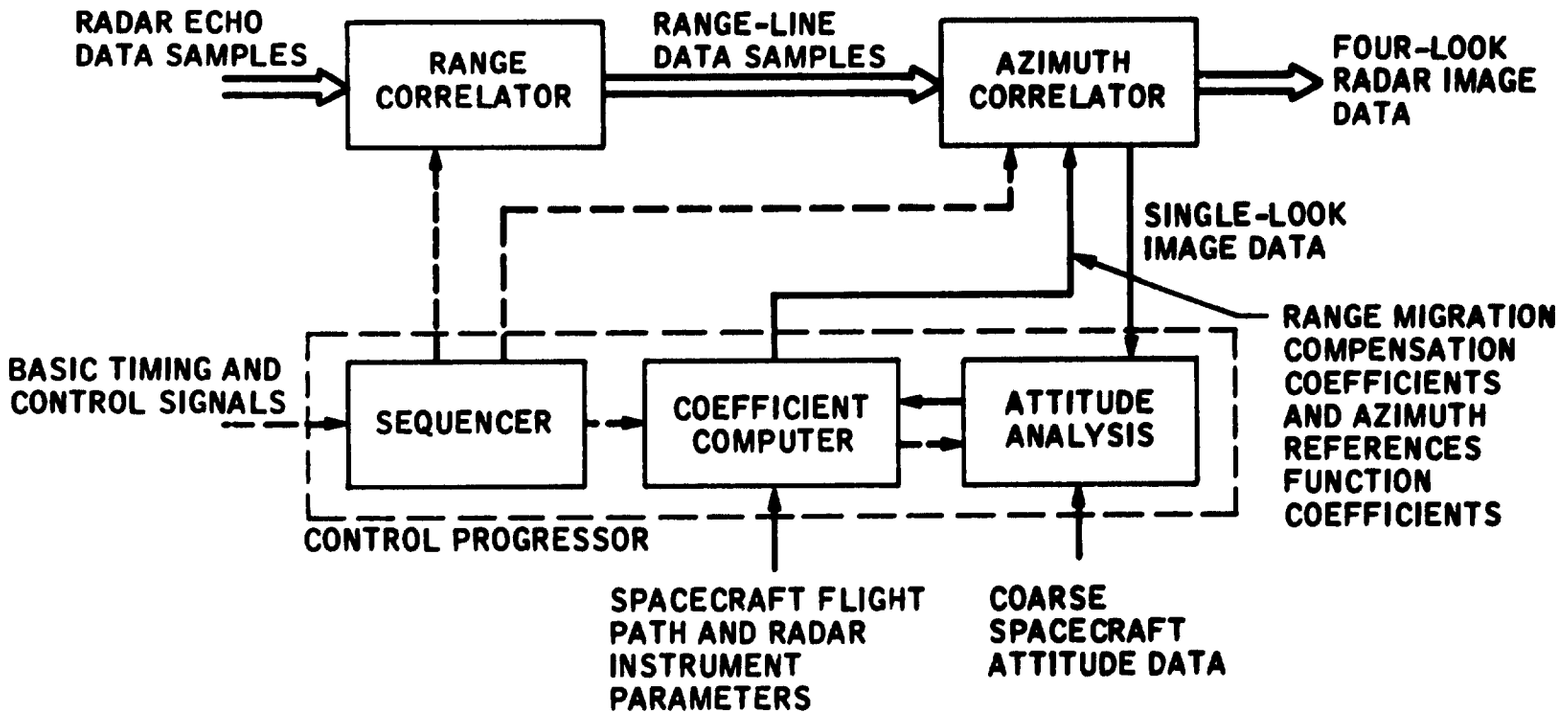

Figure 3. Developmental Model SAR Processor Block Diagram

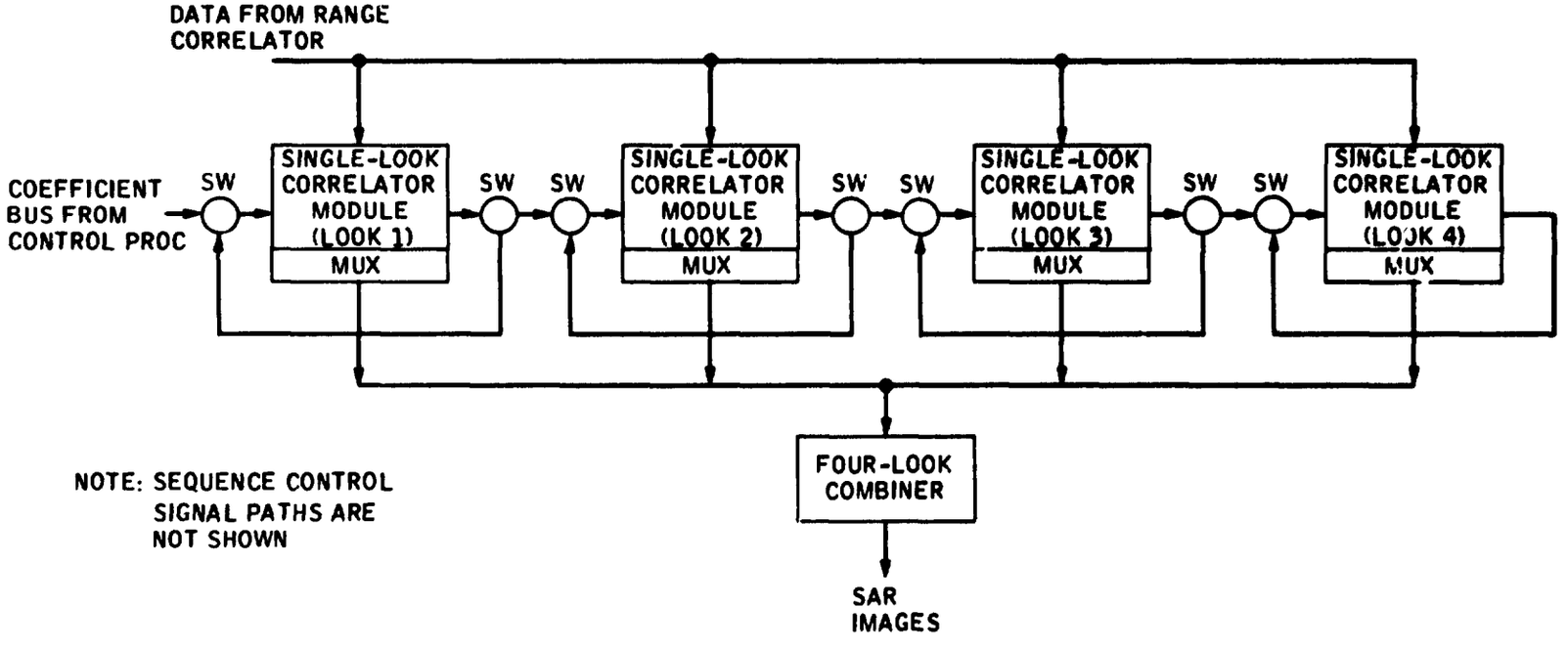

Figure 4. Azimuth Correlator Block Diagram

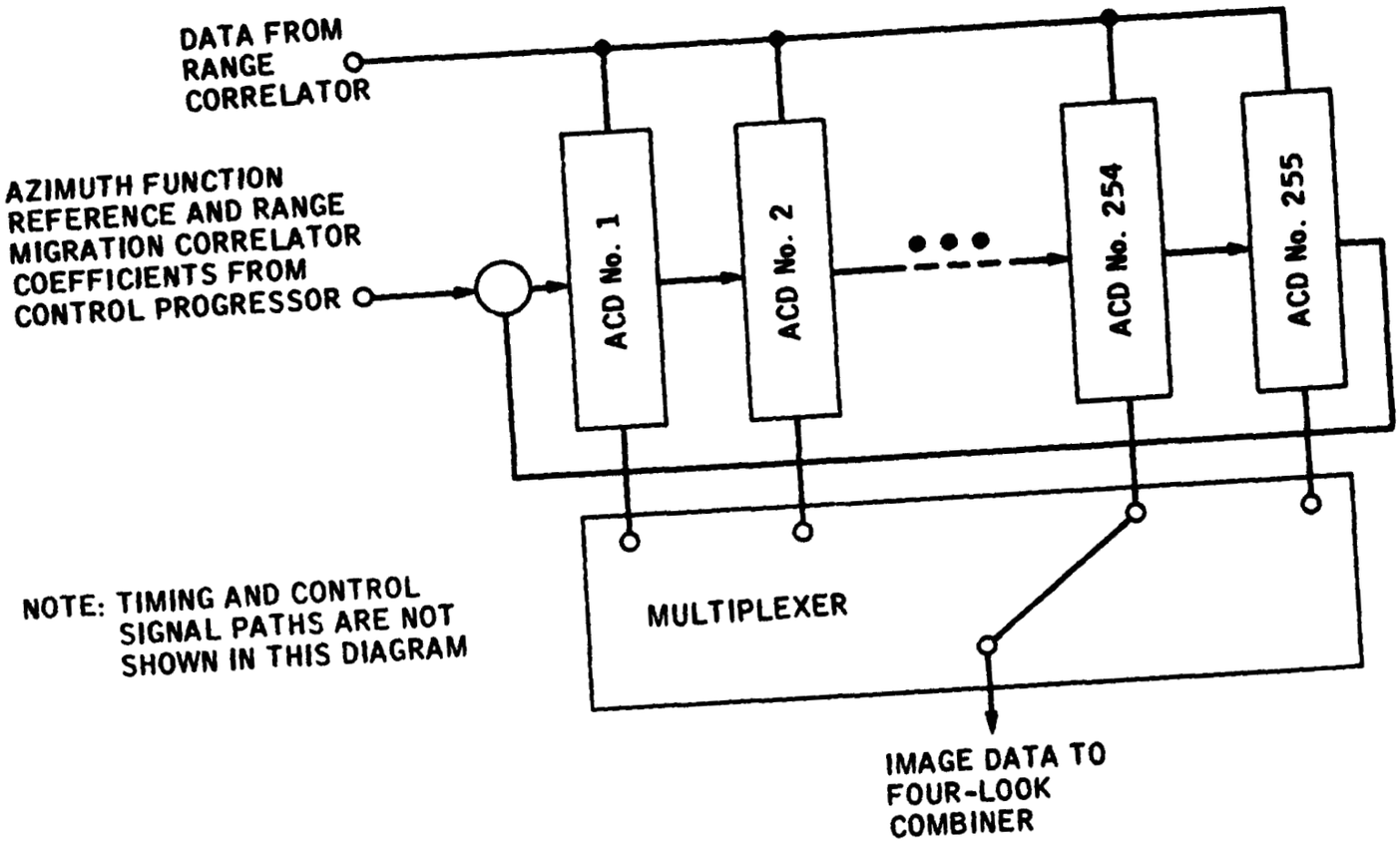

Figure 5. Block Diagram of One-Look Azimuth Correlator Module

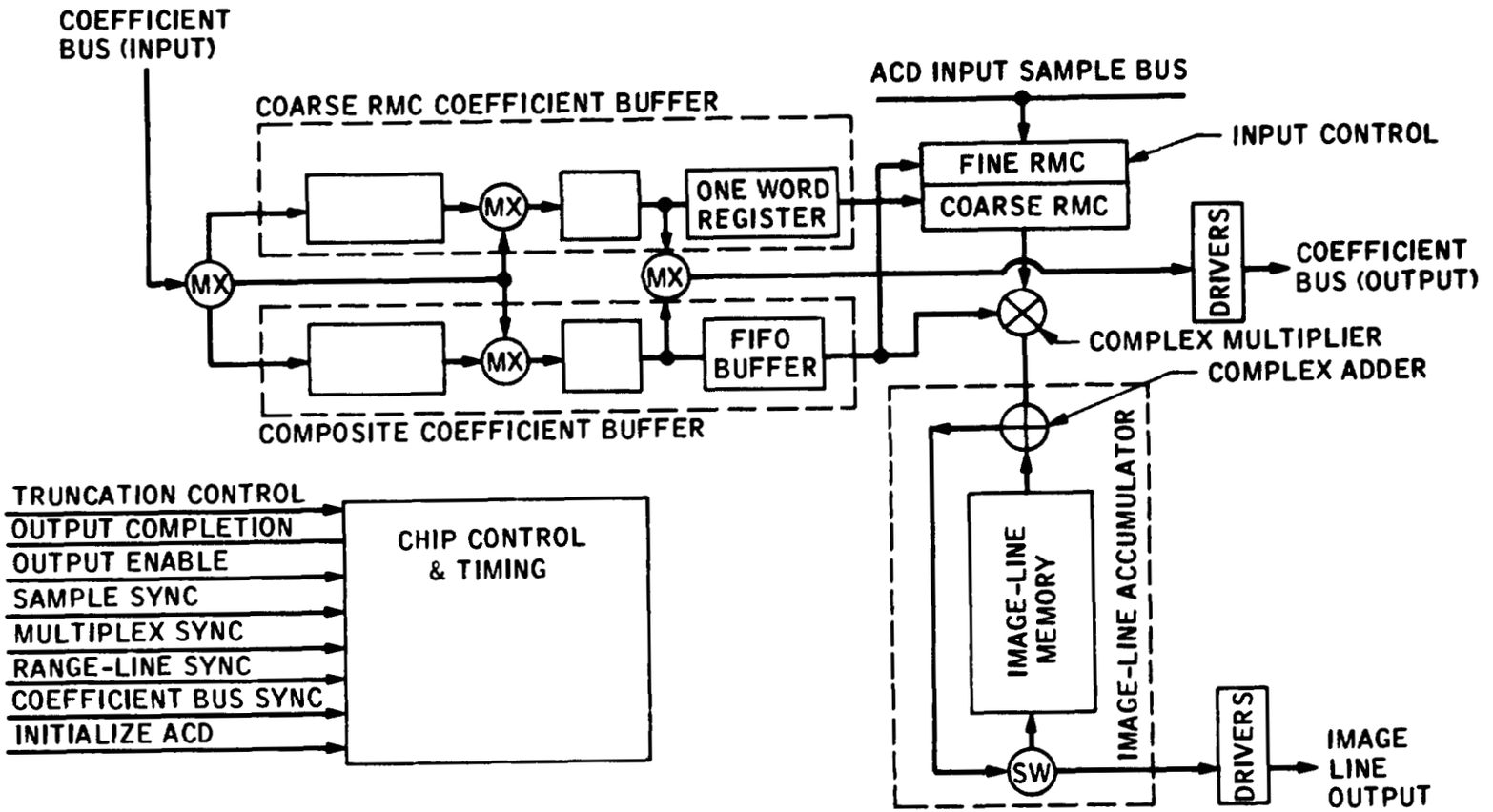

Figure 6. Azimuth Correlator Device Functional Block Diagram