REAL-TIME SAR IMAGE PROCESSING ONBOARD A VENUS ORBITING SPACECRAFT*

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SUMMARY

This paper describes the potential use of real-time synthetic aperture radar (SAR) processing to produce 200-meter resolution imagery onboard a 1983 Venus Orbiter Imaging Radar (VOIR) spacecraft. In the introductory section, the current NASA SAR processor development program and its relationship to the VOIR application is described. The VOIR SAR processing requirements are then defined in terms of a nominal baseline design evolving from a 1977 VOIR mission study by the Caltech Jet Propulsion Laboratory (JPL) [3]. A candidate on-board SAR processor architecture compatible with the VOIR requirements is next described. Finally, detailed implementation characteristics, based upon currently available integrated circuits, are estimated in terms of chip count, power, and weight.

1.0 INTRODUCTION

JPL is conducting a SAR processor advanced development program as part of an existing NASA Research and Technology Objective and Plan (RTOP). In turn, this RTOP is an approved and vital element of the NASA End-to-End Data System (NEEDS) program.

The current RTOP is funded to design and build a real-time stand-alone Developmental Model SAR Processor (DMSP) for operation in a laboratory environment. The DMSP will have the capability to process SEASAT-A SAR data at real-time rates to produce four-look, 25 meter resolution radar images covering a 20 Km swath. The objective is to demonstrate this capability by the end of FY'79.

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Since the NEEDS program is emphasizing the development of a future on-board processing capability, it is essential that the DMSP architecture be designed to be amenable to implementation for on-board SAR processing applications. A major feature of the DMSP task is the development of a custom LSI device to be used in the azimuth correlator. This device will employ current state-of the-art charge-coupled device (CCD) technology [1].

Following the DMSP development, it is planned to design and build a SAR processor for use in an SAR processing experiment on-board a future space shuttle flight. This experiment would demonstrate the ability of a space-borne processor to produce high-resolution multi-look radar imagery in real-time. The detail functional requirements imposed on this processor are intended to be representative of those anticipated on future earth observation missions [2].

A study of a complete SAR system for VOIR was performed during 1977. This paper reports on the results of that study pertaining to the feasibililty of developing an on-board SAR processor for VOIR. Although the SAR processor functional requirements assumed for that VOIR study were much less demanding than those imposed on the DMSP design, the VOIR processor design was adapted from the preliminary design developed from the DMSP. It is expected that many results from the DMSP development program will be directly applicable to the final design of an on-board SAR processor for VOIR.

2.0 NOMINAL VOIR SAR PROCESSING REQUIREMENTS

The VOIR mission study conducted during 1977 assumed a 1983 launch date. This study produced a baseline mission definition and design in support of the current FY'78 VOIR pre-project activity. The baseline scenario provides for 200-meter low resolution mapping of the entire planetary surface and 25-meter high resolution imagery of selected areas. An on-board real-time synthetic aperature radar (SAR) image processor was included in the proposed baseline design, for the low resolution mode, in order to achieve a SAR data rate reduction commensurate with the available telecommunications line capability [3].

Nominal radar system design values applicable to establishing the necessary SAR processing design parameters are tabulated in Table 1. Using the values of Table 1, the nominal processing design parameters of Table 2 have been derived using the equations of Table 3. As noted from Table 2, coherent

TABLE 1

· NOMINAL VOIR RADAR SYSTEM DESIGN VALUES

Design Parameter		Value
Transmitter Frequency	f	1275 MHz
Radar Wavelength	λ	0.235 m
Pulse Repetition Frequency	PRF	1225 Hz
Interpulse Period	IPP	816 μsec
Spacecraft Velocity	V	7.14 Km/sec
Altitude	H	375 Km
Look Angle	θ	46^{o}
Incidence Angle	θ_i	49^{o}
Range	R	559 Km
Swath Width	SW	100 Km
Antenna Width	W	2.0 m
Range Beamwidth	Ω_r	6.73^{o}
Range Pulsewidth	T_r	33.8 μsec
Range Bandwidth	Δf_r	1.25 MHz
Antenna Length	L	12.0 m
Azimuth Beamwidth	Ω_a	1.12^{o}
Time in Beam	T_{beam}	1.54 sec
Azimuth Bandwidth	Δf_a	1.19 KHz
Oversample Factor	f_{os}	1.2

TABLE 2

NOMINAL VOIR RADAR PROCESSING PARAMETERS

Processing Parameter		Value
Range Resolution	ρ_r	191 m
Range Time-Bandwidth Product	TB_r	42.25
Range Compression Ratio	RCR	60
Sampling Rate	SR	3 Msps
Samples Per Echo	N_s	1320
Sampling Window	T_s	440 μsec
Pulses Coherently Integrated	N_{coh}	60
Coherent Integration Time	T_{coh}	0.049 sec
Azimuth Resolution	ρ_a	225 m
Pulses Per Data Dump	N_{dump}	30
Time Per Data Dump	T_{dump}	0.0245 sec
Distance Per Data Dump	Δ_{dump}	175 m
Pulses in Beamwidth	N_{total}	1886
Looks	N_{look}	30
Filter Channels Per Look	N_{chan}	2

integration over 60 pulses is necessary to achieve a single-look image of approximately 200-meter resolution.

Analysis conducted during the FY'77 VOIR mission study has shown that range migration correction is not required for the 200-meter low resolution mode[3]. This significantly simplifies the on-board computational requirements. However, azimuth focusing computations must be updated and effected commensurate

TABLE 3

RADAR EQUATIONS

Range Processing

$$\rho_r = \frac{(f_{os})\ C}{2(\Delta f_r)\ \sin\theta_i} \qquad SR = 2(\Delta f_r)\ (f_{os})$$

$$TB_r = (T_r)\ (\Delta f_r) \qquad \Omega_r = \frac{\lambda}{W}$$

$$RCR = (TB_r)(f_{os}) \qquad SW = \frac{\lambda R}{W \cos\theta_i}$$

Azimuth Processing

$$N_{coh} = (T_{coh})(PRF) \qquad T_{beam} = \frac{R\lambda}{VL}$$

$$T_{coh} = \frac{(f_{os})\ R\lambda}{2\ V\ \rho_a} \qquad N_{total} = (T_{beam})(PRF)$$

$$\rho_a = \frac{(f_{os})\ R\lambda}{2\ V\ T_{coh}} \qquad N_{look} = \frac{N_{total}}{N_{coh}}$$

$$N_{dump} = \frac{\Delta_{dump}\ (PRF)}{V} \qquad N_{chan} = \frac{N_{coh}}{N_{dump}}$$

$$T_{dump} = (N_{dump})\ (IPP) \qquad \Omega_a = \frac{\lambda}{L}$$

$$\Delta_{dump} = (T_{dump})\ V \qquad \Delta f_a = \frac{2V}{L}$$

with orbital variations in Doppler chirp rate and antenna beam pointing angle. The parametric data that must be provided in real time to effect these computations is defined in Figure 1. Referring to Figure 1, outside information defining the spacecraft attitude, antenna beam angles, and the spacecraft state-of-motion are necessary in order to generate the proper azimuth reference coefficients. To reduce the accuracy requirements of the spacecraft attitude information, the proposed design of Figure 1 incorporates the capability to compute a refined measure of the spacecraft attitude based on the characteristics of the SAR data itself. This Doppler centroid information is derived by means of energy spectral analysis of single-look images following azimuth correlation. These calculations would be performed by appropriate microprocessors which are part of the on-board SAR processor.

The detailed outside information requirements with respect to parameter and accuracy are tabulated in Table 4. The criteria for resolution is a nominal 200 meters ±25 percent. It should be noted that the ±1 Km position accuracy is based on satisfactorily meeting the resolution requirements. This does impose a pixel registration error of that magnitude which may or may not be acceptable.

3.0 ON-BOARD SAR PROCESSOR ARCHITECTURE

A functional block diagram of the proposed on-board SAR processor is defined in Figure 2. Referring to Figure 2, the data interface unit receives, conditions, and distributes incoming raw SAR video and parametric engineering data required to process SAR images. The range correlator performs the range correlation function. The azimuth correlator performs the azimuth correlation function, antenna beam pointing correction, digital magnituding, and multi look superposition. The microprocessor controller computes the necessary corrections and effects control functions for all functional elements of the processor.

Referring to the processing requirements listed in Table 2, the range correlation function could be achieved with four 60-stage transversal filters as shown in Figure 3. The block diagram of Figure 3 assumes real (I) and quadrature (Q) channels from the radar receiver. If the output data from the SAR receiver is "range offset" so that it only contains real components over a

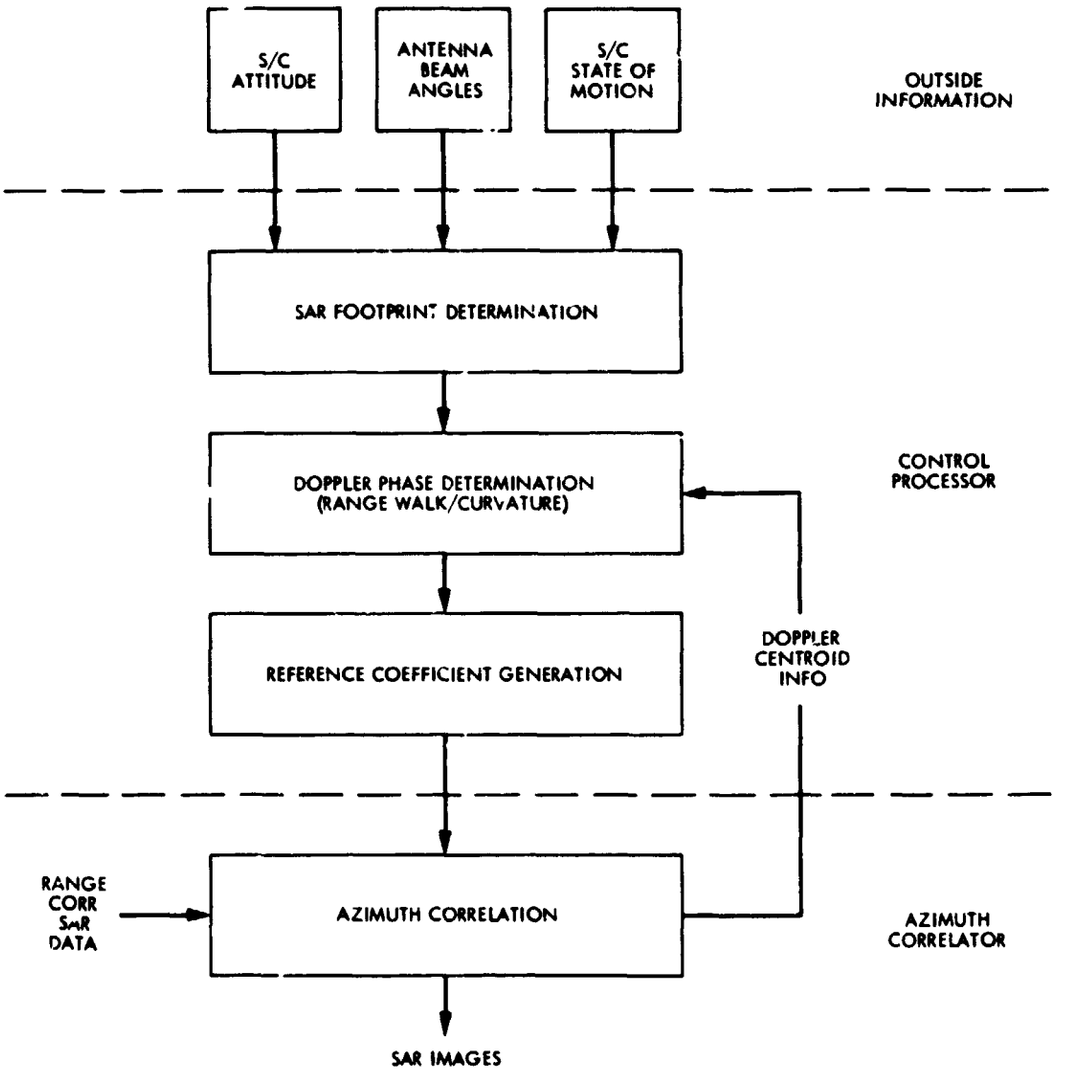

Figure 1. VOIR Azimuth Reference Function Generation

TABLE 4

OUTSIDE INFORMATION REQUIREMENTS

Parameter	Accuracy	Effects of Inaccuracy
S/C Attitude		
Roll	$\pm 1^{o}$	Reduced SNR
Pitch	$\pm 0.4^{o}$	Reduced SNR + Doppler Ambiguity
Yaw	$\pm 0.4^{o}$	Reduced SNR + Doppler Ambiguity
Antenna Beam Angles		
θ_{look}	$\pm 0.4^{o}$	Reduced SNR + Doppler Ambiguity
ϕ_{az}	$\pm 0.4^{o}$	Reduced SNR + Doppler Ambiguity
S/C State of Motion		
Position	± 1 Km in Three Directions	Pixel Registration Error of that Magnitude + Resolution Degradation
Velocity	± 60 m/sec in Three Directions	Resolution Degradation
Acceleration	± 0.1 m/sec^2 in Three Directions	Resolution Degradation

single channel, the range correlator implementation of Figure 4 could be used. Use of two 128-stage transversal filters (one cosine filter and one sine filter) would provide an output equivalent to that from Figure 3.

The azimuth correlator of Figure 2 could be implemented to meet the requirements listed in Table 2 using 60 parallel azimuth filter channels as shown in Figure 5. Two filter channels are required to process a single look.

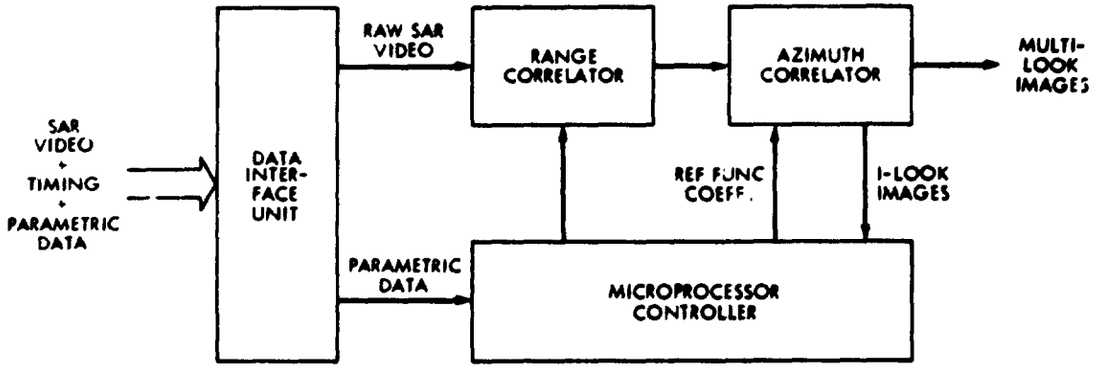

Figure 2. VOIR On-Board SAR Processor Block Diagram

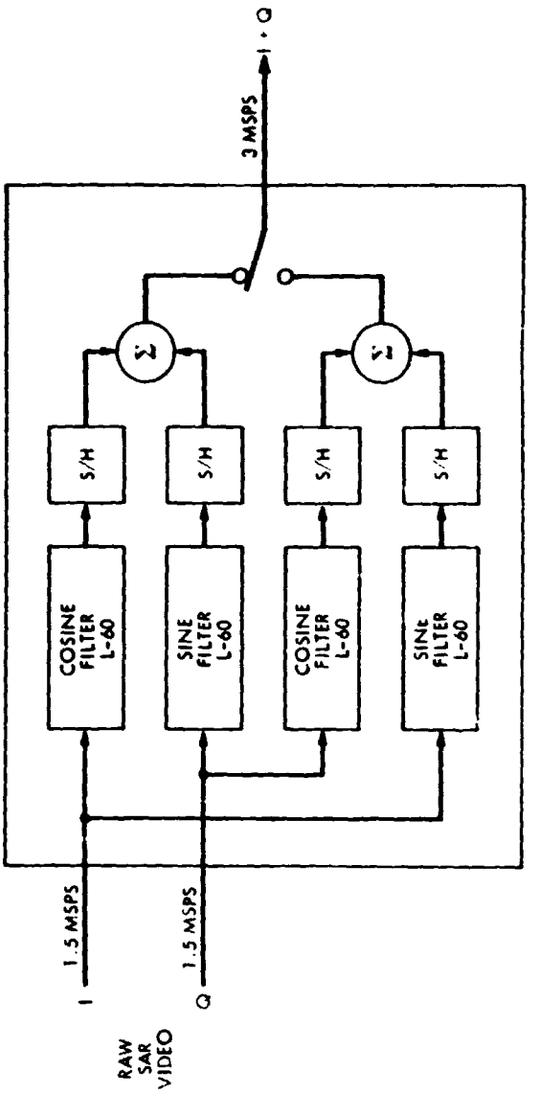

Figure 3. VOIR Range Correlator (Complex Input)

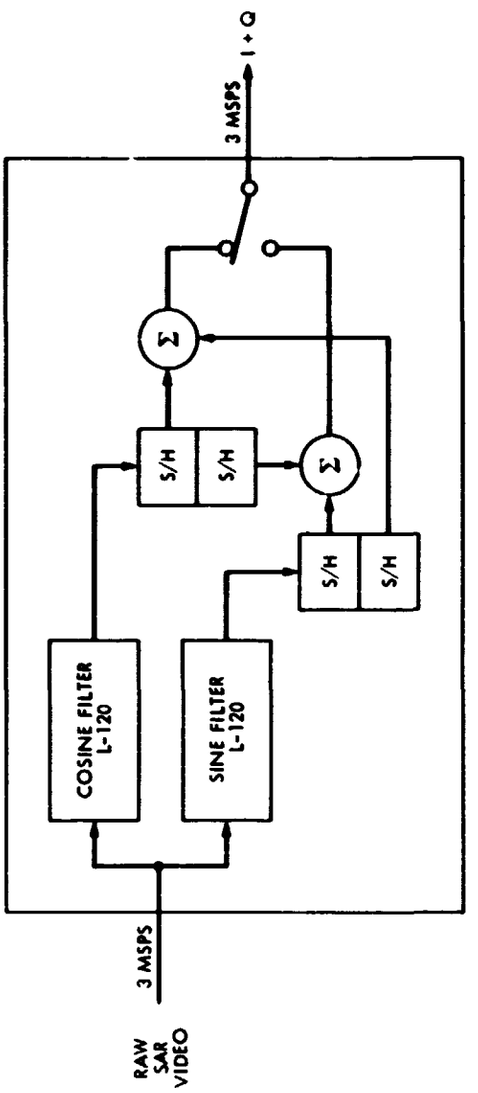

Figure 4. VOIR Range Correlator (Range Offset Input)

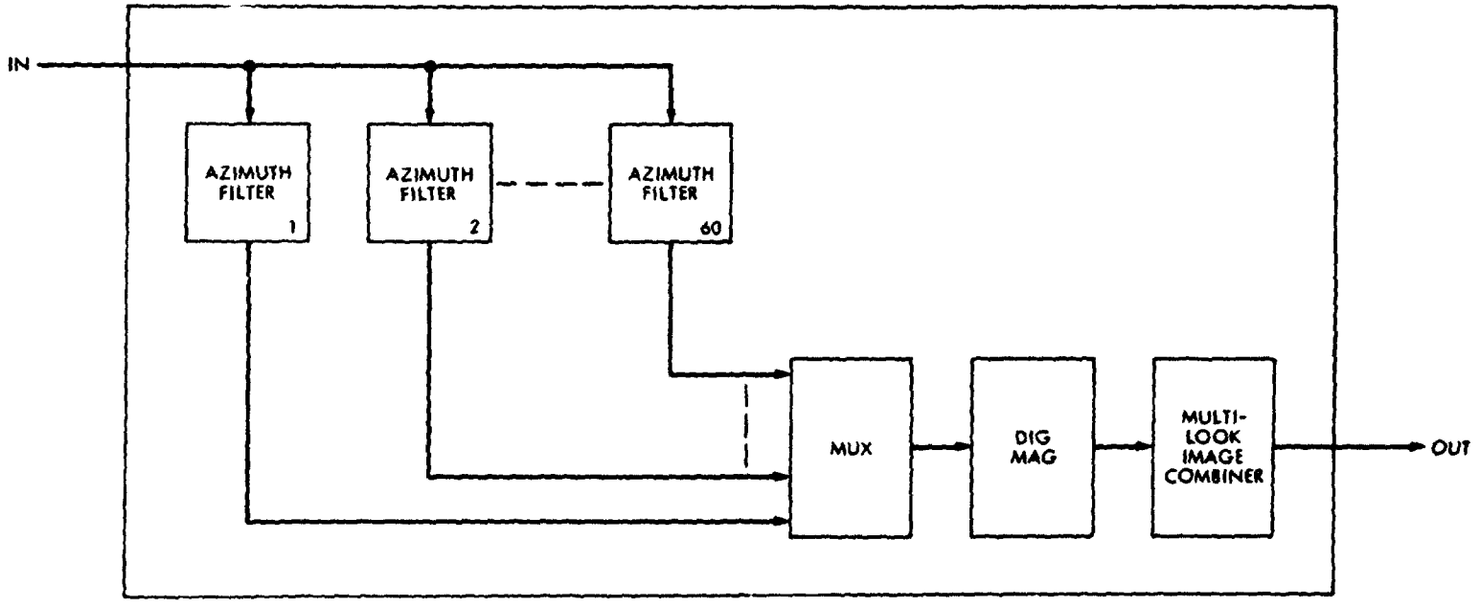

Figure 5. VOIR Azimuth Correlator

Therefore, the implementation of Figure 5 is capable of processing and superimposing 30 looks. The digital magnituding and multi-look combining functions of Figure 5 are achieved as defined in the FY'77 JPL VOIR mission study report [3].

A functional block diagram of a single azimuth filter channel is given in Figure 6. The complex multiplier must accommodate 8-bit complex words containing 4 bits of I and 4 bits of Q. The accumulator register must accommodate 600 complex words of up to 28 bits. If there is no transfer of coefficients between channels, a reference table would have to accommodate 120 complex coefficients assuming there are 2 coefficients per range line. An alternative design approach would be to store only 60 coefficients per channel and transfer sets of coefficients between channels.

4.0 IMPLEMENTATION CHARACTERISTICS

Referring to Figure 1, the baseline design assumes CMOS-SOS technology for implementation of the data interface unit and the microprocessor controller. It appears that two 16-bit CMOS-SOS microprocessors will accommodate the computational load for the controller.

Charge-coupled device (CCD) transversal filter chips are assumed for the range correlator implementation. This is based on having a fixed digital reference function.

Implementation of the azimuth correlator is assumed to be accomplished with existing CMOS-SOS chip designs so that it is not dependent upon the custom digital CCD chip being developed for the DMSP. Assuming a mask change is made to two existing universal array CMOS-SOS chips to accomplish the complex multiply and add function of Figure 6, 15 chips would be required per azimuth filter channel with a per channel power requirement of 0.35 watts.

Based upon the foregoing assumptions, a chip count has been made for implementation of each functional block of Figure 1. The required number of chips, with the associated power and weight estimates to implement the VOIR on-board SAR processor of Figure 2, are tabulated in Table 5.

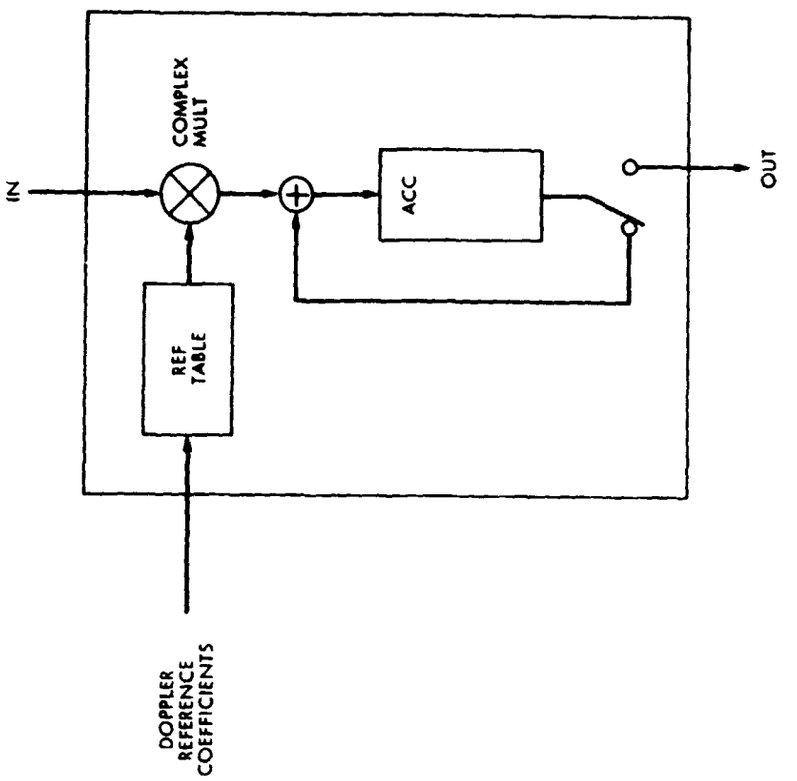

Figure 6. VOIR Azimuth Filter

TABLE 5

IMPLEMENTATION CHARACTERISTICS

Function	Chips	Power (Watts)	Weight (Kg)
Data Interface Unit	60	4	1.5
Range Correlator	10	1	0.5
Azimuth Correlator	1050	30	24
Controller	170	20	4
Totals	1290	55	30

5.0 REFERENCES

1. Arens, W.E., The Application of Charge-Coupled Device Technology to Produce Imagery from Synthetic Aperture Radar Data, Proceedings of the AIAA System Design Driven by Sensors Conference, Pasadena, California/ October, 1976.
2. Arens, W.E., CCD Architecture for Spacecraft SAR Image Processing, Proceedings of the AIAA Computers in Aerospace Conference, Los Angeles, California/October, 1977.
3. Beal, R.C., Venus Orbiter Imaging Radar FY'77 Study Report - Radar Studies, Document No. 660-60, Jet Propulsion Laboratory, California Institute of Technology, Pasadena, California/May, 1977.