APPLICATIONS AND LIMITATIONS OF VERY LARGE-SCALE INTEGRATION IN SAR AZIMUTH PROCESSING

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SUMMARY

By using digital CCD's for data storage and single-chip multiplier accumulators, a low-power, high-density convolution processor may be designed. The memory tradeoffs involving chip design and speed are related to the operation of the processor and several optimum memory organizations are given. The major limitation of a convolution processor designed with CCD memory chips is the inability to operate in real time except for slow aircraft speeds or coarse resolutions. Two methods of summing the products are evaluated with respect to speed, power, and space requirements. A convolution processor is designed, and the number of chips as well as the power and volume requirements are determined using 4-, 6-, and 8-bit data words. The processor is flexible because range samples may be traded for additional azimuth samples by altering the control signals. The processor is also modular, and additional range or azimuth samples may be processed by adding more cards. Additional azimuth looks may be obtained by duplicating the single-look processor.

1.0 INTRODUCTION

The largest amount of hardware and the highest power requirement in a SAR data processor have been used to process the data in the azimuth or along-track dimension. The prefiltered azimuth data are stored in a corner-turning memory for the length of a synthetic aperture and convolved with the azimuth reference function to obtain processed azimuth samples. All range samples for a given azimuth position are processed before processing the

next group of range samples. The convolution operation performed on N azimuth samples may be expressed by the equation:

$$S_o(mT) = \sum_{n=(N-1)/2}^{n=(N+1)/2} h(nT)S_i(mT - nT) \quad , \qquad (1)$$

where

$S_o(mT)$ = complex output samples
N = samples in synthetic aperture
$h(nT)$ = complex reference
$S_i(mT - nT)$ = complex input samples.

From eq. (1), the number of complex multiplications required per output sample is N, and the number of summations is N - 1. The in-phase and quadrature samples representing digitized radar returns collected for a synthetic aperture are stored in the CCD memories, multiplied by the complex reference function, and accumulated to give the azimuth-compressed signal (see Fig. 1). Convolution processing requires a continuous stream of data with the oldest data sample being replaced by the newest sample after each azimuth output.

2.0 CCD MEMORY CHARACTERISTICS

The first element in the data path of Fig. 1 is the CCD memories, which store the samples until a synthetic aperture length of data has been collected. Three types of 65K CCD memories are presently available from different sources. The 65K CCD memories from Fairchild, F464, and Texas Instruments, TMS 3064, are organized as sixteen 4K shift registers which operate at a maximum speed of 5 MHz. The single-bit output is selected from one of the 16 shift registers by a 4-bit address. The Intel device, 2462, is organized as 256 registers of 256 bits each, and the maximum clock rate is 1 MHz. All three memories have a read-circulate, write, and read-modify-write mode. When performing the convolution operation, the read-

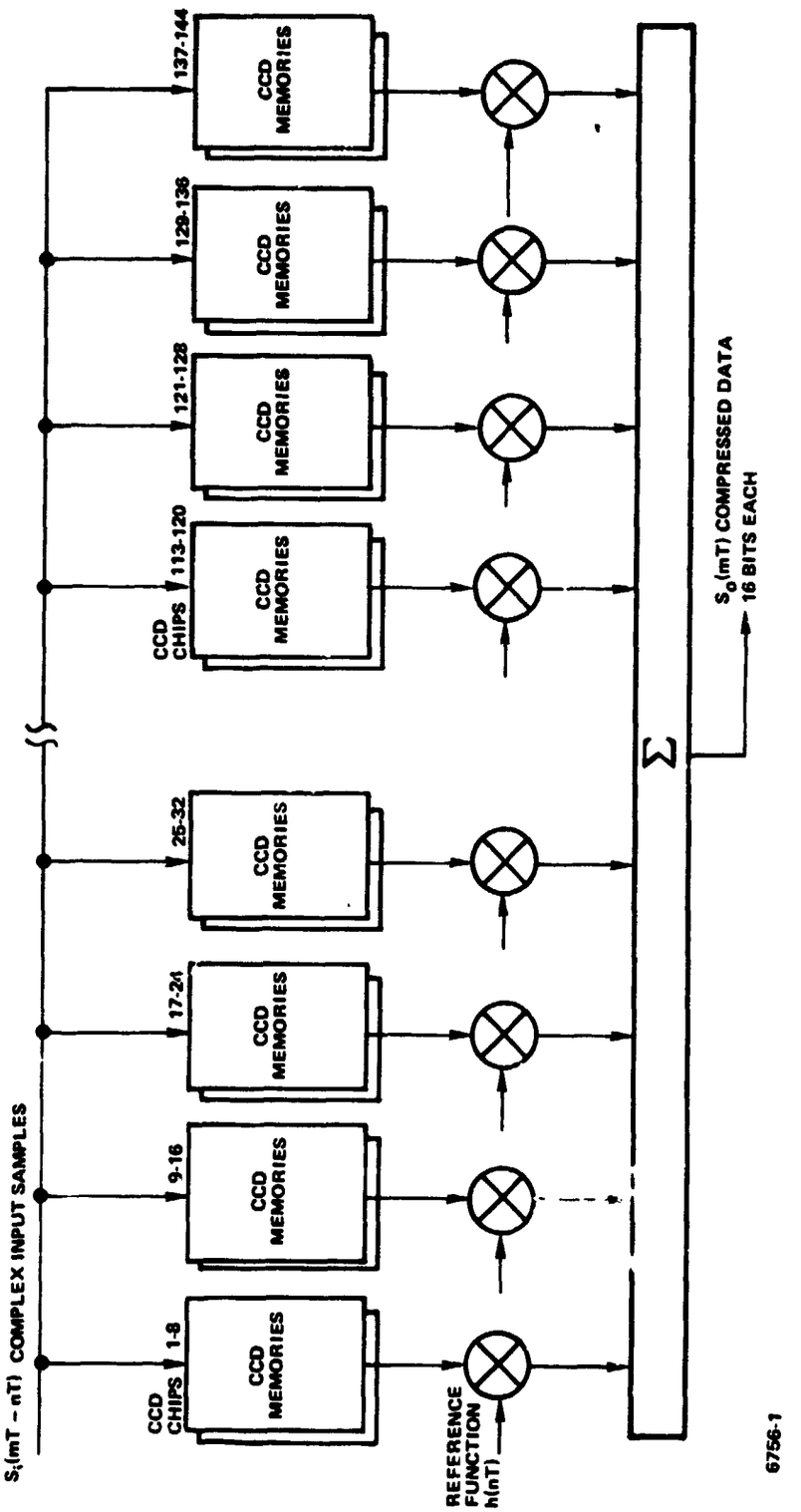

Fig. 1. Azimuth Convolution Processor

recirculate and write modes are used. The TMS 3064 and the F464 chips require 12-V clock drivers, while T^2L clocks are used on the 2462. The time required to output all 65K bits from the CCD memories (T_o) is 13.1×10^{-3} s for the TMS 3064 and the F464 when operating at a 5-MHz clock rate and 65.5×10^{-3} s from the 2464 when operating at a 1-MHz clock rate. This is the minimum time to process all range samples for a particular azimuth position and provides a real-time azimuth resolution, W_a, of

$$W_A = 1.25 T_o V_a \quad , \tag{2}$$

where V_a is the aircraft velocity, and 1.25 azimuth samples per resolvable element are processed to give 30-dB azimuth sidelobes.

Assuming an aircraft speed of 1000 ft/s, the best azimuth resolution available in real time is 16.4 ft from the F464 and TMS 3064 devices and 81.8 ft from Intel's 2464. Better azimuth resolution may be obtained by recording the data on magnetic tape in real time and using a lower speed for playback. Five-ft resolution may be obtained by reducing the tape playback speed by a factor of 3.3. This assumes enough complex multipliers are used so that the shift rate in the CCD memory is the limiting parameter.

3.0 PROCESSOR MEMORY ORGANIZATION

Many combinations of bit length, range samples, and azimuth samples for a CCD memory chip are available as shown in Table 1. To avoid complex timing or address record keeping, the product of the bits per data word and the range samples should equal some multiple of the shift register length. Because the chips are organized as single-bit input and output, several bits of the same word may be stored sequentially in each shift register. However, if parallel multipliers are used in the correlator, a serial-to-parallel converter must be used at each CCD output. Such an organization is desirable only if the number of range samples is less than the CCD shift register length, in which case part of the shift register would remain unused. The number of bits per data word, N_B, column 1 of Table 1, is determined by

TABLE 1 - OPTIMUM CHIP ORGANIZATIONS

N_B Bits in I or Q	C_P Clock pulses/ word	N_R Range samples/ range line	N_{AZ} Azimuth samples/ chip
4	1 2 4	$\frac{N_{sh} \cdot m}{CP}$	$\frac{2^{16}}{N_{sh} \cdot m}$
6	1 2	↓	↓
8	1 2 4 8	↓	↓

the dynamic range requirements and will be considered fixed at 4, 6, or 8 bits, although there is some interest in single-bit processors. The number of clock pulses per data word, C_P, determines how many bits of each data word are stored on a chip. The most practical combinations are a single-clock pulse, $C_P = 1$, in which case a single bit is stored in each chip and N_B parallel chips are required; and $C_P = N_B$, in which case all bits of a data word are stored on a single chip and the data are output serially. The number of range samples, N_R, stored for each azimuth sample (column 3 of Table 1) is given by

$$N_R = \frac{N_{sh} \times m}{C_P} \quad , \tag{3}$$

where N_{sh} is the number of bits per shift register in the CCD, and m is the number of shift registers filled by a range line of data. The upper limit

of m is the number of shift registers in the CCD, 16 in the TMS 3064 and F464, and 256 in the Intel 2462. The number of range samples per PRF is given by

$$N_R = \frac{K\Delta S}{W_r} \quad , \tag{4}$$

where ΔS is the slant range swath and W_r is the slant range resolution. The number of shift registers in a CCD required to store a range sample is given by combining eq. (3) and (4) and solving for m:

$$m = \frac{K\Delta S C_P}{W_r N_{SH}} \quad . \tag{5}$$

The number of azimuth samples stored in a CCD memory, column 4 of Table 1, is given by:

$$N_{AZ} = \frac{N_{CCD}}{N_R \cdot C_P} = \frac{2^{16}}{N_{SH} \cdot m} \quad , \tag{6}$$

where N_{CCD} is the number of bits in a CCD (64K). The number of azimuth samples across the synthetic aperture, N_{LS}, required to process the data to an azimuth resolution, W_a, is given by.

$$N_{LS} = L_S \cdot \frac{K}{W_a} = \frac{K^2 R\lambda}{2W_a^2} \quad . \tag{7}$$

The number of chips required to store a fraction C_P/N_B of the data is determined by dividing eq. (7) by eq. (6):

$$\frac{N_{LS}}{N_{AZ}} = \frac{K^2 R\lambda}{2W_a^2} \cdot \frac{N_R C_P}{N_{CCD}} \quad . \tag{8}$$

The total number of memory chips, N_{CH}, is then obtained by multiplying eq. (8) by N_B/C_P to give:

$$N_{CH} = \frac{K^2 R \lambda}{2W_a^2} \cdot \frac{N_R C_P}{N_{CCD}} \cdot \frac{N_B}{C_P} = \frac{N_{LS} N_R N_B}{N_{CCD}} \quad . \tag{9}$$

The number of chips required varies inversely as the range resolution, inversely as the square of the azimuth resolution, and directly as the range and range swath.

4.0 PROCESSOR DESIGN

As an example of azimuth processor design, a slant range swath of 10 mi is imaged at a maximum range of 30 mi with azimuth and range resolution of 10 ft with I and Q data channels of 4 bits each. The displacement caused by range curvature may be determined from the equation:

$$D = \frac{L_S^2}{8R_o} \quad , \tag{10}$$

which for an X-band radar, $\lambda = 0.1$ ft, is 1.75 ft. This is sufficiently small so that range curvature correction is unnecessary. The value of m is, from eq. (5) when using $N_{SH} = 4096$, and $C_P = 1$,

$$m = \frac{K \Delta S C_P}{N_{sh} W_r} = \frac{1.25 \times 10 \text{ NMI} \times 6000 \text{ ft/NMI} \times 1}{4096 \times 10 \text{ ft}} = 1.83 \quad .$$

Because m must be an integer, the next highest value, m = 2, is chosen. This increases the slant range swath from 10 NMI to 10.9 NMI. The number of range samples is, from eq. (3),

$$N_R = \frac{N_{SH} \cdot m}{C_P} = \frac{4096 \times 2}{1} = 8192 \quad .$$

The number of azimuth samples stored per chip is, from eq. (6),

$$N_{AZ} = \frac{N_{CCD}}{N_R \cdot C_P} = \frac{65\ 536}{8192} = 8 \quad .$$

The number of azimuth samples across the synthetic aperture, N_{LS}, is determined from eq. (7) to be:

$$N_{LS} = \frac{K^2 R\lambda}{2W_a^2} = \frac{(1.25)^2 \times 30 \text{ NMI} \times 6000 \text{ ft/NMI} \times 0.1 \text{ ft}}{2 \times (10 \text{ ft})^2} = 140.6 \quad .$$

Because 8 azimuth samples are stored per chip, the number of azimuth chips required is 140/8 = 17.5, so 18 azimuth chips are used, increasing the number of azimuth samples, N_{LS}, to 144. The total number of CCD chips required for azimuth processing may be determined from eq. (9) to be:

$$N_{CH} = \frac{N_{LS} \cdot N_R \cdot N_B}{N_{CCD}} = \frac{144 \times 8192 \times 8}{65\,536} = 144 \quad .$$

The power required is approximately 0.25 W/chip, or 36 W total, for the memory and 19 W for the 42 clock drivers. The memory and clock drivers require three printed-circuit boards.

5.0 MULTIPLIER ACCUMULATOR

The data are output from the memory to the multipliers (see Fig. 1). The product of the complex signal and the complex reference is formed and summed for all azimuth data points. The four products which are formed to give the in-phase and quadrature components are:

$$\left.\begin{aligned} \text{In-phase} &= S_I R_I - S_Q R_Q \\ \text{Quadrature} &= S_I R_Q + S_Q R_I \end{aligned}\right\} \quad . \tag{11}$$

The choices of integrated circuits to perform the complex multiplications are an 8-bit multiplier from Monolithic Memories and an 8-bit multiplier-accumulator from TRW. The multiplier chip requires an output latch as well as an adder stage and an accumulator to equal the capability of the 8-bit TRW multiplier accumulator. The combined space and power requirements of the multiplier, latch adder, and accumulator combination are greater by

a factor α 2 than the space and power required by the TRW chip, which uses 1.2 W to accomplish a multiply-accumulate operation in 70 ns. Because the multiplier accumulator operates at greater than a 10-MHz rate, a single chip can accumulate the products of either the in-phase or quadrature components of eq. (11) by forming the first product and then adding or subtracting the second. The multiplier accumulator output is a 19-bit sum of products which may accommodate sixteen 15-bit products without overflow. Fifteen-bit products result from the multiplication of two 8-bit words. Sixty-four products of 11 bits each may be accumulated without overflow when there are 6 bits in the signal and the reference, and 256 products of 7 bits each when there are 4 bits in the signal and the reference. If the data rate to the compression filter is slowed sufficiently so that 256 products of 7 bits each may be stored in the accumulator, only a minimum number of accumulators are required to do the convolution indicated in eq. (1).

Assuming a 5-MHz shift rate in the CCD's, a single accumulator may store the in-phase or quadrature products for the eight azimuth samples stored in a CCD memory. The required number of multiplier accumulators is then $144/8 \times 2 = 36$. The required power is 1.2 W/chip $\times$ 36 chips = 43 W. An additional 8 W is required to multiplex the CCD outputs to form the two products indicated in eq. (11) for the in-phase and quadrature channels. The final operation in performing the convolution operation is to add the outputs of the multiplier accumulators (18 I and 18 Q accumulators). The number of bits output from each accumulator in the example used is 11 (16 products of 7 bits each). The power required to accumulate the final products is 20 W, and the number of chips required to sum the accumulator outputs is 260, consisting of latches and adders. The output is a 16-bit sum of products in I and Q, occurring each 1.6 μs. The power and chip requirements for each function are listed in Table 2. The reference function generator is not included in the table, but a reasonable estimate would be two cards and a total power consumption of 10 W.

TABLE 2 - SUMMARY OF PROCESSOR REQUIREMENTS

Bits I or Q input	Chips (W)					Power required (W)	Volume requirements	Bits I or Q output	Output data rate (Mbs)
	Memory	Clock driver	Multiplexer	Multiplier accumulator	Final accumulator				
4	144 (36)	42 (19)	36 (8)	36 (43)	260 (20)	126	11 boards 0.35 cu ft	16	20×10^6
6	216 (54)	60 (27)	72 (16)	36 (43)	334 (26)	166	19 boards 0.604 cu ft	20	25×10^6
8	288 (72)	78 (36)	72 (16)	36 (43)	422 (32)	199	19 boards 0.604 cu ft	24	30×10^6

6.0 CONCLUSIONS

Modern CCD memories and signal processing chips provide the capability to design and build radar signal processors using a fraction of the volume and power required by present processors. As a comparison with current technology as exemplified by the SAPPHIRE processor, the size of an azimuth processor employing CCD memories and signal processing chips would occupy seven percent of the volume and use five percent of the power. It would have applications where near-real-time processing was satisfactory and where low power, size, and volume were desirable.

Other desirable attributes include a reduction in the number of individual printed circuit card types and the number of interconnections which enhance the reliability and reduce the cost. The processor is flexible because range and azimuth tradeoffs may be performed within each chip as given in Table 1. The processor is also modular with the basic module consisting of a single processor card which includes both the memory and the multiplier accumulator. As a result of fewer parts and simpler design, the life cycle costs of operation and maintenance are also reduced.

FRIDAY, MARCH 10, 1978

VI. SYSTEM DESIGN (8:00 - 11:20), Chairman: D. Held, Jet Propulsion Laboratory

**Withdrawn