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# NUCLEAR SURVIVABILITY CONCEPTS FOR AIRBORNE COMPUTERS

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## Abstract

This paper reviews design concepts for nuclear survivability of computers used in aircraft and spacecraft. Data is provided to relate dose rate and total dose tolerance. The vulnerability of available solid state devices is examined and limitations (failure modes) discussed in relation to overall system survivability. The approach is to avoid hardening "overkill" and reduce cost. Two methods of hardening are considered: (1) microprogram or software circumvention for microprocessors containing ROM memory but suffering from transient logic upset, and (2), an instruction/program reload configuration for fast, low-cost random access reloading of a microprocessor containing RAM memories. It is pointed out that LSI semiconductors and microcomputers can be seriously affected by radiation levels which are lower than that required to incapacitate the crew or destroy vehicle structure, from thermal or blast effects. Another consideration is the presence of RF energy known as electromagnetic pulse (EMP) that can damage or degrade semiconductors and produce logic upset. Methods of circumvention described in this paper have been implemented by laboratory model.

## I. Introduction

Survivability of military aircraft from nuclear weapons effects has become a prime consideration in the integration of avionic hardware. Radiation levels, for example, neutron fluence, gamma dose rate and total dose are determined by establishing the maximum allowable dose prior to incapacitation of the crew that would not produce structural damage to the aircraft from thermal and blast effects. With neutron type tactical weapons, however, thermal and blast environments become secondary to incapacitation from the radiation. Many types of LSI semiconductors and microcomputers are seriously affected at radiation levels which do not incapacitate the crew or destroy aircraft structures. To complicate this, RF energy, known as electromagnetic pulse (EMP), also couples into antennas through metallic fuselage structures, apertures, cockpit, etc., of the aircraft and can degrade sensitive semiconductors as well as cause logic upset in digital circuits. The greatest problem associated with radiation effects has been the practice of redesigning avionics to meet specified radiation survivability levels and then requalifying it for general DOD applications. This imposes a prohibitive cost increase; in fact, in a number of cases the projected cost has been so high that the radiation survivability requirement has been eliminated, even though it was needed. Figure 1 shows that the direction that LSI technology is moving would cause concern for their use in military applications.

In the past, radiation specifications led to the need for a custom circuit employing custom technology such as thin film resistors, dielectric isolation, and photocurrent compensating elements. For aircraft (and many satellite applications) this method is a costly overkill. A review of radiation hardening concepts may reveal that in many cases survivability requirements can be met with existing technologies and hardware.

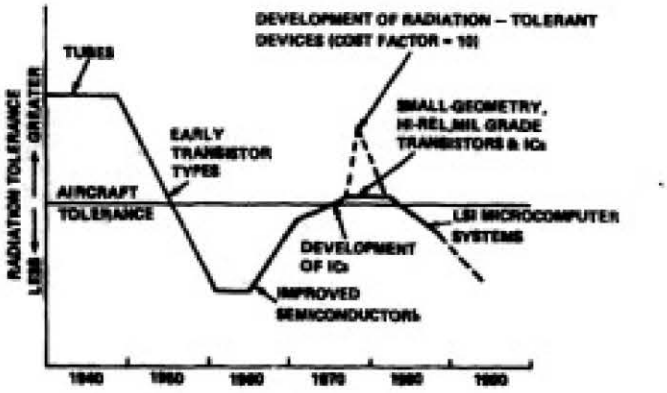



Fig. 1 Chronological Use of Semiconductors in Avionic System Integration

## II. Basic Semiconductor Effects

Gamma radiation will produce photocurrent injection in semiconductor devices in proportion to the dose rate, causing signal perturbations, transient circuit upset and, in some instances junction burnout or circuit latch-up. Neutron fluence interacts within bipolar semiconductors and results in decreased $h_{FE}$ (beta), increased reverse current leakage, increased junction resistance and changes in voltage breakdown and switching parameters.* The $h_{FE}$ of the device is the electrical parameter that changes the greatest and is the signal characteristic which is most critical to circuit function. In general, semiconductor devices with large junction areas (e.g., power transistors) are the most vulnerable to neutron radiation. Conversely, high-frequency devices with relatively small junction areas are less vulnerable.

Both gamma and neutron radiation contribute to the total ionizing dose effects. The total dose affects certain types of devices such as metal oxide silicon field-effect transistors (MOSFETs) and medium-scale integration/large-scale integration devices (MSI/LSI) that contain MOSFETs. The primary effect is the trapping of charges in the gate oxide layers resulting in changes in the threshold levels of switching voltages.

The EMP fields associated with a nuclear weapon burst couple into antennas, metallic fuselage structure, apertures, cockpit, etc. of the aircraft causing large-magnitude, short-duration currents to flow on the surface of the structure. The generated surface charge or currents do not cause damage to the airframe itself, but the recoupling of voltages and fields into interconnecting wiring and circuits can result in induced signals that damage or cause digital upset to sensitive semiconductor devices. Typical skin currents for aircraft can range from 1,000 amperes to 10,000 amperes at the related frequencies of the EMP fields.

* Although these effects all occur due to neutron fluence radiation; except for serious gain ($n_{FE}$) degradation, other effects are minimal for aircraft radiation environments.



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Table 1 Dose Rate Tolerance Levels* of Integrated Circuits[4]

| TECHNOLOGY | DOSE RATE HARDNESS LEVEL, RADS (Si)/SEC | REMARKS |
|---|---|---|
| $T^2L$ | $5\times10^8$ to $1\times10^9$ | UNHARDENED CIRCUITS. |
| $T^2L$/DI | $5\times10^9$ to $2\times10^{10}$ | INCLUDES THE FULL RANGE OF HARDENING TECHNIQUES. |
| $LST^2L$ | $5\times10^7$ to $5\times10^8$ | PRESENTLY ACHIEVED ON UNHARDENDED CIRCUITS. |
| $LST^2L$/DI | $2\times10^9$ to $5\times10^9$ | PROJECTED VALUE USING THE FULL RANGE OF HARDENING TECHNOLOGY. |
| ECL | $8\times10^8$ to $2\times10^9$ | PRESENTLY ACHIEVED IN UNHARDENED CIRCUITS. |
| ECL/DI | $2\times10^9$ to $1\times10^{10}$ | PROJECTED VALUE USING THE FULL RANGE OF HARDENING TECHNOLOGY. |
| $I^2L$ | $2\times10^8$ to $5\times10^9$ | PRESENTLY ACHIEVED IN UNHARDENED CIRCUITS. |
| | $5\times10^9$ to $4\times10^{10}$ | PROJECTED VALUE USING. |
| NMOS/BULK PMOS/BULK | $1\times10^8$ to $1\times10^9$ | UNHARDENED CIRCUIT . |
| | $1\times10^6$ to $1\times10^7$ | DYNAMIC MOS CIRCUITS. |
| | $1\times10^8$ to $1\times10^9$ | HARDENED CIRCUITS, LOWER THRESHOLD FOR WIDE PULSE. |
| CMOS/BULK | $8\times10^8$ x $2\times10^9$ | PRESENTLY ACHIEVED: LOWER VALUES FOR LONG PULSES. |
| | $2\times10^9$ to $5\times10^9$ | |
| NMOS/SOS PMOS/SOS | $1\times10^9$ to $1\times10^{10}$ | LITTLE EXPERIMENTAL DATA IS AVAILABLE TO VERIFY THIS LIMIT. |
| CMOS/SOS | $2\times10^{10}$ to $1\times10^{11}$ | THE HIGHEST DOSE RATE HARDNESS HAS SO FAR BEEN ACHIEVED IN THIS TECHNOLOGY. |

DI = DIELECTRIC ISOLATION
BULK = BULK SEMICONDUCTOR SUBSTRATE
SOS = SILICON-ON-SAPPHIRE SUBSTRATE
FF = FLIP-FLOP

Table 2 Total Dose Tolerance Levels* of Integrated Circuits[4]

| TECHNOLOGY | TOTAL DOSE RADS (Si) | REMARKS |
|---|---|---|
| $T^2L$, $ST^2L$ | $10^5$ to $10^7$ | COMMERCIAL UNHARDENED |
| | $10^6$ to $10^8$ | HARDENED COMMERCIAL (SURFACE DAMAGE A MINOR THREAT; HIGHLY CURRENT DEPENDENT) |
| ECL | $10^7$ to $10^8$ | COMMERCIAL UNHARDENED (SURFACE DAMAGE A MINOR THREAT) |
| $I^2L$ | $10^3$ to $10^4$ | COMMERCIAL, .01 mW/GATE |
| | $10^4$ to $10^5$ | COMMERCIAL, .01 mW/GATE |
| | $10^5$ to $10^6$ | COMMERCIAL, .1 mW/GATE |
| | $10^6$ to $10^7$ | PROJECTED, HARDENED VERSION |
| PMOS/BULK | $10^4$ to $2\times10^5$ | COMMERCIAL |
| | $10^7$ | LABORATORY DEMONSTRATED |
| PMOS/SOS | 1 to $5\times10^6$ | LABORATORY DEMONSTRATED |
| CMOS/BULK | $5\times10^3$ to $10^5$ | COMMERCIAL UNHARDENED |
| | $10^5$ | MODIFIED COMMERCIAL |
| | $10^6$ to $10^7$ | LABORATORY DEMONSTRATED |
| CMOS/SOS | $10^3$ to $10^5$ | COMMERCIAL UNHARDENED |
| | 1 to $5\times10^5$ | LABORATORY DEMONSTRATED Si-GATE |
| | $10^5$ to $10^6$ | LABORATORY DEMONSTRATED Al-GATE |

*NEUTRON FLUENCE TOLERANCE OF ICS IS ASSESSED TO BE RELATIVELY HIGH. IN GENERAL, THIS RADIATION DOES NOT PRESENT SIGNIFICANT PROBLEMS FOR MOST AIRCRAFT OR SATELLITE APPLICATIONS HOWEVER, THIS DATA REFLECTS TOLERANCE OF SSI & MSI CLASS OF INTEGRATED CIRCUIT DEVICES. AS DEVICES APPROACH LSI LEVELS, AS IN MICROPROCESSORS, BOTH DOSE RATE & TOTAL DOSE TOLERANCE CAN BE SIGNIFICANTLY LOWERED.

and transient tolerance to aircraft radiation levels may be sufficient to be considered for low cost microcomputer application. It is not recommended for satellite applications without significant shielding.

Emitter Coupled Logic (ECL) has not been included since its power, chip density and cost for microcomputer application are excessive. Nevertheless, ISO II ECL* which is now being produced may change this characteristic as its power dissipation per gate and geometry have been substantially reduced.

## IV. Generalized Viewpoints on Computer Radiation Effects and Hardening

As with all electronic hardware, radiation effects are defined in terms of permanent and transient responses. Basically, permanent effects from neutron fluence, total dose or pulse power failure (EMP) are eliminated by technology selection. In the transient dose effect, however, there are a number of mechanisms in computer or microcomputer operations which significantly differ from performance of other electronic equipment exposed to radiation environment. These are:

- Transient dose-rates can introduce a type of permanent failure to a computer by erasing a stored program in the memory.
- Even if the stored program is not erased, dose-rates effects change the content of accumulators, counters, instruction registers and I/O buffers (logic failures) causing erroneous computational data.
- Additional responses are alteration of timing cycles because of clock effects and disruption of the power supply for microsecond durations.

As indicated, transient dose-rate effects cause a complex combination of hardware interactions eventually nullifying the integrity of the computational processes. Corrective measures then include either elimination of the foregoing effects or schemes which provide for return of computations without introducing gross system errors. Figure 3 characterizes the possible malfunction modes associated with computer processing.

Based on the foregoing analysis, malfunction can be classified according to:

- Memory Malfunction
- Register Content Upset
- Timing Cycle Perturbations
- Power Supply Disruption

* Fairchild Semiconductor

The theoretical aspects of nuclear weapon physics and the equations representing interactions with semiconductors will not be discussed since they are well documented in many excellent reports and publications.[1,2] For this paper, the basic concepts of low cost aircraft survivability will be reviewed.

## III. Technology Consideration

Survivability to radiation has been based upon the selection of semiconductors that meet a specified environment. This means that a class of semiconductor devices (bipolar or insulated gate MOS) are selected that provide optimum tolerance to permanent effects and transient radiation upset of digital hardware. Common practice has been to select the semiconductor technology exhibiting highest tolerance to radiation, for example $T^2L$, or devices previously specified for missile applications even though penalties are paid in overdesign, power dissipation and possible interface incompatibilities. In general, the selection of semiconductors best suited for a given system is becoming more difficult as the number and the performance capability of available semiconductor technologies increase. For the designer of radiation-hardened electronics the choice is further complicated by the operating environment. Tradeoffs between performance in adverse environments and cost and availability of components add to the complexity of the decision.

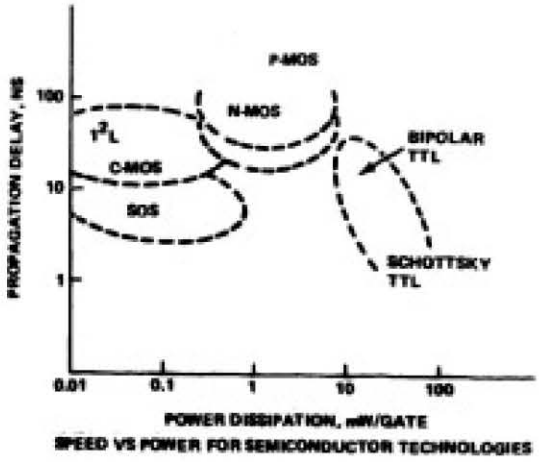
Eight technologies are currently used in design of computer/microcomputers, e.g., four bipolar ($T^2L$, Schottky $T^2L$, ECL, $I^2L$) and four MOS (bulk MNOS, bulk CMOS, CMOS/SOS and NMOS/SOS). $I^2L$ and CMOS/SOS are emerging as less developed, hence risky, technologies but are the two technologies with potentially greatest payoff for radiation-hardened electronics. CMOS is the preferred MOS technology because of its low standby power requirements and high noise immunity. SOS construction reduces the photocurrents generated by a transient radiation pulse and increases circuit speed and packing density. The total dose vulnerability of CMOS/SOS, initially a serious shortcoming, is now reported to be on the order of $10^5 - 10^6$ rads (Si).[3]

$I^2L$ is the leading bipolar candidate for LSI in the 1980s because its packing density and speed-power product are superior to those of the other bipolar technologies. This circuit technique uses no resistors and can be fabricated as a self-isolating structure which enhances its ability to maintain performance in a radiation environment. A general idea of speed vs. power dissipation and density is shown in Figure 2. As indicated, Schottky $T^2L$ will always provide the fastest device, with CMOS/SOS optimized toward power dissipation. Emitter coupled logic (ECL) will not be discussed as the power penalties are excessive, thus limiting its applications.

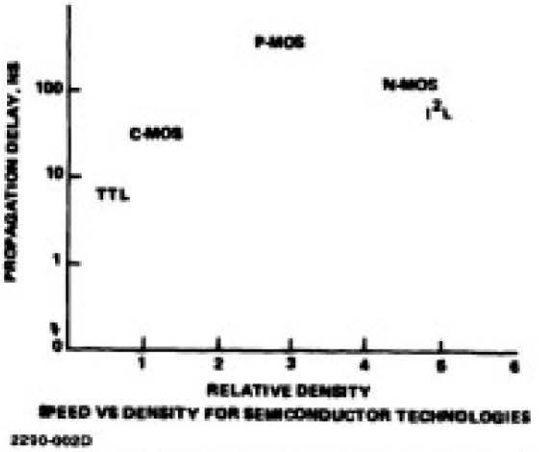
The emerging $I^2L$ has not matured, but certainly is becoming a contender based on its density/power tradeoff Tables 1 and 2 summarize the generic radiation tolerances of IC's currently used in some phase of microcomputer development.[4] Based on existing semiconductor development, the technologies assessed as prominent in aerospace computer/microcomputer applications are as follows:

### Low Power Schottky Transistor-Transistor Logic ($LST^2L$)

This technology will be the mainstream of high speed processing. The primary drawbacks are power and density. Radiation tolerance for both aircraft and satellite environments is estimated to be fair to good.



SPEED VS POWER FOR SEMICONDUCTOR TECHNOLOGIES



SPEED VS DENSITY FOR SEMICONDUCTOR TECHNOLOGIES

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Fig. 2 Characteristic Speeds and Transistor-on-the Chip Densities for Various IC Technologies

Standard $T^2L$ will provide increased dose rate radiation tolerance (about a factor of 5) compared to $LST^2L$. In many instances, no special hardening techniques may be required for aircraft systems that completely utilize this technology.

### Integrated Injection Logic ($I^2L$)

Both low power and chip density are the driving force for this technology. It is estimated that $I^2L$ will replace $LST^2L$ in the commercial market. Radiation tolerance for this technology is fair, basically requiring some form of hardening (circumvention) to overcome the transient upset effects. As this technology matures, further improvement in radiation tolerance can be anticipated.

### Complementary MOS on Sapphire (CMOS/SOS)

Low power dissipation combined with good speed characteristics are the primary features of this technology. Although it exhibits higher speed characteristics than $I^2L$, chip density falls significantly lower. This technology offers excellent radiation tolerance effects. However, it is limited in total dose capabilities compared to its bipolar counterparts. Therefore, in satellite applications, shielding may be required for long duration missions within the Van Allen Belts.

### N-Channel MOS (NMOS)

This technology will remain as the primary low cost IC technology. Speed and tolerance to total dose radiation become its primary drawback. However, neutron fluence

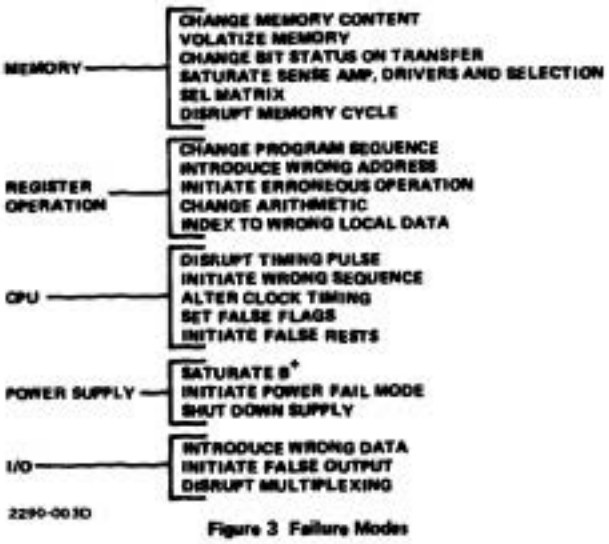



Figure 3 Failure Modes

Hardening techniques usually can provide for eliminating memory and power supply failures. However, specialized hardware and software techniques must be developed based upon machine architecture to minimize errors introduced by logic upset or register content changes. In general, as the complexity of the computer increases, (multiprocessing, specialized I/O features and high speed operation), photocurrent transients produce more serious malfunction. Additional corrective measures both in software and hardware require greater sophistication and complexities.

## Basic Computer Hardening Concepts

Two hardening approaches should be considered - Intrinsic Hardening and Extrinsic Hardening. These approaches are defined as follows:

Intrinsic Hardening - This method utilizes devices which are found to be tolerant to the specific radiation environment and ignores special hardening techniques. It directly depends on the radiation levels considering only aircraft and, to a lesser extent, satellite nuclear environments. Selection of the semiconductor technology (MSI or LSI) usually will involve mil spec devices, screened military grade and special developed hardened devices. For intrinsic application the computer will not be interrupted, but will operate throughout the radiation burst. This procedure normally cannot be used in missile and severe satellite radiation environmental applications. Usually the standard $T^2L$, CMOS/SOS and some instances $LST^2L$ technologies may be utilized for this category. Also, special radiation hardened computer LSI chips under development by various DOD programs may be used for this category.

Extrinsic Hardening - This technique involves development of specialized software or firmware circumvention schemes (roll-back, redundant store, reloading, etc.) and for hardware (NDRO magnetic memories, ROM's, radiation detectors, and hardened timers) to achieve radiation tolerance. This approach is utilized where radiation levels exceed the tolerance of transient response characteristics causing logic upset of the semiconductor devices (photocurrent "turn-on").

For most of-the-shelf microcomputer applications some degree of extrinsic hardening can be utilized. Early consideration usually will avoid costly architectural, hardware and/or software modifications to meet a potential threat scenario. An optimized approach for this category would consist of:

- Computer state put-away (circumvention)
- Dedicated priority interrupt flags for radiation detectors
- Shutdown/Startup procedures
- Microprogrammed optimization

Permanent radiation tolerance of memories, CPU, I/O and power supplies is directly related to the specific semiconductor technologies utilized. Generally, the technologies previously described will meet the neutron fluence requirements for nearly all aerospace requirements. Total dose, on the other hand, must be more critically assessed since a number of NMOS (and PMOS) devices may be marginal for aircraft applications. For the most part, upset logic tolerance will be difficult to achieve unless the radiation environments are significantly low. For memory applications, NDRO or non-volatility characteristics offer the first level of hardening to transient disturbances since a dose-rate induced power-down will not promote loss of memory contents. Magnetics (plated wires, thin films), or ROM and MNOS semiconductors are suitable memory elements in a transient radiation environment. However, additional procedures such as "radiation-clamps" may be required for magnetic memory applications in high level radiation environment since driver "turn-on" and consequent erroneous writing can occur.

## The Circumvention Approach

Circumvention may be accomplished by check points in the main program to store the state of the computer at selected points in the primary program. If a radiation dose rate which exceeds logic malfunction levels ( $\approx 10^8$ rads (Si)/sec) is encountered, the main memory is first checked for program correctness; then the computation is rolled back to the last checkpoint which contains a previous state of the computer. The central processor unit (CPU) is then reloaded with the previous information and reprocessing begins from that point. The number of checkpoints is established on the basis of allowable errors and speed characteristics of the computer. Some considerations necessary for evaluating a microcomputer system for circumvention are shown in Table 3.

Table 3 Microcomputer Hardening Considerations

**ANALYSIS**
- SEMICONDUCTOR TECHNOLOGY
- MEMORY – ROM, RAM
- ARCHITECTURE
- CIRCUMVENTION INSTRUCTIONS – SOFTWARE, FIRMWARE

**ARCHITECTURE**
- BIT SLICE, FIXED BYTE
- PROGRAMMABLE
- INTERNAL/EXTERNAL REGISTERS
- BUS ORGANIZATION
- PC AVAILABILITY
- STACK
- INTERRUPT/FLAGS
- I/O – DMA
- ADDRESSING MODES

**CIRCUMVENTION**
- INTERNAL REGISTER STATES
- CHECKPOINT
- RESTART/RELOAD
- HARD EXTERNAL REGISTERS/MEMORY

The basic principle in microprogrammed or machine language circumvention is to provide a set of micro-instructions (macros associated with the microcomputer), and set up checkpoint (CHKPT) and restart (RESRT) routines. These macros correct for computational errors that might arise from logic upset since the "state" of the microcomputer is stored at defined intervals in the program by the CHKPT instruction. The program is recalled following a transient disturbance by the RSRT instruction. CHKPT and RSRT instructions are either microprograms which reside in the control store of a computer or software subroutines which are included as part of the main program. The programmer initiates circumvention simply by including the CHKPT and RSRT instructions in the normal coding process of a software module. To increase utility of the approach, specially hardened registers can be added to a microcomputer having a multibus organization. Figures 4 and 5 illustrate the circumvention method and results that would be obtained in correcting the computational error.

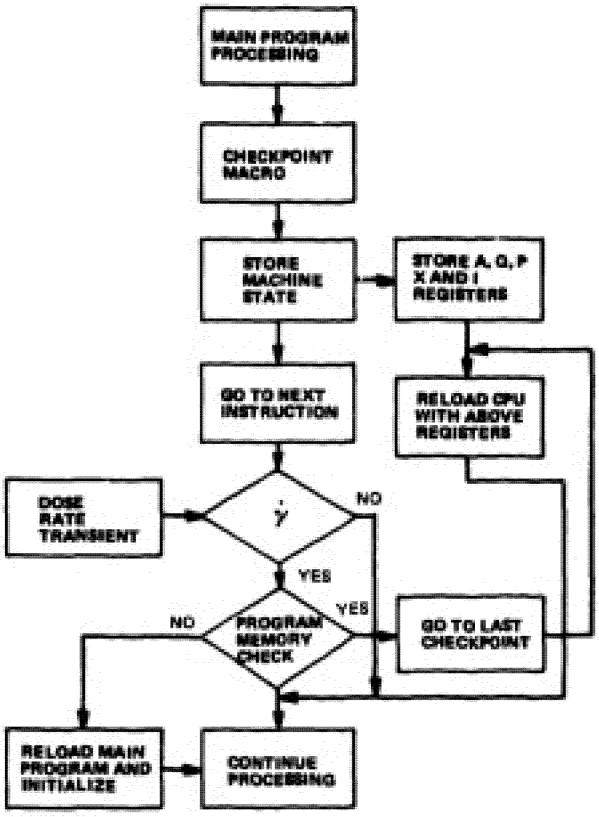



Fig. 4 Circumvention Using Rollback Techniques

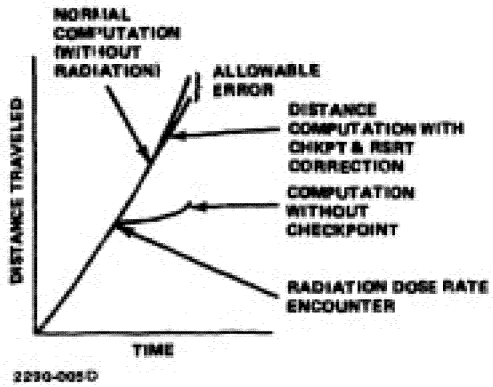



Fig. 5 The Result of Using Circumvention

## V. Implementation Procedure

The modern trend has been to use microcomputers with semiconductor memories as replacements for existing aerospace computers. One approach in developing radiation hardening techniques is based on the principle that many modern aerospace computers, including the new microcomputers, utilize a control-store (microprogrammed) architecture which can be organized to include a special method for circumventing the transient radiation effect. Previously developed software circumvention routines thus can be modified for microprogramming to minimize dose rate induced computational errors and optimize the computer for survivability. Two catagories of microcomputer must be separately studied: those that use read only memories (ROM) as their main storage component and those that use conventional, semiconductor random access memories (RAM) as their main memory. Separate approaches are required for these devices because of their significantly different response to radiation. An ROM memory, for example, has inherent radiation hardness for stored programs, since it is neither affected by transient upset nor power disruption. The use of an RAM, on the other hand, is likely to result in loss of the stored program since it is disturbed by transient upset or power supply disruption. Both devices, however, are subject to logic errors produced within other sections of the microprocessor.

Microcomputers that utilize ROM's as their main storage component can be radiation hardened simply by using circumvention to eliminate computational errors caused by logic upset. As previously described, this circumvention technique enables computation to be restarted at a desired point within the program. Microcomputers that utilize conventional RAMs as the storage element must be equipped with an external auxiliary metal-nitride-oxide semiconductor (EAROM), which is not subject to logic upsets and exhibits relatively high survivability levels. The MNOS memory contains a redundant program, and thus provides a means for supplying the main program with individual instructions, memory pages, or entire memory blocks so that processing can be continued after the exposure to radiation. Reloading the stored program lost in the volatile RAM can be easily accomplished by a simple initiation procedure. In this procedure, both microprogrammed and non-microprogrammed microcomputer can be used. However, the use of a microprogrammed design is more versatile as it reduces main memory storage requirements. It is also faster and allows for restarting at a specified location in the memory. Figure 6 illustrates a hardened microcomputer organization. As shown, reloading of the microprocessor can be accomplished through the direct memory access (DMA) bus. A bootstrap program initiates the microprogram circumvention mode (stored in a control store ROM) and processing commences.

## VI. Conclusions

Accomplishing computer or microcomputer survivability is feasible from cost-effective a standpoint. Basic factors that must be utilized in hardening approaches are:

- Consideration of radiation environmental scenarios
- Selection of semiconductor technologies
- Analysis of radiation induced computer effects
- Memory radiation tolerance assessment
- Software/firmware corrective techniques (circumvention)

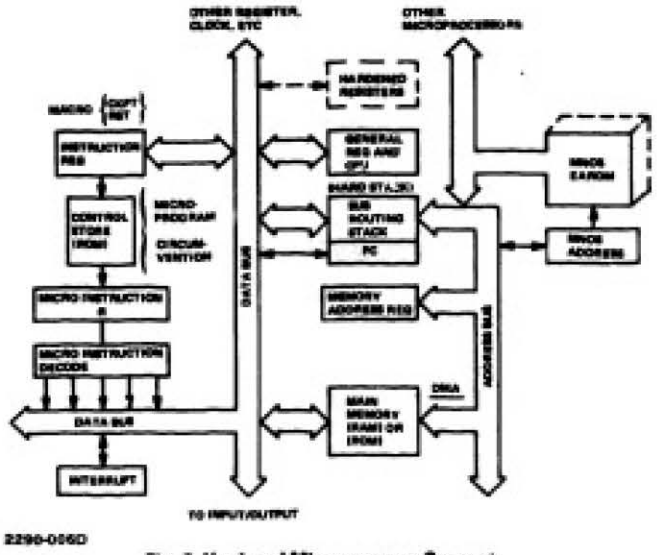



Fig. 6 Hardened Microprocessor Concept

Complexity of the circumvention approach will depend on mission constraints and required computational accuracies. Other features such as radiation detectors, hardened counters, multiple store and special stacks may be necessary.


## Acknowledgements

The author wishes to acknowledge the efforts of Messrs. L. Della Salle and R. Hong for their worthwhile review and comments of this paper. Also, appreciation is extended to Mr. J. Vitale for his dilligent effort in implementing working models of the circumvention approaches in the laboratory.


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