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77-1392

CCD ARCHITECTURE FOR SPACECRAFT SAR IMAGE PROCESSING*

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Abstract

A real-time synthetic aperture radar (SAR) image processing architecture amenable to future on-board spacecraft applications is currently under development. Using state-of-the-art charge-coupled device (CCD) technology, low cost and power are inherent features. Other characteristics include the ability to reprogram correlation reference functions, correct for range migration, and compensate for antenna beam pointing errors on the spacecraft in real time. The first spaceborne demonstration is scheduled to be flown as an experiment on a 1982 Shuttle imaging radar mission (SIR-B). This paper describes the architecture and implementation characteristics of this initial spaceborne CCD SAR image processor.

I. Introduction

Synthetic aperture radar (SAR) image processing is inherently very complex. In space applications it is further complicated by such factors as planetary rotation, atmospheric refraction, and range migration. However, previous research and development performed at the Caltech Jet Propulsion Laboratory (JPL) indicate that it is feasible to develop a spacecraft real-time on-board SAR processing capability using charge-coupled device (CCD) technology.[1,2] A practical on-board processing capability could significantly reduce the data rate and volume requirements currently limiting future mission capability. To pursue this potential benefit, the Office of Applications (OA) and the Office of Aeronautics and Space Technology (OAST) of NASA Headquarters are jointly funding a program to produce a Developmental Model SAR Processor (DMSP) capable of processing spacecraft SAR data in real time. It should be noted that the DMSP task represents only a part of a much larger long-range development program to produce a suitable on-board SAR processing capability in time for SAR missions in the period from 1981 to 1986. The DMSP itself will be a ground-based breadboard system capable of demonstrating both an architecture and an implementation technology that is amenable to on-board applications. It will use SEASAT-A data as a tool for demonstrating the real-time processing of 4-look SAR data over a 20-kilometer swath to 25-meter resolution. Furthermore, the DMSP will provide the technical basis for the development of a 1982 Shuttle Imaging Radar (SIR-B) on-board image processor experiment. This paper describes the performance requirements and implementation architecture for the experimental SIR-B on-board processor.

II. Processing Constraints and Guidelines

Data System Description

A block diagram for the proposed SIR-B on-board SAR data handling system is provided in Figure 1. Referring to Figure 1, three radar data channels (two X-band and one C-band) will be simultaneously accommodated. Therefore, a SAR data interface unit capable of preprocessing all three channels simultaneously must be provided to prepare data for tape storage. Due to the large volume of required data, high density tape (HDT) recording is required. It is also noted from Figure 1 that a real-time image processor, capable of processing SAR images from HDT tape formatted data for any radar channel, is also included onboard. As noted previously, this represents an experiment which is part of a current research and advanced development (R/AD) plan for real-time on-board SAR processing development.

Radar System Design Values

The assumed radar system design values applicable to establishing the necessary SAR processing design parameters are tabulated in Table 1 for both an X-band and a C-band radar. Referring to Table 1, it is noted that three operating modes for each radar are defined. These correspond to look angles of 15°, 47°, and 60°. For each look angle, it is assumed that one X-band radar (with dual polarized reception) and one C-band radar will be operational resulting in three data channels.

Certain radar parameters, such as transmitter frequency, have been selected as typical for the purpose of establishing and evaluating a design approach. The capability to accommodate moderate changes in these assumed values is being allowed for in developing the data system design approach. Other values in Table 1, such as range bandwidth and swath width, have been defined to optimize the processing implementation rather than what is theoretically possible. For instance, the range bandwidth is held constant for all modes so that only a single sampling frequency will be required. In like manner, the swath width is chosen in order that the number of required data samples is the same for each radar for any given operating mode.

Radar Processing Parameters

The processing design parameters for both the X-band and C-band radars for each of the aforementioned three operating modes are defined in Table 2. Referring to Table 2, the required resolution for the 47° and 60° modes is nominally 25 m; while, the nominal resolution requirement for the

*This paper presents the results of one phase of research carried out by the Jet Propulsion Laboratory, California Institute of Technology, under Contract No. NAS 7-100, sponsored by the National Aeronautics and Space Administration.

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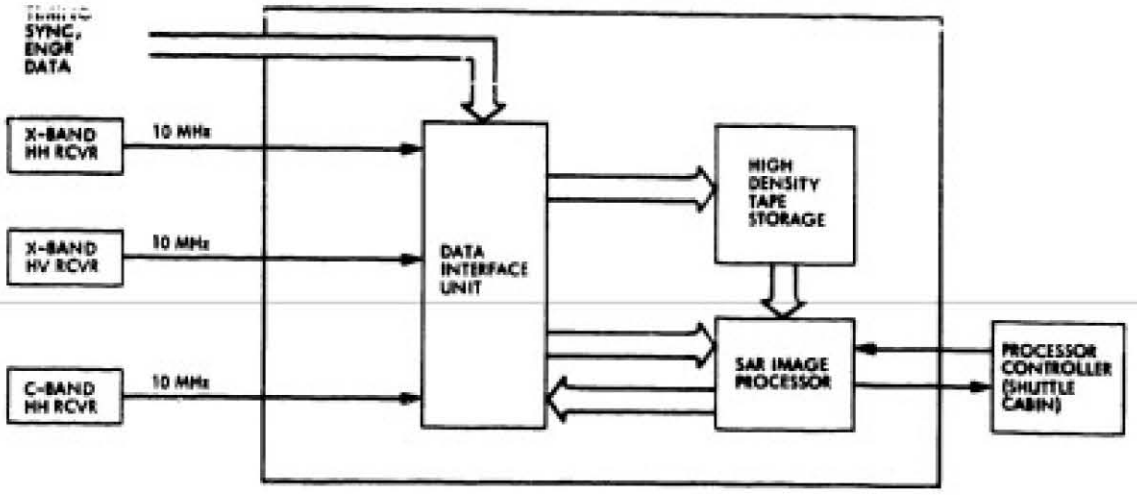


Figure 1. On-Board SAR Data Handling

15^{o} mode is only 75 m. The specific range and azimuth resolution numbers listed in Table 2 have been derived based upon implementation considerations. For instance, a single sampling frequency, constant bandwidth, and constant time-bandwidth product typify the range processing parameters for each radar. Also, the number of data samples required for each operating mode has been carefully selected for each radar to simplify the data handling implmentation. With respect to azimuth processing, the number of pulses per dump and the number of looks have been made equal for each operating mode. Furthermore, the number of looks is independent of the radar for any given mode. Therefore, a single processor implementation capable of accommodating any radar channel becomes feasible.

Data Rates

The raw and image data rates (RDR and IDR) per radar have been calculated and are tabulated in Table 3. In deriving the RDR values of Table 3, the number of bits per sample (N_{bit}) was assumed to be 5 bits. As noted, this results in a worst case RDR of 60 Mbps for the 60^{o} look angle operating mode. Although a 5-bit quantization level is being assumed for Seasat-A, it is probably not necessary for a 60^{o} look angle on SIR-B. In fact, analysis to date indicates that a 2-bit quantization level for the raw data at $\theta = 60^{o}$ is probably satisfactory. This could be a viable implementation trade-off for achieving a reduction in high density tape recorder system complexity (60 Mbps versus 24 Mbps).

III. A Processor Architecture

Block Diagram

A proposed block diagram for the on-board SAR image processor of Figure 1 is given in Figure 2. As noted from Figure 2, incoming data is routed through a processor interface unit which functionally separates the header data from the SAR video. The header data, containing the parametric engineering information required for computing the processing control functions, is routed to the microprocessor controller. The microprocessor controller computes the necessary corrections and effects control functions for all functional elements of the processor. The SAR video is first applied to a range processor for range correlation purposes. Following range correlation, the SAR video is applied to an azimuth processor. The azimuth processor performs the azimuth correlation function, range migration correction, and antenna beam pointing correction. The processed image data from the azimuth processor is also passed through the processor interface unit prior to being recorded or displayed. The image data is combined with appropriate header data from the microprocessor controller on a line-by-line basis so that it can be properly identified and evaluated.

Range Processor

A candidate implementation for the range processor of Figure 2 is shown in Figure 3. Referring to Figure 3, the range processor is seen to consist of three functional blocks. The input unit receives the incoming HDT formatted data stream and conditions it for application to the range correlator block. Following range correlation, the data is properly formatted by the output unit for application to the azimuth processor of Figure 2.

A proposed block diagram for the range processor input unit is provided in Figure 4. Referring to Figure 4, the incoming raw SAR video digital data stream from the processor interface unit is applied to a digital-to-analog converter (DAC) for conversion to analog voltage samples. Following digital-to-analog conversion, the analog samples for a given range line or echo are loaded into a range line buffer through an input multiplexer. The samples for the next echo are then multiplexed into a second line buffer. Each subsequent range line is stored in a different buffer until seven range line buffers are filled. The samples for the seventh echo following the original given echo are then stored in the first buffer and the cycle repeats.

A candidate implementation approach for a line buffer of Figure 4 is described in Figure 5. Referring to Table 2, up to 6,000 samples may be taken per echo under worst case conditions. Therefore, each line buffer must be capable of storing up to 6,000 samples. This could be accommodated by sequentially loading six 1000-stage CCD sampler chips.

The purpose of the parallel line buffers of Figure 4 is to reduce the rate that range line samples are clocked to the range correlator. It is noted from Figure 6 that the available readout time for

Table 1. Radar System Design Values

Design Parameter		X-Band			C-Band		
		$\theta = 15^\circ$	$\theta = 47^\circ$	$\theta = 60^\circ$	$\theta = 15^\circ$	$\theta = 47^\circ$	$\theta = 60^\circ$
Transmitter frequency	f	9100 MHz	9100 MHz	9100 MHz	4750 MHz	4750 MHz	4750 MHz
Radar Wavelength	λ	0.0329 m	0.0329 m	0.0329 m	0.0631 m	0.0631 m	0.0631 m
Pulse Repetition Frequency	PRF	2000 Hz	2000 Hz	2000 Hz	2000 Hz	2000 Hz	2000 Hz
Interpulse Period	IPP	500 μsec	500 μsec	500 μsec	500 μsec	500 μsec	500 μsec
Spacecraft Velocity	V	7.77 km/s	7.77 km/s	7.77 km/s	7.77 km/s	7.77 km/s	7.77 km/s
Altitude	H	225 km	225 km	225 km	225 km	225 km	225 km
Angle of Incidence	θ_i	15°	49.2°	63°	15°	49.2°	63°
Range	R	233 km	338 km	478 km	233 km	338 km	478 km
Sampled Swath Width (as opposed to 3 dB Antenna Swath)	SW	42.6 km	30.4 km	51.8 km	63.7 km	22.5 km	45 km
Antenna Width	W	0.15 m	0.6 m	0.6 m	0.3 m	1.2 m	1.2 m
Range Beamwidth	Ω_r	12.56°	3.14°	3.14°	12.04°	3.01°	3.01°
Range Pulsewidth	T_r	1 μsec	1 μsec	1 μsec	33 μsec	33 μsec	33 μsec
Range Bandwidth	Δf_r	10 MHz	10 MHz	10 MHz	10 MHz	10 MHz	10 MHz
Antenna Length	L	8.0 m	8.0 m	8.0 m	8.0 m	8.0 m	8.0 m
Azimuth Beamwidth	Ω_a	0.235°	0.235°	0.235°	0.452°	0.452°	0.452°
Time in Beam	T_{beam}	0.123 sec	0.179 sec	0.253 sec	0.236 sec	0.343 sec	0.485 sec
Azimuth Bandwidth	Δf_a	1942 Hz	1942 Hz	1942 Hz	1942 Hz	1942 Hz	1942 Hz
Oversample Factor	f_{os}	1.2	1.2	1.2	1.2	1.2	1.2

each line buffer is six times greater than the time required to read the data in. Therefore, the output sample rate from each line buffer is 1/6 of the input sample rate. By selectively multiplexing at the output of the seven line buffers, six output lines, each providing a continuous readout of different range lines at 1/6 the range line input rate, result.

The need for the range line sample rate reduction becomes apparent when one considers the worst case input data rate and the proposed range correlator implementation approach. Offering a potential savings of several orders of magnitude in cost, power, and implementation complexity compared with conventional digital LSI, analog CCD transversal filtering techniques are proposed for the range correlator implementation. However, such CCD filter devices are currently limited to input clock rates of less than 5 MHz. Referring to Table 3, it is noted that a worst case time expanded sample rate of 12 msps occurs for the 60° look angle operating mode. Therefore, in order to use CCD transversal filters for range correlation, it is necessary to significantly reduce this rate. By employing the buffering technique of Figure 4, complete range lines can be read from each of six lines to separate correlators at individual worst case clock rates of 2 msps. This rate allows existing CCD transversal filter device technology to be used for the range correlator implementation.

A candidate range correlator implementation is illustrated in Figure 7. As noted from Figure 7, the six outputs from the range processor input unit are applied to six corresponding range filters. As indicated in Figure 6, each range line filter performs the range compression function for every sixth range line. By using six identical filters, all of the incoming range lines are fully correlated in range. An additional feature of each filter of Figure 7 is the conversion from range offset to I/Q data. In other words, the range filters can perform complex range correlation from range offset input data and yet provide the real (I) and quadrature (Q) output components required for the subsequent azimuth processing.

Since the X-band and C-band radars described in Table 1 have different range time-bandwidth products, the number of points to be compressed in range differ. It is noted from Table 2 that the X-band radar requires correlation over 16 points; while, the C-band radar requires a 400-point correlation. A possible design for the X-band and

Table 2. Radar Processing Parameters

Processing Parameter		X-Band			C-Band		
		$\theta = 15^\circ$	$\theta = 47^\circ$	$\theta = 60^\circ$	$\theta = 15^\circ$	$\theta = 47^\circ$	$\theta = 60^\circ$
Range Resolution	ρ_r	69.5 m	24.6 m	20.8 m	69.5 m	24.6 m	20.8 m
Range Time-Bandwidth Product	TB_r	10	10	10	330	330	330
Range Compression Ratio	RCR	16	16	16	400	400	400
Sampling Rate	SR	24 msps	24 msps	24 msps	24 msps	24 msps	24 msps
Samples per Echo	N_s	1500	3000	6000	3000	3000	6000
Sampling Window	T_s	62.5 μsec	125 μsec	250 μsec	125 μsec	125 μsec	250 μsec
Pulses Coherently Integrated	N_{coh}	15	70	100	30	135	190
Coherent Integration Time	T_{coh}	0.0075 sec	0.035 sec	0.050 sec	0.015 sec	0.0675 sec	0.095 sec
Azimuth Resolution	ρ_a	79.0 m	24.5 m	24.3 m	75.7 m	24.4 m	24.6 m
Pulses per Data Dump	N_{dump}	15	5	5	15	5	5
Time per Data Dump	T_{dump}	0.0075 sec	0.0025 sec	0.0025 sec	0.0075 sec	0.0025 sec	0.0025 sec
Distance per Data Dump	Δ_{dump}	58.3 m	19.45 m	19.45 m	58.3 m	19.45 m	19.45 m
Pulses in Beamwidth	N_{total}	246	358	506	472	686	970
Looks	N_{look}	15	5	5	15	5	5
Filter Channels Per Look	N_{chan}	1	14	20	2	27	38

Table 3. Data Rates

θ	X-Band		C-Band	
	RDR	IDR	RDR	IDR
15°	15 mbps	782 kbps	30 mbps	1.17 mbps
47°	30 mbps	4.75 mbps	30 mbps	3.52 mbps
60°	60 mbps	9.55 mbps	60 mbps	8.31 mbps

C-band range correlators is shown in Figure 8. By using two transversal filters, each of a length twice the required range compression ratio (RCR), complex correlation plus conversion to I and Q components can be effected. This results in two 32-stage transversal filters for the X-band signal and two 800-stage transversal filters for the C-band signal.

Since the proposed radar transmitters will employ a fixed digital PN reference function, the filters of Figure 8 do not have to be programmable. Therefore, existing analog CCD fixed-tap weighted transversal filter chip designs may be used to perform the required correlation process. This enables a reduction in the number of components required to implement the range correlator by several orders of magnitude when compared with a digital large-scale-integration (LSI) approach.

The interleaved I and Q samples from each of the six range correlator channels are applied to the output unit of Figure 9. Each of six range correlator input multiplexers of Figure 9 selects 1/6 of the total samples from each range line sequentially across all six input channels. Referring to Figure 6, the output of each input multiplexer can therefore provide a continuous flow of sequential range lines representing 1/6 of the total radar system swath width. For instance, if a total swath were 6,000 samples, each input multiplexer of Figure 9 would be outputting sequential range lines corresponding to a designated 1,000 samples of the swath. By employing appropriate gating, each output line of the output unit would correspond to a different 1,000 sample section of the total swath. These output lines are then routed to six separate azimuth processor modules. By accomplishing parallel processing of sections of the total swath, the individual input data rate to each azimuth processor module may be adequately reduced to allow the use of existing CCD implementation technology. For the worst case data rate of 12 msps for the X-band 60° look angle mode, the output rate to each azimuth processor channel would be reduced to less than 2 msps.

Azimuth Processor

A candidate implementation for the azimuth processor of Figure 2 is shown in Figure 10. Referring to Figure 10, six identical azimuth processor modules are used to process each 1/6 section of the total range swath. An output buffer is then used to recombine the individual swath segments into image range lines covering the full swath width. As noted from Figure 11, each azimuth processor module consists of four functional blocks, i.e., a presum filter, an azimuth delay compensator, an azimuth correlator, and a digital magnituder.

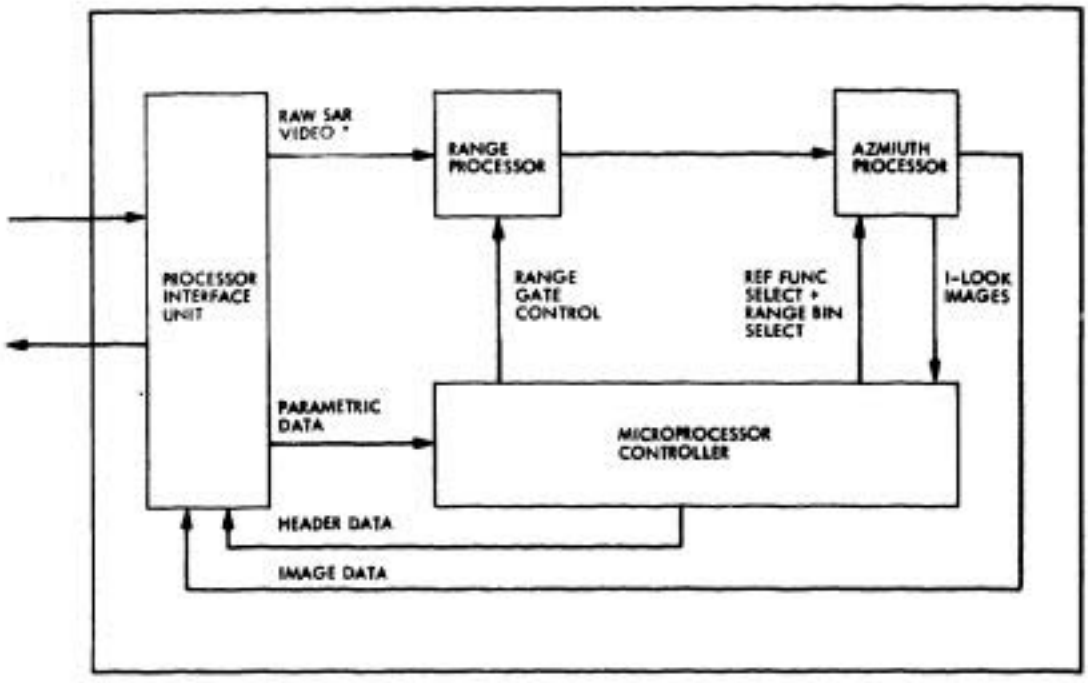


Figure 2. On-board SAR Image Processor

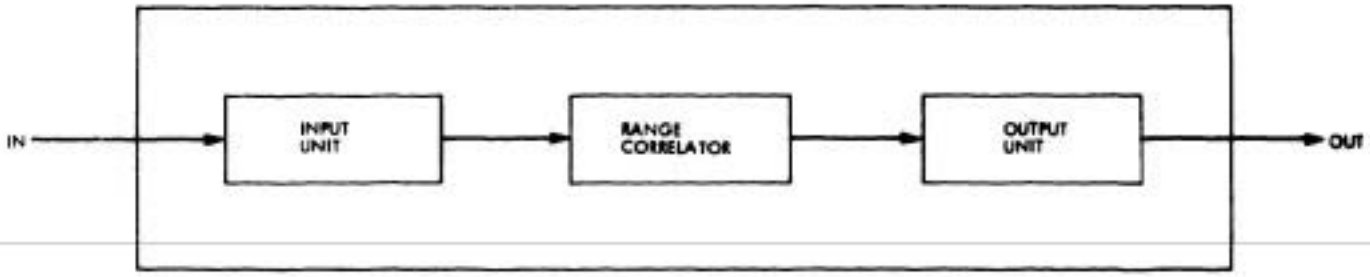


Figure 3. Range Processor

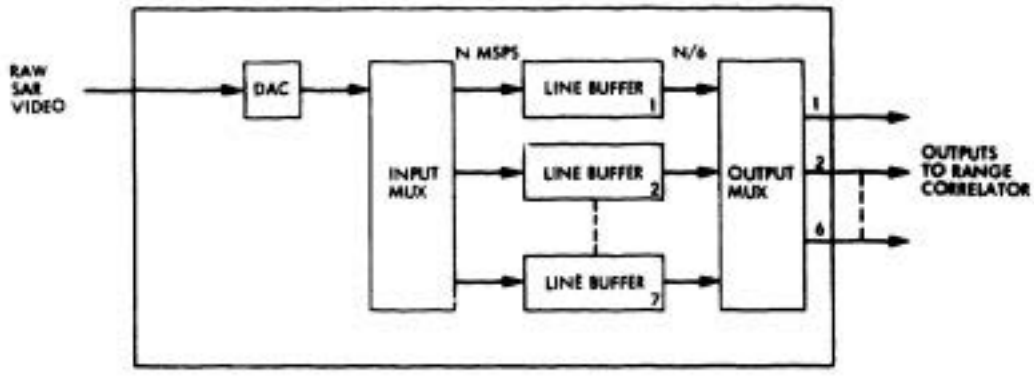


Figure 4. Range Processor Input Unit

The azimuth processor design approach of Figure 10 is characterized by a two-step filtering implementation. The initial filter, designated the presum filter, divides the azimuth spectrum into five parts or channels. Since the total azimuth bandwidth is capable of providing 5-meter resolution, 25-meter resolution imagery may be derived from each channel of the spectrum. Furthermore, only one-fifth of the bandwidth of each channel is really required to achieve the 25-meter resolution due to oversampling. Therefore, if each channel were properly filtered, the output data rate to the azimuth correlator of Figure 10 could be reduced by a factor of 5. Potentially, such presum filtering would provide an 80 percent reduction in the azimuth correlator power requirements.

A detailed block diagram for a possible presum filter design is provided in Figure 11. Referring to Figure 11, the interleaved I and Q samples from one of the range processor output channels are applied to a CCD range bin interpolator chip where repositioning and resampling of data within a range bin can be accomplished to precisely fit a given range migration correction curve, if necessary. A candidate design for an interpolator chip capable

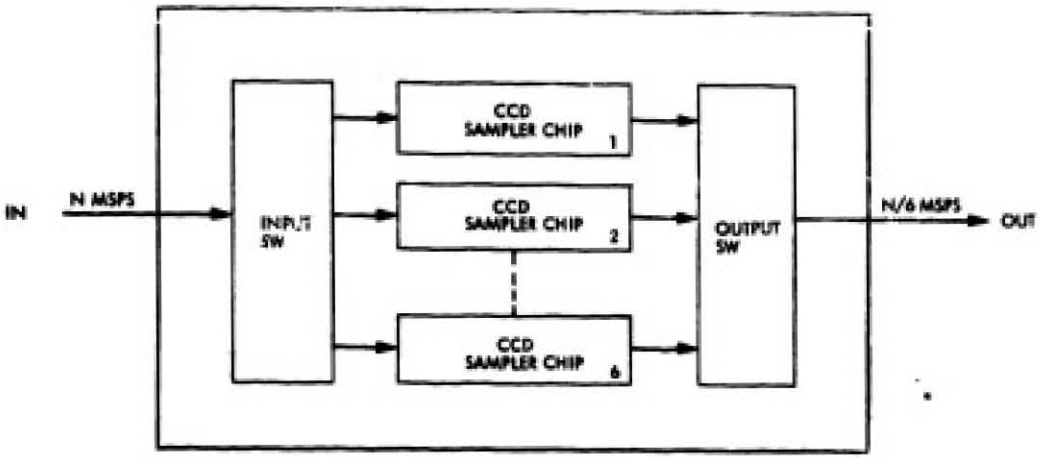


Figure 5. Line Buffer Block Diagram

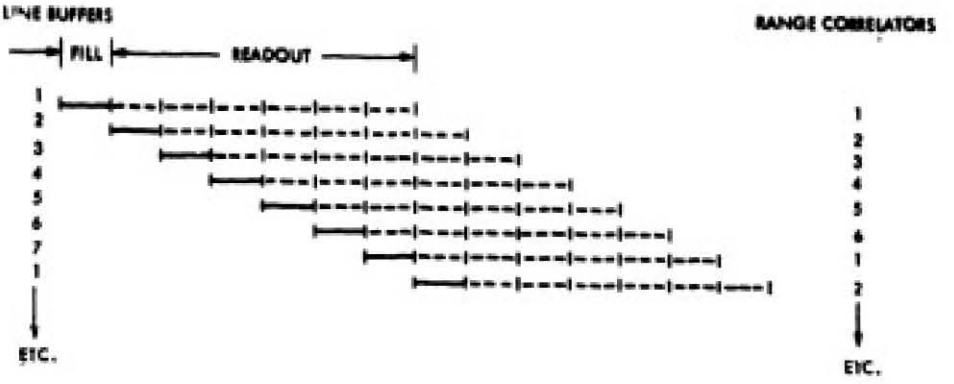


Figure 6. Range Correlator Line Sequencing Format

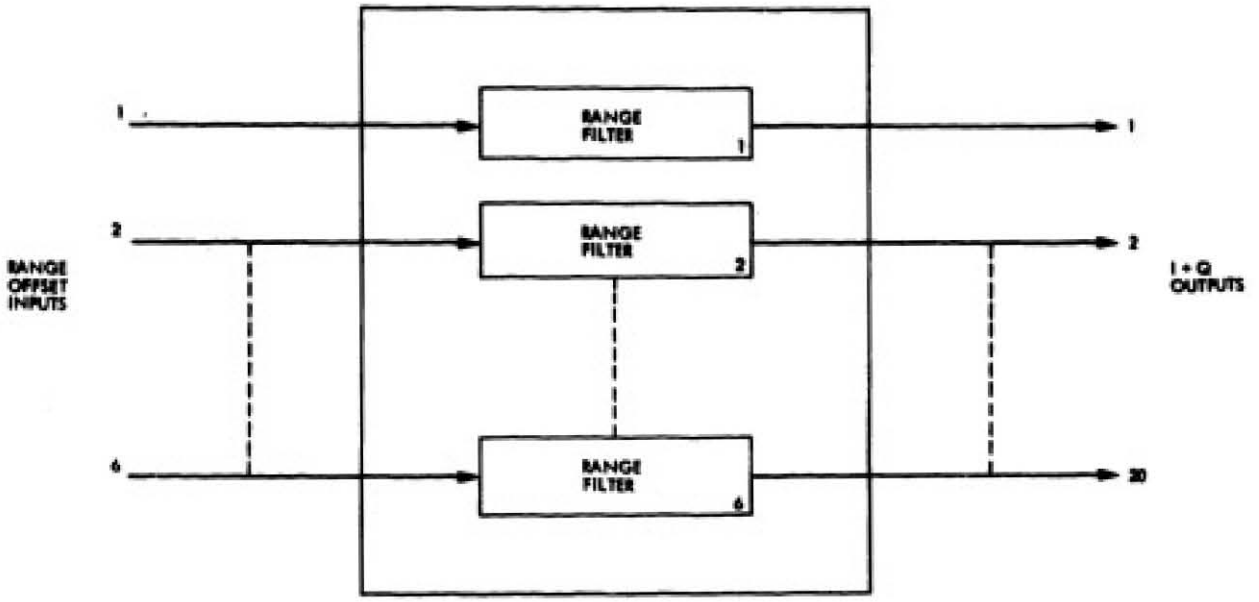


Figure 7. Range Correlator

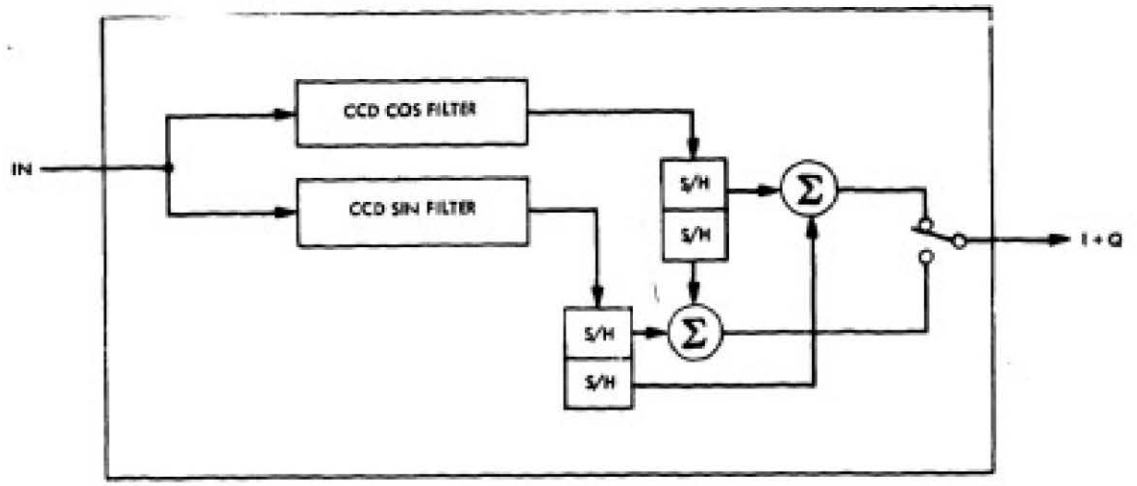


Figure 8. Range Filter Block Diagram

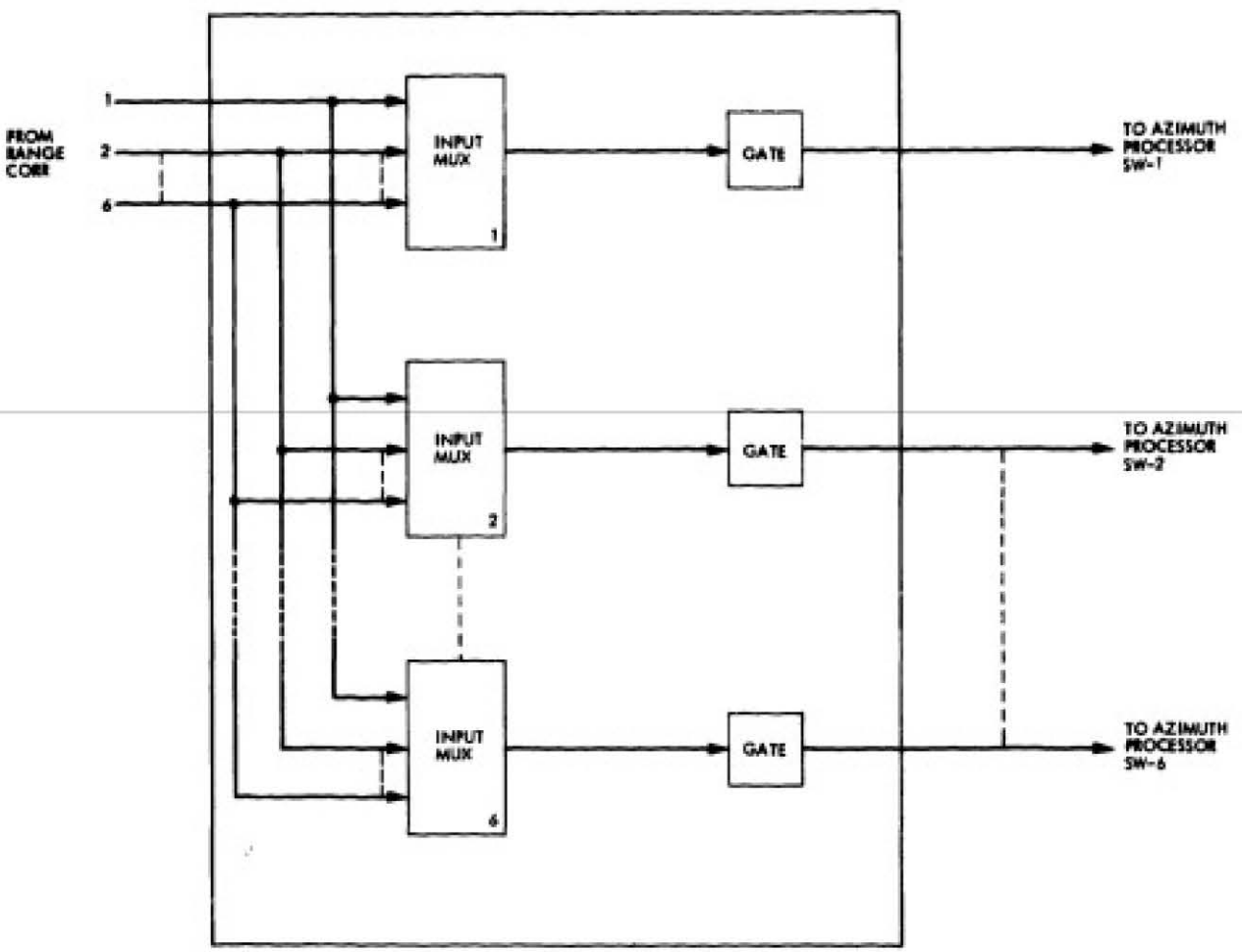


Figure 9. Range Processor Output Unit

of providing M = 32, N = 4 interpolation within a range bin would consist of four fixed-tap weighted CCD transversal filters providing convolution of the incoming video with an appropriate phase of a six x/x reference function. (M refers to the number of samples involved in the interpolation calculation and N is the factor of increase in effective sampling frequency after interpolating.)

Following interpolation, the data is applied simultaneously to three CCD azimuth filter chips. A functional description of the CCD azimuth filter chip is provided in Figure 12. Referring to Figure 12, each such chip independently achieves (1) range migration correction by placing each incoming range interpolated sample in the proper range bin, (2) convolution with the proper filter weighting function, and (3) accumulation of filtered range line information over the desired portion of the azimuth beam. For the presum filtering operation, if filtering were accomplished over 15 range lines in azimuth, then each chip would accumulate 15 weighted lines prior to readout. The presum filter for each channel, being implemented with only three

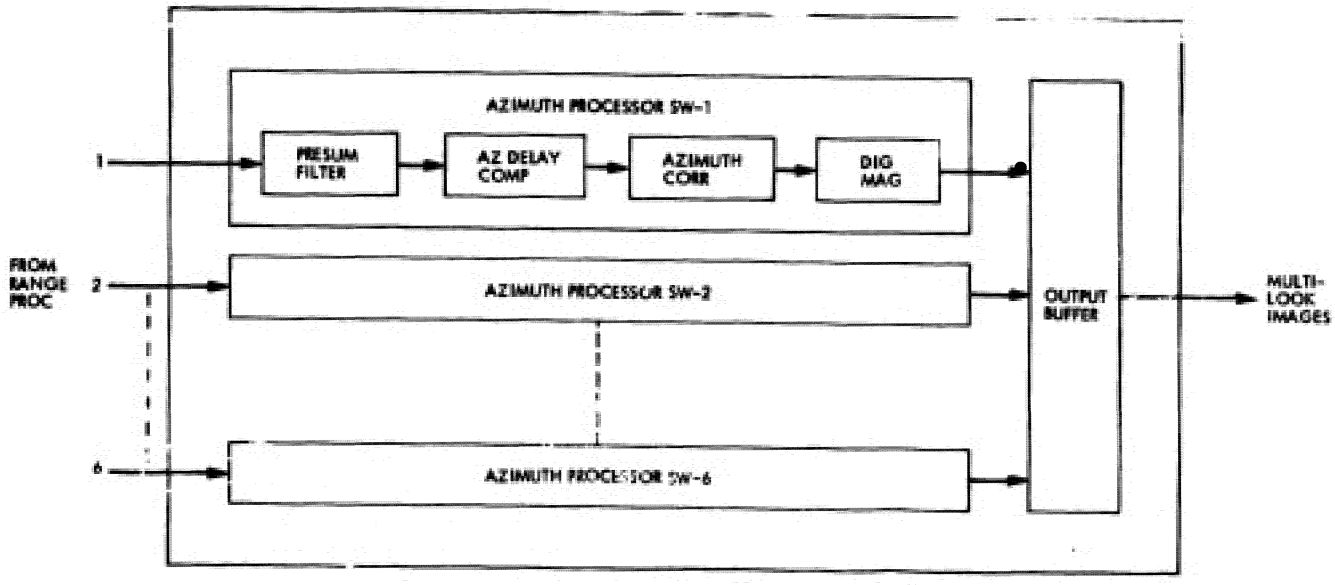


Figure 10. Azimuth Processor

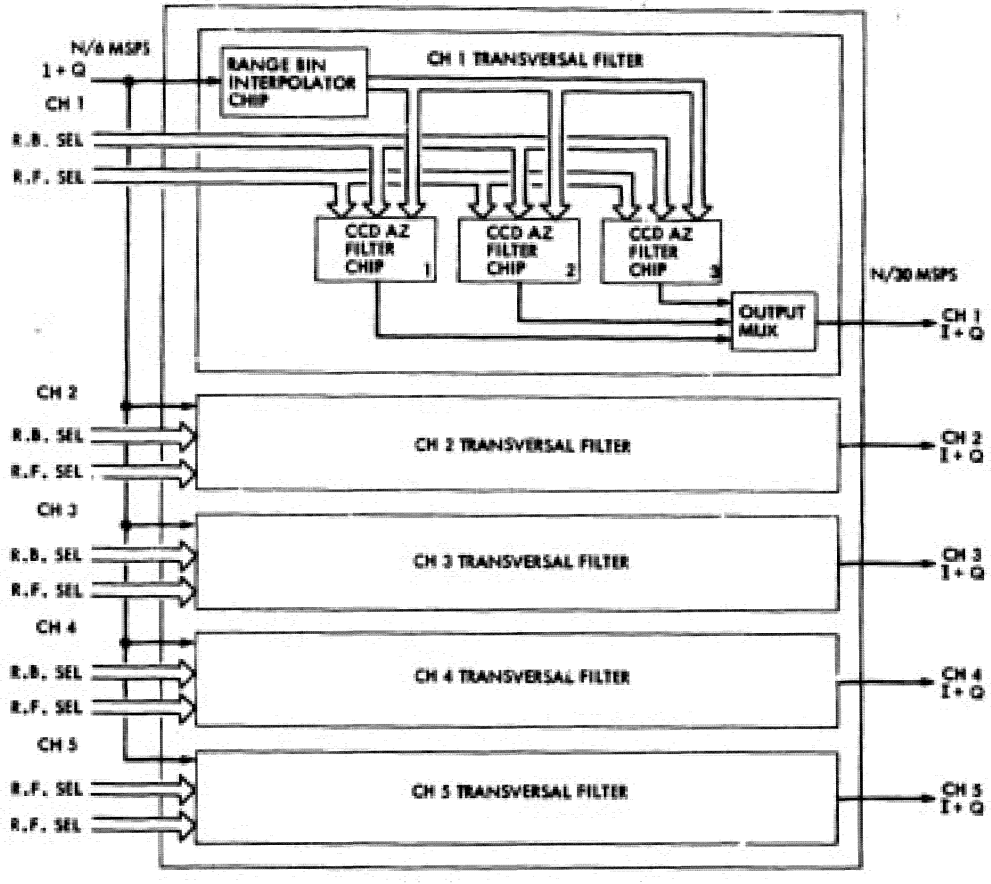


Figure 11. Presur Filter

CCD chips, provides a 5:1 reduction in channel data rate.

It should be noted that each presum filter channel is only capable of providing information to the azimuth correlator to achieve a single-look image. Therefore, five channels are required to produce 5-look images. This will not change the total number of filters required to achieve 5-look imagery from a single channel design using no presum filtering.

Since multiple-look images are being achieved by processing five single-look images from five sections of the azimuth spectrum, the problem of proper registration must be addressed. In order to combine the five single-look images into a single 5-look image, appropriate delay lines must be implemented. Each single-look channel must be phase compensated by an appropriate number of range lines with respect to its adjacent single-look channel. This delay compensation may be achieved prior to or after azimuth correlation and

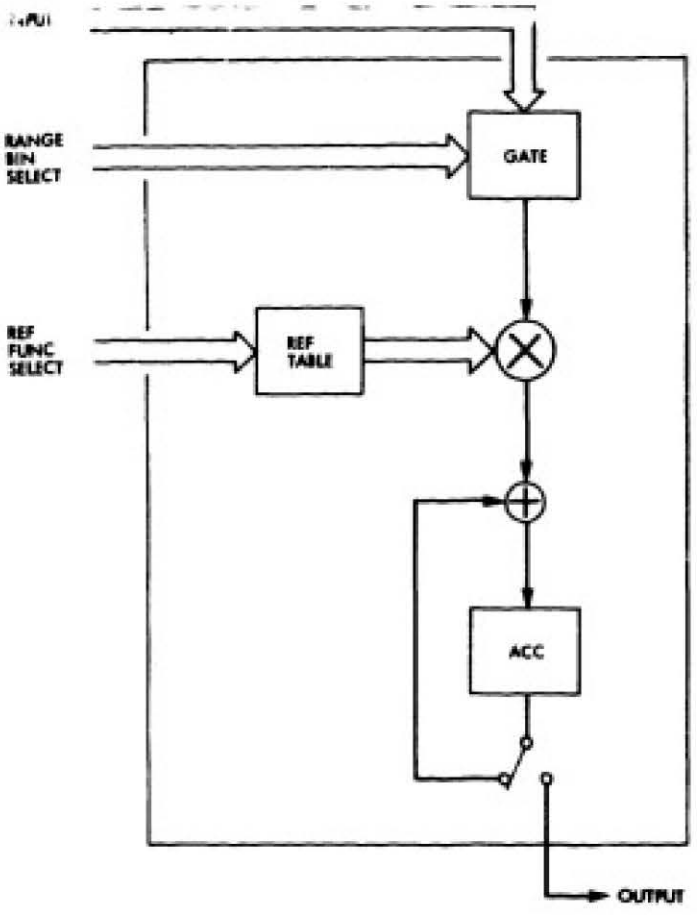


Figure 12. CCD Azimuth Filter Chip

digital magnituding using CCD SPS memory techniques. The only advantage to pre-filter compensation before digital magnituding would be if it were achieved in the analog domain. If such compensation is achieved following azimuth correlation and digital magnituding, the delay line memory requirements are increased by a factor of 4. Although the I and Q samples are combined into pixels providing a factor of two savings, the assumed requirement for 8-bit pixel quantization imposes a factor of eight increase in memory requirements. In addition to achieving a reduction in memory requirements, the use of analog CCD SPS memory compensation techniques prior to azimuth correlation could also provide a potentially significant reduction in power requirements compared with digital delay compensation following azimuth correlation.

The output from each channel of the azimuth delay compensator is applied to a corresponding transversal filter in the azimuth correlator for convolution with the appropriate doppler chirp reference function. The proposed architecture of the azimuth correlator is illustrated in the block diagram of Figure 13. As noted from Figure 13, the architecture of the azimuth correlator is virtually identical to that for the previously described presum filter. The incoming range line samples are first passed through a CCD range interpolator chip. The range interpolator outputs are then applied in parallel to each of N_{chan} CCD azimuth filter chips as defined in Figure 12. The number of required channels, N_{chan}, is defined for each radar operating mode in Table 2. As noted from Figure 13 and Table 2, the system implementation provides 38 filter chips per look in order to accommodate the worst case operating mode occurring for the C-band radar at a 60° look angle. Referring to

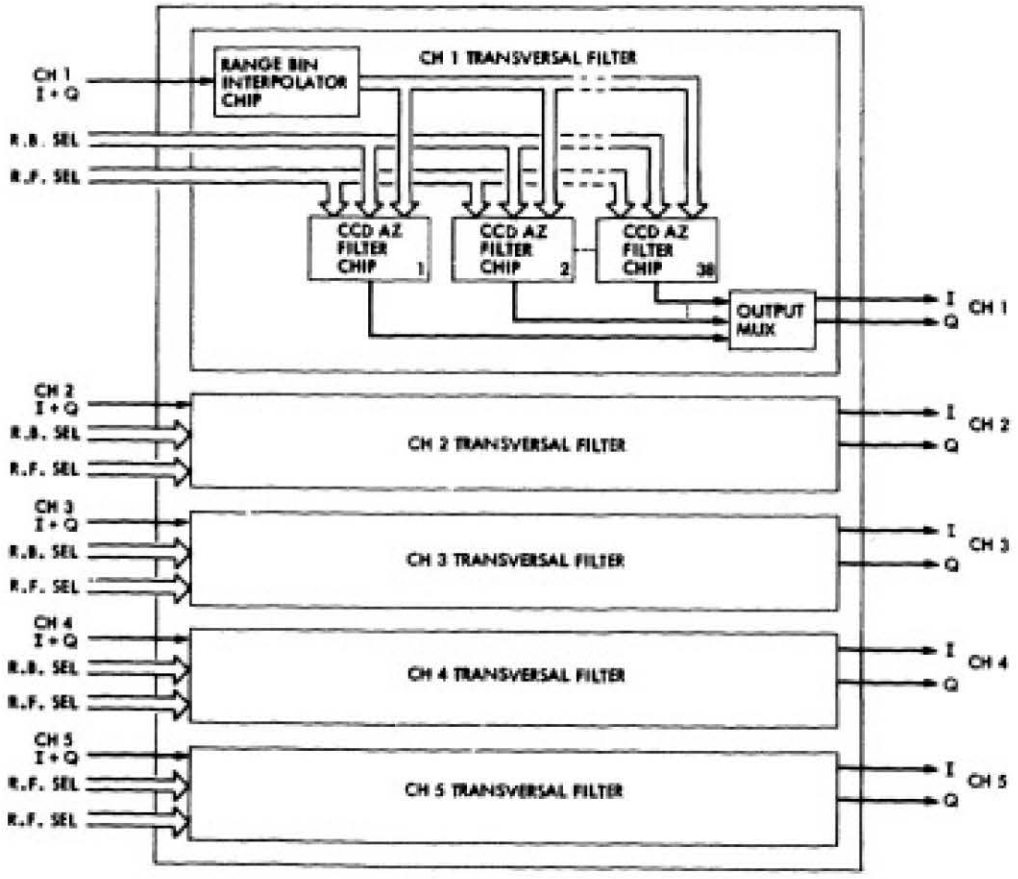


Figure 13. Azimuth Correlator

Figure 12, range migration correction is achieved on each CCD [illegible] chip for [illegible] incoming range line by (1) selecting the desired range interpolator output and (2) gating the desired range line samples to a complex multiplier. Using the complex multiplier, each corrected range line is convolved with the desired azimuth chirp reference. The doppler reference function can be reprogrammed, as necessary, from the microprocessor controller of Figure 2. Following complex multiplication, the I and Q samples for each such range line are temporarily stored in an accumulator register. Following N_{chan} such accumulations on a given chip corresponding to the transfer of N_{chan} range lines, an accumulator register will contain the I and Q samples of correlated image data. At this point, the I and Q image data is read out for digital magnituding purposes. By multiplexing between chips on a line-by-line basis, a continuous real-time data flow is achieved. Referring to Figure 13, each single-look channel provides both an I and a Q output line.

The I and Q output data from the azimuth correlator of Figure 13 is applied to a digital magnituder for pixel formation. A possible implementation for the digital magnituder is defined in Figure 14. Referring to Figure 14, the I and Q samples from each single-look channel are sequentially multiplexed into a common output line. The resultant interleaved I and Q samples are then digitized forming 16-bit address words (an 8-bit I word plus an 8-bit Q word). Each such address word is then used to derive already computed and stored $I^2 + Q^2$ pixel values from a programmable read only memory (PROM) look-up table. As noted from Figure 14, channel 1 will produce a single 8-bit word corresponding to a single-look pixel from the multiplexed I and Q lines. Before the subsequent I and Q samples from channel 1 are interrogated, the corresponding I and Q lines are sequentially sampled for channels 2, 3, 4, and 5. In this process, five 8-bit words, each corresponding to a pixel for a different look are sequenced, [illegible]. Two 8-bit registers are used as shown in Figure 14 to combine and buffer corresponding pixels from five single-look images into one 5-look pixel. Repetitive multiplexing of the five input channels produces a continuous stream of 5-look image pixels. If single-look image pixels are desired, they may be accessed at the output of the PROM look-up table prior to pixel superposition.

As noted from Table 2 for the 15° look angle operating mode, 15 looks can be achieved from the available azimuth bandwidth for the specified resolution. For that mode, every three consecutive 5-look image pixels from the 8-bit output register correspond to independent looks from three different portions of the azimuth spectrum. Therefore, additional azimuth delay compensation and multi-look superposition circuitry must be provided to produce the 15-look pixels. As noted in Figure 14, two existing 8 x 1000 digital CCD SPS chips are adequate to provide the necessary delay compensation to produce the 15-look pixels.

Referring to Figure 10, an output buffer receives an image line covering a different 1/6 of the total swath from each of six identical azimuth processor modules and combines them into image lines covering the full range swath. A block diagram for a possible output buffer implementation is defined in Figure 15. As noted from Figure 15, each 1/6 swath increment is read into a buffer memory consisting of an existing 8 x 1000 digital CCD SPS chip identical to that defined for delay compensation in the digital magnituder of Figure 14. During one interpulse period, each buffer chip is loaded with that portion of the total swath corresponding to its designated channel. While each 8-bit pixel word is read into each buffer chip, a word stored from the

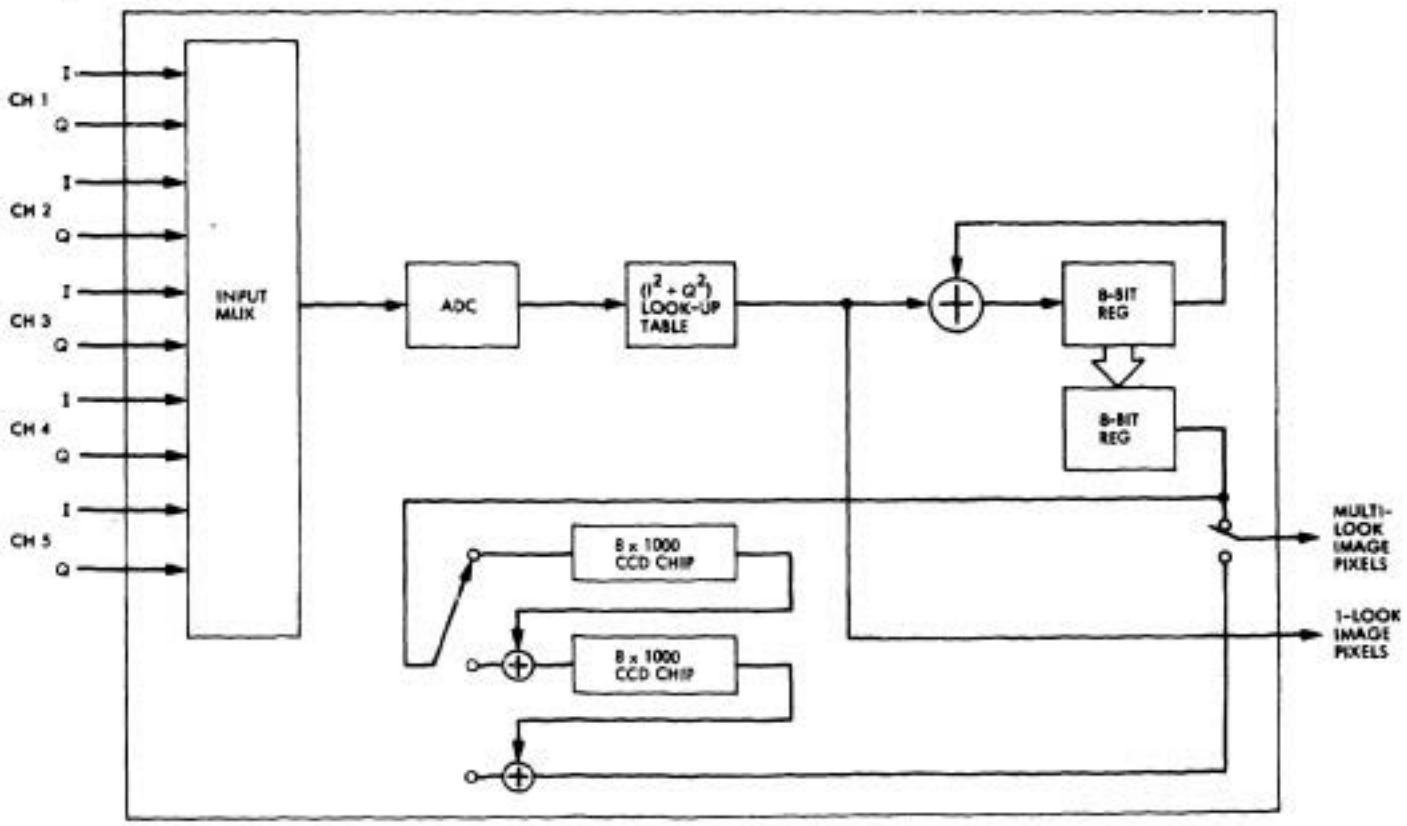


Figure 14. Digital Magnituder

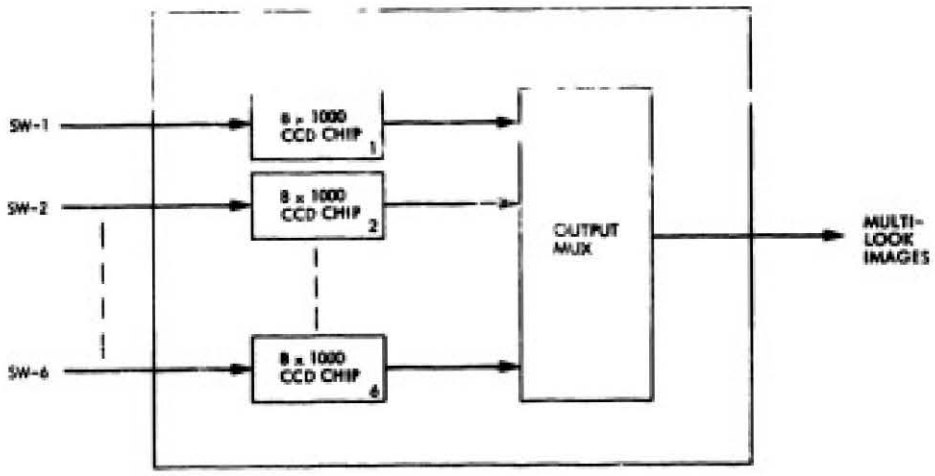


Figure 15. Output Buffer

previous interpulse period is read out. However, the readout is accomplished sequentially across the five channels at six times the per channel input rate. Therefore, a continuous stream of bits corresponding to a full image line covering the full range swath is outputted each interpulse period. The output multiplexer of Figure 15 is used to sequentially switch between buffer chips.

IV. Conclusions

A promising candidate implementation architecture for the SIR-B on-board SAR image processor experiment has been defined. The salient characteristic of the proposed architecture is a real-time, programmable processing capability.

The azimuth processor implementation architecture is especially unique in that it readily accomplishes both linear and quadratic range migration correction with nothing more than a logic-controlled gating operation. Furthermore, it can accommodate a high degree of interpolation capability if required. In addition, the need for a corner-turning memory is eliminated, thereby simplifying the memory organization requirements. Finally, it appears very amenable to a custom chip implementation wherein changes in mission requirements may be easily accommodated by simply adding or deleting identical chips from a modular configuration.

Low cost and power characteristics are also possible with the proposed implementation. This can be achieved in (1) the range processor by using analog CCD transversal filtering techniques, (2) the azimuth processor by employing a two-stage, time domain filtering architecture implemented with a programmable custom CCD filter chip, and (3) the controller by employing advanced digital LSI microprocessor chips for control of the overall on-board image processor experiment.

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