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TESTING EMBEDDED MICROPROCESSORS - SPACE APPLICATION REQUIREMENTS

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Abstract

Microprocessors are finding increased application in space systems as components, replacements, and as more sophisticated computational subsystems. Some of these applications require the development of new LSI circuits and technologies and some require the adaptation of commercially available devices.

Usage for military space requires special tests to verify that they meet Space Standard Requirements, and these special tests may require specific hardware/software configurations.

This paper describes the methodology and testing requirements to standardize the parts, the tests required at the part and system level, when to test as a component or embedded system, and some of the current activities and issues in the test and utilization of microprocessors.

I. Introduction

Progress in the development and application of microprocessors (μPs) has been both rapid and spectacular. These devices are finding increased application in satellite, space communication and space sensor systems. These space-based systems require extensive testing at the part, subsystem and system level, because of the very high cost of mission failure.

Test philosophy and procedures have been well established in the form of military standards, specifications, regulations, procedures, and guidelines. μPs, because of their complexity, because they are new devices, and because they have characteristics of both a component and a system, have raised the question as to whether existing test procedures are acceptable. In general, the answer is yes, but updating of existing procedures may be required. All standards and procedures are under review to insure their applicability to μPs and detailed specification and test procedures are being formulated for the various LSI devices.

The Microprocessor as a New Nonstandard Device

Incorporation of new technologies and circuits in space applications is a common occurrence. In fact, MIL-STD-749B[1] establishes the procedures for approval of nonstandard parts prior to use in military equipment. The terms "standard" and "nonstandard" parts are defined in the governing equipment specification or contract. For military space applications, standard microelectronic parts are those that have been obtained with the criteria and guidelines of SAMSO-STD 73-2C.[2] This standard establishes the standard control program for electronic part utilization in equipment used in space. For microelectronics, this standard imposes MIL-M-0038510, Class S,[3] the "General Specification for Microcircuits" and its associated MIL-STD-883, "Test Methods and Procedures for Microcircuits."

The Microprocessor as a Standard Part

Considerable effort is presently underway to qualify μPs in accordance with MIL-M-0038510 and MIL-STD-883. Specific activities in μP space qualification are discussed in Section II. As standard devices, we can expect increased applications of μPs particularly in embedded configurations, which will require special attention to test requirements for acceptance, pre-launch, and on-orbit operations.

Embedded Systems Applications

AFR 800-14[5] entitled, "Management of Computer Resources in Systems" has provided both policy and guidelines for computer requirements and software procurements for Space Applications. However, μPs are being used as simple logic components in some systems and as a result the applicability of AFR 800-14 must be evaluated. Section III covers the considerations of μP as a part and as a system, and also the pre-launch testing activities. Test vector generation and test equipment considerations are also covered in this section.

Distributed Embedded Systems for Fault Tolerance

Space applications, by and large, are for long life missions, much greater than one year. The ability to test μPs embedded in systems and while on-orbit is being investigated. Current practice is to perform functional or diagnostic tests. To achieve high reliability long duration missions, fault tolerant μP configurations are evolving. Fault tolerant systems require fault diagnosis capability and thus testing is a fundamental requirement. Fault tolerance concepts and their impact on μP design are covered in Section IV.

II. Microprocessor Qualification

A variety of μP families have become available over the last three years. These differ widely in complexity and performance characteristics. The technologies used for manufacturing μPs also vary widely; these include the following: PMOS, NMOS, CMOS, T^2L, I^2L and ECL.

Space applications have stringent reliability and qualification specifications to assure mission success. SAMSO-STD 73-2C provides a standard control program for parts to be used in missile and space applications. The purpose of the control program is to assure that uniform devices will be produced, to give uniform responses to (their) tests and/or screens. This Standard requires that microcircuits conforming to MIL-M-38510, JAN class A or with MIL-M-0038510, class S or equivalent be used.

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A microcircuit qualified to class A or to class S is required to be manufactured on a production line which has been audited by NASA or SAMSO/Aerospace and certified as conforming to NHB 5300.4(3C) "Line Certification Requirements for Microcircuits" (Class A) or MIL-STD-0038510 (USAF) "General Specification for Microcircuits" (Class S). These line certification specifications will be replaced by MIL-STD-976 "Military Standard Certification Requirements for JAN Microcircuits" in the near future. Qualified microcircuits also meet the qualification requirements of MIL-STD-883, METHOD 5005 "Qualification and Quality Conformance Procedures". However, prior to qualification, a detailed specification (slash sheet) in accordance with MIL-M-38510 is prepared, coordinated and issued by the DESC (Defense Electronic Supply Center) at Dayton, Ohio. Each qualified microcircuit must conform to the electrical, mechanical and screening requirements of the detailed specification. It is, therefore, essential that all of the applicable tests for these requirements are included in the detailed specification. The device screening requirements for Class A parts are specified in MIL-STD-883, METHOD 5004, "Screening Procedures", however, these screening requirements may be modified by the detailed specification which takes precedence over the general specification.

If a part is to be used in a high reliability application and detailed specifications and/or military qualifications are not available, the part will be procured to the design, construction, qualification, screening, quality conformance, process control and failure analysis requirements equivalent to Class A or S. In this case, a contractor prepares a detailed drawing which contains all of the essential ingredients of a MIL-M-38510 slash sheet. This drawing is then approved by the appropriate procuring activity.

Much of the testing and qualification inspections are standard, these include: operating life tests for 1000 hours, hermetic package seal, temperature cycling, acceleration, etc. Functional testing is usually performed at ambient temperatures: -55°C, 25°C and 125°C to assure adequate operating margins and improved reliability as compared to room temperatures testing alone.

As discussed below, (Section III), complete μP functional testing of all possible combinations is not feasible; however, alternate approaches, such as use of: reliability test patterns and use of qualified technologies with associated CAD (Computer Aided Design), software and qualified standard cell libraries are under consideration. The Reliability test patterns contain all of the structures of devices and cells contained within the microcircuit; however, testing is facilitated by bringing out accessible contacts for test purposes.[5] The Defense Department is currently evaluating some of these alternatives[6] as well as use of custom LSIC designs.

Use of qualified technologies, etc., is not, at this time, a generally accepted approach to improved reliability and microcircuit qualification. However, with the proliferation of LSIC's (large scale integrated circuits) and the need for custom LSIC designs, qualified technologies may become viable for future procurements.

μP circuits can be designed with built-in test structures at the expense of additional logic and interconnects. To facilitate testing, there should be no non-accessible stored states, i.e. every state should be readable or writable, and it should be possible to always set all storage states to a known initial state by means of an external signal.

An additional feature which would facilitate functional testing is to design the μP in a regular matrix array such that data travels one way across the chip (e.g. horizontally) and with control signals vertical. This type of design permits more detailed functional testing and analysis, as each data bit is locatable at a given instant of time.[7]

Providing new μP designs is facilitated at the wafer level (prior to cutting up at the dice and packaging) by a technique known as microprobing. In this technique, very sharp electrical probes controlled by precision micromanipulators are used to contact the metallization directly within the microcircuit in order to pick up data signals or to measure voltage levels at various points in a circuit. This method is somewhat analagous to testing a breadboard circuit using hand probes; however, correcting errors in a microcircuit requires: a redesign, new photolithographic masks and production of testable wafers fabricated with the new masks. Microprobing is not usually possible to perform on previously packaged devices as all the metal intraconnects are covered by an insulating layer called "glassivation", which is required for Class A or Class S parts as a protective layer to prevent scratches and to help protect against internal shorts which may be caused by loose particles.

The traditional "shake, rattle, and roll" type of screening for microcircuits is not totally adequate to weed out all marginal devices. Emphasis today is being placed more on proper design and construction of microcircuits along with more inprocess inspection and use of controlled or monitored production lines. Military specifications are being upgraded to provide for these reliability improvements.

RADC (Rome Air Development Center) has the primary responsibility and is the preparing activity for MIL-M-38510. They are currently developing detailed specifications for a large variety of μPs.

Table 1 indicates the status of RADC development of detailed specifications for available, off the shelf, μPs.[8] When the μP numbers are followed by a "/", the number following the "/" is the MIL-M-38510 slash sheet number and indicates that these devices are in process of being qualified.

The μPs listed in Table 1 without slash numbers have not, as yet, started through the qualification cycle. Additional μPs will be added to the list as the military need develops for their use.

III. Ground Testing

The life cycle of space systems consists of five phases: a) conceptual, b) validation,

Table 1 Microprocessors by part number and technology

NMOS	PMOS	CMOS	ST^2L	LST^2L	I^2L	ECL
8080A/420	PPS-8	1802/470	3000	2901A/440	9900/460	10800
6800/400	PPS-16	6100	5701			
Z80			8X300			

c) engineering development, d) production, and e) deployment. A considerable number of systems incorporating μPs are now in the engineering development phase. μPs are being applied to attitude control systems, guidance sensors, signal processors, communications equipment, telemetry equipment, command and control equipment, and general purpose computers.

Changing Computer Resource Management

Computers (with the associated software) have been complex, expensive and critical components in the overall system. As a result, they have been treated as a Configuration Item (CI) where their specification, development, fabrication and test are carefully controlled. In particular, as a CI, the computer can be tested directly, with GSE (Ground Support Equipment) providing flexible stimulus operation and response monitoring.

Recent and near-term μP technology development will permit the μP-based computer to be embedded within other systems. Air Force Regulation 800-14, Volumes I and II [9, 10] provide guidelines for the planning, development, acquisition, support and test of computer resources embedded in systems.

Hardware costs and technical risk factors associated with μP applications, as compared with past aerospace computer developments, have been reduced considerably, and there is some question as to whether they should be treated as CIs. The answer to this question is not clear and will probably depend on the specific situation; if the μP is used as a universal logic element, or if it is used in a simple configuration where it can be tested conclusively, then it need not be treated as a CI. On the other hand, if the μP is embedded in an application that requires considerable supporting I/O, memory circuits along with extensive software development, it should be emphasized by treating it, still, as a CI. [9] In between these two extremes there will no doubt be a gray area which will need to be resolved by the procuring agency.

System Testing

Once μPs are incorporated into a system, they undergo development, qualification, acceptance, and pre-launch validation testing. MIL-STD 1540A (USAF), "Test Requirements for Space Vehicles", provides the general requirements for ground testing. Specific projects augment this specification as necessary. This specification defines the functional and environmental tests to be performed. Typical tests performed include functional, electrical, vibration, acceleration, shock, thermal-vacuum (altitude), temperature cycling, voltage-frequency margins, radiation, EMI, humidity, and burn-in. For each test performed, the following steps are included, a) identification of what must be tested, b) formulation of test cases and test set-up, c) execution of the tests, d) verification of results obtained.

Before (ground) system testing begins, however, a substantial amount of testing at the subsystem (computer) level has taken place. Embedded μPs have the potential of eliminating some of this testing, because the overall testing at the μP part level (which has evolved primarily from commercial considerations) provides a very high level of confidence in the μP as a part. The concentration on a small group of parts (the μPs) by a large number of users (testers) provides assurance of test quality at the device level. The question that remains to be answered is: Can μP based systems be built with well specified parts which will perform as intended, with only minimal testing at the subsystem level, which can then be installed for testing at the system's level, and can the system's operation be verified adequately for off-nominal and contingency conditions in addition to meeting the normal requirements?

μP-Based System Validation

Computer software programs have developed extensive verification and validation (V&V) procedures. This is because the combination of data bit states, instructions, I/O and interrupts have been so extensive that special tests are required to validate that there are no undesirable computational paths. The internal complexity of the μP, along with the unpredictable sequencing of the interrupts and of the instructions by the user, have resulted in problems similar to those faced in software development.

Some of the techniques used in software V&V (such as structured testing and independent testing) are finding application in μP testing. In some cases, a replica is being constructed, which will provide access as required for testing; the replica corresponds to the ICS (Interpretive Computer Simulation) used during software V&V.

The current approach is to make use of lower cost components to actually construct a replica of the hardware system to be tested. This permits an independent validation/verification of both the hardware and the operational software, and their interaction. Also, many facets that cannot be easily tested in the embedded configuration can be easily driven by appropriate software inputs.

Independent hardware/software validation will become more important as more sophisticated redundancy is designed into our systems.

Testers and Test Patterns

A major problem has been the greater complexity involved in formulating the test patterns required to validate the μP operation. On the system level, this problem is really not unique to μPs. Discrete/SSI/MSI implementations also required equivalent effort in formulating the tests, but the accessibility of internal test points (even though not accessed to any exhaustive degree), and the overdrive capability of the circuits, provided a more comfortable situation in the minds of many users.

Logistically it is easier to test one component type rather than several that would be involved in a discrete/SSI/MSI implementation, i.e., temperature, vibration, electrical and other tests need be done once rather than several times on the individual components. Also, microcomputer development systems are available that facilitate proper development and functional check-out.[12] In addition, automated test equipment has been developed that permits thorough functional, electrical and environmental testing.[12, 13]

μPs exhibit both soft and hard failures. Out of tolerance DC and AC measurements are used to ferret out such problems.[14] "Shmoo" plots are also made to verify proper response within a range of variables.[15] For example, V_{DD} and V_{BB} are varied over their limits and I_{DD} is measured to verify that it does not exceed a certain limit. For each μP, 20 to 30 Shmoo plots may be needed. Automated test equipment is needed to perform all these tests.

As has been pointed out previously, exhaustive testing of all combinations is impossible. For system level testing the concept of stress testing performed during qualification testing is invoked; that is, the electrical and environmental test levels are raised and lowered to levels exceeding those to be encountered in normal operation. The expectation is that any weak points in the design will show up during the qualification tests. Qualification testing is usually performed on a single unit or a few. Acceptance testing is performed using test levels equivalent to those expected to be encountered in operation and is performed on all units to be delivered.

An exhaustive test of a μP device would involve electrical and environmental testing of all combinations of the combinational and sequential states than can occur on the external and internal nodes of the device. Exhaustive testing not only tests for normal operation but checks for coupling effects between the various data paths, and active and passive elements. The number of combinations is the number two to some power. Just taking the number of instructions as N and the number of bits as M, the number of combinations C is $C = 2^{MN}$. For a μP with 8 data bits and 30 instructions, $C = 2^{240} = 1.7 \times 10^{72}$ --a very large number! If one assumes that each combination can be tested in one microsecond, it would require many thousands of centuries to test the device. Since each device is actually only tested for a few seconds to a few minutes, it can be seen that test coverage of the combinations is minuscule. But experience shows that reliability wise the devices work well in spite of the lack of exhaustive testing. The reason for this is that the devices are designed (by understanding and control of electrical, material, processing and geometry parameters) so that cross coupling effects are not extensive, and, therefore, testing all combinations is not necessary. The key effort in μP testing is to identify what combinations should be tested and to formulate test patterns, electrical and environmental tests to provide maximum test coverage with minimum test time. To a large extent, acceptable tests are obtained after several iterations.

Methods for testing μPs include a combination of, a) self testing, b) comparison testing, c) stored pattern testing, and d) algorithm aided pattern testing.[16, 17] All of these methods require that the internal blocks of the μP be identified and appropriate test patterns or test vectors be formulated. Each test vector in turn may involve several clock cycles. For example, checking a 65K program counter may require executing repeatedly a test vector (such as the "ADD" instruction test pattern) 65K times. Current μPs, depending on their complexity, require between 3,000 and 20,000 test vectors. It is estimated that a one man year of effort is required to design a good test.

Several LSI testers are available for testing μPs. These testers have the capability to apply test patterns and to monitor, record and analyze responses. These testers are costly, i.e., up to about $400,000, and, therefore, independent contract testing is commonly used. Some of the older testers are becoming capability limited for such reasons as inability to generate the proper timing and test patterns, or pin limitations.

IV. Operational Testing and Fault Tolerant μPs

The purpose of testing is to uncover failures. While in space, the normal functioning of a component provides the most practical means of checking its health status. Telemetry signals of key test points, along with mission data, allow the detection of any abnormal conditions. In some instances, diagnostics, self tests and command-response tests are executed to perform a more exhaustive checkout. If unacceptable performance is detected, redundant designs permit the turn-off of a failed system and the turn-on of a standby. In the past, standby redundancy with ground reconfiguration control has been used extensively with acceptable results.

During the past several years, fault tolerant computer designs have been investigated.[18, 19] Fault tolerant designs permit uninterrupted processing, even when failures have occurred. μPs, because of their low weight and power characteristics, are particularly attractive for fault tolerant designs. Fault tolerant designs require the ability to detect failures, and to invoke corrective actions. In a sense, the real time testing and failure detection capability performs continuous testing of the system, with the fault monitoring circuits serving as the test equipment.

In a fault tolerant configuration, the system must be able to detect all types of failure that can occur. Failures can result internal to the μP or from external sources such as faulty inputs, failed power supply and failed clock sources. Various techniques have been developed to detect and mask the various faults that can occur. The

basic operation of some of these techniques are described in the following paragraphs.

In order to detect internal μP faults, one technique used is to operate one μP as the active processor and a second as a monitor. Both processors operate independently and the results are compared continuously. If a discrepancy is indicated, an error signal is sent to a multiredundant reconfiguration unit which turns off one μP, turns on another. Each of the two μPs now active, roll back their program and re-execute the program. If a fault persists another pair of μPs is selected until the failure is circumvented. For long mission duration guidance applications, this technique has been found to be of particular interest, mainly because it can handle a series of single failures and it minimizes the number of spare μP modules required. There are other techniques that can be used, each with its own advantages and disadvantages.

Another technique, the "pair and spare" concept, utilizes three μPs, each performing the identical computations. The outputs from two of the μPs are sent to a comparator. If a failure occurs, the outputs from the third μP are used.

Another concept is to use two μPs and compare their outputs. If a failure occurs, both μPs are forced into a diagnostic mode, with the one which passes its diagnostic taking control of the outputs. This technique has slow recovery response time, but at lower hardware penalties.

A μP may indicate false outputs because it has received faulty inputs. The technique used to detect such failures is to encode the data and perform error detection and perhaps correction upon its receipt. The μP must also encode its outputs prior to its placement in the output bus. This is to allow the receiving unit to detect line failures.

Data, address and control buses are used extensively in μP-based systems. A short on any device coupled to the bus results in correlated faults in all devices using the bus. Redundant buses can be used to circumvent bus failures, but since buses consist of many lines, such as a 16 bit data bus, and since devices are pin limited, spare lines are used rather than complete redundant buses. This technique requires switching electronics to remove the faulty line and to replace it with a failure free line.

Voltage and frequency monitors are used to detect out of tolerance conditions and appropriate switching to unfailed units is performed.

Fault tolerant computers are being designed so that specific hardware and software faults can be injected into the system in order to check out the operation of the fault detectors and the reconfiguration units. Also, the circuits required for fault tolerance are designed to be testable. For example, a data encoder can be forced to place improperly coded data on the line so that the operation of the error detection decoder can be checked out.

Fault tolerant μP-based systems have been demonstrated. Viewing such systems, one is struck with the fact that the circuits required for fault tolerance such as for data comparison, voltage/data switching, data encoding, error detection and correction, and voltage frequency monitoring far outnumber the basic μP circuits. The reason for this is that these functions are now being performed by discrete and MSI circuits. Considerable parts count reduction can be achieved if many of the fault detection and correction circuits were built into the LSI, μP and other circuits. Some trend in this direction has been achieved in the commercial market. For example, an LSI device for a microcomputer already has ROM, RAM, I/O ports and a time out counter on a single die. A monolithic LSI analog voltage regulator device exists which in addition to its voltage switching, pulse width modulation and voltage regulation functions has an input that can switch off its outputs. All of these capabilities can be used to simplify considerably the design of fault tolerant systems. Military projects are also underway to design μP and LSI circuits suitable for high reliability fault tolerant systems. Considerable activity and progress is expected in the development of LSI devices with built-in fault tolerant capability.

V. Conclusions

Testing of μPs in space applications is continuing at an accelerated rate. The methodology for testing μPs and other LSI devices from the processing level to an on-orbit checkout has been well established in previous military and commercial systems. Specific μPs are being qualified to military specifications, and more will be added to the list. Experience to date has not uncovered any generic weak links within the μP.

The general environmental and electrical test conditions are well established in previous space projects. However, the specific applicability to μPs is being investigated. Improvements are evolving and detailed test procedures and requirements are being formulated. Specific devices are in various stages of qualification to space environments. Testing to date has shown that μP can meet the environmental and functional requirements for space applications. The formulation of worst case functional and electrical testing has not been solved. The functional tests now performed incorporate worst case postulated conditions. Preparation of good tests required intimate knowledge with the internal structure and processing of the μP along with intimate knowledge of electrical coupling effects, and the failure modes uncovered by experience.

The high cost of failure for space applications requires high reliability designs. High reliability mandates extensive testing and in many instances fault tolerant and redundant designs. Fault tolerant features built into μPs and other LSI circuits are expected to receive considerable attention in the future. Such activity will benefit not only space systems but many ground based civilian applications.

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