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TEST AND EVALUATION OF A DISTRIBUTED PROGRAMMABLE SIGNAL PROCESSOR

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Abstract

McDonnell Douglas Astronautics Company (MDAC) has developed a high performance real time, signal processor by functionally distributing both software and hardware processing components. This distributed processing architecture concept permits a single, suitably designed, microprocessing module to be interconnected to form an integrated network of processing modules. This paper describes the test and evaluation of this programmable distributed signal processor which was developed for real time processing of optical sensor data. The test methodology was structured to provide test results to evaluate: (1) the performance of individual microprocessing modules; (2) the distributed architecture concept; and (3) the overall performance of the distributed signal processor.

I. Processor Description

The MDAC signal processor (Figure 1) is a physically integrated, functionally distributed processing system, designed for optical sensor processor applications. The architecture provides for growth and flexibility by accommodating parallel processing and utilizing high speed programmable processing modules. The signal processor consists of a multistage design where each stage is composed of one or more programmable MDAC model 673 microprocessors with dedicated memory. These processing stages are interconnected by means of first in/first out queues as shown in figure 1. Each queue has four input ports and 4 output ports with fixed priority, to handle conflicts. Each processing stage performs a partitionable set of processing functions, and each processor in a given stage performs the same function(s). The design of the signal processor permits up to four 673 microprocessors to be used in each stage. Stages may be added, if desired, to accommodate additional sets of processing functions. The hardware is physically partitioned to be compatible with the architecture. There are, for example two cards (circuit boards) comprising each MDAC 673 microprocessor, one card for each 4000 words of memory (which may be 2000 RAM and 2000 PROM, or 4000 RAM), and one card for each I/O queue. Thus a particular configuration of this architecture can be derived by simply defining the required functional partitioning, throughput rate, and memory storage requirements and selecting the respective number and type of hardware cards.

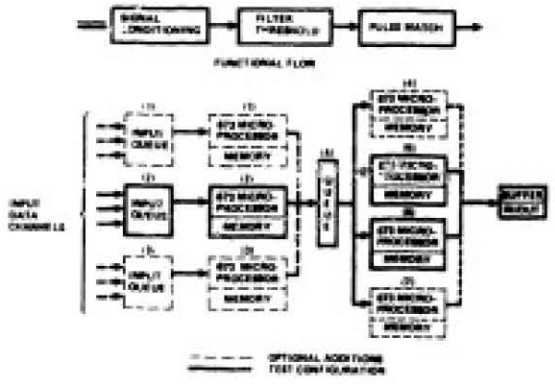


Figure 1. MDAC Signal Processor Architecture

Programmable Processing Module

The MDAC 673 microprocessor architecture (figure 2) is based on a dual bus structure and features parallelism and pipelinability. The 673 is a high speed (167-nanosecond cycle time), microprogrammable, 16-bit digital processor capable of performing fixed point arithmetic and logic operations.

It includes a CPU consisting of 16 general purpose 16-bit registers, a 16-bit accumulator/holding register, a 16-bit index register, a 16-bit base register and 16-bit arithmetic logic unit (ALU). Also included is a high speed hardware multiplier capable of multiplying two 16-bit words, resulting in a 32 bit product in 667 nanoseconds. ALU, multiplier and address generation operations can all be performed concurrently, resulting in a significant increase in performance. Special modulo addition logic is provided for data memory addressing to allow automatic addressing of sequentially stored data in circular buffers. Up to 4,000 words of programmable read-only memory (PROM) and 64,000 words of read/write random-access memory (RAM) can be directly addressed. The input/output interface was designed for ease of interfacing with special purpose input/output modules. It consists of a 16-bit parallel data input port, a 16-bit parallel data output port, status input lines, individually setable and resetable status output lines, and one maskable interrupt input line. All memory and logic components are Schottky or low power Schottky TTL. Only second sourced, LSI and MSI bipolar components are utilized in the construction of the microprocessor.

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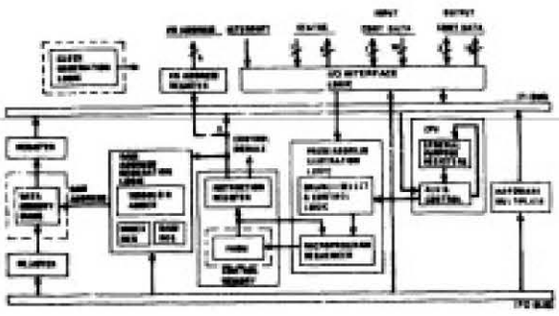


Figure 2. Microprocessor Block Diagram

II. Test Facilities

Test facilities shown in Figure 3 provide the capability to test and evaluate the MDAC signal processor and its processing modules. These facilities provide the means to simulate the processor at the functional level, assemble and develop the real time software/firmware, and to fully evaluate the operating software/firmware and support the testing of the signal processor.

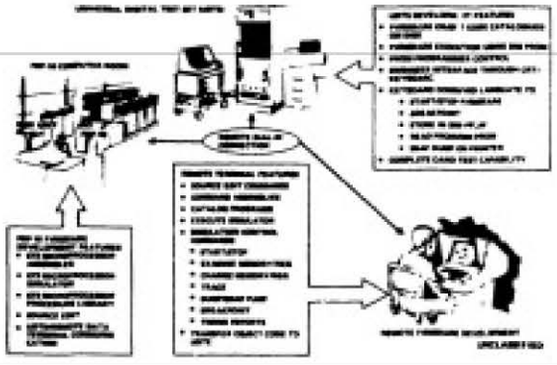


Figure 3. Test/Evaluation Facilities

The software/firmware development system for the MDAC Model 673 processor is a complete development tool. It incorporates assembly, debugging, optimization and validation capabilities with a reliable and efficient Model 673 simulator program that can be operated in either the interactive or batch mode.

The user communicates with the development system by means of a structured set of either idling commands or running commands. Idling commands are used to initialize the state of the processor; examine, change, save and restore that state; declare input and output data files; set and reset breakpoints; traps and traces; and other operations including starting or continuing the running simulation. Running commands provide such capabilities as halting the running simulation, simulating the generation of an interrupt, and checking the simulated processor without interrupting the running simulation. This system is operable on the DEC PDP-10.

Coding is done using a free format micro assembly language, assembled with an MDAC developed reconfigurable meta assembler. The microassembly language for the Model 673 processor is a compact, systematic, mnemonic language that allows the microprogrammer to code and think in terms of the functions of the machine, thus eliminating concern about the details of microinstruction control fields.

The UDTS (Universal Digital Test Set) is a programmable multiple purpose tester capable of testing individual cards and groups of cards, including the 673 microprocessor as well as the MDAC signal processor. The test set is also used to support the software/firmware development for the microprocessors. Following the debug and testing, using the simulator on the PDP-10, the code is executed on the hardware with the aid of the UDTS. Writeable control store is available on the UDTS to hold the 673 microcode for near real time execution. The UDTS also contains a dual drive floppy disk for storage of test programs and test results. The PDP-10 and UDTS are interconnected by a 9600 baud line, permitting direct transfer of object code and data between the two. The UDTS provides a man machine interface between the user and the 673 very similar to the man machine interface with the 673 simulator, which includes the ability to examine and change registers and memory, simple step, set/reset breakpoints, run, halt execution and save programs and data.

Another test capability not shown in the figure is the ability to interface the MDAC signal processor directly to the PDP-10, and a tape drive. This provides for reading sensor data (recorded on magnetic tape) by the signal processor, processing the results in real time and storing the results on the PDP-10 system for off line evaluation.

III. Processing Tests and Evaluation

The testing of the MDAC signal processor was structured to evaluate: (1) the processing capability of the individual building block modules (673 microprocessor) that are basic to the signal processor; (2) the operation and performance of the signal processor distributed architecture (a network of 673 microprocessor modules - see figure 1); and (3) the overall capability and adequacy of performance of the signal processor.

Architecture Concept Test and Evaluation

The distributed architecture of the MDAC signal processor was evaluated by using recorded sensor data as input, and executing a set of signal processing functions, in real time, on a test version of the signal processor. The signal processing functions consisted of thresholding and pulse matching (see table 1 and figure 1). The test version consisted of three processors (2, 5 and 6) and two queues (2 and 4) (see heavily outlined portion of figure 1).

The test driving data was obtained from results of functional tests on a 49 detector infrared sensor (see figure 4). The sensor functional tests were conducted in the MDAC Advanced Sensor Evaluation Test (ASET) facility. For these tests, a threat scenario was simulated in real time. A dynamic target simulator installed in the ASET chamber simulated the infrared characteristics of a target complex. The sensor output responses to these tests were recorded in real time, and subsequently used in this evaluation. Data from a group of 16 detectors used in this test represented a real time data input rate of approximately one million bits per second. Three test cases were selected, covering the more stressing signal processing cases. These cases included the discrimination and homing phase for isolated objects, crossing objects and clusters of many objects. Only the homing results (most stressing throughput case) will be discussed further in this paper. During the collection of the homing data, the sensor mirror was dithered at a 10 Hertz rate, resulting in a very large number of signal responses from the 16 detectors.

To support test and evaluation, hardware was added to permit instrumenting the processor. In addition, processing identifiers and busy/not busy controls were added to the software/firmware. For each queue in the signal processor a digital to analog (D/A) converter was added. The D/A converter was connected to the logic used to determine the fullness of the queue. By recording the output of the D/A on a strip chart, a time history of the amount of data on each queue was obtained. Also recorded with this information were the microprocessor busy/not busy indications, for the two processors used in the second stage of the signal processor. This information permitted evaluation of processor utilization and determination of whether or not the queues were sized properly.

A 150 millisecond segment of recorded signal processor instrumentation data is shown in figure 5. (Refer to figure 1 for processor and queue identifiers. This data shows that both second stage processors (processors 5 and 6) are heavily utilized during this segment of processing time. The input queue (queue 4) for the second stage is rapidly filled during each dither cycle. Slightly after the filling of queue 4, the input queue (queue 2) to the first state begins to fill to about 30% capacity (right side of figure 5) and then to 60% of capacity (left side of figure 5). The filling of queue 2 in this manner, is evidence that the first stage processor is waiting to output data to queue 4. This particular data also indicates that queue 2 is sized adequately (at least for this test case). For the case shown the size of queue 4 is adequate and no information was lost. However, for a somewhat more stressing input (more objects), a loss of data could result. Hence, increasing queue 4 in size, from 1024 words to 2048 words, would ensure an adequate margin. The fact that queue 4 empties each dither cycle indicates that sufficient processing power is available.

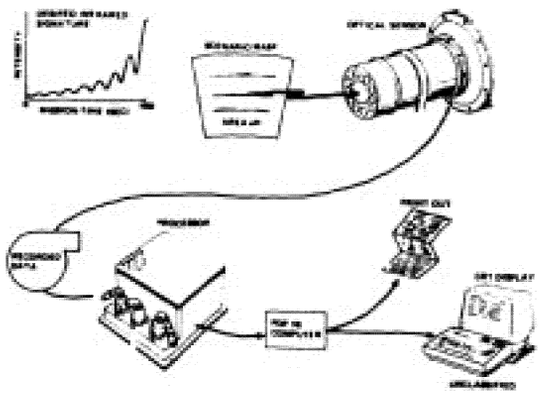


Figure 4. Processor Performance Test

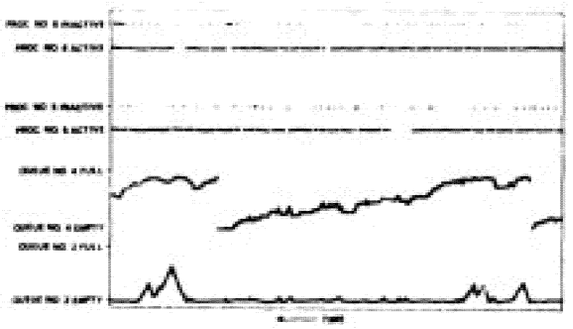


Figure 5. Signal Processor Instrumented Data

Processing Module Evaluation

The performance of the individual 673 microprocessor was evaluted by coding and then executing several key signal processing algorithms as well as the first and second stage real time signal processing functions on the 673 simulator and the 673 hardware.

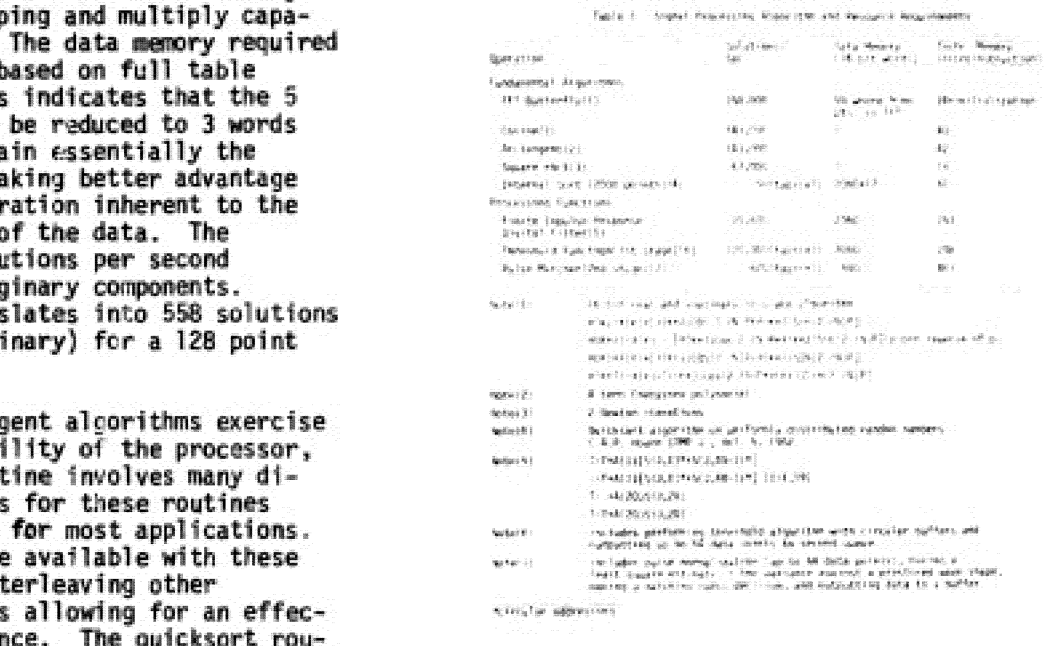
The software/firmware was developed and initially tested, using the 673 functional simulator, resident on the PDP-10. The 673 simulator has the capability to gather statistics on instructions executed. These statistics together with the number of elapsed microprocessor machine cycles, also provided by the 673 simulator, allow determination of the real time required to execute the program and the number and types of instructions executed. These same statistics were also used to assist in program testing by verifying that all statements in the code were tested. Following verification on the 673 simulator, the programs (routines) were validated by execution on the 673 hardware, under control of the UDTS, and comparing the two sets of results.

The set of signal processing algorithms and functions for this phase of the evaluation are identified and defined in table 1, along with the results, memory requirements and number of 673 micro instructions. All results are based on single precision (16 bit) operations. The FFT algorithm exercises the bookeeping and multiply capability of the processor. The data memory required for the FFT butterfly is based on full table look up. Current analysis indicates that the 5 words per FFT point could be reduced to 3 words per point and still maintain essentially the same execution time, by taking better advantage of the concurrency of operation inherent to the 673, and generating some of the data. The 250,000 FFT butterfly solutions per second include both real and imaginary components. This processing rate translates into 558 solutions per second (real and imaginary) for a 128 point FFT.

The cosine and arctangent algorithms exercise the shift and multiply ability of the processor, while the square root routine involves many divides. The solution rates for these routines appear to be satisfactory for most applications. The unused execution space available with these three routines, permit interleaving other operations with them, thus allowing for an effective increase in performance. The quicksort routine utilizes the data handling capability of the processor. The typical execution rate for the sort routine is extremely fast.

The FIR Filter exercises the modulo addressing ability of the processor. The 25,600 solutions per second of the 39 point FIR filter is adequate to accommodate a sample rate in excess of 500,000 samples per second, assuming 50 percent overlap. The execution rates given in Table 1 for the first and second stage processing functions are typical rates since the specific execution times are a function of the number of sampled data points. These times are based on both simulation and actual processor execution times. The solution rate of 120,000 per second for the threshold function is sufficiently fast that other functions, such as band pass filtering can easily be combined with it within the same microprocessor. The 625 pulse matches per second includes normalization of pulses containing up to 64 sampled data points, computing the variance of each pulse passing threshold and outputting the results along with other data such as angles, delta angles, time and detector identification to the output buffer.

Our conclusions from this phase of the evaluation is that the MDAC 673 is a high performance microprocessor with a large amount of flexibility and a high degree of adaptability to signal processing problems. Further more, since the 673 is packaged on only two 6 inch x 10 inch circuit cards and uses only available militarized MSI and LSI logic and memory components, it can be fabricated at relatively low cost, even in small quantities.



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A review of all the test data indicated that the processor assigned the highest priority, by means of its connection to interfacing queues, has a higher utilization than the other processor. For a configuration of three of four processors per stage, it is expected that processor utilization would correspond to assigned processor priority. Disabling one of the second stage processors, while it was executing, resulted in the other processor performing all the processing for the stage. This was as expected and provides for the possibility of built-in redundancy and automatic switching due to failure.

Evaluation of the test results also shows the use of queues is an effective way to interconnect processing stages in an asynchronous manner. The queues also allow for conveniently adding processing stages and increasing or decreasing processing capability within a stage. Software/firmware overhead is also reduced in this architecture, since much of the control is embedded in the hardware, allowing autonomous operation of each microprocessor. Each processor in a given stage has identical software/firmware, with the exception of identifiers needed for test purposes. The price paid for this modular capability is, of course, additional memory and non-optimum processor utilization. The payoff is high speed performance and flexibility. Today's semi-conductor technology permits this trade off to be favorable for this architecture.

Overall Signal Processor Performance

The overall capability and adequacy of performance of the MDAC signal processor was evaluated by comparing its results with results obtained from runs of a high fidelity, non-real time version of the same functions programmed on the DEC PDP-10 (a 36 bit machine) used as a truth model. Identical data were used as input to the processing on both machines. The thresholding and pulse matching functions, identified earlier were coded and executed on both machines. These functions were coded in Fortran for the PDP-10 and in 673 micro assembly language for the MDAC signal processor.

The key issue addressed in this phase of the evaluation was accuracy (is a 16 bit real time implementation adequate?). The comparison analysis was directed towards the differences in the pulse matcher processing, i.e., the computed variance and peak amplitude of the signals that were output from the threshold function. Since the threshold function is primarily a data handling function, the results of processing in the signal processor and truth model were identical. The analysis of the two sets of pulse matcher results showed a very favorable comparison. Only minor differences existed in the computed values for the variance and peak amplitude. The values differed only in the least significant place and were within three percent. Based on these results, it appears that a 16 bit machine meets the accuracy requirements.

IV. Conclusions

The test and evaluation of the signal processor would not have been possible without adequate instrumentation aids built into the hardware and application software/firmware. Establishing satisfactory test and evaluation aids, combined with a complete test and evaluation facility that includes both hardware and software test and evaluation tests, are key for a successful test program on a distributed processor. The instrumentation aids serve a dual purpose, since they are also desireable operationally, to analyse performance and to establish complete operability of the processor.

The MDAC distributed programmable signal processor is an extremely powerful high speed processor. The real time processing results of the signal processor compare favorably with results produced by the truth model program implemented on the DEC PDP-10. The three processor version of the signal processor, used in the evaluation, was able to execute the signal processing functions in real time, illustrating the desireability of a distributed architecture for this class of processing. The modular architecture of the signal processor provides for ease of growth in the number of processing stages, as well as the number of processing modules per stage. The feasibility of this architecture is due primarily to the state of today's semi-conductor technology. The MDAC 673 microprocessor, used as the processing module in the MDAC signal processor, is a high speed microprocessor, well suited for signal processing applications, and is producable at relatively low cost.

V. Acknowledgements

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