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FINAL REPORT
Contract No. NAS8-32607

DESIGN, PROCESSING AND TESTING OF LSI ARRAYS HYBRID MICROELECTRONICS TASK 3 AUGUST 1977 - 2 AUGUST 1978

15 SEPTEMBER 1978

Prepared for
George C. Marshall Space Flight Center
Marshall Space Flight Center
Alabama 35812

HUGHES
MICROELECTRONIC PRODUCTS DIVISION
NEWPORT BEACH, CALIFORNIA 92663

DESIGN, PROCESSING AND TESTING OF LSI ARRAYS

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R. P. Himmel
S. M. Stuhlbarg
S. Salmassy

INDUSTRIAL ELECTRONICS GROUP
Microelectronic Products Division
Hughes Aircraft Company • Newport Beach, California 92663

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1.0 INTRODUCTION AND SUMMARY

This report summarizes the effort on Contract NAS 8-32607, which involved determination of those factors affecting the cost of electronic subsystems utilizing LSI microcircuits, and development of the most efficient methods for low-cost packaging of LSI devices as a function of density and reliability.

This one-year program has been divided into three Tasks as follows:

TASK 1. Cost Factors Study

Perform a cost study to identify all the factors involved in packaged electronic subsystems as a function of density and reliability. The study should encompass LSI devices packaged both by hybrid technology and standard discrete packaging.

TASK 2. Study Areas

Based on an analysis of the cost factors determined in Task 1, provide recommendations for study in the area(s) that show the most promise for cost reductions in high density packaging.

TASK 3. Packaging Implementation

One specific high cost impact area in hybrid packaging has been LSI chip testing and bonding. Beam-tape technology has been established as a viable and cost saving technique for producing high-volume discrete device packages. Many types of semi-conductors are currently available on beam-tape and, with few exceptions, most semiconductors can be adapted to beam-tape. It is required during this study that a demonstration program be performed to adapt LSI chips on beam-tape for hybrid packaging.

Tasks I and II essentially have been combined to constitute the COST FACTORS STUDY, which has been expanded at NASA request and by mutual consent to include limited mathematical modeling. Both the cost factors

and the mathematical modeling are intended for usage as guidelines for the preparation of mathematical pricing models suitable for computer programming. The combined Tasks I and II previously have been published in the Semi-Annual Report on this contract (Report No. P78-162, dated 10 March 1978). This information is repeated herein, after addition of minor corrections, and expansion in several areas related to process yield.

Task III, a Packaging Implementation program comprising demonstration and testing of tape chip carrier (TCC) processes, was initiated on contract award, in parallel with Tasks I and II. This effort (reported herein) has been completed essentially as proposed and reported during the program, with demonstratable results in all areas except gang burn-in on tape.

Recommendations are included; both for future cost factors study efforts, and for further process refinement related to TCC technology.

2.0 TECHNICAL DISCUSSION

This combination study/development program comprises both the identification of cost factors related to LSI/hybrid technology, and the demonstration of a particular packaging approach: tape chip carrier technology, as applied to the adaptation of LSI chips for hybrid packaging.

The Program Schedule of Figure 2-1 includes the Sub-Tasks involved in both the cost factors and the TCC packaging implementation portions of the program. As indicated in the Introduction and Summary Section, the combined Tasks I/II have been modified somewhat by NASA/Hughes mutual consent, and this report includes results of the modified task.

With respect to Task III, the effort has included TCC tape/wafer process/materials evaluation, inner-lead bonding (ILB) evaluation, outer-lead bonding (OLB) evaluation, test sample fabrication, and environmental testing/data analysis. Table 2-1 is a summary/breakdown of Task III subtasks, indicating qualitatively the degree of progress achieved on each of them.

2.1 TASKS I AND II - COST FACTORS STUDY

To initiate the required cost factors study involving LSI devices packaged both by hybrid technology and standard discrete parts assembly methods, a survey questionnaire was formulated, and a proposed mailing list was prepared comprising approximately 100 selected LSI packaging experts and hybrid microelectronics managers. When this was reviewed by MSFC personnel, it was determined that interviews with cognizant Hughes personnel, coupled with a literature survey, would be preferable, and that the resulting cost factors data would be more useful than an industry-wide survey in making an initial cost model which could be programmed for computer input.

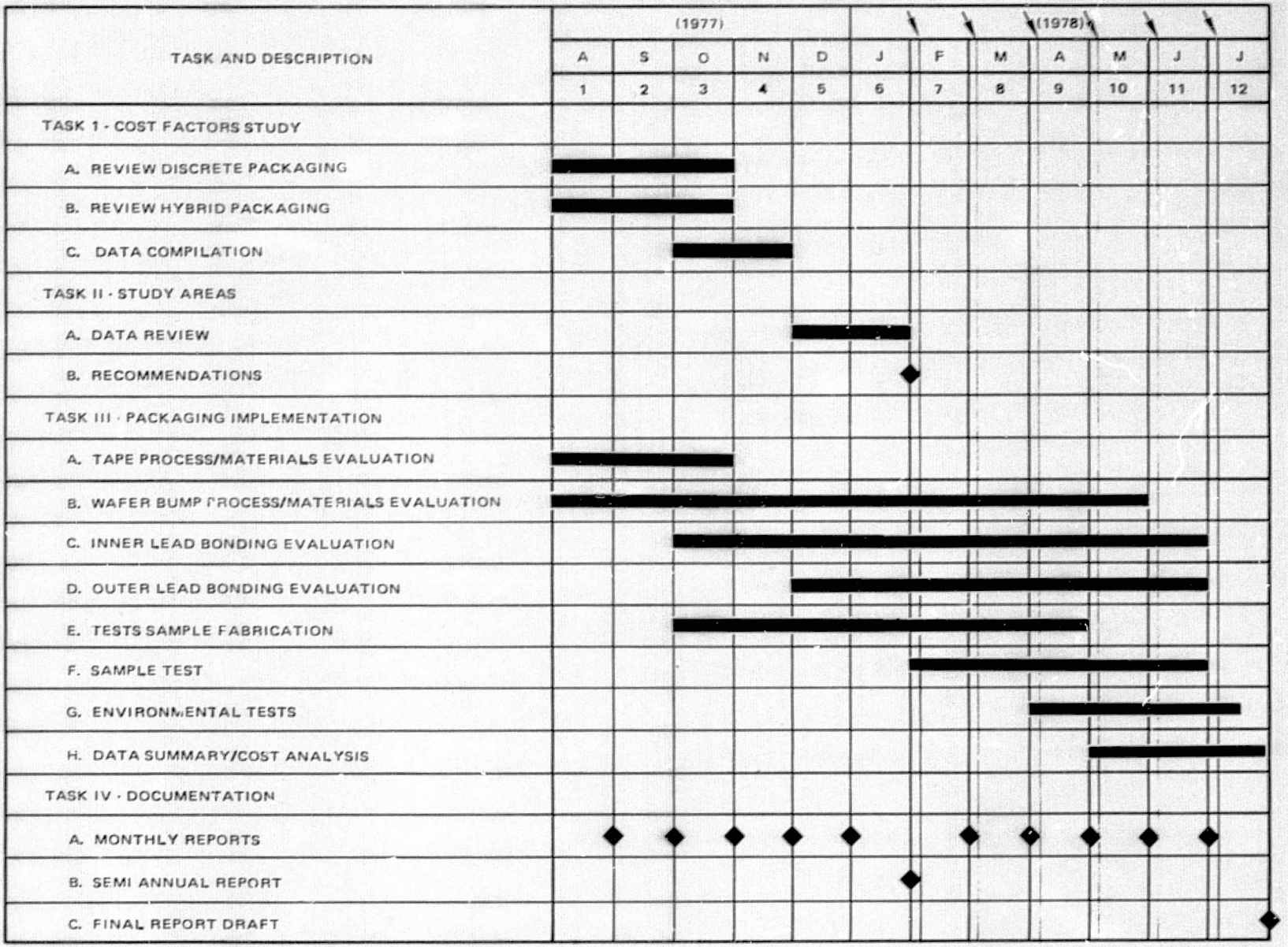


Figure 2-1. Program schedule - NASA Contract No. NAS8-32607.

TABLE 2-1. PACKAGING IMPLEMENTATION SUB-TASK BREAKDOWN

CONTRACT NO. NAS8-32607, TASK III

12 AUGUST 1978

	PLAN	EXECUTE
A. TAPE PROCESS/MATERIALS EVALUATION — PERCENTAGE COMPLETION	25 50 75 100	25 50 75 100
A.1 SELECT T^2L (A), MOS (B), AND ECL (C) VEHICLES		
A.2 PREPARE TAPE WORKSHEETS (A), (B), (C)		
A.3 PROCURE MASKS (A), (B), (C)		
A.4 ALIGN/EXPOSE/DEVELOP/ETCH TAPES (A), (B), (C)		
A.5 FABRICATE UP TO 100 EACH TAPE POSITIONS (A), (B), (C)		
A.6 PLATE/PUNCH-OUT PLATING LINKS (FOR GOLD PLATING, PLATE PRIOR TO PUNCH-OUT)		
B. WAFER BUMP PROCESS/MATERIALS EVALUATION		
B.1 DEMONSTRATE WAFER DC CHARACTERIZATION (B) ONLY		
B.2 DEMONSTRATE WAFER BUMPING (A), (B), (C) (W-Ti/Au)		
B.3 DEMONSTRATE WAFER RE-CHARACTERIZATION (B) ONLY		
B.4 DEMONSTRATE SHEAR TEST (A), (B), (C) (SAMPLE BASIS)		
C. INNER-LEAD BONDING EVALUATION		
C.1 PROCURE ILB COLLETS (THERMODES AS REQUIRED)		
C.2 MOUNT AND SAW WAFERS (A), (B), (C)		
C.3 DEMONSTRATE ILB (A), (B), (C)) (APPROXIMATELY 40 TAPE POSITIONS EACH)		
C.4 CHECK-OUT PULL-STRENGTH (EXCISE SAMPLES AND DESTRUCTIVE-TEST)		
F. SAMPLE TEST/BURN-IN STUDY		
F.1 DEMONSTRATE GANG BURN-IN (A) ONLY (CONTROL SAMPLE NOT BURNED-IN)		
F.2 PROCURE CUSTOM TAPE PROBER ((B) AND (C))		
F.3 DEMONSTRATE FUNCTIONAL TESTING ON TAPE (A) AND (B) (CONTROL SAMPLE NOT FUNCTIONALLY TESTED)		
E. TEST NETWORK FABRICATION		
E.1 FABRICATE TEST NETWORKS FROM EXISTING SCREENS (A) ONLY (10 FRITTED PD-Ag, 10 MIXED-PHASE GOLD; 16 CHIP POSITIONS PER NETWORK)		
E.2 PROCURE 10 CUSTOM HERMETIC CHIP CARRIERS (HCC's FROM EXISTING HUGHES STOCK (B) ONLY (W-Ni-Au)		
D. OUTER-LEAD BONDING EVALUATION		
D.1 DEMONSTRATE OLB USING EXISTING TOOLING (A) ONLY (40 CHIPS GOLD/GOLD: TC BOND TO MIXED-PHASE Au AND Pd-Ag		
D.2 DEMONSTRATE OLB TO 10 HCC's (C) ONLY (GOLD/GOLD)		
D.3 CHECK-OUT PULL STRENGTH (SAMPLE BASIS; DESTRUCTIVE TEST)		
D.4 DEMONSTRATE NON-DESTRUCTIVE PULL-TEST		
G. ENVIRONMENTAL TEST		
G.1 PREPARE TWO EACH TEST NETWORKS (A) (Pd-Ag AND Au) AND THEIR CLB CHIPS FOR ENVIRONMENTAL TESTS BY SCRIBING/ BREAKING SUBSTRATES, AND THEN MOUNTING THEM INTO STANDARD PLATFORM-TYPE SEALABLE METAL PACKAGES		
G.2 PREPARE 10 HCC's (C); SEALING 7 UNITS		
G.3 CONDUCT HIGH TEMPERATURE STORAGE TEST PER MIL-STD-883, METHOD 1008.1, CONDITION C (150°) (A) ONLY		
G.4 CONDUCT THERMAL CYCLING TESTS PER MIL-STD-883, METHOD 1008.1 CONDITION B (A) ONLY INCLUDE UNSEALED CONTROL SAMPLES		
G.5 REPEAT PULL TESTING ON A SAMPLE BASIS		
G.6 CONDUCT 85-85 MOISTURE RESISTANCE TEST (A) ONLY (INCLUDE UNSEALED CONTROL SAMPLES)		
H. DATA SUMMARY/COST ANALYSIS		
H. 1 CONSOLIDATE AND EVALUATE DATA		
H. 2 PUBLISH DATA		

Cost Factors Data Search

Table 2-2 summarizes the computerized cost factors data search, from which the most promising abstracts were selected. Abstracted data in the form of table, graphs, and key sentences were clipped from the 225 reviewed reference articles and organized in the form of a data summary. In addition, a brief search of the microelectronics technical literature resulted in several other articles of interest.

In-House Cost Factors Data Search

Four Hughes facilities were surveyed through personal interviews with pertinent people in the pricing, estimating, and planning areas. These sites include both prototype and production areas. Most Hughes electronics subsystems are intended for military systems, including avionics, missiles, and ground systems applications.

Task Re-Direction

In November 1977, Tasks I, II were expanded to include mathematical modeling information which will be more directly applicable to the desired computer programming. The distribution between cost factors data and the

TABLE 2-2. COMPUTERIZED COST FACTORS DATA CLASSIFICATION

1.	General	Miscellaneous observations and data about the impact of LSI device manufacturing technology on the electronics industry.
2.	Specific	Cost comparison data of circuits employing LSI devices. Representative factors found to be related to dollar figures include: chip density, chip area, memory chip capacity, gate density, interconnection types, density, ceramic vs. epoxy boards, packaging methodology, and cost trade-offs pertaining to systems within which LSIs could be or have been used.
3.	Cost Projections	Involving electronic systems using LSI devices, plus similar projections related to the LSI devices themselves.
4.	Cost Models	Two models were found in the references.

mathematical models, as accomplished during this combined Task, is summarized in Table 2-3.

2.1.1 Cost Factors

The printed wiring board (PWB) cost factors listed in the following discussion were collected by interviews with engineering, estimating, and planning personnel at four different Hughes locations. These areas have years of experience in both prototype and production fabrication and assembly of PWBs for missile systems, airborne radar systems, ground systems, space systems, and other military applications.

Cost factors can be broadly categorized into many basic divisions, including areas such as indirect/direct, recurring/nonrecurring, and manufacturing/engineering. For purposes of this study, the cost factors have been divided into three classifications:

- Nonrecurring cost factors
- Manufacturing cost factors
- Production support cost factors

A listing of the major cost factors in the basic PWB areas (Fabrication and Assembly) has been prepared for each of these three classifications, giving a total tabulation of the following six separate cost factor listings:

1. Nonrecurring Cost Factors Associated with PWB Fabrication

TABLE 2-3. TASK I/II DISTRIBUTION BETWEEN COST FACTORS DATA AND MATHEMATICAL MODELING

	Hybrid Technology	Standard Discrete Packaging
Cost Factors Data	–	PWB Technology
Mathematical Modeling	Thin/Thick Films	–
Examples:	A. Tape Chip Carrier Usage B. LSI Usage C. Wafer Bumping	–

2. Manufacturing Cost Factors Associated with PWB Fabrication
3. Production Support Cost Factors Associated with PWB Fabrication
4. Nonrecurring Cost Factors Associated with PWB Assembly
5. Manufacturing Cost Factors Associated with PWB Assembly
6. Production Support Cost Factors Associated with PWB Assembly

Both Production Support and Manufacturing cost factors normally are "recurring." Basic administrative costs may or may not be charged directly to a program. Usually such costs are a part of the company's general administrative and overhead expenses. Specific program management costs incurred by direct labor personnel however, would be a significant recurring cost factor and as such, should be accounted for in any mathematical model for pricing. The time of a shop supervisor or foreman would be an example of a direct administrative cost. Administrative costs can indirectly affect the total pricing picture if they appear as a part of the burdened labor rate.

Nonrecurring Cost Factors Associated with PWB Fabrication

Table 2-4 is a listing of the primary nonrecurring cost factors associated with the fabrication of PWBs. Several of these factors will be affected if the task is done automatically, such as with the aid of an automated design facility. For example, a manual PWB layout can be digitized, resulting in:

1. A set of 1:1 masters
2. A drill tape for numerically-controlled hole drilling
3. A testing program
4. A set of released drawings.

Certain of these nonrecurring costs are dependent on the complexity of PWB design (e.g., number of conductor lines, number of layers, or card density). Using computer-aided design for example, it may cost $250 per layer to produce reduced masters for a low density PWB and $350 per layer for a high density PWB. In addition, a highly complex board will require considerably more engineering design time than will a simple board. By using an Interactive Graphic System, the time spent for engineering design can be reduced.

TABLE 2-4. PRIMARY NONRECURRING COST FACTORS ASSOCIATED WITH PWBs

1. Engineering design, including design reviews and redesigns.
2. Special fixtures and hard tooling.
3. Implementation support, such as engineering labor spent in setting up certain processes.
4. Artwork (1:1 film masters).
5. Drill Tape.
6. Computer program for automatic bareboard testing.
7. Initial planning.
8. PWB layout.
9. Preparation of any necessary specifications.

Manufacturing Cost Factors Associated with PWB Fabrication

A listing of the fifteen major manufacturing cost factors involved in the fabrication of printed wiring boards is shown in Table 2-5. In some facilities, quality control (QC), inspection, and testing cost factors are compiled separately, rather than being included as part of manufacturing costs. Testing and QC also could be considered as a part of Production Support. Automation primarily enters the picture in hole drilling and testing.

Production Support Cost Factors Associated with PWB Fabrication

The two most important production support cost factors are:

1. Coordination and dispatch. This could be about 15 percent of the total cost; it includes the planning, labor, and paperwork necessary to move PWBs between the various work stations.
2. Sustaining engineering support. This includes process engineering and test engineering.

Nonrecurring Cost Factors Associated with PWB Assembly

Table 2-6 is a listing of the primary nonrecurring cost factors associated with PWB assembly.

TABLE 2-5. MAJOR MANUFACTURING COST FACTORS INVOLVED IN FABRICATION OF PWBs

1. Number of holes.
2. Number of different hole sizes (i.e., number of drill changes).
3. Material costs (e.g., type of PWB material and/or hardware), plus an attrition factor.
4. Size of the board. This is relevant in that it governs the number of smaller PWBs which simultaneously can be made from a larger standard panel size (e.g., 9" x 12", 9" x 18", 12" x 18").
5. Quantity of PWBs in the lot.
6. Whether the PWB is two-sided or multilayer (and the number of layers).
7. Yield or scrap factor. A typical yield might be from 80 to 90 percent.
8. Complexity factor. This factor normally is related to the number of holes, line widths, pad sizes, line spacings, and hole sizes.
9. Automatic or scope drilling of holes (if no numerically-controlled drill tape is available).
10. Type of electroplating (e.g., gold, solder, tin).
11. Rework factor.
12. Inspection and quality control cost factors. These factors could be up to 10/20 percent of the total unit cost.
13. Automatic or manual electrical testing of the PWB.
14. Copper thickness (e.g., 1 oz, 2 oz).
15. Any special features, such as special markings, special hardware installation, or special machining of the PWB.

TABLE 2-6. PRIMARY NONRECURRING COST FACTORS ASSOCIATED WITH PWB ASSEMBLY

1.	Engineering design, including design reviews and redesigns.
2.	Layout of the PWB assembly and preparation of a complete drawing package. This layout may be computerized to some degree by using an Interactive Graphics System.
3.	Initial planning.
4.	Design and fabrication of any special fixtures, tooling, and assembly aids.
5.	Preparation of any necessary test specifications, process instructions, and material specifications.
6.	Implementation support.

In many cases, the engineering design/layout of the PWB for fabrication and the preparation of PWB assembly drawings are accomplished in conjunction with one another, and are priced as an overall drawing package. For purposes of a mathematical model, it primarily is necessary to know that these cost factors exist, and they they comprise a relatively large part of the nonrecurring costs.

Manufacturing Cost Factors Associated with PWB Assembly

A listing of the seventeen major manufacturing cost factors involved in the assembly of PWBs is included in Table 2-7. Many of these could be lumped together for convenience as a "manufacturing technique" cost factor. Such manufacturing techniques can include component parts preparation, component parts insertion, soldering/coating methods, hardware installation, and miscellaneous cost factors. Automatic or semi-automatic machinery normally is used for operations such as component lead preparation, component insertion, flow-soldering, reflow soldering, and coating. If quantities are small, it may not pay to automate to any great extent.

TABLE 2-7. MAJOR MANUFACTURING COST FACTORS INVOLVED IN PWB ASSEMBLY

1. Quantity of PWBs to be assembled.
2. Material and parts costs, plus an attrition allowance. This would include costs for all components (e.g., resistors, SICs) and hardware. The reliability level of the design can affect costs considerably, since higher levels mean increased costs for parts and materials.
3. Yield cost factor.
4. Amount of rework from both assembly and electrical test operations.
5. Component parts preparation. This may be done manually or automatically, and includes operations such as lead forming and tinning.
6. Parts complexity cost factor. This usually is based on the number of component parts (or total number of leads) and the parts count per unit PWB area.
7. Standardization. This cost factor can affect both assembly time and the initial cost of parts, since standard off-the-shelf parts cost less than do custom parts.
8. Packaging concept cost factor. As an example of this cost factor, consider a PWB design where the engineer has the option of using either DIPs or flatpacks. DIPs are cheaper, do not require lead forming, and can be flow-soldered. Flatpacks do not require board holes, however.
9. Testing Cost factor. This includes electrical functional testing, plus any environmental testing required. In many facilities, testing also includes the troubleshooting time which goes along with rework. The more complex the circuit, the more it costs to test that circuit. Automated test programs can be a big cost saver.
10. Reliability or quality cost factor. This factor either directly or indirectly affects many of the others. The reliability level can affect the cost of parts, rework, inspection time, testing costs and others. A higher reliability level could increase manufacturing costs by 50 to 100 percent.
11. Component Insertion Cost Factor. This factor depends on whether the particular component part can be inserted automatically or semi-automatically. Most DIPs, flatpacks, and axial lead parts can be automatically assembled to the PWB.
12. Soldering method cost factor. The pricing figure will vary, depending upon whether the PWB is flow-soldered, reflow-soldered, hand-soldered, or welded. Both flow-soldering and reflow-soldering can be done automatically.
13. Coating cost factor. This factor is concerned with whether the PWB is conformally coated, parylene coated, foamed, encapsulated, or otherwise protected by some coating. Operations such as masking, unmasking, cleaning, and touch-up, all of which are related to coating, are included.
14. Hardware installation cost factor. This factor sometimes may be included under Fabrication costs rather than Manufacturing costs. It includes those additional costs caused by the use of special heat sinks, connectors, lugs, terminals, and rivets which must be installed on the PWB.
15. Set-up cost factor. This includes the labor necessary for setting up certain operations in readiness for a production run.
16. Inspection and quality control cost factors.
17. Miscellaneous cost factors, such as special markings, special wire types, and special wire color codings.

Production Support Cost Factors Associated with PWB Assembly

Table 2-8 is a listing of the most important production support cost factors associated with PWB assembly. Many of these factors (such as Numbers 3 through 10) may not necessarily be applied directly to a particular PWB design, but instead may be part of an overall cost which is chargeable to a complete program. Some PWB assembly facilities may consider cost factors; such as quality assurance, inspection, and testing as a part of Production Support rather than Manufacturing.

For purposes of a mathematical model, it is difficult to assign a number or formula to most of the Production Support cost factors, since these ordinarily are not a specific percentage of the total manufacturing cost, and they do not have "standard hour" rates assigned to them. For purposes of discussion, sustaining engineering might be 17 percent of the manufacturing unit cost, and coordination, dispatch might be 15 to 19 percent.

TABLE 2-8. PWB ASSEMBLY – PRODUCTION COST FACTORS

1.	Coordination and Dispatch. This includes kit preparation, planning, scheduling, and similar tasks involved in moving the PWBS between the various work stations.
2.	Sustaining Engineering Support, including process engineering and test engineering.
3.	Inventory control.
4.	Spares control.
5.	Materials control.
6.	Data processing.
7.	Test Equipment Calibration.
8.	Tool Maintenance.
9.	Line Coordination.
10.	Configuration Control.

2.1.2 Flow Charts

A series of nineteen flow charts have been prepared, as listed in Table 2-9 and included as Appendix A. These charts represent those manufacturing processes which are concerned with LSI devices packaged both by hybrid microcircuit technology and standard discrete packaging. They are intended as guides for the preparation of mathematical pricing models. Flow Chart Number 1 is a Summary Chart which presents an overall picture of how the other flow charts relate to one another. The charts generally are brief, and contain only essential steps in the processes. Dashed lines have been used to indicate alternate (or optional) process steps.

These flow charts basically cover the history of semiconductor chips (presumably LSI devices) from the time they are separated from the wafers until they finally become an integral part of an electronic subsystem. For purposes of these charts, the electronic subsystem was carried to the level of a printed wiring board (PWB) or alternately, to a PWB equivalent (i.e., a Large Area Hybrid (LAH) or a Buried Multilayer Ceramic-Based Network). As shown by the charts, an LSI chip can take many paths (representing different packaging concepts) before it is mounted on the PWB or CWB. Many of these paths lead to a hybrid microcircuit package, while others lead to special packages (e.g., DIPs, hermetic chip carrier (HCCs)) which are mounted directly on the boards. A single PWB or CWB may contain a mixture of packaging technologies. For example, it may contain DIPs, hybrid microcircuits, and discrete axial lead devices.

If the basic wafer is bumped, or if beams are formed on the wafer, the device becomes a flip-chip or beam-lead chip ready for assembly to a hybrid microcircuit network. It also is possible for the entire wafer to be mounted on a special large area hybrid or a buried multilayer ceramic-based network.

Flow Chart Nos. 2 through 8 cover the basic thin-film and thick-film hybrid processes (both single and multilayer), including assembly and acceptance testing. Flow Chart Nos. 9 through 11 cover PWB fabrication and assembly (flatpacks and DIPs). The other flow charts cover single-chip processing and other processes (e.g., tape chip carrier, hermetic chip carrier) which are applicable to LSI devices.

TABLE 2-9. FLOW CHART LISTING (Attached as Appendix "A")

1.	Summary Process Flow Chart from Wafer to Final Assembly and Test
2.	Hybrid Microcircuit Assembly Process
3.	Hybrid Microcircuit Acceptance Testing Process
4.	Thick-Film Substrate Fabrication Process
5.	Thick-Film Multilayer Substrate Fabrication Process
6.	Thin-Film Substrate Fabrication Process
7.	Thin-Film Multilayer Air Gap Process
8.	Thin-Film Substrate Metallization Process
9.	Printed Wiring Board Assembly Process for Surface-Mounted Components
10.	Printed Wiring Board Assembly Process for DIPs
11.	Typical Printed Wiring Board Processing Sequences
12.	Large Area Hybrid Process
13.	Tape Chip Carrier Process
14.	Buried Multilayer Ceramic Substrate Fabrication Process
15.	Hermetic Chip Carrier (HCC) Process
16.	Process Sequence Flow Chart for a Higher Power Transistor Captive Line
17.	Flip Chip Processing and Assembly
18.	Beam Lead Processing and Chip Assembly
19.	MOS Integrated Circuit Chip Packaging Process

2.1.3 Mathematical Models

Mathematical cost models have been built for hybrid electronic subsystems, and fundamental equations modeling the total hybrid manufacturing cost using thin and thick film technologies have been derived. Also, the total manufacturing cost variations when tape chip carrier and LSI devices are introduced into the hybrid technology have been evaluated quantitatively. Where possible, terms of the equations have been compared to each other, and observations about their respective importance to the manufacturing costs have been made.

2.1.3.1 Background

The manufacturing cost model for hybrid electronic subsystems is built on

1. Literature and in-house search data
2. Assumptions of functional relationships between parameters characterizing the hybrid technology
3. Definitions relating quantitative process and product parameters
4. Simplifications of actual manufacturing processes (only those terms most relevant to the total hybrid cost were considered).

To obtain a comprehensive and simple model where sophistication of the mathematical algorithm does not overcome its own ability of expression, many assumptions and simplifications were made. Doing so, the general validity of the model was not affected. A "working model" has been built; one which is quantitatively accurate in the range of its limitations. Outside the range, severe lack of specific data on which to build accurate definitions was found. The model therefore is accurate outside its limitation range only when the qualitative behavior of some cost function is sought.

All of the mathematical formulas can be applied readily by using the parameter values reported in Tables 2-10 and 2-11. Also, any hybrid microcircuit can be defined readily in terms of the "Reference Hybrid" which was built to obtain fundamental constants of the equations. The reference hybrid is an average-complexity electronic subsystem for aerospace applications. Parameters characterising this hybrid can be found in Table 2-12.

TABLE 2-10. SUBSTRATE PROCESSING – VALUES OF CONSTANTS AND PARAMETERS

	Constants	Thin Film	Thick Film
C_{OS}	dollars	30.00	0.64
C_{OE}	standard hours (STDH)	0.124	0.024
Y_o	non-dimensional	1.56	1.5
K_T	STDH x in^2	0.205	0.038
K_{QC}	STDH	7.2×10^{-2}	4×10^{-2}
K_C	in^2	2.4×10^{-3}	4.6×10^{-3}
K_C'	non-dimensional	7.1×10^{-3}	7.1×10^{-3}

	Parameters	Thin Film	Thick Film
δ_R	Number of resistors/in^2	76	23
δ_c	Number of chips/in^2	144	70
δ_{SR}	Area of one resistor/ hybrid area	5.4×10^{-4}	2.28×10^{-3}
t_R	Inverse of tolerance	5	5
$S_{\%}$	Hybrid size factor	1.0 for 1.5 x 2 in substrate 0.5 for 0.75 x 1.75 substrate 0.3 for 1 x 1 substrate	
C_c	Hybrid complexity factor	0.5	
δ_{pmax}	Maximum number of pads found on IC	16	
W_r	Wage rate (arbitrary constant assigned for relative comparison only), $/Hr	12.00	

TABLE 2-11. ASSEMBLY AND TESTING – VALUES OF CONSTANTS AND PARAMETERS

	Constants	
C_{op}	dollars	23
β_o	non-dimensional	7×10^{-6}
β_1	dollars	0.13
β_2	dollars	0.80
β_3	dollars	1.6
C_{OPT}	standard hours (STDH)	0.033
a	STDH	9.3×10^{-4}
b	STDH	6.6×10^{-4}
d	STDH	0.033
K_{QC1}	STDH	0.088
g	STDH	0.088
g'	STDH	2.76
h	STDH	0.025
K_{QC2}	STDH	0.51
ℓ	STDH	0.186
C_{TT}	STDH	0.22
g''	STDH	1.38
h'	STDH	0.044
K_{QC3}	STDH	0.02
C_o	STDH	0.25
u	STDH	0.0275
u_B	dollars	0.20

	Parameters	Thick Film	Thin Film
N_{TRJ}	Total number of transistor junction of ICs	800	480
N_{TRD}	Total number of transistors and diodes	30	13
N_{CAP}	Total number of capacitors	40	20
N_C	Total number of chips	90	45
N_{CIC}	Total number of ICs	20	12

(Continued next page)

(Table 2-11 concluded)

	Parameters	Thick Film	Thin Film
N_{WB}	Total number of bonds	640	340
N_R	Total number of resistors	100	30
t_y	Package type factor (Figure 4)	2.0 for butterfly package; 1.0 for HAC-PAC	
Q	Number of packages purchased in a lot (Figure 4)	10,000	
C_L'	Average cost of a package lid	$1.70	
n'	Number of lids	1.0	
C_{BS}	STDH for substrate bonding	0.12	
m	Die attachment factor	1.0 for epoxy attachment 2 for moly tab attachment	
δ_p	Number of pads/IC	16	
f	Fraction of other connections (jumpers and to package leads)	0.40	
r	Reliability level	1 for military or space 0 for low and high cost	
$\overline{N}_{TRJ}$	Average number of transistor junctions/chips	40	
n	Number of reworks before sealing	1	
n'	Number of reworks after sealing	1	
g_1	Fraction of chips reworked before sealing	0.1	
g_2	Fraction of bonds reworked before sealing	0.05	
g_1'	Fraction of chips reworked after sealing	0.02	
g_2'	Fraction of bonds reworked after sealing	0.004	
C_{LR}	Rework due to lid substitution, STDH	1.20	
C_{TT}	Acceptance Test, STDH	0.25	
V	Number of hybrids produced per year	1.2×10^5	

TABLE 2-12. REFERENCE HYBRID

Hybrid size	0.75" x 1.75" Area = 1.3125 in^2	
Number of package leads	74 (only 60 are actually used)	
Number of connections (pads) per chip	16	
Active chip (reference) Sn 54LS 138, Elmo Semiconductor Corp.	40 transistors (9 gates)	
Number of hybrids produced/yr	1.2×10^5	
Number of components on a 0.75" x 1.75" Area		
Components	Thin	Thick
Active Chips		
Transistors and Diode (area =1/4 IC area)	30	13
ICs (50 x 65 mils)	20	12
Passive Devices		
Capacitors (area =1.5 - 2.5 IC area)	40	20
Resistors	100	30
Resistor size (3 KΩ)	0.0075" x 0.090"	0.04" x 0.075"
Space taken by active and passive devices (including resistors)*	50 - 70%	35 - 50%
(% of this space taken by resistors	20%	35%)
Number of bonds (Length of bond 50 mils)	640	340
Overall process yield	95%	91%

*The remaining space is taken by the conductor network.

2.1.3.2 Hybrid Manufacturing Costs

The total manufacturing cost for a hybrid, C_H, is given, in dollars, by

$$C_H = C_{SP} + C_{AT}$$

where C_{SP} is the cost of thin or thick film substrate processing and C_{AT} is the cost of the assembly process and testing.

I. Substrate Processing

The cost, in dollars, of thin or thick film substrate processing, C_{SP}, is modeled by the following equation:

$$C_{SP} = C_S + (C_P + C_U + C_{RT} + C_{QC})\, W_r \qquad (2)$$

where W_r is an arbitrary wage rate constant in dollars/hour and all the other symbols are identified with the steps in the flow charts of Figure 2-2 or Figure 2-3. The terms in parentheses are in units of standard hours (STDH). During the follow-on program recommended in Section 3.0, additional in-process testing and rework cycles will be added to these flow charts, and mathematical provisions for determining in-process yields will be included.

Equation 2 can be rewritten as

$$C_{SP} = C_{OS}\, S_Z + (C_{OE}/Y_o e^{-C_c} + C_U + K_T\, \delta_{SR}\, \delta_R\, t_R + K_{QC}\, C_c\, S_Z)\, W_r \qquad (3)$$

The above equation is based on the following assumptions and definitions:

A. Substrate Material — Assume this cost C_S to be a function of the hybrid size factor S_Z. Define

$$C_S = C_{OS}\, S_Z$$

where C_{OS} is a proportionality constant.

B. Circuit Processing — Assume this cost, C_p, to be a function of the circuit complexity, C_c.

$$C_p = C_{OE}/Yoe^{-C_c}$$

where C_{OE} is constant with STDH dimension and Y_o is a dimensional constant. The term Yoe^{-C_c} can be considered the yield of the process.

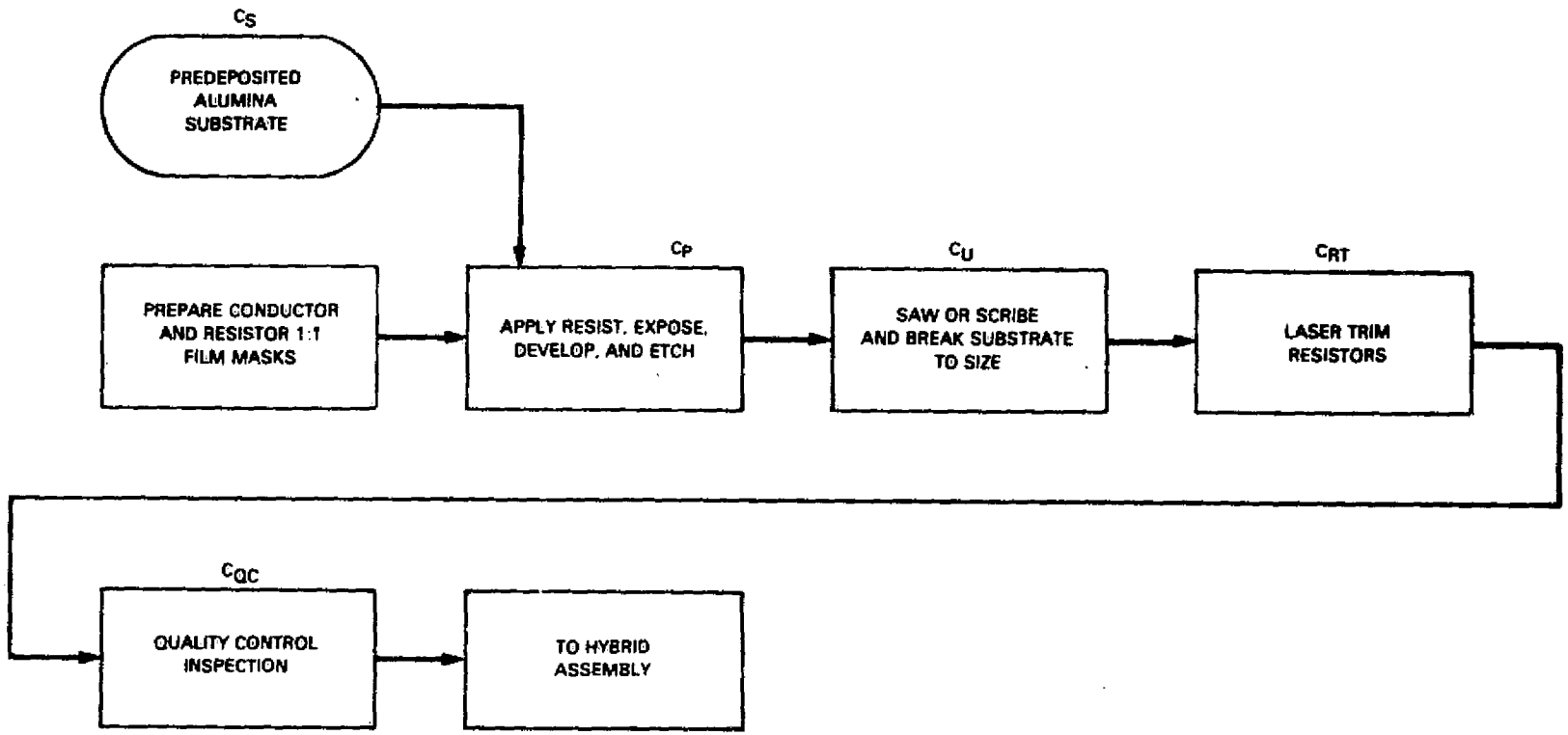


Figure 2-2. Thin film substrate fabrication.

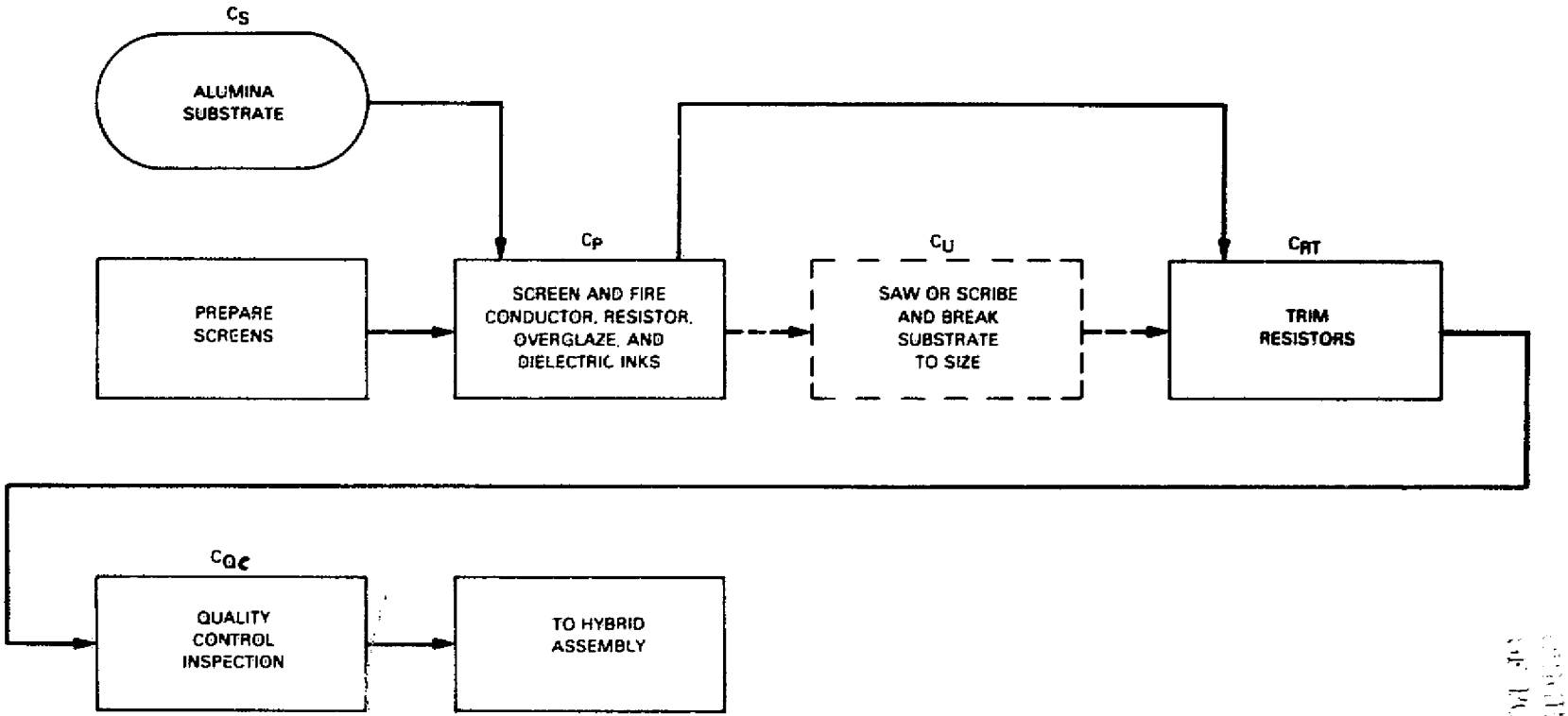


Figure 2-3. Thick film substrate fabrication.

This term can be expanded to express process yield explicitly as a function of those parameters which cause rejects (as has been done for the assembly and testing terms). The implicit form was chosen here for simplicity, since the substrate fabrication cost is a small portion of the total hybrid cost. Yield parameters will be expanded and expressed mathematically in a more detailed manner in connection with any follow-on program such as that recommended in Section 3.0.

C. Circuit Complexity — Assume this factor, C_c, as a function of the total number of chips (active and passive) per in^2, δ_c, the total number of resistors per in^2, δ_R, and maximum number of pads found on one chip, δ_{pmax}. Define this factor as

$$C_c = K_C (\delta_c + \delta_R) + K_c' \delta_{pmax}^{1.1}$$

where K_c and K_c' are two proportional constants. The exponent of the term $\delta_{pmax}^{1.1}$ has been found empirically by the best fit approach from the available data.

NOTE: C_c approaches the value 1 as the circuit complexity increases. This also means that multilayer technology should then be used.

D. Resistor Trimming — Assume this cost, C_{RT} to be a function of resistor size factor δ_{SR}, resistor density δ_R and resistor tolerance factor t_R. Define as

$$C_{RT} = K_T \delta_{SR} \delta_R t_R$$

where K_T is a constant having the dimensions of STDHxin^2. The factor t_R is taken as the inverse of the tolerance. For tolerance greater than 20 percent, t_R equals 0. The resistor size factor δ_{SR} is defined as the ratio of the average area of one resistor is the total hybrid area.

E. QC Inspection — Assume this cost to be a function of circuit complexity C_c and hybrid size factor S_Z. Define as

$$C_{QC} = K_{QC} C_c S_Z$$

where K_{QC} is a constant with STDH dimensions.

II. Assembly and Test

The cost, in dollars, of the assembly process and testing, C_{AT}, is modeled by the following equation:

$$C_{AT} = C_P + C_{CC} + C_L + (C_{PT} + C_{BS} + C_{BC} + C_{WB} + C_{ND} + C_{QC1} + C_{EPS} + C_{TROB} + C_{RWB} + C_{QC2} + C_{SL} + C'_{AT} + C_{TRQA} + C_{RWA} + C_{QC3} + C_O) W_r \quad (4)$$

where C_L is the unit cost in dollars of the package lid and all the other symbols are identified by the steps in the flow chart of Figure 2-4. The terms in the parentheses have the units of standard hours.

Equation (4) can be rewritten as

$$C_{AT} = C_{op} t_y S_Z e^{-\beta_o Q} + (\beta_1 N_{TRJ} + \beta_2 N_{TRD} + \beta_3 N_{CAP}) + n' C'_L + \left\{ C_{opt} S_Z + C_{BS} + m\alpha N_c + b + (\delta_p N_{CIC} + 2 [N_{TRD} + N_{CAP}]) \times \right.$$

$$\left. \times (1+f) \right\} + d(rN_{WB}) + K_{QC1} C_c S_Z + g(\bar{N}_{TRJ})^{0.1} C_c +$$

$$+ g' (\bar{N}_{TRJ})^{0.1} C_c + nh(g_1 N_c + g_2 N_{WB}) + K_{QC2} C_c S_Z +$$

$$+ \ell S_Z + rC_{TT} + g''(\bar{N}_{TRJ})^{0.1} C_c + n' [h' (g'_1 N_c + g'_2 N_{WB}) + C_{LR}] +$$

$$\left. + K_{QC3} S_Z + C_o \right\} \times W_r \quad (5)$$

The above equation is based on the following assumptions and definitions:

A. Package Cost — Assume this cost, C_p to be a function of package type factor t_y, hybrid size factor S_Z and purchase quantity Q. Define as

$$C_p = C_{op} t_y S_Z e^{-\beta_o Q}$$

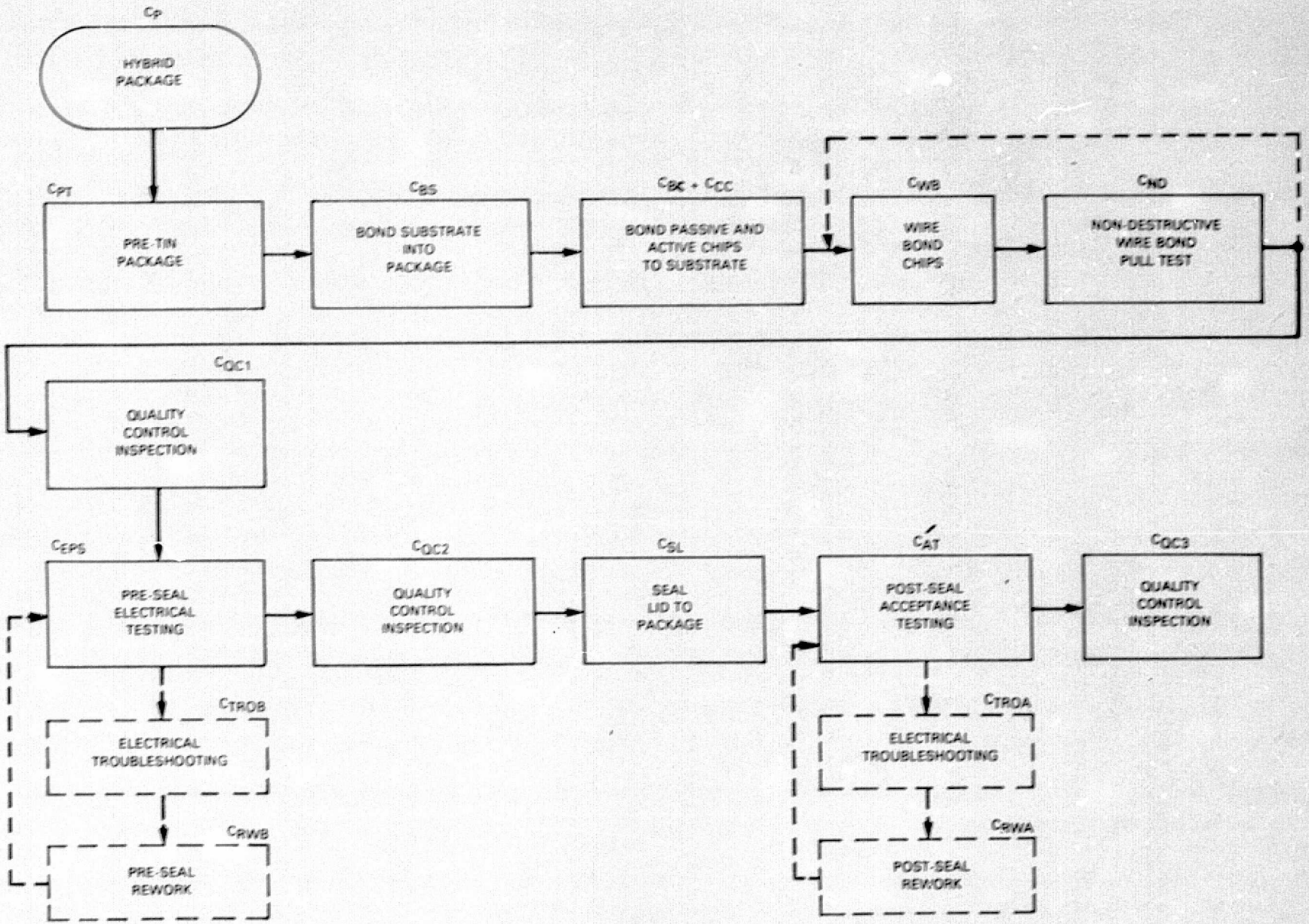


Figure 2-4. Hybrid Microcircuit Assembly and Test.

where C_{op} is a constant having the dimensions of STDH and β_o is an adimensional constant. The exponential behavior of the relationship has been deducted from the graph of Figure 2-5. (The purchase quantity was considered here because of the relatively high cost of this item.)

B. Active and Passive Chips — Assume the cost of active chips proportional to the complexity of the chip expressed as the number of transistors. Define the total chip cost as

$$C_{cc} = \beta_1 N_{TRJ} + \beta_2 N_{TRD} + \beta_3 N_{CAP}$$

where N_{TRJ} is the total number of transistor junctions in the ICs, N_{TRD} is the total number of transistors and diodes, and N_{CAP} is the total number of capacitors. β_1, β_2, and β_3 are three constants of proportionality having dimensional units of dollars.

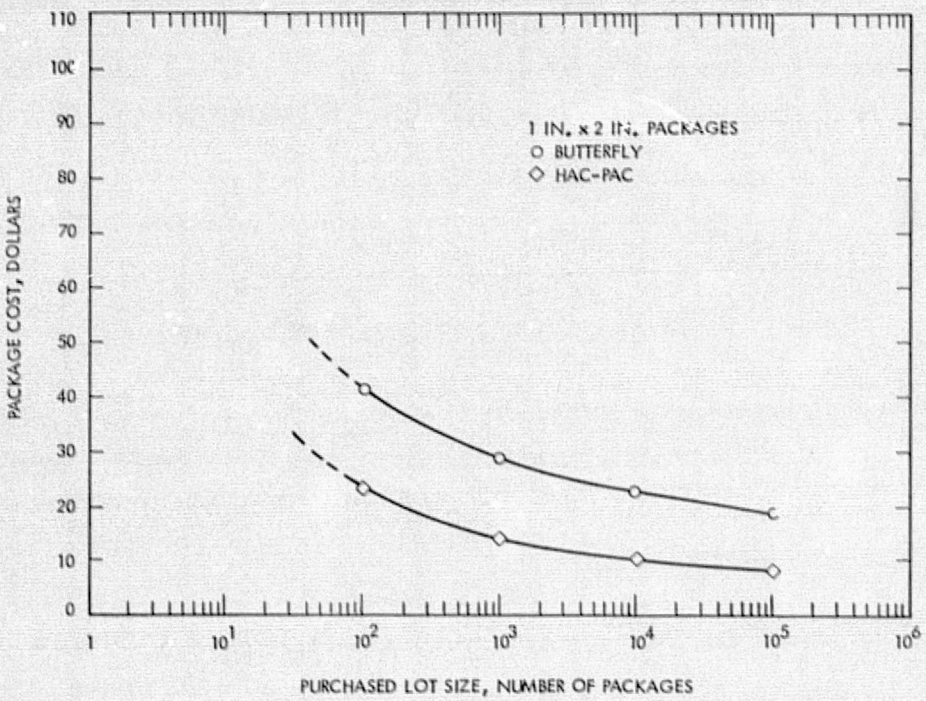


Figure 2-5. Package cost versus purchased lot size.

C. Package Lid – Define this cost, C_L, as

$$C_L = n' C'_L$$

where n' is the number of lids used for the same package. Normally $n' = 1$ but it can take other positive integer values (2, 3, etc.) when rework occurs.

D. Pre-Tin Cost – Assume this cost, C_{PT}, to be a function of the hybrid size factor, S_Z. Define as

$$C_{PT} = S_Z C_{OPT}$$

where C_{OPT} is a constant of proportionality having STDH dimensional units.

E. Bonding Chips – Assume this cost, C_{BC}, proportional to the number of chips, N_C, active and passive. Define

$$C_{BC} = m\alpha N_c$$

where m takes the value of 1 or 2 if the molytab is not or is used, respectively. The constant α has STDH for dimensional units.

F. Wire Bonding – Assume this cost, C_{WB}, to be a function of the total number of active chips, capacitors, lead connections and jumpers. Define

$$C_{WB} = b\left[(\delta_p N_{CIC} + 2\left[N_{TRD} + N_{CAP}\right])\ (1 + f)\right]$$

where δ_p is the number of pads/chips, N_{CIC}, N_{TRD} and N_{CAP} are the total number of ICs, transistors and diodes and capacitors, respectively, and f is a factor which takes into account jumper bonds and bonds to the leads of the package.

G. Non-Destructive Pull Test - Assume this cost, C_{ND}, to be a function of the total number of bonds N_{WB}, and of a factor r, which takes the value 1 or 0 for high- or low-reliability hybrids, respectively. Define

$$CND = d(rN_{WB}),$$

where d is a constant having STDH for dimensions.

H. Pre-Seal Visual QC – Assume this cost, C_{QC1}, to be a function of circuit complexity and hybrid size. Define as

$$C_{QC1} = K_{QC1} C_c S_Z$$

where K_{QC1} is a constant having STDH for dimensions.

I. Pre-Seal Electrical Test – Assume this cost, C_{EPS}, to be a function of the number of transistors/chip, $\overline{N}_{TRJ}$, and circuit complexity factor C_c. Define

$$C_{EPS} = g(\overline{N}_{TRJ})^{0.1} C_c$$

where g is a constant having STDH for dimensional units. The exponent 0.1 has been found empirically by the best fit approach from available data.

J. Troubleshooting Before Sealing – Assume this cost, C_{TROB}, to be a function of the average number of transistors/chips, $\overline{N}_{TRJ}$, and circuit complexity C_c. Define

$$C_{TROB} = g' (\overline{N}_{TRJ})^{0.1} C_c$$

where g' is a constant having STDH for dimensional units.

K. Rework Before Sealing – Assume this cost, C_{RWB}, to be a function of the number of chips, $g_1 N_c$, and bonds, $g_2 N_{WB}$, reworked. Define

$$C_{RWB} = n h (g_1 N_c + g_2 N_{WB})$$

where n is the number of reworks, and h is a constant of proportionality having the dimensions of STDH. g_1 and g_2 are adimensional and can be regarded as percentage fractions.

L. Pre-Seal QC Inspection – Assume this cost, C_{QC2}, to be a function of circuit complexity and hybrid size. Define

$$C_{QC2} = K_{QC2} C_c S_Z$$

where K_{QC2} is a proportional constant having STDH for dimensions.

M. Sealing – Assume this cost, C_{SL}, proportional to the hybrid size factor. Define

$$C_{SL} = \ell S_Z$$

where ℓ is a proportional constant having STDH for dimensions.

N. Post-Seal Acceptance Test – Assume this cost, C'_{AT}, proportional to the reliability level, r. Define

$$C'_{AT} = rC_{TT}$$

where C_{TT} is a constant expressed in STDH units.

O. Troubleshooting After Sealing – Assume this cost, C_{TROA}, to be a function of the average number of transistors/chips, $\bar{N}_{TRJ}$, and circuit complexity, C_c. Define

$$C_{TROA} = g'' (\bar{N}_{TRJ})^{0.1} C_c$$

where g'' is a constant in STDH units.

P. Rework After Sealing – Assume this cost, C_{RWA}, to be a function of the number of chips, $g_1 N_c$, bonds, $g_2 N_{WB}$, and lids reworked. Define

$$C_{RWA} = n' [h' (g'_1 N_c + g'_2 N_{WB}) + C_{LR}]$$

where n' is the number of reworks, and C_{LR} is the cost in STDH needed to rework one lid.

Q. Final QC Inspection – Assume this cost, C_{QC3}, proportional to the hybrid size. Define

$$C_{QC3} = K_{QC3} S_Z$$

R. The constant, C_o, expressed in STDH units, has been added into equation 5 to take into account other steps of the process which have not been reported in the flow chart because of their small impact on the manufacturing cost of the hybrid.

Factors expressing yield in the Assembly and Testing terms have been expressed explicitly as a function of those parameters which cause rejects. The terms C_{TROB}, C_{RWB}, C_{TRDA}, and C_{RWA} contain these parameters.

2.1.3.3 Calculation of the Manufacturing Cost for a Typical Hybrid

The total manufacturing cost for a typical hybrid is calculated by substituting equations 3 and 5 into equation 1, and by giving to the symbols their respective quantitative values which have been reported earlier in Table 2-10 and Table 2-11.

Substrate Processing Cost. This cost is calculated by applying equation (3).

a. Thin Film

$$C_{SP} = 15 + (0.132 + 0.024 + 0.04 + 0.018) \times 12$$
$$= 15 + 2.5$$
$$= 17.5 \text{ dollars}$$

Observation I - The cost of the metallized substrate material is approximately six times the manufacturing cost.

b. Thick Film

$$C_{SP} = 0.32 + [0.026 + 0.024 + 0.01 + 0.01] \times 12$$
$$= 0.32 + 0.84$$
$$= 1.16 \text{ dollars}$$

Observation II — Manufacturing cost is 2.6 times the substrate material cost.

Assembly and Testing. This cost is calculated by applying equation (5).

$$C_{AT} = 10.70 + \underset{(105)}{192} + 1.70 + \{0.0165 + 0.12 + \underset{(0.042)}{0.084} + \underset{(0.224)}{0.425} + \underset{(1.56)}{2.95} + 0.022 + 0.064 + 0.128 + 2.0 + \underset{(.53)}{1.0} + 0.093 + 1.0 + \underset{(0.09)}{(0.22 + 1.2)} + 0.22 + 0.01 + 0.25\} \times 12$$

$$= 204.4 + \{9.8\} \times 12$$

$$= 204.4 + 117.6$$

$$= 322 \text{ dollars} \qquad (8) \text{ thin film hybrid}$$

$$= 117.4 + \{7.56\} \times 12$$

$$= 117.4 + 90.72$$

$$= 208.12 \text{ dollars} \qquad (9) \text{ thick film hybrid}$$

Note: The numbers in parentheses above other numbers in the thin film hybrid equation are the respective values for thick film technology. Terms in the assembly and testing equation which depend upon the type of technology used are easily identified in this way.

Observation III – The cost of materials, namely package, chips, and lid, is about 1.5 times the other costs.

Observation IV – The cost of testing is about 41 percent the total assembly and testing cost.

Observation V – The cost of troubleshooting and rework is about 55 percent the total assembly and testing cost.

Observation VI – The cost of assembly and testing is 18.5 times the cost of substrate fabrication for thin film hybrids, and 180 times the cost of substrate fabrication for thick film hybrids.

Total Hybrid Manufacturing Cost

This total cost is calculated by adding equations (6) and (8) for thin film technology and equations (7) and (9) for thick film technology. Therefore,

$$C_H = C_{SP} + C_{AT}$$

$$= 17.5 + 322 = 339.5 \text{ dollars} \quad (10) \text{ thin film hybrid}$$

$$= 1.16 + 208.12 = 209.28 \text{ dollars} \quad (11) \text{ thick film hybrid}$$

A rough estimate of the total manufacturing cost as a function of the number of hybrids produced per year can be obtained by using the equation

$$C_H = 1.54 \times 10^3 \, e^{-1.26 \times 10^{-5}} \, V, \quad 1,500 < V < 150,000 \qquad (*)$$

where V is the number of hybrids produced in one year.

The hybrid cost expressed in this way is comprehensive of the non-recurring costs (masks, screens, engineering assistance, tec.). These costs have a large impact on the final low-volume production hybrid cost.

2.1.3.4 Effects of Tape Chip Carrier (TCC) Technology on the Hybrid Manufacturing Cost

The effects of substituting TCC technology for chip-and-wire assembly are calculated by inserting key comparison factors or "operators" into the basic equations derived earlier. Such operators can take the form of decimal numbers; e.g., 0.9, 0.8, 0.7, applied as multiplying factors which serve to determine the degrees of cost reduction involved.

Obviously, the cost effects of TCC usage can vary widely depending upon the specific operator chosen, and this choice becomes vital to the analysis. Those operators utilized as preliminary examples in this report have been chosen on the basis of in-house discussions with personnel who have been exposed to TCC technology for varying times, and who have varying levels of management and/or "hands-on" experience with this concept. The results of applying such factors is speculative at this time, but confidence in their

integrity will increase as they are revised during the remainder of the contractual time period. In any follow-on effort associated with this program, Hughes will generate the maximum feasible amount of quantitative/derivation data to justify the particular operators chosen at that time for determination of TTC comparative cost factors.

Assumptions and Definitions

Assume that the pre-seal electrical test cost, C_{EPS}, the rework before sealing cost, C_{RWB}, and the chip bonding cost, C_{BC}, are affected. Redefine these quantities as

$$C'_{EPS} = (0.7)\, C_{EPS}$$

$$C'_{RWB} = (0.6)\, C_{RWB}$$

$$C'_{BC} = (0.9\, C_{BC}$$

Assume the total cost of testing the chips, C_{TC}, (with TCC), proportional to the total number of ICs, N_{CIC}. Define this cost

$$C_{TC} = u\, N_{CIC}$$

where u is a constant expressed in STDH units.

Define a new IC chip cost, the bumping cost, C_{BP}. Assume the total cost, proportional to the number of ICs, N_{CIC}.

$$C_{BP} = u_B\, N_{CIC}$$

where u_B is the cost in dollars to bump one chip (having 16 pads)
The cost of making wire bonds to ICs is eliminated, $b\delta_p N_{CIC} = 0$.

Assume the non-destructive pull testing cost, C_{ND}, on wire bonds substituted with some other equivalent non-destructive test cost, C'_{ND}. Define

$$C'_{NP} = 0.30\, C_{ND}$$

Then the total cost variation if TCC is used in the manufacturing of hybrids is

$$C_{TCC} = [(C'_{EPS} - C_{EPS}) + (C'_{RWB} - C_{RWB}) + (C'_{BC} - C_{BC}) + (C'_{WB} - C_{WB}) + (C'_{ND} - C_{ND}) + C_{TC}] \times W_r + C_{BP}$$

$$= (-0.019 - 0.4 - 0.0084 - 0.21 - 2.065 + 0.55) \times 12 + 4$$

$$= -25.8 + 4$$

$$= -21.8 \text{ dollars/hybrid}$$

Observation VII - Based on the operators used at this time, TCC usage represents a 6.4 percent savings on the total thin film manufacturing cost and a 10.4 percent savings on the total thick film manufacturing cost. (No substantive decision or opinions should be drawn from such data at this time. As discussed earlier in this Section, more precise operator determination is recommended as a part of any associated follow-on activities which may take place).

2.1.3.5 Wafer/Chip Bumping Cost Analysis

A significant portion of the total TCC processing and cost package relates to wafer bumping, as indicated in Flow Chart No. 13 of Appendix "A". A simplified wafer bumping process flow chart is shown in Figure 2-6 which also includes typical per-wafer processing time for each operation. Using this information, the wafer/chip bumping cost is calculated as follows:

- Total manufacturing bumping cost/wafer:

$$C_{BPw} = (1.0 + 1.0 + 0.5 + 0.084 + 0.17 + 1.5 + 0.075 + 0.25 + 1.5 + 0.25 + 0.50 + 1.0) \times 12 \text{ \$/hour} + 1.00$$

$$= (7.83 \text{ Hr}) \times 12 \text{ \$/hour} + 1.00 = 95 \text{ Dollars}$$

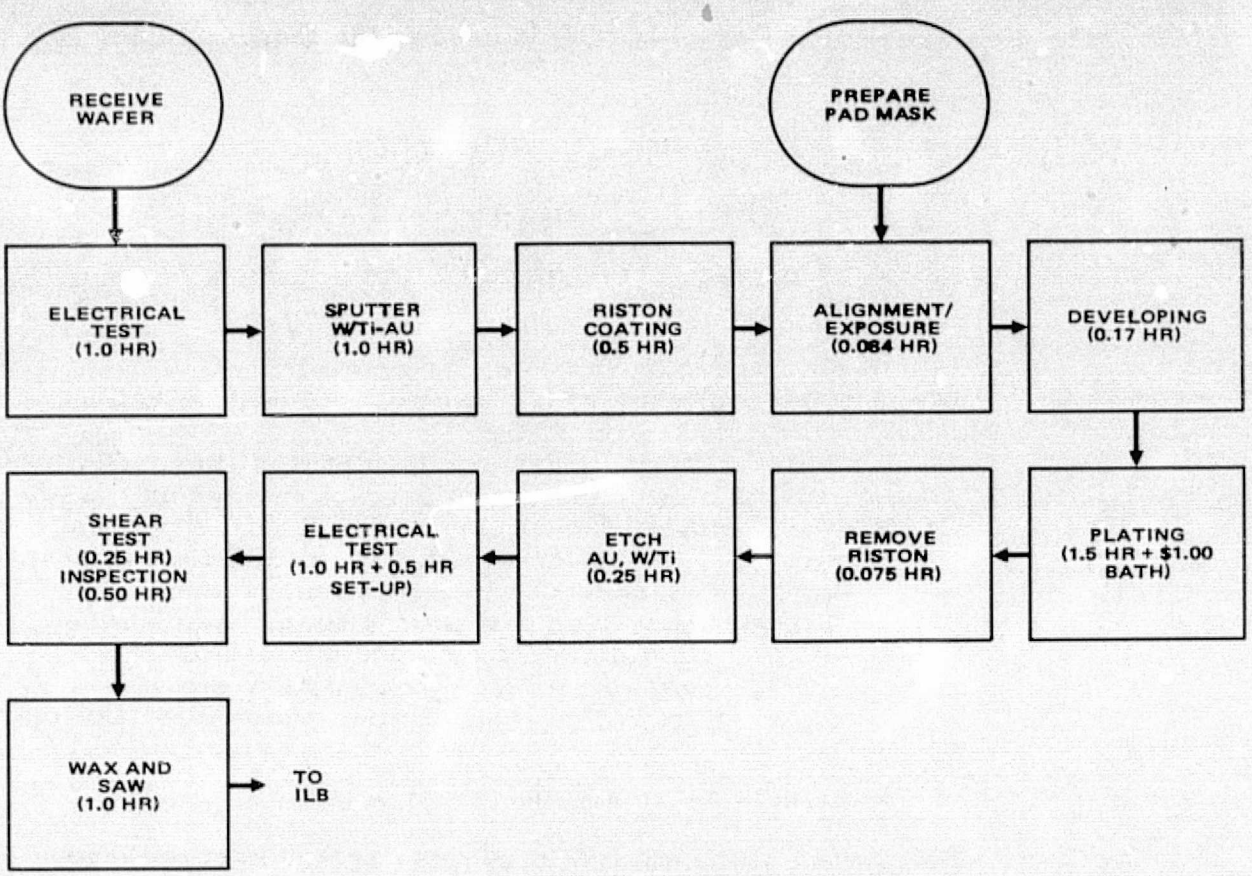


Figure 2-6. Wafer bumping process.

Then, the manufacturing bumping cost/chip is:

- 0.095 $/chip (when 50 x 50 mils chips, 1000 chips/wafer are produced with a process yield of 90 percent)
- 0.63 $/chip (when 150 x 150 mils chips, 150 chips/wafer are produced with a process yield of 5 percent)
- Non-Recurring Cost: $200.00 probe card
  $250.00 mask

The number of bumped chips to be produced in order to amortize the non-recurring cost can be found as follows:

Definition: Amortization volume is that number of bumped chips produced so that the non-recurring cost per chip is small compared to the total manufacturing cost.

Let 10 percent of the recurring manufacturing cost be the upper limit of the non-recurring cost/chip that the factory can allow to add to the manufacturing cost/chip. Then,

$$\frac{\$450}{0.1 \times 0.095} = 45,000$$ (number of 50 x 50-mil chips necessary to be produced before the cost/chip is $0.105/chip

and

$$\frac{\$450}{0.1 \times 0.63} = 7,143$$ (number of 150 x 150-mil chips necessary to be produced before the cost/chip is $0.70/chip

2.1.3.6 Effect of One LSI Chip on the Hybrid Manufacturing Cost

Assumptions and Defintions

Assume that one LSI chip substitutes n-m ICs, where n is the total number of ICs and m is the number of ICs left in the hybrid. Assume also that this substitution will reduce the total number of chips, N_c, by X percent and the total number of resistors, N_R, by Y percent. Define

$$n-m = 50\% \, n \quad , \; n = N_{CIC}$$
$$N'_C = 50\% \, N_c$$
$$N'_R = 50\% \, N_R$$

Note 1. Reduction in the number of components can vary between 30 percent - 80 percent depending upon the circuit application.

Note 2. As a consequence of the above assumptions, the circuit complexity factor, C_c, will change.

Assume that the total number of wire bonds, N_{WB}, will be reduced by Z percent. Define

$$N'_{WB} = 50\% \, N_{WB}$$

The Intel 8080 microprocessor with 40 pads (δ_p) and about 5,000 transistor junctions, priced at $7.40 (chip size about 0.167 x 0.194 in.), has been taken as a Reference LSI.

The total cost of the hybrid manufacturing process when a LSI is introduced into the circuit is given by equations 3 and 5 substituted into equation 1 with the above parameter changes.

$$C_H = C_{SP} + C_{AT}$$

$$= [15 + (0.144 + 0.024 + 0.02 + 0.014) \times 12] +$$

$$+ \{10.70 + 103.4 + 1.70 + [0.0165 + 0.12 + 0.021 + 0.112 +$$

$$+ 1.42 + 0.026 + 0.124 + 0.153 + 3.85 + 0.5 + 0.093$$

$$+ 1.93 + (0.11 + 1.2) + 0.22 + 0.01 + 0.25] \times 12\}$$

$$= [15 + 2.4] + \{115.8 + [10.15 \times 12]\}$$

$$= 17.4 + 115.8 + 121.8$$

$$= 17.4 + 237.6$$

$$= 255 \text{ dollars} \qquad \text{(13) thin film hybrid}$$

$$= 1.16 + \{69.8 + [7.83 \times 12]\}$$

$$= 1.16 + \{69.8 + 94.0\}$$

$$= 1.16 + 163.8$$

$$= 164.96 \text{ dollars} \qquad \text{(14) thick film hybrid}$$

The savings are obtained by comparing equation (13) to equation (10) and equation (14) to equation (11).

ΔC_H = -85 dollars — thin film hybrid

ΔC_H = -44.84 dollars — thick film hybrid

Observation VIII - This represents a 25 percent savings on the total thin film manufacturing cost and a 27 percent savings on the total thick film manufacturing cost.

Observation IX - By adding a LSI device, the manufacturing hybrid costs along remain about the same. A considerable savings is obtained however, in material (chips) cost.

2.2 TASK III PACKAGING IMPLEMENTATION

This study required that a demonstration program be performed to adapt LSI devices on with tape chip carriers for hybrid packaging. Program requirements included low volume applications involving testing, screening, and burn-in on tape carriers, and a demonstration of processing compatibility with high density hybrid technology.

The semiconductor devices used as demonstration vehicles were:

1. TTL SSI Device - Type 5400 Quadruple 2-Input Positive - NAND-Gate; 10 milliwatts dissipation; 0.040-inch x 0.032-inch, with 14 pads.
2. CMOS LSI Device - Type 1824 32 x 8 Static RAM chip; 500 milliwatts dissipation; 0.120-inch x 0.160-inch, with 18 pads.
3. ECL LSI Device - Type UDA/MUX; 1.5-watts dissipation; 0.180-inch x 0.190-inch, with 82 pads.

Tape carriers were fabricated for each of these device types, and all three chip types were post-processed to add gold bumps. Inner-lead bonding (ILB) was accomplished for all devices, but outer-lead bonding (OLB) was performed on the TTL and CMOS devices only.

2.2.1 Tape Process/Materials Evaluation

A flow diagram for the fabrication of tape carriers is shown in Figure 2-7.

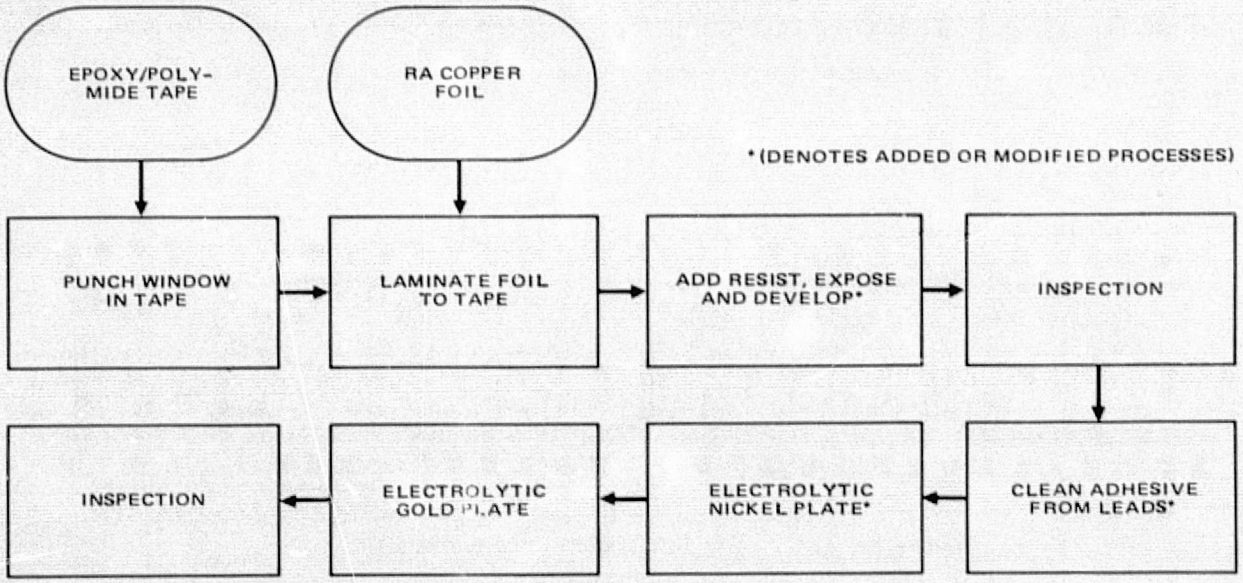


Figure 2-7. Flow diagram - modified tape processing.

The processing used to fabricate tape carriers during this program reflects significant modification of previously-used processes. These modifications, which correct faults, improve yields, and/or solve encountered problems, are explained in the subsequent description.

A single layer of wet photoresist is applied to the copper side of the film, after which a tape photomask (such as that shown in Figure 2-8) is aligned to the sprocket holes. The combined elements are exposed, and the resist is developed. A dry resist film then is laminated to the back side of the copper to prevent etching through, and to protect the leads after etching from mechanical damage which might occur during subsequent processing. The laminator used for this operation is shown in Figure 2-9. Previously, wet resist was used on both sides of the film, but this was unsatisfactory because it sometimes became tacky during spray etching, and the leads tended to become damaged when the etched film was removed from the back-up plastic sheets used for film transport through the machine.

The copper leads are defined by means of the Chemant Model 547 Spray Etcher, shown in Figure 2-10. The etch reagent is heated to 130°F for this operation. The tapes are spray-rinsed in water and partially dried with an air knife. During this sequence, the epoxy adhesive on the tapes tends to become somewhat soft, and the leads can be moved from their true locations if sufficient force is applied. Once the adhesive dries however, it becomes hard again and regains its strength. At this point, the leads are held securely in position by the adhesive, and by the dry-resist film backing. Both the wet resist residual on the front side of the etched copper and the

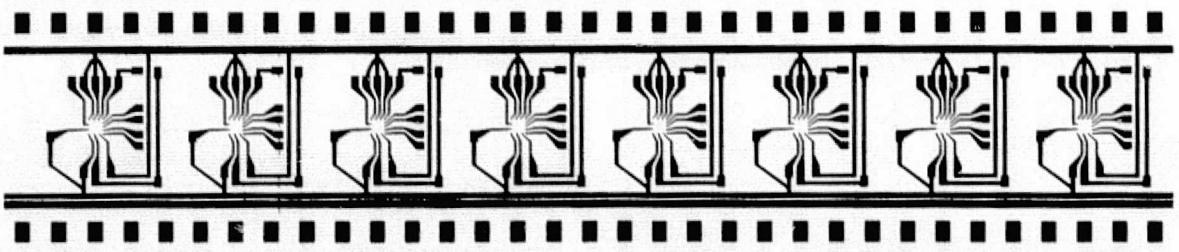


Figure 2-8. Typical tape photo-mask.

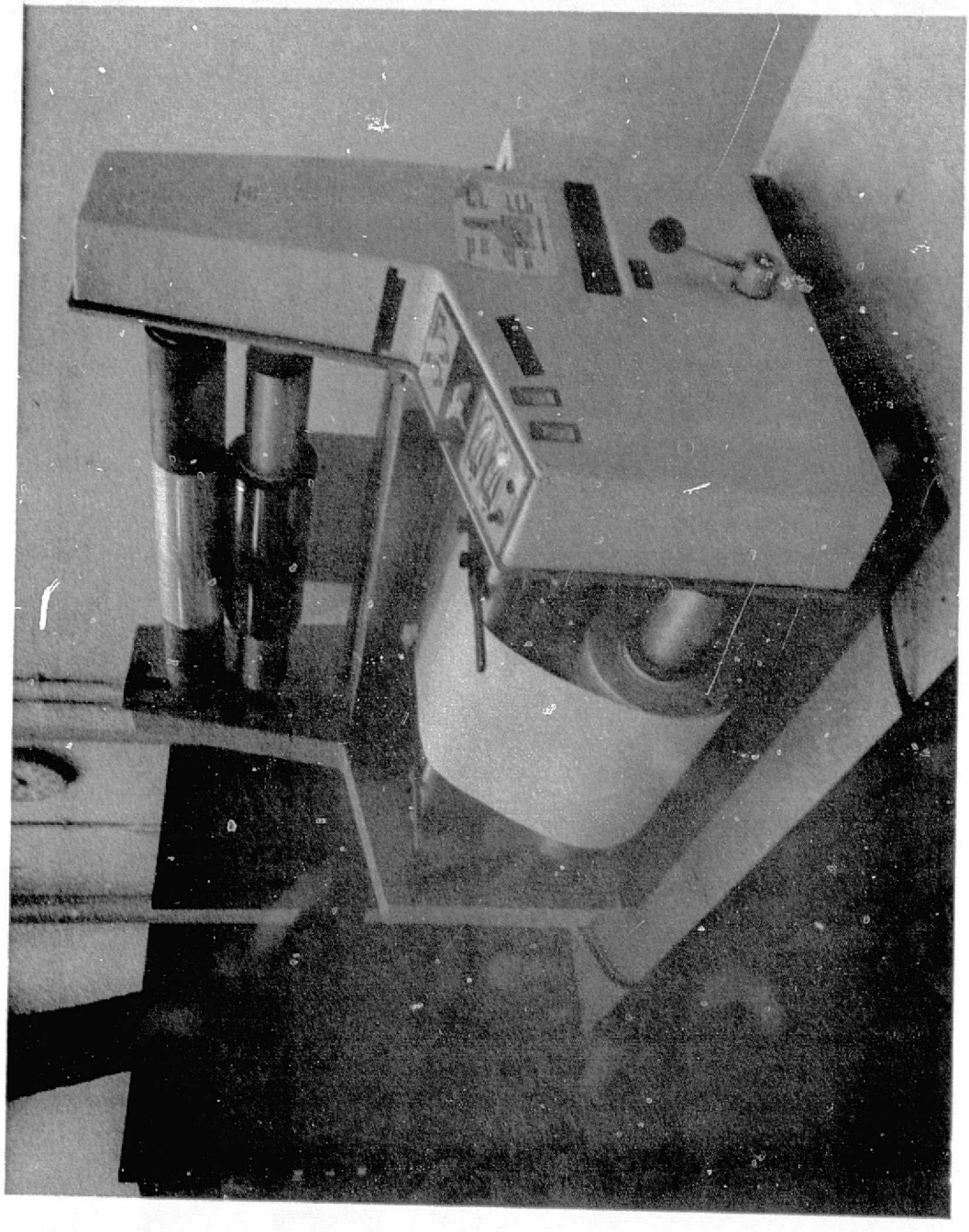


Figure 2-9. Dry film laminator.

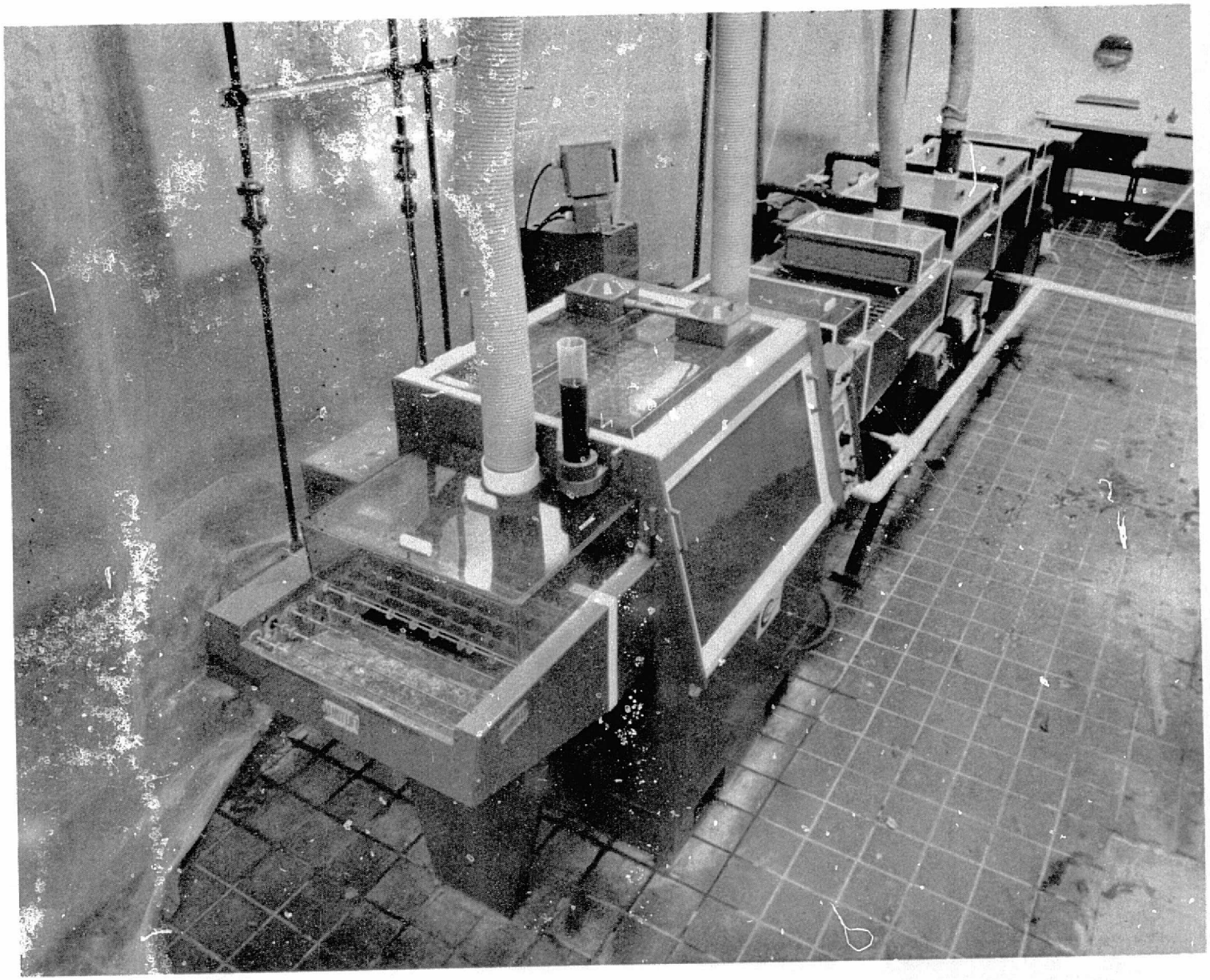


Figure 2-10. Chem cut Model 547 spray etcher.

undeveloped dry resist supportive film on the back side are removable in their respective stripper solutions; revealing the completed etched copper tape pattern, ready for plating. The photograph of Figure 2-11 shows a completed tape carrier position for the 82-pad ECL device (Device Number 3 in paragraph 2.2.0 above), processed in this manner. It is aligned over a suitably-bumped chip and a hermetic chip carrier package, for which this particular tape pattern layout was designed.

It is recognized that usage of dry resist film for tape carrier backing adds some material expense. In a production operation, this resist film cost will be less than 2¢ per chip position; an amount which may be significant in quantities of millions of chips per month (typical in commercial TCC/DIP production operations). For lower quantity military-grade hybrid microcircuits however, the chip quantity used per month is far less, and only a small percentage of this total usage is likely to utilize TCC technology within the next several years. Hughes already is investigating less expensive

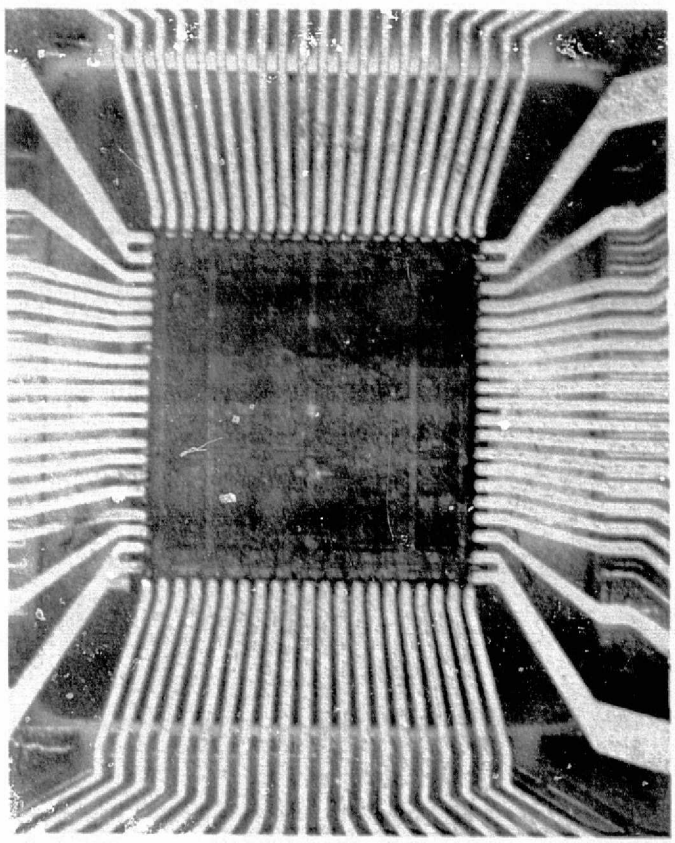


Figure 2-11. Tape carrier for 82-pad ECC devices aligned over hermetic chip carrier.

material for use as a tape carrier lead support during etching operations. This work, together with related technology involving potentially removable lead support membranes for usage within the window area, is outlined below, and will be described more fully in connection with any follow-on contractual activities which might result from the recently-completed program.

One-micron nickel plating has been added to the process sequence. Temperatures approaching 500°C are used to inner-lead-bond the tape leads to bumped devices. During this bonding, the subsequently-added gold plate and the copper leads rapidly would interdiffuse should nickel not be used. This adversely would affect the corrosion resistance and bondability of the leads. The nickel layer between the gold and copper prevents such interdiffusion and maintains lead integrity.

Electrolytic gold is plated over the nickel to facilitate inner-lead bonding to bumped devices, and to add corrosion resistance to the tape carrier metallization. The thickness of the gold deposit is 50 to 100 microinches, plated at a current density of five amperes-per-square.

Lead Support Membranes - Damage to tape carrier leads during processing affects yield adversely, especially for multiple-lead tapes such as those used with MSI or LSI devices. The leads overhang the windows in the polyimide film 100 mils or more, and they easily become bent or snagged so that alignment with their respective bumps becomes difficult or impossible. A support ring, located near the lead ends, would minimize such lead damage, as indicated in Figure 2-12. A ring can be made for this purpose by punching the polyimide in this manner before laminating with copper. An approach such as this may be used where organics are permitted inside the package. Special tape punching operations are required however; this will bring about tooling cost increases, and also will tend to complicate future tape standardization efforts. In addition, organics generally are not permitted within high-reliability packages. Such packages require a support ring that readily is removable after inner-lead bonding but before package sealing. A temperature-resistant photosensitive material that is solvent-soluble would be suitable. As indicated earlier, Hughes plans to investigate the usage of such materials and develop appropriate processes during proposed follow-on efforts related to TCC technology.

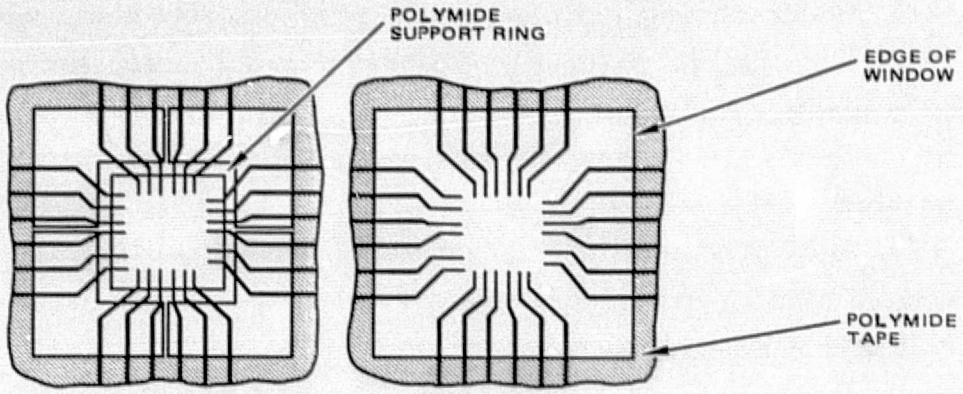


Figure 2-12. Tape chip carrier positions with and without polyimide support ring.

2.2.2 Wafer Bump Process Materials Evaluation

The flow diagram for wafer bump processing is shown in Figure 2-13. A new step has been added to the bump processing utilized earlier in this program, and refinement of previously-existing steps has occurred.

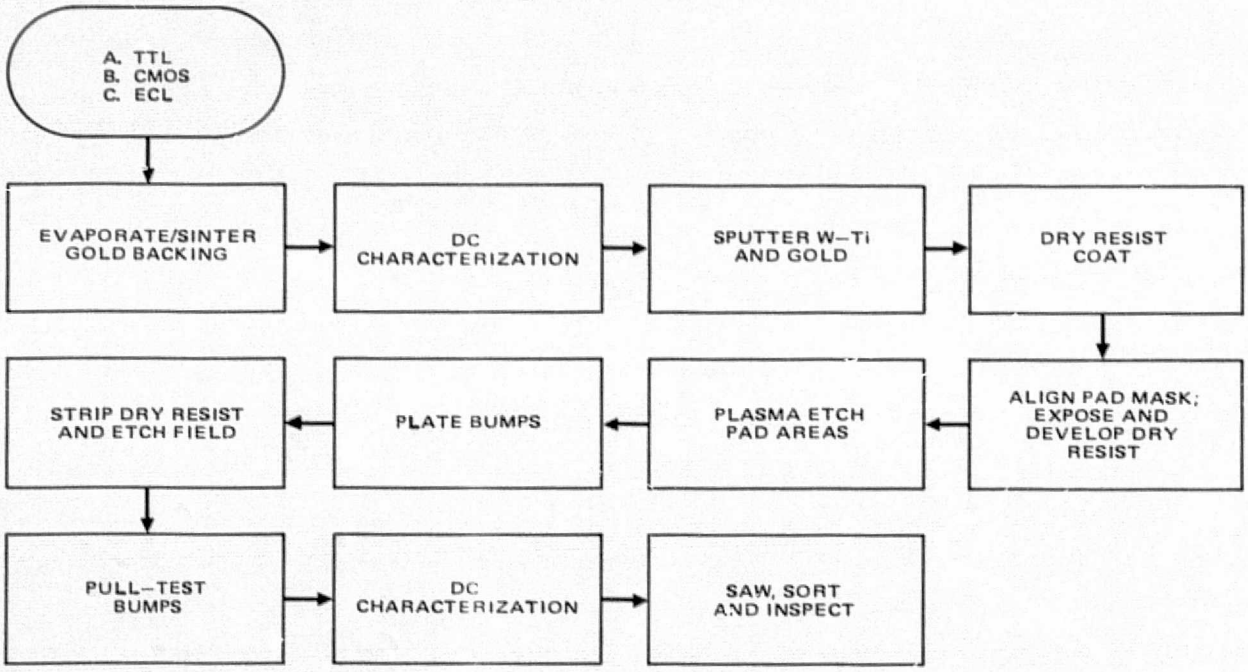


Figure 2-13. Bump process flow diagram.

Eutectic die attachment often is necessary to promote heat transfer and replace usage of organic materials in hybrid microcircuits, and particularly in hermetic chip carriers (HCCs). Prior to DC characterization of the devices to be bumped and subsequently die-bonded with eutectic material, gold is evaporated on the back of the wafer and sintered at temperatures in excess of 350°C to form a metallurgical junction. Electrical testing is performed after gold backing in case changes occur in DC characteristics as a result of this sintering step.

Barrier Layer Application - After gold backing (where required) and electrical characterization, the aluminum-metallized and CVD-glassivated wafers are sputter-cleaned, and a 3500 Å-layer of 90% tungsten - 10% titanium alloy is sputtered over the wafer at room temperature, followed by a 2000 Å-layer of gold. The tungsten-titanium layer assures adhesion of the gold to the aluminum pads, while acting as a barrier to diffusion between the gold and aluminum. Pad adhesion has been excellent to date, and there have been no problems with gold-aluminum diffusion. Equipment at Hughes utilized for this process includes MRC Model 8802, and Perkin-Elmer Model 4400 Sputtering Machines.

Wafer Coating - The sputtered wafers next are coated on both sides with 1.8-mil aqueous dry resist, using a commercial laminator such as that shown in Figure 2-9. The applied resist is exposed after it is aligned carefully with a special light-field mask, which delineates only the device pads (approximately one-mil larger on each side than the via holes in the protective CVD glass coating). A meniscus of dry resist sometimes remains at the bottom of the developed holes; this can be removed by application of developer with an air brush. On the few occasions where the resist is not completely removed in this manner, plasma etching can be used. Excessive use of plasma etch however, can cause erosion of the dry resist surfaces and hole edges over the pads.

The dry resist film must be trimmed close to the wafer edges so that it will fit into the mask aligner prior to exposure. When so trimmed, the resist film tends to lift away at the wafer edges. For this reason, these edges must be touched up with wet resist so that excess plating current is prevented from flowing, and spurious plating is minimized.

Wafer Plating - Both conventional and pulse-plating techniques have been used at Hughes to form gold bumps on wafers. Conventional plating with 3 to 5 amperes-per-square-foot produces ductile, bondable bumps which are fine-grained, and which have a relatively smooth texture, as indicated in Figure 2-14. Wafers plated with higher current densities have yielded bumps that are large-grained and coarse in texture, with many voids, as shown in Figure 2-15.

Some difficulty has been experienced in attaining optimum bump height uniformity. Approximately 85% of the bumps generally are within four microns of the desired height, while the balance may vary in height by 5 to 20 microns. The major cause of such variations was found to be gas bubbles developing within the dry resist windows during plating. Where such bubbles are present, the plating solution is prevented from coming into contact with all or part of the pad/bump. Higher circulation rates of the bath, and increased mechanical agitation of the wafer have improved this situation.

Pulse plating and fountain spray plating were evaluated as bump forming methods. Pulse plating resulted in bumps which were smoother and

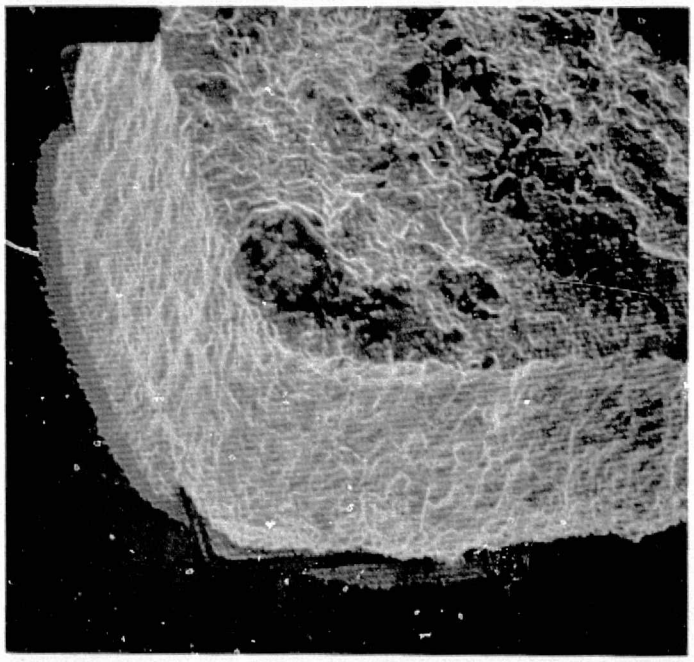


Figure 2-14. Smooth, dense, fine-grained gold bump plated at a current density of five amperes per square foot.

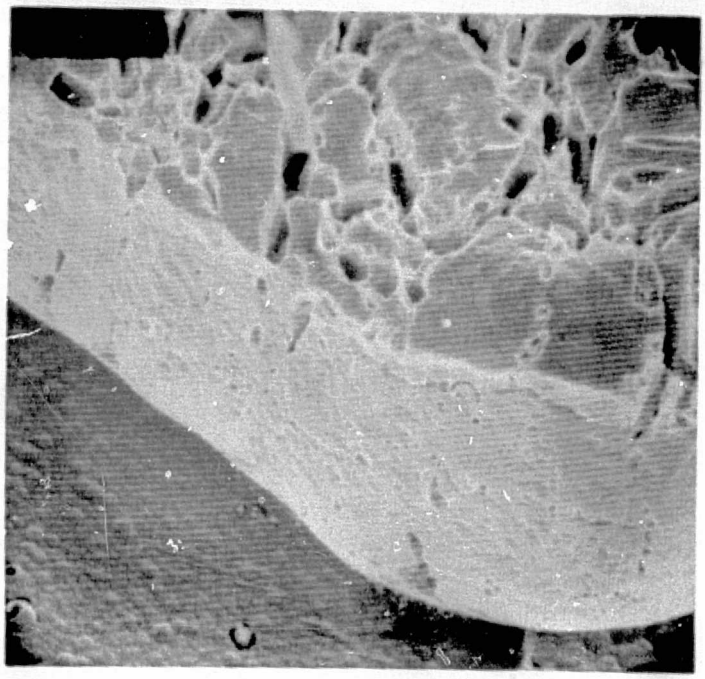


Figure 2-15. Coarse-grained, porous bump plated at a current density of 20 amperes per square foot.

more fine-grained than those attainable with conventional plating. Height uniformity was only slightly better however, while most of the resulting bumps were too hard for satisfactory inner lead bonding, as indicated in Table 2-13.

An outside source for fountain spray plating of bumps is being evaluated. This process differs from the other two in that the wafer is suspended above the bath rather than immersed in it. The bath is sprayed upward and impinges perpendicular to the wafer face.

This process will be characterized further during any follow-on effort which results from the recently-completed program.

TABLE 2-13. KNOOP HARDNESS OF PLATED BUMPS

Device Type	Plating Process	Plated By	Knoop Hardness Number (10-gm Load)
1824 CMOS RAM	Conventional	Hughes	38-43
1824 CMOS RAM	Pulse-Plating	Hughes	65
TTL 5400*	Conventional	Fairchild	28-32
*These devices were purchased with bumps already added by the vendor.			

Resist/Field Removal - The undeveloped dry resist is removed from the wafer, after which the sputtered gold is removed with a commercial stripper (Auro-Strip). The tungsten-titanium layer then is stripped with hydrogen peroxide. During this process, step damage was noted on the Type 1824 CMOS RAM devices. Devices inner-lead-bonded to tape were failing to pass functional electrical testing. Investigation revealed that when plated bumps were slightly misaligned with respect to the aluminum pads, gold etch solution would penetrate through fissures in the tungsten-titanium layer at the glass window edges, as shown in Figure 2-16. The aluminum pad was dissolved by the etching, after which the fragile tungsten-titanium layer buldged upward and was washed away (Figure 2-17). It is believed that the fissures were caused by poor step coverage by the sputtered layers, a condition aggravated by differential etch rates of the two CVD glass layers covering these particular devices. The effect is diagrammed in Figure 2-18.

Low bump yields have occurred only on wafers having plated bumps which are misaligned, and which therefore do not cover the entire pad area; as indicated in Figure 2-19. This situation was remedied by more careful fabrication, checkout, and alignment of the plating mask. When this was accomplished, the gold bumps filled the fissures and protected the pads from gold etchant solution. The problem becomes less evident when bipolar devices are used, since such wafers generally require less phosphor doping of the CVD glass layer, and the reverse-slope step profile thus is avoided.

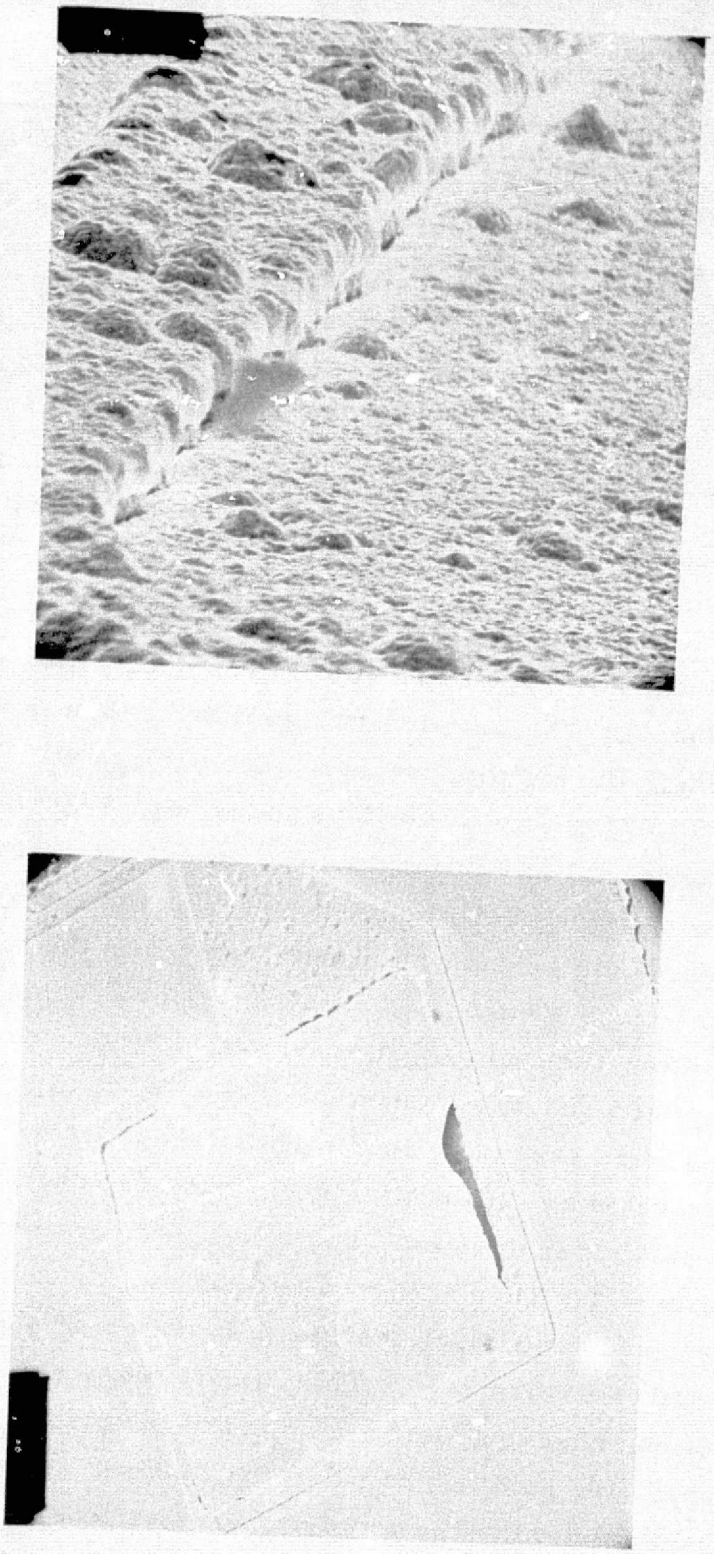


Figure 2-17. Tungsten-titanium barrier layer lifting free of chip after aluminum pad underneath is etched away.

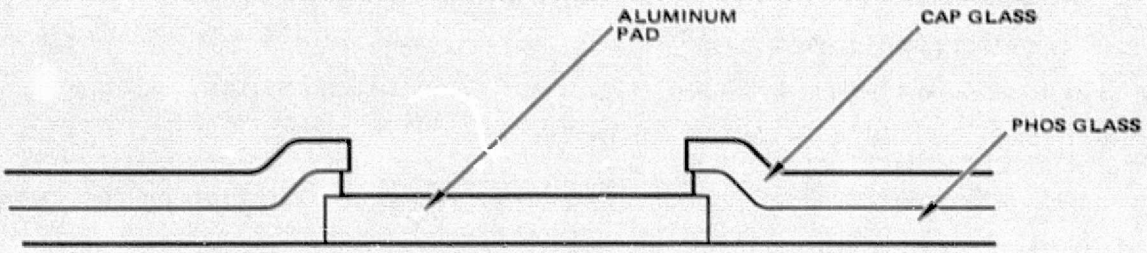


Figure 2-18. Undercut of the phosphorous glass due to differential etch rates. Undercut will cause poor step coverage of subsequent layers.

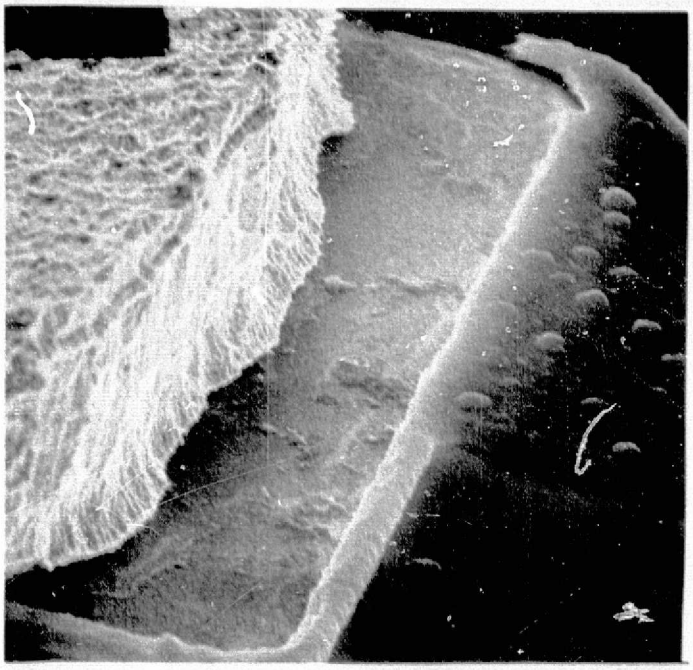


Figure 2-19. Pad area exposed due to misaligned bump. Aluminum pad is etched away.

It later was determined that the bump misalignment was caused by small cumulative errors in the pad location mask used to expose the dry resist. A new error-free mask has been made, and wafers with properly aligned bumps have been produced. It is not expected that dissolution of aluminum pads will be a problem in the future.

Bump Strength - Bump strength is measured after stripping the resist, and after etching to remove the gold and tungsten/titanium sputtered "field" layers. A special monitored push-off needle is used for destructively-testing bump adhesion through shear sampling. A minimum value of 100 grams for all tested bumps is a lot acceptance requirement. Leads also have been attached to bumps by inner-lead bonding, and pull-tested in shear. The average pull strength typically runs 45 grams, with a high reading of 80 grams and a low of 35 grams. With a 1.4-mil x 4-mil beam cross-section, the most prevalent failure point has been the interface between the bump and lead surfaces. Although these data are satisfactory, it is expected that further bump process/equipment optimization will shift more failure points to the leads, with a resulting improvement in strength.

2.2.3 Inner-Lead-Bonding Evaluation

Inner lead bonding has been demonstrated successfully for the 14-pad TTL and 18-pad CMOS devices. The bonded CMOS devices are shown in Figure 2-20. Shorts between bumps on pads 1 and 2, 3 and 4, and 17 and 18 on the CMOS device (Figure 2-21) have caused the most problems in bonding to date. These pairs of pads are too close (2 mils or less) to attain high yields from gang bonding. An additional two-mil space between the pads would make this device easier to bond with high yields. As TCC technology becomes more widely used in the future, it will become more practical to publish design guidelines defining minimum acceptable semiconductor pad spacings, and to legislate their use by device designers.

The TTL Type 5400 devices were relatively trouble-free during bonding. The bumps on these devices (purchased in a bumped form fror

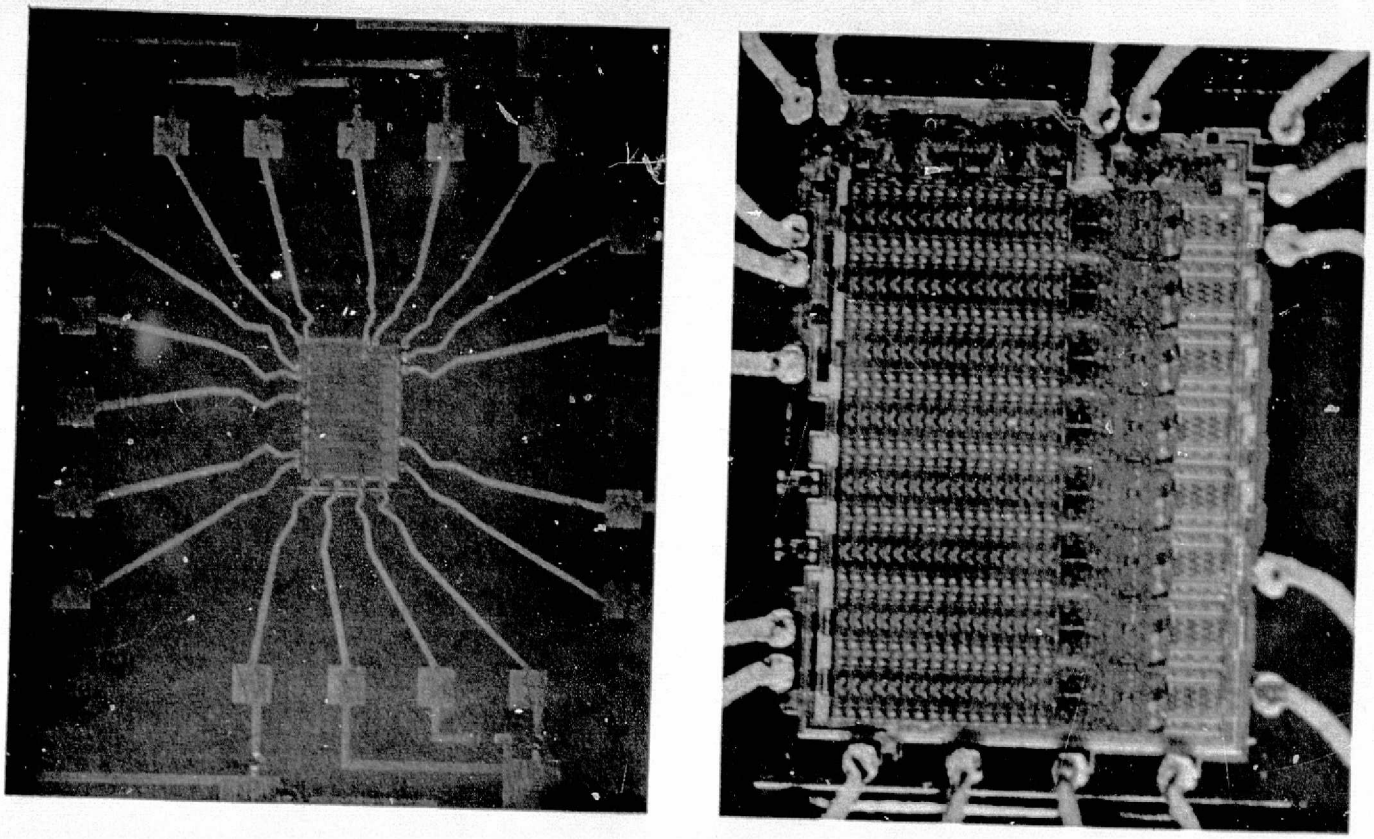
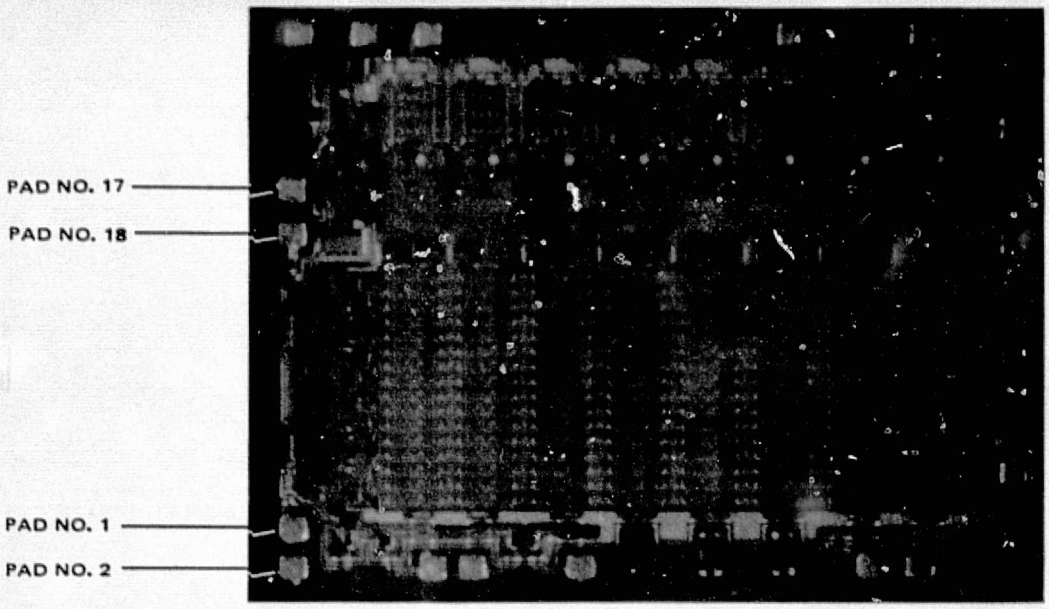
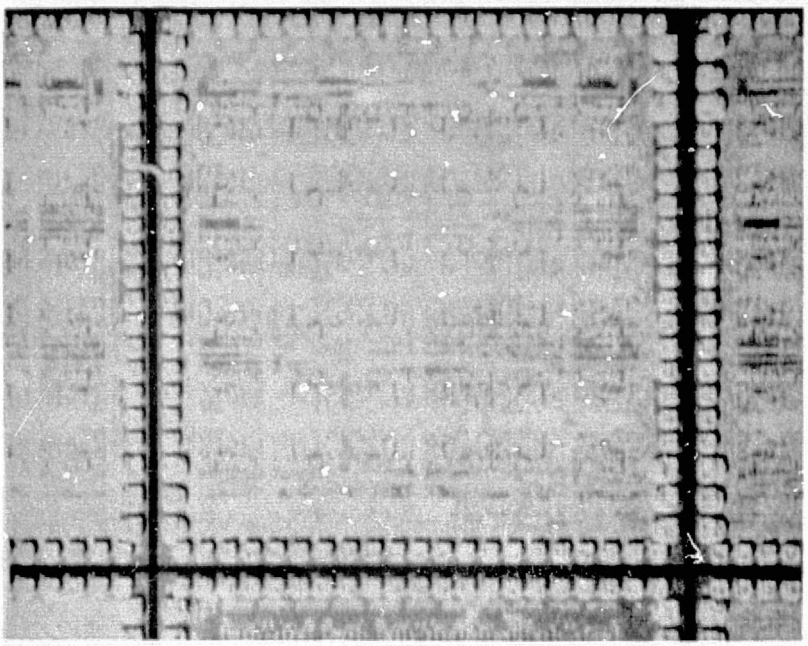


Figure 2-20. Hughes Type 1824D microprocessor RAM chips inner-leaded-bonded to 35-mm tape carriers.



a. 18-pad MOS device.



b. 82-pad ECL device.

Figure 2-21. Bumped 18-pad MOS device and 82-pad ECL devices showing close pad spacings.

Fairchild Semiconductor Division were relatively less bondable and less ductile however, than those of the 1824 CMOS RAM, which was bumped at Hughes. Higher tool temperature and force therefore were required. A TTL device inner-lead-bonded to tape is shown in Figure 2-22.

As discussed in paragraph 2.2.1, difficulties with the 82-pin ECL devices resulted from damage to the delicate lead structure during handling of the tapes during and after gold plating. As a result, the lead ends did not always remain in their true locations, and some of them bridged two bumps during inner-lead bonding, as illustrated in Figure 2-23a. The use of support rings (Figure 2-12) will aid in solving this problem. Improved ILB yield was noted however, when the more-rugged second-iteration tape

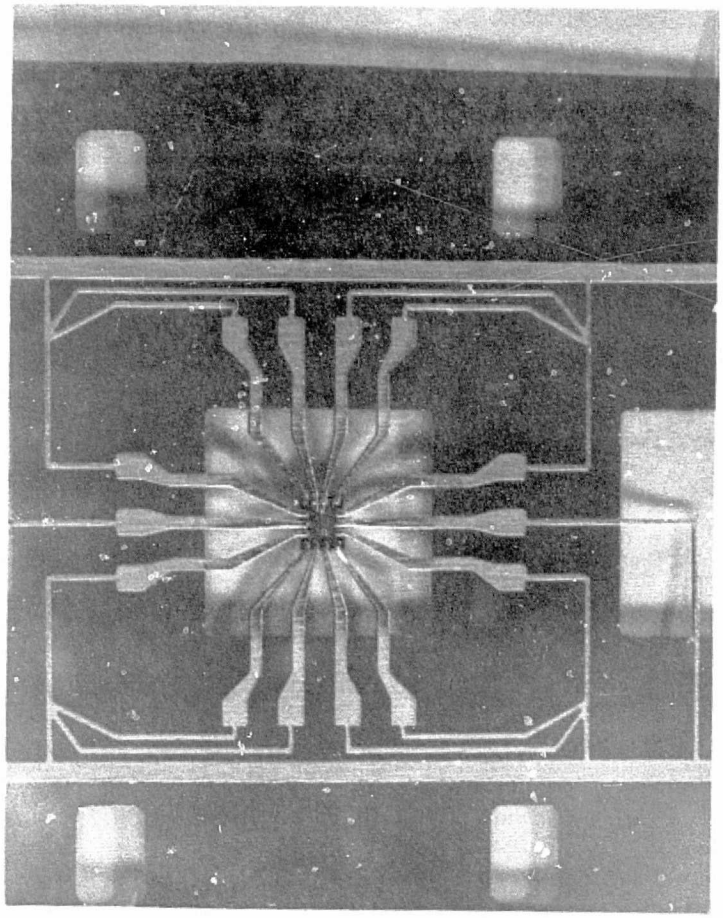


Figure 2-22. TTL device inner-lead-bonded to 16 mm tape.

carriers (fabricated with dry resist support/backing) were utilized, even without the addition of support rings. This improvement is illustrated in the photograph of Figure 2-23b.

2.2.4 Outer-Lead-Bonding Evaluation

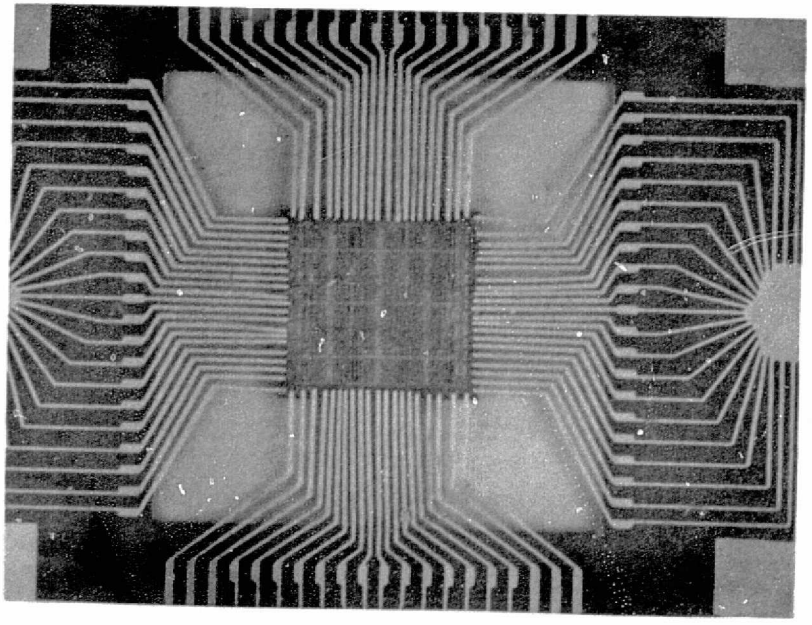
After the inner leads are bonded, the die with attached-leads ("spider") is excised from the tape. Within the same tool, the leads are formed upward and then downward from the top face of the die to facilitate outer-lead bonding. (For larger chip sizes, separate excise and forming tools may be more practicable for maintaining high yields at reduced overall tooling costs. Hughes currently is conducting trade-off studies in this area, under internal funding.)

With currently-used manual handling methods, the leaded dies (spiders) are placed upon a bond station pedestal, picked up with the outer-lead tool by vacuum, and bonded or soldered (OLB) to a ceramic-based thick film conductor network, as indicated in Figure 2-24.

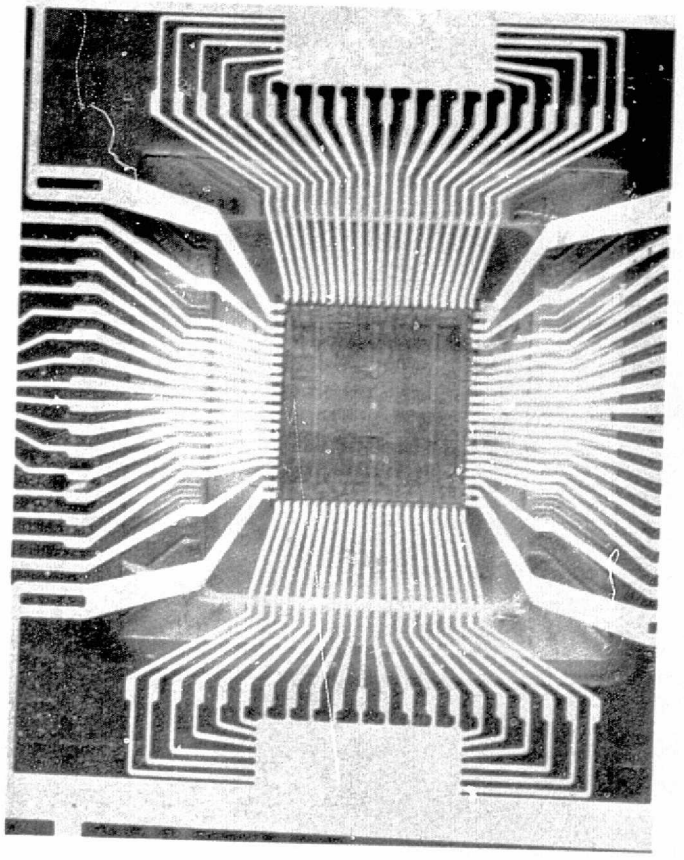
Outer lead bonding has been demonstrated successfully with 14-pad TTL devices thermocompression-bonded to "reactive" gold thick film, and soldered to palladium-silver thick film networks. Pull test strength was measured by means of a hook applying load at the knee of the formed bend in the leads. Strength values are reported in Table 2-14. Most of the failures occurred as a result of thick film pads lifting from the ceramic substrate.

2.2.5 Sample Test/Burn In Study

Metallization on tape carriers for the TTL, MOS, and ECL devices has been designed for gang burn-in. The pads are connected to buss bars along the tape edges through junctions at the perimeter of each pattern. When appropriate signals are applied to the buss bars, the devices on the tape can be exercised during burn-in (for the ECL devices, several wire bonds are required to energize each chip in a series).

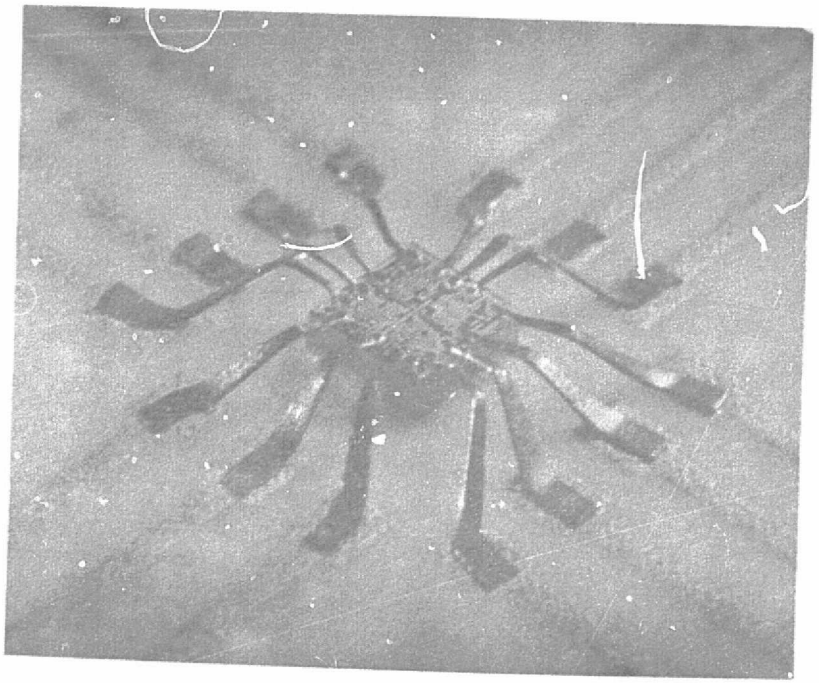


(a) First-iteration tape carrier which do not quite match bump locations.

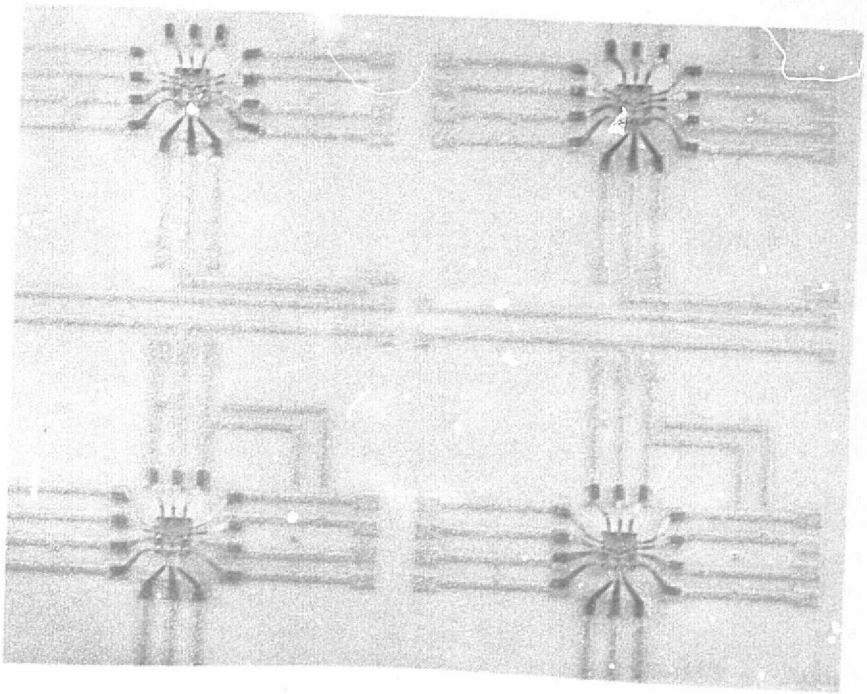


(b) Improved lead/bump matching attained through usage of dry-resist-backed second-iteration tape carriers.

Figure 2-23. Inner-lead-bonded 82-pad ECL devices.



(a) Single TTL device outer-lead-bonded to thick film network.



(b) Array.

Figure 2-24. Array of TTL devices on ceramic-based thick film network.

TABLE 2-14. OUTER LEAD PULL STRENGTHS

Device Number	Number of Tests	Pull Strength (grams)			Failure Mode (Number of Failures)		
		Average	High	Low	Thick Film	Lead	Bond Interface
1	10	60	85	45	8	2	0
2	8	50	65	25	8	0	0
3	6	45	70	35	5	0	1
4	7	60	85	30	7	0	0
5	12	50	75	35	12	0	0
Grand Total	43	55	85	25	40	2	1

After burn-in, appropriate junctions are punched out, leaving each pad on the tape electrically isolated. The devices then can be tested functionally by means of appropriately-designed probe cards which serve to transmit input and output signals/power.

A custom tape probing station has been designed, fabricated and checked out in operation. This prober was used with appropriate probe cards to test the 18-pad CMOS devices and the 14-pad TTL devices functionally on tape. Tape strips with up to seven devices can be tested in a sequence. The prober is capable of handling either 16 mm or 35 mm tapes.

2.2.6 Test Sample Fabrication

Environmental test samples were fabricated for the TTL devices. The substrates were screened/fired using a mixed-phase reactive gold ink for 50% of the samples. (A mixed-phase ink is a reactive ink to which a small amount of glass frit has been added.) The balance were screened/fired using fritted palladium-silver (Pd/Ag) ink over which tin-lead-2% silver (Sn-Pb-2Ag) solder paste was screened and then reflowed. The TTL devices

were excised from the tapes and attached to the substrates with conductive epoxy. The outer leads were thermocompression-bonded to the substrates on which gold conductors were screened/fired; and reflow-bonded to those on which solder was utilized. Each substrate was epoxy-attached to a metal platform package, and wire bonded to the package pins, as shown in Figure 2-25. Electrical function testing was accomplished on a computer-controlled GR Model 1790 parametric tester. It originally was planned to perform additional environmental testing on a second lot of samples comprising CMOS devices, outer-lead-bonded into the 24-lead hermetic chip carriers shown in Figure 2-26. This additional testing could not be accomplished within the contractual funding and time limitations, but these efforts will be continued on internal Hughes funding, and applicable results will be reported in connection with any resultant follow-on efforts related to the program just completed. Devices from the 14-lead TTL lot have been exposed to high temperature storage, thermal cycle, and thermal shock tests. Sample lead pull tests have been performed on devices so subjected, and results are summarized in Table 2-15. A detailed test matrix diagram is shown in Figure 2-27.

2.2.7 Environmental Test Results

Screened/fired network samples fabricated with each thick film ink (reactive gold and solder-coated Pd-Ag) were divided into three groups. Each group was exposed to one of the following MIL-STD-883 tests:

1. Thermal Shock; Method 1011, Condition A;
2. Temperature Cycling; Method 1010, Condition B;
3. High Temperature Storage (150°C); Method 1008, Condition C.

All samples passed electrical function testing after environmental tests were completed. Lead pull-test data after environmental test exposure are included in Table 2-14.

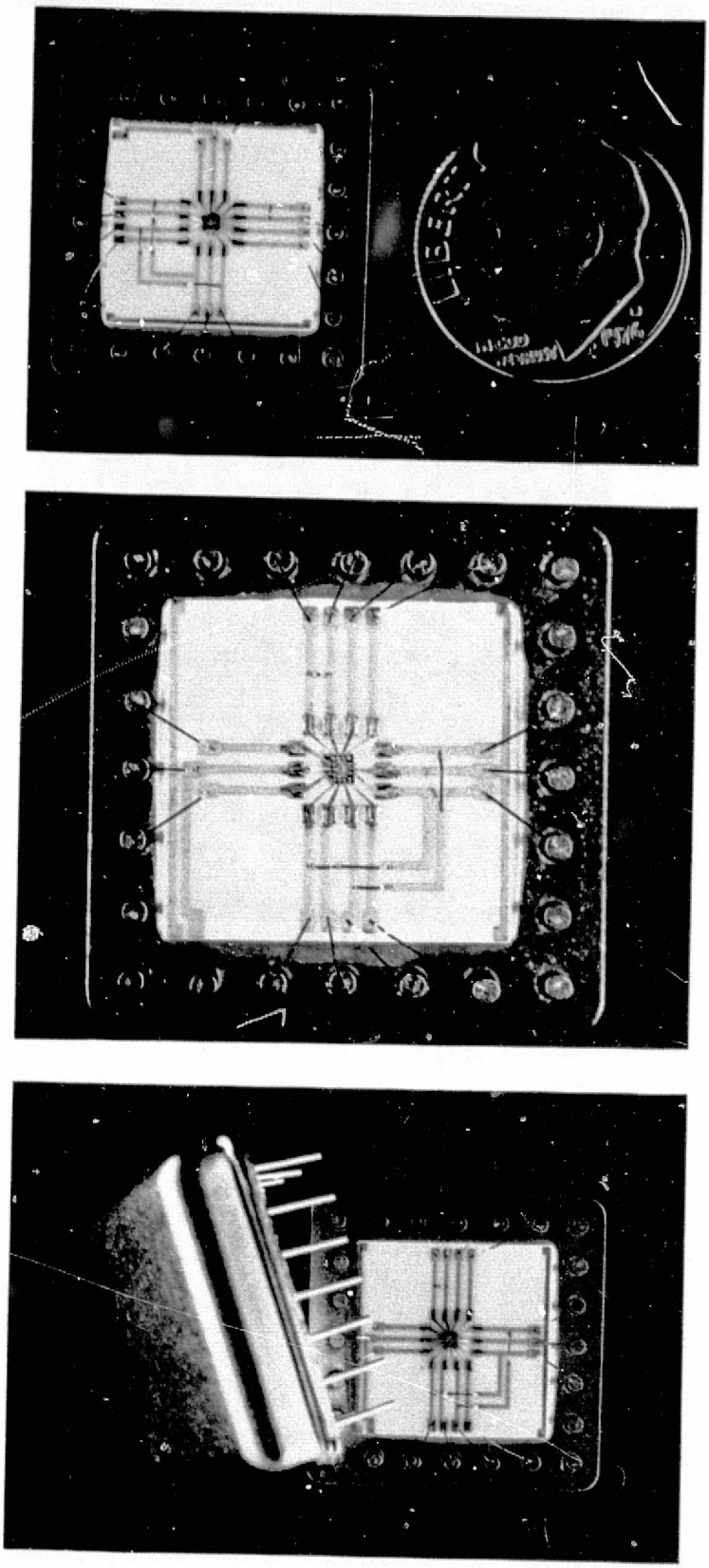


Figure 2-25. Environmental test packages for TTL devices.

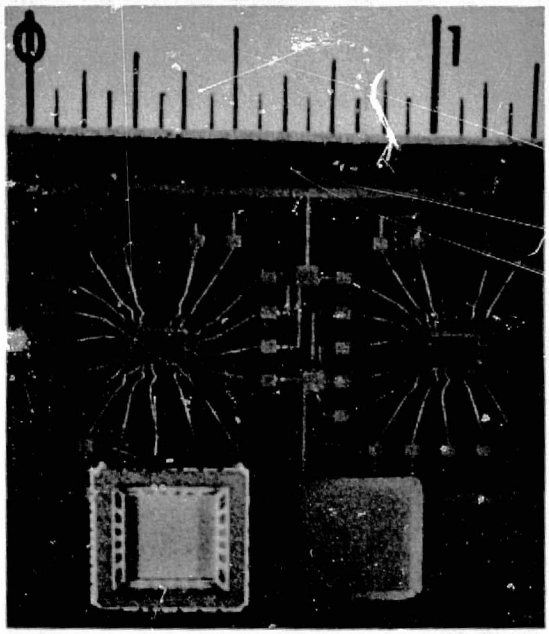


Figure 2-26. Hermetic chip carrier (24 pads) shown with metal lid/sealing pre-forms, adjacent to tape-mounted 18-pad Hughes Type 1824D micro-processor RAM semiconductor device.

TABLE 2-15. ENVIRONMENTAL TEST RESULTS - TTL TYPE 5400 DEVICES

Substrate Ink and OLB Bond Process	Type of Environmental Test	Pull Test Strength			Failure Mode of Majority	Passed Electrical Function Test
		Average	High	Low		
Mixed-phase gold-thermocompression bonded	None	37	70	15	OLB or ILB lifted	100%
	High Temperature storage	44	57	9	Thru lead or bump failure	100%
	Thermal Cycle	30	56	2	Bump-lead or thick film-lead interfaces	100%
	Thermal Shock	35	63	7		
Pd-Ag with Sn-Pb-Ag Solder - Reflowed	None	47	85	15	Lifted ILB or through lead	100%
	High Temperature Storage	52	80	30	Thru bump or thru Solder	100%
	Thermal Cycle	24	35+	15	Bump-lead interface	100%
	Thermal Shock	46	98	26	Thru bump or at bump-lead interface	100%

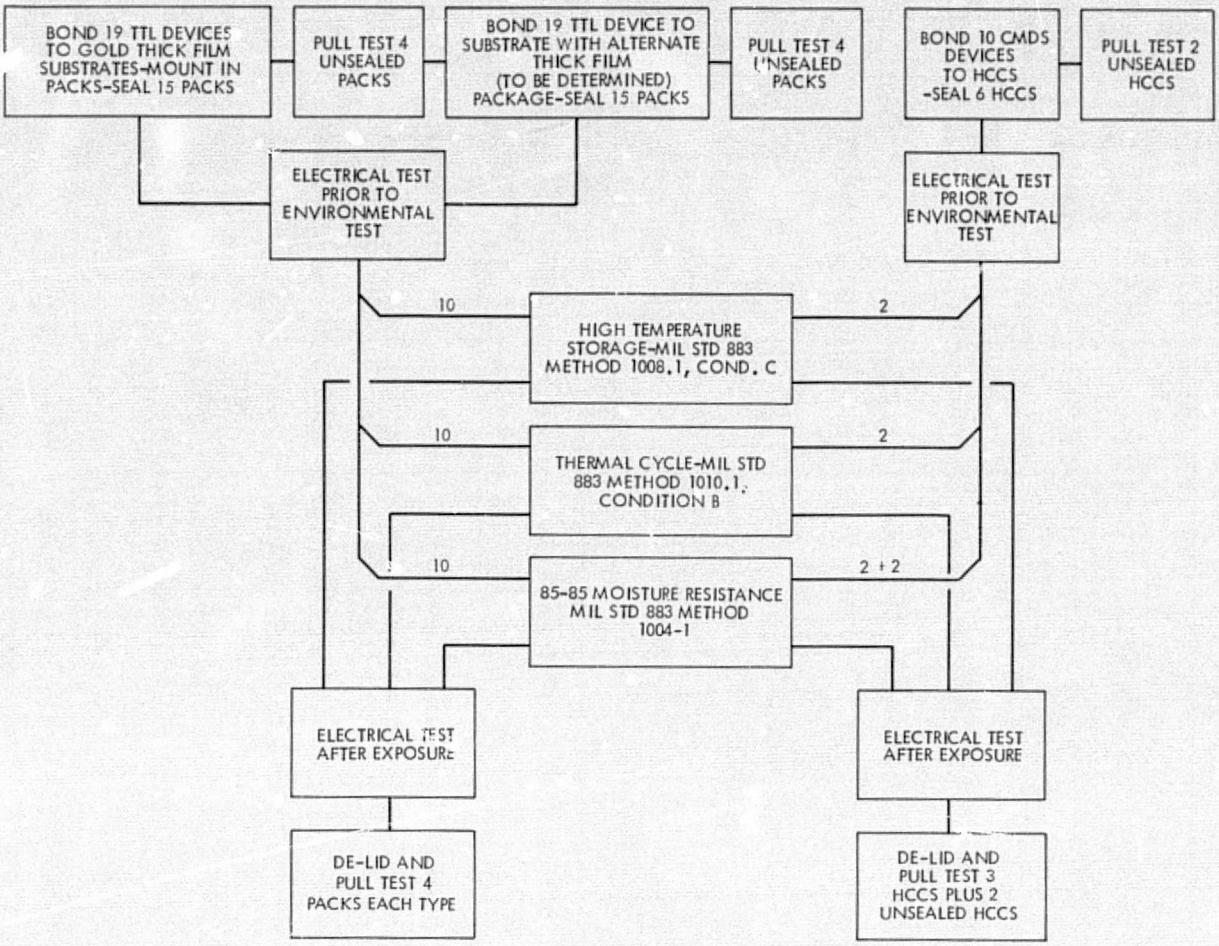


Figure 2-27. Environmental test matrix.

3.0 PROGRAM RECOMMENDATIONS

Hughes/NASA discussions regarding the program reported herein have led to the following recommended follow-on Statement of Work:

Task A. Cost Factors Study - Mathematical cost models for various discrete and hybrid microcircuit package concepts have been developed under the recently completed contract. It is recommended that these mathematical models be refined and broadened to include other state-of-art packaging techniques, such as ceramic chip carriers, multichip LSI "subassembly" arrays, and plastic LSI packages; in addition to more detailed analyses regarding tape chip carrier technology. The costing factors previously developed will be refined and reduced to formulas for computerization. The computer programs would be compatible with MSFC microelectronics equipment, and would be made available to MSFC for ready accessibility by engineers for costing and technology evaluation purposes.

Task B. Tape Chip Carrier Development Study - The data obtained to date on this contract indicates that tape chip carrier technology is a viable approach to low cost LSI packaging, and also could reduce hybrid microcircuit costs. It is recommended that work be continued in the areas of wafer bumping, inner/outer lead bonding, testing, and tape processing. To further develop this technology, studies and laboratory efforts would be conducted to show the feasibility of interconnecting an array of two, four, or more LSI chips on a tape carrier. These arrays would form standard building "blocks", from which a larger assembly or subassembly, including minicomputers or high density memory arrays, could be made.

3.1 TASK A APPROACH

The approach followed would be substantially the same as that which was followed under Task I, as reported under Subsection 2.1 of this Final Report. Qualitative and quantitative cost factors would be collected where needed, and functional relationships relating these factors would be found. Definitions, assumptions, and limitations would be stated. The mathematical cost models would be formulated upon them. Constants appearing in the formulas would be expressed in tables for ready reference, together with typical cost parameters. The simplified processes used for mathematical modeling would be shown as block diagram flow charts.

In conducting the recommended Task A follow-on Cost Factors Study, Hughes would cover the following specific tasks:

I. Refinement of mathematical cost models developed for hybrid microcircuits under Task I of the recently-completed contract.

II. Development of mathematical cost models for discrete packaging technology (Printed Wiring Board Technology) by using the cost factors collected in Task I of the recently-completed contract.

III. Broadening of the discrete packaging and tape chip carrier mathematical cost models which were initiated under Task I of the recently completed contract, and extension of these models to include:

   a. Ceramic chip carriers,

   b. Plastic LSI packages, and

   c. Multichip LSI "subassembly" arrays.

IV. Development of the computer software for the mathematical algorithms of the cost models. These models will be refined and verified by computer simulation, using actual examples of real packaging techniques.

3.2 TASK B APPROACH

The work approach recommended for the Task B effort discussed above is shown in Table 3-1, which summarizes the tasks completed under the recently completed program and indicates the direction of effort which would be accomplished on a Task/Goal basis under a follow-on program.

TABLE 3-1. RECOMMENDED TAPE CHIP CARRIER WORK APPROACH - TASK B

Task Description	Current Program Synopsis	Proposed Program Task Goals	Remarks	
			Current Programs	Proposed Program Goals
1. Wafer Bumping	A: OK Electrically/ Mechanically B: Mask Alignment Problems C: OK Mechanically	B: Electrically/Mechanically D: Possibly E: Electrically/Mechanically	MOS Devices Require Particularly Careful Mask Alignment	More Definitive Process Refinement Required
2. Wafer Characterization (Before/After Bumping)	A: OK B: OK	E (possibly D)	Conducted by Supplier	To be Conducted by Hughes
3. Tape Preparation	A: OK B: OK C: OK	D and E (A, B, C as required)	Limited to 3-inch lengths	Expansion to 6-in. and/or 12-in. Lengths
4. ILB	A: OK B: OK C: Partial	D and E (complete C)	Used K & S Lab Bonder	Use of Projected New IMI Production Bonder
5. Testing on Tape	A: OK B: OK	D and E (complete C)	DC Parametric Tests	Functional Testing
6. Burn in on Tape	--	A (possibly D and E)	Not Demonstrated	Demonstration
7. Excise/Forming	A: OK B: Excise Only (OLB Tool) C: Ordered Tool	D and E (complete C, Excise only for HCCs)	A: to Networks; B: to HCCs (no forming) C: None	C: Use Newly-Received Tool
8. Lead Finger Support	Preliminary Investigation Only	B, C, D and E (best efforts)	Proprietary with Hughes Supplier	Investigate for ILB Compatibility, Solubility
9. OLB to S/F Networks	A: OK	D and E	Used for Environmental in Metal Packages	Special Test Circuitry
10. OLB to HCCs	B, C: Partial	Complete B and C; possibly D and E	Preliminary Investigations	Process Demonstration, Refinement
11. Reliability Testing of Networks/HCCs	A: OK	E (possibly B and C)	HT Life, Thermal Cycling, Moisture Resistance (Packaged Networks)	Add Pressure Cooker Test HTRB; Both HCCs and Networks
12. Silicon Nitride Coating/Retest	--	Best Efforts: A, B, C, D and E	New In-House Capability	Potential Replacement for Hermetic Packages
13. Multiple-Chip TCC	--	Best Efforts: E	--	Initial Conceptual Investigation and Proof of Performance

Candidate Devices:

A: 14 Pad Type 5400 Dual Quad NAND Gates

B: 18-Pad Type 1824 D Microprocessor RAM

C: 82-Pad ECL/MUX

D: 48-Pad Type 2903 Low-Pwr. Schottky CPU

E: 16-Pad 384-Element STAR

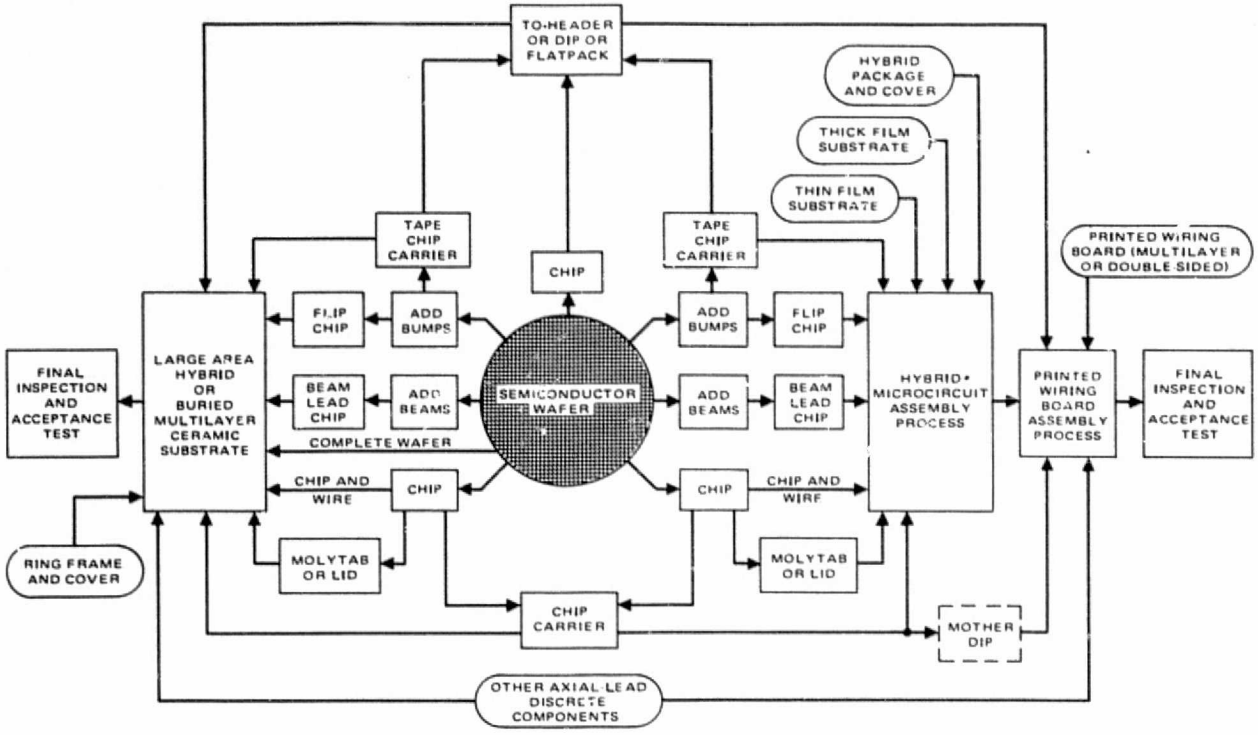
F: 64-Pad 1584 Element STAR

4.0 ACKNOWLEDGEMENTS

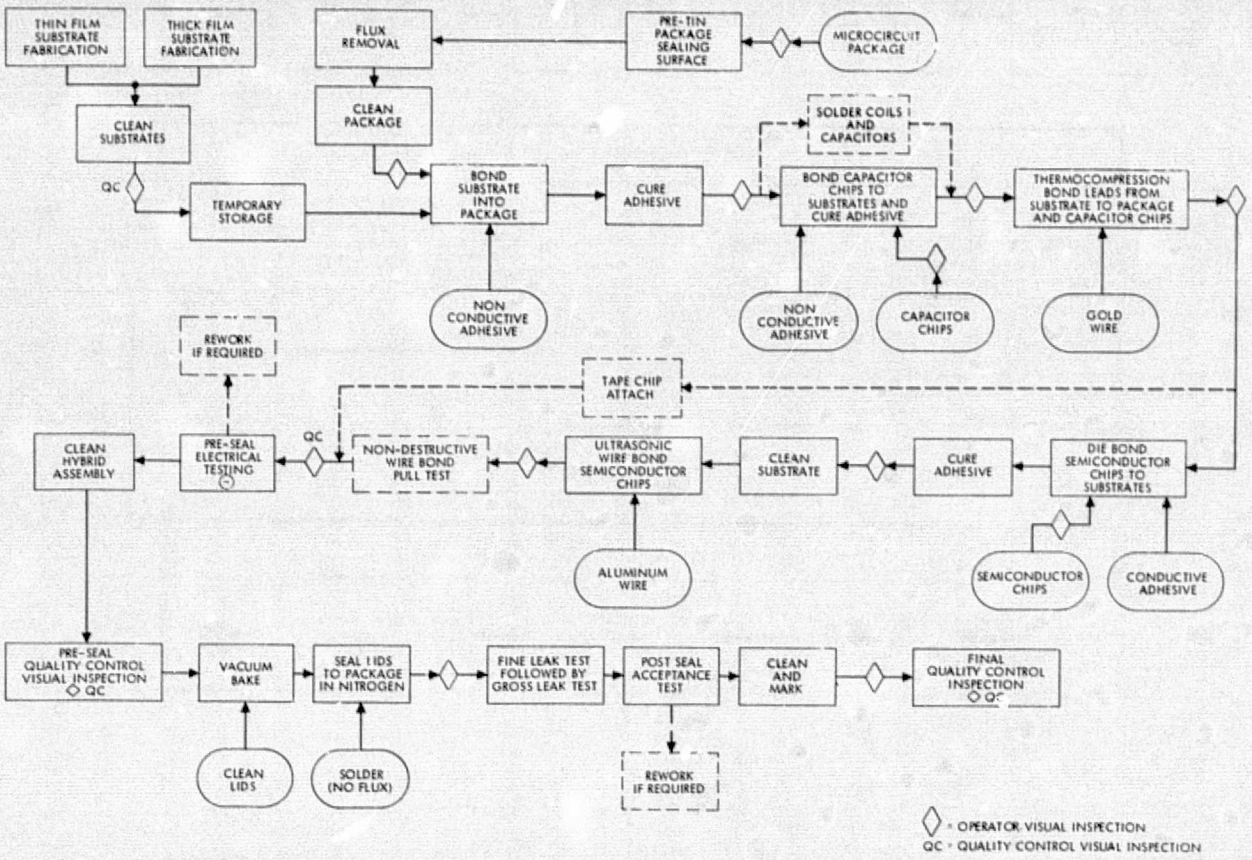
The authors acknowledge valuable assistance during this program to date, and in the preparation of this report, from Messrs. F. Z. Keister and R. G. Ravetti at Hughes-Culver City, who contributed the major work effort during Tasks I and II; and to Mr. R. Taylor of Hughes-Newport Beach, who assisted actively during Task III.

APPENDIX A
FLOW CHART LISTING

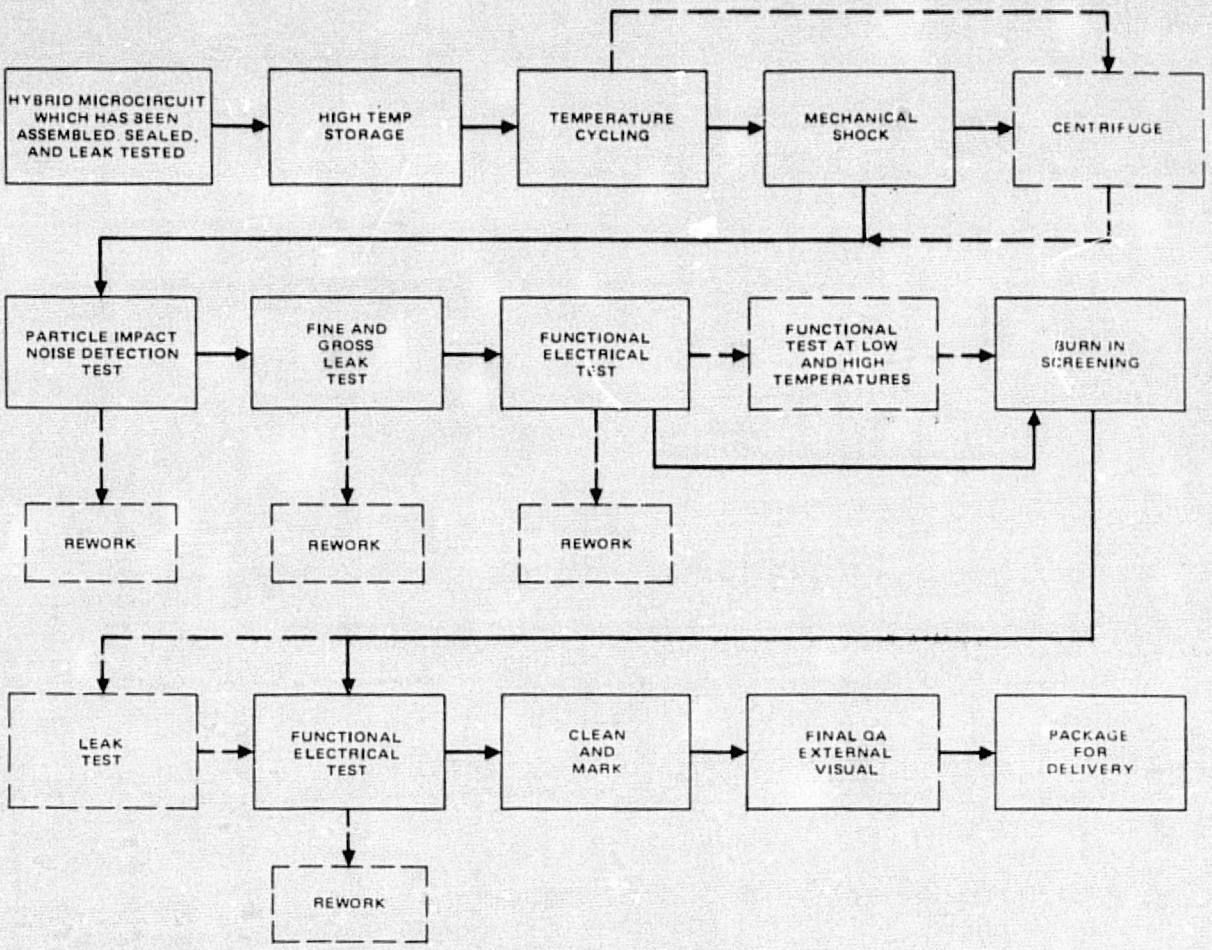
1. Summary Process Flow Chart from Wafer to Final Assembly and Test
2. Hybrid Microcircuit Assembly Process
3. Hybrid Microcuircuit Acceptance Testing Process
4. Thick-Film Substrate Fabrication Process
5. Thick-Film Multilayer Substrate Fabrication Process
6. Thin-Film Substrate Fabrication Process
7. Thin-Film Multilayer Air Gap Process
8. Thin-Film Substrate Metallization Process
9. Printed Wiring Board Assembly Process for Surface-Mounted Components
10. Printed Wiring Board Assembly Process for DIP's
11. Typical Printed Wiring Board Processing Sequences
12. Large Area Hybrid Process
13. Tape Chip Carrier Process
14. Buried Multilayer Ceramic Substrate Fabrication Process
15. Hermetic Chip Carrier (HCC) Process
16. Process Sequence Flow Chart for a High Power Transistor Captive Line
17. Flip Chip Processing and Assembly
18. Beam Lead Processing and Chip Assembly
19. MOS Integrated Circuit Chip Packaging Process



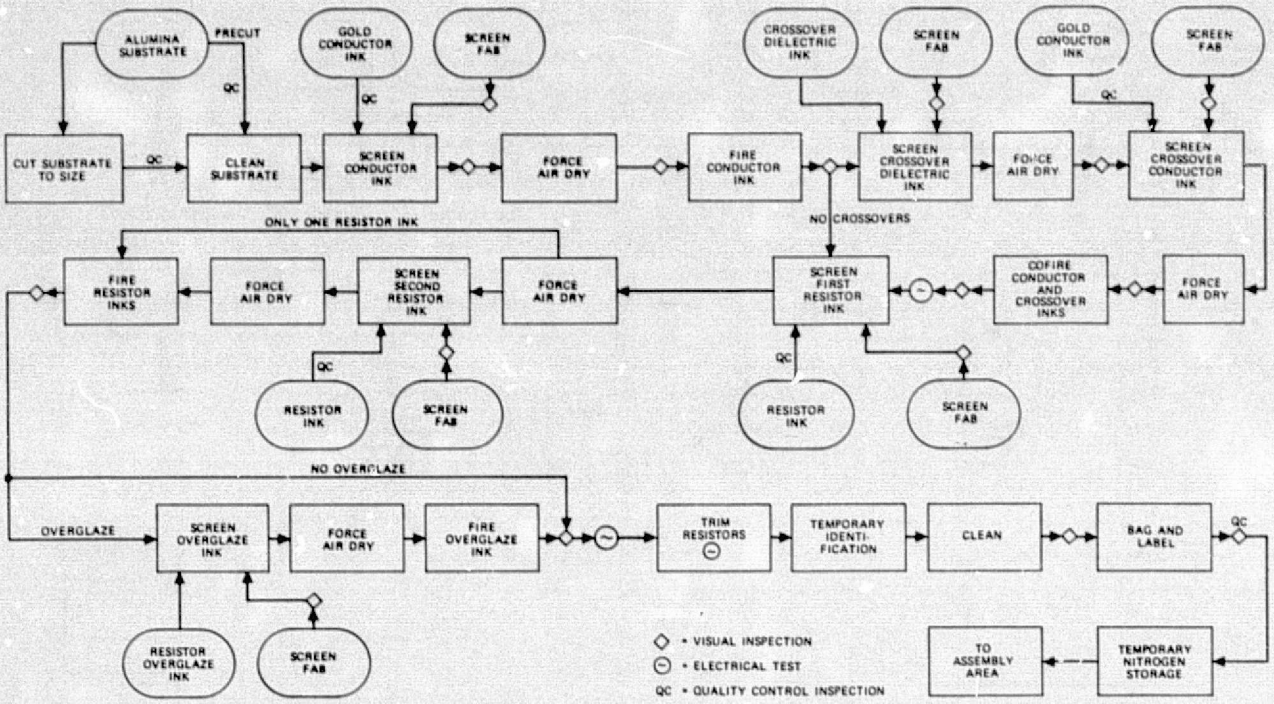
Flow Chart 1. Summary process flow chart from wafer to assembly and test.



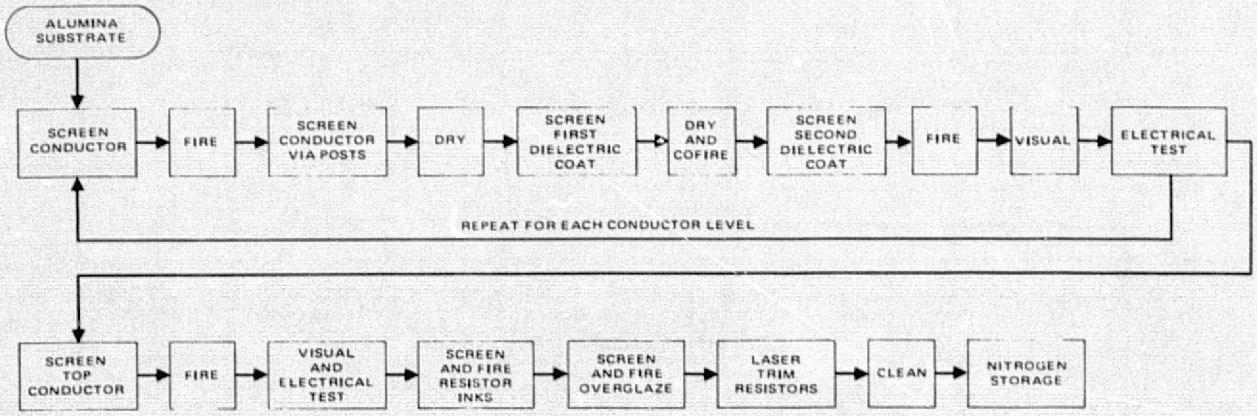
Flow Chart 2. Hybrid microcircuit assembly process.



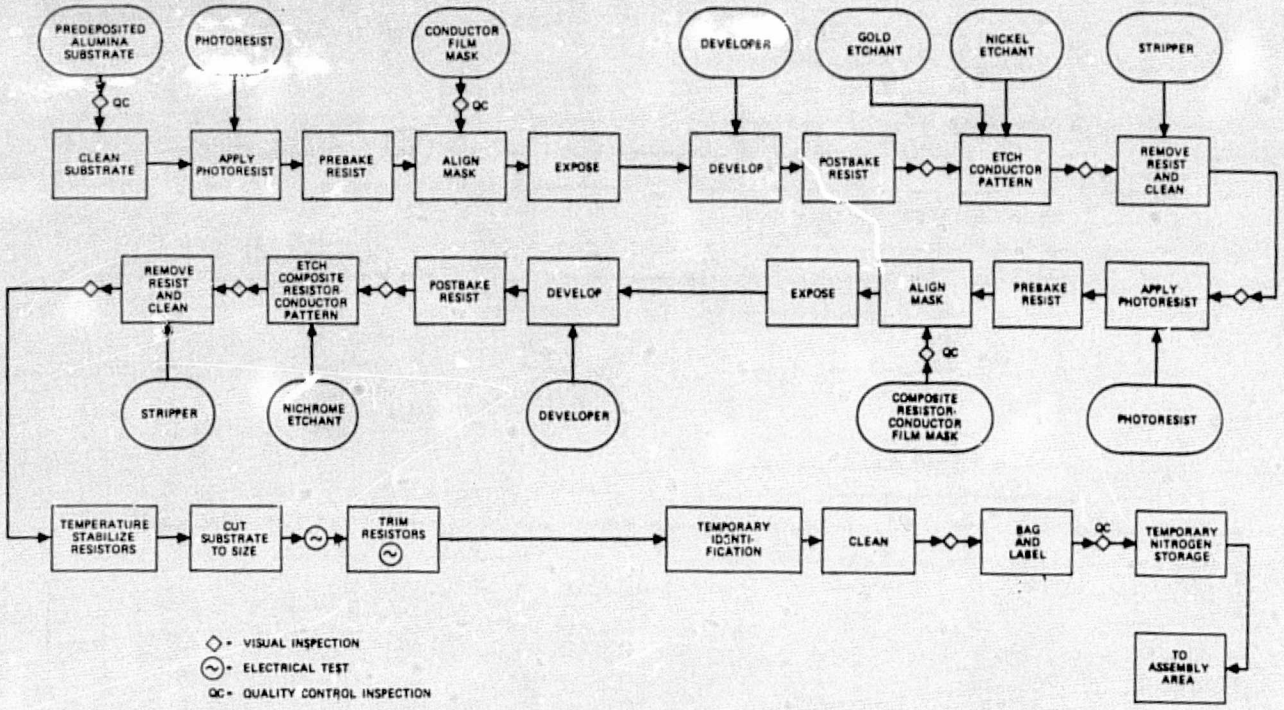
Flow Chart 3. Hybrid microcircuit acceptance testing process.



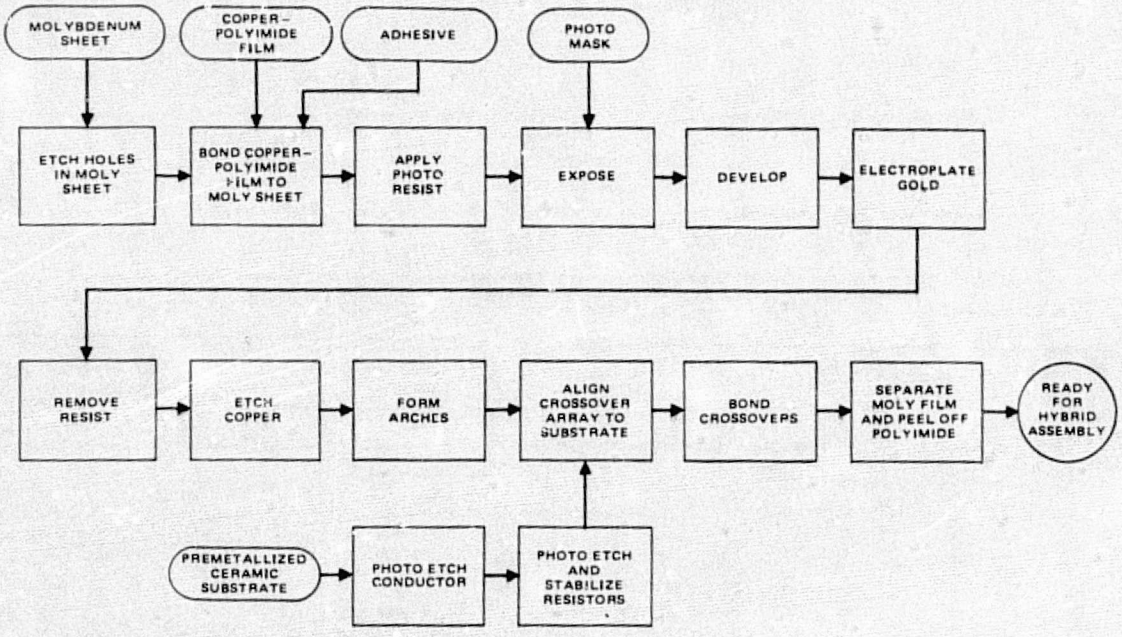
Flow Chart 4. Thick-film substrate fabrication process.



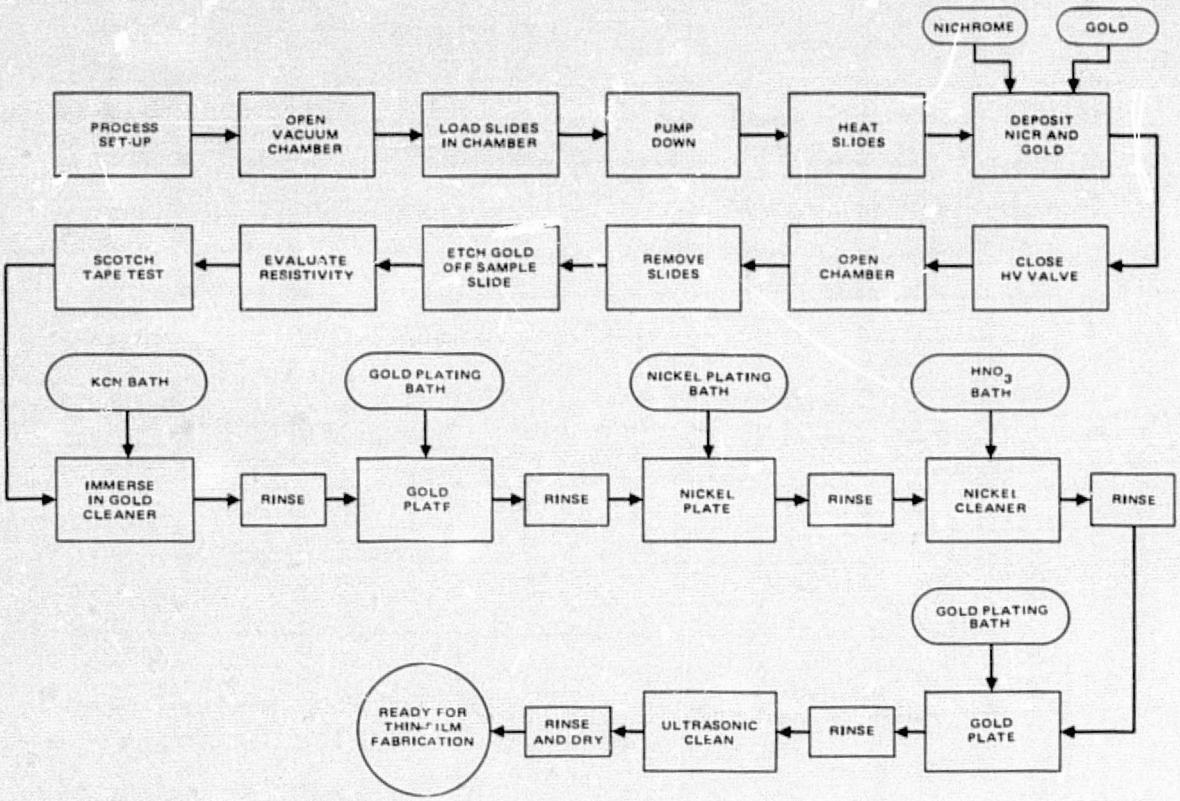
Flow Chart 5. Thick-film multilayer substrate fabrication process.



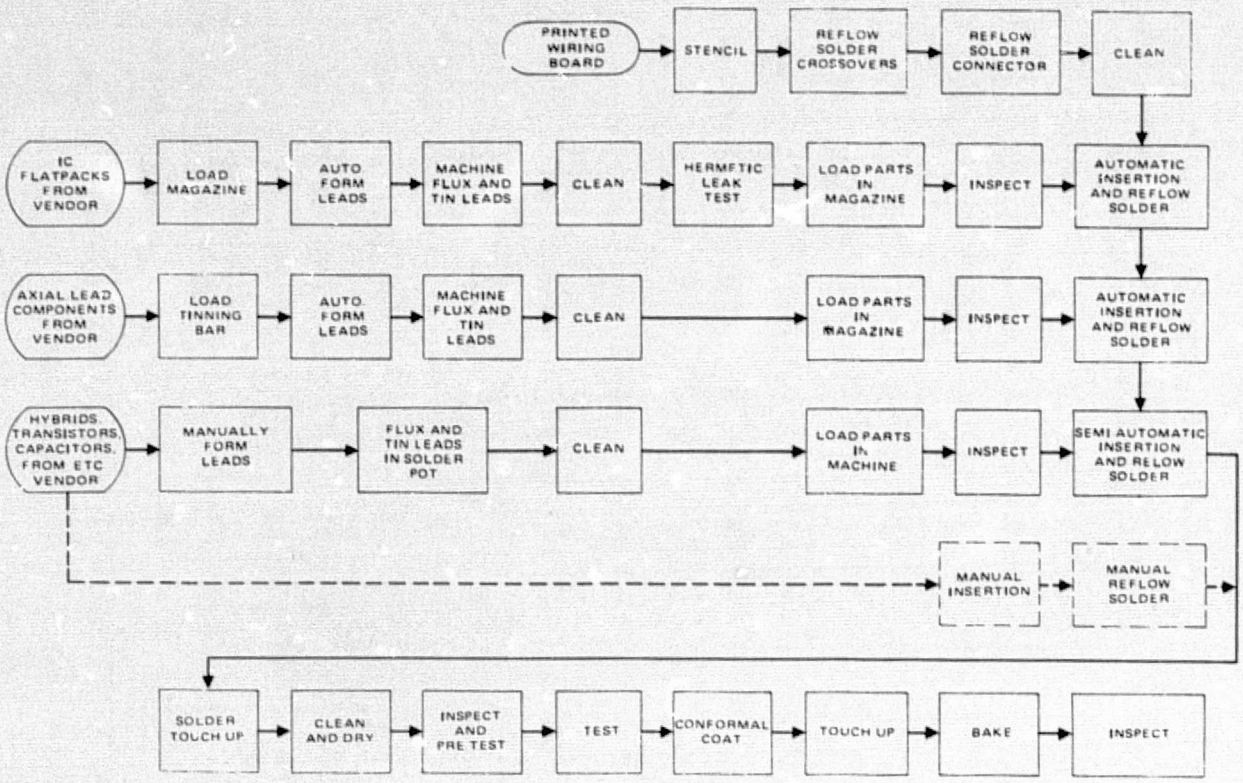
Flow Chart 6. Thin-film substrate fabrication process.



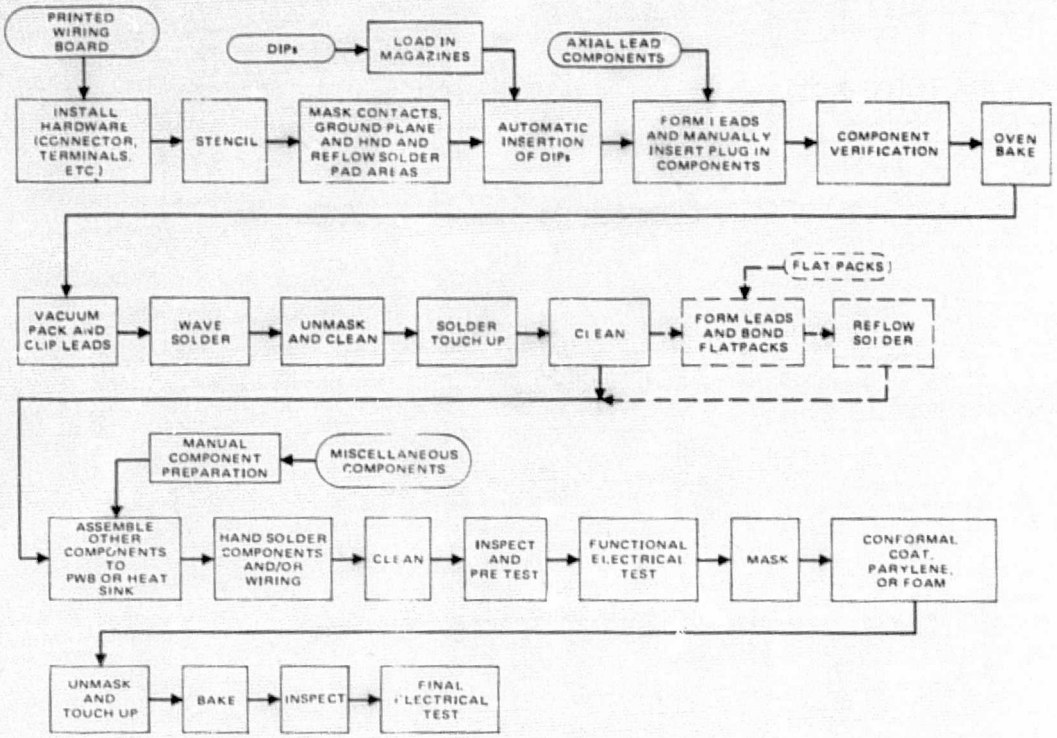
Flow Chart 7. Thin-film multilayer air gap process.



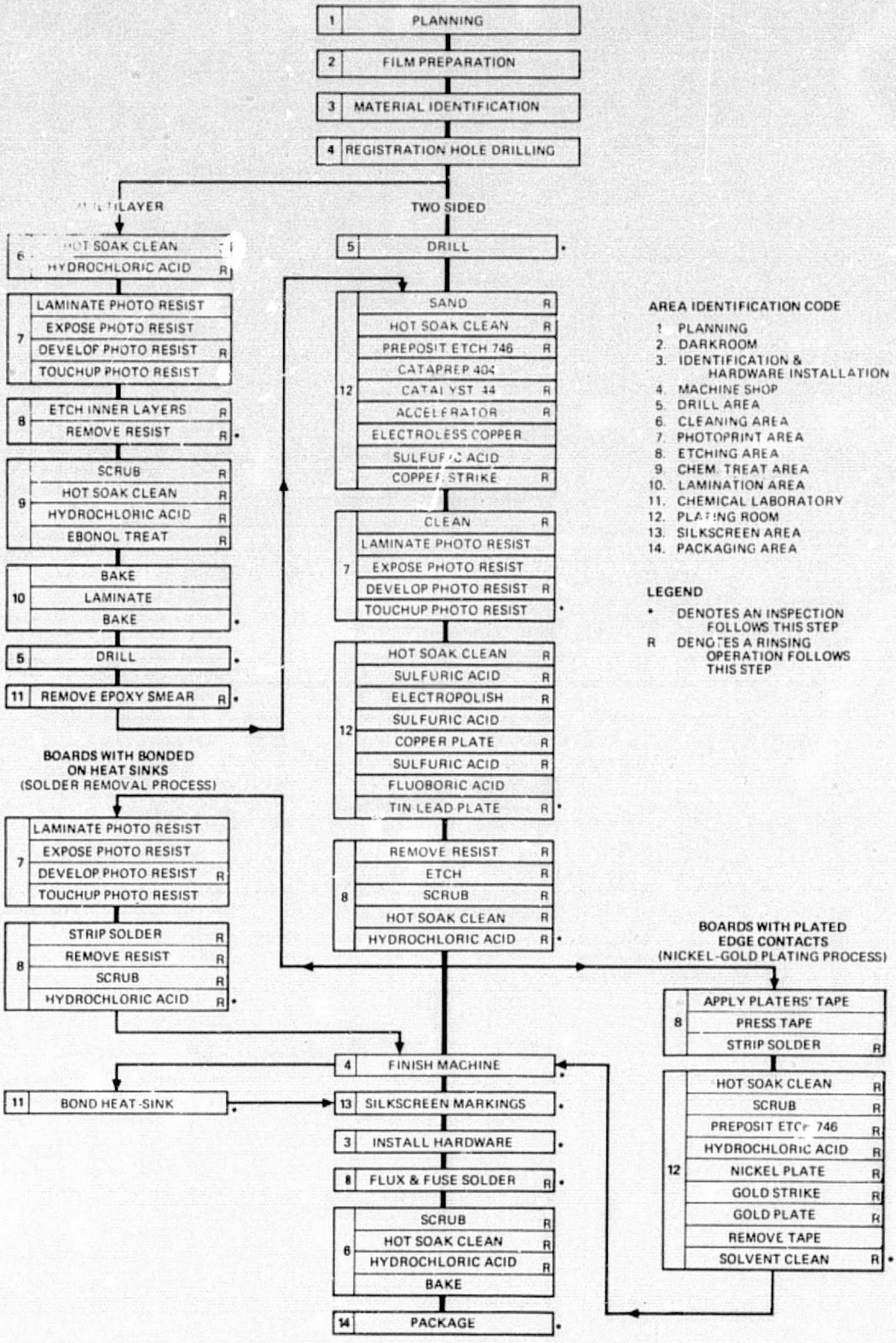
Flow Chart 8. Thin-film substrate metallization process.



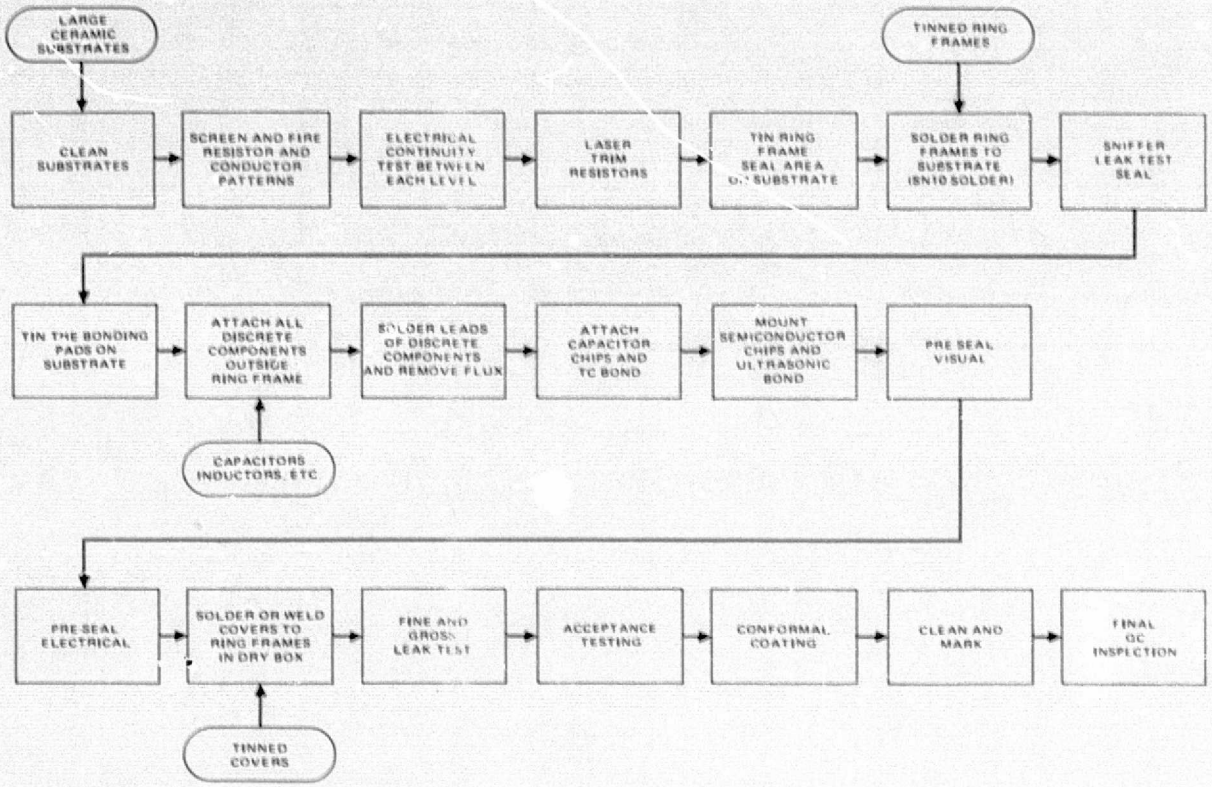
Flow Chart 9. Printed wiring board assembly process for surface-mounted components.



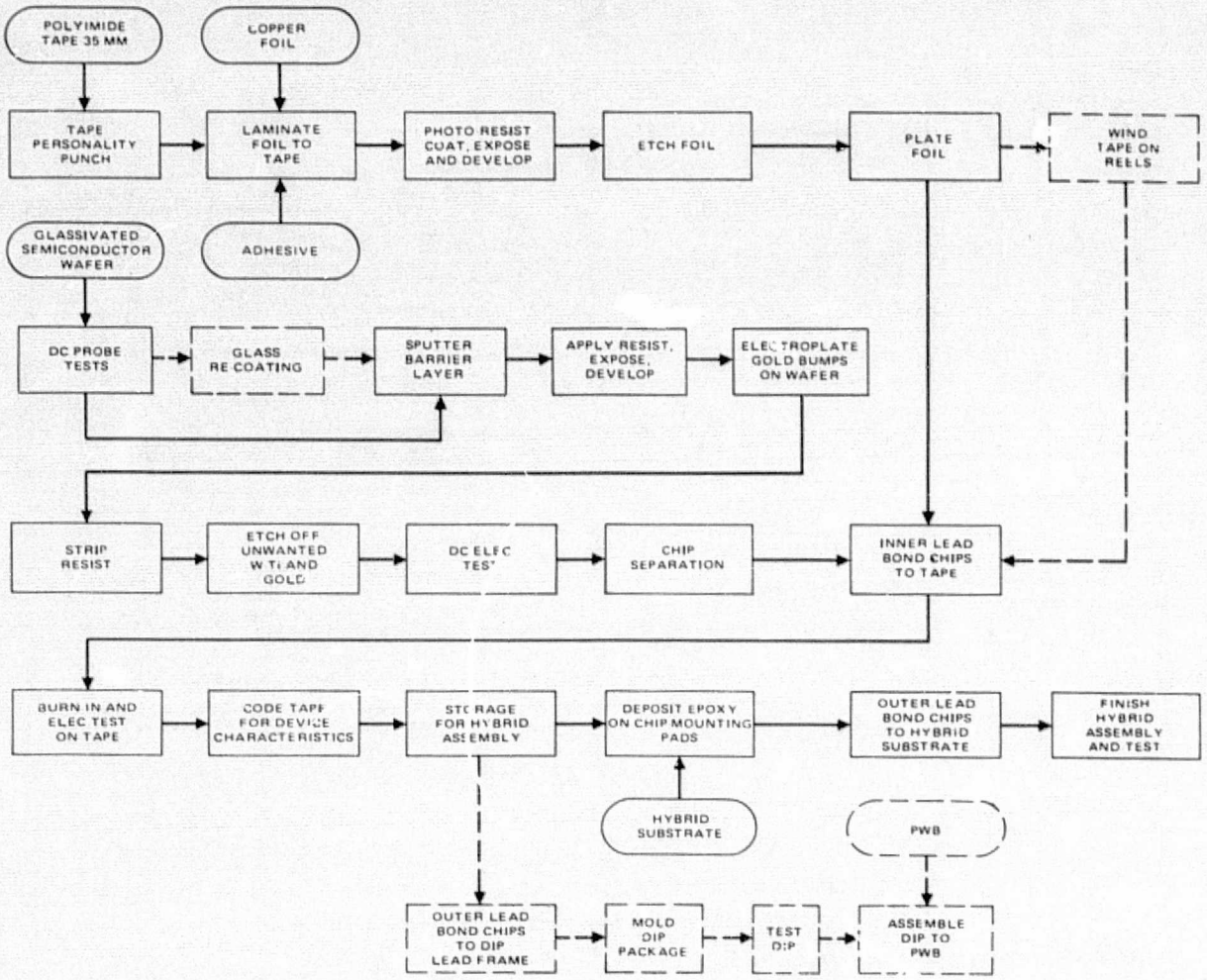
Flow Chart 10. Printed wiring board assembly process for DIP's.



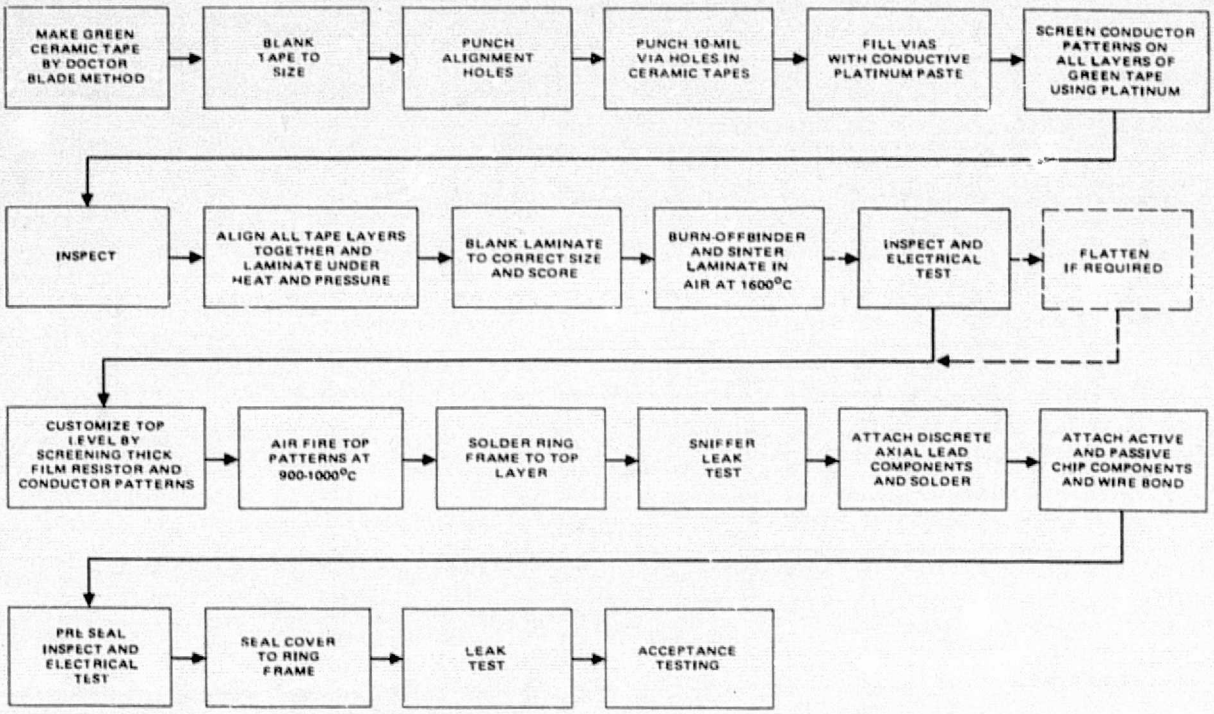
Flow Chart 11 Typical printed circuit board processing sequences.



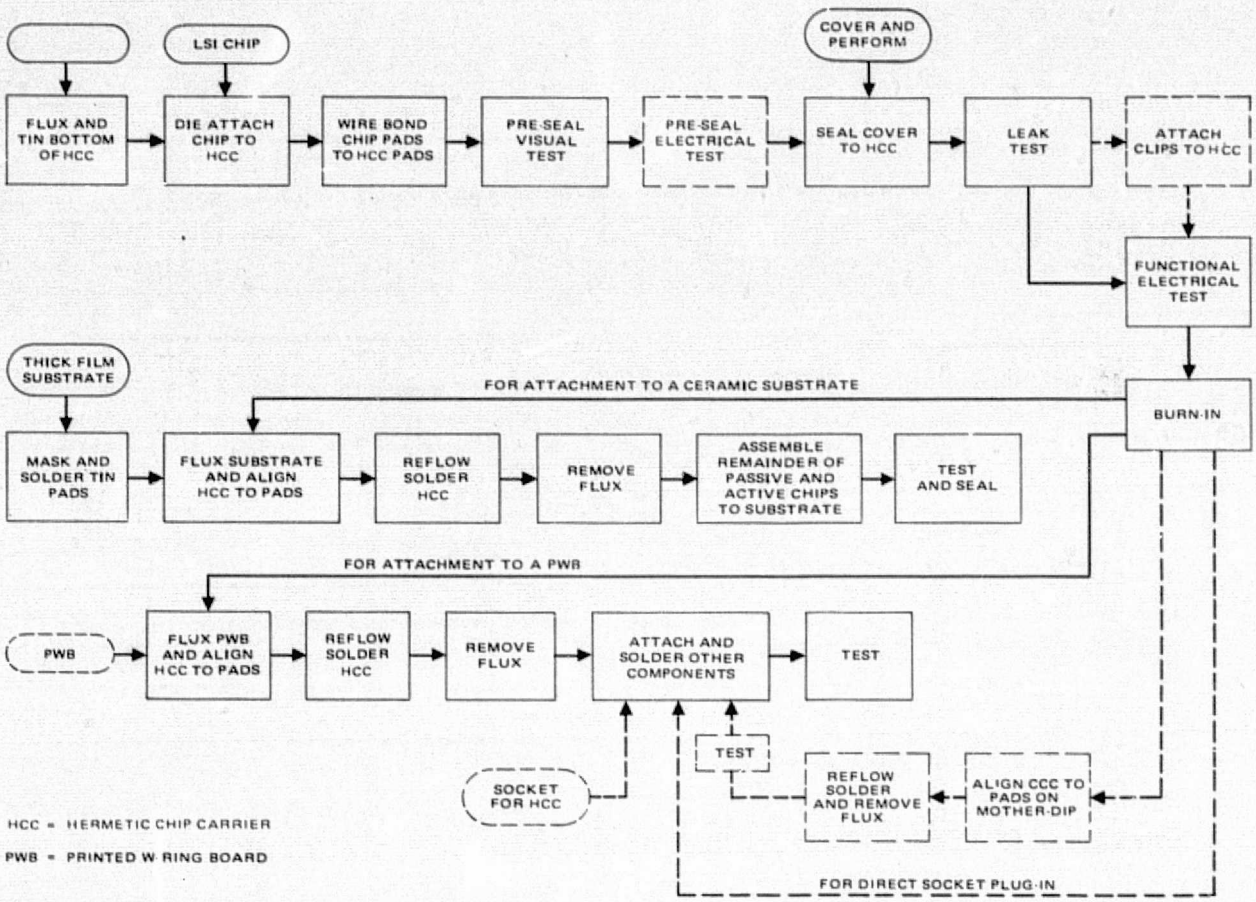
Flow Chart 12. Large area hybrid process.



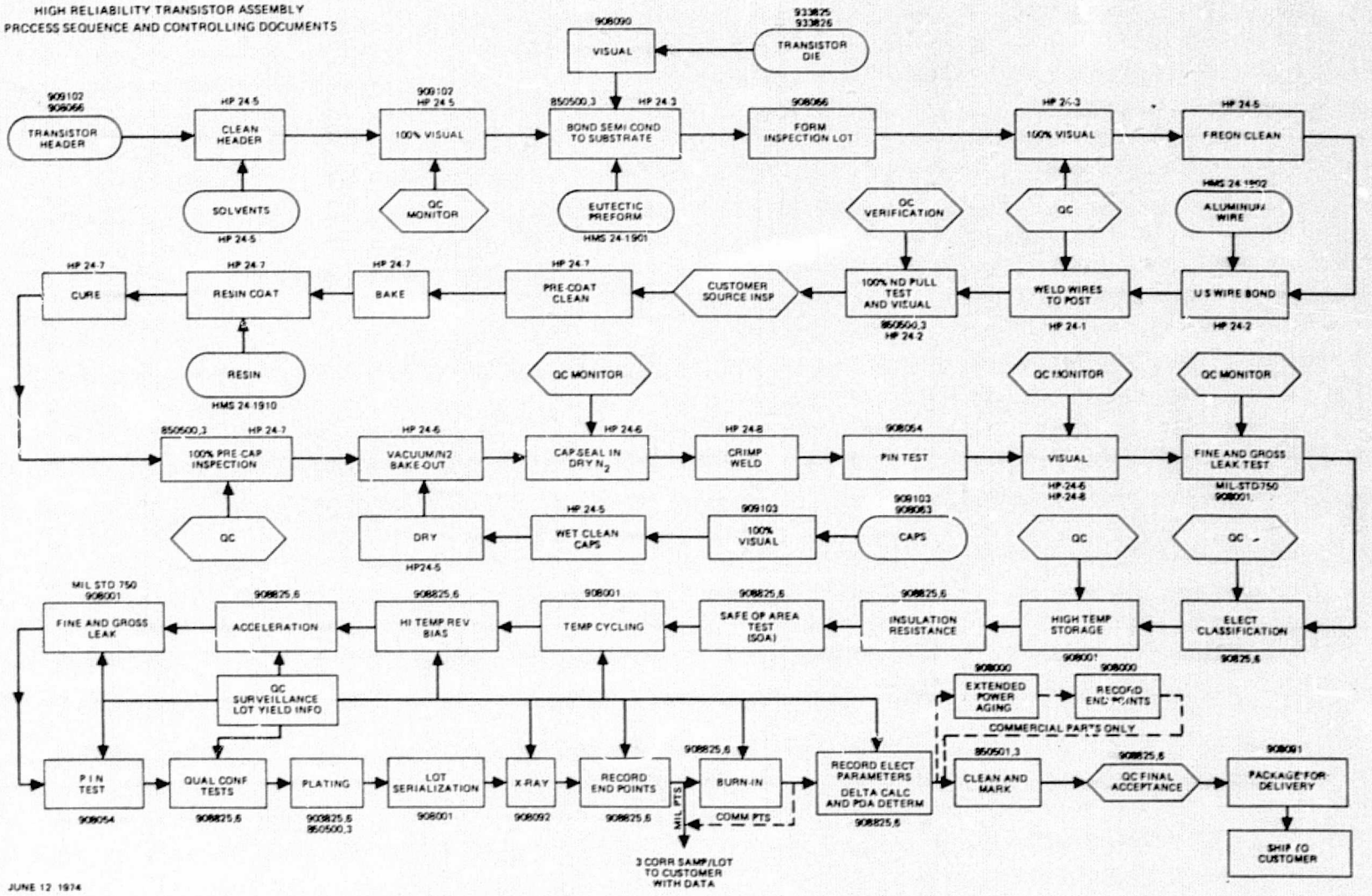
Flow Chart 13. Tape chip carrier process.



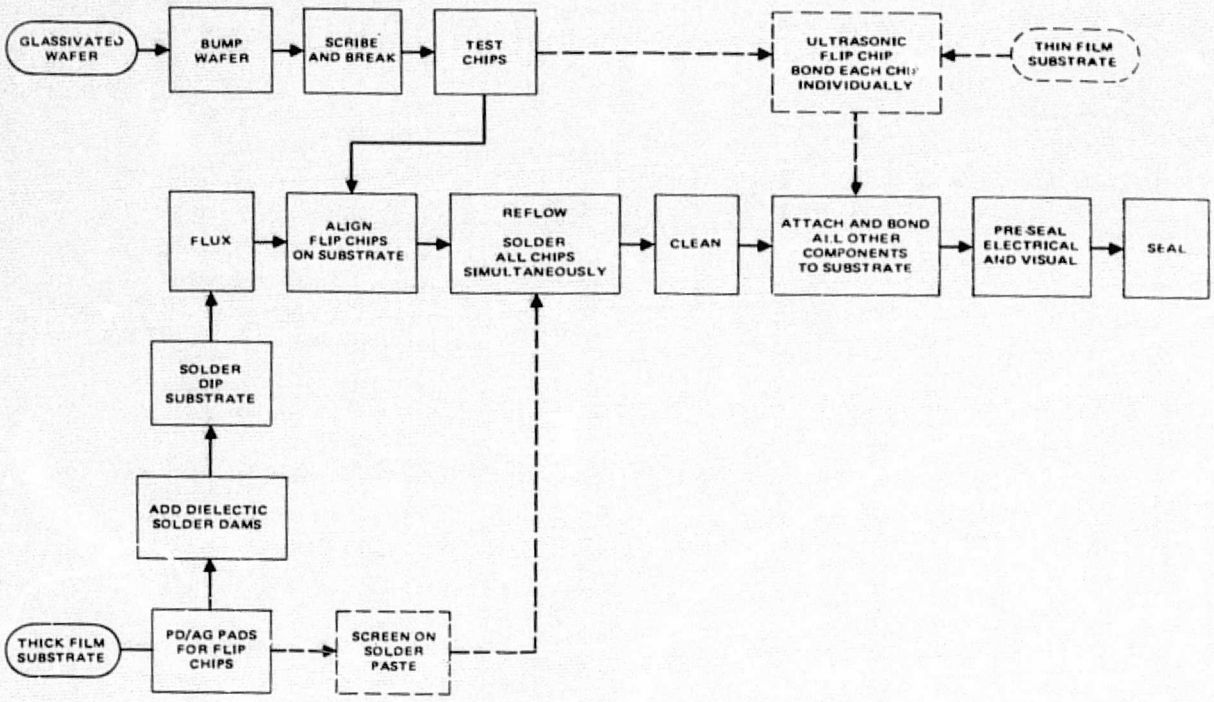
Flow Chart 14. Buried multilayer ceramic substrate fabrication process.



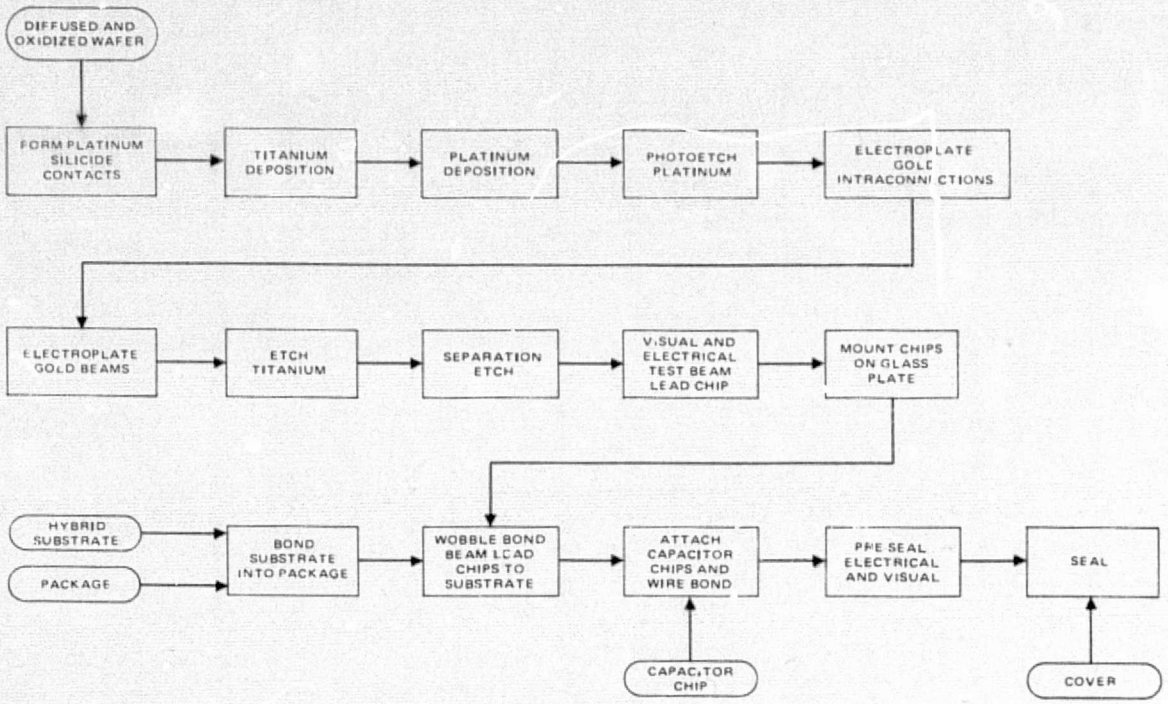
Flow Chart 15. Hermetic chip carrier (HCC) process.



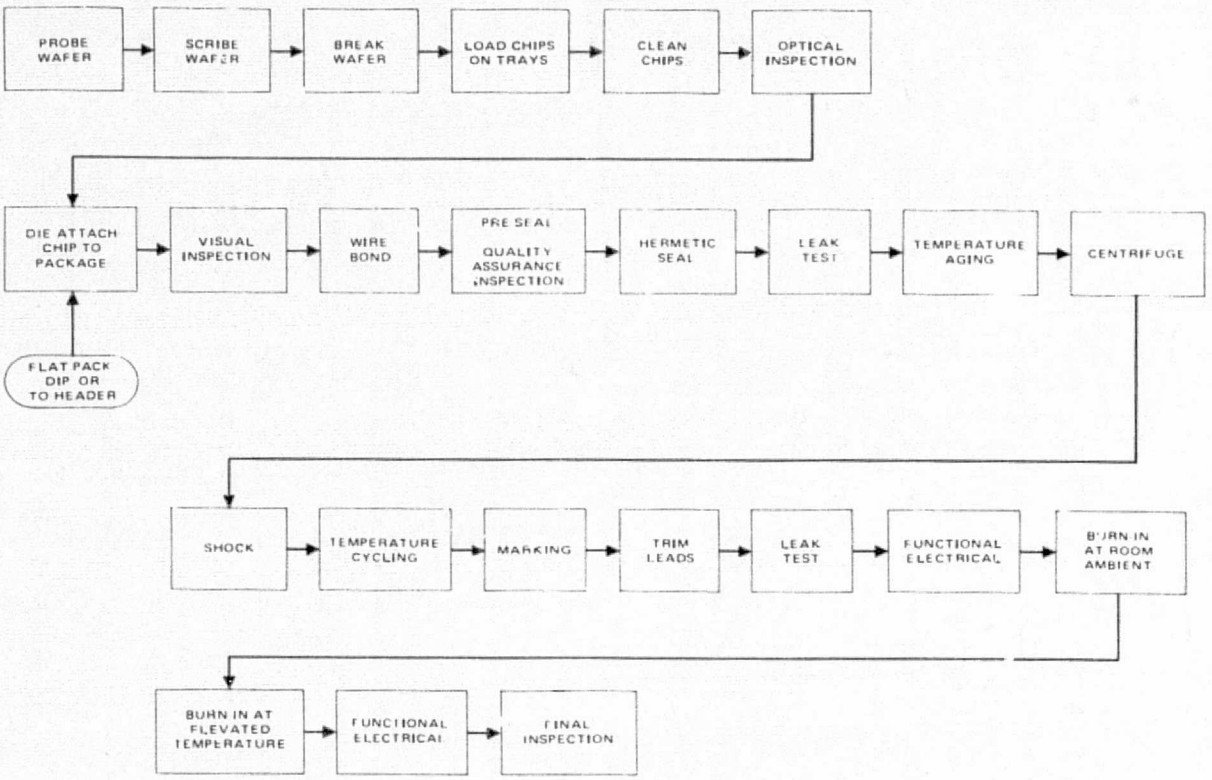
Flow Chart 16. Process sequence flow chart for a high power transistor captive line.



Flow Chart 17. Flip chip processing and assembly.



Flow Chart 18. Beam lead processing and chip assembly.



Flow Chart 19. MOS integrated circuit chip packaging process.