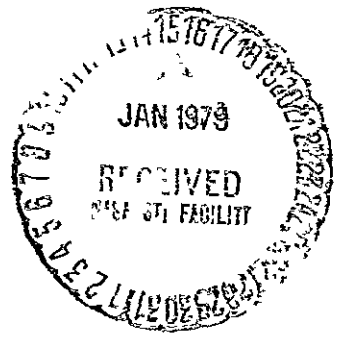
NASA Contractor Report 145334

Investigation of Charge Coupled Device Correlation Techniques

D.R. Lampe, H.C. Lin, T.J. Shutt

Westinghouse Electric Corp.
Linthicum Heights, Maryland 21090

Contract NASI-13674
Period Covered : Dec. 74 through Sept. 77
October 1978



National Aeronautics and Space Administration

Langley Research Center
Hampton, Virginia 23665

NASA CONTRACTOR REPORT 145334

INVESTIGATION OF CHARGE COUPLED DEVICE CORRELATION TECHNIQUES

D. R. LAMPE, H. C. LIN, T. J. SHUTT

Westinghouse Electric Corporation
Linthicum Heights, Maryland 21090

CONTRACT NAS1-13674
Period Covered: Dec 74 through Sep 77
October 1978

TABLE OF CONTENTS

TABLE OF CONTENTS

(CONTINUED)

1.0 INTRODUCTION

Analog charge transfer devices (CTD's) offer unique advantages to signal processing systems, which often have large development costs, making it desirable to define those devices which can be developed for general system's use. Such devices are best identified and developed early to give system's designers some interchangeable subsystem blocks, not requiring additional individual development for each new signal processing system. The objective of this work is to describe a discrete analog signal processing device with a reasonably broad system use and to implement its design, fabrication, and testing.

The "Operational Sampled Analog Processor" (OP-SAP) was selected[1] as the broadly attractive, general purpose vehicle and is functionally illustrated in Figure 1. Two sets of ANALOG data are presented to parallel analog delay means with the output taken as the sum of the true four-quadrant products. If one set of analog data are shifted by the other set of data, the resulting sequence of computations may be regarded as a discrete convolution function for relative motion in one direction; while relative motion in the other direction gives either a cross-correlation function for different sets of analog data or an autocorrelation function when the same data set is used in both channels. Transversal filters are a further example of a sequence of computations like that shown in Figure 1.

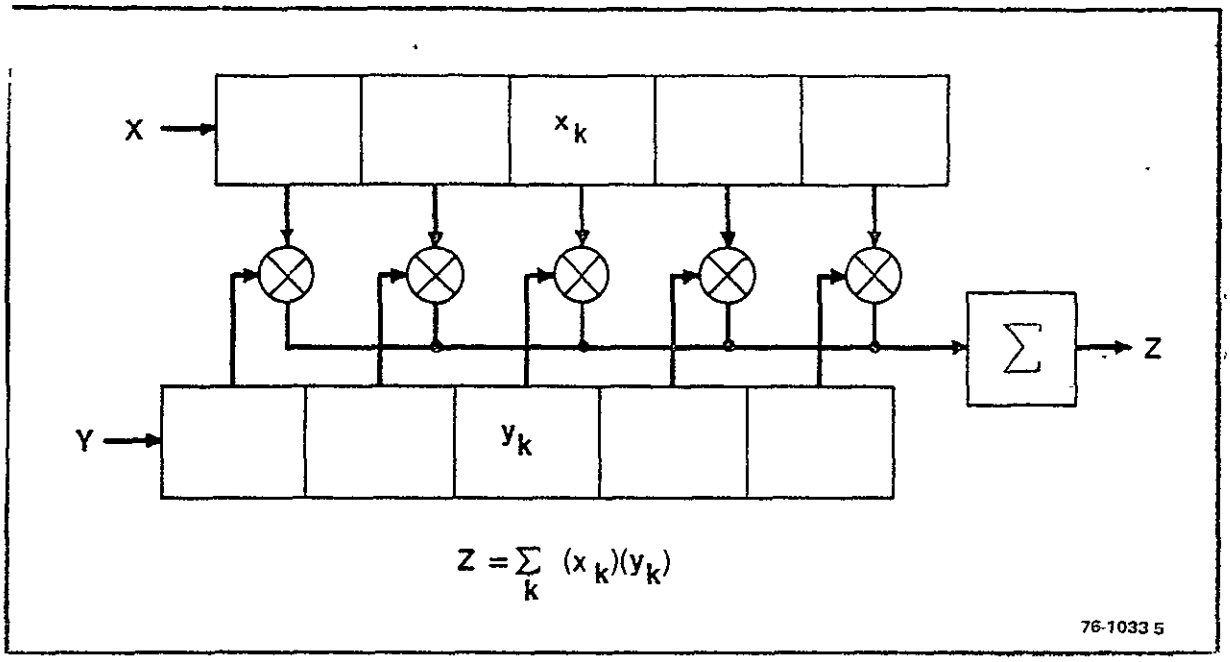


Figure 1 A CTD OP-SAP

Any device capable of the preceding correlation/convolution functions is also capable of a more limited class of applications which may be called analog matrix arithmetic. An example is the analog vector-dot product in which there is one only ONE sum computation with the pairing of analog values to be multiplied together strictly specified before the two data sets are entered into the CTD OP-SAP. Consequently, the motion of one set of analog samples relative to the other is inconsequential for this limited subset of applications. Thus, although of academic interest for the sake of completeness, any analog matrix arithmetic device limited by its inability to move one set of analog samples relative to the other will not be given detailed consideration here because it fails to meet the objective of a broadly useable analog signal processing item. A further restriction on the present investigation of CTD correlation techniques is the format of the input data: both sets of data are purely analog in contrast to binary coded analog for one of the data sets.

Within the boundaries prescribed by the above guidelines, all the essential constituents of a monolithic CTD analog-analog correlator/convolver chip have been investigated and designed on the basis of both experimental and computer model data with most of those elements subsequently incorporated into a hybrid model demonstrating the accuracy and feasibility of the preceding monolithic design effort. After the basic elements of the device are described, two attractive concepts for the bias of the multipliers are presented. Discussed next are some sources of deviations from

true analog-analog multiplication, such as harmonic distortion and direct feedthrough of the input signals due to unbalances from array threshold nonuniformities, as well as corrective measures to reduce the problems. Computer models illustrate the design technique based on the desired fabrication process and performance specifications including some broadly limiting formulas relating performance to fabrication and operation parameters. These formulas are tested against other published performanc data after a description of the previously delivered hardware. The summary and conclusions follow additional information on fixed pattern noise and multiplexing of analog-analog correlators.

2.0 ELEMENTS OF THE DEVICE

The basic device elements shown in Figure 1 are of two types: an array of multiplying means disposed between two analog delay means. Since substantial effort has previously been devoted to the needed analog delay means, only a brief comparison of the various attractive possibilities is now presented.

2.1 Analog Delay Lines With Independent Parallel Nondestructive Readout (NDRO)

A technique for NDRO in charge transfer devices is to sense the displacement of majority carrier charge which occurs when minority carriers in a CCD move beneath a floating CCD electrode. Figure 2 illustrates the use of a floating clock electrode technique to convert the signal charge q_s to a voltage v_G on the gate of a MOS electrometer amplifier:

$$v_G = \frac{C_o q_s}{C_s(C_o + C_G) + C_o C_G}$$

where C_G is the external capacitance associated with the reset switch Q_1, parasitic interelectrode capacitance, and gate capacitance of Q_2. Thus, considerable loading effects are present at each tap position in addition to a nonlinearity which results from charge sharing between C_s and the other capacitances. The minority carrier charge q_s is not disturbed, however, and the signal results from a redistribution of charge originating in the clock electrode drive circuitry. Such a technique is employed in the split-electrode type of CCD structures.

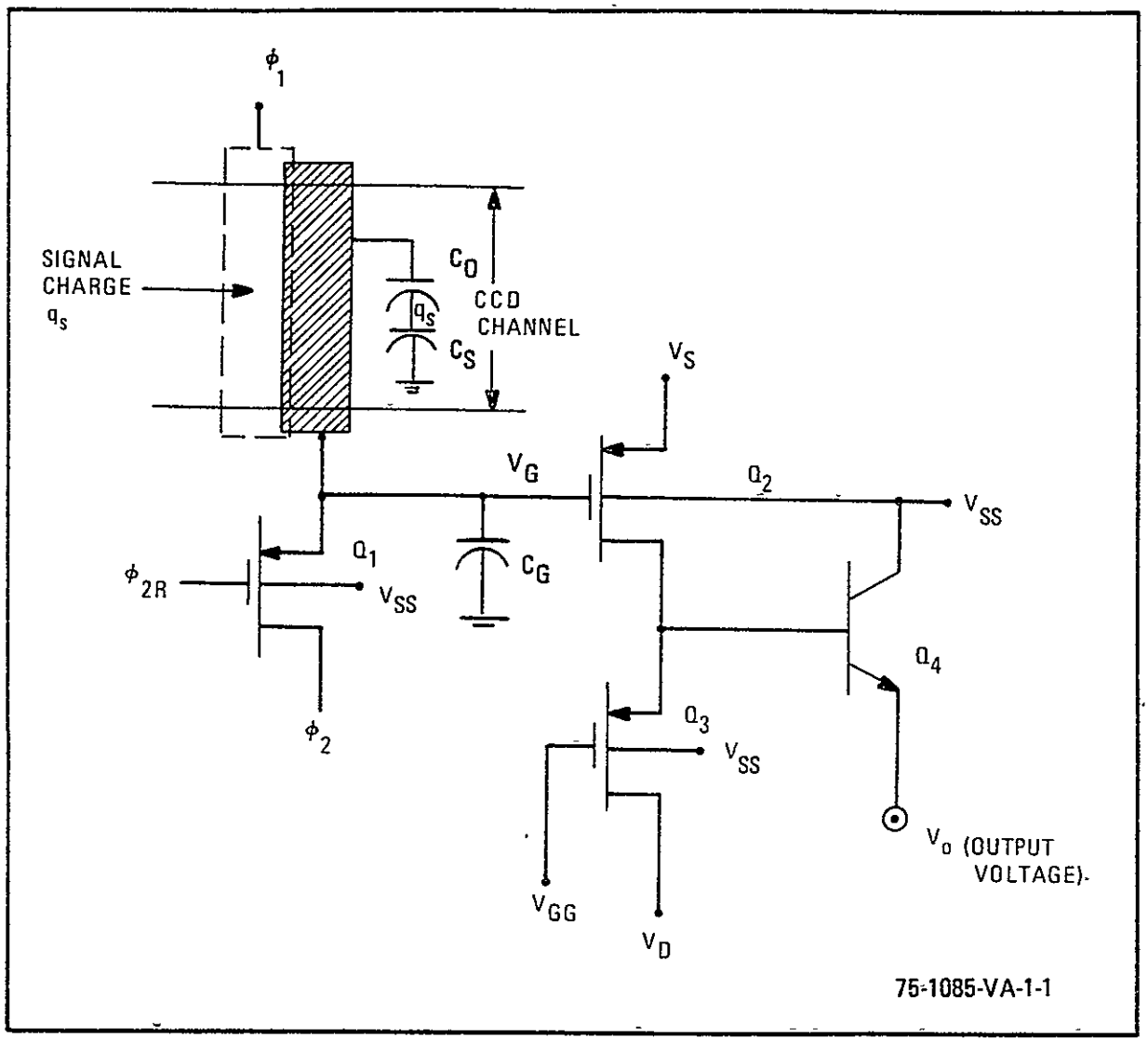


Figure 2 Floating Clock Electrode Sensor Tap Circuit for NDRO of Analog Signals in a CCD Delay Line

A reset switch is employed in the tap circuitry of Figure 2 in order to avoid long-term drift effects associated with avalanche injection charging of the floating electrode.

2.2 Multiplying Elements

Of the various schemes to achieve electrical analog multiplication, only three merit serious consideration for integration with CTD analog delay lines: MOSFET triodes, difference of squares using MOSFET pentodes, and a combined MOSFET/bipolar log-add-antilog approach. The bipolar transconductance multiplier is analogous to the MOSFET triode, but is much more sensitive to small voltages than MOSFET's, thereby leading to a potential compatibility problem. The multipliers are described in reverse order, leading up to the MOSFET triode which has been used in all published implementations[2,3,4] to date.

2.2.1. Analog Multiplication with Logarithmic Diodes, Addition, Antilog-Transistor

The characteristic of a junction diode is given approximately as

$$I_D \cong I_s e^{\Lambda V_D} \qquad (1)$$

where I_D is the dc diode current, V_D is the dc voltage across the diode, I_s is the saturation current, Λ is a constant equal to $(38.6V)^{-1}$ at $27^{\circ}C$. This equation can be rewritten as

$$V_D = \left(\frac{1}{\Lambda}\right)\left[\ell n\left(I_D/I_s\right)\right]. \qquad (2)$$

If two currents I_{D1} and I_{D2} are fed through two separate diodes, the two voltages V_{D1}, V_{D2} across the respective diodes can be added

$$V_{D1} + V_{D2} = \left(\frac{1}{\Lambda}\right)\left[\ell n\ (I_{D1}I_{D2}/I_s^2)\right] \qquad (3)$$

Note that the sum of the voltages is proportional to the logarithm of the product $I_{D1}\ I_{D2}$. Thus, if we impress this sum across the base-emitter junction of a transistor the collector current will be proportional to the product $I_{D1}\ I_{D2}$, because the collector current of a transistor is given as

$$I_C \cong I_{cs} e^{\Lambda V_{BE}} = I_{cs} e^{\Lambda (V_{D1} + V_{D2})} \qquad (4)$$

where I_{cs} is a constant and V_{BE} is the dc base-emitter voltage which is now equal to $V_{D1} + V_{D2}$. A circuit for implementing this logarithmic addition is shown in Figure 8a. The two currents are in opposite polarity. If the common point between the two diodes is grounded, then the emitter of the multiplying transistor Q_1 should not be grounded to avoid short-circuiting the lower diode D_2. A current mirror consisting of $Q_2\ Q_3\ Q_4\ Q_5$ may be used to provide a high impedance return path for the emitter of Q_1.

This circuit has some shortcomings. First, the base-emitter voltage, being equal to the sum of the two diode voltages, would cause an excessively large collector current to flow if the device sizes of the transistor and the diodes are comparable. From equations (3) and (4), one can derive the collector current

$$I_C = \frac{I_{D1}\ I_{D2}\ I_{cs}}{I_s^{\ 2}} \qquad (5)$$

If the areas and the doping concentrations of the junctions of the diodes and the transistor are comparable, then the I_C would be orders of magnitude larger than I_{D1} and I_{D2}.

$$I_C = \frac{I_{D1}\ I_{D2}}{I_s} \qquad (6)$$

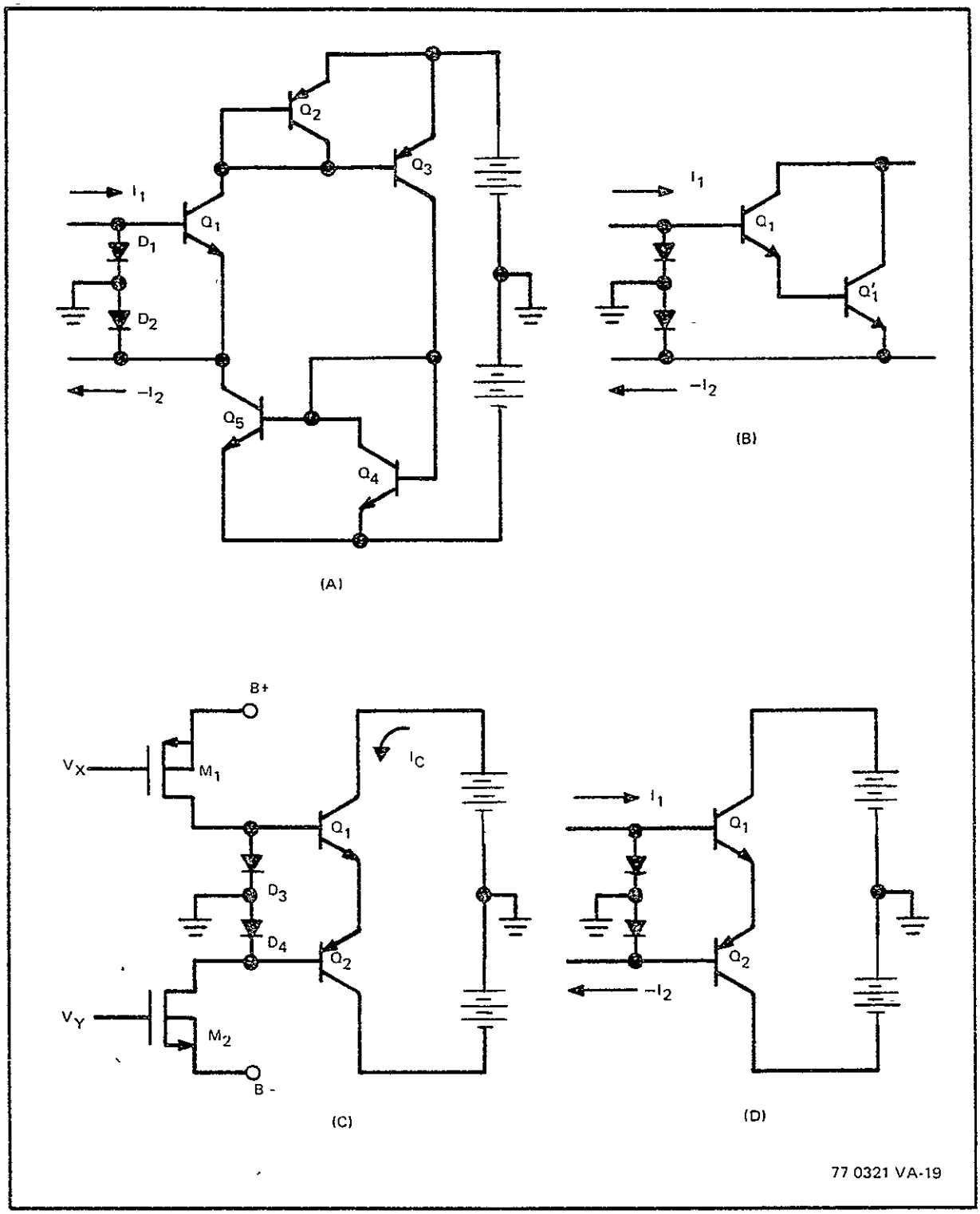


Figure 3 Various "Log-Add-Antilog" Multiplying Circuits

Since the saturation current I_s is usually much smaller than the operating current I_D, the collector current can be enormous. The foregoing problem can be solved by using two base-emitter junctions across the two diodes, such as the Darlington pair, (Q_1, Q_1') as shown in Figure 3b. However, the collector currents of the two transistors differ by a factor of β, the current gain; the respective base-emitter voltages are:

$$V_{BE1} = \frac{1}{\Lambda} \ell n \frac{I_C/\beta}{I_{Cs}} \tag{7}$$

$$V_{BE1}' = \frac{1}{\Lambda} \ell n \frac{I_C}{I_{Cs}} \tag{8}$$

Equating equations (7) and (8) with equation (3)

$$I_C = \frac{I_{Cs}}{I_s} \sqrt{I_{D1} I_{D2}/\beta} \tag{9}$$

Thus, the output current is proportional to the square root of the product of the diode currents. For linear multiplication, we should make the diode current proportional to the square of the multiplicand. Furthermore, the signal from the nondestructive readout of a CTD should preferably be applied to the gate of a MOS transistor. Thus, a MOS transistor, operating in the current saturation (pentode) region with a square-law characteristic, can be utilized to furnish both the buffering and the squaring function.

The buffered multiplier circuit is shown in Figure 3c. Note that complementary MOS transistors are used to let the drain current flow into the diode in the proper direction. The dc potentials of the gates are at ground to ensure pentode operation, so long as the

MOS transistors are enhancement-mode devices.

Another scheme for accomplishing the same purpose is to use a pair of complementary bipolar transistors as shown in Figure 3d. The output current is then

$$I_C = \left(\frac{I_{Cs}}{I_s}\right) \cdot \left(I_{D1} I_{D2}\right)^{1/2} \qquad (10)$$

In either Figure 3b or Figure 3d, it is desirable to make the base current much smaller than the diode currents. Any base current would detract from the diode current and cause deviation from the ideal logarithmic relationship. For this reason, it is desirable to have a high current gain in at least one of the transistors.

In practice, this technique involves both fabrication and performance problems. The manufacturing sequence must simultaneously yield acceptable quality devices of all of the following: CCD's, complementary MOS transistors, and complementary bipolar transistors (with the required high current gain) is hardly a well developed or widely used process. Overlooking such fabrication difficulties, one then encounters the functional problems: In Figure 3c, the voltages (V_x, V_y) from the CCD include not only the ac signals (x,y) but also biases (X_o,Y_o) representative of the zero-signal reference level. Thus, the instantaneous output from the circuit of Figure 3c may be written as

$$Z_2 = (X_o + x)\ (Y_o + y) \qquad (11)$$

To obtain the finally desired result, one must similarly generate and combine three more products:

$$xy = Z_4 - Z_3 + Z_2 - Z_1 \qquad (12)$$

where

$$Z_4 = (X_o)\ (Y_o), \quad Z_3 = (X_o + x)(Y_o), \quad Z_1 = (X_o)(Y_o + y)$$

To perform the electrical function of equation (12) simultaneously would require replicating the complete circuit of Figure 3c four times with the CMOS FET's of one such replication IDENTICALLY (not nominally) matched for all four replications so as to guarantee that the four separate sets of (X_o, Y_o) will truly be equal and cancel. That is, each such simulataneous four-quadrant multiplier would need the following sets of perfectly matched devices: 4 PMOST pentodes, 4 NMOST pentodes, 4 high-β NPN transistors with matched diodes and independent accessible nodes.

Another aspect of a correlator device based on the multiplying element of Figure 3c is the operation of the two analog delay lines with their respective non-destructive readout. For both the CMOST pentode buffers, M1 and M2, both their sources and drains are connected to low impedance nodes (practically ac virtual grounds) so that interaction from the multiplier through the buffer back into the analog delay line is negligible. But the desired pentode squaring action suggests that V_x be biased above ground while V_y be biased below ground, thereby precluding the operation of both delay lines with comparable biases and clock levels. In conclusion, however, the necessarily more

complicated fabrication sequence to obtain fully accessible, high-β complementary bipolar transistors as well as CMOST's is a powerful argument against substantial further consideration of the "log-add-antilog" type multiplying element at this time.

2.2.2 Analog Multiplication by Pentode Difference of Squares

This multiplier utilizes the square-law characteristic of an MOS transistor operating in current saturation (pentode) region. The drain current is given as:

$$I_D = K(V_{GS}-V_T)^2 \tag{13}$$

If V_{GS} is made equal to $(V_o + A + B)$ for one transistor:

$$I_{D2} = K2(V_o+A+B-V_{T2})^2 \tag{14}$$

If related signals are similarly applied to MOSFET pentode gates, we find

$$I_{D1}=K1(V_o + B -V_{T1})^2,\ I_{D3}=K3(V_o+A-V_{T3})^2$$

$$I_{D4} = K4\ (V_o- V_{T4})^2 \tag{15}$$

If four perfectly matched devices are used, (or, as we shall see later, if the four voltages are sequenced onto the same MOSFET pentode) so that

$$K1 = K2 = K3 = K4 = \text{and } V_{T1} = V_{T2} = V_{T3} = V_{T4}, \tag{16}$$

the four contributions may be combined exactly as in equation (2-12) to give

$$2K \cdot A \cdot B = I_{D4}-I_{D3}+I_{D2}-I_{D1} \tag{17}$$

The simplicity of this technique is overwhelmingly attractive from almost every aspect MOS fabrication of a single carrier type is well developed and not complicated. It would be difficult to reduce the transistor count to less than a single MOSFET pentode. MOSFET pentodes with lightly doped bodies can perform squaring efficiently. Ac virtual grounds at both source and drain of the pentode eliminate feedback from the multiplier to the CCD with no additional buffering. And finally, pentode squaring can be achieved over a fairly large range of biases. The principal limitation is implied in equation (14) which shows that the two independent quantities to be multiplied must be ADDED (or subtracted) in order to enable the multiply operation. This means that a sum of products such as

$$Z = \sum_{K=1}^{N} A_K \cdot B_K \qquad (18)$$

may easily be obtained by this technique PROVIDED the sets (A_K) and (B_K) are fixed relative to each other since each (A_K, B_K) are mixed together by addition or subtraction prior to application to the MOSFET pentode gate. Consequently, a single pentode squarer does not allow the relative motion of one data set relative to the other as needed to generate such FUNCTIONS as correlation or convolution.

This functional deficiency may be overcome by the use of a second complementary MOSFET pentode in series as shown in Figure 4, and connected to the two independent data delay lines as indicated. The drain current is proportional to the square of the sum of the two gate voltages, provided that the two transistors are in current saturation as follows.

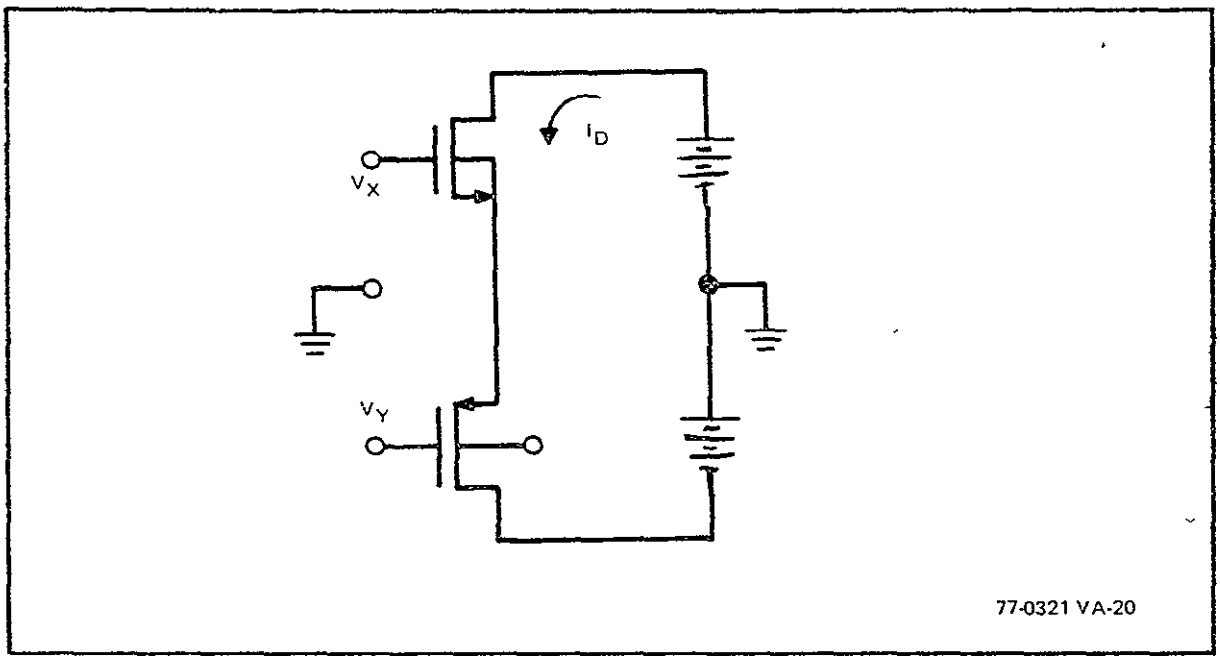


Figure 4 The CMOS Pentode "Difference of Squares" Multiplier

When two signals are applied to the gates of two series CMOS transistors, the current must be the same. If the transistors are in current saturation, the current varies as the square of the gate to source voltage. Thus, for two complementary, but not symmetrical transistors, with a ratio m for their values of K, we can represent and equate the drain currents as

$$K\ (V_I - V_S)^2 = K\ m\ (V_S - V_{II})^2 \tag{19}$$

The solution for the common source voltage is

$$V_S = \frac{V_I + m\ V_{II}}{1 + m} \tag{20}$$

and the current is

$$I_D = \frac{K\ m\ (V_I - V_{II})^2}{1 + m} \tag{21}$$

Note that the drain current remains proportional to the square of input voltage difference, so long as body effect can be ignored.

This last limitation, however, is quite serious. For conventional CMOS, where the doping of the PMOST bodies is about 1×10^{15} while that of the NMOST bodies is near 4×10^{16}, the NMOST body effect completely destroys the desired squaring action. Fortunately, the NMOST body effect can be completely eliminated by connecting each NMOST source to its respective body. The multiplying element of Figure 4 does indeed need a buffered interface from the two independent CCD analog delay lines. Since complementary source-follower action is occurring, this multiplying element can introduce interaction between the two independent data sets unless buffers are used to isolate the gates from the delay line taps. Furthermore, such buffers must be

able to provide the two independent ac signals with adequate bias separation to allow for the sum of the two threshold voltages plus the residual PMOST body effect plus the maximum signal excursion.

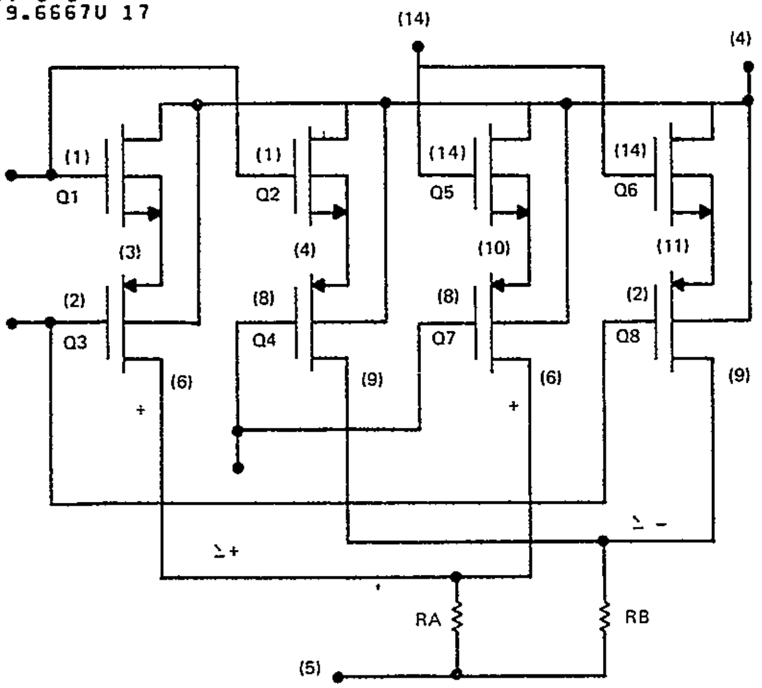
Such buffers are described in more detail in connection with their design for the triode multiplier, but we take the liberty of including some of the results here that are relevant to this CMOS, two-pentode, difference of squares multiplier. With both CCD delay line outputs at basically the same dc bias, an NMOS source follower shifts one signal in the negative direction. This NMOS buffer uses a 7 - to 10 - volt bias and needs only 18 μamps to give better than 1-MHz bandwidth for a power consumption of 180 μ watts. A depletion-mode PMOS source-follower using a 5-volt supply and drawing 20μ amps for a power of 100μ watts also gives a 1-MHz bandwidth for the other analog signal buffer. The resultant dc separation between the two signals is increased form zero to 4.5 volts. The circuit of Figure 4 was computer simulated with these results in mind. The circuit model with its operational listing are given in Figure 5, while the resultant dc operating points and the output Fourier analysis are shown in Figure 6. Equations (14) through (17) determined the circuit model with the sequencing of different signals through the series pentode pair (as in equation (16) replaced by the simultaneous or parallel arrangement shown. The spectral analysis of Figure 11 indicates a complete error rejection in excess of 50 dB. Increasing device sizes somewhat to assure a safer bias margin gives extrapolated values like 10μ amps from a 10-volt supply..

Thus, a 1-MHz CTD/CMOS difference of squares multiplying element element with about 50 dB error rejection would need (180 + 100 + 100)μ watts = 0.38 mwatts, and requires only 6 MOSFETs including buffers.

```
SQUARE LAW COMPLEMENTARY MOS CORRELATOR (SLCMC-3-9)

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

  TIME .1U 20U
  RA 6 5 10
  RB 9 5 10
  Q1 3N1 4 1 3 3 1M 2.5M 500 500 .1F .1F
  Q2 3N1 4 1 7 7 1M 2.5M 500 500 .1F .1F
  Q3 3P1 6 2 3 4 1M 2.5M 500 500 .1F .1F
  Q4 3P1 9 8 7 4 1M 2.5M 500 500 .1F .1F
  Q5 3N1 4 14 10 10 1M 2.5M 500 500 .1F .1F
  Q6 3N1 4 14 11 11 1M 2.5M 500 500 .1F .1F
  Q7 3P1 6 8 10 4 1M 2.5M 500 500 .1F .1F
  Q8 3P1 9 2 11 4 1M 2.5M 500 500 .1F .1F
  3P1 PMO VTO=-1 US=250,6E4,.15 COX=23N DNS=5E14 XJD=.3M XJS=.3M GDS=2 CSS=.5P
  3N1 NMO VTO=1 US=500,6E4,.35 COX=23N DNS=5E15 XJD=.3M XJS=.3M CDS=2 CSS=.5P
  V4 4 0 7V
  V5 5 0 -7V
  VSIN 1 0 .25V 60KHZ 0 2
  V14 14 0 2
  VSIN 2 0 .25V 300KHZ 0 -2
  V3 3 0 -2
  PLOT VOUT 6 9
  FOR 3U 19.6667U 17
  END
```



77 0321 V 23

Figure 5 Square Law Complementary MOS Correlator

```
SQUARE LAW COMPLEMENTARY MOS CORRELATOR (SLCMC-3-9)

TEMP =   300.00

NO. OF ITER. =    8

NODE VOLTAGES --
 ( 0)      .0000     ( 1)     2.0000     ( 2)    -2.0000     ( 3)     1.0332
 ( 4)     7.0000     ( 5)    -7.0000     ( 6)    -7.0000     ( 7)     1.0332
 ( 8)    -2.0000     ( 9)    -7.0000     (10)     1.0332     (11)     1.0332
 (14)     2.0000

TRANSISTOR OP. PT. --
NAME  TP       VGS              VDS              VSB              IDS(MA)
Q1    N         .9668            5.9668           .0000            .0011
Q2    N         .9668            5.9668           .0000            .0011
Q3    P       -3.0332          -8.0332          -5.9668          -.0011
Q4    P       -3.0332          -8.0332          -5.9668          -.0011
Q5    N         .9668            5.9668           .0000            .0011
Q6    N         .9668            5.9668           .0000            .0011
Q7    P       -3.0332          -8.0332          -5.9668          -.0011
Q8    P       -3.0332          -8.0332          -5.9668          -.0011

RESISTOR CURRENTS --
NAME     CURRENT (MA)       POWER (MW)
RA        .002290514         .00000005
RB        .002290514         .00000005

FOURIERANALYSIS IN   17 HARMONICS FROM   .3003-05 TILL   .1967-04 SECONDS

ORDER HARM    DSINE          COSINE          MAGNITUDE    REL MAG     PHASE
    0          .0000          .6530-11        .6530-11      1.2127      .0000
    1          .1848-09       .5058-09        .5385-09    100.0000    -20.0694
    2         -.1090-09       .5519-11        .1092-09     20.2723     87.1021
    3         -.1662-09       .8766-10        .1879-09     34.8978     62.1965
    4         -.1791-06       .3335-07        .1822-06  33824.9175     79.4499
    5         -.1914-09       .2902-09        .3393-09     63.0114     34.3270
    6         -.9557-07       .1530-06        .1753-06  32554.5704     29.2145
    7         -.2042-10       .1996-09        .2009-09     37.3024      5.8351
    8          .9637-10       .2843-09        .3002-09     55.7398    -18.7264
    9         -.2076-09       .2262-10        .2088-09     38.7808     83.7809
   10          .7098-10       .1337-09        .1513-09     28.0959    -27.9347
   11         -.1716-09       .2165-09        .2762-09     51.2986     38.4150
   12          .2774-10       .1140-09        .1173-09     21.7912    -13.6734
   13          .2167-10       .1453-09        .1469-09     27.2768     -8.4835
   14          .1491-10       .1287-09        .1296-09     24.0645     -6.6051
   15          .2333-10       .1376-09        .1396-09     25.9230     -9.6205
   16          .1009-10       .1374-09        .1378-09     25.5891     -4.1990
   17          .1790-10       .1354-09        .1366-09     25.3608     -7.5292
RUN TIME =   5.000 SECONDS
```

77-0321 V-24

Figure 6 Results of CMOS Square Law Correlator

Furthermore, the pentode squaring action does not require extremely critical biases or balancing which we will find to be a serious problem with triode multipliers. On-chip, monolithic signal-summation from the drain of pentodes (like current sources) is significantly easier than summing currents in an on-chip voltage -controlled ac-virtual-ground node. The implementation of the needed sequencing and an attractive block diagram to perform the above multiplication will be presented in a later section.

Although the preceding description appears extremely attractive, two potential problem areas have been submerged therein. First, in Figure 5, one notes the doping levels used for the CMOS fabrication: Starting material of $5X10^{14}cm^{-3}$ with the complementary isolation tubs implanted and driven to give a value of $5X10^{15}cm^{-3}$. Such very light doping seems to be the only way to achieve the needed pentode squaring by the NMOST devices because typical levels of $4X10^{16}cm^{-3}$ give very poor pentode squaring. Secondly is the difficulty of obtaining such devices for laboratory evaluation of the pentode squaring action, since such a CMOS process is a deviation from well developed techniques and would require some adjustment of the fabrication steps.

Consequently, we feel that the CMOS difference of squares approach certainly warrants more investigation than computer modelling; but the likely need for some fabrication process development suggests it is a slightly higher risk approach relative to the triode technique, which does not need fabrication development and thereby provides more rapid chip development albeit at the expense of chip power consumption.

2.2.3 Analog Multiplication by MOSFET Triode

The multiplication function can be performed with MOS transistors operating in the triode region. The drain current I_D of an MOS transistor can be approximated as

$$I_D = \alpha(V_{GS} - V_T)V_{DS} + \beta V_{DS}^2 \qquad (22)$$

where V_{GS} is the gate to source voltage, V_T is the threshold voltage, V_{DS} is the drain to source voltage and (α,β) are physical parameters proportional to the width to length ratio and mobility of the channel When the drain to source voltage is small

$$I_D \approx \alpha(V_{GS}-V_T)V_{DS} \qquad (23)$$

If V_{GS} and V_{DS} represent two signals, then the drain current has a term $(\alpha\ V_{GS}\cdot V_{DS})$ which is proportional to the product of the two signals. If the two signals represented by V_{GS} and V_{DS} are substituted in equation (22) or equation (23) there are terms other than the desired multiplied outputs such as $\alpha\ V_{DS}\cdot V_T$ or $\beta/2\ (V_{DS})^2$. These extraneous components of the drain current can be reduced in a balanced multiplier as shown in Figure 12. But the signals may contian dc biases which must eventually be eliminated. One signal is given as V_x sin θ with a dc offset V_X. The other signal is V_y sin ϕ with a dc offset V_Y. The signal $V_X + V_x$ sin θ is applied to the common drain of QM and QR via the buffer (QA, QL). The signal $V_Y + V_x$ sin ϕ is applied to the gate of QM, but only the offset voltage V_Y is applied to the gate of QR.

The currents of QM and QR can be obtained by substituting in Eq. (22) $V_X + V_x \sin\theta$ as V_{DS} and $V_Y + V_y \sin\phi$ as V_{GS} for QM and V_Y as V_{GS} for QR.

$$I3 = IM = \alpha_M \left[(V_Y + V_y \sin\phi - V_{TM})(V_X + V_x \sin\theta)\right] \beta_M \left[(V_X + V_x \sin\theta)^2\right] \quad (24)$$

$$I4 = IR = \alpha_R \left[(V_Y - V_{TR})(V_X + V_x \sin\theta)\right] + \beta_R \left[(V_X + V_x \sin\theta)^2\right] \quad (25)$$

The differential output current I_{DO} is obtained by subtracting equation (25) from equation (24), assuming identical physical parameters ($\alpha_M=\alpha_R, \beta_M=\beta_R$) and a threshold difference $\Delta V_T = V_{TR} - V_{TM}$:

$$I_{DO} = IM - IR = \alpha V_x V_y \sin\theta \sin\phi + \alpha\left[V_X V_y \sin\phi + (V_X + V_x \sin\theta)(\Delta V_T)\right] \quad (26)$$

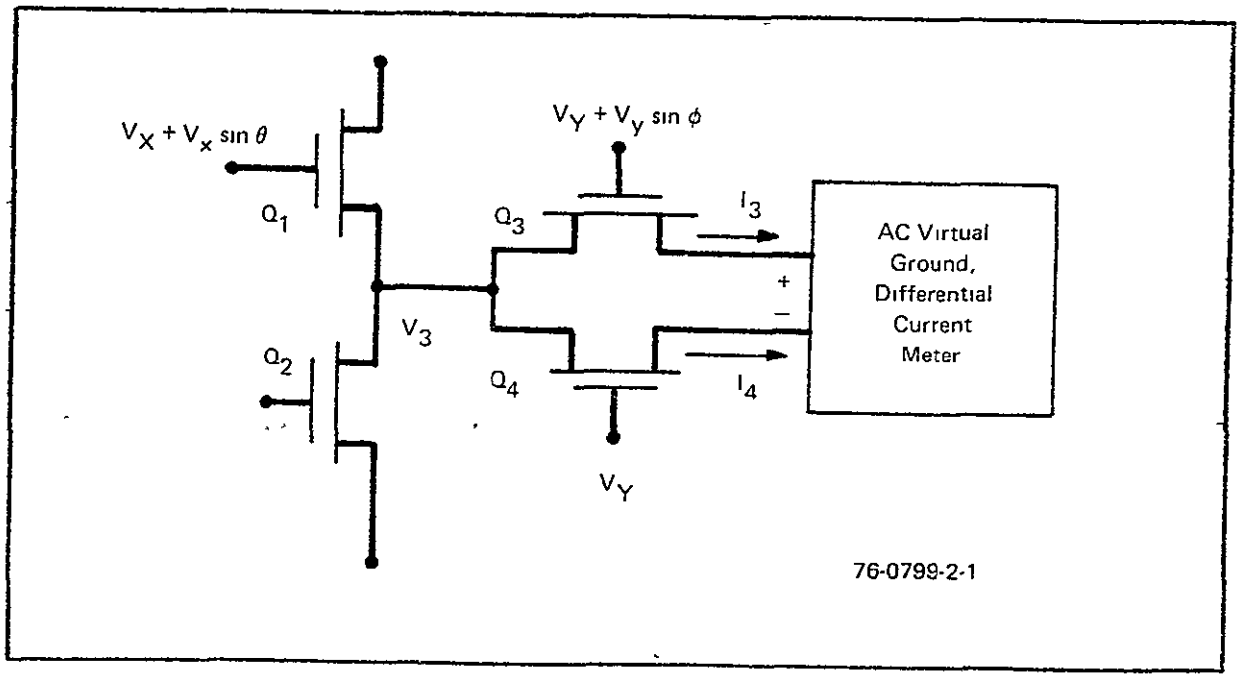


Figure 12 Conceptual Singly-Balanced Triode Multiplier

From this last equation, several important conclusions can be drawn. First, we see that any mismatch between the nominally balanced pair of MOSFET triodes such as threshold (ΔV_T), or equivalently their dc bias, contributes to the differential output a term which is directly proportional to the signal applied between drain and source of the triode. Next we see that any dc component of the drain/source voltage, V_X, contributes an output term which is directly proportional to the voltage difference between the gates of the two triodes, (QM, QR). These two observations lead us even further into the question:

How can a MOSFET triode pair be operated in practice to minimize the undesired output contributions fed through directly from the input signals in proportion to the extent of unbalance between the two MOSFET's?

This problem area we shall refer to as the rejection of input feedthrough due to a lack of precise or detailed differential balance arising mostly from MOSFET array threshold (and other) non-uniformities, which will be discussed in more detail in section five.

3.0 MULTIPLIER BIAS CONCEPTS

The existing partially-integrated singly-balanced-triode-multiplier correlator chips [2,4,5] have demonstrated the need for elaborate routines for operator-controlled, off-chip optimal biasing because of two distinctly different reasons: for best triode multiplication, the source to gate bias should be much larger than the source to drain bias which sould be as close to zero as practical. Consequently, user appeal is much enhanced by use of circuits and architecture which automatically provides on chip the following: (1) Zero soruce-drain bias and balanced source-gate biases for triode multipliers, (2) adequate offset for triode source-gate bias or the complementary gates for the CMOS pentodes difference of squares multiplier.

3.1 Triode Self-Bias

An illustrative example of one way to automatically set the bias on a MOSFET triode multiplier is given in Figure 13. In addition to the CTD stages propagating the actual data, nominally identical reference stages containing only the ZERO signal reference levels (e.g., X_o, Y_o) provide two reference levels: (1) Y_o sets the dc level applied to the gate of the reference triode, QR, to the approximate dc value on the gate of QM; (2) X_o sets the dc potential (V_s) of the "virtual ground" current-summing-node to approximate equality with the dc potential applied to the triode drains, V_D. It is important to note this self-bias concept optimally biases the triode multiplier array; that is, over the array, the average unbalance between individual sources and drains or between gate pairs goes to an acceptably small value. But the concept of Figure 8 by itself,

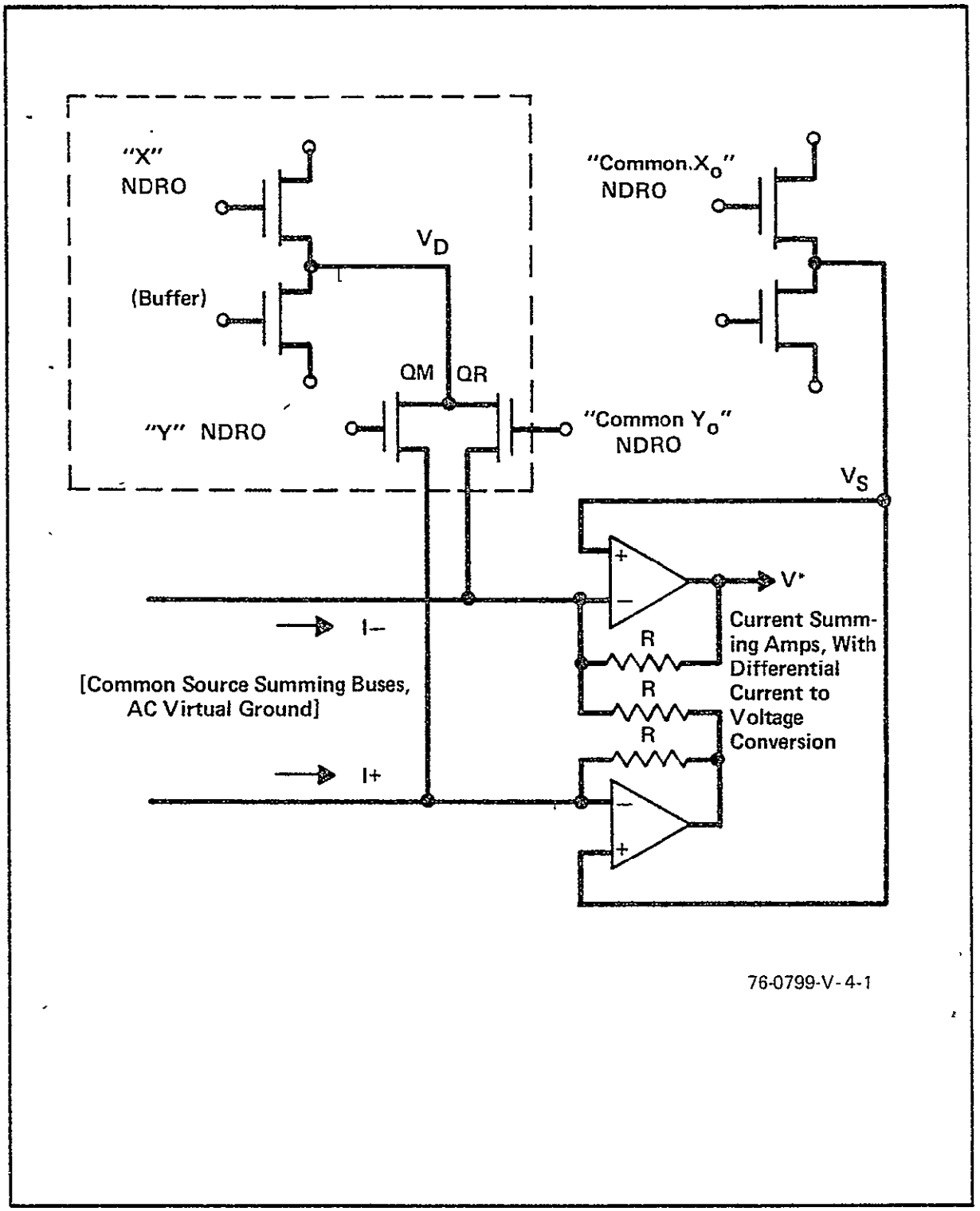


Figure 8 MOS Analog Triode Multiplier Array Self-Bias Concept

does not achieve the detailed differential balance of each multiplier within the array needed to give a high rejection of input feedthrough.

When no provision is made for any self-bias scheme, either like that illustrated in Figure 8 or some alternative, each such partially integrated device[2,4,5] required IN-SITU biasing and fine adjustment. A frequently used technique for such fine adjustment is the spectral analysis approach implied in equation (26); that is, two different sine waves are applied to the device and the output spectrum is monitored while the biases are adjusted. The dc value of the virtual ground summing node is set to minimize the feedthrough of the sine wave applied to the gates of the multiplier, thereby yielding the minimum average source/drain bias across the array. For singly-balanced triode multipliers, as illustrated in Figure 7 and 8 , where dc is applied to the gate of the reference triode, QR, the dc gate-bias for QR is likewise operator adjusted to minimize the feedthrough of the sine wave applied to the triode drains - thus giving the minimum average offset between multiplier gate pairs (inclusive of thresholds), but not necessarily balancing any pair perfectly. This routine for operator optimum biasing must be repeated whenever the conditions forthe CTD analog delay line are changed so as to affect the signals from the NDRO buffers, if input feedthrough rejection is to be maintained at its maximum value. Most practical system applications for such analog/analog convolvers would not be able to tolerate such a bias adjustment routine On the other hand, use of such a routine greatly facilitated partially integrated devices[2,4,5] demonstrating the basic principle of CTD/MOSFET-triode correlator action.

3.2 Complementary Buffers

In addition to the preceding feature desired by large systems users, another user attraction is ability to operate both analog delay lines with comparable voltage levels.

To permit such operation, the gate and drain buffer dc output levels can be used to properly bias the MOSFET triode multiplier which needs: small impedance (large conductance) for the drain buffer, minimal bias of drain to source, large bias from gate to (source, drain). We now must add the consideration of low power operation which most strongly affects the drain buffer, since that circuit must be able to supply the triode drain current. Assuming the simplicity of enhancement mode FET's with a CTD NDRO bias of V_G, one quickly finds that the two options become:

$$\underline{\text{Source Follower}}: \quad g_m = \frac{2I_o}{(V_G/2)-V_T}, \quad \text{Power} = I_o V_G$$

$$\text{Inverter}: \quad g_m = \frac{2I_o'}{V_G-V_T}, \quad \text{Power} \geq 2I_o' \; V_G \text{ (for unity gain)}$$

Requiring equal g_m gives us

$$I_o' = \frac{V_G - V_T}{(V_G/2) - V_T} \cdot I_o$$

Thus to give the same output drive, with the same gain, an inverter consumes more than twice as much power as a source follower, thereby dictating the use of a source follower to drive the triode drains.

Buffer configurations to bias the multiplier triode follow directly from the last observation. Source follower stages generally shift the output dc level toward the potential of their body. Extrapolating these generalities to CMOS circuits, we easily

see a signal applied to an NMOS source follower is shifted toward its body voltage and away from the voltage of the common PMOS body. Tabulated below are the preferred buffer configurations to give the needed triode bias:

Buffer	Singular MOS	CMOS
Drain	Source Follower	Source Follower
Gate	Inverter	Complementary Source Follower

4.0 DISTORTION ERROR TERMS FOR TRIODE MULTIPLIERS

Since the computation for the product by any REAL, CTD-compatible multiplier is necessarily imperfect, one must describe the various possible sources of errors. A very sensitive technique to study error source is spectral analysis. The application of two distinct sinusoidal signals to an ideal multiplier or correlator gives a well defined output, especially in the spectral or frequency domain. The amplitude of any other frequency components in the output (such as harmonics or higher intermodulation products) is a measure of an associated error source in the multipliers. In this section, we consider three such "harmonic" sources of error.

4.1 "Gate Signal" Harmonics form the Drain Buffer

In Figures 7 and 8, the common (drain) conductance node is driven by a source-follower MOSFET stage with both transistors in the pentode mode (characterized by a squaring relationship between gate-source voltage and drain current). In a singly balanced multipler, the modulated conductance forces the source-follower drain driver to supply a current related to the signals applied to the gate of the modulated conductance. If the transconductance of the source-follower drain driver $\left(g_{mB}\right)$ is inadequate compared to the modulated conductance g an erroneous voltage harmonically related to the multiplier gate signal is added to the common (drain) conductance node. This result may be expressed in formulas as follows: Let

$$R_{OB} = 1/g_{mG} = \frac{1}{\mu C_{ox}} \left(\frac{L}{W}\right)_B \frac{1}{(V_{GS} - V_T)_B} \qquad (27)$$

be the output impedance of the drain buffer. Then a voltage $I_{xy} R_{OB}$ would appear at the drain:

$$I_{xy}R_{OB} = \alpha_m V_x V_y R_{OB}, \text{ where } \alpha_m = \mu C_{ox} \left(\frac{W}{L}\right)_M . \tag{28}$$

When multiplied by the gate signal V_y, an undesired product current is produced:

$$I = \alpha_m V_y (\alpha_m V_x V_y R_{OB}). \tag{29}$$

This current should be much less than the desired product current $\alpha_m V_x V_y$. Since the distortion described by equation (29) is clearly associated with the signal applied to the gate, even through the drain driver is the cause of the problem, let us define a gate signal distortion rejection ratio, Γ_g:

$$\Gamma_g = \frac{\alpha_m V_x V_y}{\alpha_m V_y (\alpha_m V_x V_y R_{OB})} = \frac{1}{\alpha_m V_y R_{OB}} \tag{30}$$

or

$$\Gamma_g = \frac{(W/L)_B \cdot (V_{GS} - V_T)_B}{(W/L)_m \cdot V_y}$$

For the purposes of giving examples, let us assume a desired rejection of 40 dB (i.e., 1%). Thus, for example, if one assumes the geometric ratio of MOSFET's in equation (21) to be 50 with a typical source follower bias $(V_{GS} - V_T)_B \simeq 2$ volts, one obtains

$$y_{max} \simeq 1 \text{ volt for } \Gamma_g = 100.$$

4.2. "Drain Signal" Harmonics from the Gate Buffer

The previous section shows one absolute requirement for the buffer used to drive the drain of the triode. The parameters of this particular buffer relative to the multiplier triode, the

buffer's bias and the ac signal on the triode gate, mutually determine the gate signal distortion rejection ratio, Γ_g, as in equation (30). But, in some cases buffers to drive multiplier gates may serve only to provide reverse isolation to prevent signals within the multiplier from adversely affecting analog delay within the associated CTD. Even though some nondestructive readout schemes circumvent such a problem, the following related difficulty can occur.

Any impedance in series with the gate of the multiplier can develop a voltage by virtue of the feedthrough capacitance from the drain of the multiplier transistor. If the multiplier gate signal is directly derived from the floating gate of a CCD with sensing capacitance, C_{FG}, the impedance of the driver is the impedance of the capacitance C_{FG}. The voltage feedthrough is equal to $V_x C_{gdm}/C_{FG}$, where C_{gdm} is the multiplier triode gate to drain overlap capacitance. If the desired signal is V_y, the rejection ratio limited by gate interaction is simply

$$\frac{V_y C_{FG}}{V_x C_{gdm}} = RR(G) \tag{31}$$

One way to reduce the adverse effect of the feedthrough from the drain to the gate of the multiplier transistor is to place a buffer between the floating gate of the CCD and the gate of the multiplier. Since the gate buffer output impedance is approximately $1/(g_m)_{GB}$, the feedthrough signal from the drain now becomes

$$\frac{1}{\frac{1}{j\,C_{gcm}} + \frac{1}{(g_m)_{GB}}} \times \frac{1}{(g_m)_{GB}} \tag{32}$$

Thus the gate buffer changes equation (31) to

$$RR(G) = \frac{V_y}{V_x} \cdot \left[1 + \frac{(g_m)_{GB}}{j\omega C_{gdm}} \right] \qquad (33)$$

Typically, for $C_{gdm} \leq 0.02$ pF and one megahertz, the overlap coupling becomes 126 nanomhos, which may be easily buffered by minimal FET stages of ten to a hundred micromhos.

Consideration of the buffer frequency response gives a further condition related to that of equation (33). If GC is the gate buffer corner frequency, we have

$$f_{GC} \cong \frac{(g_m)_{GB}}{2\pi\ (C_{GBM} + C_{GP})} \qquad (34)$$

where C_{GBM} is the multiplier gate to body capacitance and C_{GP} is the parasitic capacitance on the multiplier gate node. Combining equations (33) and (34) gives

$$RR(G) = \frac{V_y}{V_x} \cdot \left[1 + \frac{C_{GBM} + C_{GP}}{j\ C_{gdm}} \cdot \frac{f_{GC}}{f} \right] \qquad (35)$$

Equation (35) suggests that self-aligned polygate technology could help reduce C_{gdm} and the transconductance of the gate buffer, $(g_m)_{GB}$, must be designed to give the needed rejection at the maximum operating frequency. Failure to observe this precaution will contribute an error term behaving like the square of the drain signal and thus becomes almost indistinguishable from the triode nonlinearity of an overly large drain signal, which is described immediately below.

4.3 "Drain Signal" Harmonics from the Multiplying Triode

To evaluate drain signal distortion rejection ratio, r_d, we require that the MOSFET multiplier always be well into the triode

region. Furthermore, we assume Γ_d is directly related to that triode characteristic; or for the worst case:

$$2(V_{GS} - V_T)_m \geq \Gamma_d (V_{DS})_m \tag{36}$$

This assumption is very simplistic since the triode drain-gate coupling of equation (33), which causes the same functional distortion, is not incorporated. At this point we must start including quantitatively such array problems as threshold voltage nonuniformity, the average value of which we designate by ΔV_T. In predicting the worst case for equation (36) we must assume the self-bias technique can result in dc errors comparable to ΔV_T. Thus, equation (36) may be written

$$\sqrt{2(Y_o - V_{T_m} - \Delta V_T - y_{max})} \geq \Gamma_d (\Delta V_T + x_{max})$$

or

$$(\Gamma_d/2)x_{max} + y_{max} \leq (Y_o - V_{T_m}) - (1 + \Gamma_d/2)(\Delta V_T). \tag{37}$$

Consequently, equations (30) and (37) prescribe upper limits on signal levels in terms of array nonuniformities, geometry, biases, and distortion rejection ratios.

5. ARRAY THRESHOLD NONUNIFORMITIES

At the end of section two, we saw how signals applied to a balanced triode multiplier were fed directly through to the output due to imperfect matching caused by typical array threshold non-uniformities.

5.1 Input Feedthrough Rejection, ψ, for Balanced Triodes

We must now apply equation (26) to an array of matched triodes using the self-bias technique to give an average source-drain dc value of ΔV_T with the applied ac signals written as (x,y) yielding:

$$I_{D0} \cong \alpha_m [xy + y(\Delta V_T) + x(\Delta V_T)]$$

Taking the ratio of the desired signal to the undesired input feed-through from equation (38) gives the rejection, ψ, which limits the minimum usable (x,y):

$$(x_{min}, y_{min}) \approx \psi \cdot (\Delta V_T).$$

Thus, for a typical $\Delta V_T \simeq 0.1$ volt and a desired input rejection of 40 dB, one finds $(x_{min}, y_{min}) \simeq 10$ volts. This result alerts us to a significant technical problem: each matched triode pair must undergo a detailed balance which self-bias cannot provide if there is to be any hope of achieving acceptable values of input rejection.

5.2 Compensation by Feedback in Floating Gate Reset

In this section, consider nondestructive readout only by means of floating gates. If one could selectively address and adjust the dc bias on each floating gate sensor, then one may postulate the following operation. After loading both CCD shift registers with zero-signal, reference-level-only charge samples, a "unit one" sample is

propagated through one of the delay lines. The output of the correlator to such a "unit one" is a random pattern which measures the nonuniformities from stage to stage of the other delay line for the combination of both the floating gate sensor and its associated buffer. If now a feedback loop were closed from the correlator output through a selective switch addressing only the stage associated with the "unit one", the feedback amplifier could sense any deviation of the correlator output from a prescribed fixed level and, thence, adjust the bias on that selected floating gate to obtain a null before moving on to the next stage. Theoretically, this could be iterated for both channels so as to completely compensate for threshold nonuniformities everywhere in the array.

In practice, however, several problems appear likely. The published data [2,3] and other estimates indicate that compensation of threshold nonuniformities must fall in the range of 40 to 60 dB to enable even a remote chance of obtaining any usable input dynamic range. Since typical MOS nonuniformities are about 100 millivolts, switched feedback control to better than 1 millivolt is thus called for. But operation of the selective/address feedback switches introduce feedthroughs (even when shielded) due to parasitic and channel coupling capacitance comparable to or larger than a millivolt. Furthermore, such a feedback scheme requires an exclusive "house-keeping" interval; and the compensation stays valid only for short periods of time as thermal leakage fixed patterns destroy the feedback settings very rapidly at MIL Spec temperatures. In contrast, the sequential multiply process

continuously compensates for threshold nonuniformities independent of ambient temperature to better than 50 dB accuracy, as we see in subsequent sections.

5.3 Compensation with the Sequential Multiply Operator

The use of CTD's to provide analog delay with nondestructive readout necessarily requires sensing by means of FET gates with all their attendant array threshold nonuniformities. This alone is a strong argument for a sequential approach whereby a calculation is performed in parts, serially, using the same device elements as well as "zero-signal reference levels for each contributory computation, independent of the functional form of the multiplying element. Traditionally, highly accurate multipliers in analog computing technology used time division multiplexing between the signals and selected references. Equations (11) and (12) suggest the sequential scheme for any ideal multiplier. We now describe the operation in detail and derive some of the extra benefits the technique offers for the triode multiplier.

In the sequential multiplying scheme, all the undesired product terms associated with the dc "fat-zero" or threshold voltage deviations are cancelled sequentially in the same multiplying transistor. The discrete/hybrid circuitry for accomplishing this time cancellation is shown in Figures 9 through 12. In both the X and Y CTD channels, samples of signals' ac-zero reference level only (X_o, Y_o) and reference-plus-signal" $|(X_o + x), (Y_o + y)|$ occupy alternate stages. The product current (I-) due to the common(Y_o) multiplied by X-channel signals is balanced against the product current (I+) due to Y-channel signal multiplied by X-channel signals. All the incremental (I-)'s are fed to a summing amplifier and the (I+)'s to another summing amplifier, to give

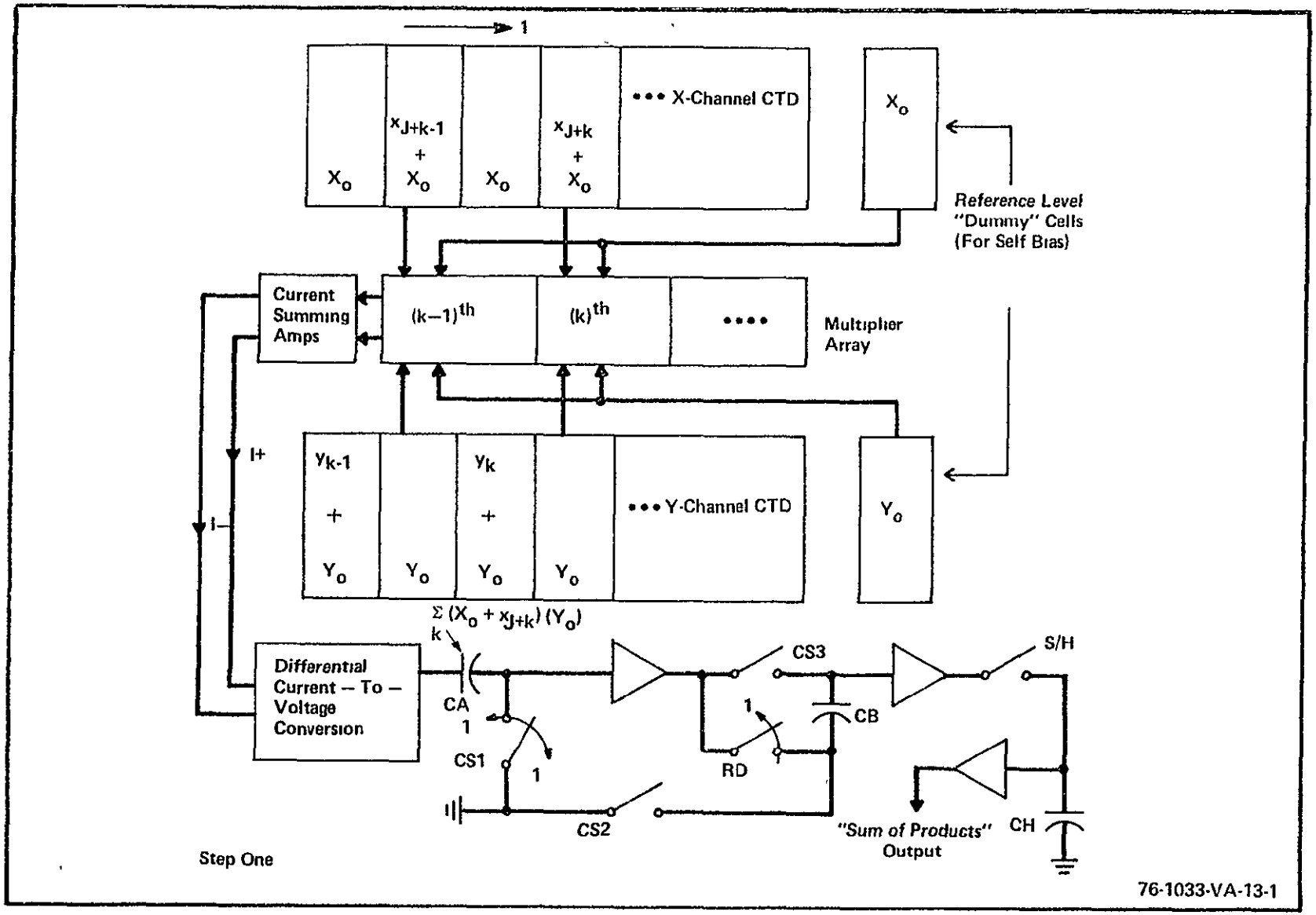


Figure 9 Step One of Sequential Multiply Operation

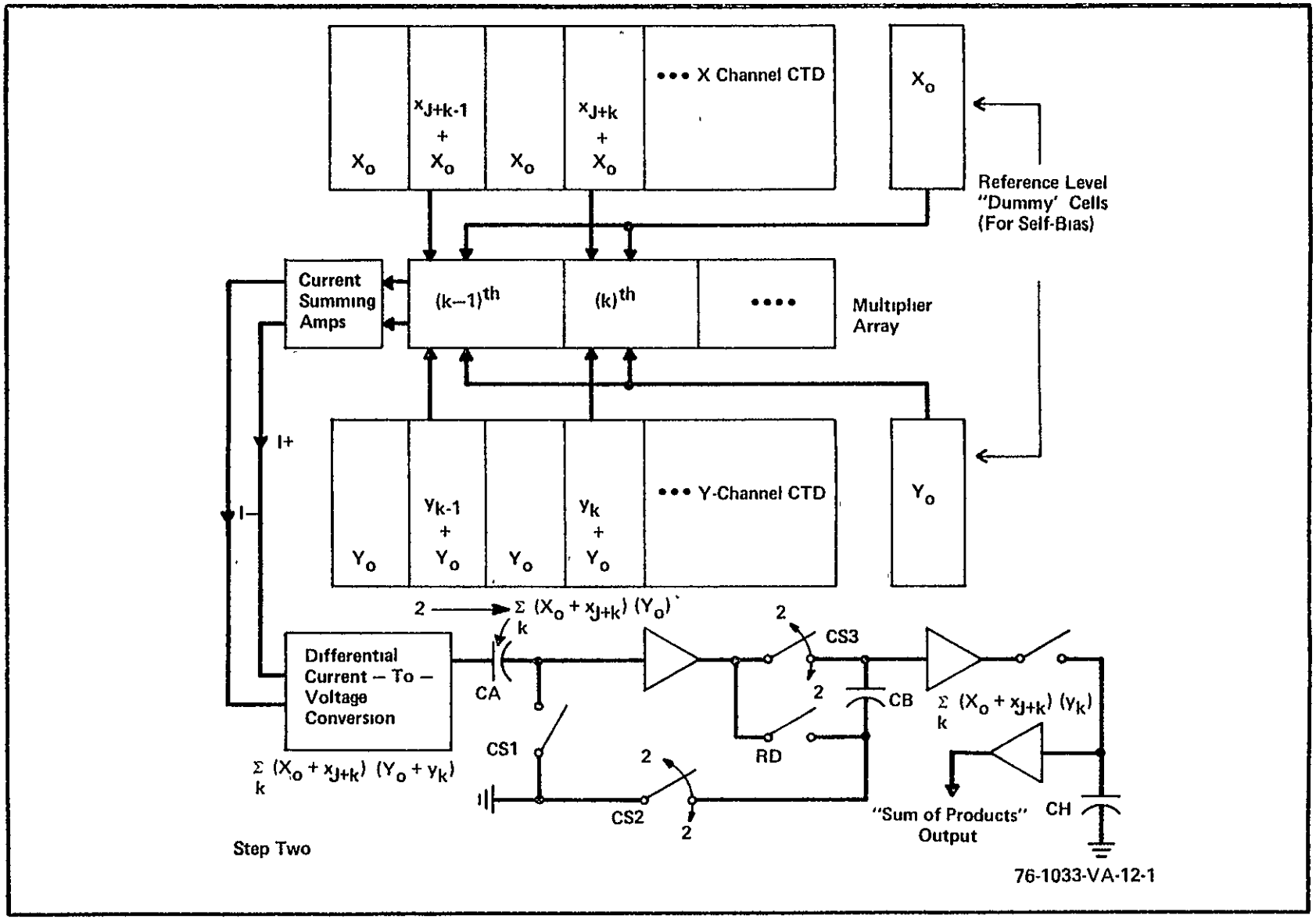


FIGURE 10 Step Two of Sequential Multiply Operation

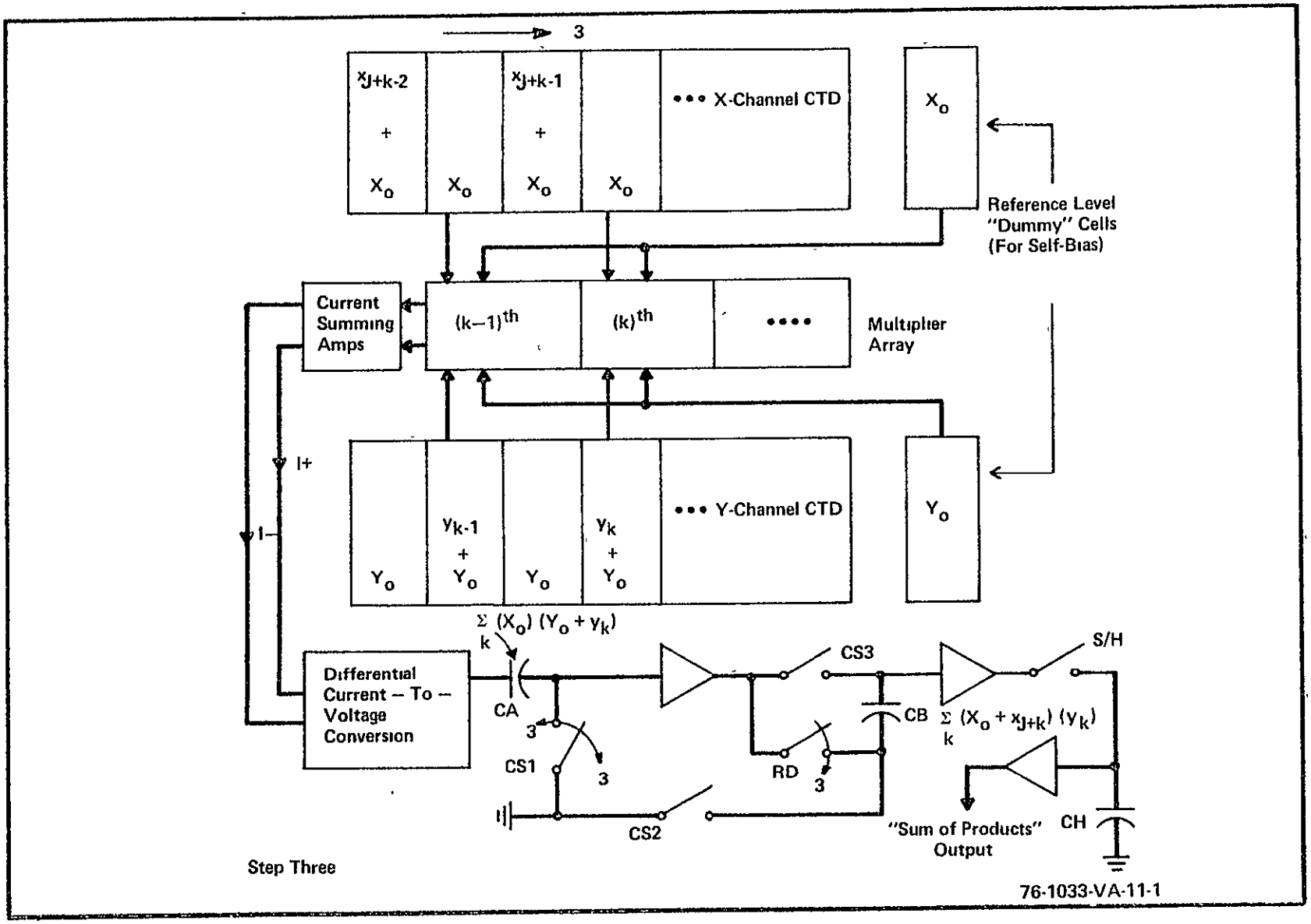


FIGURE 11 Step Three of Sequential Multiply Operation

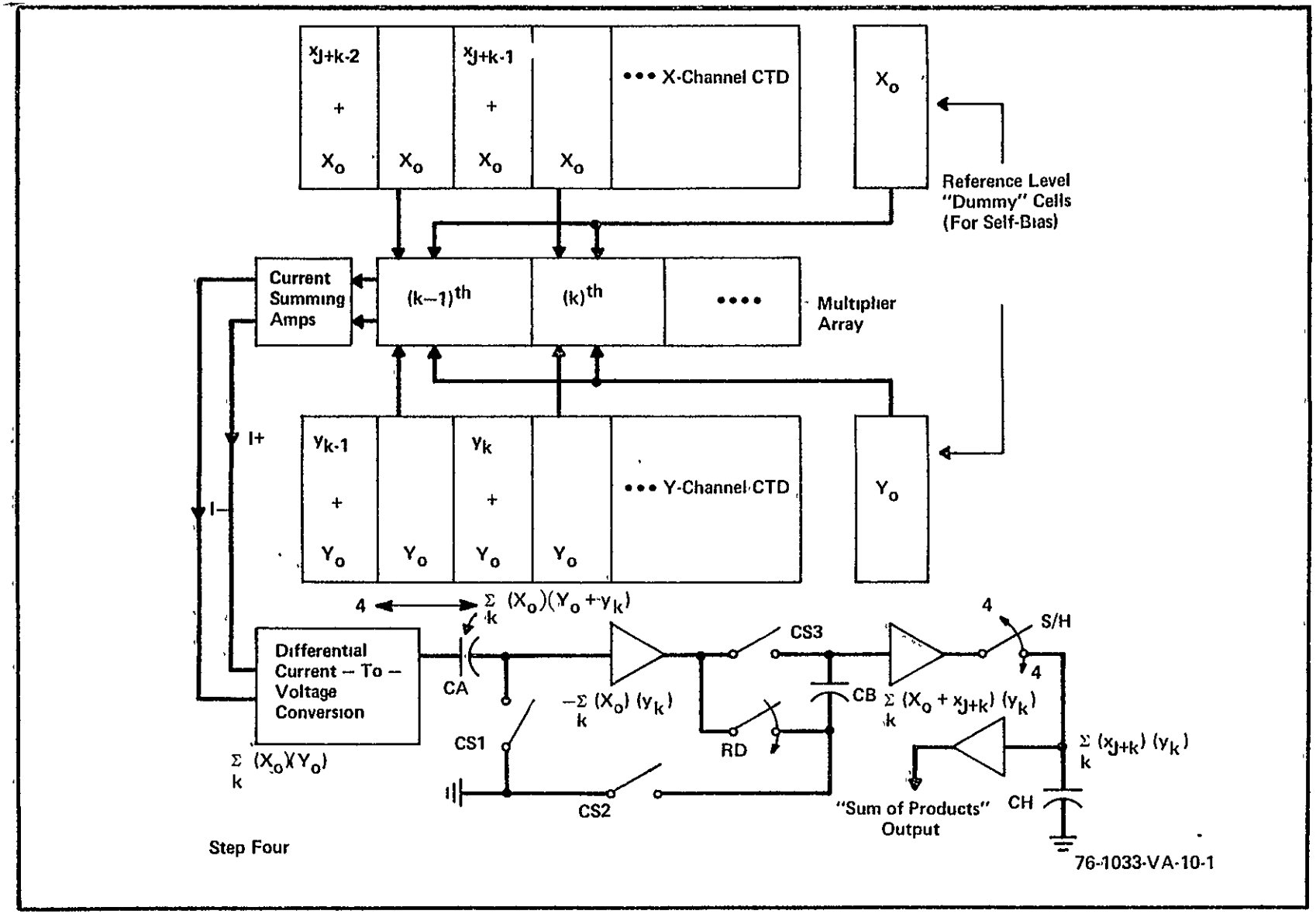


FIGURE 12 Step Four of Sequential Multiply Operation

the differential output currents, $\Delta I(t) = \Sigma |(I+)(t) - (I-)(t)|$.

The signal samples $x_{(J+K-1)}$, $x_{(J+K)}$,...are separated by common ....X_o and Y_o respectively. To multiply the quantities x_{J+K}, and y_k, four steps are required: The X-channel signals are advanced with respect to the Y-channel signal, as illustrated in figure 9 . In the first step, the signal in X-channel CTD is transferred forward by one stage with respect to the Y-channel.

The signal sample $x_{(J+k)}$ is multiplied by the common Y_o. The product current is:

$$I+(1) = \sum_{k=1}^{N} [\alpha_k^+ (Y_o - V_{T+}^k) (x_{J+k} + V_{TX}^k - V_{TX}') + \beta_k^+ (x_{J+k} + V_{TX}^k - V_{TX}')^2] \quad (40)$$

where k indicates the k^{th} multiplier,

V_{T+}^k is the equivalent threshold voltage of the k^{th} multiplying MOS transistor.

V_{TX}^k is the equivalent threshold voltage of the k^{th} source follower buffer.

V_{TX} is the equivalent threshold voltage of the common/dummy source opening of switch CS1, as in figure 9 .

In the second step, the Y-channel is advanced with respect to the X-channel and the signal $Y_o + Y_k$ is multiplied by the unchanged $x_{(J+k)}$ to give the summation current:

$$I+(2) \sum_{k=1}^{N} [\alpha_k^+ (Y_o + y_k - V_{T+}^k) (x_{J+k} + V_{TX}^k - V_{TX}') + \beta_k^+ (x_{J+k} + V_{TX}^k - V_{TX}')^2] \quad (41)$$

The switches are now set as in figure 10 such that the previous value associated with equation (2-63) subtracted from the new value equation (41) difference value:

$$[I + (2)] - [I + (1)] = \sum_{k=1}^{N} [\alpha_k^{+} (y_k) (x_{J+k} + V_{TX}^{k} - V_{TX}')] \qquad (42)$$

clamped directionally onto capacitor CB by the operation of the switches CS2 and CS3. Note that equation (42) depends on only a single multiplying transistor at each multiplier location and is basically identical to equation (26) for the balanced multiplier.

In the third step shown in figure 11 the X-channel signals are advanced with respect to the Y-channel signal. The y-channel signal $Y_o + y_k$ is multiplied by the common X_o. The summation current,

$$I + (3) = \sum_{k=1}^{N} [\alpha_k^{+} (Y_o + y_k - V_{T+}^{k}) (V_{TX}^{k} - V_{TX}) + \beta_k^{+} (V_{TX}^{k} - V_{TX}')^2] \qquad (43)$$

gives a third output which is clamped onto CA by means of CS1 as in the first step. Prior to the fourth step, read switch RD is closed as in Figure 11, so that value stored on CB adds to the output of the preceding amplifier.

In the final step as illustrated in Figure 12, the Y-channel signal may be either advanced, if a completely new vector dot-product is desired, or receded with respect to the X-channel, if additional dot-products with the same replica vector are desired, as for correlation or convolution functions. The common X_o and common Y_o are multiplied. The summation current is

$$I + (4) = \sum_{k=1}^{N} [\alpha_k^{+} (Y_o - V_{T+}^{k}) (V_{TX}^{k} - V_{TX}') + \beta_k^{+} (V_{TX}^{k} = V_{TX}')^2] \qquad (44)$$

As in the second step, the value stored on capacitor CA from step 3 subtracts from the fourth partial output, to give a second difference which is added to the first difference (as stored on capacitor CB) for a final four-quadrant sum of products output.

$$V_{out}(J) = R\,\Delta I = [\,\Delta I(4) - \Delta I(3) + \Delta I(2) - \Delta I(1)]$$
$$= R \sum_{k=1}^{N} a_k^{+}\, x_{J+k} y_k \qquad (45)$$

NOTE THAT ONLY THE DESIRED SIGNAL PRODUCT APPEARS AT THE OUTPUT, WITH MULTIPLIER "PURE DRAIN-SOURCE NONLINEARITIES" ALSO CANCELLED. THUS, IN THIS MANNER, THE SEQUENTIAL PROCESSOR ENHANCES THE DRAIN HARMONIC DISTORTION REJECTION, Γ_d, FOR THE SINGLY-BALANCED TRIODE.

5.4 A Balanced-Input Monolithic Sequential Processor

A monolithic implementation of the sequential processor described above is illustrated in Figure 13. The inherent differential action of the "fill/spill" input technique is used to subtract the applied balanced signals. A built-in bias-charge potential barrier, V_B, is used to guarantee that balanced signals of either sign can be processed.

Thus, when charge is metered and read while switch ϕ_o is activated, the quantity of charge is given by $Q^* = (CIN) \cdot (V_B)$ where the effective input capacitance is given by CIN = COX + CG2 + CIG'. The resultant potential increment on the output collecting diode, DOUT, and hence, the output capacitance for that node, COUT, is given by $V_{out} = \frac{Q^*}{C_{out}} = \left(\frac{CIN}{COUT}\right) \cdot \left(V_B\right)$, with an associated device gain of $G = \frac{CIN}{COUT}$ If multiple charge packets (such as N) are metered and collected on the

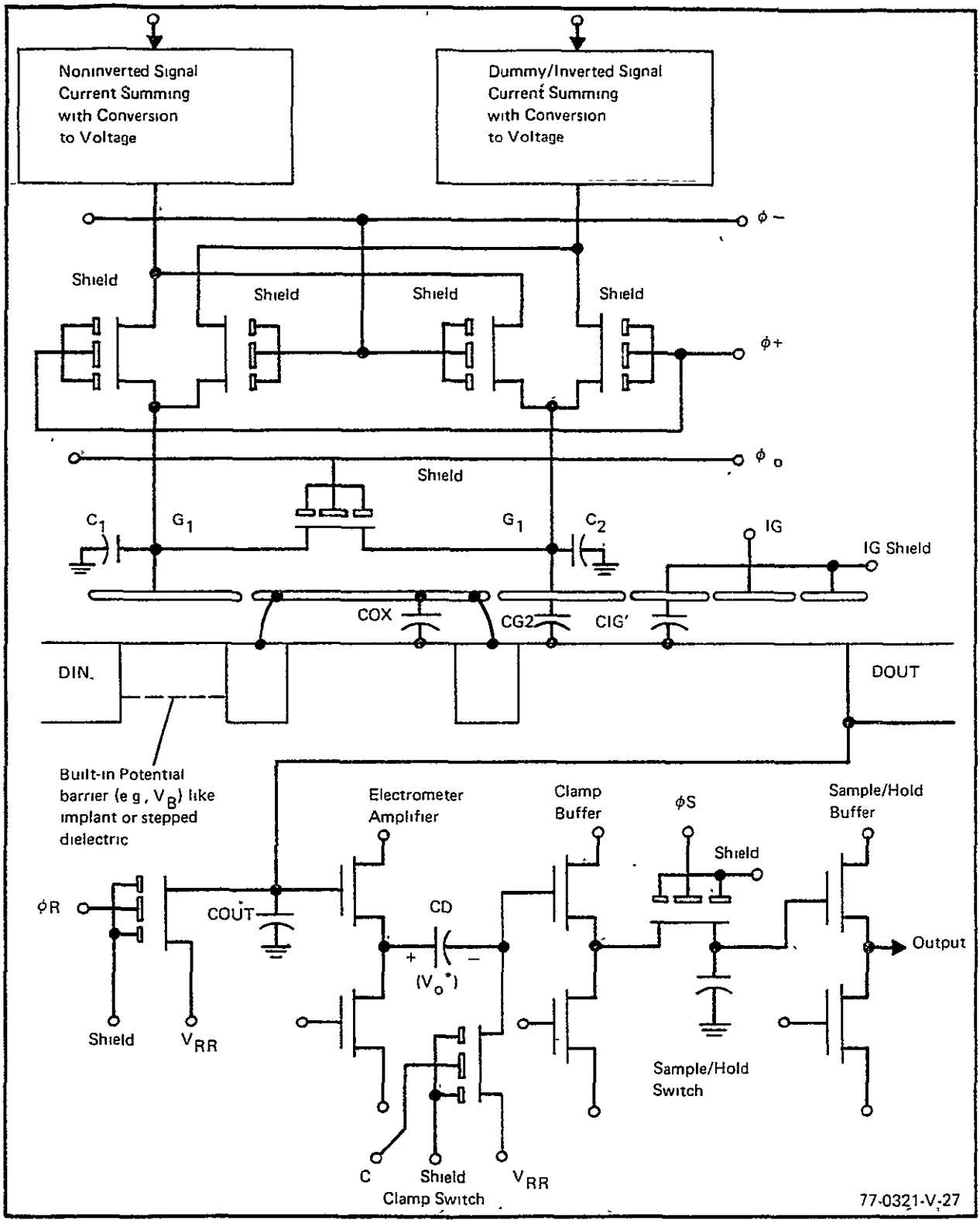


Figure 13 A Monolithic Charge-Coupled Sequential Processor

output capacitor (to give the effect of algebraic addition) before that node is reset to make the next measurement, the overall voltage excursion is limited by the bias applied to the output circuit: V_{RR}= reset reference voltage so that: $N \cdot (V) < V_{RR}$, or $V_{RR} > N \cdot G \cdot V_B$. This formula establishes a limiting relationship between the device gain, built-in barrier, algebraic addition multiplicity, and the reference reset bias voltage.

If the current-summing-to-voltage converters have an effective offset or threshold difference designated by Δ, while the resultant output voltages are indicated by $(K\pm)$, the sequence of charge packets metered on CIN and collected on COUT after the reset operation becomes:

a) Reset the output capacitor, then activate ϕ_o, disable ϕ + and ϕ-, repeat the metering operation four times to give $Q_o = 4Q^*$. The output of the electrometer at that instant (V_o^*) is stored on the "difference" capacitor, CD, by momentarily activating the clamp switch via the ϕC pulse, in the direction indicated in figure 18, which effectively subtracts V_o^* from all subsequent signals output by the electrometer.

b) Reset the output capacitor, then activate ϕ+, disable ϕ-and ϕ_o, to meter $Q_1 = Q^* + CIN\ (\Delta + (A+) - (A-)$, onto COUT.

c) Activate ϕ-, disable ϕ+ and ϕ_o, to add $Q_2 = Q^* + CIN\ (\ (B-) - \Delta - (B+)\ )$, with Q_1 on COUT.

d) Activate $\phi+$, disable $\phi-$ and ϕ_o, to add $Q_3 = Q^* + CIN$ $(\Delta + (C+) - (C-)$, with $(Q_1 + Q_2)$ on COUT.

e) Activate $\phi-$, disable $\phi+$ and ϕ; to add $Q_4 = Q^*$ CIN $(D-) - \Delta -$ $(D+)$, with $(Q_1 + Q_2 + Q_3)$ on COUT.

With all four charge packets added algebraically on the output capacitor:

$$\sum_{1}^{4} Q_K = 4Q^* + CIN \cdot [\delta A - \delta B + \delta C - \delta D], \text{ where } \delta K = (K+) - (K-). \tag{46}$$

But the voltage V_o^*, derived from the electrometer output at a time when $Q_o = 4Q^*$ had been added on its gate, previously stored on CD cancels the contribution from $4Q^*$, leaving only the increment

$$V_{SIG} = \frac{CIN}{COUT} [\delta A - \delta B + \delta C - \delta D],$$

applied to the gate of the clamp buffer. At this instant, the Sample/Hold switch is momentarily activated to update the final output stage. In this manner, a fully reconstructed step-wise output waveform, including dc restoration, is generated. The clamp or dc restoration part of the circuit is optional and may be omitted if ac coupling is permitted.

5.4 A MONOLITHIC READOUT WITH SELF-BIAS AND DIFFERENTIAL CURRENT-TO-VOLTAGE CONVERSION

The actual multiplying elements need a readout scheme which provides DC-balanced virtual ground input nodes, the DC bias of which is controlled by a voltage applied to further node. One conceptual and two simplistic forms of a single-sided or unbalanced version of such a scheme are illustrated in Figure 14. Since most analog multiplying devices consist of counterbalancing elements, yielding currents which

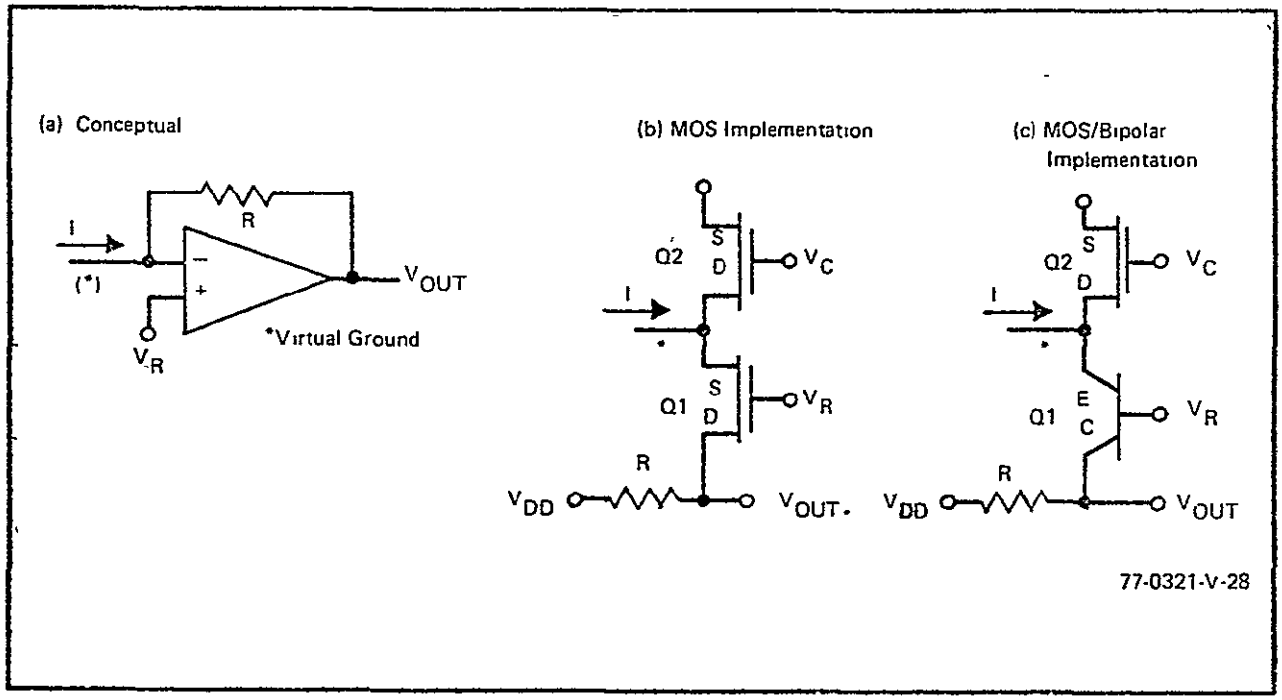


Figure 14 . Current-to-Voltage Converters

must be subtracted, an attractive technique gives the differential current directly from high impedance current sources that can be added in parallel (without interaction) to feed a high resistance for conversion of small differential signal currents into large signal voltages. Use of such a desirable large resistor in the circuits of Figures 14-b and 14-c is severely limited, however, because the full bias current needed to increase the g_m of the virtual-ground stage must flow through that resistor. Consequently, paired circuits, each like that of Figure 14-b mated with the differential monolithic sequential

processor, give smaller differential signal voltages due to the smaller allowed resistor; thereby, yielding a reduced output signal-to noise ratio (S/N) or requiring a larger area output sequential processor to maintain the same S/N achieved with a higher resistance.

A possible CMOS circuit to difference the two currents (cancelling the DC bias components) so as to enable higher resistances to be used is illustrated in Figure 15. The circuit consists partly of a DC balanced pair of virtual-ground stages similar to those of Figure19-b. The remainder is the basic current differencing part of the circuit and closely resembles a modified current-mirror circuit. That is, the currents through transistors (DXCS) and (NOCS), which are nominally matched, try to establish themselves at very near equality

$$I_D + I_P = I_N + \Delta I \qquad (47)$$

where (I_p, I_N) are the signal (IXP, IXN, IY), plus bias currents for the two counterbalancing legs of the multiplier as fed into their respective AC virtual ground nodes, ΔI is a fixed incremental offset current to enable readout of bipolar current differentials, and I_D is the differential readout current. When a complete quadruply balanced triode multiplier cell replaces the test sources, (IXP, IXN, IY), the circuit of Figure 16 results.

In Figure 16 the transistors to the left of the dot-dash line are those belonging to whatever multiplier cell is selected and needs to be duplicated for each such multiplier needed within the correlator chip. The remaining elements form part of the readout mechanism and may be scaled according to the number of multipliers involved, for incorporation as a single common readout stage. Some advantages, however, may be obtained if the part of the readout stage which provides the DC-balanced AC-virtual-ground node-pair, and which is enclosed by a dashed box in Figure 15 is distributed along with each individual multiplier rather than lumped into a common readout stage: The resultant closer proximity of each DC-controlled AC-virtual ground node to its associated counterpart, which includes one of the input signals, may give statistically better matching across each multiplier

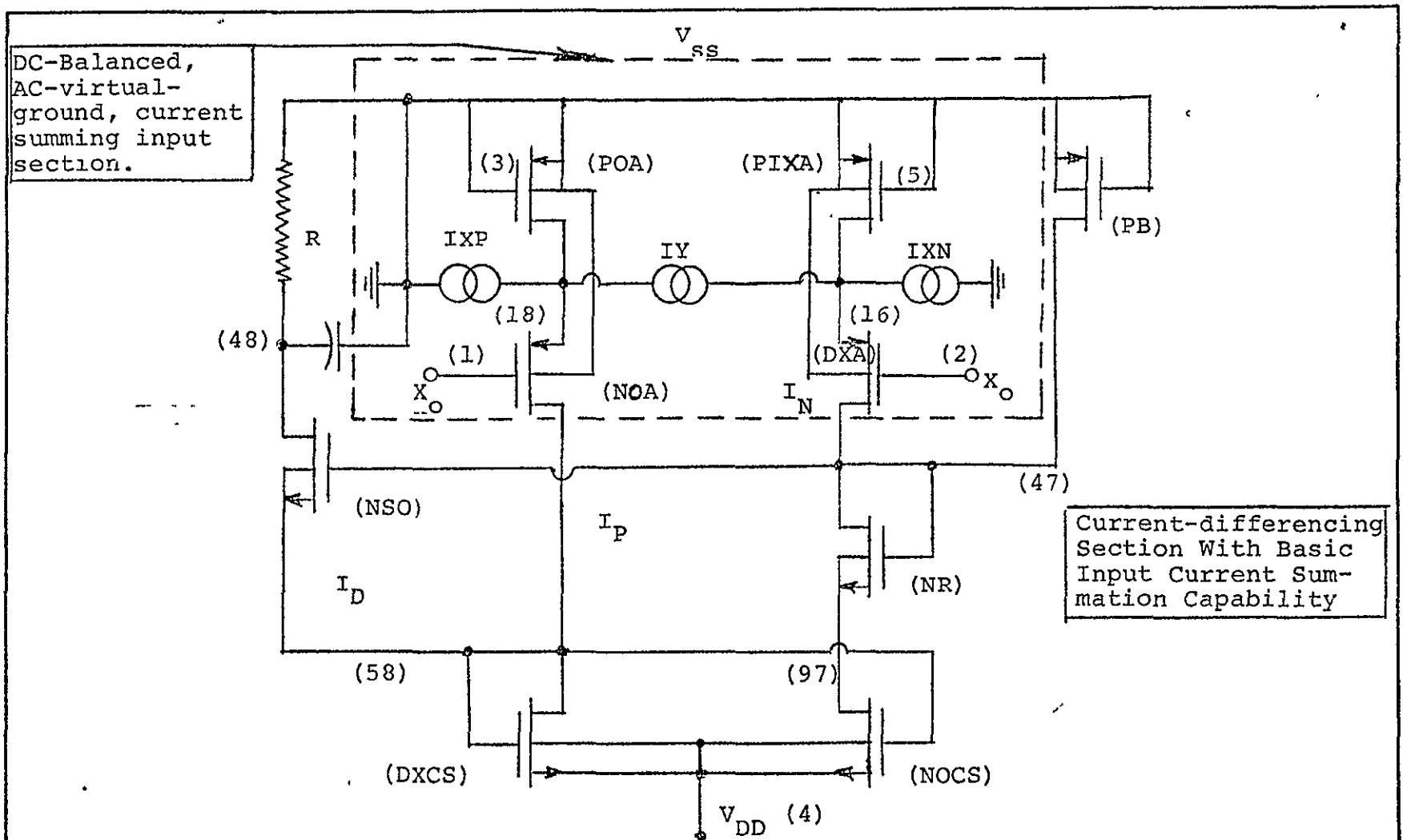


Figure 15 A CMOS CURRENT-DIFFERENCING READOUT WITH INPUT CURRENT SUMMATION AND OPTIONAL DC-BALANCED, AC-VIRTUAL-GROUND INPUTS

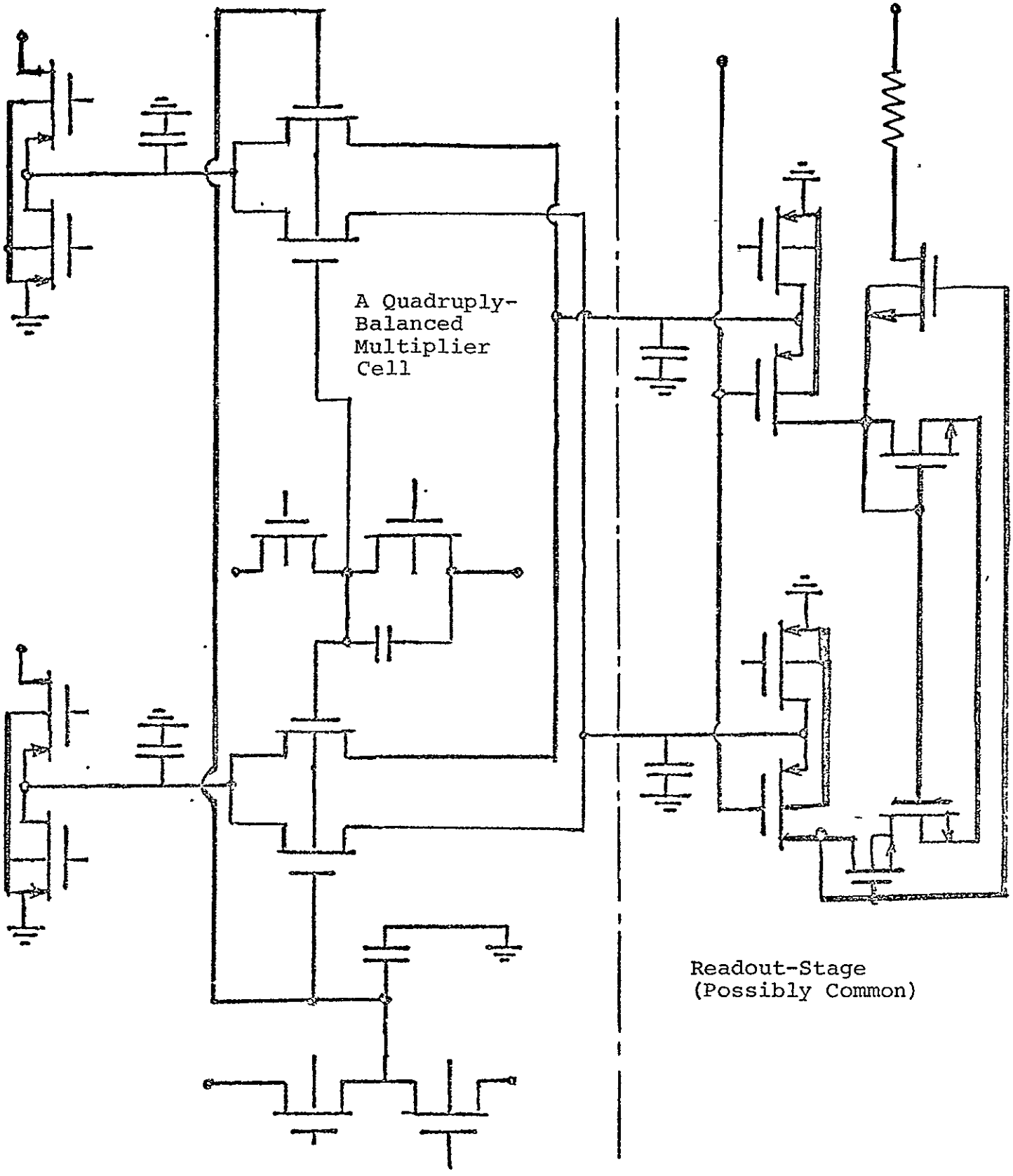


Figure 16 : A CMOS CORRELATOR CELL WITH SELF-BIAS AND DIFFERENTIAL CURRENT-TO-VOLTAGE READOUT

as well as some averaging across the array and a more uniform distribution of heat generation around the chip.

We may now briefly describe the circuit operation, assuming the bias currents for the AC-virtual ground stages are given by (IB±):

$$I_P = (IB+) + (IXP) - (IY)$$
$$I_N = (IB-) + (IXN) + (IY) \qquad (48)$$

Combining the last few equations gives:

$$I_D = (\Delta I) + 2(IY) + \{(IXN)-(IXP)\}+\{(IB-)-(IB+)\} \qquad (49)$$

For MOS triode-type multipliers, (IXP, IXN) are the drain-source currents when a common signal is applied jointly to both drains, so that any AC component of such a common drain signal cancels to the extent that the matched pair of MOSFET triodes are truly identical. The last equation further tells us that the fixed bias current, ΔI, must be comparable to the worst case of unbalance for the virtual-ground stage biases, PLUS the unbalance between the nominally matched multiplier MOSFETS, plus the peak signal excursion. Consequently, one may ascribe a common-mode rejection ratio(CMRR) to this circuit:

$$CMRR = \frac{IX]_{IN}}{IX]_{OUT}} \qquad (50)$$

Indeed, this parameter as well as other measures of performance have been modeled using the commercially available ISPICE routine. The switch from the computer aided design routines like MSINC to ISPICE was made primarily because of the superior convergence of the latter routine; and ISPICE also combined the most attractive features of both MSINC and older SPICE programs for the pertinent class of problems: a) Transistor input specifications are those needed by design/process engineers such as dimensions and doping densities, b) Fourier analysis

of multiple/critical nodes, c) Sensitivity to small threshold non-uniformities, d) Tabulation of transistor operating points for the circuit quiescent point, e) Swept frequency response to give mainly high frequency limitations. The ISPICE program list for the circuit of Figure 15 is shown in Figure 17.

The CSRO (CMOS Selective Read-Out) program list of Fig. 17 illustrates various features of both the ISPICE routine, in general, and the CMOS circuit, in particular. In addition to the five advantages mentioned above, we note that the transistor models may be entered in a parametric form so as to accentuate the quantities which the design engineer can easily change on his mask set (like channel widths and lengths) or on his process sheet (like threshold and body doping.) Thus we can very easily compare performance between a conventional CMOS process (with approximately two volt enhancement thresholds and body dopings of $1x10^{15}cm^{-3}$ and $4x16^{16}cm^{-3}$ for the P and N channel MOSFET's, respectively) and that indicated in Figure 17. The wafer processing indicated in Figure 17 emphasizes low doping densities: The starting N-wafer has a doping of $5x10^{14}cm^{-3}$, which receives a P-Isolation tub implanted and driven to give a density of $5x10^{15}cm^{-3}$, yielding an N-MOST threshold of about one volt enhancement. Another P-implant gives depletion mode P-MOST's with pinch-off voltages near two volts. As we have already seen in the sections on the multipliers and their buffers, depletion mode P-MOST's give better performance with reduced voltage (and power) than enhancement mode transistors. Many of the transistors have five micron source/drain spacings which start on the working plates at about eight microns, thereby making photoengraving-resolution relatively easy.

The bias voltages have been selected to allow the sensitivity routine for parametric fluctuations on voltage sources to simulate threshold nonuniformities across an array. The applied or input signal currents are spectrally separated: ΔIX = 1μamp at 10 KHz and ΔIY = 0.1μamp at 50 KHz, so that $\{(\Delta IX)/(\Delta IY)\}_{IN} = 10$. The spectral separation facilitates pinpointing sources of harmonic distortion as well as reading the respective output signal components for determining the CMRR.

Figure 17- ISPICE Program List for the CMOS Selective Readout (CSRO) Circuit

```
CSRO:     PRINTF CSRO CKT

FILE: CSRO      CKT       FROM: P DISK

RSP 64 4 1
RSN 74 4 1
RN 48 0 100K
R6 6 19 750
R7 7 29 750
R8 8 39 750
C48 48 0 1P
MPIXA 16 5 0 0 MPD(-2.5E14) 7M .5M
MPOA 18 3 0 0 MPD(-2.5E14) 7M .5M
MPB 47 9 0 0 MPD(-2.5E14) .7M .5M
MNOA 58 1 18 0 MPD(-2.5E14) 28M .5M
MDIA  47 2 16 0 MPD(-2.5E14) 28M .5M
MDICS 58 19 64 4 MCN(1.5E15) 3.5M .5M
MNDCS 97 29 74 4 MCN(1.5E15) 3.5M .5M
MNP 47 39 97 97 MCN(1.5E15) 3.5M .5M
MN3D 48 47  58 58 MCN(1.5E15) .8M 1.6M
VREF 11 0 DC -.75
V1 1 11 DC -.75
V2 2 11 DC -.75
V3 3 11 DC .75
V5 5 11 DC .75
V6 58 6 DC .75
V7 58 7 DC .75
V8 47 8 DC .75
V9 9 11 DC .75
VDD 4 0 DC -12
I6 6 19 DC 1M
I7 7 29 DC 1M
I8 8 39 DC 1M
INP 0 18 DC 3U AC 1U
ISNP 0 18 SINE(3U 1U 10MEG 0 0)
INN 0 16 DC 3U AC 0
ISNN 0 16 SINE(3U 1U 10MEG 0 0)
IY 18 16 DC 1U AC 0
ISY 18 16 SINE(1U .1U 50KHZ 0 0)

CSRO:     PRINTF MPD MODEL

FILE: MPD       MODEL     FROM: P DISK

MPD(VTP BDP)
PSCM( VTO=VTP PHI=.58 UO=200 ND=BDP PD=.1 PS=.1 CO=34N C1=7P C2=7P C
CBD=65P CBS=65P PB=.5 KN=1.4E-3 MN=1.91 LL=2.5 ECRIT=30K)

CSRO:     PRINTF MCN MODEL

FILE: MCN       MODEL     FROM: P DISK

MCN(VTN BDN)
NSCM ( VTO=VTN PHI=.77 UO=400 ND=BDN RD=.05 PS= .05 CO=34N C1= 7P C
C2= 7P CBD= 130P CBS= 130P PB=.5 KN=1.4E-3 MN=2.8 LL=2 ECRIT=30K)
```

The quiescent operating point of the circuit is shown in Figure 18 including the operating status for the MOSFET's all of which are well into the pentode region. The power consumption for the circuit is also very easily computed from the data of Figure 18. Figure 19 shows the sensitivity of the output to such parameter changes as device threshold voltages. Let's consider the entries in the table under "voltage sources", except for the row labeled "VDD". The column labeled "1.00% SENS" gives the voltage change in the output node (48) when the named voltage source is changed by 1%, which is 7.5 millivolts in this case. Since (V6) is associated with transistor DXCS; the table indicates a 7.5 mV change in the threshold of DXCS results in a 48 mV change in the output node voltage, which is equivalent to 0.48μa change in current flowing through transistor (NSO). This indication of sensitivity, however, assumes linear variations based on the small signal parameters for the circuit at its quiescent point.

Also included in Figure 19 is a frequency response curve for the "CSRO"(CMOS Selective Readout) circuit showing both the output node (48) labeled "1" and a key internal node (47) on the gate of the "subtracting" transistor (NSO) labeled"2". With the one picofarad loading on the output node, as if connected directly to a monolithic sequential processor, the circuit appears capable of nearly one megahertz operation. The spectral analysis of the output of the circuit, as measured well below its cutoff frequency, is tabulated in Figure 20. The simulated drain currents for a doubly-balanced triode multiplier correspond to the first harmonic, while the fifth harmonic corresponds to the gate signal. The rejection of harmonic distortion of the drain signal (i.e., the square root of the sum of the squares of the second and third harmonics) appears slightly better than 40 dB. The nonlinear interaction between the fundamental and the fifth harmonic (gate signal) is noticeable, but still very small, in the fourth and sixth harmonics. But the most striking feature is the cancellation of the fundamental relative to the fifth harmonic to 1/39 in the output from 10/1 in the input with an overall common mode rejection ratio of

$$CMRR = -20 \log (3.328 \times 10^{-3}) = 49.6dB$$

Figure 18   The Quiescent Operating Point

CSRO: DCOP
*   SINGLE POINT DC   SIMULATION OF CIRCUIT: CSRO   COMPLETED

CSRO: PROBE NV *

**** NODE VOLTAGES

NODE	VOLTAGE
1	-1.500D+00
2	-1.500D+00
3	0.0
4	-1.200D+01
5	0.0
6	-9.104D+00
7	-9.104D+00
8	-5.151D+00
9	0.0
11	-7.500D-01
16	-2.216D+00
18	-2.338D+00
19	-8.354D+00
29	-8.354D+00
39	-4.401D+00
47	-4.401D+00
48	-1.762D+00
58	-8.354D+00
64	-1.200D+01
74	-1.200D+01
97	-8.057D+00

CSRO: PROBE OP M*

**** MOSFETS

NAME	MODEL	VGS	VDS	VBS	ID
MPIXA	MPD	0.0	-2.216	0.0	-1.329D-04
MPOA	MPD	0.0	-2.338	0.0	-1.347D-04
MPB	MPD	0.0	-4.401	0.0	-1.648D-05
MNOA	MPD	0.838	-6.016	2.338	-1.387D-04
MDNA	MPD	0.716	-2.189	2.216	-1.409D-04
MDNCI	MCN	3.646	3.646	-0.000	1.563D-04
MNOCI	MCN	3.646	3.943	-0.000	1.573D-04
MNP	MCN	3.656	3.656	0.0	1.573D-04
MNIO	MCN	3.953	6.592	0.0	1.762D-05

CSRO: PROBE HYPI M*

**** MOSFETS

NAME	MODEL	GM	GDS	CGS	CGD	CGB
MPIXA	MPD	1.030D-04	1.559D-05	1.283D-13	4.900D-14	0.0
MPOA	MPD	1.045D-04	1.533D-05	1.203D-13	4.900D-14	0.0
MPB	MPD	1.247D-05	1.468D-06	1.283D-14	4.900D-15	0.0
MNOA	MPD	3.095D-04	9.727D-06	5.133D-13	1.960D-13	0.0
MDNA	MPD	2.703D-04	1.031D-05	5.133D-13	1.960D-13	0.0
MDNCI	MCN	9.497D-05	3.305D-06	6.417D-14	2.450D-14	0.0
MNOCI	MCN	9.508D-05	3.264D-06	6.417D-14	2.450D-14	0.0
MNP	MCN	9.470D-05	3.400D-06	6.417D-14	2.450D-14	0.0
MNIO	MCN	1.108D-05	1.100D-07	3.461D-14	5.600D-15	0.0

Figure 19 Sensitivity to Threshold Changes and Swept Frequency Response

```
ISPICE 2.04    (13APR77) - 03MAY77 16.14.20

DC   SIMULATION OF CIRCUIT : CIRD

SENSITIVITY OF V(48) = -1.762D+00

**** RESISTORS
```

NAME	VALUE	UNIT SENS	1.00 % SENS	% CHANGE
RCP	1.000D+00	1.689D-03	1.689D-05	-9.596D-04
PSN	1.000D+00	-1.675D-03	-1.675D-05	9.506D-04
RN	1.000D+05	-1.756D-05	-1.756D-02	9.966D-01

```
**** VOLTAGE SOURCES
```

NAME	VALUE	UNIT SENS	1.00 % SENS	% CHANGE
V1	-7.500D-01	8.821D-01	6.616D-03	-3.755D-01
V2	-7.500D-01	-6.832D+00	-5.124D-02	2.902D+00
V3	7.500D-01	6.771D+00	5.078D-02	-2.862D+00
V5	7.500D-01	6.445D+00	4.837D-02	-2.743D+00
V6	7.500D-01	-6.346D+00	-4.759D-02	2.701D+00
V7	7.500D-01	-2.105D-01	-1.579D-03	8.962D-02
V8	7.500D-01	8.595D-01	6.446D-03	-3.659D-01
V9	7.500D-01	8.211D-01	6.158D-03	-3.495D-01
VDD	-1.200D+01	1.113D-01	1.336D-02	-7.522D-01

```
ISPICE 2.04    (13APR77) - 03MAY77 16.16.25

CMOS SELECTIVE READOUT (CIRD-5-5)

LEGEND
X  : FREQ
Y1 : VM(48)
Y2 : VM(47)

             1.000D-05      1.000D-04      1.000D-03      1.000D-02      1.000D-0
        X     :..............:..............:..............:..............:
    1.000D+02 .              .              .              .          21  .
    2.154D+02 .              .              .              .          21  .
    4.642D+02 .              .              .              .          21  .
    1.000D+03 .              .              .              .          21  .
    2.154D+03 .              .              .              .          21  .
    4.642D+03 .              .              .              .          21  .
    1.000D+04 .              .              .              .          21  .
    2.154D+04 .              .              .              .          21  .
    4.642D+04 .              .              .              .          21  .
    1.000D+05 .              .              .              .          21  .
    2.154D+05 .              .              .              .          21  .
    4.642D+05 .              .              .              .          +   .
    1.000D+06 .              .              .              .         +    .
    2.154D+06 .              .              .              .     1  2     .
    4.642D+06 .              .              .             1.    2         .
    1.000D+07 .              .              .   1          2              .
    2.154D+07 .              .      1       .      2       .              .
    4.642D+07 .           1  .         2    .              .              .
    1.000D+08 .  1        2  .              .              .              .
              :..............:..............:..............:..............:
```

Figure 20: Fourier Analysis of Output

ISPICE 2.04 (13APR77) - 03MAY77 16.18.45

FOURIER COMPONENTS OF TRANSIENT RESPONSE: V(48)

DC COMPONENT = -1.762D+00

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000D+04	3.328D-04	1.000000	179.960	0.0
2	2.000D+04	2.533D-06	0.007612	77.435	-102.525
3	3.000D+04	2.014D-06	0.006050	-71.323	-251.283
4	4.000D+04	4.236D-06	0.012729	73.819	-106.141
5	5.000D+04	1.313D-02	39.450323	176.834	-3.125
6	6.000D+04	7.985D-06	0.023991	-83.678	-263.638
7	7.000D+04	2.505D-06	0.007526	-52.291	-232.251
8	8.000D+04	2.666D-06	0.008011	-48.911	-228.871
9	9.000D+04	2.843D-06	0.008543	-45.896	-225.856
10	1.000D+05	2.853D-06	0.008573	32.269	-147.691
11	1.100D+05	3.242D-06	0.009741	-40.927	-220.887
12	1.200D+05	3.455D-06	0.010380	-38.931	-218.891
13	1.300D+05	3.680D-06	0.011060	-37.191	-217.151
14	1.400D+05	3.917D-06	0.011769	-35.684	-215.644
15	1.500D+05	4.150D-06	0.012471	-34.476	-214.436
16	1.600D+05	4.423D-06	0.013291	-33.260	-213.220
17	1.700D+05	4.694D-06	0.014104	-32.304	-212.264

TOTAL HARMONIC DISTORTION = 3945.035 PERCENT

Other absolute signal values may also be of interest. The previous formula for the output of a perfectly subtracting circuit gives $\Delta IY\}_{OUT} = 2\{\Delta IY\}_{IN}$. But Figure 2Ø shows $\Delta IY\}_{OUT} = \Delta VY\}_{OUT} / R_L = 131.3$ nanoamps with an input current of 0.1μa. to give an overall attenuation of the difference signal of about 3.7dB. These results depend on both the applied voltages and how well the nominally paired transistors {(POA/PIXA), (NOA,DXA), (DXCS/NOCS)} are actually matched, as partially illustrated in Table 1.

The greater sensitivity of the output to array nonuniformities (unbalance) in the actual complementary current-differencing section (DXCS/NOCS) of the circuit presented a substantial barrier to lower power operation as follows. As long as one assumes perfect matching for (DXCS/NOCS), this pair of transistors may be made with an extremely large width to length ratio, thereby reducing the associated voltage drop for a given current with a resultant lower power. At the same time, the greatly increased G_M values for (DXCS/NOCS) make the CSRO circuit hypersensitive to threshold unbalances within that transistor pair. Indeed, to give acceptable sensitivity in the output to array threshold unbalances, not only must the size of the (DXCS/NOCS) pair be varied; but the sizes of (NSO) and (NR) must be changed, too.

5-5 A Single-sided Monolithic Sequential Processor

In this section we continue the nomenclature used elsewhere with the "Balanced input" monolithic sequential processor to now describe the simplification of the processor enabled by the "CSRO" current differencing circuit. Whereas, in the "balanced input" monolithic sequential processor, the instantaneous difference between the two balanced halves of the multiplier was generated at the primary input charge metering position; this instantaneous subtraction function is now performed by the CSRO circuit to give $\delta K = (K+) - (K-)$ with the

TABLE 1 CMOS READOUT CIRCUIT SENSITIVITY & PERFORMANCE

RUN NO.	FEATURE	VDD	CMRR (db)	DIFFERENTIAL GAIN (db)	V(48)	EQUIVALENT TRANSCONDUCTIO SENSITIVITY: OUTPUT CURRENT SHIFT/THRESHOL SHIFT)
5-4	Balanced, Higher Voltage	-15	72.9	-3.5	-2.116	N/A
5-5	Balanced	-12	49.6	-3.7	-1.762	N/A
5-6	0.2V Increase In (NOA) Pinch-off	-12	46.1	-3.8	-1.593	8.45μv
5-7	0.2V Increase In (DXA) Pinch-Off	-12	52.3	-3.5	-1.938	8.8μv
5-8	0.2V Increase In (DXCS) Threshold	-12	51.8	-5.7	-0.594	58.4μv

final requirement of the form ($\delta A - \delta B + \delta C - \delta D$). The alternating arithmetic signs were achieved in the "balanced input" monolithic sequential processor by steering the (K+, K-) data alternately to the opposite gates of the charge metering input, thereby requiring the addition of four such charge packets to obtain the needed combination.

The simplified monolithic sequential processor for use with the CSRO circuit, on the other hand, is illustrated in Figure 21 and requires the addition of only two charge packets to give the needed four part combination. The desired operation for the processor of Figure 21 follows: 1) Reset the clamp difference capacitor CD by activating gate C and reset COUT by pulse activating ϕR. Activate gate ϕ_o and repeat the charge metering operation twice so as to store V_o proportional to $2Q^*$ on capacitor CD when gate C is deactivated. (Q^* is the bias charge associated with the built-in potential (V_B) of the input charge meter: $Q^* = V_B \cdot CIN$.) 2) With ϕ_o still activated, store the initial difference value δA on capacitor C1 and gate G1. Also reset COUT by pulse activating ϕR. 3) Deactivate ϕ_o to apply the second difference δB to gate G2 and capacitor C2. Meter a packet of charge, Q1, onto capacitor COUT: $Q1 = Q^* + CIN \cdot (\delta A - \delta B)$. 4) Activate ϕ_o to store the third difference value δC on G1. 5) Deactivate ϕ_o to apply the fourth difference value δD on G2. Meter a packet of charge, Q2, onto capacitor COUT: $Q2 = Q^* + CIN \cdot (\delta C - \delta D)$. This yields a total charge increment stored on COUT specified by:

$$QTotal = 2Q^* + CIN \cdot (\delta A - \delta B + \delta C - \delta D),$$

with an associated voltage appearing at the output of the electrometer amplifier stage. But V_o proportional to $2Q^*$ was previously stored on CD so as to subtract from all subsequent outputs from the electrometer. Thus a signal proportional to

$$QTotal - 2Q^* = CIN \cdot (\delta A - \delta B + \delta C - \delta D) \qquad (51)$$

is sampled and held on the holding capacitor CH by pulse activating ϕS so as to update the analog output data.

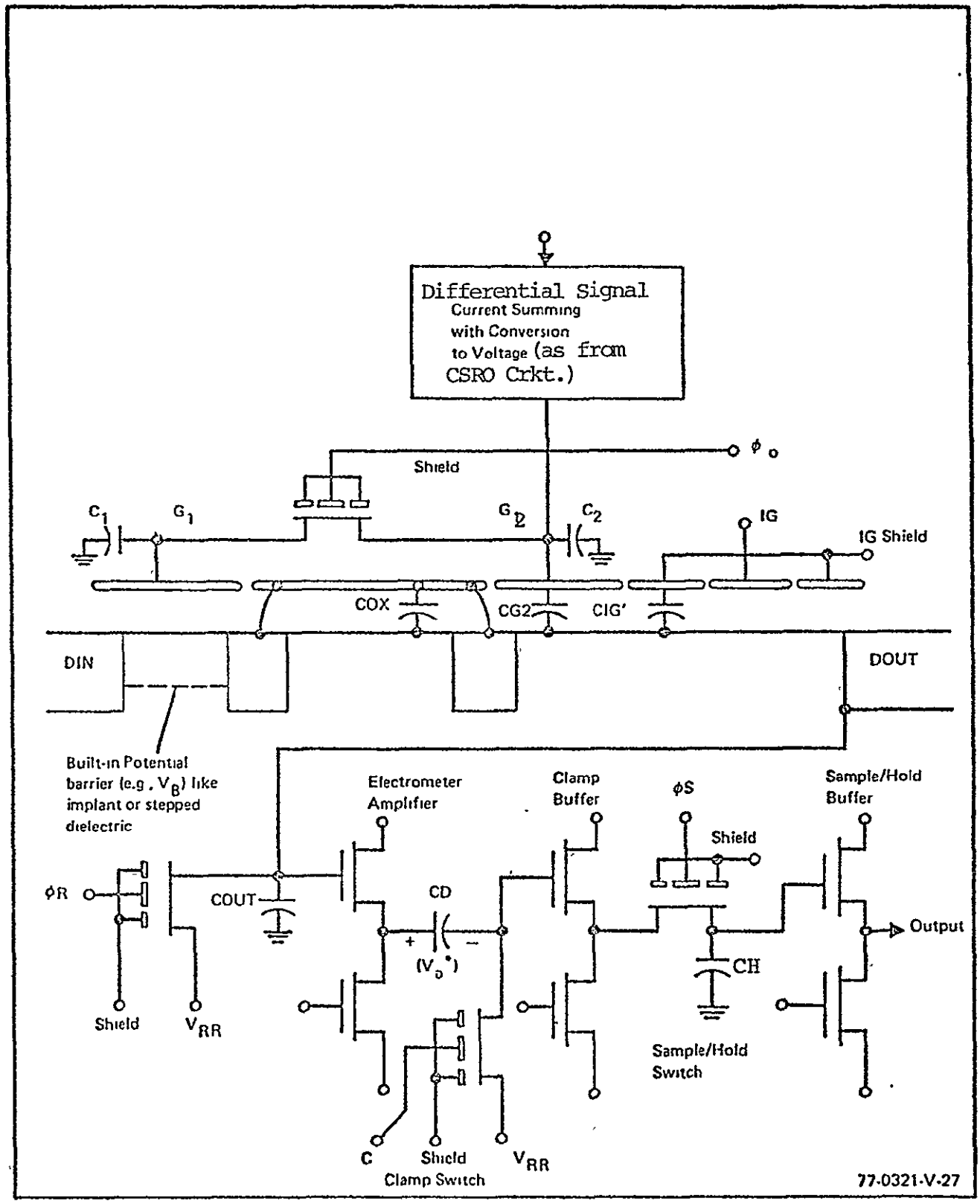


Figure 21 A SINGLE-SIDED (UNBALANCED) MONOLITHIC CHARGE-COUPLED SEQUENTIAL PROCESSOR

6.0 COMPUTER MODELING

Various computer-aided-design (CAD) routines have been employed to analyze many circuit possibilities. The most used routine is M-SINC (Modular Simulator for Integrated Nonlinear Cricuits), a nonlinear dc and transient simulator of MOS transistor circuits developed by T. K. Young and R. W. Dutton of the Electrical Engineering Dept. at the Standford University. The M-SINC program features a second order MOS transistor model which includes specification of a field dependent mobility as well as three choices for the dominant mode of channel depletion. In addition to the transient analysis of integrated circuits driven by repetitive pulses M-SINC performs Fourier analysis of waveforms at selected nodes as follows: For up to 200 points, it predicts the output of the prescribed circuit resulting from specified input signals and driving sources. A discrete Fourier transform is applied to the time-domain sequence of computed output values to give both the phase and amplitude in the frequency domain. Purely sinusoidal input signals thus produce well defined output spectra with the undesired spectral components providing a measure of the error or distortion from the desired function Such a spectral analysis technique for both computer and experimental modeling greatly facilitates pin pointing the dominant sources of errors as already described in sections four and five. Earlier "SPICE" CAD routines provide complementary data not readily available from M-SINC, such as swept frequency response and sensitivity to elementary parameters.

Consequently, we present the results of two typical complementary models: one by M-SINC on a MOS circuit having all transistors of the same type ("Singular MOS") as illustrated in Figure 22, and a second one by SPICE for a CMOS version of the "singular MOS" circuit. Figure 22 includes only the identifiable circuit elements of a monolithic configuration and specifically excludes the differential current-to-voltage circuit of section 5.4 as well as fictitious circuit elements (like one ohm resistors) used to facilitate study of the circuits. In describing the following models, we point out the significant information from each CAD routine. The salient features of the quadruply-balanced triode circuit of Figure 22 will be detailed later in this section.

6.1 M-SINC Models a "Singular MOS" Triode Multiplier

The M-SINC program list for the circuit of Figure 22 is given in Figure 23 with that model given the label "MCISM-7-1". The constituent subcircuits are labeled by function as well as the input signal drives. The gate buffers are reasonably simulated with both, 0.2 volt offset and a 20% gain differential. Since this particular computer run is an interim step in tracing the nature and source of errors, the triode multiplier source/drain buffer situation is the following. A 0.2 volt offset is applied to the source virtual-ground buffer; but both drain buffers were not yet changed from their per= fectly identical situation, thereby leading to a better than normally anticipated rejection of gate input feedthrough. Notice that large goemetries are used in the inverters and multiplying FET's to help give better dimensional uniformity within an array. The resulting quiescent operating point of the circuit is shown in Figure 24 where

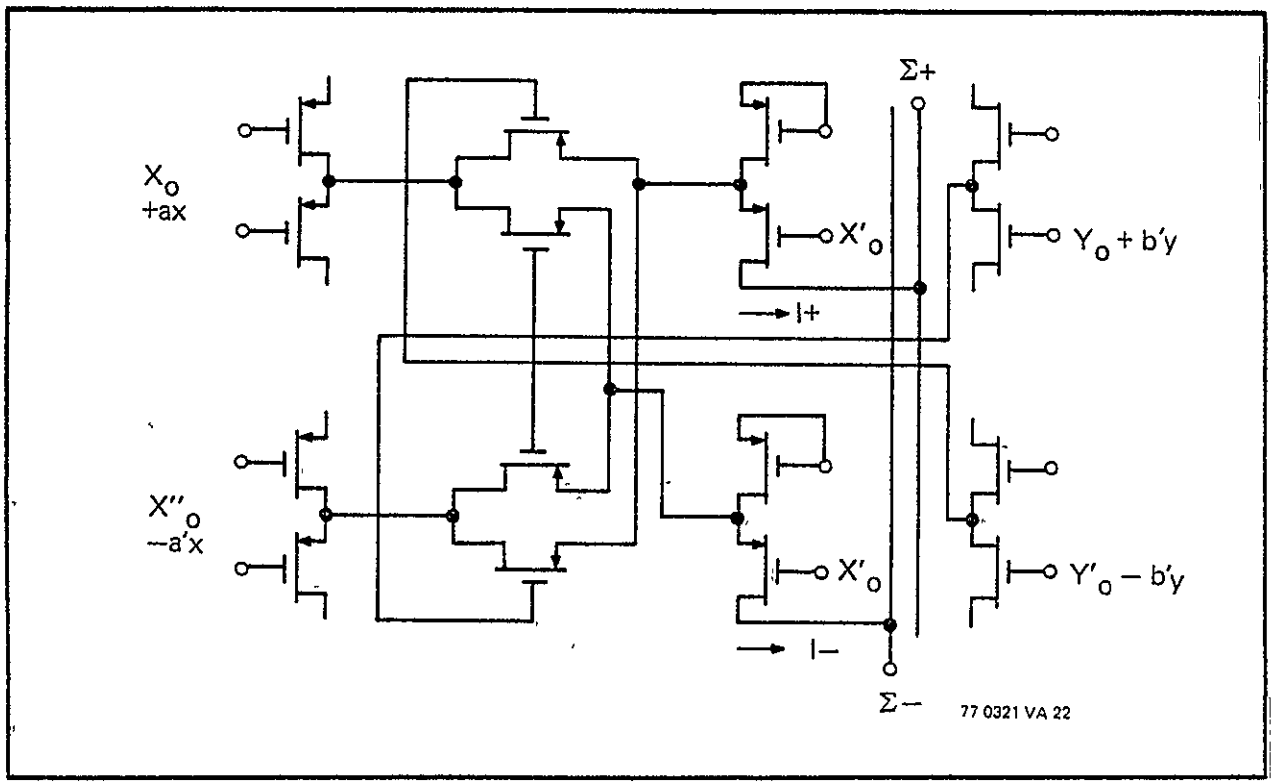


Figure 22 Quadruply-Balanced Triode Multiplier

Figure 23 MSINC Program List for a "Singular MOS" Triode Multiplier (MCISM-7-1)

```
- M S I N C - - VER. A2     DATE  03/22/77      CLOCK  12:22:19

MOS CORRELATOR WITH INTEGRATED SEQUENTIAL MULTIPLIER (MCISM-7-1)

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

TIME .1U 20U
R? 18 4 20K
R? 48 4 20K
RD 36 4 20K
RG 86 4 20K
C3 3 0 .5F
C15 16 0 2P
C76 76 0 1P
C16 16 0 1P
C47 47 0 1F
C48 48 0 5P
C17 17 0 1P
C18 18 0 5P
C10 10 0 .5F
Q45 BF1 47 47 0 0 20M .7M 500 500 2P 2P  )= source-follower source buffer (virtual ground)
Q47 BF1 48 7 47 0 20M .7M 500 500 2F 2P  )
Q74 BF1 76 76 0 0 20M .7M 500 500 2P 2P  )= source-follower drain buffer
Q76 BF1 86 86 76 0 20M .7M 500 500 2P 2P )
Q1 BF1 3 2 3 0 2M 2M 500 500 .2P .2P     )=  Inverter gate buffer
Q2 BF1 4 4 3 0 2M 2M 500 500 .2F .2F     )
Q4 BF1 16 3 47 0 2M 2M 500 500 .2P .2P   )
Q5 BF1 16 10 17 0 2M 2M 500 500 .2P .2P  )= Multiplying Triodes
Q64 BF1 76 10 47 0 2M 2M 500 500 .2F .2P )
Q65 BF1 76 3 17 0 2M 2M 500 500 .2P .2P  )
Q3 BF1 10 37 0 0 2M 2M 500 500 .2F .2F   )=  Inverter gate buffer
Q8 BF1 4 4 10 0 2M 2M 500 500 .2F .2F    )
Q14 BF1 16 16 0 0 20M .7M 500 500 2P 2P  )
Q15 BF1 17 17 0 0 20M .7M 500 500 2F 2P  )= Follower drain/source  buffer pair,
Q16 BF1 36 6 16 0 20M .7M 500 500 2F 2P  )
Q17 BF1 18 7 17 0 20M .7M 500 500 2F 2F  )
BF1 PMO VTO=-2 UB=250,6E4,.15 COX=23N DNB=1E15 XJD=.3M GDS=2 CSS=.5P
BF2 PMO VTO=-2.25 UB=250,6E4,.15 COX=23N DNB=1E15 XJD=.3M GDS=2 CSS=.5P
V4 4 0 -20
V7 7 0 -7.2
VSIN 6 0 125MV 60KHZ 0 -7         )= Drive for quadruply balanced operation with gate
VSIN 66 0 125MV 60KHZ 180 -7      )  unbalance of 0.2 volt and both source-drain offsets
VSIN 2 0 250MV 300KHZ 0 -6.8      )  of 0.2 volt.
VSIN 37 0 300MV 300KHZ 180 -7     )
PLOT VOUT 48 18
PLOT VX 48 0
PLOT VD 16 0
PLOT VSF 47 0
PLOT VG 3 0
PLOT VGC 10 0
FOR 3U 19.6667U 17
END
```

ORIGINAL PAGE IS OF POOR QUALITY

Figure 24 The Quiescent Operating Point for MCISM-7-1

```
MCS CORRELATOR WITH INTEGRATED SEQUENTIAL MULTIPLIER (MCISM-7-1)

TEMP =   300.00

NO. OF ITER. =  13

NODE VOLTAGES --
 ( 0)      .0000     ( 2)    -6.8000     ( 3)   -11.0000     ( 4)   -20.0000
 ( 6)    -7.0000     ( 7)    -7.2000     (10)   -10.8090     (16)    -3.1235
 (17)    -3.2024     (18)   -17.9208     (36)   -18.3096     (37)    -7.0000
 (47)    -3.2024     (48)   -17.9208     (66)    -7.0000     (76)    -3.1235
 (86)   -18.3096

TRANSISTOR OP. PT. --
NAME  TP      VGS          VDS          VSB          IDS(MA)
345   P      -3.2024      -3.2024       .0000       -.1007
347   P      -3.9976     -14.7184     -3.2024       -.1040
374   P      -3.1235      -3.1235       .0000       -.0278
376   P      -3.8765     -15.1861     -3.1235       -.0345
[illegible]  -6.0000     -11.0060       .0000       -.0543
[illegible]  -8.9940      -8.9940    -11.0060       -.0543
[illegible]  -7.8036        .0789     -3.2024        .0017
665   P      -7.6066        .0789     -3.2024        .0016
664   P      -7.6066        .0789     -3.2024        .0016
665   P      -7.8036        .0789     -3.2024        .0017
[illegible]  -7.0000     -10.8090       .0000       -.0589
[illegible]  -9.1910      -9.1910    -10.8090       -.0589
914   P      -3.1235      -3.1235       .0000       -.0278
915   P      -3.2024      -3.2024       .0000       -.1007
916   P      -3.8765     -15.1861     -3.1235       -.0845
917   P      -3.9976     -14.7184     -3.2024       -.1040

RESISTOR CURRENTS --
NAME     CURRENT (MA)        POWER (MW)
[illegible]  .103953481          .21614731
RB       .103953481          .21614731
RD       .084517745          .14286499
RG       .084517745          .14286498
```

we see that all the transistors except the triode multiplying FET's are clearly in the pentode region.

Figure 25 illustrates the usefulness of the spectral analysis part of the CAD routine. Starting with the gate buffers, we see the primary gate signal falls at the fifth harmonic of the drain signal with its harmonics falling at the tenth, fifteenth, etc. multiples of the drain signal. The ratio five exhibits both the primary and secondary drain signal harmonics as well as their inter-modulation with the gate signal and its harmonics, while allowing a relatively inactive harmonic between each grouping of active ones. From the gate buffer spectral analyses we see rejection of harmonic distortion by the values of 53 to 58 dB and a slightly less than unity gain. Indeed the inverting buffer with output node (3) and the smaller input bias yields the better harmonic rejection, but also slightly less gain.

The spectral analysis of the source follower buffers is also given in Figure 25. The loading of the triode multiplier on the drain buffer reduces buffer gain to -7.4 dB, much worse than the unity gain inverter. The nature of the virtual-ground source buffer, i.e. pentode operation with current proportional to (gate voltage)^2, squared, is very apparent: A fifth harmonic component current flows through the virtual-ground node due to a fifth harmonic voltage on the gate of the triode multiplier. The finite, nonlinear relationship between the virtual-ground node (47) voltage and the current it sinks causes the second harmonic of the gate signal to fall on the tenth order harmonic and to be as large as - 27.5 dB from the relevant fundamental. (The large second harmonic voltage contribution derives from the imposition of a "fairly clean" sinusoidal current while

Figure 25 MCISM-7-1 Spectral Analysis

FOURIERANALYSIS of the differential output (48, 18)

ORDER	HARM	DSINE	CODSINE	MAGNITUDE	REL MAG	PHASE
0		.0000	-.1696-06	.1696-06	.0203	180.0000
1		.3906-03	.7370-03	.8342-03	100.0000	-27.9234
2		-.5784-06	-.3629-06	.6828-06	.0819	-122.1039
3		-.3812-06	-.9226-06	.9987-06	.1087	155.1362
4		.9399-03	-.4036-03	.1023-02	122.6247	-113.2414
5		-.6238-06	-.7735-07	.6286-06	.0754	97.0681 -42.5dB
6		.2107-03	-.8980-03	.9224-03	110.5830	-166.7929
7		.1921-06	-.2107-06	.2851-06	.0342	-137.6403 ←Subtraction
8		-.6522-06	-.1410-05	.1553-05	.1862	156.1759
9		-.5502-06	-.1314-05	.1427-05	.1711	157.0681
10		-.3103-06	-.7747-06	.8376-06	.1004	157.6608
11		-.6936-06	-.7422-06	.1016-05	.1218	136.9393
12		-.1151-05	-.7081-06	.7174-06	.0860	170.7714
13		-.1066-06	-.8538-06	.8605-06	.1032	172.8804
14		-.3617-08	-.7670-06	.7670-06	.0919	179.7298
15		-.9188-07	-.8131-06	.8183-06	.0981	173.5532
16		.1685-07	-.8478-06	.8480-06	.1017	-178.8612
17		-.3667-07	-.8079-06	.8087-06	.0969	177.4010

FOURIERANALYSIS of the single - sided output (48)

ORDER	HARM	DSINE	CODSINE	MAGNITUDE	REL MAG.	PHASE
0		.0000	-.1792+02	.1792+02**********		180.0000
1		.2135-03	.3530-03	.4126-03	100.0000	-31.1691
2		-.1758-05	-.8321-05	.8505-05	2.0618	168.0691
3		.3237-06	-.4377-05	.4389-05	1.0639	-175.7709
4		.4702-03	-.2059-03	.5133-03	124.4359	-113.6458
5		-.3993-04	.1086-03	.1110-03	26.9136	21.0906
6		.1058-03	-.4530-03	.4652-03	112.7824	-166.8507
7		.6220-06	-.4315-05	.4359-05	1.0568	-171.7971
8		.2814-06	-.4687-05	.4695-05	1.1381	-176.5636
9		.4345-06	-.4621-05	.4642-05	1.1253	-174.6287
10		.3773-05	-.4187-05	.5636-05	1.3663	-137.9773
11		.5087-06	-.4320-05	.4349-05	1.0544	-173.2838
12		.8662-06	-.4278-05	.4366-05	1.0584	-168.5563
13		.8323-06	-.4352-05	.4450-05	1.0800	-167.6500
14		.1003-05	-.4293-05	.4428-05	1.0733	-165.8426
15		.1112-05	-.4305-05	.4446-05	1.0778	-165.5170
16		.1244-05	-.4303-05	.4460-05	1.0859	-163.8803
17		.1290-05	-.4263-05	.4454-05	1.0798	-163.1607

Figure 25 MCISM-7-1   Spectral Analysis (continued)

FOURIERANALYSIS of *gate* buffer output (3)

ORDER HARM	DSINE	COSINE	MAGNITUDE	REL MAG	PHASE
0	.0000	-.1101+02	.1101+02	**********	180.0000
1	-.2450-04	.4377-05	.2489-04	100.0000	79.9711
2	.7074-07	.6476-04	.6476-04	260.2202	-.0626
3	-.1657-03	.9625-05	.1659-03	666.7325	86.6748
4	.1040-03	.4693-04	.1141-03	458.4861	-65.7128
5	-.1763+00	.1449+00	.2281+00	916676.6845	50.5842
6	.3122-04	-.3063-04	.4373-04	175.8926	-134.4036
7	.2150-04	.2123-03	.2133-03	857.1869	-5.7842
8	[illegible]	.6047-04	.6324-04	279.2027	8.5429
9	.3880-04	.9330-04	.1010-03	405.9896	-22.5795
10	-.1501-03	-.2403-03	.2865-03	1151.3031	146.9336
11	.2397-04	.0979-04	.7313-04	293.8166	-19.1344
12	.1183-04	.8394-04	.8477-04	340.6152	-8.0225
13	.1189-04	.6802-04	.6904-04	277.4041	-9.8706
14	.1782-04	.7942-04	.8139-04	327.0273	-12.6499
15	.6338-05	.8272-04	.8297-04	333.3587	-4.3799
16	.1716-04	.7595-04	.7777-04	312.4699	-12.7464
17	.9559-05	.8240-04	.8295-04	333.3094	-6.6168

-0.80dB gain

-58.0dB second Harmonic

FOURIERANALYSIS of the other gate buffer output (10)

ORDER HARM	DSINE	COSINE	MAGNITUDE	REL MAG	PHASE
0	.0000	-.1031+02	.1081-02	**********	180.0000
1	.2374-04	-.1218-04	.3214-04	100.0000	-112.2670
2	.1177-05	-.8641-04	.8642-04	268.9316	-179.2198
3	.1997-03	-.1990-04	.2006-03	624.0403	-95.2633
4	-.1243-03	-.6380-04	.1398-03	434.9091	117.1881
5	.2124+00	-.1737+00	.2744+00	853943.6944	-123.2611
6	[illegible]	.2333-04	.4673-04	145.4276	51.1252
7	[illegible]	-.2623-03	.2640-03	821.4436	174.5477
8	[illegible]	-.9126-04	.9316-04	289.8868	-170.8003
9	-.4575-04	-.1179-03	.1265-03	393.5664	158.7941
10	-.1800-03	-.5259-03	.5658-03	1760.7857	161.4523
11	-.2020-04	-.9955-04	.9331-04	290.3759	163.6776
12	-.1475-04	-.1095-03	.1095-03	340.7023	172.2597
13	-.1249-04	-.9922-04	.9309-04	289.3236	172.0316
14	[illegible]	-.1024-03	.1043-03	324.5798	168.9416
15	-.5541-05	-.1106-03	.1106-03	344.3228	177.1297
16	-.1844-04	-.9824-04	.9996-04	311.0497	169.3700
17	-.9195-05	-.1063-03	.1067-03	332.0709	175.0568

-0.77dB gain

-53.7dB Second Harmonic

Figure 25 MCISM-7-1 Spectral Analysis (continued)

FOURIERANALYSIS of drain buffer output (16)

ORDER HARM	DSINE	CODSINE	MAGNITUDE	REL MAG	PHASE
0	.0000	-.3124+01	.3124+01	5865.3513	180.0000
1	.2235-01	.4311-01	.5326-01	100.0000	-25.4070
2	-.1275-03	-.1115-03	.1694-03	.3181	131.1784
3	-.2269-05	-.6515-06	.2361-05	.0044	106.0211
4	.1295-04	-.2571-05	.1320-04	.0248	-101.2310
5	.3695-04	-.1449-04	.3970-04	.0745	-111.4104
6	.5025-05	-.1112-04	.1255-04	.0236	-152.3473
7	.2430-05	-.3296-06	.4099-06	.0008	-143.5319
8	.3662-06	.9855-07	.3793-06	.0007	-74.9151
9	-.2353-06	-.4290-06	.4393-06	.0009	151.2514
10	-.3778-06	-.9430-06	.1016-05	.0019	158.1655
11	-.3959-06	.1236-06	.4147-06	.0009	72.6658
12	.1868-06	.3354-07	.1898-06	.0004	-79.8194
13	.2057-06	.1391-06	.2483-06	.0005	-55.9295
14	.1380-06	.8256-07	.1609-06	.0003	-59.1095
15	.2069-06	.1197-06	.2391-06	.0004	-59.3476
16	.1221-06	.1519-06	.1947-06	.0004	-38.8109
17	.1675-06	.1268-06	.2101-06	.0004	-52.8788

-7.4dB gain
-49.9dB second Harmonic

FOURIERANALYSIS of source buffer virtual ground (47)

ORDER HARM	DSINE	CODSINE	MAGNITUDE	REL MAG	PHASE
0	.0000	-.3202+01	.3202+01	**********	180.0000
1	.4290-04	.7823-04	.8922-04	100.0000	-28.7382
2	-.3242-05	-.1581-05	.1712-05	1.9191	169.0962
3	.5758-07	-.7908-06	.7928-06	.8886	-175.8369
4	.1129-03	-.3047-04	.1169-03	130.9976	-105.1092
5	-.1363-04	.2254-04	.2634-04	29.5274	31.1669
6	.4602-04	-.1026-03	.1124-03	125.9935	-155.8348
7	.1167-06	-.7738-06	.7826-06	.8771	-171.4213
8	.4762-07	-.8781-06	.8793-06	.9856	-176.8958
9	.6794-07	-.8758-06	.8784-06	.9845	-175.5643
10	.9530-06	-.5643-06	.1108-05	1.2414	-120.6321
11	.5260-07	-.7928-06	.8005-06	.8972	-176.2269
12	.1503-06	-.7786-06	.7930-06	.8888	-169.0757
13	.1665-06	-.7941-06	.8113-06	.9094	-168.1753
14	.1913-06	-.7801-06	.8032-06	.9002	-166.2228
15	.1935-06	-.7847-06	.8082-06	.9058	-166.1481
16	.2195-06	-.7845-06	.8146-06	.9130	-164.3683
17	.2250-06	-.7761-06	.8080-06	.9056	-163.8349

-27.5dB second Harmonic

RMS = 1.85mv

ORIGINAL PAGE IS OF POOR QUALITY

spectrally analyzing the resultant source voltage.) On the other hand, with the source follower drain buffer, a sinusoidal voltage is applied to the gate while spectrally analyzing the source voltage to find a 49.9 dB rejection of the second harmonic in that case.

Finally we examine the spectral analysis of the output: both the differential output and a single side of it. The cancellation of the gate signal component between the two sides results in that component subtracting in the differential output to a value 42.5 dB below its value in one side of the balanced output, as also indicated in Figure 25. We must now use this part of the information for mating with the differential current to voltage stage described in the previous section. Examination of Table 1 shows the "CSRO" circuit readily provides subtraction cancellation exceeding 42.5 dB, thereby confirming the functional compatability between the (MCISM-7-1) and (CSRO-5-5) circuit. But use of the CMOS readout circuit suggests simultaneous use of a CMOS multiplier cell (like that described below) to take full advantage of the fabrication technology.

6.2 SPICE Models A CMOS Triode Multiplier

A CMOS version of the multiplier of Figure 22 is given in the SPICE CAD program list of Figure 26. As in Figure 23, we point out some of the key constituent subcircuits, which are consistent with the earlier self-bias scheme suggestion to use complementary source followers as gate buffers and depletion-mode PMOS source followers as drain buffers and source virtual-grounds. As indicated, a D in the name of a transistor shows that it is used in "dummy" or "current-mirror" type subcircuits with only one such set of transistors per integrated chip in order to establish the various load device gate

Figure 26 SPICE Program List for CMOS Triode Multiplier (LCTBR-1)

```
**********************************************************************

LOW POWER CMOS CORRELATOR WITH SELF BALANCING & READOUT (LCTBR-1)

                    DATE  040577          CLOCK  105510          VERSION
**********************************************************************

RN 4C 4B 1E6
RF 4D 1B 1E6
RND 4D 8E 1E6
RFD 4D 3E 1E6
R1 1E 5I 1
R2 16 92 1
R3 76 93 1
R4 76 94 1
C36 36 0 1F
C86 86 0 1F
C53 53 0 10P
C57 57 0 10F
C58 58 0 10P
C18 18 0 5F
C48 48 0 5F
C17 17 0 1F
C47 47 0 1F
C16 16 0 1F
C76 76 0 1F
C3 3 0 1F
C10 10 0 1F
MM1 91 3 47 0 MFMD
MM2 92 1C 17 0 MFMD
MM3 93 10 47 0 MFMD
MM4 94 3 17 0 MFMD
MFIYL 3 53 4 4 MN1
MNIYL 10 53 4 4 MN1
MDYL 53 53 4 4 MN1
MFIYA 7 2 3 4 MN1
MNIYA 7 37 10 4 MN1
MDYA 7 1 53 4 MN1
MFIXL 16 0 0 0 MFD1 2S
MNIXL 76 C 0 0 MFD1 2S
MNOL 47 0 0 0 MFD1 2S
MFOL 17 C 0 0 MFD1 2S
MDXL 57 0 C 0 MFD1 2S
MFIXA 36 -E 1S C MFD1 2S
MNIXA 86 66 76 0 MFD1 2S
MNOA 48 1 47 0 MFD1 2S
MFOA 18 1 17 0 MFD1 2S
MDXA 58 1 57 0 MFD1 2S
MFIXCS 36 58 4 4 MN1 2S
MNIXCS 86 58 4 4 MN1 2S
MNOCS 48 59 4 4 MN1 2S
MFOCS 18 58 4 4 MN1 2S
MDXCS 58 58 4 4 MN1 2S
.MODEL MFD1 FMC VTC=-2 PHI=.58 BETA=3E-6 GAMMA=.2 LAMBDA=1E-2 RD=5CC
+RS=50D CGS=7E-15 CGD=7E-15 CGB=2E-14 CBD=.1P CBS=.1P PB=.5 IS=1E-14
.MODEL MFMD FMC VTC=-2 PHI=.58 BETA=2E-6 GAMMA=.2 LAMBDA=1E-2 RD=5CC
+RS=50D CGS=1.4E-14 CGD=1.4E-14 CGB=.1P CBD=.1P CBS=.1P PB=.5 IS=1E-14
.MODEL MFD2 FMC VTC=-2.25 PHI=.58 BETA=3E-6 GAMMA=.2 LAMBDA=1E-2 RD=5CC
+RS=50D CGS=7E-15 CGD=7E-15 CGB=2E-14 CBD=.1P CBS=.1P PB=.5 IS=1E-14
.MODEL MN1 NMC VTC=1 PHI=.77 BETA=6E-6 GAMMA=1.6 LAMBDA=5E-3 RD=3CC
+RS=30D CGS=7E-15 CGD=7E-15 CGB=2E-14 CBD=.2P CBS=.2P PB=.5 IS=1E-14
.MODEL MN2 NMC VTC=1.25 PHI=.77 BETA=6E-6 GAMMA=1.6 LAMBDA=5E-3 RD=3CC
+RS=30D CGS=7E-15 CGD=7E-15 CGB=2E-14 CBD=.2P CBS=.2P PB=.5 IS=1E-14
.MODEL MFE1 FMC VTC=1.5 PHI=.58 BETA=3E-6 GAMMA=.2 LAMBDA=1E-2
+RD=50D RS=50D CGS=7E-15 CGD=7E-15 CGB=2E-14 CBD=.1P CBS=.1P PB=.5 IS=1E-14
VR 1S C DC -3 AC 100M
VYP 2 19 DC 0 SIN 0 100M 400X47 0
VYA 37 0 DC -3 SIN -3 -10CM 4CCKHZ 0
VXP 6 19 DC 0 SIN 0 100M 100KHZ 0
VXA 66 0 DC -3 SIN -3 -10CM 1CCKHZ 0
V1 1 0 -3
VCC 7 C DC -3
VDD 4 0 DC -10
VGG 40 0 DC -15
.OUTPUT VOUTD 18 48 PLOT DC MA TR
.OUTPUT VOUTP 18 0 PLOT DC MA TR
.OUTPUT VD 16 0 PLOT DC MA TR
.OUTPUT VG 3 0 PLOT DC MA TR
.OUTPUT VSP 17 0 PLOT DC MA TR
.OUTPUT VFXCS 3E C PLOT DC TR
.OUTPUT VM1 16 91 PLOT DC TR
.OUTPUT VM2 16 92 PLOT DC TR
.OUTPUT VM3 76 93 PLOT DC TR
.OUTPUT VM4 76 94 PLOT DC TR
.DC OF VOUTD VR TC VR 2 -8 .1
.AC DEC 3 10HZ 1E8HZ
.TRAN .1US 10US FOUR VOUTD 100KHZ
.END
```

D designates "dummy" circuits, only one per chip to set follower load device gate biases much like "current mirror" function)

= Depletion PMOST multipliers.

= Complementary source-follower gate buffers.

= Drain buffers and source virtual-ground buffers.

biases. The resultant circuit node quiescent voltages are tabulated in Figure 27 with the associated transistor quiescent values given in Figure 28, we notice all transistors excluding the multiplying triodes are in the pentode operating region except the last five NMOSTs , which represent an early attempt at the differential readout circuit which ultimately developed into "CSRO." A completely balanced model (LCTBR-1) is presented since the early readout scheme was very sensitive to array threshold nonuniformities.

The available SPICE CAD routine provided the swept frequency response curves given in Figure 29. Thus, we may now correlate the subcircuit upper frequency limits with other criteria like power consumption and device geometry. First, we notice that the complementary - follower gate buffer appears usable to signal frequencies near 2 MHz, while it draws only 17.5μa from a 7 volt power supply for a total of 123 μW. with a transconductance of about 20 micromhos (consistent with the requirement predicted in section 4.2). Note that, together, the two types of buffers provide a DC bias for the multipler of 4.5 volts to give $(V_{GS} - V_T) = 6.5$ volts in LCTBR-1 and 7.7 volts to give $(V_{GS} - V_T) = 5.7$ volts in MCISM-7-1. The acceptable harmonic error rejection values indicated in Figures 25 and 30 show two important points. (1) Harmonic distortion by the buffers is acceptably low for all three types: PMOS drain-buffer source followers, PMOS gate buffer inverter, and NMOS (complementary) gate buffer follower. (2) The self bias provided by the complementary scheme gives multiplier DC bias adequate for good linear triode multiplication.

Figure 27 - LCTBR-1 Circuit Quiescent Points.

```
**********************************************************************

LOW POWER CMOS CORRELATOR WITH SELF BALANCING & READOUT (LCTBR-1)

                    SMALL SIGNAL BIAS SOLUTION

**********************************************************************

 NODE   VOLTAGE    NODE   VOLTAGE    NODE   VOLTAGE    NODE   VOLTAGE

(  1)  -3.0000   (  2)  -3.0000   (  3)  -7.2877   (  4) -15.0000
(  6)  -3.0000   (  7)  -3.0000   ( 10)  -7.2877   ( 16)  -2.8007
( 17)  -2.8007   ( 18)  -8.7628   ( 19)  -3.0000   ( 36)  -8.7628
( 37)  -3.0000   ( 40) -15.0000   ( 47)  -2.8007   ( 48)  -8.7628
( 53)  -7.2877   ( 57)  -2.7952   ( 58)  -7.5759   ( 66)  -3.0000
( 76)  -2.8007   ( 86)  -8.7628   ( 91)  -2.8007   ( 92)  -2.8007
( 93)  -2.8007   ( 94)  -2.8007


    VOLTAGE SOURCE CURRENTS
       NAME          CURRENT

        VR           0.000      AMPS
        VYF          0.000      AMPS
        VYN          0.000      AMPS
        VXP          0.000      AMPS
        VXN          0.000      AMPS
        VI           0.000      AMPS
        VCC         -5.257-05   AMPS
        VDD          1.537-03   AMPS
        VGG          2.495-05   AMPS
```

Figure 28 The Quiescent Operating Points for LCTBR-1 Transistor

MOSFET OPERATING POINTS

NAME	MODEL	ID	VGS	VDS	VBS	GM	GDS	GMBS	CBD	CB
M1	MPMD	-1.000-14	-4.487+00	0.000	2.801+00	0.000	2.521-05	0.000	3.892-14	3.892-14
M2	MPMD	-1.000-14	-4.487+00	0.000	2.801+00	0.000	2.521-05	0.000	3.892-14	3.892-14
M3	MPMD	-1.000-14	-4.487+00	0.000	2.801+00	0.000	2.521-05	0.000	3.892-14	3.892-14
M4	MPMD	-1.000-14	-4.487+00	0.000	2.801+00	0.000	2.521-05	0.000	3.892-14	3.892-14
PIYL	MN1	1.752-05	2.712+00	2.712+00	0.000	2.051-05	5.107-08	1.863-05	7.897-14	1.990-13
NIYL	MN1	1.752-05	2.712+00	2.712+00	0.000	2.051-05	5.107-08	1.863-05	7.897-14	1.990-13
DYL	MN1	1.752-05	2.712+00	2.712+00	0.000	2.051-05	5.107-08	1.863-05	7.897-14	1.990-13
PIYA	MN1	1.752-05	4.288+00	4.288+00	-2.712+00	2.051-05	5.095-08	8.786-06	5.166-14	7.884-14
NIYA	MN1	1.752-05	4.288+00	4.288+00	-2.712+00	2.051-05	5.095-08	8.786-06	5.166-14	7.884-14
DYA	MN1	1.752-05	4.288+00	4.288+00	-2.712+00	2.051-05	5.095-08	8.786-06	5.166-14	7.884-14
PIXL	MPD1	-3.021-04	0.000	-2.801+00	0.000	3.011-04	1.495-06	3.933-05	9.739-13	2.485-12
NIXL	MPD1	-3.021-04	0.000	-2.801+00	0.000	3.011-04	1.495-06	3.933-05	9.739-13	2.485-12
NCL	MPD1	-3.021-04	0.000	-2.801+00	0.000	3.011-04	1.495-06	3.933-05	9.739-13	2.485-12
PCL	MPD1	-3.021-04	0.000	-2.801+00	0.000	3.011-04	1.495-06	3.933-05	9.739-13	2.485-12
DXL	MPD1	-3.021-04	0.000	-2.795+00	0.000	3.011-04	1.495-06	3.933-05	9.747-13	2.485-12
PIXA	MPD1	-3.021-04	-1.993-01	-5.962+00	2.801+00	3.011-04	1.483-06	1.636-05	5.810-13	9.721-13
NIXA	MPD1	-3.021-04	-1.993-01	-5.962+00	2.801+00	3.011-04	1.483-06	1.636-05	5.810-13	9.721-13
NOA	MPD1	-3.021-04	-1.993-01	-5.962+00	2.801+00	3.011-04	1.483-06	1.636-05	5.810-13	9.721-13
POA	MPD1	-3.021-04	-1.993-01	-5.962+00	2.801+00	3.011-04	1.483-06	1.636-05	5.810-13	9.721-13
DXA	MPD1	-3.021-04	-2.048-01	-4.785+00	2.795+00	3.011-04	1.487-06	1.637-05	6.221-13	9.729-13
PIXCS	MN1	2.959-04	2.420+00	1.237+00	0.000	3.699-04	5.603-05	3.365-04	2.685-12	4.982-13
NIXCS	MN1	2.959-04	2.420+00	1.237+00	0.000	3.699-04	5.603-05	3.365-04	2.685-12	4.982-13
NCCS	MN1	2.959-04	2.420+00	1.237+00	0.000	3.699-04	5.603-05	3.365-04	2.685-12	4.982-13
PCCS	MN1	2.959-04	2.420+00	1.237+00	0.000	3.699-04	5.603-05	3.365-04	2.685-12	4.982-13
DXCS	MN1	3.021-04	2.420+00	2.420+00	0.000	4.258-04	1.060-06	3.872-04	2.070-12	4.982-13

Figure 29 LCTBR-1 Swept Frequency Response

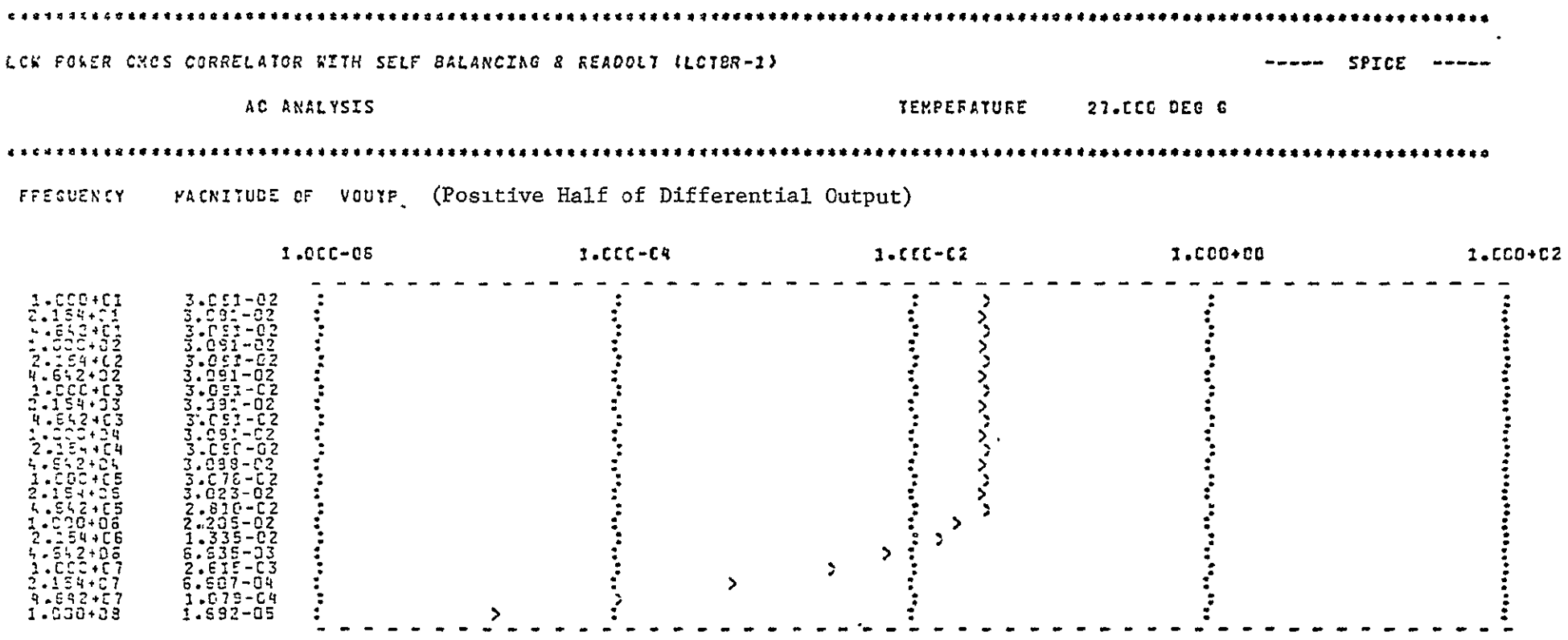


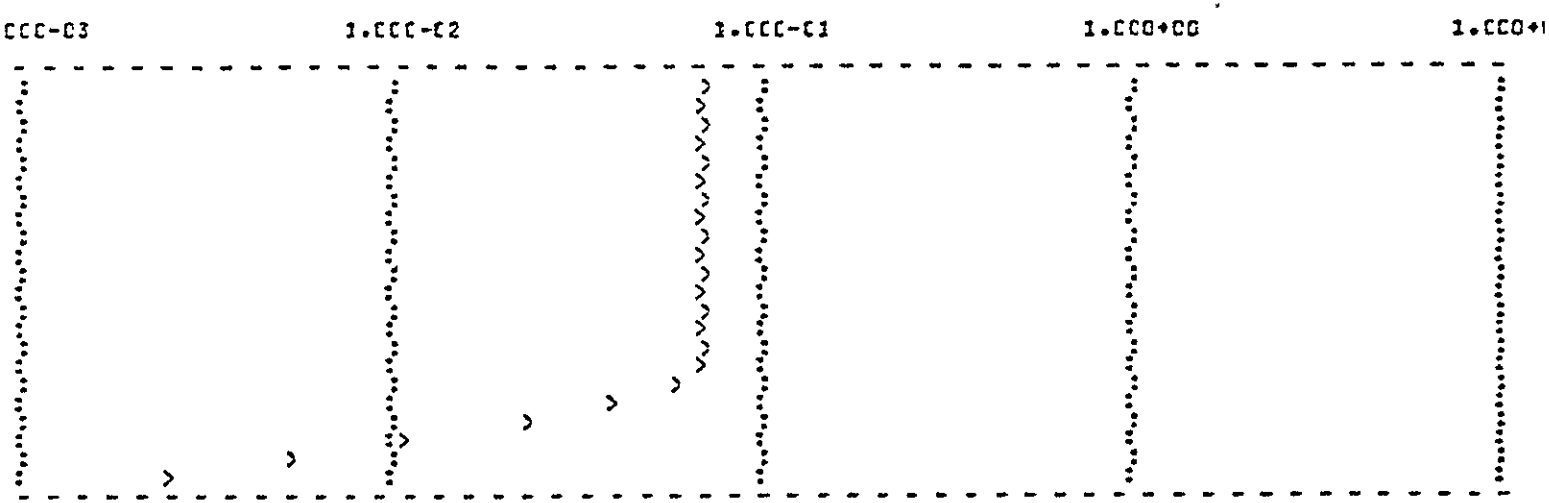
Figure 29 LCTBR-1 Swept Frequency Response (continued)

LCW POWER CMOS CORRELATOR WITH SELF BALANCING & READOUT (LCTBR-1) ----- SPICE -----

AC ANALYSIS TEMPERATURE 27.000 DEG C

FREQUENCY MAGNITUDE OF VG (Gate buffer)

FREQUENCY	MAGNITUDE OF VG
1.000+01	6.977-02
2.154+01	6.977-02
4.642+01	6.977-02
1.000+02	6.977-02
2.154+02	6.977-02
4.642+02	6.977-02
1.000+03	6.977-02
2.154+03	6.977-02
4.642+03	6.977-02
1.000+04	6.977-02
2.154+04	6.977-02
4.642+04	6.976-02
1.000+05	6.973-02
2.154+05	6.961-02
4.642+05	6.906-02
1.000+06	6.668-02
2.154+06	5.801-02
4.642+06	4.024-02
1.000+07	2.196-02
2.154+07	1.085-02
4.642+07	5.106-03
1.000+08	2.458-03



FREQUENCY MAGNITUDE OF VD (Drain buffer)

FREQUENCY	MAGNITUDE OF VD
1.000+01	8.198-02
2.154+01	8.196-02
4.642+01	8.198-02
1.000+02	8.198-02
2.154+02	8.199-02
4.642+02	8.198-02
1.000+03	8.198-02
2.154+03	8.198-02
4.642+03	8.198-02
1.000+04	8.198-02
2.154+04	8.198-02
4.642+04	8.198-02
1.000+05	8.199-02
2.154+05	8.197-02
4.642+05	8.185-02
1.000+06	8.175-02
2.154+06	8.126-02
4.642+06	7.904-02
1.000+07	7.062-02
2.154+07	5.059-02
4.642+07	2.976-02
1.000+08	1.474-02

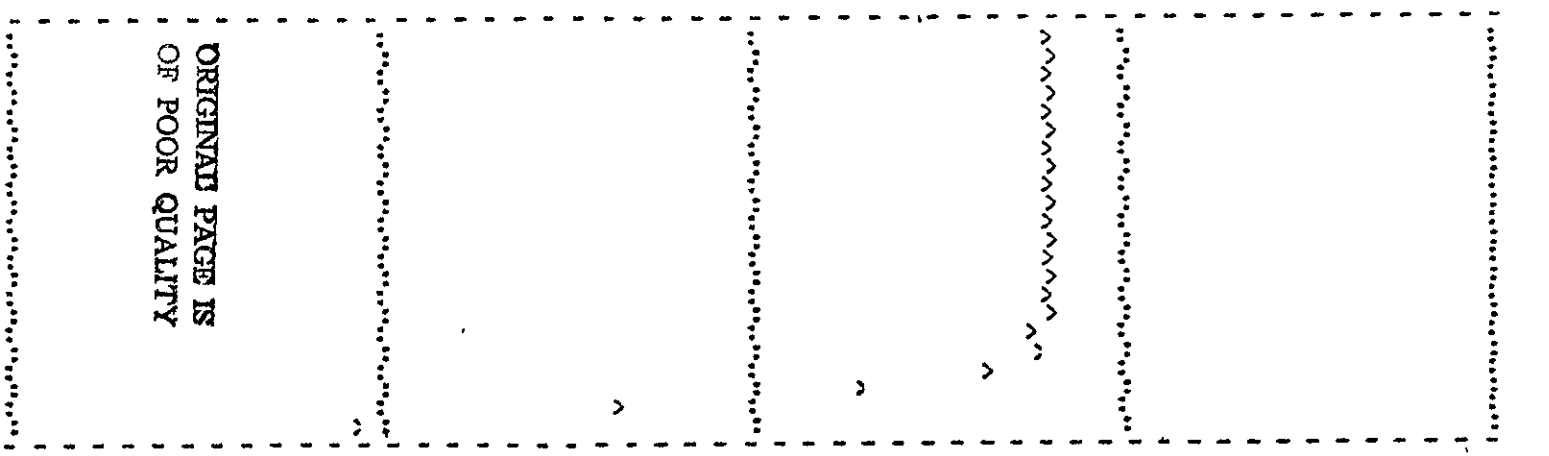


Figure 30 LCTBR-1 Differential Output Spectral Analysis

LOW POWER CMOS CORRELATOR WITH SELF BALANCING & READOUT (LCTBR-1)

FOURIER ANALYSIS

FOURIER COMPONENTS OF TRANSIENT RESPONSE OF VOUTD

DC COMPONENT = -2.671-06

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALISED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000+05	5.518-06	1.000000	-94.085	.000
2	2.000+05	5.216-06	.945268	-100.004	-5.920
3	3.000+05	6.234-04	112.963194	55.288	149.373
4	4.000+05	4.915-06	.890590	-108.896	-14.812
5	5.000+05	5.928-04	107.415090	-142.540	-48.455
6	6.000+05	4.582-06	.830230	-117.398	-23.313
7	7.000+05	4.547-06	.823984	-118.689	-24.604
8	8.000+05	4.170-06	.755599	-129.798	-35.713
9	9.000+05	3.925-06	.711250	-129.393	-34.308

TOTAL HARMONIC DISTORTION = 15588.360352 PERCENT

Additional data from the two typical CAD models are presented in Table 2 for easier comparison and analysis. Quite apparent is the reduced power consumption of the complementary follower versus the small inverter for providing comparable gate buffering. Also shown in Table 2 are the power economies enabled by the use of depletion mode PMOS in the CSRO and LCTBR-1 models versus the enhancment-mode MCISM-7-1 model.

6.3 Performance As A Function of Design and Process Parameters

In the above section, we saw the impact of depletion mode versus enhancement mode transistors on power consumption. Also implied was a dependence on device geometry. Consequently, further specification of performance limits the range of many of the device design parameters.

TABLE 2 TRIODE MULTIPLIER BUFFERS' SPEED AND POWER

ITEM	CIRCUIT MC1SM-7-1	LCTBR-1	CSRO
Gate Buffer	PMOS INVERTER	NMOS FOLLOWER	-
current, μa.	54.3	17.5	-
power supply, volts	20	7	-
power consumption, mW	1.086	0.123	-
transconductance, micromhos	(22.6)	20.5	-
maximum frequency, MHz	(2.2)	2	-
Drain Source Buffers	PMOS FOLLOWERS		
Drain Buffer Transistor Name	Q45	MPIXL	MPOA
geometry (W/L)	28.6	(40.34)	14
current, μa.	100.7	302.1	134.7
(VGS-VT), volts	1.20	2	2
transconductance, micromhos	(168)	301.1	104.5
power supply, volts	8	8	5
power consumption, mW	0.806	2.42	0.674
maximum frequency, MHz	(2.5)	5	(1.7)
Multiplier Triode (W/L)	1	(1.1)	-
Buffer/Multiplier Ratio	28.6	37.5	-
Multiplier "Self-Bais" (V_{GS} - VT), volts	5.7	6.5	-
Source-Current Readout: current, μa.	-	-	151.2
power supply, volts	-	-	12
power consumption for half of balanced triode multiplier, mW,	-	-	1.81
maximum frequency, MHz	-	-	1

(XXX) indicates data not predicted by CAD routine but extrapolated therefrom.

6.3.1 Input Dynamic Range

If one defines the input dynamic range as the ratio of the maximum to minimum usable signals as prescribed by the desired rejection ratios, then combining the results of the preceding sections (i.e., equations 30,37, and 39) give a direct formula for the input dynamic range in terms of chip geometry and voltages. It may readily be shown that the greatest input dynamic range is obtained when the ac drain signal is held constant at its minimum value:

$$x_{max} = x \text{ (constant)} = x_{min} = \psi \cdot \overline{(\Delta V_T)} \tag{52}$$

We then derive

$$\bar{y}_{max} = \zeta \, y_{min} = \zeta \, \psi \, (\Delta V_T) \tag{53}$$

by substitution into equation (37):

$$\bar{\psi} \, \overline{(\Delta V_T)} \, (\Gamma_d/2 + \zeta) \leq (Y_o - V_{T_m}) - (1 + \Gamma_d/2) \, \overline{(\Delta V_T)}$$

or, for a singly-balanced triode multiplier, the direct output is governed by

$$\overline{(Y_o - V_{T_m})} \geq (\Delta V_T) \left\{ \psi (\Gamma_d/2 + \zeta) + \Gamma_d/2 + 1 \right\} . \tag{54}$$

Using equation (54) for the case of 0.1 volt threshold uniformity and both ψ and Γ_d are to be 40 dB, with $\zeta = 10$, gives the result $(Y_o - V_{T_m}) \geq 605$ volts. This absurd result is further evidence of the need for a special technique to ease the rigorous conditions imposed by equation (54). One final remark on equation (54) is needed here before we show how published experimental array data[1] support equation (54). From Equation (54), it is obvious that the input dynamic range to a multiplier array, ζ, as defined by equation (53) is severely limited, at best. The limited input dynamic range

of the multiplier array contrasts sharply with the average dynamic range of many imaging or simple analog delay CTD's which may sometimes be as large as 80 dB. That is, the multiplier array cannot fully use the typical dyanmic range of the CTD analog delay lines at its input.

An alternate definition for input dynamic range may also be considered. Above, the two minimum signals are defined as comparable to the array threshold nonuniformities, (ΔV_T), since sample-to-sample signal increments of that value would be difficult to distinguish from the comparable "voltage" increments arising from fabrication nonuniformities. The alternate definition for minimum input signal is the minimum input signal-increment needed to give signal detection at the output with unity signal-to-noise ratio. Thus, over and above the array nonuniformity problem (which is likely to be indistinguishable from the signal); this definition is more complex and involves the specific nature of the output, especially its minimum detectable signal, as well as some effective device transfer function. Independent of the fine points of the definition of input dynamic range, we must still address the question "can a CTD/MOS triode correlator chip not requiring exotic fabrication ever become a practical reality?"

In applying equation (54), we can no longer ignore the restriciton of equation (30) which was not previously incorporated into equation (54). We recall equation (30) relates the maximum ac signal on the gate to the gate harmonic distortion rejection, Γ_g, as well as the geometric ratios of the buffer and the triode:

$$\underline{y}_{max} = \frac{g_{mB}}{\alpha_m \Gamma_g} \quad (30)$$

As derived earlier, the drain buffer is best configured as a source follower fed by a current source (CS), thereby enabling us to give some additional useful relationships for equation (30). From the pentode equation:

$$I = \frac{\mu C_{ox}}{2} \cdot \left(\frac{W}{L}\right) (V_{GS} - V_T)^2 \quad , \tag{55}$$

it may be shown that

$$g_{mB} = \frac{2 I_{cs}}{(V_{GS} - V_T)_B} = \frac{2 I_{cs}}{(V_{GS} - V_T)_{CS}} \times \left[\frac{(W/L)_B}{(W/L)_{CS}}\right]^{1/2} \tag{56}$$

or

$$g_{mB} = \mu C_{ox} \left[\left(\frac{W}{L}\right)_B \cdot \left(\frac{W}{L}\right)_{CS}\right]^{1/2} (V_{GS} - V_T)_{CS} \tag{57}$$

Combining equations (30) and (57) gives

$$y_{max} = \frac{(V_{GS} - V_T)_{CS}}{\Gamma_g} \cdot \frac{[(W/L)_B (W/L)_{CS}]^{1/2}}{(W/L)_m} \tag{58}$$

Substituting equation (58) into (53) yields a more useful description of the input dyanmic range, ζ:

$$\zeta = \frac{y_{max}}{y_{min}} = \frac{(V_{GS} - V_T)_{CS}}{(\Delta V_T \ \psi \Gamma_g)} \cdot \frac{[(W/L)_B (W/L)_{CS}]^{1/2}}{(W/L)_m} \tag{59}$$

Use of CMOS with depletion mode P-channel for lower power gives $(V_{GS} - V_T)_{CS} \sim$ pinch-off voltage ~2 volts; and for $\Delta V_T \sim$ 0.1 volt,

we find,

$$\frac{(V_{GS} - V_T)_{CS}}{\Delta V_T} \sim 20,$$

thereby leaving the input dynamic range ζ dominantly controlled by the buffer/multiplier triode geometry and the desired error rejection ratios. Having reformulated ζ into a more useful expression, we may do likewise for equation (54), and at the same time incorporate additional factors to account for the benefits of the sequential multiply operator as well as doubly versus singly balanced operation.

We define a new set of performance parameters, designated with a prime, which specify the desired performance at the output of the sequential processor and are related to the corresponding performance parameters within an equivalent singly balanced triode array. Table 3 concisely summarizes such a relationship for modifying formulas (54) and (59) by means of a minimum expected enhancement ratio.

TABLE 3

PROJECTED PERFORMANCE ENHANCEMENT FOR A BALANCED TRIODE MULTIPLIER

Item	Symbol for Value After Sequential Processing	Expected Enhancement			Equivalent Unprocessed Singly Balanced
		Source	Typical	Minimum	
Gate Harmonic Distortion Rejection	Γ'_g	Double vs Single Balance	10 dB	6 dB	$\Gamma_g = (\Gamma'_g)/2$
Drain Harmonic Distortion Rejection	Γ_d'	Sequential Multiply Operator	10 dB	6 dB	$\Gamma_d = (\Gamma'_g)/2$
Input Feedthrough Rejection	Ψ'	Sequential Multiply Operator	60 dB	50 dB	$\Psi = (\Psi')/316$

Substituting from Table 3 into (54) and (59) we find

$$\zeta = (632)\,\frac{(V_{GS} - V_T)_{CS}}{(\Delta V_T)\ \psi' \Gamma'_g} \cdot \frac{[(W/L)_B\,(W/L)_{CS}]^{1/2}}{(W/L)_m} \qquad (60)$$

$$\frac{(Y_o - V_{T_m})}{\Delta V_T} \geqq 3.16 \times 10^{-3}\ \psi'(\Gamma_d'/4 + \zeta) + \Gamma_d'/4 + 1 \tag{61}$$

These formulas now enable us to use an attractive 40-dB rejection ratio for each source of error $(\psi' = \Gamma'_d = \Gamma'_g = 100)$ to predict the resultant input dynamic range. For the low power CMOS with depletion mode P-channnel buffers, a reasonable range for $(Y_o - V_{T_m})$ is 5 to 7 volts with an approximate value of 0.1 volts for ΔV_T, thereby giving an estimate of

$$\zeta = \frac{316}{\psi'}\left[\frac{Y_o - V_{T_m}}{\Delta V_T} - \Gamma_d'/4 - 1\right] - \Gamma_d'/4 \tag{62}$$

or $\zeta = 82$ or 38.3 dB. This result, however, cannot exceed the restriction of equation (60). A typical pinchoff for our depletion mode P-channel is about 2 volts, thereby yielding

$$\frac{[(W/L)_B\,(W/L)_{CS}]^{1/2}}{(W/L)_m} \cong 65. \tag{63}$$

6.3.2 Power and Speed versus Size

Design decisions made at this point strongly influence the power consumption per multiplier, since it affects the main power users in the multipliers, namely, the source and drain buffers The 38-dB input dynamic range arose from a triode bias that can be achieved from the same complementary buffers mentioned in the description of the pentode squaring multiplier, and partially incorporated in the LCTBR-1 model so as to give a 4.5 volt dc gate bias augmented by a 2 volt pinch-off. Now for the drain-source buffers to meet the condition of equation (63), we note that a 2-volt pinch-off P-channel FET with gate and source connected conducts about 12 μA for unity (W/L), so for (W/L) = 65

the current becomes 780 μA for a minimum power consumption of 3.9 mW per buffer.

An attractive option, however, is to use a smaller current source with a larger source-follower buffer. While this saves power in direct proportion to the reduction of the current source, the size of the buffer rapidly becomes unmanagable. A potential compromise is to reduce the current source by a factor of three while increasing the buffer by three times so as to still satisfy equation (63). This results in a drain buffer power of 1.3 mW (that is, 260 μA at 5 volts) while the frequency response of this buffer extends to nearly 7.5 MHz. Allowing for a 5 micrometer source drain spacing after diffusion, the net transverse dimension becomes 0.0384 inch, which is a rather sizable MOSFET.

6.4 Performance Enhancement Techniques

So far much of the discussion and derived formation involves singly-balanced triode multipliers as illustrated in Figures (7) and (8), with occasional references to more highly balanced configurations as in Figure (22). As long as the complementary buffers provide adequate bias to the multipliers, more distortion errors arise from the pentode mode buffers carrying the multiplier currents than from the nonlinearities of the multiplier triode itself.

6.4.1 Double-Balanced Triode Configuration

In Figures (7) and (8), the reference triode, QR, is given a dc gate bias which is equivalent to creating a fixed conductance equal to the dc average value of the modulated conductance, QM. Since the currents through the two conductances are differenced,

the large components of the currents due directly to the signal applied to the common (drain) conductance node should cancel, leaving only the product current arising from the modulated conductances, as implied in equation (26). Now, if an ac signal shifted 180° in phase from the ac component on the gate of QM is added to the dc already on the gate of QR, we observe two important improvements in the multiplication.

First is a doubling of the desired product current since subtraction of currents through conductances which are modulated 180° out of phase gives constructive addition of the two components. Note the dc conductances are still the same and help cancel a direct feedthrough of the signal applied to the multiplier drain. But with the second conductance modulated 180° out of phase from the first, the incremental currents related to the multiplier gate signal nominally cancel at the common (drain) conductance node driven by the drain buffer. Or equivalently, in order to apply equation (30), we may describe the balanced (push-pull) gate operation as nominally cancelling the effective ac voltage V_y to a much smaller value, thereby increasing the rejection of gate signal distortion.

The benefits of such nominal cancellation are clearly listed in Table 4 which is derived by MSINC computer-aided-design (CAD) modelling of the various multiplier circuits. The four parts of the Table give the spectral analysis of the output for basically identical triodes, buffers, and biases configured first as singly balanced, then doubly balanced, and finally as quadruply balanced multipliers. Figure 22 illustrates the important elements needed to give (1) self-biasing implied by the "dummy" reference

TABLE 4

COMPARISON OF TRIODE MULTIPLIER CONFIGURATION (INCLUDING BUFFERS)

Configuration (MCISM)	Single Bal (4-4)	Double Bal (6-9)	Quad Bal (7-1)	Quad Bal (7-2)
Input. (mV)				
Drain – F_D = 60 KHz	0 DC; 125 AC	200 DC; 125 AC	+200, +200 DC, ±125 AC	+200 DC; 125 AC
Gate – F_G = 300 KHz	0 DC, 125 AC	200 DC; 250,-300 AC	200 DC; +250,-300 AC	–200 DC, –150 AC 200 DC; +250, –300 AC
Output (Fourier Coef)				
(μV) $F_G - F_D$	244	982	1023	1139
$F_G + F_D$	208	838	922	1028
RSS ($F_G \pm F_D$)	321	1290	1377	1534
F_D	174	851	834	929
F_G	106	2730	0 629	3159
$2F_D$	0.704	2 266	0 629	1.823
$2F_G$	1 042	2 908	0 838	3.803
RSS ($2F_G \pm F_D$)	1 937	3.280	1 752	3.879
RSS ($F_G \pm 2F_D$)	1 004	3 486	.950	3.900
Drain Harmonic Rejection	53.2 dB	55 1 dB	66 8 dB	58 5
Gate Harmonic Rejection	49 8 dB	52 9 dB	64 3 dB	52.1
RSS ($2F_G$, $2F_G \pm F_D$) Distortion	43.3 dB	49 4 dB	57.0 dB	49 0
RSS ($2F_D$, $F_G \pm 2F_D$) Distortion	48.3 dB	49 8 dB	61 4 dB	51 0
Total RSS Distortion	42 1 dB	46 6 dB	55 7 dB	46.9
Input Feedthrough Rejection. Drain	5.3 dB	3 6 dB	4 4 dB	4 4
Gate	9.6 dB	– 6.5 dB	66.8 dB	– 6.3

77-0321-T-21

level, X'_o, and (2) on-chip product-current-summation at internal-voltage-controlled, ac-virtual-ground node with current-to-voltage conversion by means of the "grounded-gate" source-input stages having the "dummy" reference level X'_o on their gates and operating in the pentode mode so that voltage fluctuations on the drains (which are connected in common as indicated in the figure) have negligible effect on the virtual ground nodes. In fact, in the CAD simulation, the summation busses were biased through 20K ohm resistor to convert current to voltage with the differential output voltage equal to the voltage difference between the two pentode drains connected to the summation busses. Unneeded elements were simply disconnected for the single and double balanced simulations.

In Table 4, all ac values are Fourier coefficients giving the center-to-peak value of the sine wave. The input dc values are the quantities $(X_o - X'_o)$, $(X''_o - X'_o)$ for the drain and $(Y_o - Y'_o)$ for the gate, and are intended to approximate a worst-case array threshold nonuniformity which may develop at any individual multiplier due to the self-bias technique or the user/operator bias routine described earlier. No such threshold nonuniformities were incorporated in the singly balanced model, so we must assume those output results to be the best performance limit. Thus, in the first two columns, we are really comparing "best case" of singly balanced versus "worst case" of doubly balanced, with the gate signal more than doubled for the latter case.

First, the four fold increase in output signal is obvious: twice for the larger input signal and twice for the double balancing. Secondly, rejection of distortion at $(2\ f_G,\ 2\ f_G \pm f_D)$ is improved by

6 dB despite a more than doubled gate signal and a dc source/drain bias, both of which should have rejection of that distortion worse in a singly balanced multiplier.

Consequently, the doubly balanced version appears to have a significant performance advantage of about 10-dB harmonic distortion rejection over the single balanced model, at no extra cost of power or complexity within the basic multiplier cell.

The true added cost of the better performance is the differential input stage with balanced outputs feeding two rather than one CTD analog delay line.

An important comment on achieving the balanced or push-pull gate signal is needed here. Use of a differential-input balanced output circuit at each and every multiplier location has been previously investigated both at Westinghouse and elsewhere.[7] It is our conclusion that such an approach not only adds extra complexity, real estate, and power consumption at each multiplier location, but also is likely to result in greater nonuniformities across an array. A single serial differential-input, balanced-output circuit feeding two delay lines with source-follower buffer is more likely to give uniform parallel outputs than an array of dif-amps (whose balanced outputs resemble the output drains of MOSFET inverter stages) with nonuniform inputs and current sources.

6.4.2 Quadruply-Balanced Triode Configuration

In the preceding configurations, a single drain driver applied a signal to the common drain node of a matched pair of conductances which are modulated by a suitably applied gate signal.

That is, the (complementary) y-related "gate-signal" currents may be pictured as circulating in the QM/QR loop of Figure 13, which becomes a closed loop by means of the virtual-ground source buffers connected to the two triode sources, with only the uncancelled/ differential constituent of the y-related current flowing in the drain buffer. The next level of balancing requires the addition of a second drain driver and a second set of matched MOSFET triode conductances, as shown in Figure 22, with their sources cross-coupled to the two previously-used, self-biasing ac-virtual-grounds. As with the doubly-balanced triode configuration, the (complementary) x-related,"drain-signal" currents may be pictured as circulating between the two oppositely-phased drain buffers through the two pairs of triodes with only a small unbalanced differential component flowing through the virtual-ground source buffers. The second drain driver is associated with a second CTD analog delay line transporting a signal of opposite phase relative to that in the CTD shift register which supplies the first drain driver. As with the balanced gate signals, the "push-pull" operation for the two drain drivers is easily achieved via a single differential-input, balanced-output circuit feeding two CTD shift registers. In this case, however, the second shift register was already previously used as the dummy reference level element and requires only minimal change to provide the needed "push-pull" signals to the two drain drivers.

Examination of the results in Table 4 for the quadruply balanced configuration show nearly 10 dB additional total harmonic distortion rejection for the case when the equivalent dc offsets are the same and the ac signals are equal and opposite. The more likely case is that both the ac and dc components will be different.

It may indeed be shown that the input feedthrough rejection of the gate drains are opposing. On the other hand, the output signal did not double relative to the output of the comparable doubly balanced configuration. Thus, Table 4 does not demonstrate an obvious vastly superior performance for the quadruply balanced configuration. Consequently, additonal computer simulation and breadboard investigation are still needed to evaluate the merits of the quadruply balanced multiplier, since each basic multiplier cell contains an extra buffer and triode pair not needed in the simpler version.

6.4.3 Sequential Multiply Architecture

The general architectural requirements for the sequential multiply were presented in Figure 9 through 12. Namely there must be interlaced storage for both reference and data in both signal channels. For the self-bias of triode multipliers, there must be additional"reference-only" cells which are used to set the voltage for the ac-virtual-ground current summing. All these requirements have been incorporated in Figure 31, 32, 33 and 34, which may be regarded as block diagrams for the various attractive multiplier configurations.

To provide for a valid self-bias reference level needed at all times by the singly balanced (Figure 31) and the quadruply-balanced (Figure 34) triodes, both configurations use the sample/hold buffered tap described in Figure 2. Fully synchronized analog data availability in both the double balanced triode (Figure 32) and the dual pentode (Figure 33) permit virtually any type of NDRO tap. This feature in the doubly-balanced triode is achieved by means of a full "dummy" reference only channel solely for averaging

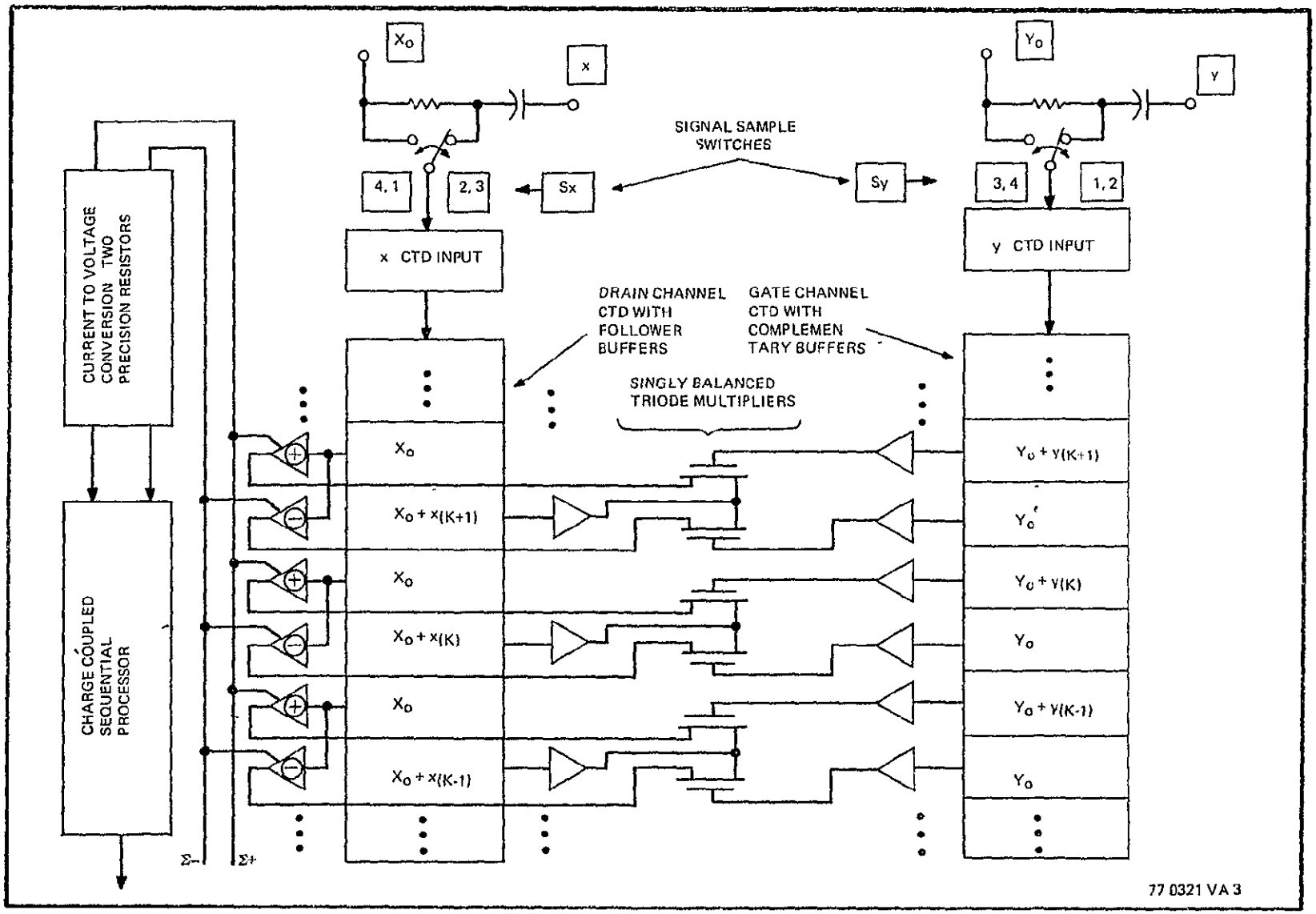


Figure 31 Singly-Balanced Triode Multiplier Architecture

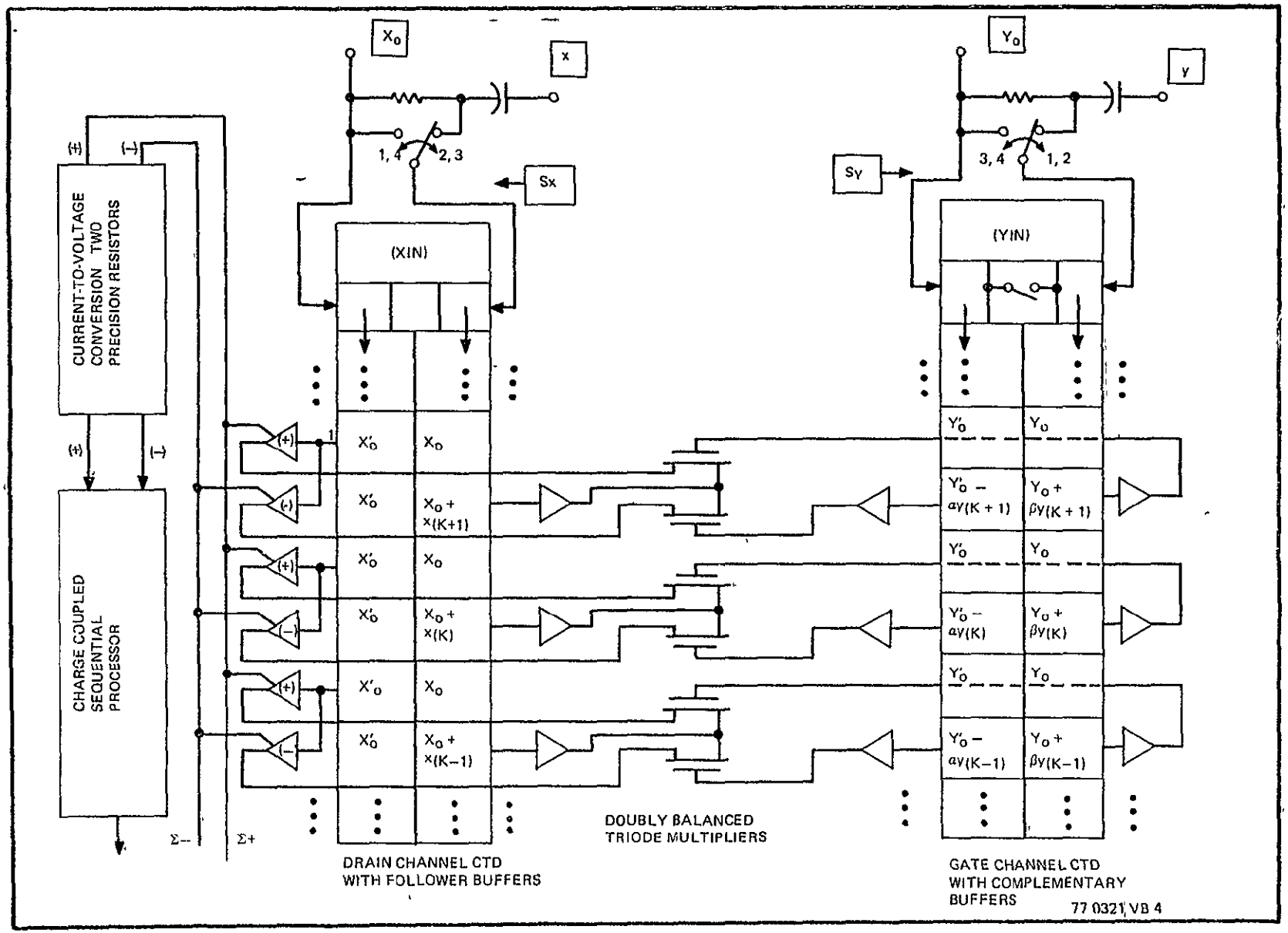


Figure 32. Architecture of Doubly-Balanced Triode Multiplier Array

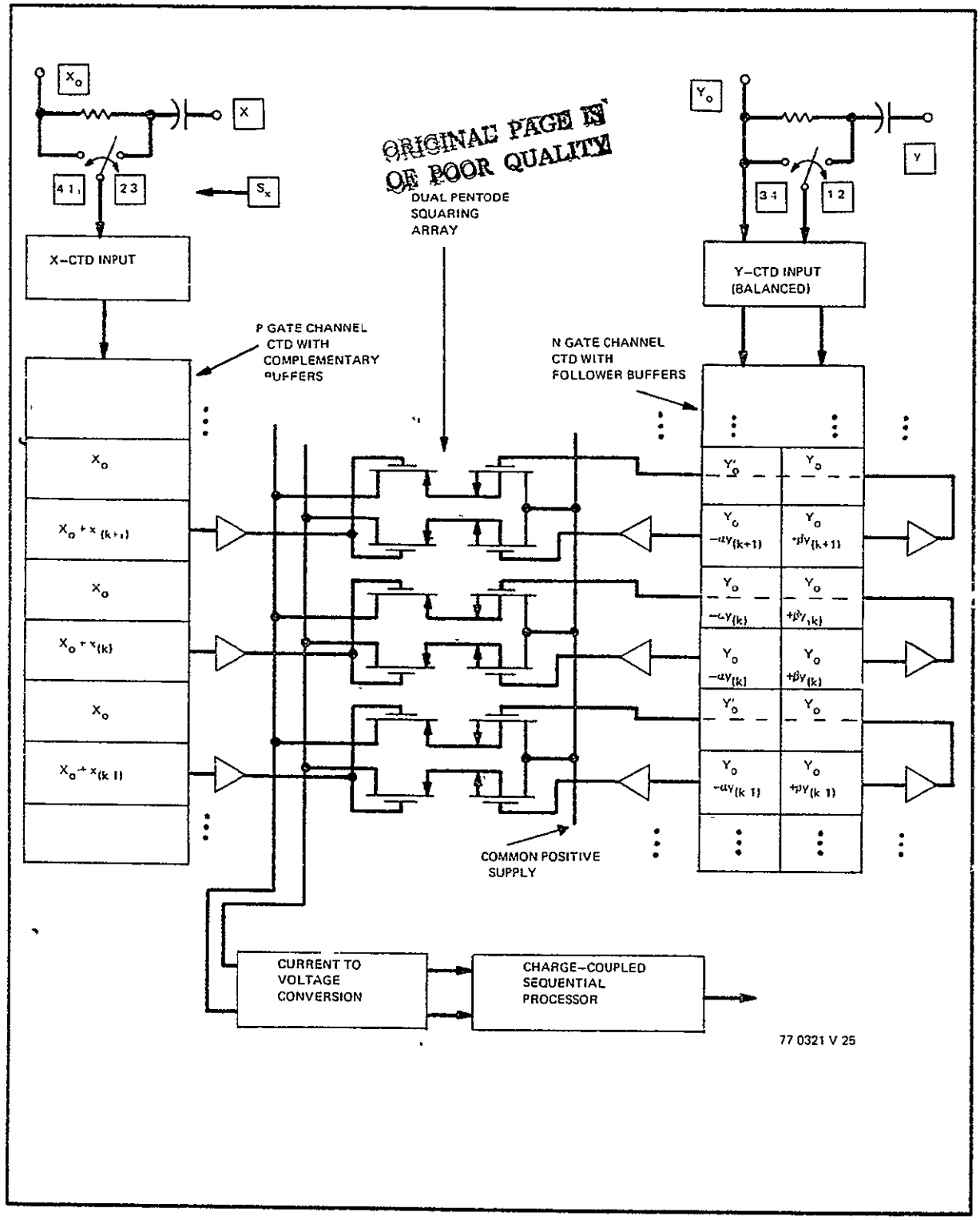


Figure 33. Dual CMOS Pentode
"Difference of Squares"
Correlator

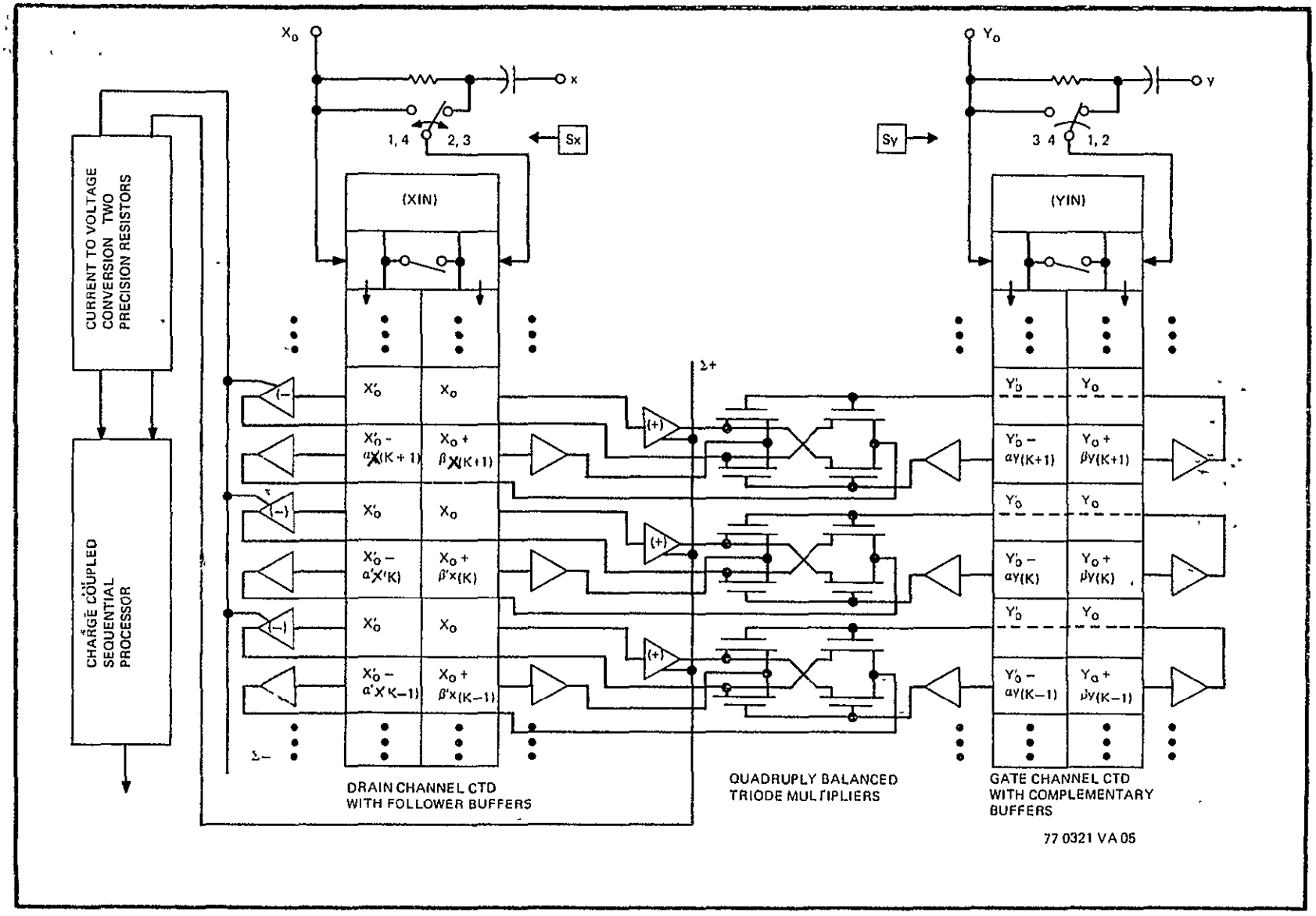


Figure 34. Architecture of Quadruply Balanced Triode Multiplier Array

over the array to set the self-bias. In all cases where "push-pull" balancing is used (i.e. all except for the singly-balanced triode of Figure 31), a serial input differential stage with balanced outputs is used to feed two symmetric shift registers for each such channel. In such push-pull channels, complementary data are interlaced with reference-only samples and move together through the registers as indicated in Figure 32. 33, and 34.

A final comment on the use of balanced configurations with the serial multiply operator: the previously presented theory based only on a single (not paired) triode suggests that such a single multiplying element could give a usable output product when processed by an ideal sequential multiply operator. The real limitation, however, is the accuracy of the four sequential additions/subtractions. Consequently, coarse "geometric" balancing is used in all cases to provide an initial approximate cancellation so as to relax the accuracy requirements for the sequential arithmetic.

6.5 Performance Comparison: Single Multiplier Versus Multiplier Array

So far we have examined many of the components of CCD-based correlators as well as some of their interactions. We will now discuss the probable characteristics of an array of such components as illustrated in Figure 31. Buffer stages indicated by triangles are essentially like those included in the circuit of Figure 22, where the self-bias, ac-virtual-ground readout buffers of Figure 22 correspond to the triangles containing the algebraic signs. While alternate means can be used to achieve the self-bias function, the approach implied in Figure 31 accomplishes array threshold averaging and is also amenable to the slight change needed to incorporate other necessary schemes required for desired perfor-

mance. Thus, for the remainder of the technical discussion, the architecture of Figure 31 will be the minimally assumed configuration.

In order to better understand how an array like that of Figure 31 operates, we must first describe the behavior of the array in terms of the previously described behavior of its constituents,

> Hence, we define an analog multiplier cell building block to consist of those CCD analog delay stages with suitably buffered nondestructive readouts appropriately interconnected with multiplying elements so as to provide all the necessary simultaneous (parallel) analog data to a common (on-chip) output-processing circuit which completes the computation of a true four-quadrant multiply (to include dc restoration as needed) and gives a fully-reconstructed, step-wise output waveform.

For example, the circuit of Figure 22 with the addition of the associated CCD delay stages forms the building block for a quadruply-balanced triode multiplier cell.

Previously, we observed that any such multiplier cell is most critically characterized by spectral analysis of its output. The relative amplitudes of the various spectral components of the output (when two sine waves are applied inputs) readily pinpoints such problem areas as lack of detailed balance, excessively large signals or other harmonic/intermodulation distortions arising from inadequate buffer conductance, etc. But, this analysis tool must be corrected for use with arrays like that of Figure 31. From the CAD simulations presented in Table 4 we recall the Fourier components of interest included: f_D, f_G, $f_G \pm f_D$ $2f_G$, $2f_D$, $2f_G \pm f_D$, and $f_G \pm 2f_D$,

where f_D and f_G are the frequencies applied respectively to the drain and gate of the triode multiplier. To see the effect on each Fourier component, we first examine an array of ideal multipliers as illustrated in Figure 1. From sampled data theory we have

$$x_k = x \sin 2\pi f_D (t - kT_c)$$
$$y_k = y \sin 2\pi f_G (t-kT_c) \tag{64}$$

where $1 \leq k \leq N$ is the index within the array and T_c is the data sampling interval. Hence, the ideal output becomes

$$z(t) = \sum_{k=1}^{N} xy \sin 2\pi f_D (t-kT_c) \sin 2\pi f_G (t-kT_c) \tag{65}$$

Rewriting,

$$z(t) = \frac{xy}{2} \sum_{k=1}^{N} \left\{ \cos 2\pi (f_G - f_D) (t-kT_c) - \cos 2\pi (f_G + f_D) (t-kT_c) \right\} \tag{66}$$

Hence, the general summation is of the form

$$S = \sum_{k=1}^{N} \cos 2\pi f (t-kT_c) \tag{67}$$

To simplify the analysis, we approximate the discrete summation of equation (67) by an integral over the same time period, letting $g = t-kT_c$ and $dg = -T_c dk$, to obtain

$$S \cong (-1/T_c) \int_{t-T_c}^{t-N\,T_c} \cos 2\pi fg \, dg \tag{68}$$

Thus $S = (2\pi f T_c)^{-1} \left[\sin 2\pi f (t-T_c) - \sin 2\pi f (t-N\,T_c)\right]$

Rearranging,

$$S \cong - (\pi f T_c)^{-1} \sin \pi f (N-1) T_c \cos 2\pi f \left(t - \frac{N+1}{2} T_c\right) \tag{69}$$

or
$$S = \sum_{k=1}^{N} \cos 2\pi f(t-kT_c) \cong -(N-1)\left[\frac{\sin \pi f (N-1) T_c}{\pi f (N-1) T_c}\right] \cos 2\pi f\left(t-\frac{N+1}{2} T_c\right) \tag{70}$$

Now we may apply the result of equation (70) to either the ideal multiplier array of equation (66) or the more realistic predictions of Table 4. The output spectrum of such an array will have different amplitudes approximately adjusted by the factor

$$(N-1)\left[\frac{\sin \pi f (N-1) T_c}{\pi f (N-1) T_c}\right] \tag{71}$$

where the array contains N cells and f is the frequency of the spectral component of interest. Let us consider a hypothetical example where a 10 μsec sample interval is used while the inputs to a 32 point array are sine waves with the frequencies, f_D=6kHz and f_G =7kHz. The resultant relative correction factors from equation (71) relating array spectra to Average cell spectra become:

Fourier Component	f_G-f_D	f_D	f_G	$2f_D$	f_G+f_D	$2f_G$
Frequency	1 kHz	6kHz	7kHz	12kHz	13 kHz	14 kHz
Adjustment	1.42dB	22.75dB	22.54dB	23.62dB	42.58dB	23.84dB

That is, if the average constituent cell had an input feedthrough of f_D comparable to the sum or difference frequency, in the array output that feedthrough would appear to be (22.75-1.42) = 21.33 dB below the difference frequency output due solely to the sampled data correction factor of equation (71). Thus, formula (71) enables diagnosis of array spectra data into that for the Average cell so as to pinpoint problem areas of inadequate performance.

7.0 DELIVERED HARDWARE

During the course of the contract a few hardware items have been fabricated and delivered. In this section, we first briefly describe the various delivered items, followed by a summary of the published performance data.

7.1 MOSFET/CCD "Building Blocks"

To experimentally investigate the various sources of distortion and/or offsets as well as other circuit performance characteristics, a general purpose array of sixteen PMOSFET's were fabricated on a CCD chip. The metallization pattern for this array is illustrated in Figure 35. The MOST's have a variety of width to length ratios (W/L), indicated by the number adjacent to each gate. The following distribution of devices was selected:

8 with W/L = 5
4 with W/L = 10
2 with W/L = 50
2 with W/L = 100

The serial in/parallel out analog delay lines initially used were those developed at Westinghouse for use in various CTD discrete analog signal processing programs, such as some supported by the Naval Research Laboratories (contract number N00014-75-C-0283 and N00173-76-C-0147), and described in the IEEE ISSCC-76 Digest of Technical Papers (pp. 194-95).[6]

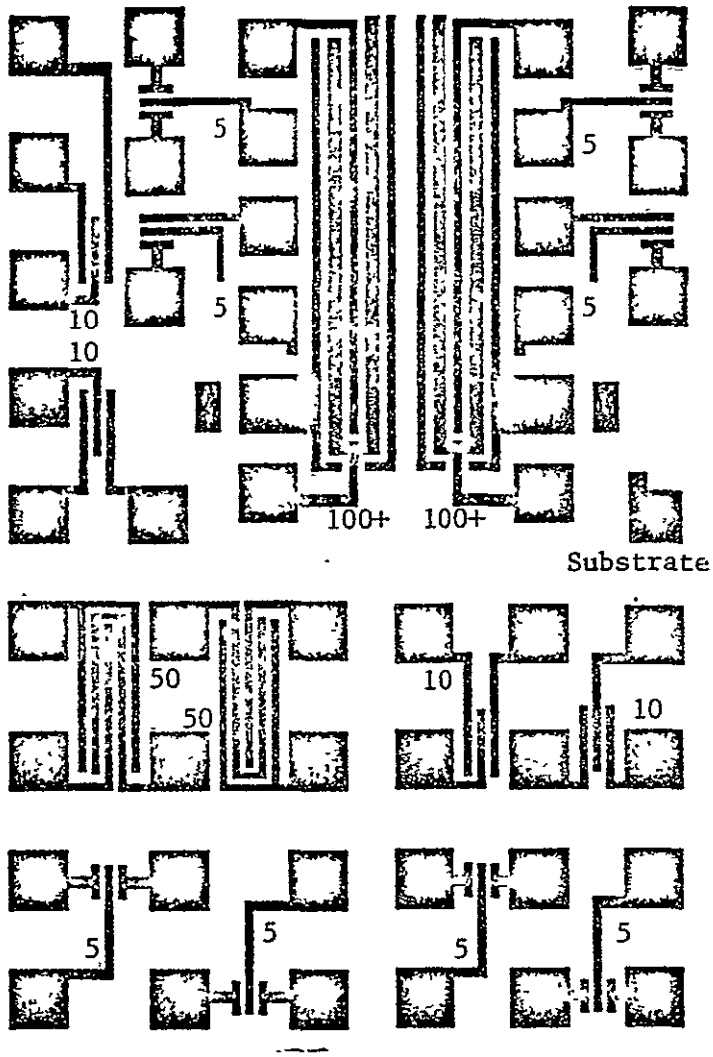


Figure 35 CCD Correlator PMOST modeling array (metallization pattern)

7.2 Feasibility Demonstrator for Sequential Multiplication with Self-Bias

The "Sequential Mulitply", schematically pictured in Figure 36, is designed to demonstrate a four step sequential multiplication of two signals. The exerciser is intended to be a feasibility demonstration unit and as such contains all necessary power supplies and a crystal clock. The control circuitry for the two CCD's and the sequential multiplier is contained on three circuit boards. One board generates all of the digital control signals Another board contains the regulators that supply the various voltage levels to the CCD and multiplier. The third board is the analog processor.

The digital board shown in Figure 37 has a crystal controlled oscillator which provides the basic frequency for the control logic. This frequency is divided by counters B and C. Counter B divides by 12 and counter C by 16. These two counter address 3 PROMs. One PROM (D) provides the timing for the X channel CCD. An identical PROM (E) provides the timing for the Y channel CCD. The waveforms for the X and Y channel PROM are inverted to provide the necessary phase difference between the two channels. The third PROM (F) provides the signals needed to do the clamp, sample, and difference operations in the analog processor. Two signals (that control the inputs to the CCD's) are decoded directly from the counters.

All of the control signals from the ROM's are strobed into flip-flops (G,H,J,K,L,M) to remove spikes associated with the decoding in the PROM's. The outputs of these flip-flops go to drivers which convert the logic level signals to higher voltages needed to operate

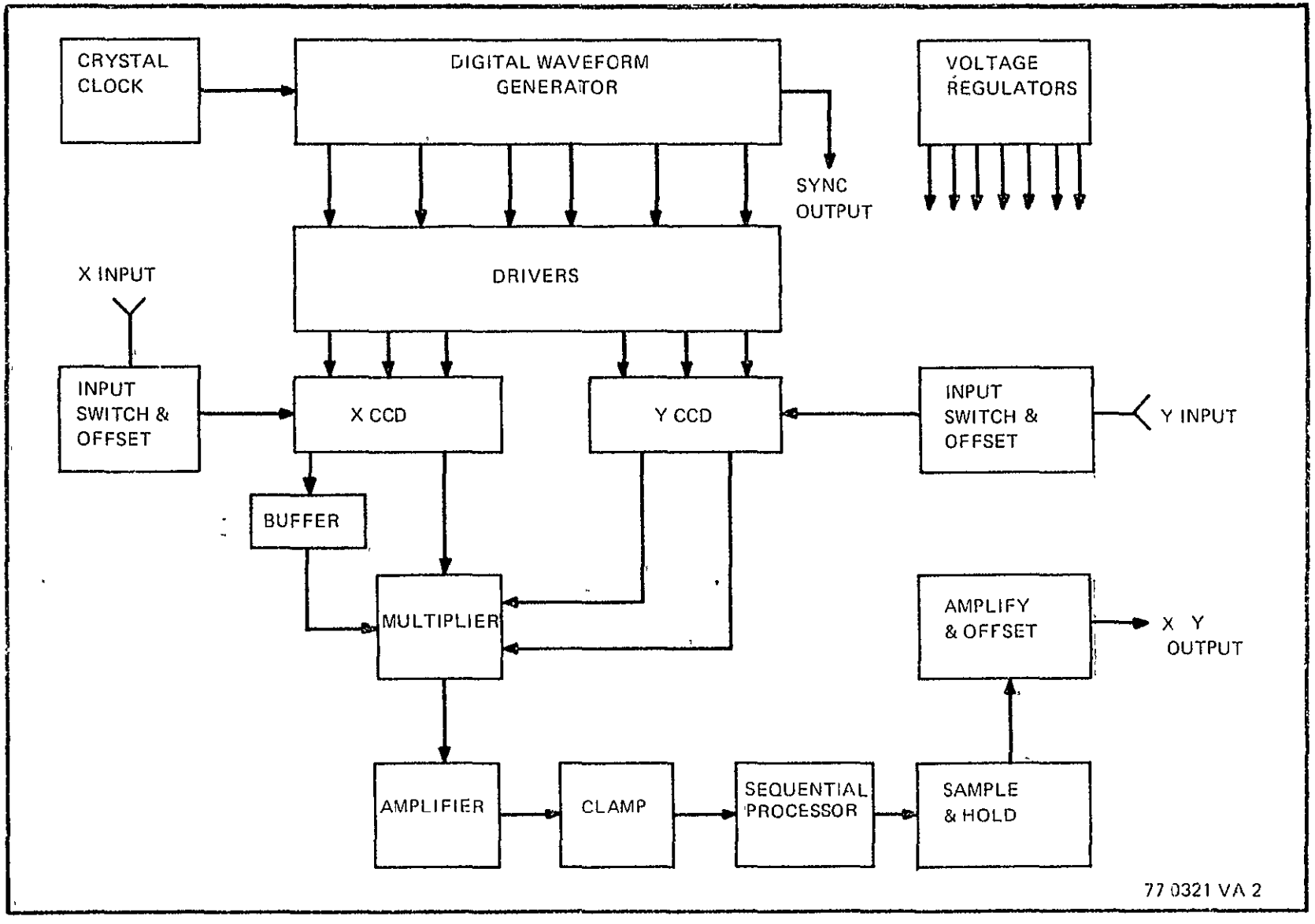


Figure 36 Sequential Multiply Exerciser

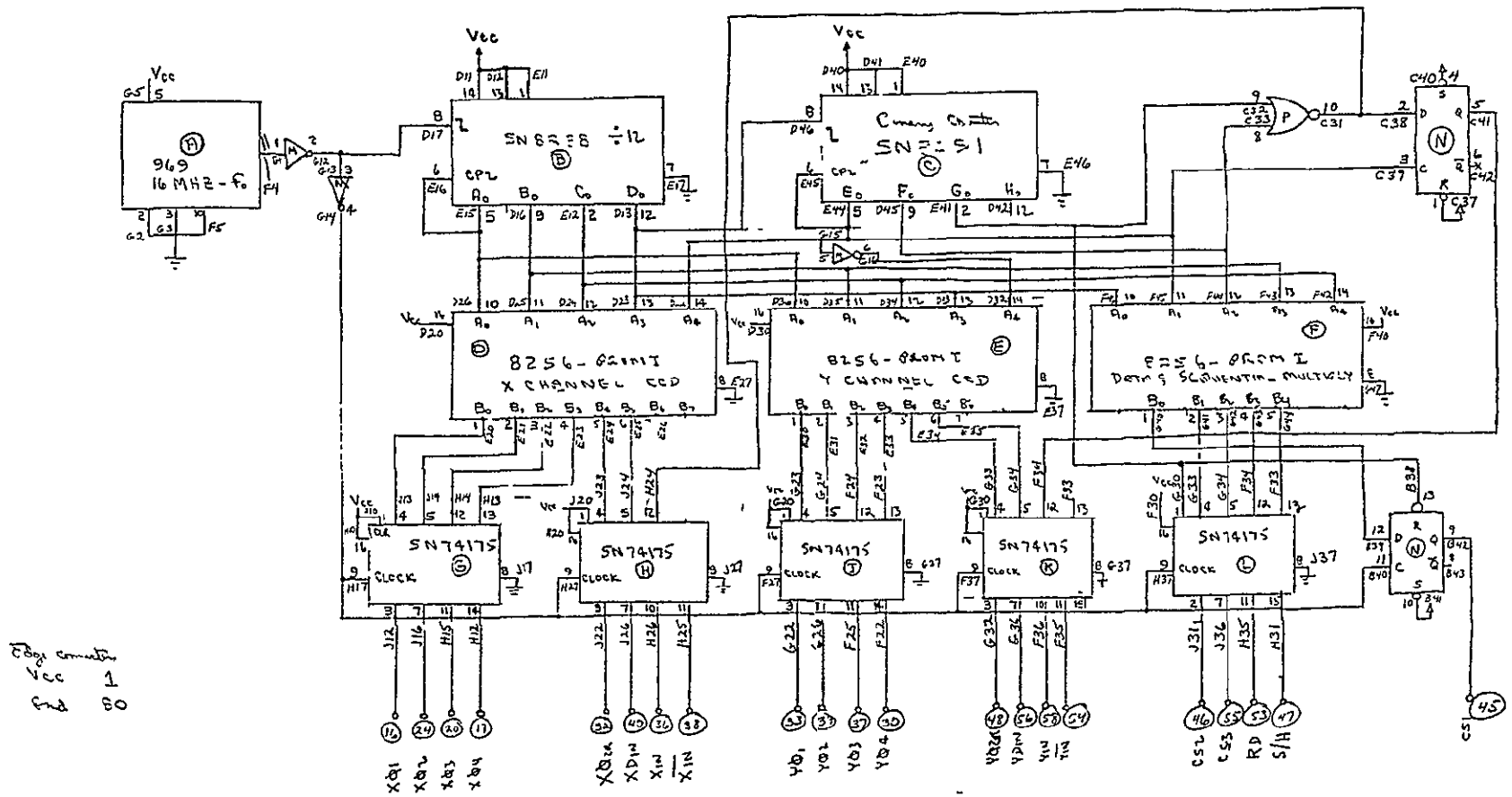


Figure 37. Sequential Multiply Exerciser Digital Board.

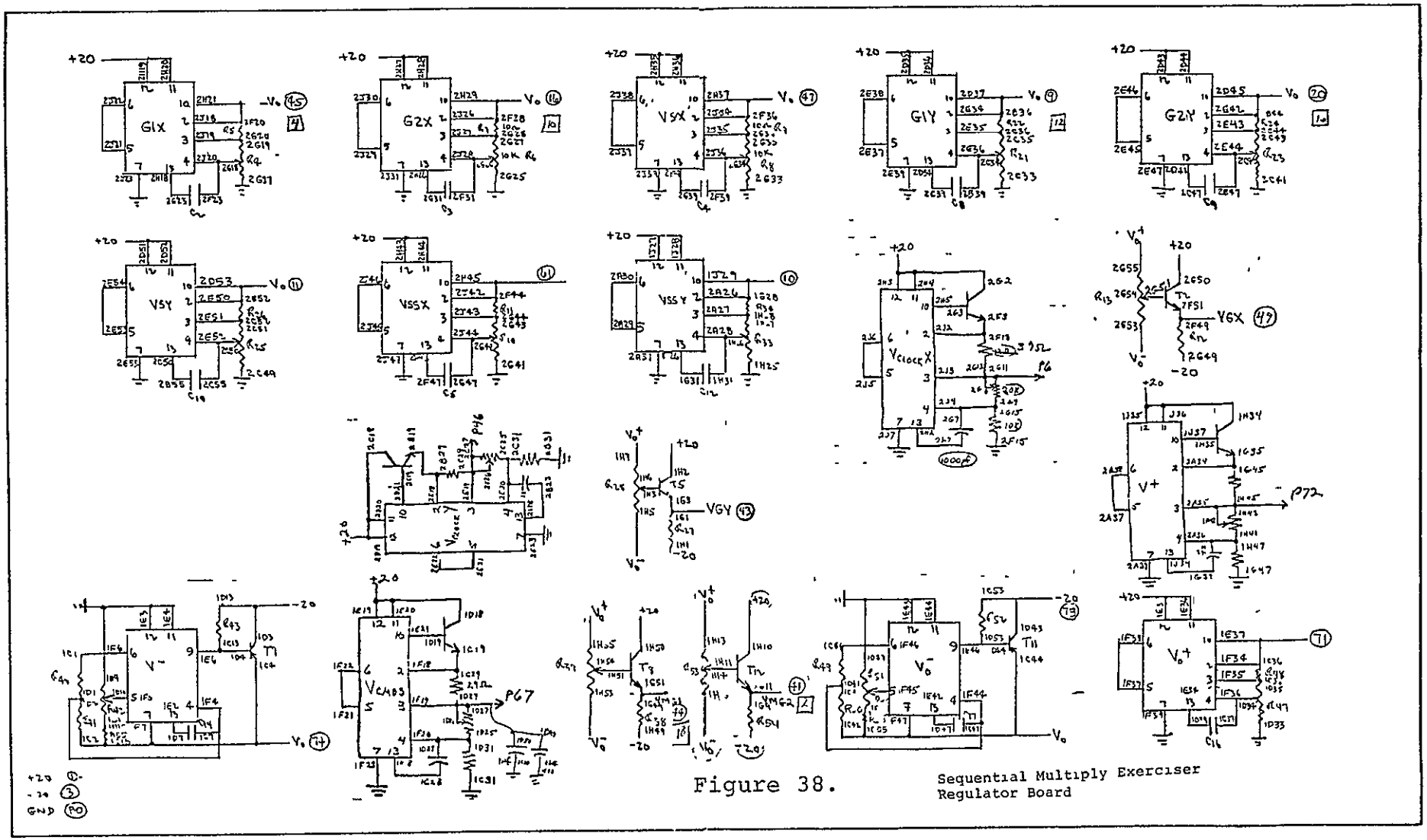
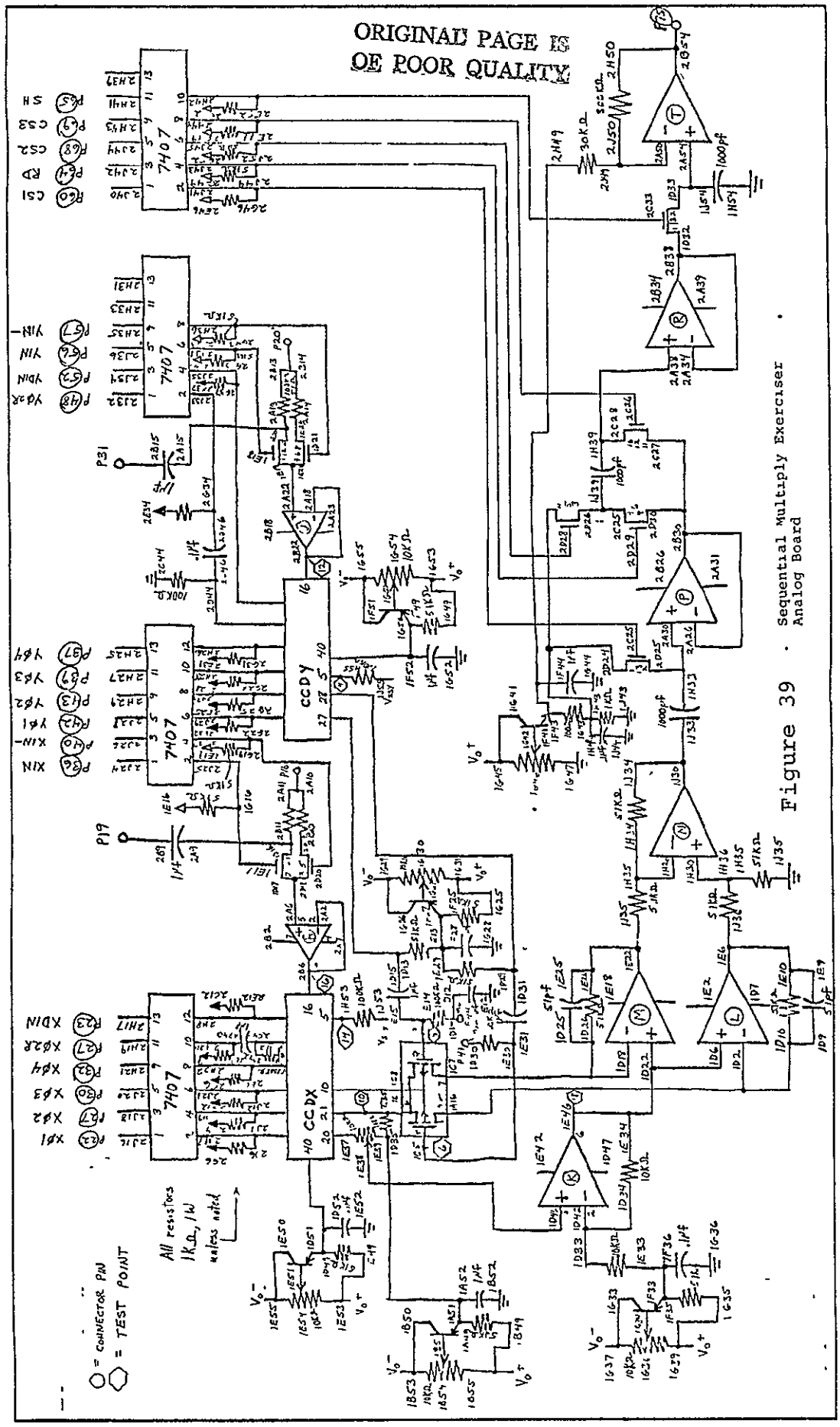


Figure 38. Sequential Multiply Exerciser Regulator Board


ORIGINAL PAGE IS
OF POOR QUALITY
Figure 39 · Sequential Multiply Exercise Analog Board

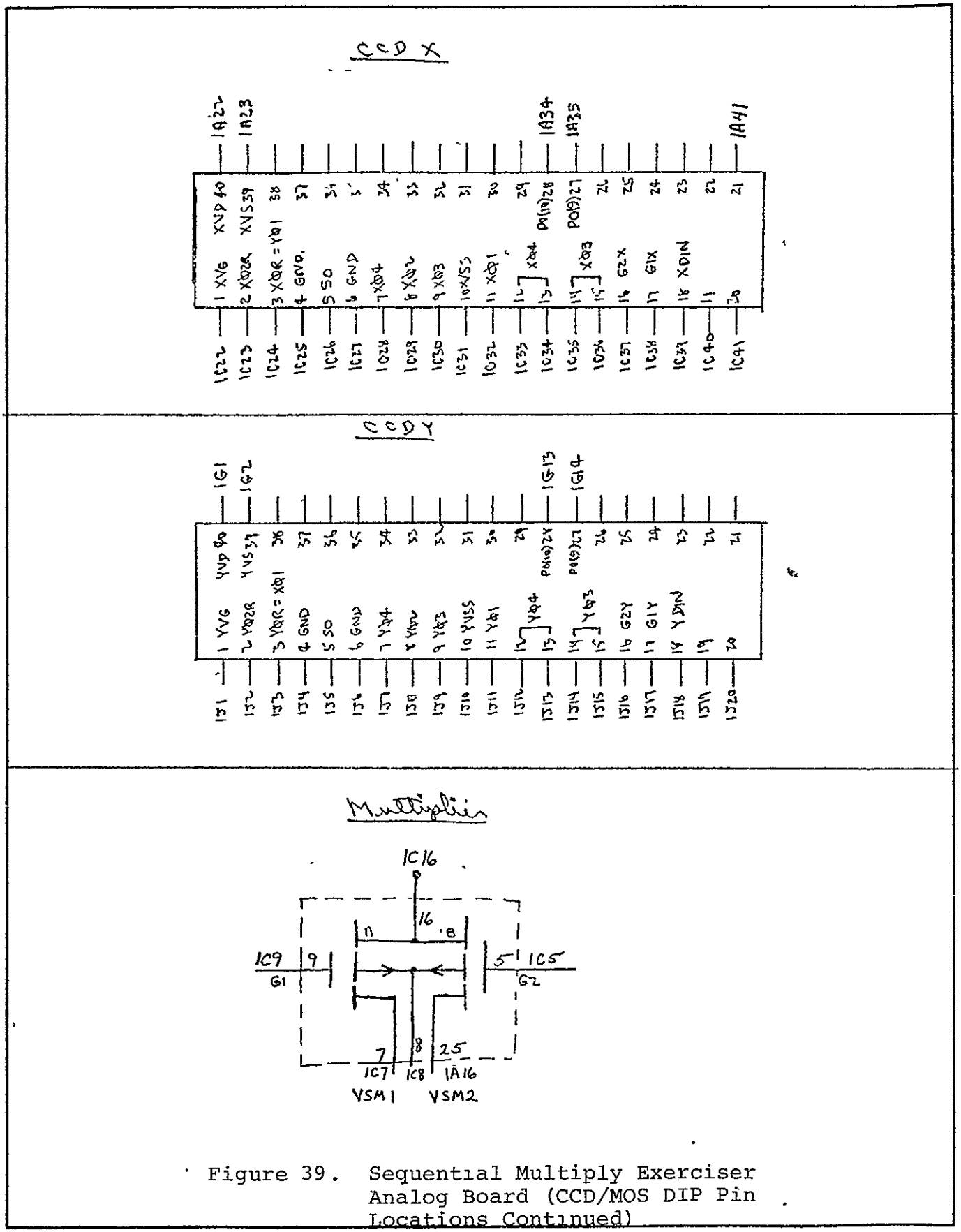


Figure 39. Sequential Multiply Exerciser Analog Board (CCD/MOS DIP Pin Locations Continued)

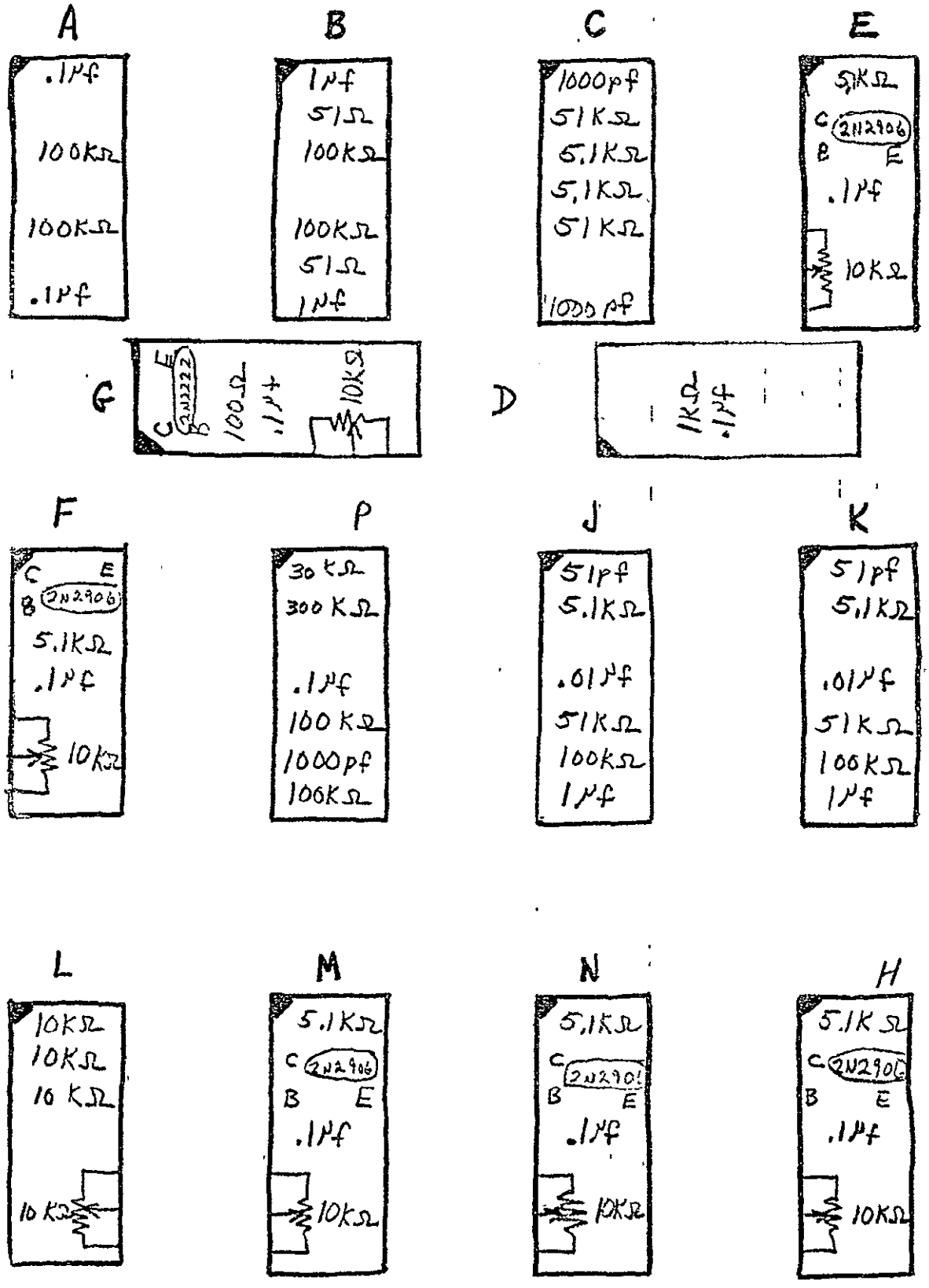


Figure 40. AP Discrete Components Carriers

MOS devices.

The regulator board of Figure 38 contains all of the regulators which provide all of the voltages used by the analog processor board shown in Figure 39. All of the regulators have a variable output voltage and are powered by the two main 20v supplies.

The analog processor (AP) board has the two CCD's and the sequential multiplier circuitry. This board also contains the drivers for the signals that come from the digital control board, with passive component carriers illustrated in Figure 40.

Each of the two inputs from the front panel to the multiplier is conditioned before it is fed into a CCD. Each input to the multiplier is passed through a capacitor to remove any DC level associated with it. Two CMOS switches are used to switch between the input and a reference bias for the CCD. This signal is buffered by an op amp and applied to one of the input gates of the CCD. Such initial processing simulates the input processor sections of Figures 31 through 34.

Two output taps from each CCD are used in performing the multiplication. One tap from the X channel CCD is used to provide a reference to the virtual-ground source buffer. This signal is conditioned by op amp K. The magnitude and offset of this signal can be changed by two pots. The gain and offset adjustments to facilitate simulation of both matched and mismatched quiescent points for the triode source and drain buffers. (Due to the Design of the CCD outputs, there are differences in gain and offset voltage between odd output taps and even output taps.) The output of op amp K is fed to the non-inverting inputs of op amps L and M which

provide virtual-ground nodes for the sources of the multiplying transistors in the manner shown in Figures 8 and 14-a. The signal from the other output tap of the X channel CCD is applied to the drains of the multiplying transistors. The signals from the Y channel CCD outputs are passed through an RC network to introduce a DC offset since "complementary" buffers for multiplier self-bias were not readily available. This provides the needed gate to source bias voltage for the multiplying transistors. The two current outputs of the multplier are fed to op amps L and M where the current is converted to a voltage. The outputs of these two op amps are feedthrough resistor networks to op amp N. This op amp is set up to eliminate the common mode signal due to the X channel reference and to amplify the difference between the outputs of L and M which represent the product signal.

Following op amp N are 2 op amps, 5 switches, and 3 capacitors which clamp, sample, and difference the signal and store the processed signal on C_9. At the beginning of the processing sequence, switch F13 is closed and the first product is stored on C_7. Switch F13 is opened and when the second product is available from op am N, the difference of the two products is at the output of op amp P. Switches F5 and F12 are closed and the difference of the first two products is stored on C_8. Switch F13 is closed again and the third product is stored on C_7. With switches F5 and F12 open, switch F6 is closed. Switch F13 is opened and when the final product is available at the output of op amp N, the difference of the second two products is at the output of op amp P and the result of the four products is at the output of op amp R. This result is the sum of the two differences. Switch G13 is closed and this result is stored

on capacitor C_9. This signal is amplified by factor of ten and offset back to ground by op amp T. This signal is available on a connector on the front panel of the exerciser.

The multiplier operates best with a drain to source bias of 0 volts. This voltage may be adjusted by the two pots that control the offset and gain of op amp K. The gate to source bias for the multiplier should be approximately -4 to -7 volts. This voltage can be changed by adjusting the V_{MG1} and V_{MG2} pots located on the regulator board. The voltage on the gates should be equal for matched transistors. For poorly matched transistors, this voltage may be adjusted to improve operation. The voltage used in the clamp/sample circuit should be set to 6 to 7 volts which is half of the voltage to the CMOS switches. The product signal is available on the X Y connector. A sync signal controlled by the internal logic is available to sync an oscilliscope to the internal sampling rate. One demonstration of the multiplier is using sine waves for inputs and observing the sum and difference frequencies at the output. Good results may be obtained by using a sine wave of 1.5v p-p @200 Hz on the X input and 2v p-p @ 1300 Hz on the Y input. The effective sampling frequency of the multiplier is approximately 10 KHz so input frequencies whose sum is less than 5KHz should be used to avoid aliasing problems. The input signals mentioned are only examples of typical frequencies and amplitudes for this particular hybrid model of the sequential multiplier, due primarily to the electromechanical construction and not limitations from the CCD/MOS circuits used.

7.3 A 16-Point-Correlator Hybrid Feasibility Demonstrator

The objective of the second demonstrator equipment is to model as accurately as practical in hybrid fashion the most attractive "Sum of Products" device based on the results of all the preceding theoretical and experimental investigations, with the constraint that the model be available in approximately four months for test and evaluation during the summer quarter of 1977. The hybrid approach not only permits observation (by monitoring with a scope probe) of every node within the "Sum of Products" device model, but also allows slight extra flexibility in component selection. Furthermore, even minimal monolithic integration of a complete "Sum of Products" device would have required substantially more resources than available for the hybrid model. This situation led to the following rationale and critical design decision concerning the hybrid model.

A. Analog Delay Lines With Independent Nondestructive Readout

The previous model of the sequential multiply operator had featured Westinghouse CCD's of the serial in/parallel out configuration with integrated emitter-follower buffers. These 20-tap devices functioned best with fairly complex clock waveforms and initially suffered from a symmetry-induced, odd-even fixed pattern. Since more than ten uniform taps were needed, a commercially-available 32-tap tetrode-gate bucket-brigade device was selected for the analog delay line, so as to permit comparison of BBD performance with that of CCD's in view of the potential for simpler fabrication, operation, and user interface.

B. Multiplying Elements

Even though the very lightly doped CMOS-pentode difference of squares multiplier appears most attractive; such CMOS arrays are not available either commercially or internally without the need for some mask set and/or fabrication process development, thereby forbidding their use in the allowed time period. The next most attractive scheme is the doubly balanced MOSFET triode multiplier that needs a nominally identical pair of MOSFET's. Here, fabrication of such arrays internally promised to give the desired matched pairs in the allotted time while commercial suppliers asked for much longer delivery times to achieve the target matching. Indeed, when measured at their anticipated quiescent operating points, many of the Westinghouse MOSFET pairs matched to within one percent for "resistance" as measured on transistor curve tracers.

C. Buffers

The MOSFET arrays of the proper type and size (adequately large relative to the multiplier MOSFET pairs) were readily available commercially and used throughout the hybrid model.

D. Sequential Multiply Operator

Even though existing Westinghouse CCD's have sufficient flexibility to permit a hybrid model of the monolithic implementation of the sequential multiply operation, a high probability of success in the limited time allocation dictated continued use of the hybrid

technique of the first demonstrator because of uncertainty in "debugging" the model of the monolithic sequential operator (not previously executed experimentally).

E. Differential Current to Voltage Readout (viz. CSRO) Circuit

Strict adherence to the circuit "recipe" given in Figures 15-17 suggests the use of three more transistors per multiplier comparable in conductance to those in the source-drain buffers plus other smaller MOSFETS. Thus at least sixteen more "DIPS" would have to be added to an already large and crowded hybrid model circuit card. Considerable experience with the bipolar version of the CSRO circuit as well as adequate current handling capability with much fewer "DIPS" dictated the use of the bipolar version of this subcircuit.

The preceding critical design decisions were then incorporated into a block diagram essentially identical to Figure 36, except the single multiplier was replaced by an array of 16 multipliers. The circuits and related wiring details are presented in their entirety in the Appendix.

7.4 Published Performance Data

A partially integrated device[2] with 32 singly-balanced triode pairs was operated at a sampling rate of 100kHz with sinusoidal inputs of $f_D \triangleq 6$ kHz and $f_G \triangleq 7$ kHz. The array was operator biased using a spectrum analyzer to simultaneously, minimize both input feedthroughs as well as the harmonic distortion. For the array

operation, the amplitude of the undesired Fourier components fell in the range of 30 to 40 dB below the difference frequency. Adjusting the array data to reflect the average performance per multiplier gives rejections of 10 to 20 dB or equivalently

$$\psi \approx \Gamma_d \approx 6$$

The triode gate bias was approximately 2.5 to 4.5 volts. The gate signal could not be changed without degrading either ψ or Γ_d, resulting in $\zeta = 1$ to give an estimated array nonuniformity of $\Delta V_T \sim 89$ to 160 mvolts, which agrees with typical MOS array results and supports the claim of equation (54). Furthermore, these results strengthen the questions: Can CTD/MOS triode multiplierarrays be fabricated to give better performance than the marginal values cited above? If so, what performance and voltage or power levels can be expected?

In publications[3] by Westinghouse investigators, more data was presented on the problem areas of the basic multiplier building block with emphasis on a serial (or common) technique external to the parallel array, which could relieve at least one of the severe restrictions implicit in equation (54). Thus, the sequential multiply technique relies on four constituent product currents for each four quadrant multiply which are generated with the same set of MOSFET devices sequentially in time. When these constituent product currents are combined algebraically, the effects of the nonuniform thresholds nominally cancel completely, thereby virtually eliminating the requirement on input feedthrough rejection, ψ, as well as reducing drain harmonic distortion (as shown in equations 40 through 45). Other schemes, such as the doubly-balanced technique already described, also help ease the restriction on harmonic distortion rejection, Γ_d.

Results of the Westinghouse developments are illustrated in Figures 41 through 43. Figure 41 shows the spectrum from a singly-balanced triode pair before sequential processing. This is the result expected for each singly-balanced triode pair, on the average, before parallel summing and sequential processing (the latter, to cancel effects of threshold nonuniformities and reduce input feedthrough). Note here, all published existing partially integrated devices[2,4] are equivalent to the parallel summation of a certain number of singly balanced triode pairs. Furthermore, in keeping with CCD compatibility objectives, two similar but not matched MOSFET triodes from an earlier CCD chip test pattern were used to generate the results of Figure 41 with the following optimal biases giving the best drain input feedthrough rejection: $Y_o=V_{GS}=4V.$, V_{SB}= Source Body Bias = 11.8V, V_{DS}= 51mV, ΔV_G= 142mV, x=y=200mV (pp), and y could not be changed without

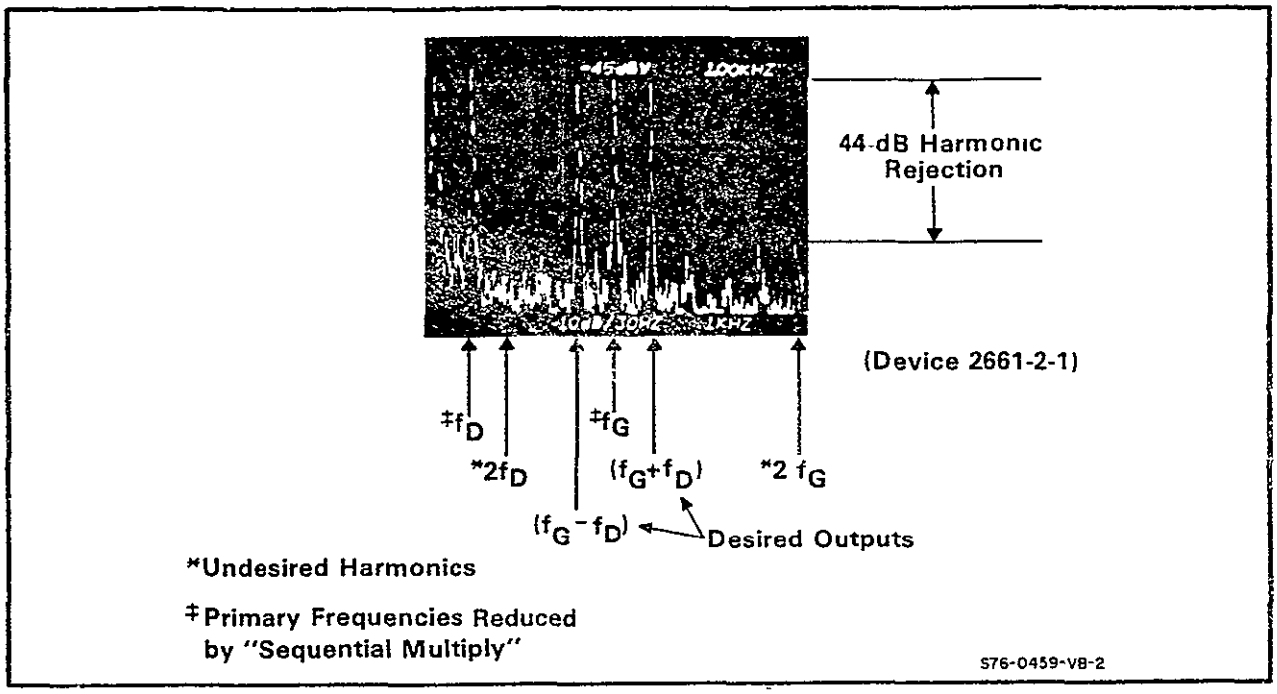


Figure 41 Spectrum from a Single-Balanced Triode Pair Before Sequential Processing

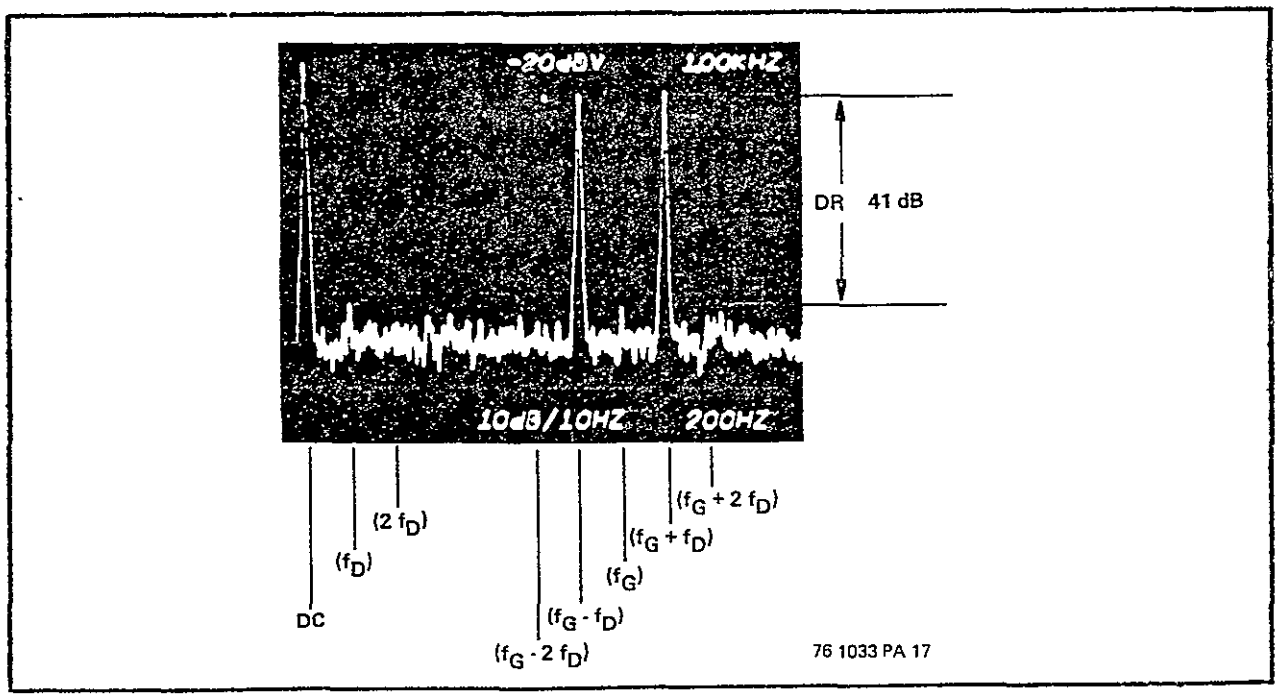


Figure 42 Single Multiplier Output Spectra After Sequential Processing (High Resolution Frequency Scan)

degrading the values indicated in the photo by $\psi \simeq 0.8$ for the drain input feedthrough rejection and of $\Gamma_d \simeq 150$ for the harmonic rejection.

Despite the less than ideal simulation of nominally-matched, CCD-compatible triodes, when similar MOSFET doublets were used in the published hybrid model[3], the results shown in Figures 42 and 43 were obtained. In the hybrid model the previously described self-bias scheme was used rather than the selected bias adjustment used for Figure 41. Due to the nonoptimum biases, the effective array drain input feedthrough rejection was about -11 to -17 dB for a ψ of approximately 0.2. Thus, from a rather poor starting point, Figures 42 and 43 show the sequential processor achieved a final input feedthrough rejection of 41 dB for a total compensation or cancellation of threshold nonuniformities of nearly 58 dB., by means of a hybrid sequential processor mounted on conventional wire-wrap boards, and implemented primarily with single chip monolithic bipolar op amps and complementary MOST switches frequently used for special purpose CMOS digital logic. Furthermore, the same data just cited for the output prior to sequential processing also shows a drain harmonic rejection of only 30dB in contrast to the photo of Figures 42 and 43 indicating 41 dB after sequential processing. Hence, the sequential multiply operation provides an additional 10-dB drain harmonic rejection not present in the triode pair by itself.

Even in its initial hybrid implementation, the sequential multiply operation has been shown to contribute up to 58-dB additional input feedthrough rejection and up to 10-dB additional drain harmonic

rejection. Due to expected improvements in common-mode rejection, sample and hold retention, and noise immunity, these sequential processor enhancement factors are likely to be larger for a monolithic implementation. Furthermore, Table 4 suggests the use of a doubly-balanced triode provides another 10-dB of gate harmonic rejection. These improvements in performance may readily be incorporated into the equations (54) to nominally correct them from a singly-balanced triode without sequential processing to the case of a doubly-balanced triode using the sequential multiply operator with the projections listed in Table 3.

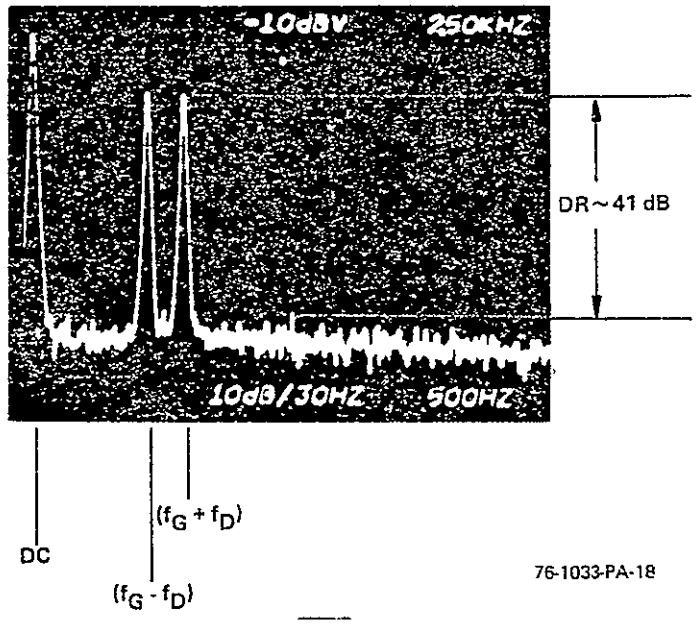


Figure 43 Single Multiplier Output Spectra After Sequential Processing (Extended Frequency Scan)

8 ADDITIONAL FACETS OF THE ANALOG-ANALOG CORRELATOR

Some aspects of analog-analog correlators are important when the devices are used to generate convolution/correlation functions, such as data processing speed or the numerical count of multipliers; while others are important for analog matrix arithmetic applications, such as erroneous "fixed pattern" contributions, the adverse affects of which may be diminished for convolution/correlation function applications by special operational modes. This section describes these additional facets of CTD analog correlators.

8.1 Fixed Pattern Noise/Errors

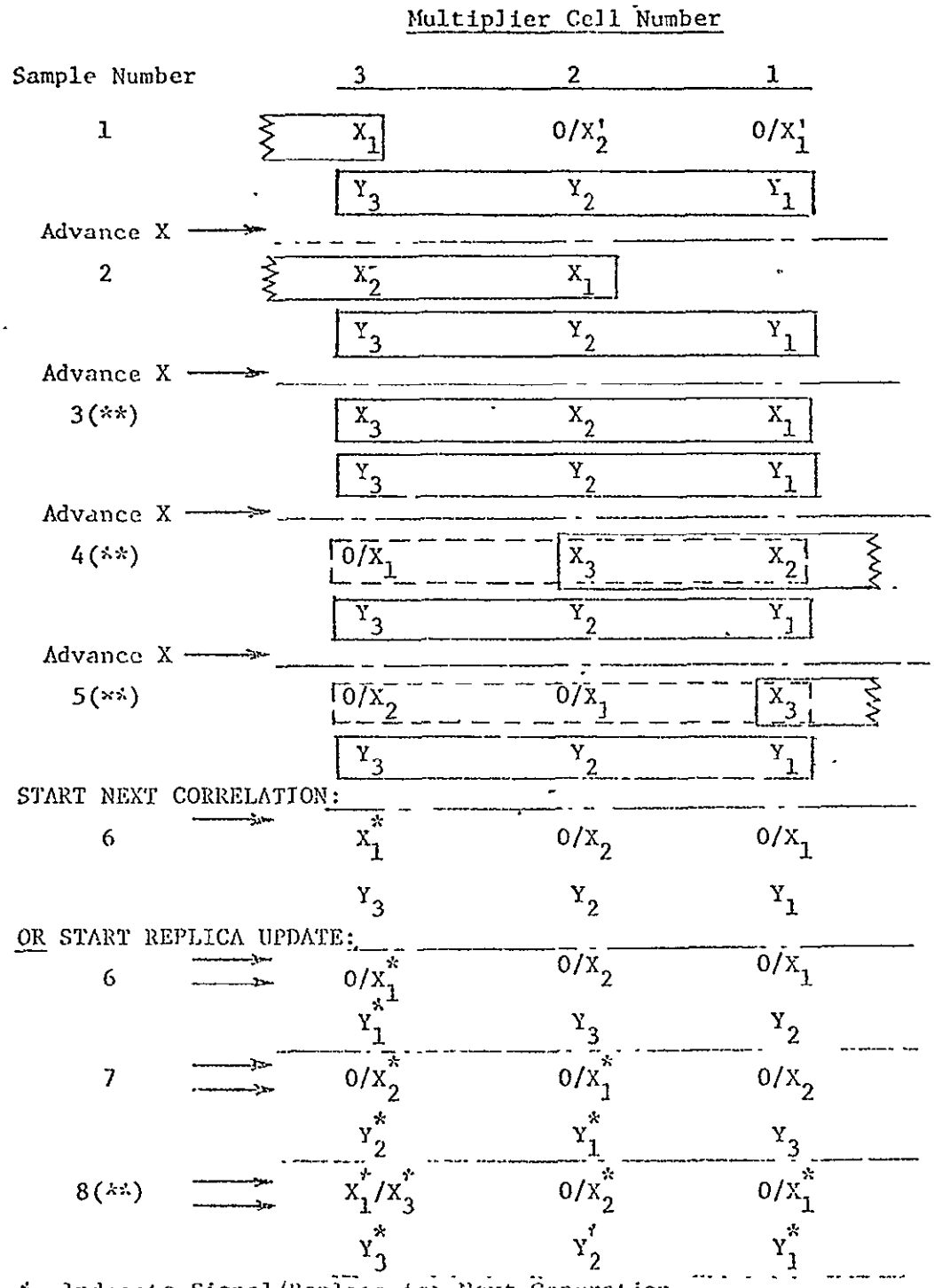
In most analog signal processing devices, the parallel or simultaneous performance of any function on NOMINALLY identical device elements, with subsequent combination or serial readout, often gives slightly different results from one device to the next due to spatial nonuniformities. For the analog correlator, such nonuniformities show themselves in two distinct ways: Varying threshold or flat-band voltages across an array; AND nonuniform "geometric" parameters which involve the local effective widths, lengths, and thicknesses as well as the effective charge mobility at each spatial location within the array. The problem of nonuniform thresholds is best overcome by the sequential multiply operation whereby constituent computations of the true analog multiply are done serially on the same device element (with subsequent combination) which effectively cancels any influence by the threshold voltage on the final result. The sequential multiply technique, however, has no effect on the so-called "geometric" nonuniformities. Consequently, in this section, we analyze the effects of these "geometric" nonuniformities on the performance of the correlator.

8.1.1 Inpulse Response and Frequency Spectra of Nonuniformities (Or Fixed Patterns)

The data flow architecture and operating sequences of a few more attractive schemes are illustrated in Figures 44,45, and 46 The architecture of Figure 44 is basically identical to that discussed previously: where a multiplier is associated with one pair of analog delay stages for EACH channel, wherein one of said pair of stages being the nondestructive readout type. This architecture is most closely associated with the operating scheme in which a correlation or convolution function is generated by holding the set of multiplicative weights effectively stationary in their respective analog shift register while the unknown signal slides by the prescribed multiplicative weight pattern. In Figures 45 and 46, the correlation function is generated while both analog shift registers uniformly propagate their analog data forward. But now, the analog shift register of one channel has twice as many stages as the other channel, thereby resulting in a data propagation rate (passing by the multiplier cells) of only one-half the rate of the other channel. This gives the effect of data in the singly-sampled register "sliding" by the data in the doubly-sampled register, even though both are advancing with the same dwell time per stage.

In summary, in the scheme of Figure 44 the set of multiplicative weights appears imbedded in the spatial array during generation of the correlation function. Thus, if the relative nonuniformity of the k^{th} cell is ε_k; the error contribution for the k^{th} cell is given by $\varepsilon_k Y_k$, which remains unchanged for the complete correlation function. On the other hand, the techniques of Figures 45 and 46

Figure 44 REAL TIME CCD CORRELATION USING SEQUENTIAL MULTIPLIERS WITH SINGLE CCD ADVANCE (WITH STATIONARY WEIGHTS)

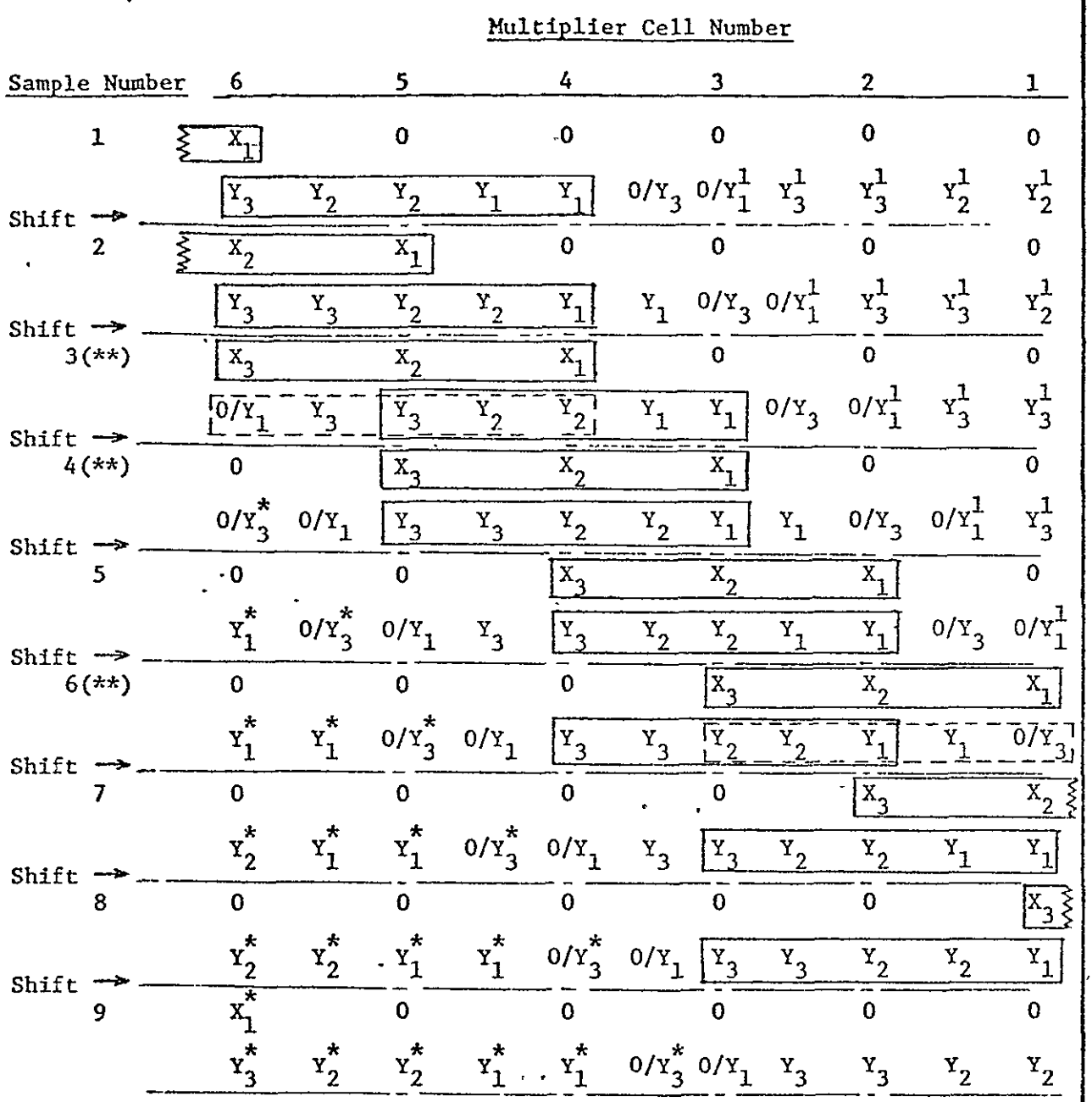


* Indicate Signal/Replica for Next Generation

X'_i are Previous Signal

(**) Outputs at these times give the DELTIC, RING, or CYCLIC correlation, if the X values below the slash gives conventional correlation.

Figure 45 REAL TIME CCD CORRELATION USING SEQUENTIAL MULTIPLIERS FOR BATCH PROCESSING OF SIGNALS WITH DUAL UNIFORM SHIFTING

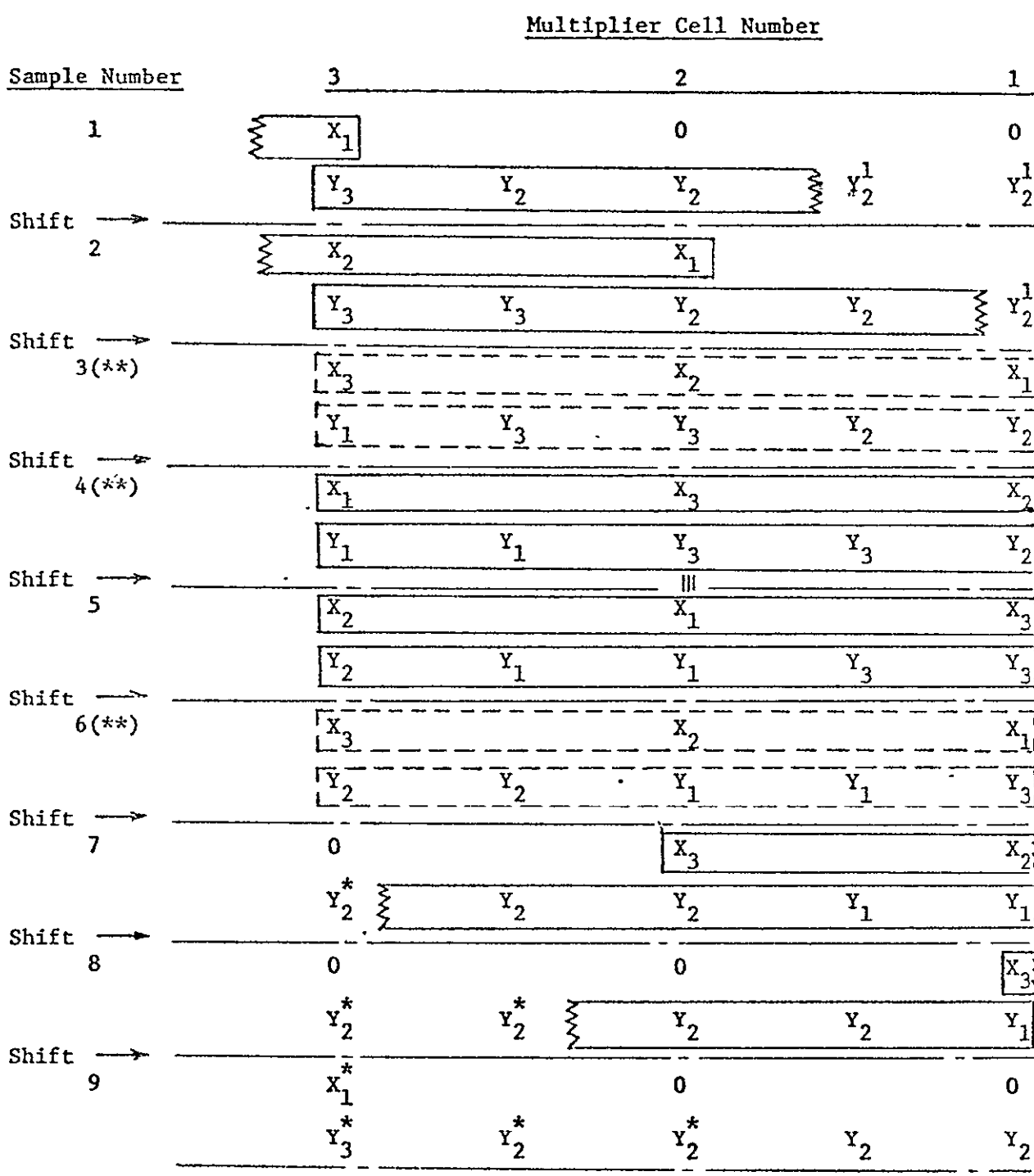


* Indicates Signal/Replica for Next Correlation

Y_J^1 are Previous Correlation Replica

(**) Outputs at these times give the DELTIC, RING, or CYCLIC correlation, if the Y values below the slash are used. Use of zeroes above the slash gives conventional correlation

Figure 46 REAL TIME CCD CORRELATION USING SEQUENTIAL MULTIPLIERS FOR PROCESSING OF REPETITIVE SIGNALS WITH DUAL UNIFORM SHIFTING



* Indicates Signal/Replica for Next Correlation.

Y_J^1 are Previous Correlation Replica.

(**) Outputs at these times give the DELTIC, RING, or CYCLIC correlation; they can be passed over for the conventional correlation.

move or convolve the multiplicative weights relative to the spatial location which gives a slightly different spectral treatment to the fixed pattern noise.

To simplify the derivation of fixed pattern noise, consider first the impulse response of the device when a unit amplitude impulse propagates through the X-channel CTD. In the ideal case, in the absence of nonuniformities, the impulse response may readily be written as:

$$h(t) = \sum_{K=1}^{N} y_K \, \delta\left[t-(N+1-K)T_c\right] = \sum_{K=1}^{N} y\left[t-(N+1-K)T_c\right] \qquad (72)$$

where T_c = clock time, f_{NYQ} = Nyquist Sampling limit = $1/2T_c$, $\tau = (N-1)T_c$ = overall shift register delay, $f_o = 1/\tau$ = associated fundamental frequency of shift register. If the N discrete sample values for the Y-channel are regarded as the values of a repetitive waveform of period τ which is sampled at the rate $f_c = 1/T_c$, the following formulas are obtained (where the index and discrete samples are module N):

$$h(t) = \sum_{K=-\infty}^{+\infty} (y_K) \cdot \delta\left[t - \frac{N+1-K}{N-1}\tau\right] = \sum_{K=-\infty}^{+\infty} y\left[t - \frac{N+1-K}{N-1}\tau\right], \qquad (73)$$

$$Y_n = f_o \int_0^{\tau} y(t) \cdot \exp\left(-2\pi i \frac{nt}{\tau}\right) dt = f_o \int_0^{\tau} y(t) \cdot \exp\left(-2\pi i n f_o t\right) dt,$$

so that $$Y_n = f_o \int_0^{\tau} \sum_{K=-\infty}^{+\infty} y_K \, \delta\left[t - \frac{N+1-K}{N-1}\tau\right] \exp\left(-2\pi i n f_o t\right) dt \qquad \text{or}$$

$$Y_n = f_o \sum_{K=1}^{N} y_K \exp\left(-2\pi i n \frac{N+1-K}{N-1}\right) \qquad (74),$$

for a final result of

$$Y(f) = f_c \sum_{n=-\infty}^{+\infty} \sum_{K=1}^{N} y_K \cdot \exp\left(-2\pi i n \frac{N+1-K}{N-1}\right) \cdot \delta\left(f - n f_o\right). \qquad (75)$$

We may now consider the more realistic case of array non-uniformities, ϵ_k, for a device operated as shown in Figure 44 with stationary weights to give an ERROR impulse response function:

$$h_\epsilon(t) = \sum_{K=1}^{N} \epsilon_K y_K \delta\left[t-(N+1-K)T_c\right] \qquad (76)$$

with an associated spectrum of

$$H_\epsilon(f) = f_o \sum_{h=-\infty}^{+\infty} \sum_{K=1}^{N} \epsilon_K y_K \exp\left(-2\pi i \frac{N+1-K}{N-1}\right) \delta\left(f-nf_o\right) \qquad (77)$$

For the operating modes of Figures 45 and 46 the error impulse response function is written as:

$$\phi_\epsilon(t) = \sum_{K=1}^{N} \sum_{l=-\infty}^{+\infty} \epsilon_K y_{l-K} \delta\left(t-lT_c\right) \qquad (78)$$

so that

$$\Phi_{\epsilon/n} = f_o \int_0^\tau \phi_\epsilon(t) \exp\left(-2\pi i n f_o t\right) dt = f_o \sum_{K=1}^{N} \sum_{l=1}^{N} \epsilon_K y_{l-K} \exp\left(-2\pi i \frac{n(l-K)}{N-1}\right) \qquad (79)$$

Since $$\Phi_\epsilon(f) = \sum_{n=-\infty}^{\infty} \Phi_{\epsilon/n} \delta(f-nf_o) \qquad (80)$$

, substitution yields

$$\Phi_\epsilon(f) = f_o \sum_{n=-\infty}^{+\infty} \left\{\delta(f-nf_o)\right\}\left\{\sum_{K=1}^{N} \epsilon_K \exp\left(-2\pi i \frac{nK}{N-1}\right)\right\}\left\{\sum_{l=1}^{N} y_{l-K} \exp\left(-2\pi i \frac{n(l-K)}{N-1}\right)\right\} \qquad (81)$$

Such a result is entirely expected: For operation with non-stationary weights, where they convolve in the time domain through all allowed spatial positions, the frequency domain function is related to the direct product of the individual frequency domain functions: The second is the frequency spectrum of the selected weights; while the first is the frequency spectrum of the geometric, fixed pattern errors.

8.1.2 Statistical Evaluation for Devices

For formula (81) in the case of the nonstationary weights, we see the spectra of the filter and of the fixed pattern errors

multiply together. This is equivalent to applying the desired filter not only to the input signal but the fixed pattern errors, too. But indeed, there is a more important side effect of this behavior: The geometric fixed pattern errors are probablistic, being described by some multivariate probability density function, $p(\epsilon_i, \epsilon_j)$, which is used to predict such experimentally measured parameters as:

1) mean error = $\bar{\epsilon}_k = E(\epsilon_k)$ (82)

2) RMS error = $\left(\overline{\epsilon_k^2}\right)^{1/2} = \left[E(\epsilon_k^2)\right]^{1/2}$ (83)

3) Error variance = $\sigma_\epsilon^2 = E\left|(\epsilon_k - \bar{\epsilon}_k)^2\right| = (\bar{\epsilon}_k^2) - (\bar{\epsilon}_k)^2$ (84)

We may now apply such a statistical evaluation to our proceeding error analysis, incorporating a time domain average over a block of data of duration equal to the characteristic repetition time, NT_c. We designate $\langle f(t) \rangle$ = Time average of $f(t)$ over $0 \leq t \leq NT_c$.

First we consider the case of the stationary weights:

$$\langle h_\epsilon(t) \rangle = \sum_{K=1}^{N} \epsilon_K y_K \cdot \quad \text{Thus,} \quad E\left(\langle h_\epsilon(t) \rangle\right) = \sum_{K=1}^{N} \bar{\epsilon}_K y_K \; ;$$

or

$$E^2\left(\langle h_\epsilon(t) \rangle\right) = \sum_{K=1}^{N} \sum_{l=1}^{N} \bar{\epsilon}_K \bar{\epsilon}_l y_K y_l \cdot$$

and

$$\langle h_\epsilon(t) \rangle = N^{-1} \sum_{K=1}^{N} \epsilon_K y_K \int_0^{NT_c} \delta\left[t - (N+1-K)T_c\right] dt \; ,$$

Since $\left(\langle h_\epsilon(t) \rangle\right)^2 = \sum_{K=1}^{N} \sum_{l=1}^{N} \epsilon_K \epsilon_l y_K y_l \; ,$ we find

$$E\left[\left(\langle h_\epsilon(t) \rangle\right)^2\right] = \sum_{K=1}^{N} \sum_{l=1}^{N} \overline{\epsilon_K \epsilon_l} \, y_K y_l \; ;$$ which gives the variance:

$$\mathrm{Var}\left(\langle h_\epsilon(t)\rangle\right) = \sum_{K=1}^{N}\sum_{l=1}^{N} y_K y_l \left[\overline{\epsilon_K \epsilon_n} - \bar{\epsilon}_K \bar{\epsilon}_l\right]. \tag{86}$$

The impulse response of a filter with uniform weights (that is, h_ε^1 has $Y_K \equiv 1$ for all $1 \le k \le N$) gives an output dependent only on array nonuniformities:

$$\mathrm{Var}\left(\langle h_\epsilon^1(t)\rangle\right) = \sum_{K,l=1}^{N}\left(\overline{\epsilon_K \epsilon_l} - \bar{\epsilon}_K \bar{\epsilon}_l\right) \tag{87}$$

Further assumption that the fixed pattern errors are statistically independent between array spatial locations; that is,

we have $$\overline{\epsilon_K \epsilon_l} = \overline{\epsilon_K^2} \text{ for } l = K \text{ & } \overline{\epsilon_K \epsilon_l} = \bar{\epsilon}_K \bar{\epsilon}_l \text{ for } l \neq K, \tag{88}$$

$$\mathrm{Var}\left(\langle h_c^1(t)\rangle\right) = N \cdot \left[\mathrm{Var}(\epsilon_K)\right].$$

This actually follows directly, because $\langle h_\varepsilon^1(t)\rangle$ has become merely the sum of statistically independent variables, all having the same mean and variance.

In reality, of course, some of the factors causing array nonuniformities are not statistically independent random variables from one spatial position in the array to another; such as dielectric thickness and background/body doping which may vary gradually across a wafer. Consequently, such statistical dependence affects both variance or amplitude of the fixed pattern noise as well as the fine structural details of the spectra. For example, fabrication of a mask set incorporating some forms of mirror symmetry may result in an undesirable

"odd-even" pattern giving an extraordinarily large spectral component directly at the Nyquist sampling limit.

We may now consider the case of non-stationary weights: Because the multiplicative weights are convolved through all possible spatial locations within the array, we may extend the preceeding development for stationary weights by postulating an "effective" fixed pattern error:

$$\epsilon_K^*(t) = \sum_{l=1}^{N} \epsilon_{l-K}\, \delta(t - l T_c) \quad \text{for} \quad 0 \le t \le N T_c ,$$

directly resultant from the comparison of the formulas for $h_\varepsilon(t)$ and $\phi_\varepsilon(t)$. Following the same derivation as before yields:

$$\langle \epsilon_K^*(t) \rangle = N^{-1} \sum_{l=1}^{N} \epsilon_l$$

or

$$E^2\left[\langle \epsilon_K^*(t) \rangle\right] = N^{-2} \sum_{l=1}^{N}\sum_{m=1}^{N} \bar{\epsilon}_l\, \bar{\epsilon}_m .$$

Similarly

$$\left(\langle \epsilon_K^*(t) \rangle\right)^2 = N^{-2} \sum_{l=1}^{N}\sum_{m=1}^{N} \epsilon_l\, \epsilon_m \; ;$$

so that

$$E\left[\left(\langle \epsilon_K^*(t) \rangle\right)^2\right] = N^{-2} \sum_{l=1}^{N}\sum_{m=1}^{N} \overline{\epsilon_l\, \epsilon_m}$$

which yields the variance

$$\mathrm{Var}\left(\langle \epsilon_K^*(t) \rangle\right) = N^{-2}\left[\sum_{l=1}^{N}\sum_{m=1}^{N}\left(\overline{\epsilon_l\, \epsilon_m} - \bar{\epsilon}_l\, \bar{\epsilon}_m\right)\right] \qquad (89)$$

Again, statistically independent errors give the result

$$Var\left(\langle \epsilon_K^*(t) \rangle\right) = N^{-1}\left[Var\left(\epsilon_K\right)\right] \qquad (90)$$

Thus, the "effective" error variance from time averaging each multiplicative weight over all N spatial positions is reduced by the factor N compared to the case for stationary weights:

$$Var\left(\langle \varphi_\epsilon^{\,i}(t) \rangle\right) = N^{-1}\left[Var\left(\langle h_\epsilon^{\,i}(t) \right)\right] \qquad (91)$$

for statistically independent fixed pattern errors.

This improvement with non-stationary weights may be explained heuristically: The "effective" error is reduced by the probabilistic cancellation of the various independent random values with some increasing and some decreasing the desired multiplicative value.

8.1.3 Further Comparison: Stationary Versus Nonstationary Weights

The above discussion covers the multiplicative fixed pattern error noise, but other items are also affected by the selection of stationary versus nonstationary weights, such as errors due to nonuniform leakage, chip architecture (like the number of multiplier cells needed), and the times needed to compute the double-sided correlation functions indicated in Figures 44, 45 and 46 all of which are compared in Table 5.

Table 5: Comparison of "N-Point" Correlator Modes: Stationary Versus Nonstationary

ITEM	STATIONARY WEIGHTS		NONSTATIONARY WEIGHTS	
Multiplicative Fixed Pattern Noise	(Array Variance)~(N)•(Single-Point Variance)		(Array Variance)~(Single-Point Variance) Array averaging reduces this (error) noise.	
Non Uniform Leakage	Accumulation of leakage charge during correlation function shifts DC value of multiplicative weights.		Uniform shifting of weights eliminates nonuniform leakage and associated errors.	
Analog S/R Stages per Array Multiplier	One pair for each channel.		One pair for signal channel, Two pairs for multiplier/replica channel.	
Signal Process Type	Nonrepetitive* (Batch)	Repetitive (Cyclic)	Nonrepetitive* (Batch)	Repetitive (Cyclic)
No. of Multiplier Cells	N	N	2N	N
Associated Figure No.	1	1	2	3
No. of Signal Sample Intervals Needed for:				
New Signal Only	2N-1	2N-1	3N-1	2N
Full Update of Signal and Multipliers/Replica	3N-2	2N-1	3N-1	2N

*A double-sided correlation function (as indicated in Figures 44,45,46) has been assumed.

First, consider the effects of nonuniform leakage in the analog shift register which stores the set of multipliers. For the case of stationary weights as in Figure 44 the accumulation of nonuniform leakage charge during the computation time for the correlation function is indistinguishable from a change during that computation in the stored value of the multiplicative weights. On the other hand, Figures 45 and 46 feature uniform shifting of both analog shift registers so that leaky spots contribute equal charge quanta to all charge packets; thereby eliminating the nonuniform charges in multiplier values and the resultant errors. But this improved performance does not come without cost.

Comparison of Figures 45 and 46 with Figure 44 shows some of the extra elements needed to give the improved performance. Whereas, for the stationary weights mode, each multiplier in the physical array needs one pair of analog shift register stages for each channel (one stage for reference only, the other stage for "reference plus signal") the nonstationary weights mode requires that one of the channels incorporate two such pairs of stages per multiplier in one of the analog shift registers. Although the architecture is somewhat different, the analog sampling rates for both channels for either operational mode stay the same. That is, one channel stores double samples of the weights, for example, while the other channel stores single samples of the signal. Since the two analog delay channels are uniformly shifting at the same rate, the batch of signal samples "slides" by the batch of weights as in Figure 45 Furthermore, in this mode of operation, while the analog sampling of the signal is straightforward; providing double samples of the weights for shifting at the

same rate as the signal introduces a new and different analog input-interface situation.

Some additional differences are included in the lower part of Table 5. For conventional double-sided correlations of non-repetitive data (as in Figure 46), the use of nonstationary weights requires an array of 2N multipliers to perform an N-point correlation, in contrast to the other schemes which require only N multipliers. Also, more computation time (more shift register advances) is needed for the nonstationary weights scheme.

We may summarize the relative merits as follows: It is important to note that computations for analog matix arithmetic (involving specific sums of products) uniquely define the needed products, that is, a single exactly prescribed alignment of the components of the analog vectors. Thus analog matrix arithmetic applications do not allow the choice of using nonstationary weights versus stationary weights. The impulse responses for uniform weights, $h_{\varepsilon}^{1}(t)$ and $\phi_{\varepsilon}^{1}(t)$, however do serve as useful tools to measure the errors due to array nonuniformities and the extent of correlation of those nonuniformities, respectively. Applications involving complete correlation/convolution functions (i.e., time-sequential streams of output data points), in contrast to those for analog matrix arithmetic with a single output in time, have the option of using nonstationary weights to obtain reduced errors from fixed pattern nonuniformities in array element parameters (including leakage) at the expense of needing somewhat larger arrays and longer processing times. Hence this becomes an important consideration for the period of early development of a fully-integrated, monolithic implementation of an analog-analog

correlator: The architecture needed for the nonstationary weights scheme for computing correlation functions can easily be used in the stationary weights mode, but the converse is not true; thus suggesting that any developmental chip for demonstrating feasibility of monolithic implementation and featuring the architecture for nonstationary weights operation greatly facilitates actual comparison of the two schemes thereby broadening the spectrum of possible users.

8.2 Speed/Multiplicity Enhancement by Multiplexing

For various applications, either the number of multipliers required or the data processing rate or both may be so high that appreciable degradation of data occurs before the desired multiplication takes place due primarily to poor charge transfer efficiency (CTE). Even with extremely bad CTE, the signal attenuation per stage is so small that geometric pre-emphasis by means of tapering the size of the multiplying element larger, as the signal progresses through the delay line, is not feasible. Furthermore, even if a correlator chip based on floating gates and buried channel CCD were to give good error rejection and a large input dynamic range at very high speeds with large numbers of stages, new application areas most certainly would open with more demanding requirements. Consequently, techniques to multiply the effective speed and number of stages by means of multiplexing deserve some consideration from the outset, if for no other reason than to guarantee that multiplexing is not rendered impossible because of an accidental oversight.

The four-step sequential process lends itself naturally to either a 4:1 or 8:1 multiplexing ratio. A likely block diagram for

4:1 multiplexing of doubly-balanced triodes is illustrated in Figure 47 with emphasis on the clocking simplicity due to the symmetric nature of the sequential multiply. Each "quadrant" of the large composite chip is immediately recognized as the block diagram of Figure 32, including charge-coupled sequential processor with fully reconstructed output waveforms. Although all quadrants are computing at a quarter of the total data rate, they are phased 90^{o} relative to each other so that a new computation is added into the output at every quarter of the reduced clock rate, i.e., at exactly the total effective data rate. Thanks to the sample and hold output within each constituent subarray (quadrant), the passive output summation scheme illustrated in Figure 48 may be used. Difficulty with such a passive scheme (i.e., no active selective address switching, only pentode current addition) most likely would involve subarray output amplifier matching. Gain matching may be approached by using large dimensions for the MOSFET's. Threshold nonuniformities add to give a constant dc offset which can be removed by a final clamping or dc restoration if ac coupling is not allowed.

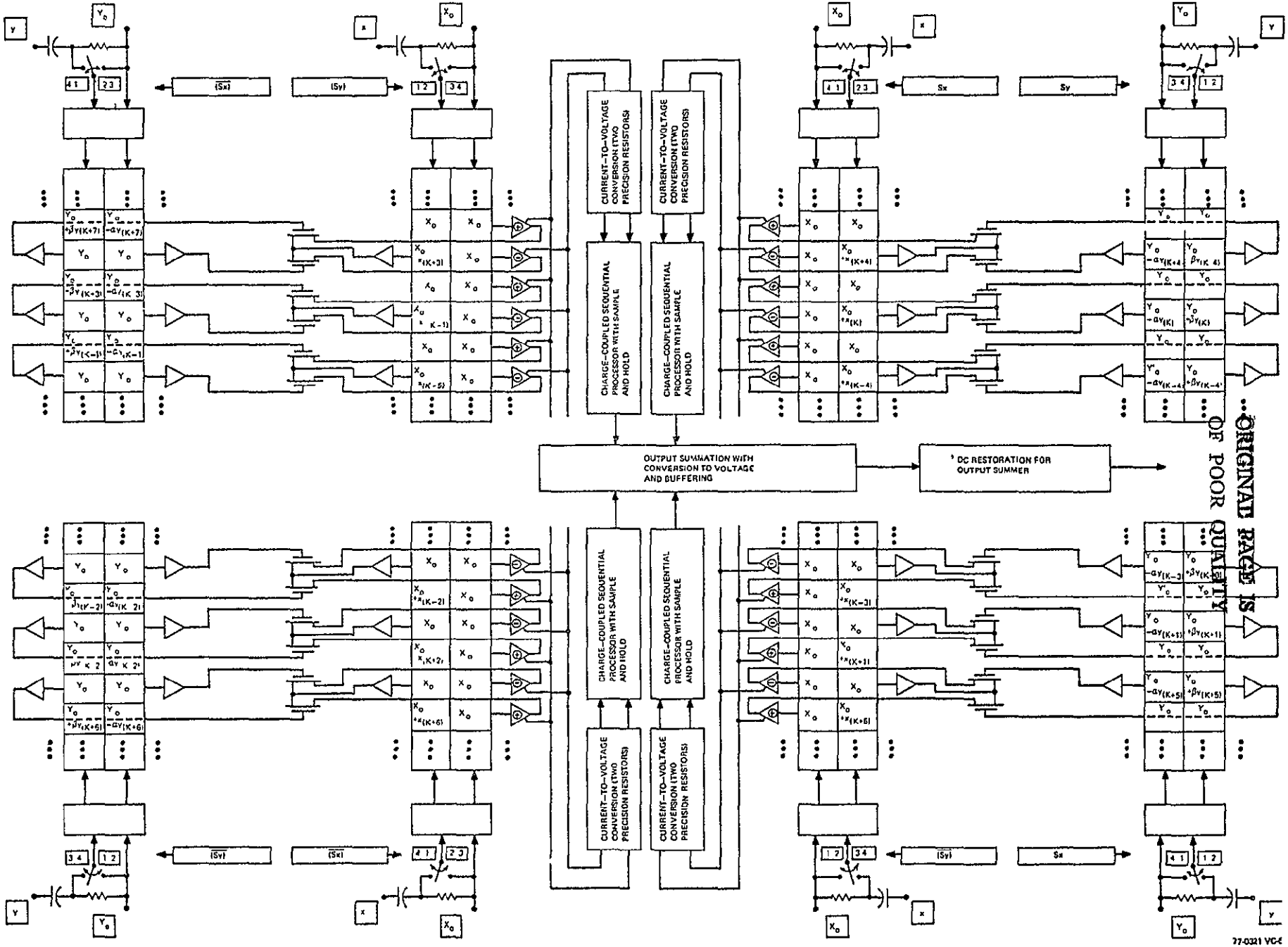


Figure 47. Multiplex of Doubly-Balanced Triode Multiplier Arrays

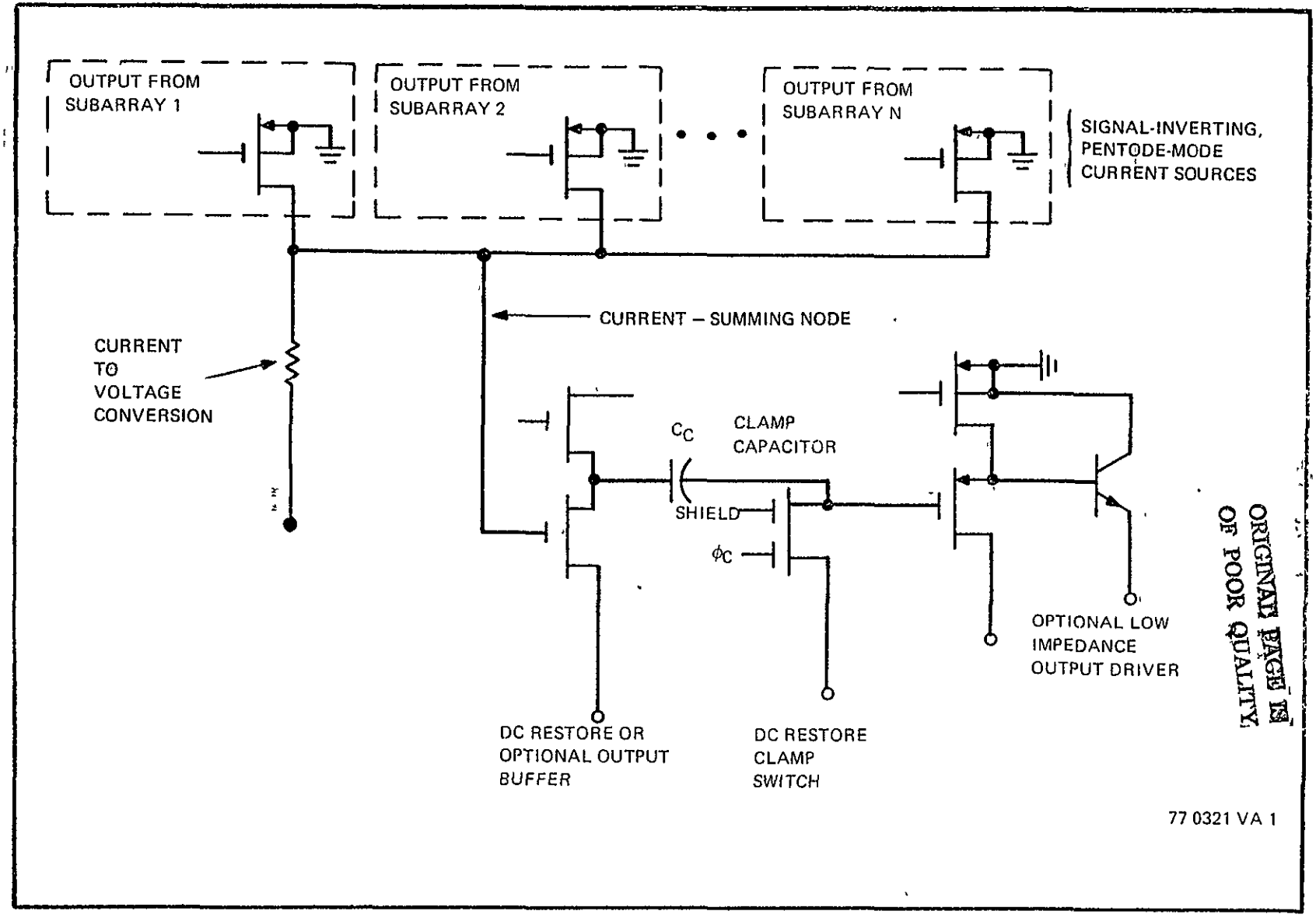


Figure 48 Output Summation of Demultiplexed Constituents

9) SUMMARY AND CONCLUSIONS

The information presented in the preceding sections describes almost every important aspect of analog-analog correlators or convolvers based on CTD's. An elementary investigation of various multiplying elements and their marriage with CTD analog delay lines was experimentally verified in both hybrid[3,5] and partially integrated[2,4] versions, all of which served very useful functions by demonstrating:

1) The successful marriage between CTD's and triode multipliers.

2) The need for elaborate routines for operator-controlled off-chip optimal biasing (via spectral analysis), thereby emphasizing the necessity for an on-chip self-bias technique.

3) Uncompensated-array error rejection limited by threshold nonuniformities to give a per multiplier input feedthrough rejection not exceeding 15dB.

4)Power levels of three to five milliwatts per buffer.

Since the difficulties highlighted by the last three items above had been anticipated from the outset, contract work was strongly focused on developing solutions to those problems as well as others related to making such devices attractive to users so as to achieve a larger potential market in accordance with the objectives presented in the introduction. As a direct consequence of the analog-analog correlator program, many more broadly applicable techniques have been developed and specialized to CTD correlators. A partial list of some of the more significant contributions follows:

1) The sequential multiply operation permits the joint operation of arrays of multipliers by providing detailed compensation for array threshold nonuniformities and cancellation for some harmonic distortion, too.

2) Relaxed fabrication uniformity tolerances for nominally matched circuit elements, because the objective of the nominal matching is merely to help ease the requirements on the serial subtraction steps in the sequential multiply operation.

3) The self-bias technique provides for the multiplying elements both the needed balanced and biased drives by means of complementary type circuits and reference sources incorporated within the device architecture so as to eliminate the need for operator optimized biasing, while simultaneously enabling essentially identical operation for both analog delay channels.

4) A CMOS pentode multiplier cell featuring very low power consumption with reduced sensitivity to bias and threshold problems, but requiring some additional fabrication technology development beyond today's commercial CMOS process.

5) Formulas relating correlator design (sizes), operation (biases), and performance (error rejection, power, speed) which facilitate tradeoffs or optimizing such devices for the intended user.

6) A simplified MOS implementation of a current differencing function capable of providing balanced ac-virtual-ground current-input nodes with optional external dc voltage control and either current or voltage readout.

7) A monolithic, MOS/CTD design for the sequential multiply operator,

For the most part, these contributions (except numbers 4 and 7 above) have been experimentally implemented and feasibility/veracity was demonstrated. Consequently, all the above results may be applied to a typical problem to illustrate how to use the findings of the investigation.

Suppose an analysis of system requirements shows a need for submegahertz multiply rates with 40dB rejection of input feedthrough and harmonic distortion but also with an input dynamic range of only 30dB for each multiplier cell in the correlator. Substituting these values into formula (61) yields the result

$$\frac{Y_o - V_{T_m}}{\Delta V_T} \geq 43.9$$

Thus a typical value of $Y_o - V_{T_m} \approx 6$ volts (as from Table 2) gives the fabrication requirement of $\Delta V_T \leq 0.137$ volt, which is quite reasonable. This result is then substituted into equation (60) to determine geometric ratios versus current source (CS) drive. For the assumption implied in table 2 (i.e., a two volt pinch-off, grounded gate) the result becomes $\frac{|(W/L)_B (W/L)_{CS}|^{1/2}}{(W/L)_m} \approx 34.2$

Since these results so closely approximate the values given in Table 2, we know the doubly-balanced triode multiplier cell just now calculated can handle the desired multiply rates. Indeed, for the next step of considering power consumption, we take advantage of the similarity between the desired multiplier cell and those described in Table 2.

When the architectural requirements of the various multiplier cells are applied to the data of Table 2 and Figure 6 , one obtains the comparison of Table 6. The two doubly-balanced triode multiplier cells are basically the doubly-balanced versions (rather than quadruply balanced) of the circuit of Figure 16 . The difference of squares balanced pentode cell is shown in Figure 33 with buffers like those of Table 2; except the basic follower buffer can be much smaller, since it drives

Table 6 Projected Performance Comparison for Correlator Multiplier Cells With 40-dB Rejection of Input Feedthrough and Harmonic Distortion, and 1 MHz Operation.

Technology	Singular MOS Depletion Mode	CMOS Depletion Mode P-Channel with 5E14 cm^{-3} Substrate, 5E15 cm^{-3} Isolation Tub	
Circuit Configuration	Doubly Balanced Triode as per Figure 37	Doubly Balanced Triode as per Figure 37	Difference of Square Balanced Pentodes as per Figure 38
Basic Follower Buffer			
Number needed	3	3	2
Voltage supply	5	5	5
Current, a	135	135	18
Power, mW	2,025	2,025	0.18
Complementary Buffer	Inverter	Complementary Follower	Complementary Follower
Number needed	2	3	1
Voltage Supply	15	7	7
Current,μa	54	18	18
Power, mW	1.62	0.252	0.126
Multiplying Element	Matched Triode Pair	Matched Triode Pair	Dual CMOS Pentode Pairs
Voltage	0	0	15
Current,μa			5
Power, mW	0	0	0.150
Differential Current to Voltage Circuit Incremental Current, μa Voltage Supply Power, mW	(CSRO Circuit not usable because it needs CMOS Process) 2.25	15 (per leg) 12 (2)(7)(0.135)+(12)(0.03) = 2.25	2.5 22 (2)(7)(0.005)+(22)(0.0025) = 0.125
Total Power, mW	5.895	4.527	0.581
Relative Power	10.1	7.8	1.0

only a gate with no current drive or conductance ratio requirements. Likewise the differential current to voltage circuit need only subtract the much smaller pentode "square" currents. Immediately apparent from Table 6 is the effect on power consumption of the requirement by the triode multiplier that the basic follower buffers provide much lower impedance than the triode multiplying elements in order to behave like voltage sources controlling the triode multipliers' source-to-drain voltage.

Table 6 shows the difference of squares balanced pentodes multiplier cell to be very attractive for various reasons: Not only is the power consumption much lower than for triode cells of comparable performance, but the required number of transistors and active semiconductor area are also substantially less. Another advantage indirectly implied in Table 6 results from the pentode operating mode for every transistor, thereby providing reduced sensitivity in the multiplying function to both bias and threshold changes. On the negative side, the difference of squares balanced pentode multiplier cell involves two uncertainties: First is the fabrication requirement for doping levels substantially below those presently used by commercial suppliers. The second uncertainty is the lack of predictive information or formulas describing the dynamic range of the multiplication function and relating it other parameters (as equations (60) and (61) do for triode multipliers) because of the unavailability of either devices or data as per the specification of Figure 6 .

Table 6 also helps with additional conclusions concerning triode multiplier cells. While CMOS fabrication provides somewhat lower power by virtue of the complementary follower gate buffer, the singular

MOS approach gives simpler fabrication with some tradeoffs available to lower power consumption. One such compromise is to replace the higher power inverter with a lower power source-follower, which is then likely to require operating the two analog delay channels with different effective biases in order to obtain the minimal biases needed by the multiplier. Another observation which is true for all the schemes shown in Table 6, but which most strongly affects the power consumption of the singular MOS approach, concerns the use or omission of the ion-implant step to give depletion mode operation. Enhancement mode circuitry requires increasing the voltage supply values by an amount equal to the sum of the depletion pinch-off plus enhancement threshold times the number of series transistors so changed. For example, changing from a 2 volt pinch-off to a 2 volt enhancement threshold for a simple inverter of two series transistors gives a probable need to increase the supply voltage by (2)(2+2)=8 volts or more to allow for a larger reverse-bias source-body effect. Finally we note the simplified current differencing technique of Figures 15,16,17 and 18 is not practical for singular MOS devices, thereby requiring a more complex approach as indicated in Figure 13.

We now summarize the preceding conclusions. For CTD analog-analog correlators or convolvers, many design rules and formulas as well as new techniques have been developed and experimentally demonstrated. When provided performance requirements, the design formulas give limiting values to key circuit parameters, with allowances incorporated for the specifics of the fabrication process. Consequently, the techniques described herein may be applied to the results of a survey of the

requirements of potential users of such a device in order to design (or at least specify) one or a limited set of such CTD analog-analog correlator devices, which are attractive to the largest practical market.

10.0 REFERENCES

1. H. F. Benz, C. Husson, "Satellite Onboard Feature Classification Using CCD's," International Symposium on Circuits and Systems, Phoenix, Arizona, 25-27 April, 1977.

2. Gene. P. Weckler, "Sampled Data Processing with CTD's, "NASA/JPL Conference on CCD Technology and Applications 30 Nov. - 2 Dec. 1976, Washington D.C. (Preceedings pp. 28-32).

3. D. R. Lampe, M. H. White, I. A. Mack, H. C. Lin, "Four Quadrant Analog Multiplier for CCD Signal Processing," GOMAC (9-11 Nov. 1976) Digest of Papers, Vol. VI, pp 238-41.

   D. R. Lampe, H. C. Lin, M. H. White, I. A. Mack,"Fourier Analysis Computer Aided Design of CCD Signal Processing Analog-Multiplier Arrays," NASA/JPL Conference on CCD Technology and Application, 30 Nov - 2 Dec., 1976 Washington, D.C. (Proc., pp. 33-44).

4. P. W. Bosshart, D. D. Buss, C. R. Hewes, M. deWitt, "CCD Correlation Techniques, " NASA/JPL Conference on CCD Technology & Applications, 30 Nov. - 2 Dec 1976, Washington, D.C.

5. J. G. Harp, G. F. Hanstone, D. J. MacLennan, J. Mavor," Analogue Correlators, Using CCD's."Proceedings of 1975 Internationl Conference on the Application of CCD's (29-31 October, 1975, San Diego) pp. 229-35.

6. M. H. White, I. A. Mack, F. J. Kub, D. R. Lampe, J. L. Fagan, "An Analog CCD Transversal Filter with Floating Clock Electrode Sensor and Variable Tap Gains," IEEE ISSCC Digest of Technical Papers, pp. 194-95, 20 Feb. 1976.

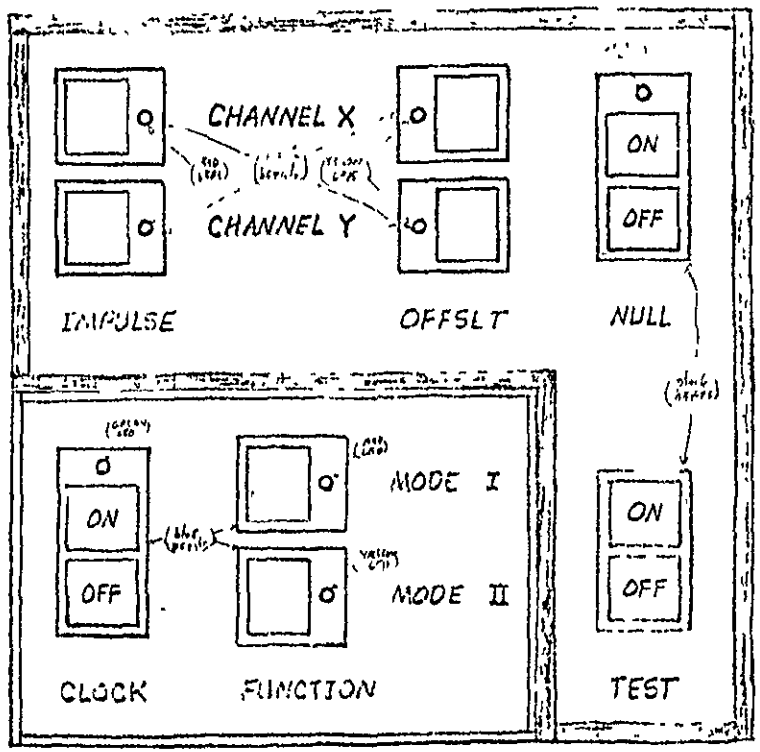
11.0 ACKNOWLEDGEMENT

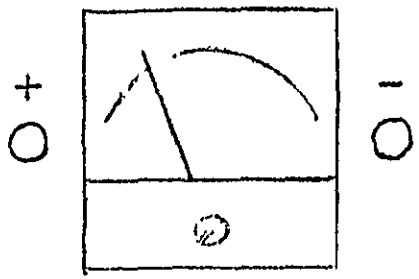
The authors gratefully acknowlege the following technical contributions to the program: C. W. Brooks for early wook on the sequential multiply operation and experimental circuit characterization, I. A. Mack for implementation of the sequential multiply hybrid demonstrator, D. Farnsworth for implementation of the 16-point hybrid correlator model, as well as H. F. Benz, C. Husson, M. H. White, and W. S. Corak for general supportive consultation involving both user requirements and device design.

12.0 APPENDIX A

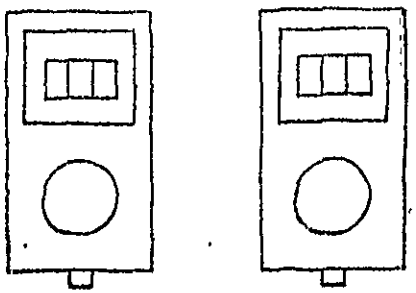
A 16-Point - Correlator Hybrid Feasibility Demonstrator

CTD FOUR QUADRANT ANALOG PROCESSOR

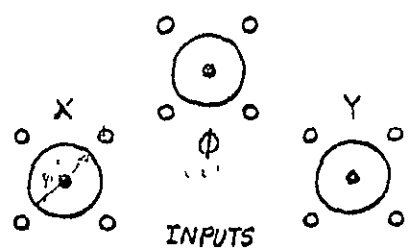




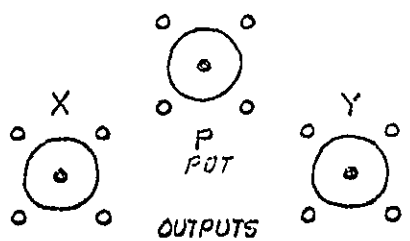
IMPULSE OFFSET



AMPLITUDE



INPUTS

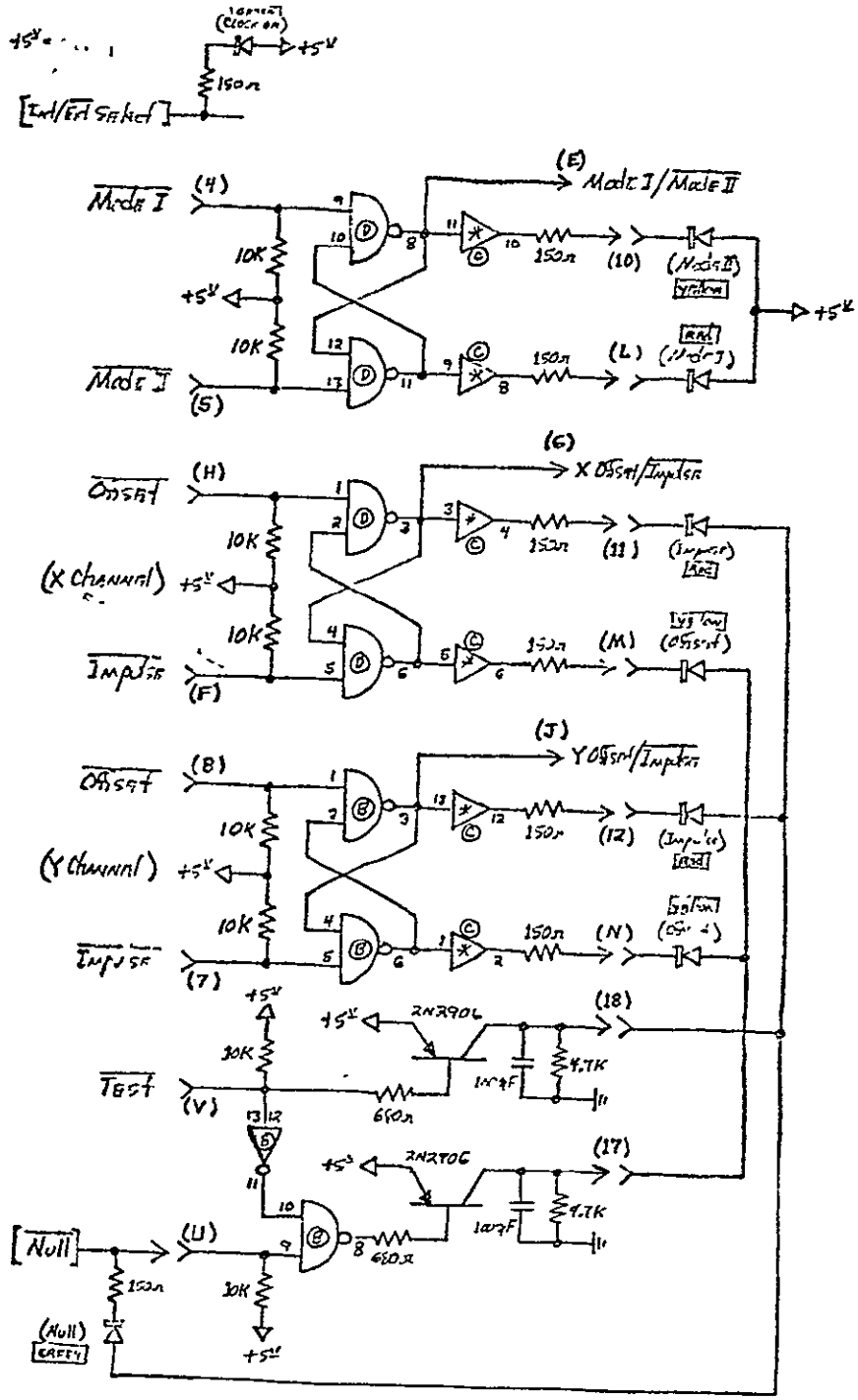


OUTPUTS

FRONT PANEL CONTROL SWITCH LAYOUT GROUPING

ON
POWER
OFF
0.5A
FUSE
SCOPE SYNC
FLS-777
MK-I
SERIAL NO. WAP-0002
110 VAC
60 HZ
LINE

(Sht 1 of 2)



Driver Listing:

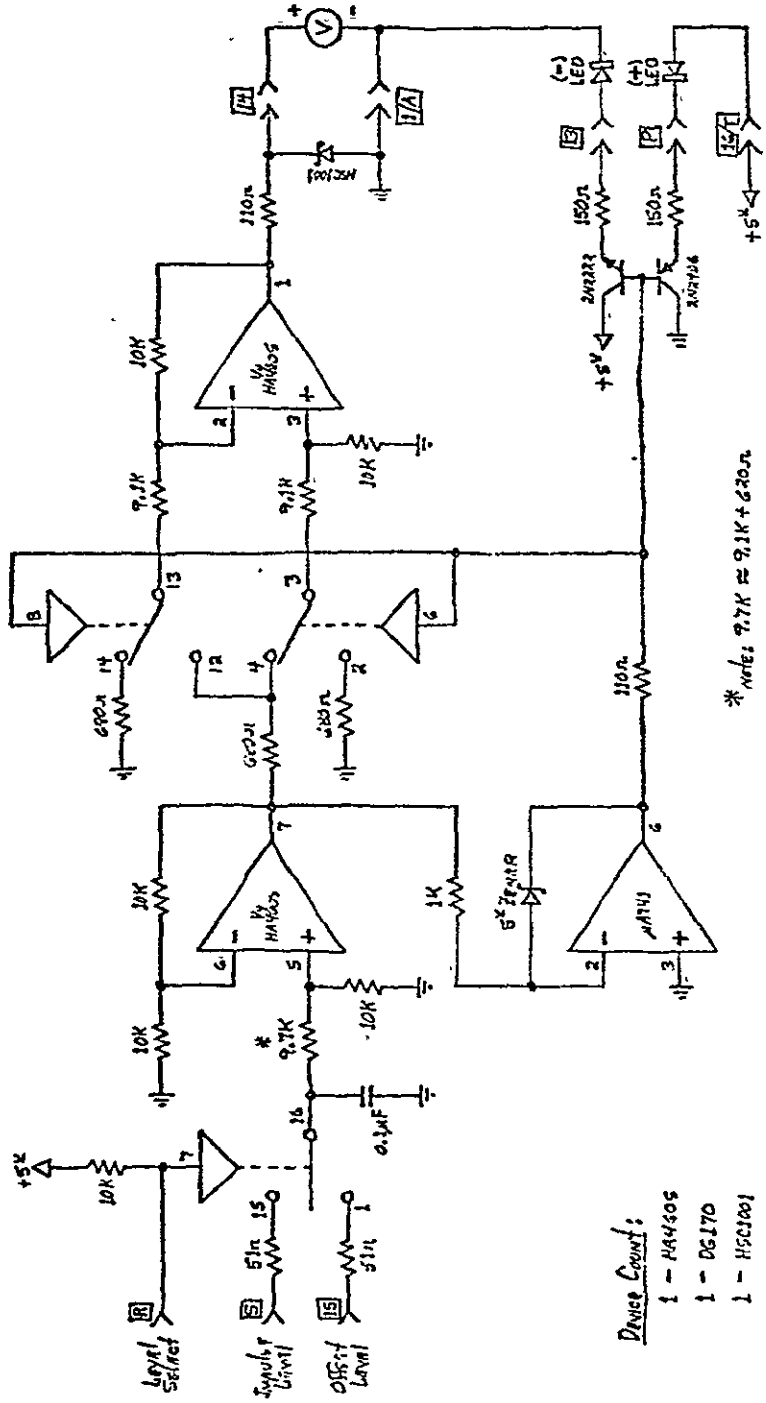
2 - 74LS37	⑧ & ⑨
2 - 2N2906	
1 - 7407	③
1 - 7815	⑥

Passive Components:

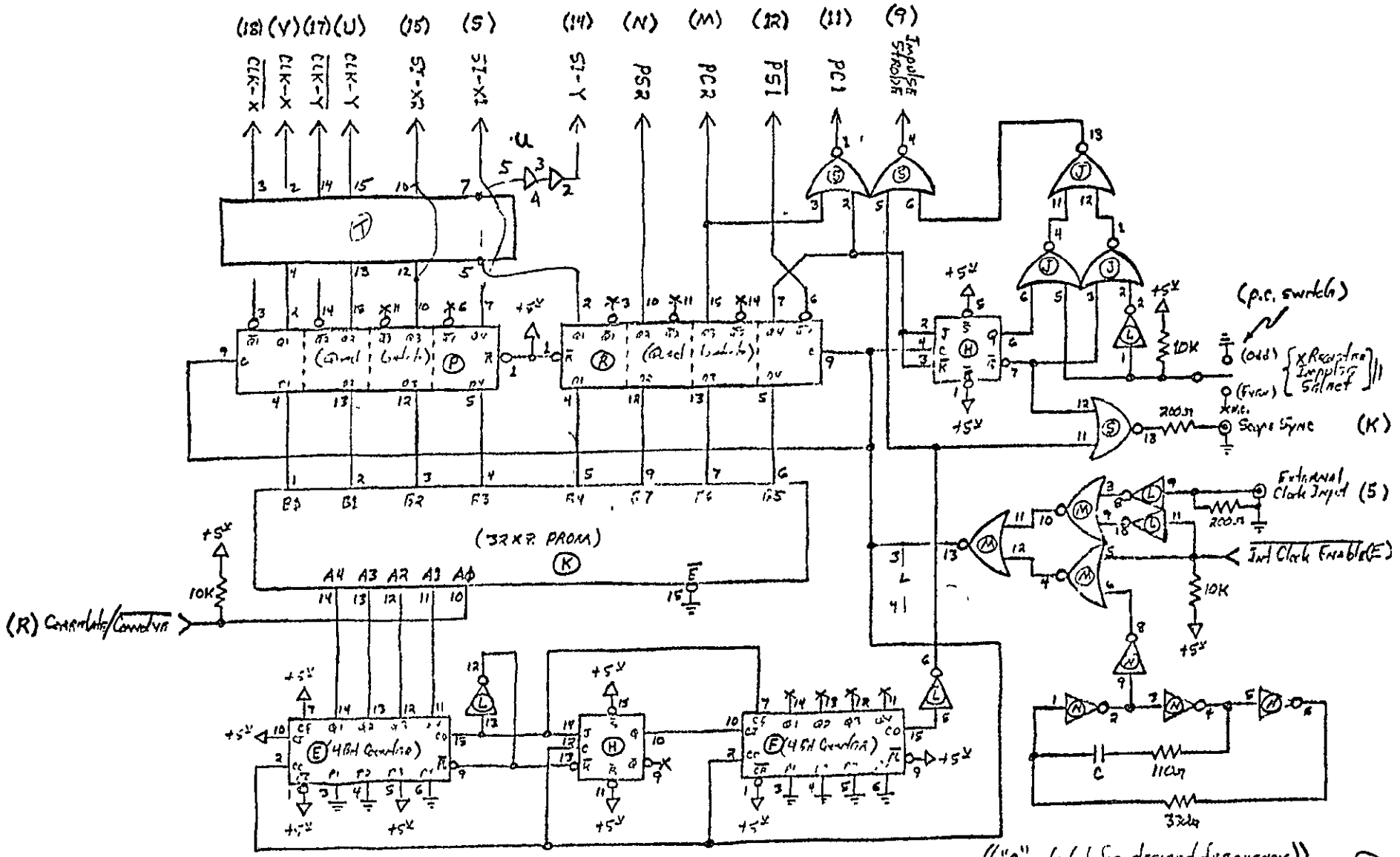
6 - 150Ω	
8 - 10KΩ	
2 - 680Ω	
2 - 4.7KΩ	
2 - 1000pF	

Front Panel Control Switch Logic Interface Circuitry
(Board G-1)

(sheet 2 of 2)



Front Panel Polarity Control Interface Circuitry
(Board B-1)



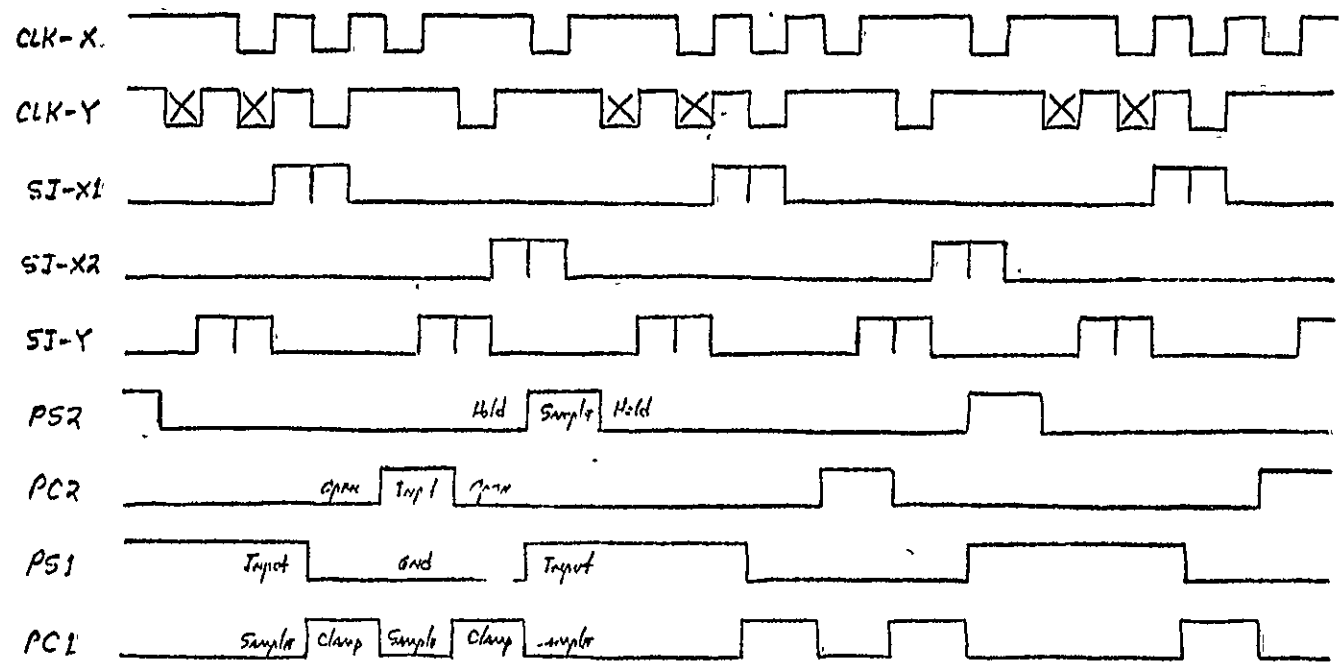
CTD Correlator/Convolver Timing Control Circuitry

(Board B-2)

[device listing]

2@ - 74161	1@ - 7407
2@ - 74174	3@ - 7412
2@ - 7404	1@ - 7

(Fig. 1-2-4)



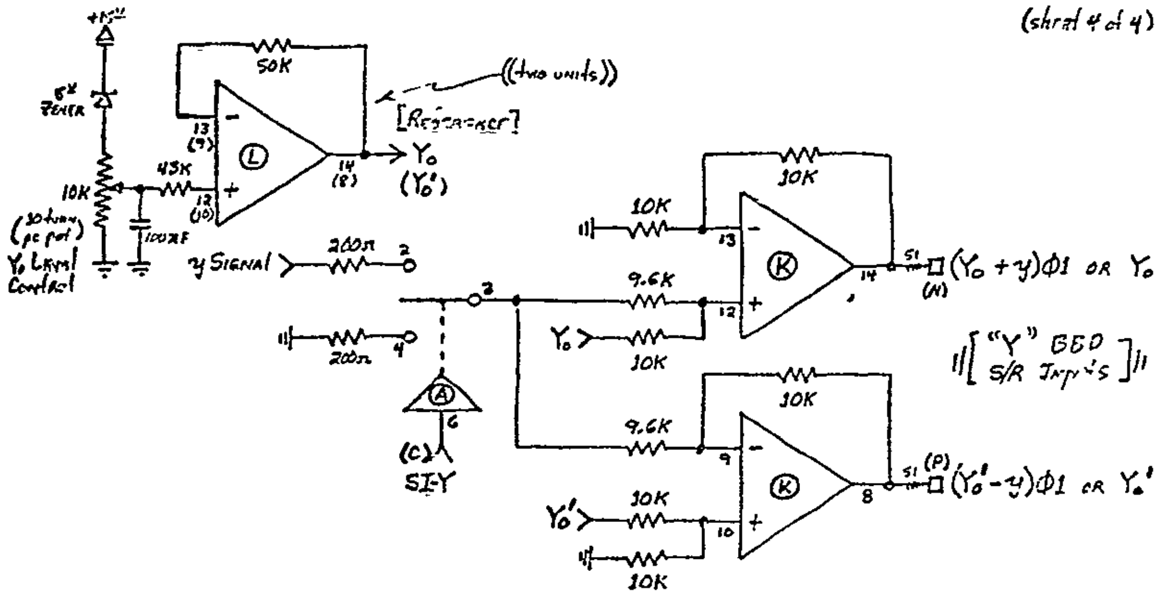
Correlation Function Timing Waveforms Diagram

note: Convolution Timing is same except for definition of CLK-Y pulse levels made at with "X's"

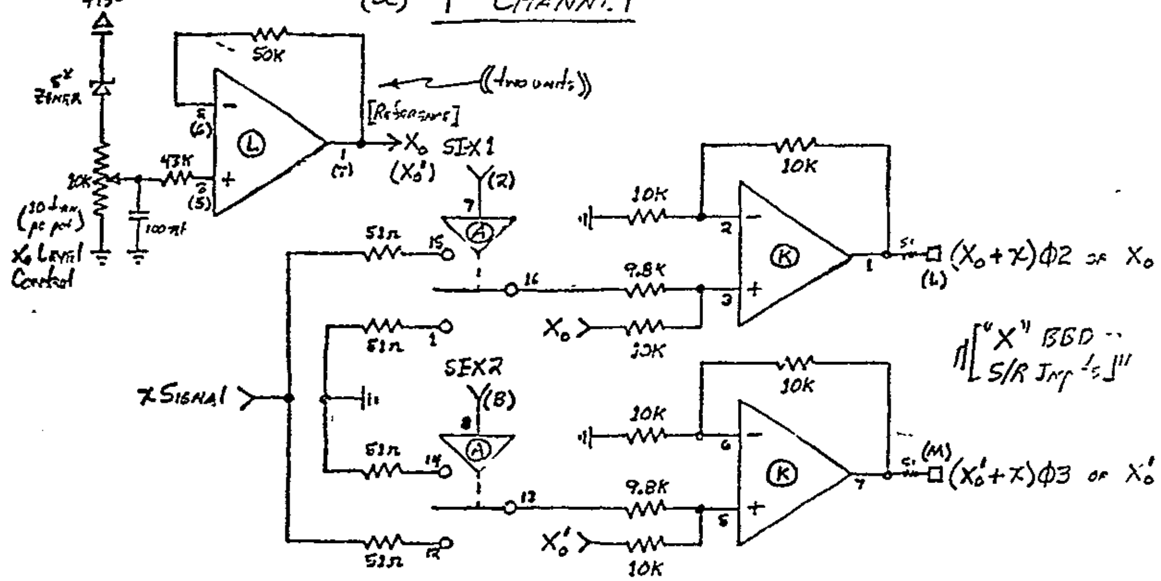
(Sept 72 ; 4)

CTD Correlator/Processor Signal Source Interface Circuitry
(Board B-3)

(Sht 3 of 4)



(a) "Y" Channel



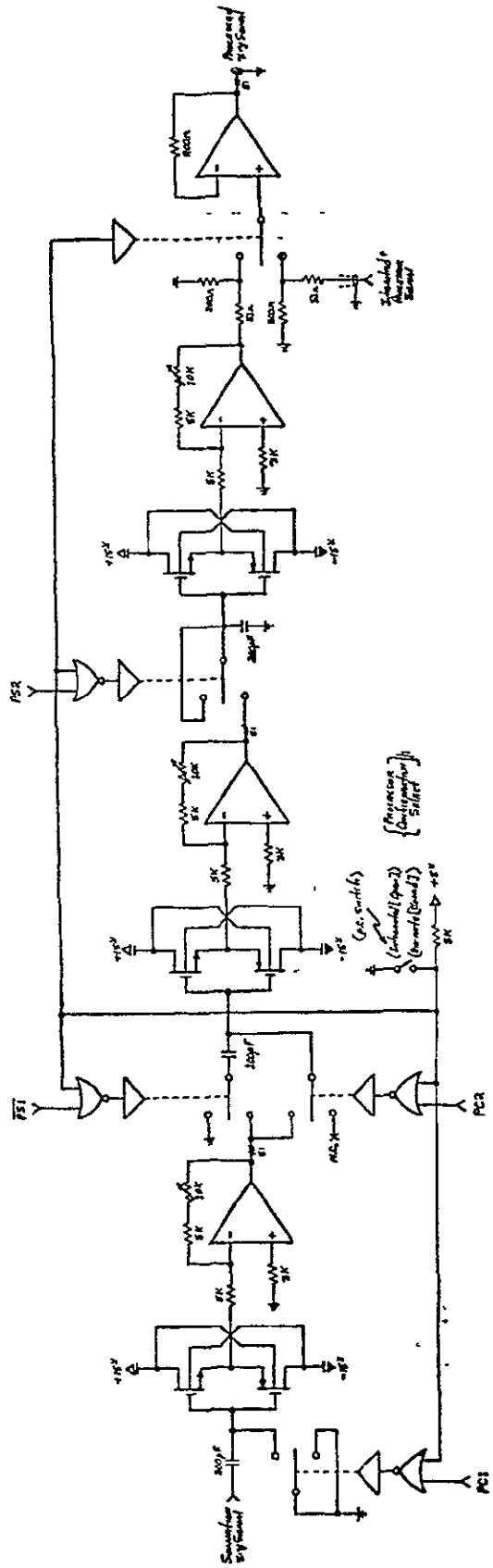
(b) "X" Channel

CTD C... / Convolver Input Circuitry

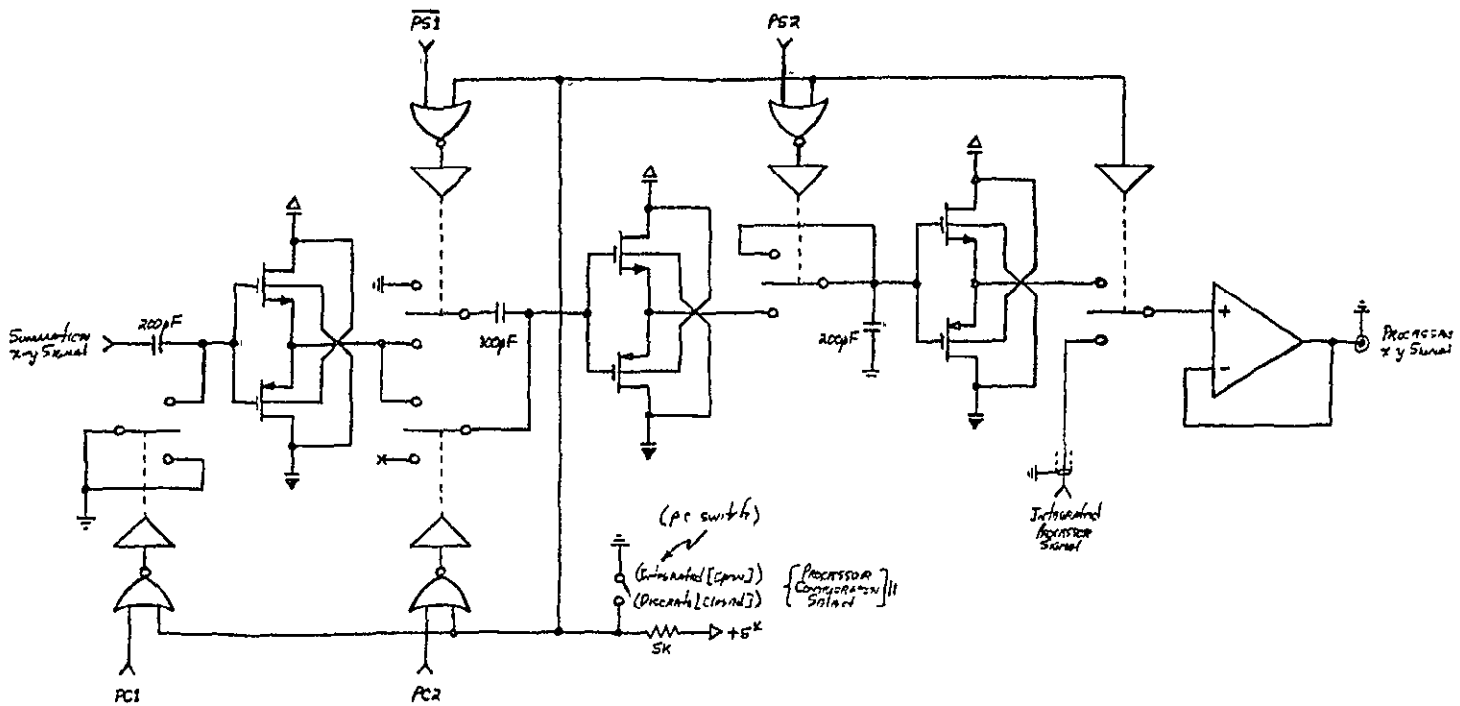
L...: ... — HA4605 — Quad HP Op Amp *
1s — DG170 — Trip SPDT ... Switch

(Figure 5-3)

* ... is the HA4605/4602



CTD Correlator/Convolver Chirp-Sample Analog Processor Chain
Discrete Configuration Type I-A
(Board 6-4)
(Board 6-6B)



CTD Correlator/Convolver Clamp-Sample Analog Processor Chain

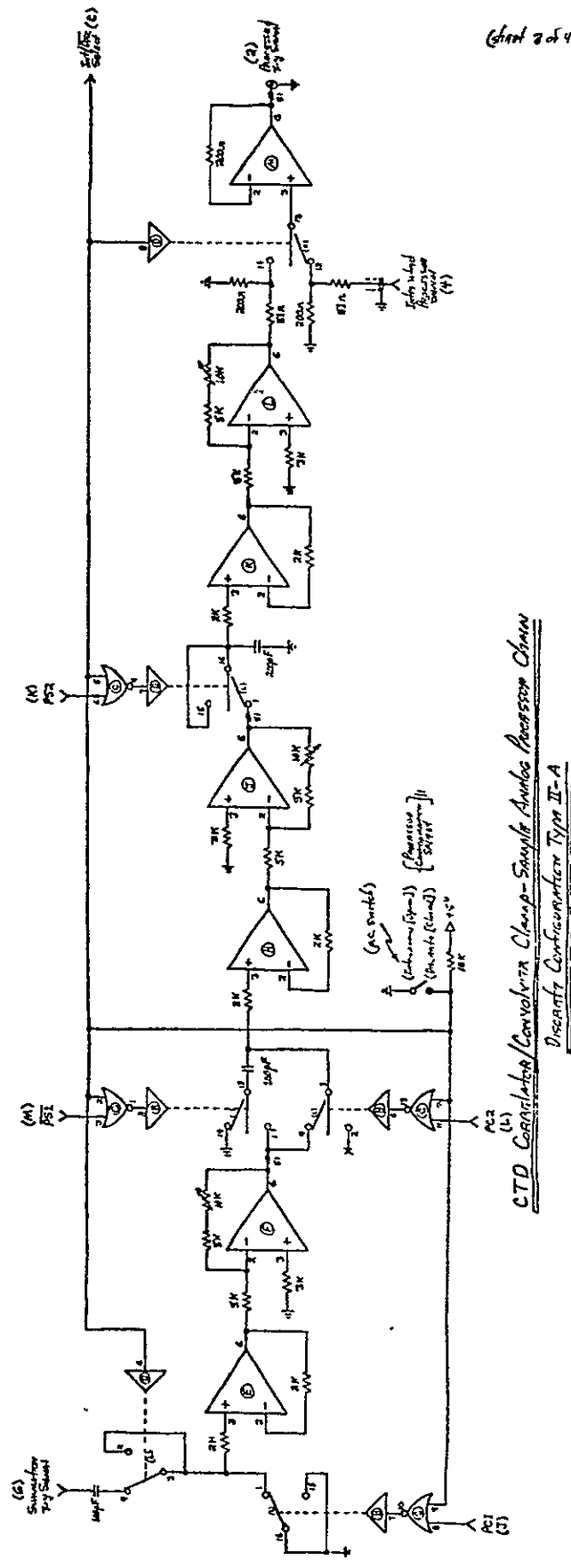
Discrete Configuration Type I-E

(Board B-4)

OR

(Board B-6B)

(Sheet 2 of 4)



(Sheet 3 of 4)

CTD Correlator/Converter Clamp-Sample Analog Processor Chain
Discrete Configuration Type II-A
(Sheet 3-4)

CTD Correlator/Convolver Clamp-Sample Analog Processing Chain

Discrete Configuration Type II-B

(Board B-4)

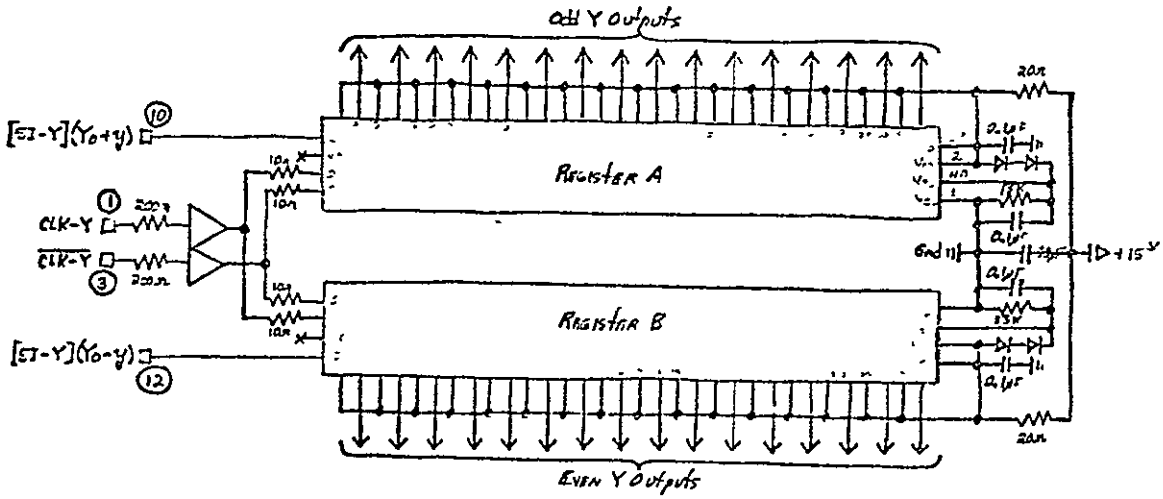
or

(Board B-63)

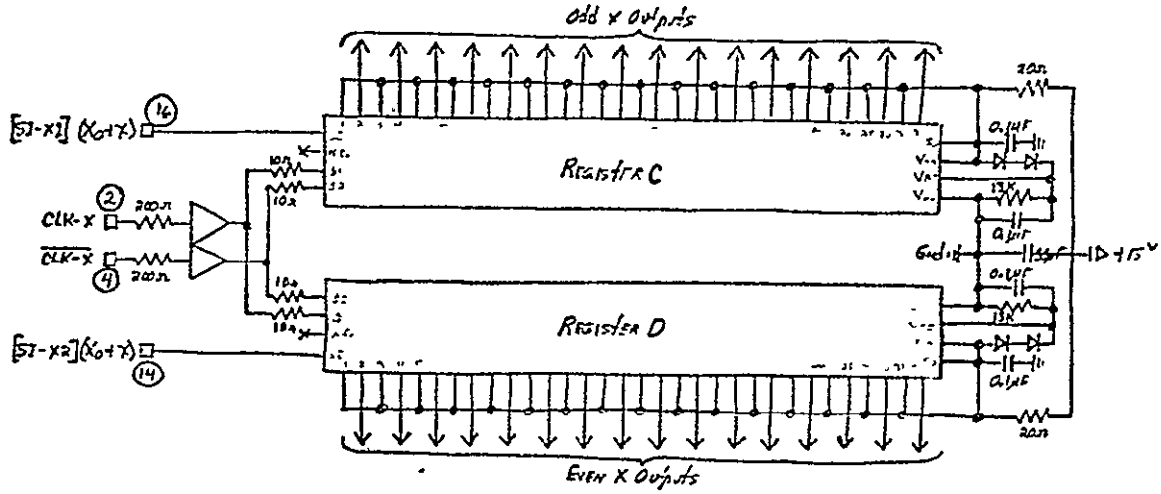
160

(Sheet 4 of 4)

(Sheet 1 of 4)



(a) Y Register Pair

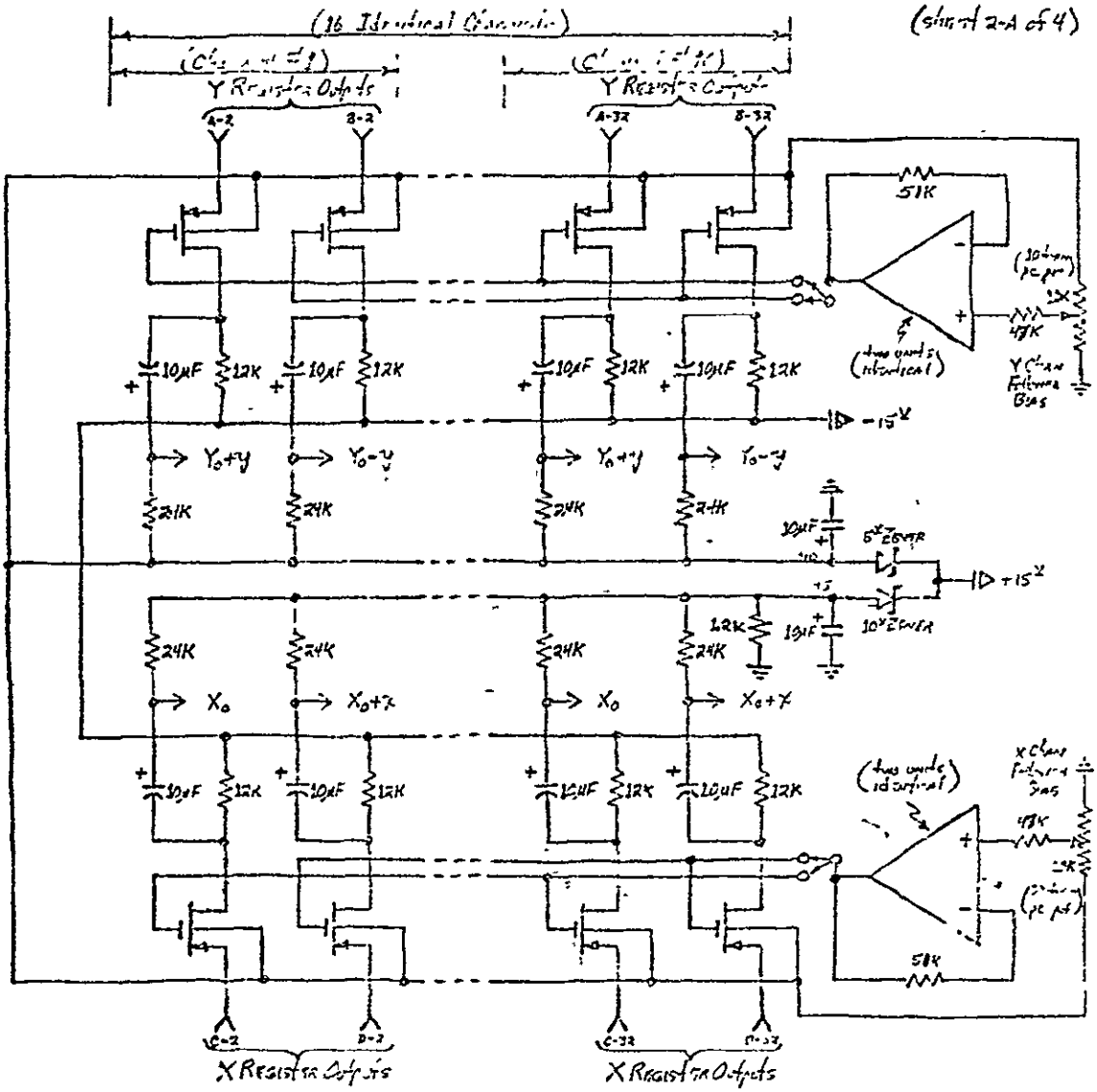


(b) X Register Pair

CTD Correlator/Converter BBD Register Circuitry

(Board B-6A)

4	TAD-32	40p..
2	MH0026	8pin



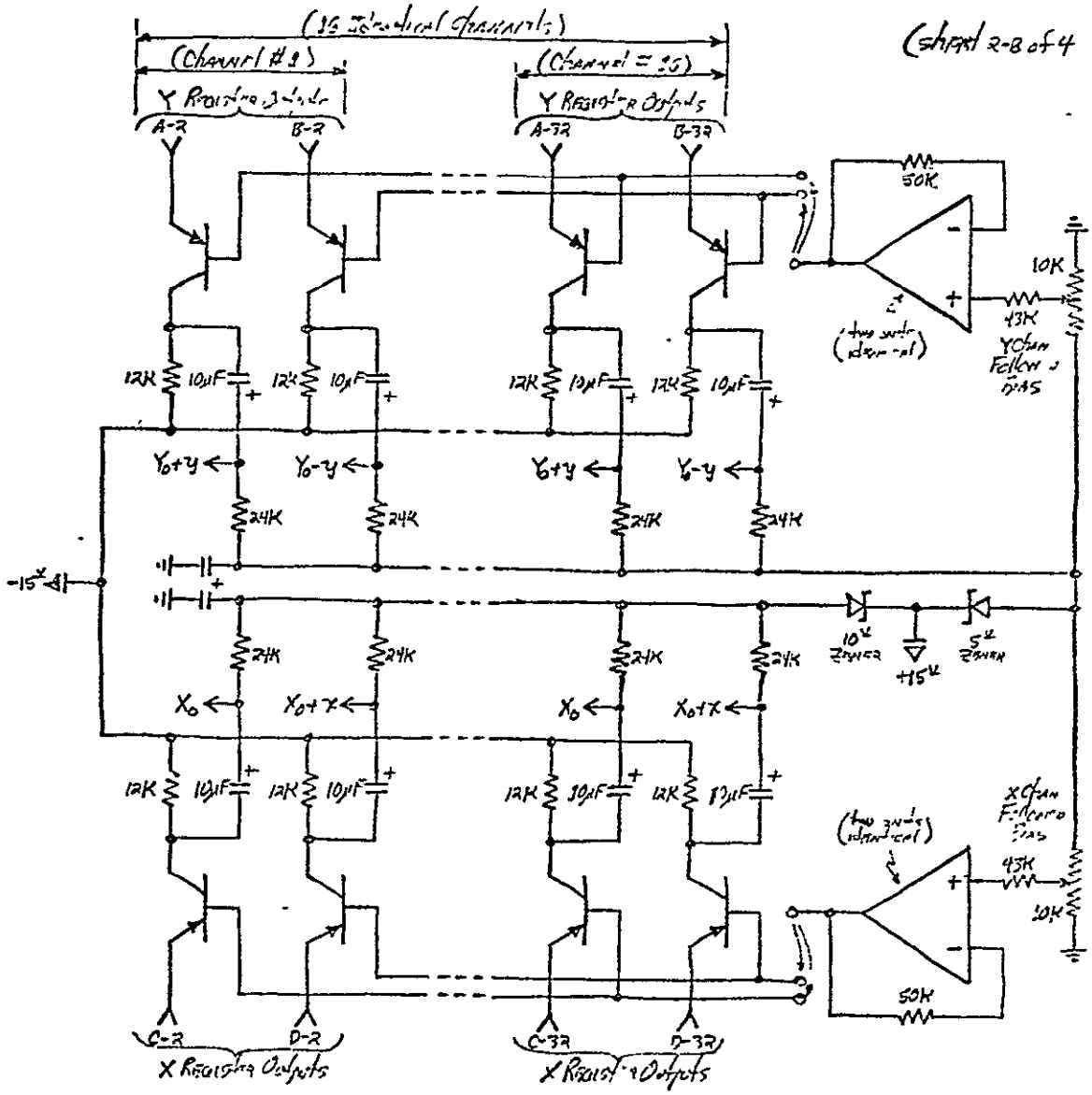
A Register — propagates X_o values only
B Register — propagates alternate X_o & X_o+x values
C Register — propagates alternate Y_o & Y_o+y values
D Register — propagates alternate Y_o & Y_o-y values

Dual-Listing:
16 - HA4552 - 14 pin
1 @ - HA4505 14 pin

BBD Type CTD Register/Multiplier Interface Circuitry

(Board 5-6A)

P-Chan MOS Follower Based Design



A Register – propogates X_0 values only
B " – " alternate X_0 & X_0+X values
C " – " " Y_0 & Y_0+y "
D " – " " Y_0 & Y_0-y "

Device Listing:
16 @ – MHR2207 14 pin
1 @ – HA4605 14 pin

BBD Type CTD Register/Multiplier Interface Circuitry

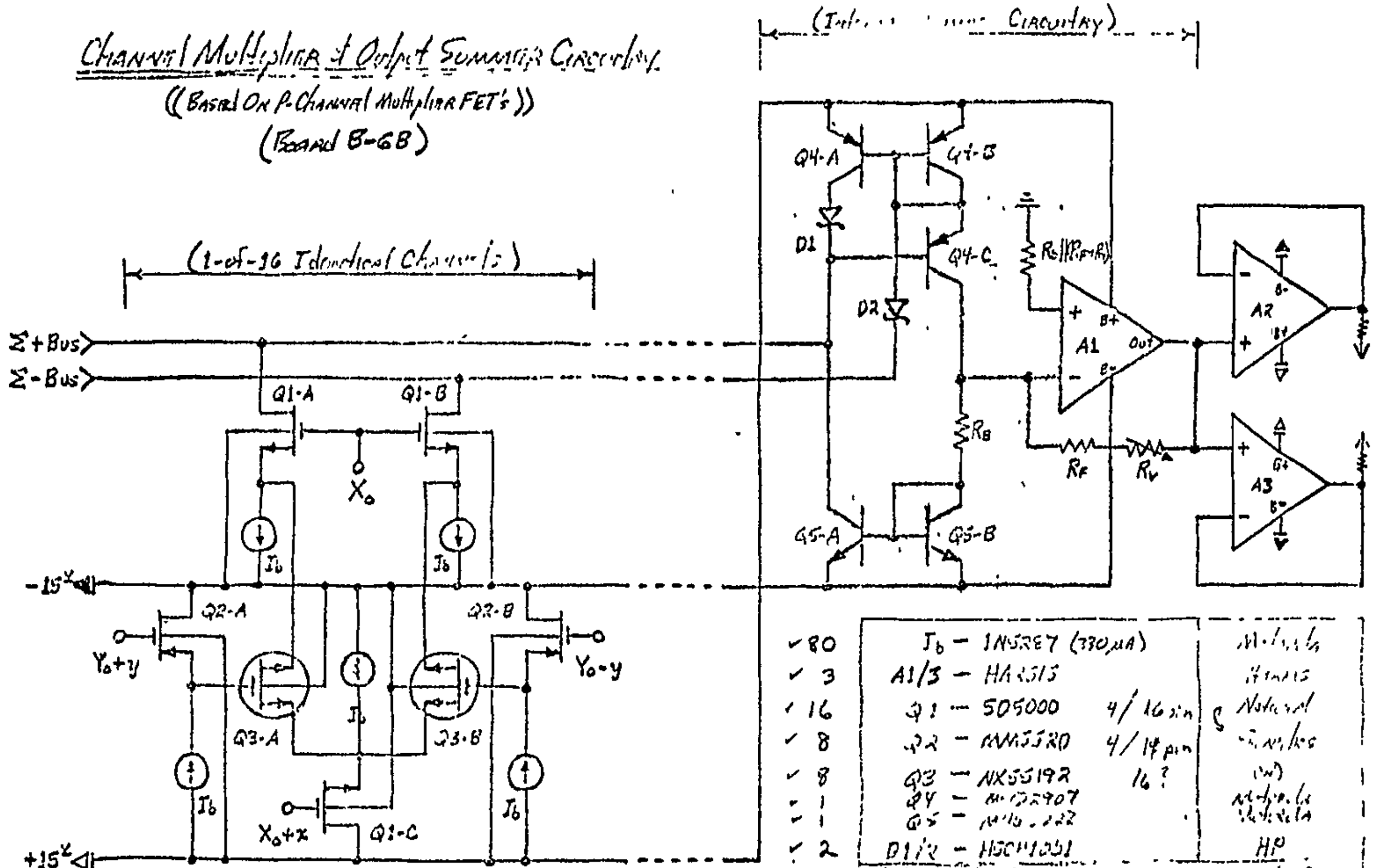
(Board B-6A)

[[PNP Bipolar Follower Based Design]]

Channel Multiplier & Output Summer Circuitry

((Based On P-Channel Multiplier FET's))

(Board B-6B)



[X₀ dc level ≈ +10ᵛ ; Y₀ dc level ≈ +5ᵛ] $(X_0 - Y_0)_{dc}$ = multiplier offset bias

Qty	Part		Source
✓ 80	I_b – 1N5287 (330 µA)		Motorola
✓ 3	A1/3 – HA2515		Harris
✓ 16	Q1 – SD5000	4/16 pin	Natural
✓ 8	Q2 – MM5580	4/14 pin	Siemens
✓ 8	Q3 – NX55192	16?	(*)
✓ 1	Q4 – M[illegible]2907		Motorola
✓ 1	Q5 – M[illegible]2222		Motorola
✓ 2	D1/2 – HSCH1001		HP

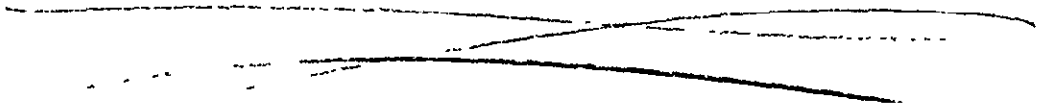
(*) matched pair D-MOS & P-MOS with spec of $r_{ds_{on}} \cong 2K\Omega$, $V_p \cong -2^V$ (lot screened), $\Delta V_p(\text{pair}) \leq 10^{mV}$, $\Delta V_p(\text{lot}) \cong 100^{mV}$.

[[Hughes Array]]

Component Listing

(Sheet 3 of 7)

CTD Correlator/Controller Board Components



Boards:

(1) Front Panel
(2) Rear Panel
(3) Board B-8 (ADC)
(4) Board B-1
(5) Board B-2
(6) Board B-3
(7) Board B-4
(8) Board B-5
(9) Board B-6 (ADC)

Front Panel Components

A. BNC Input Jacks
   1. Ext Clock
   2. Ext x
   3. Ext y

B. BNC Output Jacks
   1. Monitor x
   2. Monitor y
   3. Processed x·y

C. Adjustment Pots (10-turn)
   1. Offset Level
   2. Impulse Level

D. 0-15[X] Panel Voltmeter (autoscaling)

E. Meter Function Toggle Switch

F. Touch Control Switches
   1. Function Select
      a. Correlate
      b. Convolve
   2. Impulse Select
      a. X Chan
      b. Y Chan
   3. Offset Select
      a. X Chan
      b. Y Chan
   4. Offset Null
   5. Function Test
   6. Internal Clock

Rear Panel Components

A. BNC Scope Sync Jack

B. Power Line Fuse Holder (½ Amp)

C. Power Cord Strain Relief

D. Power Switch (lighted rocker)

Board B-1 Component Listing

Active Devices

1 – 7805 – +5V Regulator
1 – 7815 – +15V "
1 – 7915 – -15V "
2 – 74LS37 – Quad NAND
1 – 7407 – Hex Open C Buff
1 – HA4605 – Quad Op Amp
1 – µA741 – LF " "
1 – DG170 – Twin SPDT Switch
4 – 2N2906 – PNP Transistor
2 – 2N2222 – NPN "
1 – HSC1001 – Schottky Diode

Resistors

8 – 150Ω
14 – 10KΩ
5 – 680Ω
2 – 4.7KΩ
1 – 620Ω
3 – 9.1KΩ
2 – 51Ω
2 – 110Ω
1 – 1KΩ

Capacitors

3 – 100pF
1 – 10µF
2 – 47µF
3 – 4.7µF

Board B-2 Component Listing

Active Devices

1 – 7805 – +5V Regulator
1 – 74109 – Dual J-K Flip Flop
1 – 8256 – 32x8 Bipolar PROM
2 – 74LS161 – 4 Bit Binary Counter
2 – 74LS175 – Quad D Latch
2 – 74LS04 – Hex Inv
3 – 74LS02 – Quad NOR

Resistors

1 – 110Ω
1 – 330Ω
2 – 220Ω
2 – 10KΩ

P.C. Switches

1 – SPST DIL Slide

Capacitors

1 – (see Tana cap)
1 – 47µF
1 – 10µF
3 – 100pF

Board B-3 Component Listing

Active Devices

4	HA4605	Quad Op Amp
3	DG170	Trip SPDT Switch
4	IN758A	10V Zener Diode
2	IN751A	5V Zener Diode
1	7815	+15V Regulator
1	7805	+5V "
1	7915	-15V "

Resistors

6	43Kn
6	51Kn
16	51n
10	9.1Kn
4	680n
6	510n
22	10Kn
4	200n

P.C. Trim Pots

4	10Kn

Capacitors

2	47μF
3	4.7μF
1	10μF
10	100ηF
4	10ηF

Board B-4 Component Listing
(Type II-A)

Active Devices

7	HA2515	Hi Perf Op Amp
2	DG170	Trip SPDT Switch
1	74L502	Quad NOR
1	7815	+15V Regulator
1	7805	+5V "
1	7915	-15V "

Resistors

6	2Kn
3	3Kn
6	5Kn
5	51n
3	200n
1	10Kn

P.C. Trim Pots

3	10Kn

P.C. Switches

1	SPST DIL Slide

Capacitors

2	200pF
1	100pF
2	47μF
3	4.7μF
1	10μF
3	100ηF

B1-A/1 ⟶ Meter Negative Lead ⟶ Meter-Polarity LED Cathode ⟶ Level Select Toggle Switch Contact
B1-E ⟶ B2-R
B1-F ⟶ X Impulse Touch Switch Output
B1-H ⟶ X Offset Touch Switch Output
B1-J ⟶ B3-E
B1-L ⟶ Mode 1 LED Cathode
B1-M ⟶ X Offset LED Cathode
B1-N ⟶ Y Offset LED Cathode
B1-P ⟶ Meter+Polarity LED Cathode
B1-R ⟶ Level Select Toggle Switch Alone ((acts as SPST with ground contact))
B1-S ⟶ B3-F
B1-T/G ⟶ Meter+Polarity LED Anode ⟶ Clock Select LED Anode ⟶ Mode 1 LED Anode ⟶ Mode 2 LED Anode
B1-U ⟶ B3-4 ⟶ Offset Null Touch Switch Output
B1-V ⟶ B3-5 ⟶ Function Test Touch Switch Output
B1-18 ⟶ X Impulse LED Anode ⟶ Y Impulse LED Anode ⟶ Offset Null LED Anode
B1-17 ⟶ X Offset LED Anode ⟶ Y Offset LED Anode
B1-15 ⟶ B3-6
B1-14 ⟶ Meter Positive Lead
B1-13 ⟶ Meter-Polarity LED-Anode
B1-12 ⟶ Y Impulse LED Cathode
B1-11 ⟶ X Impulse LED Cathode
B1-10 ⟶ Mode 2 LED Cathode
B1-8 ⟶ Y Offset Touch Switch Output
B1-7 ⟶ Y Impulse Touch Switch Output
B1-6 ⟶ B3-D
B1-5 ⟶ Mode 2 Touch Switch Output
B1-4 ⟶ Mode 1 Touch Switch Output

B2-E ⟶ Clock Select Touch Switch Output
B2-K ⟶ Back Panel Test Scope Sync BNC ((coax shield grounded only at BNC))
B2-M ⟶ B4-L ⟶ BGB-J10
B2-N ⟶ B4-K ⟶ BGB-J8
B2-R ⟶ B1-E
B2-S ⟶ B3-2
B2-U ⟶ BGA-J1
B2-V ⟶ BGA-J2
B2-18 ⟶ BGA-J4
B2-17 ⟶ BGA-J3
B2-15 ⟶ B3-B

(continued)

(continued)

B2-14 ⟶ B3-C
B2-12 ⟶ B4-M ⟶ BGB-J12
B2-11 ⟶ B4-J ⟶ BGB-J6
B2-9 ⟶ B3-3
B2-5 ⟶ Front Panel Φ Input BNC ((coax shield grounded only at BNC))

B3-B ⟶ B2-15
B3-C ⟶ B2-14
B3-D ⟶ B1-6
B3-E ⟶ B1-J
B3-F ⟶ B1-S
B3-H ⟶ Front Panel Y Input BNC ((coax shield grounded only at BNC))
B3-J ⟶ Front Panel X Input BNC ((coax shield grounded only at BNC))
B3-L ⟶ BGA-J16 [[twisted pair ground lead tied to B3-10 ⟶ BGA-J15]]
B3-M ⟶ BGA-J14 [[twisted pair ground lead tied to B3-11 ⟶ BGA-J13]]
B3-N ⟶ BGA-J12 [[twisted pair ground lead tied to B3-12 ⟶ BGA-J11]]
B3-P ⟶ BGA-J10 [[twisted pair ground lead tied to B3-13 ⟶ BGA-J9]]
B3-S ⟶ Offset Trim Pot Arm
B3-T ⟶ Offset Trim Pot CCW Reference Contact (low)
B3-U ⟶ Offset Trim Pot CW Reference Contact (high)
B3-17 ⟶ Impulse Trim Pot CCW Reference Contact (low)
B3-16 ⟶ Impulse Trim Pot CW Reference Contact (high)
B3-15 ⟶ Impulse Trim Pot Arm
B3-8 ⟶ Front Panel X Output BNC ((coax shield grounded only at BNC))
B3-7 ⟶ Front Panel Y Output BNC ((coax shield grounded only at BNC))
B3-6 ⟶ B1-15
B3-5 ⟶ B1-V ⟶ Function Test Switch Transfer Output
B3-4 ⟶ B1-U ⟶ Offset Null Touch Switch Output
B3-3 ⟶ B2-9
B3-2 ⟶ B2-5

B4-C ⟶ BGB-J1
B4-J ⟶ BGB-J6 [[twisted pair ground lead tied to B4-8 ⟶ BGB-J7]]
B4-K ⟶ BGB-J8 [[twisted pair ground lead tied to B4-9 ⟶ BGB-J9]]
B4-L ⟶ BGB-J10 [[twisted pair ground lead tied to B4-10 ⟶ BGB-J11]]
B4-M ⟶ BGB-J12 [[twisted pair ground lead tied to B4-11 ⟶ BGB-J13]]
B4-6 ⟶ BGB-J4 [[twisted pair ground lead tied to B4-7 ⟶ BGB-J5]]
B4-4 ⟶ BGB-J2 [[twisted pair ground lead tied to B4-5 ⟶ BGB-J3]]
B4-2 ⟶ Front Panel P Cal + BNC ((coax shield grounded only at BNC))

(CONTINUED)

BU	BGA - J1	⟶	CLK-Y	⟶ B2-U
R	BGA - J2	⟶	CLK-X	⟶ B2-V
O	BGA - J3	⟶	$\overline{\text{CLK-Y}}$	⟶ B2-18
Y	BGA - J4	⟶	$\overline{\text{CLK-X}}$	⟶ B2-17
G	- J5	⟶	GROUND	⟶ B2-W
BU	- J6	⟶	+17	⟶ BUS Y,21
V	- J7	⟶	+7	⟶ BUS Z,22
G	- J8	⟶	-17	⟶ BUS X,20
W	- J9	⟶	GROUND	⟶ B3-13
BK	- J10	⟶	$Y_0' - \frac{\alpha}{2}$	⟶ B3-P
BN	- J11	⟶	GROUND	⟶ B3-12
R	- J12	⟶	$Y_0 + \frac{\alpha}{2}$	⟶ B3-N
O	- J13	⟶	GROUND	⟶ B3-11
Y	- J14	⟶	$(X_0' + \alpha)_2$	⟶ B3-M
G	- J15	⟶	GROUND	⟶ B3-10
BU	- J16	⟶	$(X_0 + \alpha)_1$	⟶ B3-L

BGB - J1	⟶	INTG/$\overline{\text{DESC}}$ CLL	⟶	B4-C
- J2	⟶	INTG PROC SIGNAL	⟶	B4-4
- J3	⟶	GROUND	⟶	B4-5
- J4	⟶	X-Y SUM SIGNAL	⟶	B4-6
- J5	⟶	GROUND	⟶	B4-7
- J6	⟶	PC1	⟶	B4-J
- J7	⟶	GROUND	⟶	B4-8
- J8	⟶	PS2	⟶	B4-K
- J9	⟶	GROUND	⟶	B4-9
- J10	⟶	PC2	⟶	B4-L
- J11	⟶	GROUND	⟶	B4-10
- J12	⟶	$\overline{\text{PS1}}$	⟶	B4-M
- J13	⟶	GROUND	⟶	B4-11
- J14	⟶	-17V	⟶	BUS-X,20
- J15	⟶	+17V	⟶	BUS Y,21
- J16	⟶	+7V	⟶	BUS Z,22