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DEVELOPMENT OF HIGH RELIABILITY, HIGH FREQUENCY POWER CONDITIONING MODELS OF CONVERTER-REGULATORS

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PREFACE

Objective

The objective of this study program was to optimize the techniques necessary for high efficiency conversion, regulation, and filtering of power using high conversion frequencies, and to apply these techniques to two sample converters representative of the two basic types of converters required in the normal space mission. One of these is a low power converter typical of an instrument type converter designed to power the circuitry involved in an individual instrument. The second of these is a higher power converter typical of the type that would be used to provide the primary power bus for an entire spacecraft or group of experiments. The overall objective of the work is to determine the feasibility of designing converters of this type for operation at the higher frequencies and secondly to optimize and document the techniques, components, and materials most suited for this usage.

Scope of Work

The scope of work included a review of the available components, both active and passive and the materials, specifically magnetic core materials available for use in high frequency designs. These components were then used to produce individual circuits of the types necessary to build an overall converter. These circuits included oscillator circuits, duty cycle modulator circuits, converter circuits, rectifier circuits, and filter circuits. In addition to the above, a reasonable effort was expended in the investigation of other possible approaches to the high frequency conversion and regulation of power. The results of this preliminary work were then applied to the design of two sample converters as described above. These converters were then fabricated in a packaged breadboard configuration and test data was taken to indicate the level of performance obtained.

Conclusions

The overall conclusion is that useful performance can be provided at the extremes of power level chosen for the two sample converters. There are definite strengths and weaknesses of the high frequency approach as opposed to the more standard low frequency approach. The weaknesses may be summarized as a somewhat lowered efficiency especially in the low power case, a reduced selection of components and materials which can be utilized, and increased difficulty in design and reproduction of the final circuits. It is felt that useful performance can be obtained with relatively conventional circuitry tailored to take advantage of the higher frequencies where this advantage exists and to minimize the negative effects in terms of lower breakdown voltage devices, higher transient currents, etc.

Summary of Recommendations

It is recommended that relatively conventional techniques be utilized should the need arise to accomplish conversion and regulation at the frequencies utilized for this study and that these techniques be upgraded in terms of the component selection presently available.

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Introduction

Intent of Program

The general requirements of the study contract are to investigate the techniques required to process power using switching frequencies from 1 to 2 orders of magnitude higher than those currently used in present day power converters, while maintaining overall efficiencies at or near the levels achieved at the lower frequencies and achieving this performance without degrading the overall reliability of the system. The techniques developed are then applied to the design of two sample converters, one of which is a medium power instrument type converter having two output voltages and a total output power of approximately 20 watts and operating in the frequency range of 1 to 5 MHz. The second of these is a primary or spacecraft type converter having a single output with a maximum output power capability of 200 watts and operating in the frequency range from 200 - 500 KHz with the additional feature that the power section be capable of being stacked in order to increase the output power level.

Approach

The approach utilized during the study was to investigate each of the areas which go to make up a total power converter design. Conventional techniques, i.e., those used at lower frequencies, were evaluated in terms of performance at the higher frequencies under consideration. Data was solicited from manufacturers in order to allow a preliminary selection of components and materials suitable for the purpose. A review of the possible overall configurations of the sample converters was undertaken and consideration was given to special reliability problems encountered due to the high speed operation. All of the foregoing was used as a baseline to guide the direction of the remainder of the investigation and the ultimate choice of techniques to be used in the sample converters. Two sample converters representative of experiment and spacecraft converter requirements having power levels and operating frequencies as outlined above were fabricated. The converters were then evaluated, optimized and documented to provide an indication of the performance achievable. As a parallel effort throughout the course of the investigation, consideration was given to more radical approaches which might lead to a significant breakthrough in the general area of high frequency conversion.

A general outline of the investigation is as follows:

1. Component and material selection
2. Magnetic component design
3. Circuits
   a. Duty cycle modulation circuits
   b. Converter circuits
   c. Rectifier circuits
   d. Filter circuits
   e. Oscillator circuits
4. Choice of overall configurations; that is, the choice of buck, boost, or buck/boost configuration
5. Reliability considerations
6. Blue sky approaches
7. Instrument converter
8. Spacecraft converter

These individual areas will be dicsussed in the following sections.

Component and Material Selection

Diodes - The general area of diodes for use as rectifiers and as coupling and gating elements would seem to present the least problem of the areas surveyed to date. The advent of the newer ion implanted devices, the introduction of Schottky barrier devices having high current capability, and the great improvement in the speed of conventional power devices would indicate that devices are available for most applications which will function at relatively high efficiency provided these devices meet or at least approach manufacturers' claims and that they do not suffer from inherent failure modes which would preclude their use in a high reliability application.

One item of concern is the relatively large junction capacity inherent in some of these devices presumably due to the use of large junction areas in order to increase forward conductance capability especially in the case of the power Schottky barrier type. A second limitation which applies most predominantly to the Schottky barrier types is the relatively low reverse voltage capability, which in the case of the Schottky barrier devices would limit their use to outputs in the order of 15 volts. On the plus side, most of the devices surveyed seemed to indicate a high degree of tolerance to large transient current surges which is a distinct advantage when one is concerned with capacitor charging and short circuit protection. A list of types selected for further evaluation and/or usage is included along with abbreviated specifications.

Transistors - This area is, of course, a critical one. Devices capable of switching the required currents and handling the

TABLE 1. HIGH SPEED DIODES

Type	If(A)	Isurge(A)	PRV(v)	Vf(v)	IR(ua)	Trr(nsec.)
			Conventional			
1N4936	1	30	400	1	1	100
SVD100-1	1	10	100	1	5	20
UTX225	2	40	250	0.6	3	75
1N5806	2.5	35	150	0.875	1	25
SVD450-3	3	30	450	1.5	5	70
SVD450-5	5	50	450	1.5	10	70
SVD100-6	6	60	100	1.2	75	25
1N3880-83	6	150	100-400	1	10	100
1N5811	6	125	150	0.875	5	30
SVD100-12	12	120	100	1.2	125	25
1N5410	12	200	150	1	100	70
1N3890-93	12	200	100-400	1	10	100
PD9050E	15	300	200	1	100	70
1N3900-03	20	250	100-400	1.1	10	100
1N5816	20	250	150	0.9	10	35
1N3910-13	30	300	100-400	1.1	10	100
1N5409	30	500	150	1.2	100	70
			Ion-Implanted			
HSR-0	1	100	100	0.9	10	9
HSR-2	3	150	100	0.9	25	10
HSR-3	8	500	100	0.9	75	20
HSR-4	20	800	100	0.9	100	25
HSR-5	30	1000	100	0.9	200	35
			Schottky Barrier			
MBD5300	5	500	20	0.35	20ma	Majority
MBD5400	25	600	20	0.45	30ma	carrier
1N5825	5	500	40	0.38	10ma	device.
1N5828	15	500	40	0.50	10ma	Majority
1N5831	25	800	40	0.48	20ma	carrier
1N5834	40	800	40	0.59	20ma	device.

TABLE 2. HIGH SPEED HIGH VOLTAGE TRANSISTORS

Type	Structure	Ic Max(A)	BVceo(v)	Tr(ns)	Ts(ns)	Tf(ns)	Switching Time Test Current(A)
2N4405	PNP	1	80	25	175	35	0.5
2N3723	NPN	1	80	18	40	25	0.5
2N3725	NPN	1	80	13	26	12	0.5
2N4014	NPN	1	80	13	26	12	0.5
2N4031	PNP	1	80	22	150	27	0.5
2N3763	PNP	1.5	60	35	80	35	1
2N3765	PNP	1.5	60	35	80	35	1
2N5861	NPN	2	50	18	35	35	0.5
SDT6103	NPN	5	50	50 (Ton)		50 (Toff)	2
SDT6106	NPN	5	50	50 (Ton)		50 (Toff)	2
SDT6112	NPN	10	50	75 (Ton)		75 (Toff)	5
SDT6115	NPN	10	50	75 (Ton)		75 (Toff)	5

voltage levels imposed by the bus line requirements and the circuit configurations must be located which can switch rapidly enough to maintain the power loss within the device to acceptable levels.

There are, of course, many transistors available today which offer extremely rapid switching specifications. Unfortunately, high speed, high voltage and high current handling capability do not, in general, go together. Many of the extremely fast devices designed for switching applications in digital circuitry have relatively low breakdown voltages and, in general, are small geometry devices with low to moderate current handling capability. While some of these devices may readily find application in the lower level portions of power converter circuitry being discussed, they do not lend themselves to straightforward application in the higher power handling sections of such converters. This situation, in general, dictates a two pronged attack on the problem of providing the required switching circuitry. The first of these is the more straightforward approach utilizing the best of the devices capable of handling the voltage and current required and optimizing the circuit configurations to minimize the effects of their relatively limited switching speeds. The second approach is to develop circuits capable of providing for reliable series-parallel operation of the switching devices in order to allow usage of lower power lower voltage devices which offer considerable improvement in switching speed.

A list of devices offering reasonable switching speed while having voltage breakdown capabilities of 50 volts or greater and current capabilities in the order of 0.5 amps and greater has been compiled and is included. It may be seen that the list is a relatively brief one. If one were to drop the limit on BVceo the list would increase quite rapidly. In addition, there is a reasonably large category of devices specifically designed and specified for RF amplifier and oscillator service. These devices have not been included as, in general, their performance in a switching mode is not defined and would require specific device evaluation in order to determine whether any of these type components are suitable for use in the present application.

Two particular devices on the accompanying list are of special interest, namely the SDT6103 and the SDT6112 manufactured by Solitron Devices, billed as 5 amp and 10 amp switching transistors respectively with 50 volt collector emitter breakdown ratings and switching speeds specified as 50 nanoseconds t_r and t_f for the SDT6103 and 75 nanoseconds for the SDT6112. These devices have a relatively low specified H_{fe} of 10, but this is not considered to be a serious drawback to their use in power conversion circuits since, in order to provide for bottoming or saturation of switching devices, it is usually deemed good practice to drive them

with collector to base current ratios in the order of 10. It should be noted also that field effect transistors may offer advantages for certain portions of the circuitry due to the absence of a charge storage mechanism and the resultant improvement in switching speeds. These applications would most likely be in relatively lower level portions of the circuitry due to the relatively low value of Igss and high value of ON resistance of most of these devices.

To summarize the situation as regards transistors for use in switching applications, there appears to be a limited number of devices which by specification would provide reasonable performance when used in relatively straightforward configuration; that is, without the need for series or parallel stacking.

Magnetic Component Design

The area of design of magnetic components, transformers, chokes, etc., has been reviewed in order to determine the most optimum materials for use in this frequency range and the most optimum configurations in which to use these materials. The choice narrows down almost immediately to three possible choices. These are very thin tape wound laminated cores available in toroidal configuration, powdered iron cores in toroidal configuration, and the various ferrite materials which are manufactured either in toroidal or cup core configuration. Other core configurations such as stacked laminations of various magnetic materials are excluded due to the fact that they are not manufactured and would not be workable in the extremely thin laminations that are required to allow reasonable performance at high frequency.

At the lower frequencies normally used for converter applications the tape wound toroidal cores usually offer the best compromise for designing high performance converters. In general, they have extremely high permeability, high saturation flux levels, good squareness ratios coupled with reasonably low losses at frequencies up to approximately 100 KHz. These properties begin to degrade as the frequency is raised, however, due to the relatively high conductivity of the continuous magnetic strip which allows the flow of eddy currents. This results in an increase in power loss within the core material and also in a decrease in effective permeability of the material due to the phenomena of magnetic skin effect which is simply an effective shielding of a portion of the magnetic media due to the flow of eddy currents. This phenomena is suppressed in the ferrite materials due to the relatively high resistivity of the magnetic material and it is possible to obtain ferrite cores having relatively flat curves of permeability versus frequency out to frequencies of many megahertz. What is available in practice is, in general, a series of materials optimized for use in different frequency ranges. In

general, lower frequency materials have higher initial and maximum permeabilities with the permeability rolling off at a lower cutoff frequency, and higher losses at the higher frequencies. As permeability is decreased the frequency range over which the permeability is maintained constant is increased and the losses at higher frequencies are lowered. It may be seen from this that once the choice is made to use ferrite materials, that additional choices are available in terms of selection of specific material type.

Disadvantages of the ferrite materials are that they have relatively low values of saturation flux density with typical values in the order of 3000 gauss, and in general, have low Curie temperatures. The first of these requires more turns to support a given voltage which is not a particular problem at the high frequencies involved since the number of turns is minimized. The second problem, the low Curie temperature, need not be a problem provided that the operating temperature range is kept within reasonable limits and these devices are designed in such a way that the internal temperature rise is limited.

At frequencies above approximately 100 KHz the ferrite materials appear to offer the best overall compromise of properties, with the thin tape wound cores perhaps being used for special applications. Of the various ferrite materials available those having properties equivalent to the Ferroxcube 3D3 material would appear to be the best choice for the usage under consideration. This material has relatively flat permeability out to 2.5 MHz, has a saturation flux density in the order of 3500 gauss and relatively low loss in this frequency range. Comparable materials are available from several manufacturers.

Once having chosen the optimum core material in the case of ferrites the next item for consideration is to determine the core structure which is most usable. In general, for a given effective core area, one should attempt to minimize the effective path length in order to reduce the magnetizing current, and minimize the volume of core material in order to reduce the core losses. Of the standard configurations available, the cup cores appear to offer the best compromise in terms of geometry and, of course, offer the added features of excellent shielding of the magnetic circuit, ease of adding or adjusting the air gap in applications where one is desirable, and in addition, are readily available and easily mountable.

A brief table follows which serves to illustrate this point. Typical cup core, toroid, and H core, configurations are listed with data excerpted from the Ferroxcube catalog. Listed are values for effective area, effective path length, the ratio of these two, and effective core volume.

	Ae	Le	Le/Ae	Vol.
		Cup Cores		
905	.101	1.25	12.4	.126
1107	.167	1.55	9.56	.251
1408	.251	1.98	7.89	.495
1811	.433	2.58	5.91	1.12
		Toroidal Cores		
266	.076	2.16	28.41	.164
768	.133	3.03	22.80	.404
846T250	.270	5.52	20.40	1.475
K300502	.373	7.50	20.1	2.58
		"H" Cores		
H10	.075	2.25	30.0	.17
H16	.349	3.57	10.2	1.24
H20	.47	4.12	8.8	1.93

It may be seen from examination of the list that for a given core area the cup core configurations have considerably shorter effective magnetic path lengths and core volumes than either of the other two configurations. It would obviously be possible to fabricate a toroidal core configuration having a lower path length to effective area ratio than the standard cores listed. It is felt, however, that the geometry chosen for the standard cores in each of the configurations are chosen for reasons of optimizing performance of the cores in the given configuration, and a deviation from these form factors would result in poorer performance. In general, at the higher frequencies, the wire losses are relatively small due to the low number of turns required to support the required voltages. Thus, it can be rather generally stated that core losses are the dominant loss factor in high frequency magnetic components. A similar situation exists in the trade-offs between leakage inductance and winding capacity with the small number of turns yielding capacity values which are not large in comparison to the inherent capacities of the switching and rectifying elements and the stray capacity of the connecting circuitry. As such, winding configurations which minimize the effective leakage inductance should be chosen. Minimizing the leakage inductance becomes especially important with the rapid transition times involved in efficient conversion at high frequencies since the voltage spikes produced by the rapid variations in current can reach significant amplitude and can readily cause damage to the switching devices if measures are not taken to suppress them.

The standard techniques for minimizing leakage inductance are the use of multifilar windings wherein a number of wires sufficient to produce the required number of coupled windings are wound together on the core resulting in close proximity of the windings and hence tight coupling. This results in a low value of leakage inductance. Where a dissimilar number of turns on the two windings occurs, such as is the case with collector and drive windings in a magnetic oscillator, or indeed, with any type of step up or step down application, the winding with the fewer number of turns should be spread as evenly as possible over the complete area encompassed by the larger winding. Use of a number of parallel strands of smaller wire in place of a single strand of larger wire can be used to improve the coupling between windings with a dissimilar number of turns as it allows more optimum interweaving of the two windings. Use of other standard techniques for minimizing leakage inductance such as layer winding wherein one winding is sandwiched between layers of the other winding are also useful if a sufficient number of turns are being wound to make this feasible. In general, considerably more care is required in analyzing each application for a magnetic component at the higher frequencies in order to optimize its performance.

An additional item which requires consideration when using ferrite cores is the problem of providing for adequate heat transfer from the winding and the core to some heatsinking surface in order to maintain the maximum temperature of the core below the relatively low curie temperatures of these materials.

Initial investigations also indicate that a somewhat more sophisticated design approach must be taken in designing transformers for these higher frequencies. In general, at the lower frequencies with tape wound materials the magnetizing current and core losses are sufficiently low that the usual practice is to minimize component size by using a relatively large portion of the flux swing capability of a given core. At the higher frequencies with relatively few turns required to support the voltage the magnetizing current becomes appreciable and constitutes a loss producing mechanism in that this current must be handled by the transistor switching element. For a given core this magnetizing element is a direct function of the total flux swing utilized. Stated another way, it is inversely proportional to the number of turns. It becomes obvious that the optimum design for a lower power handling transformer may occur with a number of turns greater than the amount required to just support the voltage. Coupled with this is the fact that the core losses increase as a function of frequency and flux level and the rate of increase is not a linear function of flux level. The significance of these statements is that the optimum configuration of a given transformer will vary with the application and power level. This, of course, has always been the case, but becomes increasingly important at the higher frequencies and thus, requires that more effort be expended in optimizing the transformer design.

The foregoing has a particular impact on the use of circuits such as the conventional magnetic oscillator wherein the core saturation is used as the timing element in a squarewave oscillator circuit where switching from one state to the other is caused by saturation of the magnetic core. Use of the core in this fashion, of course, dictates that the full flux capability of the core be used with maximum magnetizing currents and core losses for a given core resulting.

A further factor is that the materials used at the higher frequencies tend to have somewhat rounder hysteresis curves resulting in a more gradual onset of saturation and poorer switching characteristics. This coupled with the limited speed of the semiconductor switching device degrades the performance of the conventional oscillator circuit. This would indicate that in some situations the production of the timing functions by methods other than saturation of a main or auxiliary magnetic core may be the proper choice.

To summarize, it would appear that tradeoffs between achievement of minimum size, which dictates the use of the smallest core with the fewest number of turns, and maximum efficiency will, in some cases, require operation of the core at levels significantly lower than their maximum capability. This requires a larger core and/or more turns in order to reduce the flux levels and the losses.

Circuits

Duty Cycle Modulation Circuits

There are three main classes of duty cycle modulation circuits which are as follows:

(1) Phase control modulators - Duty cycle modulation may be produced by generating two waveforms, controlling the phase angle between them, and combining them such that the output is the sum of the two waveforms. If the phase angle between the two is then varied from 0 to 180°, the resultant waveform is a rectangular waveform having a duty cycle which varies from 0 to 100% or 100% to 0 depending on the choice of initial phasing.

(2) Magnetic duty cycle modulators - A duty cycle modulated waveform may be produced by placing a winding wound on a magnetic core, preferably of the squareloop variety, in series with an AC voltage. By varying the current to a control winding wound on the same core, the point at which saturation of the core occurs may be varied which in turn varies the percentage of the cycle which is blocked or fed to the load. Devices of this type may be used to produce a drive waveform for power switches or to control large amounts of power directly.

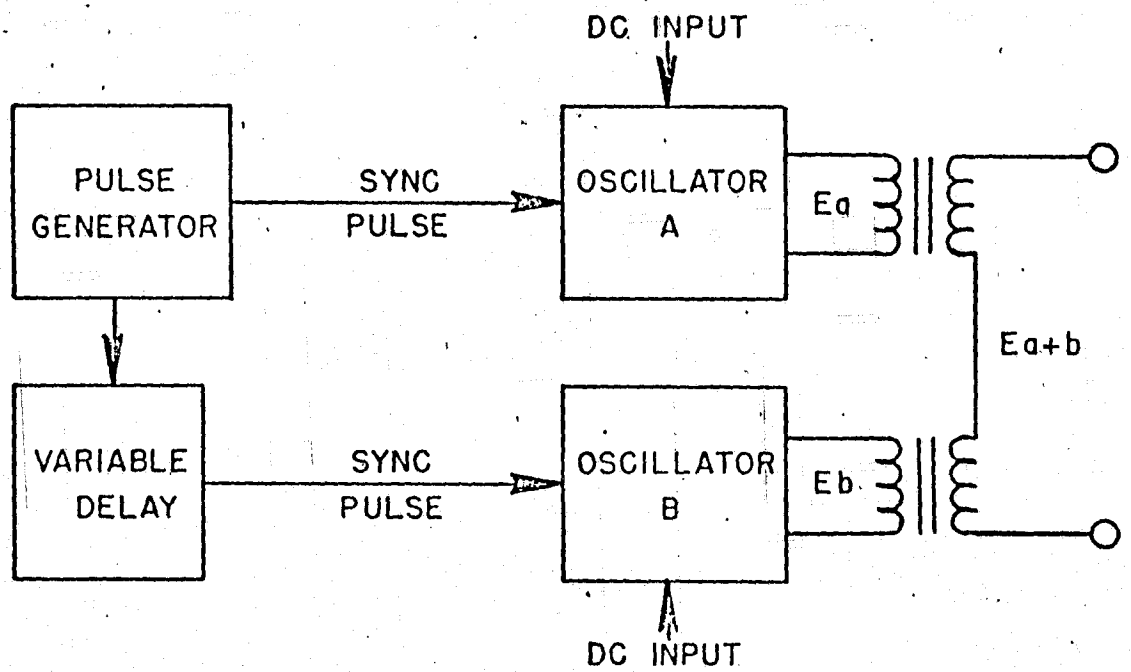
(3) Ramp and comparator - The ramp and comparator class of duty cycle modulators encompasses a wide variety of circuits which make use of a time varying waveform and a threshold detector to translate an amplitude variation to a time or duty cycle variation. Control of the duty cycle produced may be accomplished by varying either the slope or initial condition of the time varying waveform, or the firing point of the threshold detector or comparator. A wide variety of duty cycle modulators incorporating these basic features have been utilized in the past at lower conversion frequencies.

These three major classes will be discussed in the following sections.

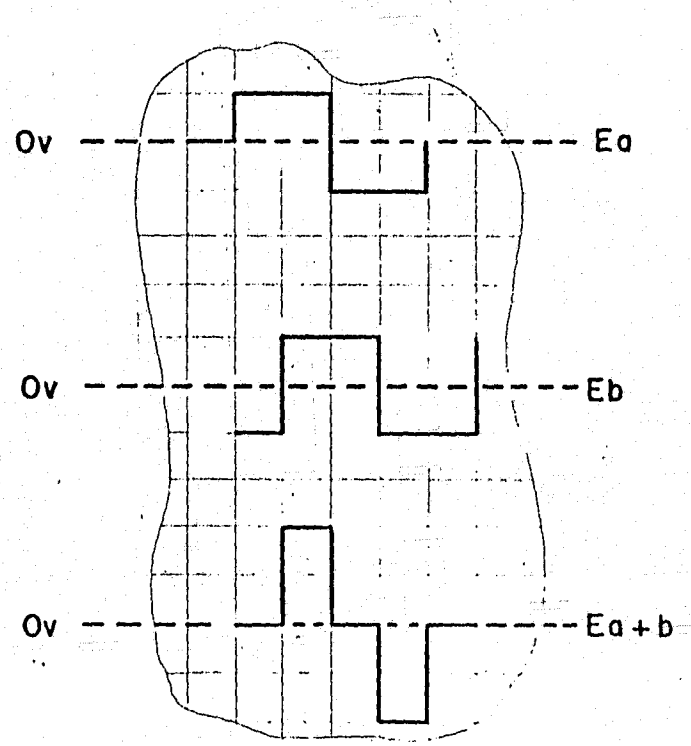
Phase Control Duty Cycle Modulators

One method of producing a phase controlled duty cycle is the two oscillator duty cycle modulator. This technique makes use of two conventional magnetic oscillators with output windings wired in series in such a way that in phase operation of the oscillators produces either full output or zero output depending on phasing of the output windings. By synchronizing the oscillators and delaying the sync pulse between them or by simply holding one and varying the frequency of the other by varying the voltage applied to it, a duty cycle modulated waveform can be produced. A simplified block diagram is included to demonstrate this operation.

The immediately obvious advantages are ease of producing zero to 100% duty cycle and extremely good low impedance output waveforms. The immediately obvious problems are the additional power consumption when operating two oscillators and the necessity of guaranteeing synchronization in a given phase in the case of the synchronized delayed configuration. A difficulty which is inherent to both the synchronized and free running variable frequency oscillator technique is that the slope of the control characteristic changes abruptly at 180°. To illustrate the point, if the oscillators are initially in phase then maximum output occurs when there is no phase shift and/or delay added. The output duty cycle then decreases linearly to a minimum at 180° of effective phase shift. A further increase in delay and/or phase shift results in an increasing duty cycle beyond this point. It can be seen from this that if the amount of delay is not strictly limited that the modulator can pass through this point and invert the sense of the loop, thus changing the desired negative feedback to positive feedback causing lockup at one limit condition or the other. This condition can be met by the addition of suitable gating to the controlled oscillator and this type of modulator can have merit since it provides fast, low impedance drive waveforms directly. Many variations on the above theme are possible.



SIMPLIFIED BLOCK DIAGRAM
PHASE CONTROL DUTY CYCLE MODULATOR



WAVEFORMS FOR THE ABOVE FOR 90° PHASE ANGLE

Figure 1. Phase control duty cycle modulator

Magnetic Duty Cycle Modulators

At lower frequencies the use of saturating magnetic components as switches to provide duty cycle modulated waveforms is relatively common and indeed offers some distinct advantages. Among these features is the relative ease of obtaining a wide duty cycle variation, the inherent ruggedness and power handling capability, the ability to incorporate multiple control windings which are electrically isolated, and a low sensitivity to higher frequency components of system noise since magnetic saturation occurs as a function of the integral of applied voltage. The disadvantages of such devices at lower operating frequencies are, of course, the relatively large size and weight, and the relatively low speed of response since in order to achieve significant power gain a relatively large number of control winding turns are required which reduces the speed of response due to the inductance of this control winding. Since operation at higher frequencies would minimize these two main negative features, it would appear that use of magnetic components as duty cycle modulators at higher frequencies would be feasible and indeed desirable.

Problems occur, however, when one attempts to implement these in a practical case. At the lower frequencies used for the predominant number of power converters presently in service, permeabilities in excess of 100,000 are obtainable while at the higher frequencies considered for this program permeabilities of a few thousand or less are more normal. Since the maximum on to off ratio of a magnetic component being used as a switch is limited by the permeability of the material, it may be seen that a 2 order of magnitude degradation in the on to off ratio may be expected when operating at the higher frequencies. This ratio is further reduced due to the higher core losses which produce an effective shunting resistance across a series gate winding. In addition, there is a distinct tendency for higher frequency core materials and lower frequency materials when operated at higher frequencies to exhibit a considerably rounder hysteresis loop. This results in a more gradual onset of core saturation and degrades the device's operation as a switch since a considerably larger portion of time is spent in the transition from high permeability high impedance area, to the low impedance fully saturated condition. As a result it is difficult to achieve waveforms with sufficiently fast transition times to be used as drive waveforms for power switching elements unless considerable wave shaping is included to sharpen the output obtained from the magnetic duty cycle modulator. A third factor is that the residual or remaining inductance subsequent to core saturation can constitute an appreciable impedance and significant voltage drop when appreciable amounts of current are being carried by the circuit.

These comments are intended to apply specifically to magnetic components used as gating or switching elements such as in the case of the conventional magnetic amplifiers. The general limitations outlined, however, apply to other usage of magnetic components as well. The above stated limitations can, of course, be minimized with careful choice of configuration and by the inclusion of circuitry to process the resulting waveforms, thereby allowing usage of this type of modulator when its specific characteristics would be of particular advantage.

One such configuration has been breadboarded and tested with fair results. This configuration consists of a standard magnetic amplifier configuration whose gate windings are connected in series between the output windings of a squarewave magnetic oscillator and the bases of the two converter transistors. The magnetic amplifier output is loaded by a two transistor equivalent of a tunnel diode. This circuit provides rather optimum loading for a magnetic amplifier in that peak point current of the circuit is adjustable and can be set to threshold above the OFF state current of the gate winding. In this configuration the magnetic amplifier functions more as a variable inductance which varies the slope of a current ramp feeding the level detector circuit and thus, the firing point of the level detector.

Ramp and Comparator

As previously stated most of the circuit type voltage to duty cycle modulators consists of some variation of the ramp and comparator scheme wherein some form of time varying waveform is compared to a reference by a comparator circuit which functions such that when the applied waveform is below the threshold level the output waveform remains in one state and switches to another state when the time varying waveform passes through the threshold level. The two state rectangular waveform thus produced has a duty cycle which varies as a function of the applied AC waveform its initial voltage level, or variations in the threshold level of the comparator device. The principal advantages of this type of duty cycle modulator are its ability to generate fast waveforms, the ease with which they can be tailored to different power levels and their relative freedom from ambiguities in the control function. Principal disadvantages are the relatively high susceptibility to high frequency noise and the added difficulty in providing isolation in the control function.

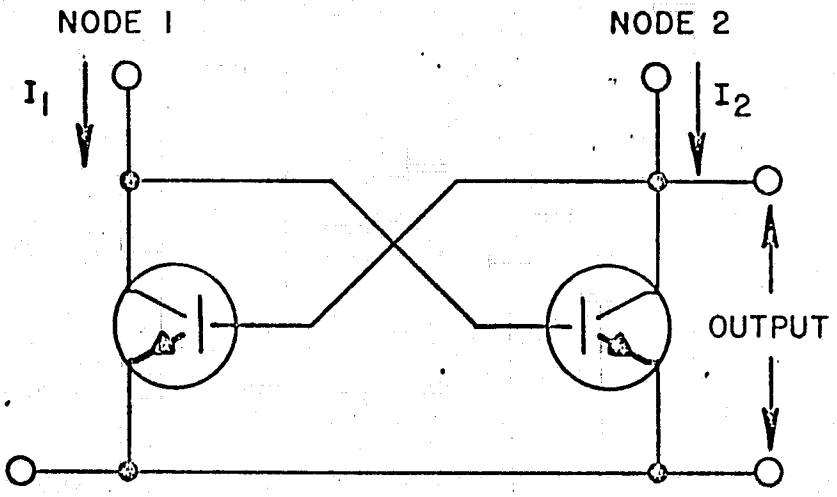
Among the criteria established for a duty cycle modulation circuit to be used on the existing program are that it have the capability of a wide variation in output duty cycle, that it be capable of being scaled to various power levels, that it have the minimum susceptibility to high frequency noise and that it ultimately provide a fast low impedance waveform capable of

driving the power converter switches directly. The low impedance requirement can be met in either of two basic ways; either the comparator can operate at a relatively low voltage and switch the required drive current levels directly or the comparison can be done at a higher voltage level and the waveform transformer coupled to the driven switches allowing the impedance transformation to be made in the coupling transformer. At lower operating frequencies the latter method has been rather extensively used since the transformers involved are relatively efficient and cause little waveform distortion. At the higher frequencies some of these advantages are partially negated by the reduced efficiency and the added difficulty in obtaining flat response from the transformer; that is, lack of overshoot, ringing, and deterioration of rise times. These problems are not sufficiently severe to preclude use of transformer coupling where the application dictates, such as when there is a requirement for isolation which cannot conveniently be handled by other means.

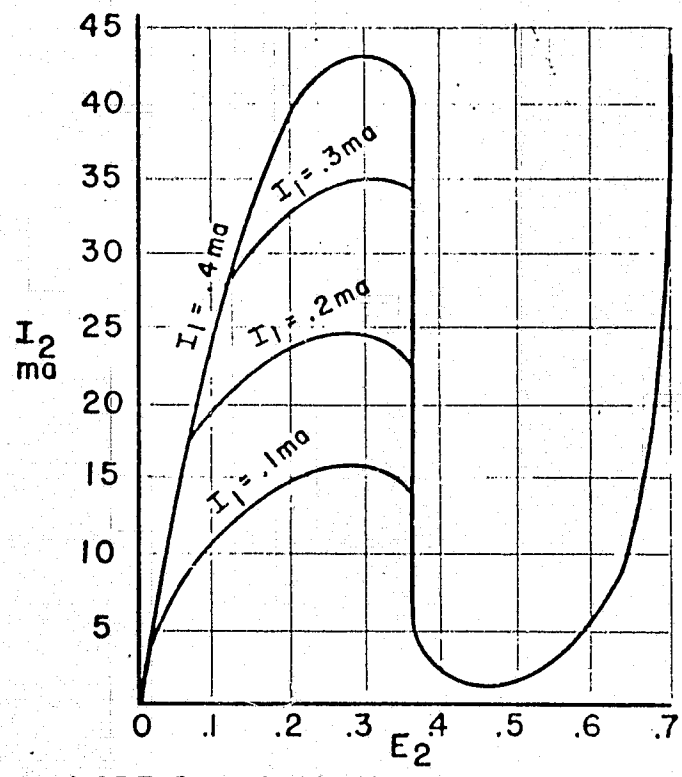
In general, it is felt, however, that the generation of the duty cycle modulated waveform which is to control the power switches should be accomplished as close as possible to the point of end use. Stated another way, there should be a minimum of power amplifying stages or coupling circuitry between the duty cycle modulator and the driven switches. This is due to the fact that each successive handling of the high speed waveform results in additional power loss, additional noise generation, and additional time delay built into the loop, all of which worsens the loop stability problem and makes the achievement of a smooth transition down to zero duty cycle increasingly difficult to achieve. This is due to the fact that significantly longer delays are encountered in attempting to turn off switching devices as opposed to turning on due to storage phenomena.

A circuit which possesses many of the attributes described above and which is simple and quite versatile is a two transistor circuit which displays behavior somewhat analogous to a tunnel diode.* In its simplest form it consists of two transistors of the same polarity with their collectors and bases cross coupled. If a varying current is applied to one of the joined collector base nodes, the device will exhibit a positive resistance characteristic up to a given current after which it will exhibit a negative resistance characteristic until a minimum current is reached and then again appears as a positive resistance with the characteristic determined by the base emitter diode of the opposite transistor. The peak point current, or the current at which the characteristic becomes negative, is determined by the current which is flowing in the opposite node.

*This circuit has been reported in the literature.



TWO TRANSISTOR LATCH EXHIBITING
NEGATIVE RESISTANCE CHARACTERISTIC



NODE 2 V-I PLOT VERSUS NODE 1 CURRENT

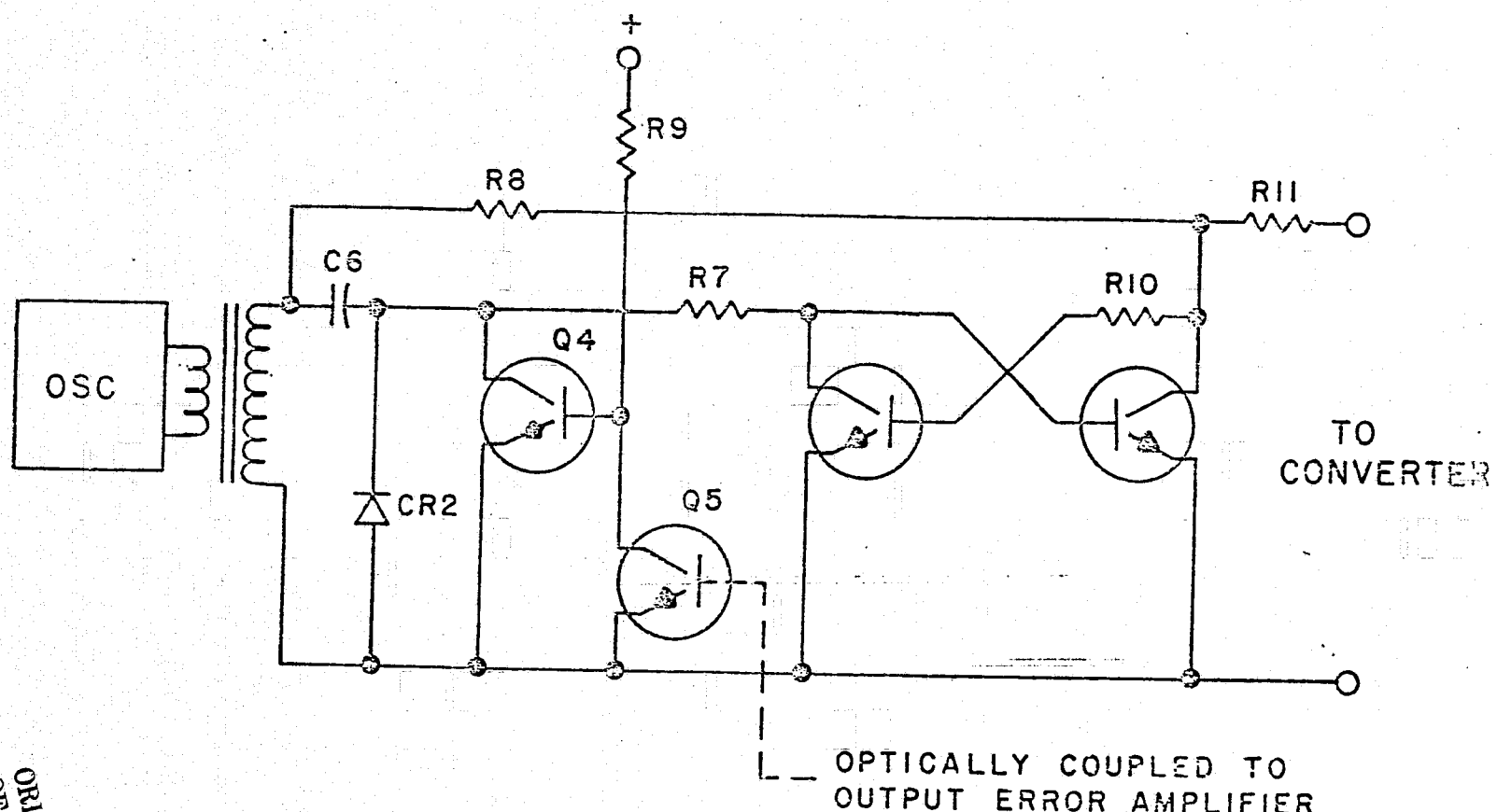
Figure 2. Schematic, two transistor latch

This circuit has a number of good features including the capability of extremely high speed switching since very fast low voltage transistors may be used and the circuit operates at a high current or low impedance level with small voltage changes involved, thus minimizing the effects of the device and stray capacity. The peak point or firing point of the device may be programmed over a wide range of currents by simply programming the current flow into the opposite node.

An additional feature of the circuit is its versatility. For instance, an AC or ramp waveform may be applied at the working node and a DC control voltage applied to the opposite node in order to vary the duty cycle. Alternately, a DC voltage may be applied to the working node and an AC waveform to the opposite node and the amplitude or DC bias of this waveform may be varied to vary the duty cycle. The circuit functions equally well at low or high operating currents and by the addition of one cross coupling resistor between the main operating node and the opposite base, the output voltage swing may be increased in order to provide sufficient swing to drive a converter transistor on and off. Since the circuit is DC coupled, there is no recovery time, or stated another way, no minimum time which the device must spend in a particular state such as is the case with many AC coupled circuits. This particular circuit configuration out of the total number investigated seemed to offer the most promise as a circuit type high level duty cycle converter and was used in the resultant breadboard in conjunction with the converter configuration discussed in the following section.

Converter Circuits

Work during this project has concentrated on two transistor driven switch converter configurations. Advantages of this type of converter include maximum transformer utilization, since the current flow is essentially balanced in two halves of the primary winding, allowing operation of a core over its full flux capability, and its ability to operate at or near 100% duty cycle. The principal disadvantage of this type of converter is that storage time of the typical device delays turn-off of the ON transistor with the result that both transistors may be on at the same time, resulting in large current surges and possible failure of the switching devices. This problem may be minimized by configuring the drive circuitry to provide fastest possible turn-off time and by restricting the maximum duty cycle to something less than 100% such that turn-off of one device prior to turn-on of the other is guaranteed. Active gating can be incorporated if required which senses turn-off of the ON device and inhibits turn-on of the opposite transistor until turn-off is accomplished. A second technique which may be used to alleviate the crossover problem and which also tends to reduce the power loss in the switching device during the switching interval is to incorporate a small



SCHEMATIC - DUTY CYCLE MODULATOR

Figure 3.

choke in series between the switching element and the main power transformer. This choke blocks the flow of current for sufficient time to allow the transistor to make the transition from ON to OFF state after which it saturates allowing the normal flow of current to the main power transformer and consequently to the load. Obviously, these improvements are gained at the expense of an additional magnetic component with its attendant losses and additional size and weight. The component, however, can be quite small since it is required to block current flow for a relatively small portion of the cycle.

Optimization of the converter chosen for any given power level consists of selection of the switching devices, design of the power transformer selection of the drive circuitry, and selection of the converter configuration.

Two distinct type converters are ultimately required to meet the requirements of this study program. The first of these is a high power converter yielding output powers in the order of 200 KHz and the second is a lower power device yielding output powers of approximately 20 watts total and operating in a frequency range of 1 to 5 MHz. watts at 200kHz

Due to the relatively low input voltages and the high power required of the spacecraft type converter, concentration was placed on optimizing the performance of a conventional push-pull driven converter. The basic configuration is shown on the attached schematic and is described as follows. The converter consists of a pair of SDT6115 which is a 10 amp 50 volt VCEO fast switching NPN device manufactured by Solitron Devices. These transistors provide push-pull drive to a center tapped transformer wound on a Ferroxcube Corporation 1811 size ungapped pot core of 3D3 material. The transformer is configured as a simple auto transformer since the 2 to 1 step-up thus provided is adequate for the purpose. Four eight turn windings are wound one on top of the other once across the bobbin. Alternate layers are then connected in parallel and in turn connected in series with the other pair in order to form the push-pull winding. Interweaving of the windings in this fashion minimizes the leakage inductance and, consequently, maximizes the coupling between windings.

The main drive to the converter is provided by means of a current transformer with its primary windings connected in series with the emitter of the switching transistors. A base drive winding with a step-up of 5 provides a base current to collector current ratio of 5 to 1. An additional step-up winding is provided to allow the drive circuitry to operate at a higher voltage lower current level.

Use of current transformer drive is desirable due to the saving in drive power and the fact that the drive level can be maintained at a fixed ratio to the current being drawn through the switch transistor. This results in an optimum drive current over

a wide variation in collector currents and temperature, which provides for adequate saturation of the switching device while minimizing the storage problem to the greatest extent possible. Drive power saving is realized since the level of drive current is controlled by the transformer ratio. This eliminates the need for producing a quasi current source by using a higher drive voltage and series limiting resistor.

Another advantage of this technique is that it is essentially regenerative. Voltage gain around the drive loop enhances switching if the effective load on the converter switch is capacitive or resistive.

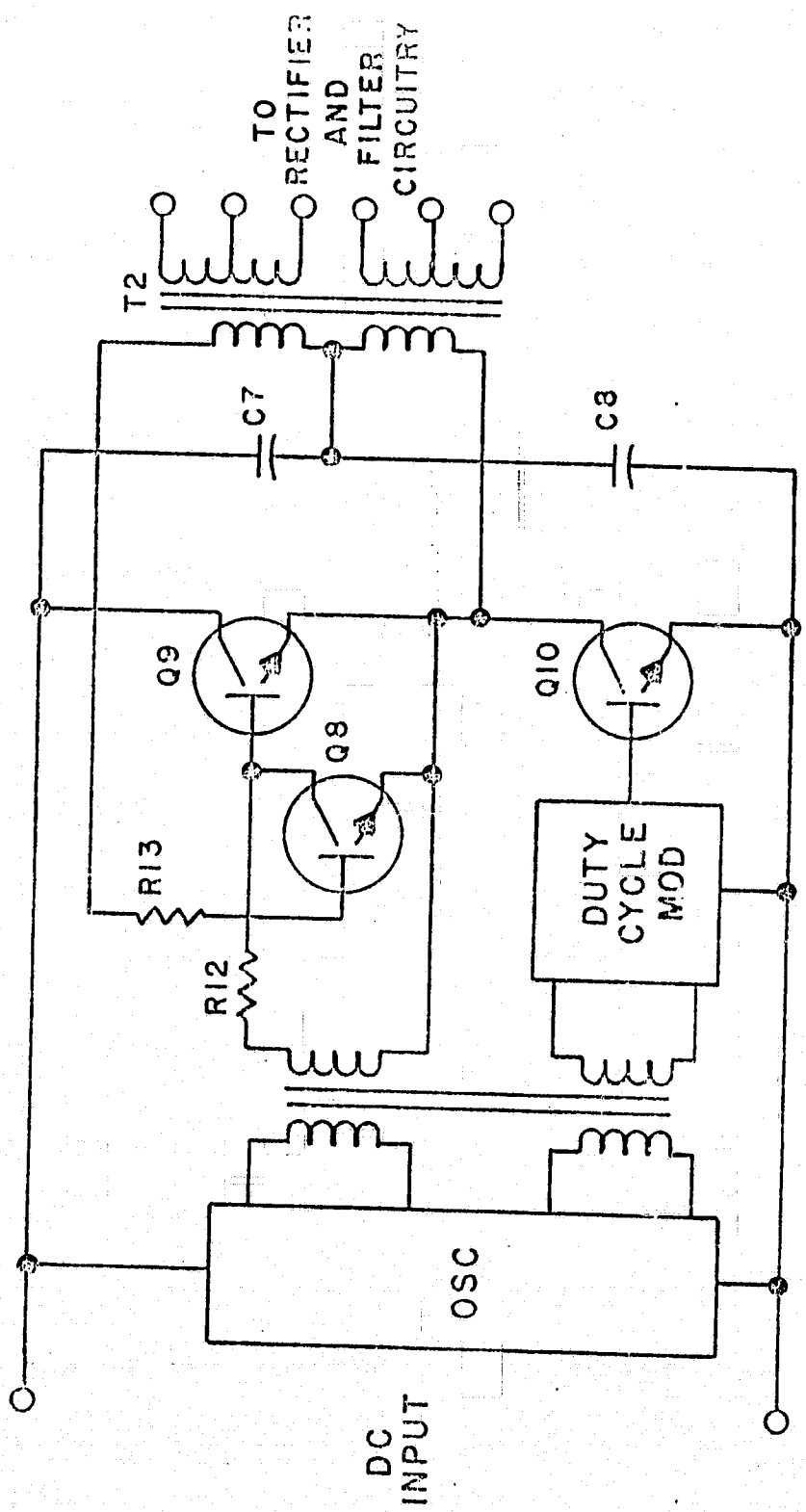
The output of the converter is rectified with a standard full wave rectifier using a center tapped transformer and fed to the input of an L/C averaging filter.

The circuit as configured is a straight boost type regulator which was chosen due to the fact that the output voltage required is higher than the maximum input line specified. This configuration yields the maximum efficiency obtainable due to the fact that only a portion of the output power is handled by the converter. It may be seen that the combination described above yields a complete power module requiring only the input of a power bus and relatively low level drive signals. As such, it lends itself readily to parallel stacking. A number of similar modules could be connected in parallel and driven from a common duty cycle modulated waveform and their outputs summed directly without the necessity of any additional circuitry to force current sharing.

For the lower power converter, some form of buck-boost configuration was dictated by the fact that the input line varies above and below the required main output of 28 volts. This coupled with the fact that isolation is a requirement between the input primary power and the output power dictates that the output power be taken from secondary windings on the transformer. The boost is provided by transformer step-up and the converter is duty cycle modulated to lower the output voltage to the required value.

A number of configurations were evaluated for this application including the standard push-pull circuits with the primary connected to the collectors and again with emitter drive. A circuit which seems to have particular merit for this application is shown in the enclosed schematic and described below.

The converter circuit is configured as what might best be described as a half bridge. It is similar to the standard bridge type inverter used frequently at lower frequencies except that one side of the bridge is replaced with passive components, namely, capacitors.



SCHEMATIC – CONVERTER CIRCUIT

Figure 4

The bridge configuration is chosen due to the reasoning previously described in that the best switching devices known to be available at the present time would have insufficient or at best marginal voltage ratings for operating over the prescribed line swing in a configuration which required the switch to handle in excess of twice the DC input voltage. Choice of half bridge configuration wherein the transformer primary current flows through the filter capacitors is made feasible due to the fact that at the high converter frequencies used, the value of capacity required is sufficiently small to allow the use of available monolithic ceramic capacitors. It should be pointed out that similar currents must be handled by the energy storage capacitors in any scheme involving duty cycle modulation.

An added feature of the circuit configuration is that due to the AC coupling to the primary of the transformer, saturation effects due to asymmetry in the drive waveform are eliminated. An advantage is taken of this fact in that only one of the converter switches is duty cycle modulated. The voltage at the junction of the filter capacitors then shifts to force an equal time voltage integral to be produced across the transformer by the upper switch.

The overlap problem, that is, both transistors on at once, is effectively eliminated by addition of a clamp transistor in the base drive circuit of the upper switch transistor which is driven by a winding on the main power transformer. The phasing is such that when the bottom switch is on, the base of the clamp transistor is positive which drives it on clamping the drive to the upper switch. On the other half cycle, overlap is prevented by limiting the maximum duty cycle to less than 100% by an amount equal to the storage and turn-off time of the upper transistor.

Rectifier Circuits

In general, the rectifier circuits used at higher frequencies would be identical to those used at lower frequencies for a given power level and input voltage. In general, the majority of rectifier circuits used at nominal voltage and medium to high current would be standard full wave, driven from a center tapped transformer winding. Diode bridge type rectifiers might be used in higher voltage, lower current applications; and in the case of lightly loaded outputs, single phase half ~~way~~ WAVE rectifiers could be used. The major variation between rectifiers for various usages would then be the type of diode selected. For the very low voltages, especially in the five volt category on up to perhaps 15 volts, the Schottky barrier type majority carrier rectifiers would be most useful at higher currents. These devices have relatively low forward drops for a given current and being majority carrier devices do not suffer from the forward and reverse recovery phenomena evidenced by PN junction diodes. The limitations as stated in the section on components and materials have to do with the relatively limited reverse voltage capability

which, with the present day devices, is approximately 40 volts and the relatively high junction capacity which leads to capacitive currents of a reasonably high magnetude which can produce losses if improperly handled.

For the somewhat higher voltages, the group of devices manufactured by ion implantation techniques yield very fast recovery times and relatively lower forward drops when compared to conventional PN junction diodes operating at the same current level. At still higher voltages, conventional PN junction diodes must be used. Modern devices offer recovery times approaching those of the more exotic devices mentioned above and in addition offer somewhat improved forward voltage drops when compared with similar older type devices primarily due to the improved means of connecting the die to the terminals of the package.

All of the devices discussed have in common the ability to withstand large short term current surges. This becomes somewhat more important at the higher frequencies due to the fact that the magnitude of capacitive current spikes is, in general, increased.

Filter Circuits

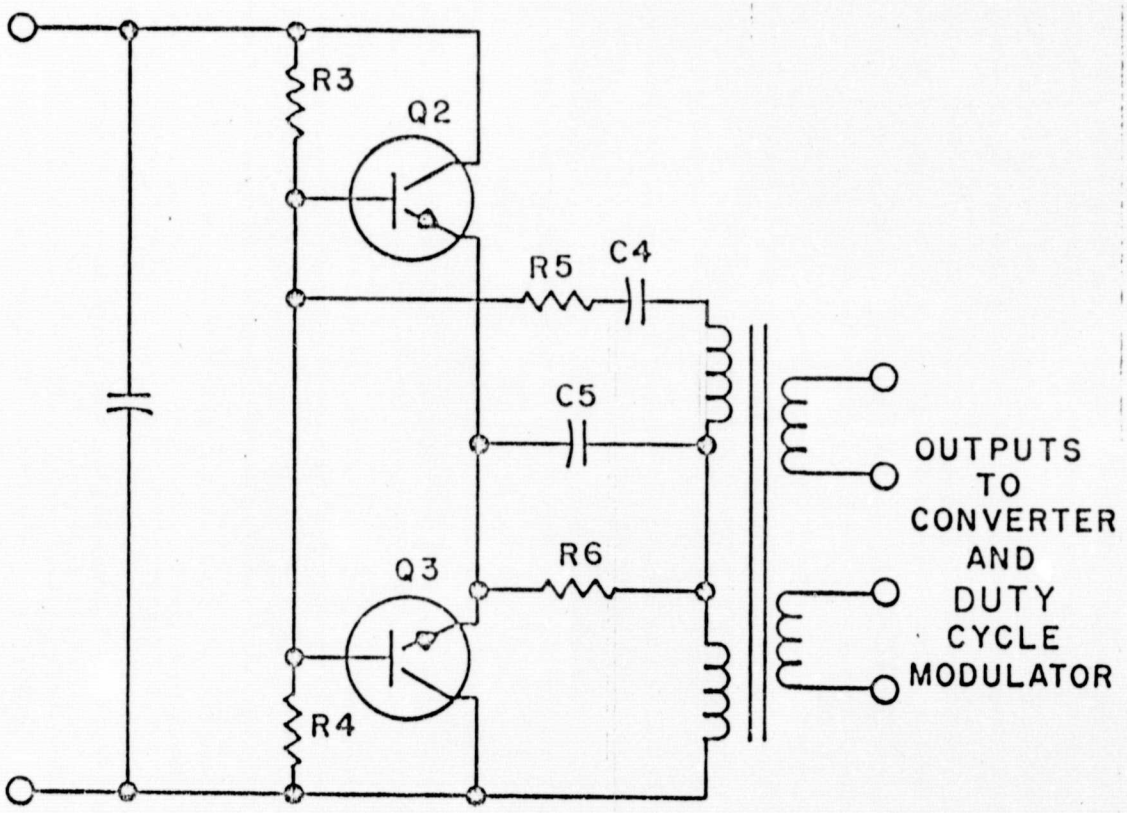
The filters required by any converter operating in the one and a half to several megacycle region assume added importance due to the fact that considerably more energy appears at higher frequencies in the spectrum to be filtered. Therefore, the filter networks must be designed to have excellent high frequency performance. In general, this simply means that the filter chokes must be wound on high frequency core materials and must be wound in such a way as to have maximum self-resonant frequency. The bypass capacitors must be dielectric material having good high frequency performance and physical structures which result in a minimum of series inductance. In general, the chokes should be wound on the lower permeability powdered iron and/or ferrite cores. The windings should ideally be configured to yield minimum shunting capacity leading to higher self-resonant frequencies. Other components having considerable utility at these frequencies are the varieties of small ferrite beads, of both the single and multiple aperature types obtainable from ferroxcube and other manufacturers, and many of the feedthrough types of coaxial capacitors and filter assemblies normally utilized in high frequency work. The ferrite beads are especially useful in that they can be placed on component leads or on interconnect wires and provide reasonably flat attenuation over a wide band of frequencies. The importance of maintaining solid ground nodes and minimizing the area of loops in which appreciable current is flowing cannot be overstated. Final bypassing of the input and output lines at the interface of the shield structure is usually necessary.

Oscillator Circuits

Numerous types of oscillator circuits were evaluated including the conventional two transistor oscillators using magnetic saturation as the timing element. As discussed in previous sections, the penalty for operating magnetic devices at saturation levels is more severe at the higher frequencies utilized in the study program. As a consequence of this, other techniques were evaluated which would result in suitable drive waveforms which could be produced without saturating the magnetic elements involved. Numerous approaches, making use of a separate oscillator driving a pair of transistor switches which, in turn, drive the transformer, exist. Any of the conventional forms of astable multivibrators and/or sinewave type oscillators could be utilized as the main timing element. While useful, all of these techniques result in added complexity and more components. A circuit which overcomes most of these difficulties and is relatively simple and reliable is shown in the accompanying schematic.

The oscillator consists of a complementary pair of transistors connected in series with their bases and emitters tied together. The output is taken from the emitters and capacitively coupled to the oscillator transformer in order that symmetrical drive may be applied to the transformer with a single ended supply. A base drive voltage is taken from a higher voltage tap and capacitively coupled to the bases of the oscillator transistors. This capacitive coupling accomplishes a number of things. First, it allows proper starting of the oscillator due to biasing current through R3 without the need of adding diodes, with their resultant drop and recovery times, in series with the drive winding. Secondly, the common connection of the two bases and use of the common drive circuitry minimizes the crossover or overlap effect since charge storage in the ON transistor clamps the base drive voltage during the recovery period and delays turn-on of the other device. The third and primary advantage of capacitive coupling of the base drive is that it allows the coupling capacitor to be used as the oscillator timing element with the frequency being determined by the capacitor value and the net impedance into which it couples. This allows timing to be accomplished without the necessity of saturating the oscillator core which results in significant savings in power. Oscillators of this type capable of switching 100 milliamps have exhibited no load current drains in the range of 5 to 8 milliamps at 1 MHz and voltages in the range of 20 to 30 volts. This is somewhat high by low frequency standards, but is relatively good by comparison with other configurations investigated at the higher frequencies.

The circuit configuration has two other important advantages in that it limits the voltage across either of the switches to the input DC voltage applied; and due to the solid clamping of the



SCHEMATIC – OSCILLATOR CIRCUIT

Figure 5.

primary to either ground or the DC bus line, the circuit exhibits little or no transient overshoot which would add to the voltage breakdown and noise problem if it were present.

In the circuit as shown Q2 and Q3 are the switch transistors. R3 provides starting bias, R6 provides the path for the initial current flow during the startup, R5 is drive limiting, C4 the base drive and timing capacitor, C5 the output coupling capacitor and R4 is added to provide symmetrical output waveforms.

It should be noted in passing, that the circuit as shown is capable of a reasonably wide variation in the symmetry of the output waveform and as such can produce duty cycle modulated drive waveforms by effectively varying either R3 or R4.

Configuration

The choice of the overall configuration is, in many respects, dictated by the specifications. If the input power bus line voltage goes above and below the required output voltage or voltages, then it is obviously necessary that some form of buck-boost configuration be used. In the special situation where the input voltage is always less than the output voltage and isolation between primary and secondary common is not a requirement, it is then possible to use a boost type configuration yielding in general higher efficiency since only a portion of the power is handled by the converter circuit. A third situation exists in which the input voltage is always higher than the required output voltage and again if isolation is not a requirement then it is possible to build a switching regulator of straight buck configuration, and in this case the power transformer can be eliminated entirely.

In addition to this basic choice, several choices of circuit configuration are possible. A switching type bus line regulator could be used followed by a converter. Alternately a converter could be used to chop the input bus line directly and this in turn followed by multiple switching regulators. Thirdly a duty cycle modulated converter could be used to perform both the function of conversion and regulation. All of these configurations are used at lower frequencies with the choice depending upon other circuit requirements such as the number of outputs, power level, degree of output regulation required, amount of load variation and speed of response required as well as efficiency required. At the high conversion frequencies being used in the present program, the relatively high contribution of the switching losses to the overall circuit losses would seem to dictate the switching of power being undertaken the minimum number of times possible. Therefore, the configuration most commonly chosen would be one which uses a duty cycle modulated converter to perform the dual functions of conversion and regulation. The primary disadvantage of this choice of configuration is that if a large number of outputs are required from the converter, then

each output must incorporate a filter capable of averaging the relatively large amplitude duty cycle modulated waveform. This disadvantage is, to a large extent, minimized by the fact that at the high frequencies the value of the components required to perform filtering is relatively small, and for a reasonable number of outputs, would not increase the size and weight by an inordinate amount. If a large number of outputs having relatively low power are required from the converter, the previously described approach using a switching bus line regulator followed by a square wave converter would be the logical choice.

Reliability Considerations

The reliability considerations which must be taken into account for converters operating at the higher frequencies are similar to those of the lower frequency converters. The main difference is found in the degree of difficulty of determining the exact stresses which will be applied to the various components. As an example, the voltage spike produced at the collector of the switching transistor utilized in a converter application, could vary appreciably with minor variations in the winding configuration of the converter transformer, the speed of the base drive waveform, which is determined by the oscillator and/or duty cycle modulator circuitry, and even the placement of interconnecting leads.

A similar situation occurs in the calculation of power dissipation within the various devices used in the converter. In the lower frequency case, the switching losses are a relatively small fraction of the total losses and the power loss calculations are much more dependent on the steady state losses and thus more easily calculable.

The fact that the higher frequency components tend to have lower breakdown voltages, makes it somewhat impractical to derate to the extent which can usually be readily obtained at lower frequencies. Stated another way, at the lower frequencies very little penalty is usually paid for derating the breakdown voltage of a converter transistor by factors of 3 or 4. This is in excess of that which is normally required but generally makes a circuit tolerant of reasonable variations in the transient spikes appearing across the switch transistors. A similar situation exists with many of the other components. For instance, the power losses in the rectifying diodes in the low frequency case are primarily due to the forward IR drops whereas at the higher frequencies the current flowing during the forward and reverse recovery times generates significant power losses and must be included in the calculation. The area of magnetic components is somewhat of a mixed bag in that the wire losses are materially reduced for a given current level due to the fact that considerably fewer turns are required to support the voltage. At the same time, however, the core losses are significantly increased and, in general, the size of the component for a given

power level is materially reduced. This leads to the possibility of a higher power density, that is watts per units volume, within the magnetic components. There are many variables in this case and the ultimate situation will depend on the configuration chosen. The flux level, and consequently number of turns involved, effects the ratio of core to winding losses. The actual speed of the waveforms applied to the magnetic device and, of course, the current and voltage levels being handled also effect the total losses.

On the negative side, the considerably lower curie temperatures of the ferrite materials makes it necessary to maintain the temperature rise within lower limits. On the positive side, the fact that an increased amount of the heat is inherently generated in the core material itself as opposed to being buried within the winding layers allows one to provide a much lower resistance thermal path between the heat generating component and the heat sink surface. In general, the fundamental difference would be that at the higher frequencies a definite attempt to tie the physical core structure of the power handling magnetics to the heat sink surface would generally be indicated. This can be done, of course, very readily in the case of the pot core assemblies since they have relatively large area flat surfaces and means for mounting the core directly to the frame. With the toroidal devices, such as are commonly used in the choke assemblies the thermally conductive resins such as epoxies filled with oxides are useful.

In general, a very careful attention to layout details is important in order to minimize the stray capacities and consequent large amplitude transient current spikes. Despiking networks consisting of small capacitors with series resistors may be used to limit the amplitude of voltage spikes. Ferrite beads connected in series with other inductors tend to limit the high frequency currents flowing in the distributed capacity of the inductors and minimizes the spikes produced.

The other main area of difference between the high frequency converters and low are that once all of the above is taken into consideration from a design standpoint it is necessary to do additional detail testing on each individual converter. It is necessary to do sufficient scope checking at various circuit points to determine that the as built unit is similar to the as designed unit. This is necessary in order to insure that the design derating is maintained.

Blue-Sky Approaches

The most straightforward approach to obtaining high efficiency at high converter frequencies is, of course, to use the fastest possible devices and circuit techniques leading to the fastest possible switching time, yielding a minimum power loss due to switching.

In theory, at least, there are other alternatives. All of these alternatives would consist of some form of isolating the load from the switching device during the switching interval. Any means of shifting the phase of the current with respect to the voltage and/or delaying the application of the switch voltage to the current drawing load should result in a decrease in switching losses. Means to accomplish this can be as simple as placing an inductor in series between the converter switches and the load transformer or as complex as attempting to design delay producing structures such as LC ladder networks which could be placed either in front of or made an integral part of the transformer itself.

Another possible approach which was considered was the use of parametric coupling; that is, the technique of coupling power to a load by modulating the reactance of the converter transformer. With this technique the primary and secondary windings of the transformer are oriented such that there is no direct magnetic coupling and the reactance of the secondary winding is caused to vary by driving its core material to or near saturation by means of flux produced by current flowing in the primary winding. The secondary circuit is resonated and useable power can be coupled in this manner with excellent isolation between the primary circuitry and the load. This technique is utilized in low frequency regulating transformers and has been described in the literature.

The third possibility which was considered was the use of multiple taps and switches such that the overall switching was accomplished in a series of lower amplitude increments in order to minimize the capacitive current flow during the switching transition. A reasonable amount of effort was expended in checking out the above possibilities and more, but none of these approaches ultimately led to performance levels equal to or better than that which could be obtained with the more straightforward fast switching interval approach. For this reason a detailed discussion of this effort is not included.

Instrument Converter

Introduction

The general guideline chosen for the design of an instrument type converter was that it be a practical design; that is, a design which provides useable, reliable performance utilizing components which are known to be available at the present time and which could reasonably be expected to yield repeatable and reliable performance in the circuit configurations chosen.

As was originally suspected and subsequently confirmed, the area of greatest limitation in terms of components has been the area of switching transistors which must handle either relatively high currents and/or reasonably high voltage. With the normally encountered excursions in input power bus lines which range up to 32 volts as a steady state input level, any of the traditional converter circuits which impose a voltage across the switching device of twice the input line voltage do not lend themselves to use of available devices having really good switching characteristics, for it is generally true that higher switching speeds and lower maximum voltage ratings go hand in hand. This particular situation is also aggravated by the fact that with the extremely high speed of the waveforms generated in such applications large amplitude voltage spikes are readily generated unless extreme care is taken to minimize such generation or to clamp them once generated. It was, therefore, a primary consideration that circuit designs which minimize the voltage applied across the switching elements be used insofar as practical.

A second criterion dictated by the requirement for a practical design, is that the control circuitry be capable of providing operation over a relatively wide range. Specifically, the duty cycle modulation and feedback amplifier combination must be capable of providing duty cycle control from near 100% to full off or 0%. The requirement for high duty cycle is less important than that of smooth operation down to or approaching zero duty cycle. The latter requirement is important in order to provide dependable current limiting in the switching mode in order to protect the converter from overloads appearing on its output. The necessity of obtaining a maximum duty cycle is somewhat diminished at the higher frequencies due to the ease with which the required filtering can be accomplished. In some cases the maximum duty cycle may be deliberately limited in order to preclude both transistors in a two transistor converter being on at once thereby causing large transient current flow, with subsequent power loss and possible damage to the switching device.

A third item which appears desirable when operating at these high frequencies is to eliminate insofar as possible operation of magnetic components in saturation. In addition to the obvious increases in power loss produced by regular saturation of the magnetic element such as is the case with the standard magnetic

oscillator, an increase in the total RMS noise level would occur due to the higher percentage of time spent at or near the saturation region.

A fourth aspect which should be considered is that one of the primary motives behind operation at higher converter frequencies is the reduction in size and weight of the ultimate unit. It is, therefore, deemed desirable that the circuit design be kept as simple as possible with a minimum component count in order that the reduction in size and weight due to the higher operating frequency not be negated by additional component count due to circuit complexity. The specific operating target specifications for the sample converter are listed below. A design was undertaken aimed at meeting these requirements and in accordance with the above discussed guidelines. The resultant circuit is shown in the accompanying schematic and discussed below.

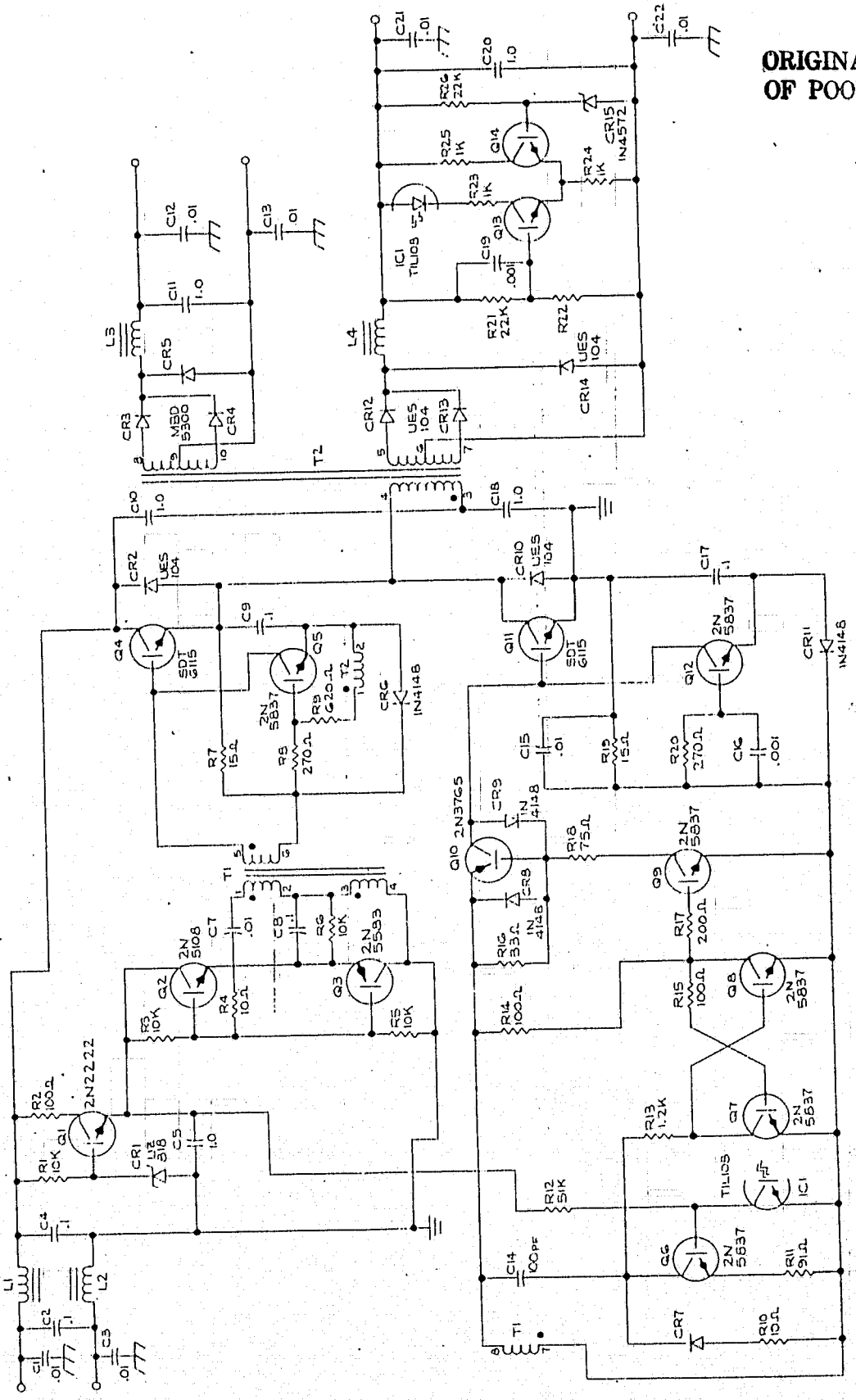
Specifications and Goals for an Instrument Type Converter

Input voltage range	28 ±5 V.D.C.
Outputs	
1.	28 V.D.C. ±0.25%
2.	3 V.D.C. ±1.0% (1A)
Regulation	As above for 50-100% load and line variations as above
Ripple	20 M.V.P.P. Max.
Output power	20 W total
Efficiency	>85%
Operating frequency	Fixed frequency in range of 1-5 MHz
Frequency variation	±5% line load and temperature -10 to +50°C
Overload protection	Limit to 150% of normal output
Source ripple	Minimize
Operating life	5 to 10 years in space environment
Operating temperature range	-40°C to +100°C

Goals: Design for minimum size and weight; minimize input line turn-on current transients; good transient response; low conducted and radiated E.M.I.; and self-starting capability.

Circuit Configuration

Several choices of circuit configuration are possible for the application. A switching type bus line regulator could be used followed by a converter. Alternately, a converter could be used to chop the input bus line directly and this, in turn, followed by multiple switching regulators on the two outputs or thirdly, a duty cycle modulated converter could be used to perform both the function of conversion and regulation. All of these configurations are used at lower frequencies with the choice



SCHEMATIC - INSTRUMENT CONVERTER

Figure 6

depending on other circuit reguirements such as number of outputs, power level, degree of output regulation required, amount of load variation and speed of response required as well as efficiency requirements.

At the high conversion frequencies being used in the present program, the relatively high contribution of the switching losses to the overall circuit losses would seem to dictate that switching of the power being handled be undertaken the minimum number of times possible. Therefore, the configuration chosen for the instrument type converter is one which uses a duty cycle modulated converter to perform the dual functions of conversion and regulation. The primary disadvantage of this choice of configuration is that, if a large number of outputs are required from the converter, then each output must incorporate a filter capable of averaging and smoothing the relatively large amplitude duty cycle modulated waveform. This disadvantage is to a large extent minimized by the fact that at the high frequencies the value of the components required to perform filtering is relatively small and for a reasonable number of outputs would not increase the size and weight by an inordinate amount.

Choice of some form of buck-boost regulator was dictated by the fact that the input line varies above and below the required main output of 28 volts and the fact that isolation is a requirement between the input primary power and the output regulated power. The boost is provided simply by transformer step up and the converter is duty cycle modulated to lower the output voltage to the required value. The circuit as shown consists of a squarewave oscillator which provides the timing and drive waveforms, a duty cycle modulator which converts the output of the feedback amplifier to a duty cycle modulated waveform, a power converter which chops the DC input in order to allow transformer coupling to the required output, rectification and filtering circuitry, and a feedback amplifier which compares the output voltage to a reference voltage and amplifies the result to provide proper control signals for the duty cycle modulator.

Circuit Description

The circuit configuration for the instrument converter is shown on the enclosed schematic diagram and described in the paragraphs below. Input power is fed through an input filter consisting of L1, L2 and main filter capacitors C10 and C18. C2 and C4 provide high frequency bypassing and C1 and C3 provide bypassing to the housing. Q1 and CR1 form a simple dissipative regulator to provide stable operating bias to the timing oscillator. This oscillator consists of a complementary pair of transistors Q2 and Q3, and is configured in the capacitively coupled configuration described in the previous sections. As stated in that section, the timing for the oscillator is accomplished by the time constant of coupling capacitor C7 and the net impedance, including R4 and the input resistance of the converter

transistors. Oscillator transformer T1 is thus not saturated. As stated in the previous section, the principal advantages of this oscillator circuit, in addition to not requiring saturation of the transformer, are the fact that the transistors see a voltage equal to the bus line voltage as opposed to twice that in the normal push-pull arrangements, the transformer primary is connected to a stiff source by one or the other of the switch transistors minimizing overshoots, and the overlap effect (both transistors on at once) is minimized by the fact that the drive voltage is clamped by the charge storage of the on transistor and delays turn-on of the other device until the stored charge is eliminated.

The output of this oscillator is used to drive the converter circuit consisting of Q4 and Q11. The converter is configured as a half bridge; that is, the second half of the bridge is made up of the filter capacitors C10 and C18. The converter transistors are series connected and the transformer primary is tied between the midpoints of these two bridge halves. The series connection of the converter transistors again minimizes the voltage applied to either device and the overshoots and ringing which would normally be produced by the transformer reactance. The bridge configuration is chosen due to the reasoning previously described in that the best switching devices known to be available at the time would have insufficient or at best marginal ratings for operation over the prescribed line swing in a configuration which required the switch to handle in excess of twice the DC input voltage. Choice of half bridge configuration wherein the transformer primary current flows through the filter capacitors is made more feasible due to the high converter frequencies used. The value of capacity required is sufficiently small to allow the use of available monolithic ceramic capacitors. It should be pointed out that similar currents must be handled by the energy storage capacitors in any scheme involving duty cycle modulation.

As previously stated, an added feature of the circuit is that, due to the AC coupling to the primary, transformer saturation effects due to asymmetry in the drive waveform are eliminated. Advantage is taken of this fact in that only one of the converter switches is duty cycle modulated. The voltage at the junction of the filter capacitor then shifts to force an equal time-voltage integral to be produced across the transformer by the upper switch. Additional circuitry is added to the converter in the form of transistors Q5 and Q12 in order to enhance turn-off. These transistors and their associated circuitry automatically switch the base of the converter transistor to a negative voltage at the time when it is desired to turn it off. This bias is developed by the drive current flowing through R7, in the case of the upper transistor, producing a negative voltage at the junction of R7 and CR6 cathode which is rectified and stored by capacitor C9 when the drive voltage is positive. When polarity reverses, that is when the base of Q4 goes negative, the bottom end of the drive winding becomes positive, turning on Q5,

which pulls the base of Q4 to the negative voltage on C9. In the case of the upper transistor, an additional drive is provided to Q5. This drive is taken from a winding on the main power transformer and is phased in such a way that, when Q11 is on, Q5 is driven on and converter transistor Q4 is held in the off state until such time as Q11 turns off. This turns off Q5 and allows the drive to be applied to Q4.

The bottom converter transistor Q11 is treated in identical manner with the exception of the fact that the drive voltage is taken from the output of a duty cycle modulator. The duty cycle modulation circuitry is basically of the ramp and comparator type consisting of a two transistor latch Q7 and Q8 and a variable ramp generated by C14 and control transistor Q6. This circuit was described in an earlier section. At initiation of the cycle which occurs when the drive winding goes positive the Q7 mode is high due to the drive current applied through C14 and the Q8 node is low. Q9 and Q10 driver transistors are off and the bottom converter transistor Q11 is held off. As capacitor C14 charges the current flowing into the Q7 node decreases until it reaches a critical state where it is insufficient to maintain Q8 in saturation. At this point, a regenerative transition takes place with Q7 going low and Q8 going high. The drive current is then applied to the converter transistor Q11 turning it on. The latch remains in this state until the drive winding goes negative at which time Q11 is turned off through the combined effects of the negative drive voltage applied through diodes CR8 and CR9 and the operation of the off circuit consisting of Q12 and associated components which was described above for the upper transistor.

With the circuit configuration shown, maximum "on" time of the Q8 node is approximately 90% of the half cycle since the drive to Q6 is insufficient to allow instantaneous charge of C14. This is done deliberately to limit the duty cycle. If a greater duty cycle is desired it can be produced by inserting a resistor in series with C14 thus allowing Q6 to turn on Q11 nearly coincident with the positive transition of the drive voltage.

The drive to Q6 is controlled by the output transistor of an optical coupler. The input light emitting diode is controlled in turn by the error amplifier which consists of transistor pair Q13 and Q14. Increasing output voltage increases the current through the light emitting diode and consequently the conduction of the output transistor. This reduces the drive to Q6 which lengthens the off time of the converter transistor reducing the output voltage.

The two required outputs are rectified from windings on the converter transformer by use of conventional diode rectifiers. The three volt output uses Schottky barrier diodes due to the inherently lower forward drop and absence of charge storage exhibited by these devices. A pair of high speed conventional rectifiers is used in the 28 volt output circuit due to the relatively high output

voltage involved and the limited voltage breakdown capability of the surface barrier devices. A conventional L-C filter is included in each output to average the duty cycled converter waveform and provide the required filtered DC. In a final unit intended for actual usage, this output filtering would include added RFI suppressing components such as ferrite beads and use feed through capacitors as input and output terminals.

It should be noted that more elaborate error amplifier circuitry would probably be required in a unit which was intended to operate over a significant temperature range and/or have extremely tight regulation and that current limiting would need to be added to complete the circuit. This could take the form of one or more current transformers placed either in the primary or in each of the secondary output windings and used to control the duty cycle modulator when the current exceeded a preset threshold. The configuration would depend upon the desired limiting scheme, that is whether the limiting can be accomplished on the basis of combined output current and/or whether it need be accomplished when either of the outputs exceeded a preset level.

Performance data indicating the performance of the circuit as configured is shown in the accompanying table. While it may be seen that the efficiencies fall below the desired 85% over the range of output powers tested, the performance would still be deemed to be useful, and indicates that a converter of this power level could be operated at frequencies in the order of a megacycle if other system requirements so dictated.

Aside from the expected problem areas of switching speed and voltage limitation of the switching devices, two other significant problem areas appear. First of these is that the combination of relatively low current gain to start with, with some of the devices in question, coupled with the rolloff of current gain at the high frequencies commensurate with the switching times required, larger than anticipated drive currents are required in order to provide reasonable saturation of the switching devices especially at the leading edge or "on" going portion of the waveform. This problem is further aggravated by the second problem area which is simply that even with the relatively few number of turns required on the transformers and chokes to support the voltage, the capacity inherent in the magnetic components is sufficient to draw rather large surges of current during the switching interval. This, as previously stated, compounds the problem of driving the switch device rapidly and cleanly into saturation. Cleaner switching of the converter can be accomplished, of course, by isolating the converter from the transformer by means of a small choke. This, however, does nothing for the transformer waveform and the isolation is accomplished at the expense of losses in the isolating choke and somewhat poorer damping of the transformer waveform. The significance of this lies mainly in the fact that instead of being able to shade the transformer design strongly in the direction of minimizing leakage inductance, the design must be a compromise one which also minimizes shunt capacity.

Table 3

TYPICAL INSTRUMENT CONVERTER PERFORMANCE

Ein(V)	Iin(A)	Pin(W)	Eo(V)	Io(A)	Po(W)	Eo(V)	Io(A)	Po(W)	Po Total(W)	Eff.(%)
23.0	0.55	12.74	27.93	.296	8.27	2.88	.468	1.35	9.62	75.5
28.0	0.48	13.44	28.05	.293	8.22	2.94	.475	1.40	9.61	71.5
33.0	0.45	14.69	28.48	.296	8.43	2.94	.478	1.40	9.83	67.7
24.8	0.82	20.32	27.82	.460	12.80	2.77	.668	1.85	14.64	72.1
28.0	0.74	20.64	27.94	.460	12.85	2.80	.677	1.90	14.75	71.4
33.0	0.67	21.95	28.03	.480	13.45	2.85	.692	1.97	15.42	70.3
28.6	1.04	29.7	27.70	.608	16.84	2.72	.875	2.38	19.22	64.7
33.0	0.95	31.3	28.00	.630	17.64	2.76	.906	2.50	20.14	64.3
23.0	0.51	11.73	27.93	.330	9.22				9.22	78.6
28.0	0.45	12.46	28.00	.327	9.16		Load on 28V		9.16	73.5
33.0	0.41	13.63	28.23	.335	9.46		output only		9.46	69.4

Spacecraft Regulator

Introduction

As a means of evaluating and demonstrating the applicability of the techniques described in the preliminary sections to a high power unit, a requirement for a so called spacecraft bus regulator was included. This converter-regulator would have specifications as listed below.

Specifications and Goals for a Spacecraft Bus Regulator

Input voltage range	20 V ±5 V.D.C.
Output voltage	28 V.D.C. ±1%
Load current range	0 to 100% of max.
Output power	200 W
Efficiency	Greater than 85%
Operating frequency	200-500 KHz
Ripple	50 ~~15~~ M.V.P.P.
Source ripple	Minimize
Operating life	5 to 10 years in space environment
Operating temperature range	-40°C to +100°C
Overload protection	Short circuit protected

Goals: Design for minimum size and weight; minimize input line turn-on current transients; good transient response; low conducted and radiated E.M.I.; and self-starting capability.

Due to the requirement for maximizing the efficiency and the fact that the input bus line is always lower than the required output voltage, a straight boost configuration was chosen for the spacecraft converter-regulator. This simply means that the converter is configured to add a voltage to the input voltage sufficient to maintain the output at the desired level. By using a boost configuration of this sort, the converter is not required to handle the total output power but only the difference between the required output and that furnished by the input bus. This circuit configuration has the advantage of maximizing the efficiency and minimizing the complexity of the circuit. With the lack of primary to secondary isolation inherent in this type of converter, circuitry utilized to couple error signals across the interface and the normal auxiliary bias and starting circuitry are eliminated. The limitations of this type of circuitry are that, with the direct path of the input voltage through to the output circuitry, there is a limitation on the maximum input which can be applied while still maintaining the output within specifications, and that under overload conditions while the converter circuitry itself can be protected by conventional means, that is the duty cycle reduced to essentially 0, the input source must be protected by a separate limiting device.

Circuit Configuration

The configuration of the spacecraft converter is shown in the attached schematic diagram and discussed in the following paragraphs.

The input bus is coupled to the converter circuitry through an input filter consisting of L1 and capacitors C11, 12, and 13. C10 is added as a high frequency bypass. The bus line is coupled directly to the output through the primary of the converter transformer, the rectifier diodes, and the output choke L2 in such a way that input power can directly supply the output.

It should be noted that the converter is divided into two main sections, the control section and the power section. The power section is designed in such a manner that it is a self-contained stackable unit consisting of filters, converter, and rectifiers necessary to supply the required output power. It can be seen that a number of such power sections could be paralleled and driven from a central control section. Equal sharing of the output power would be produced by the inductance which is part of the smoothing filter in each of these sections. In the worst case situation wherein the input voltage was nearly equal to the required output voltage the small but finite resistance of the primary windings and the filter inductor would guarantee reasonable sharing and at lower voltages the situation would improve even more due to the reactance of the filter inductor.

The converter itself is configured in a reasonably conventional push-pull center tapped transformer configuration. Due to the numbers chosen for input and output voltages of the demonstration hardware, the transformer is configured as a simple one-to-one auto transformer producing a voltage at the input of the rectifier diodes of twice the input voltage. Taps could, of course, be placed at any point along the transformer winding if the input to output voltage ratios were different. The converter transistors are driven by a current transformer. This technique was chosen for several reasons, first of these being that it yields optimum drive to the converter transistors over a wide range of output power which is a requirement of the contract. Secondly it does this with a minimum of power loss. It does this without the power losses usually encountered in providing quasi constant current drive by driving from a higher voltage through a series limiting resistor. The third advantage is that it allows a convenient impedance transformation in order that the control circuitry may be operated at optimum voltage and current levels. Thus, it allows for the stacking of several output sections without requiring inordinately high drive power. The final advantage of using transformer coupled drive to the converter transistors is that the current transformer can be designed to saturate at lower levels of asymmetry than the main power transformer thus precluding the large currents which could occur if the main power transformer

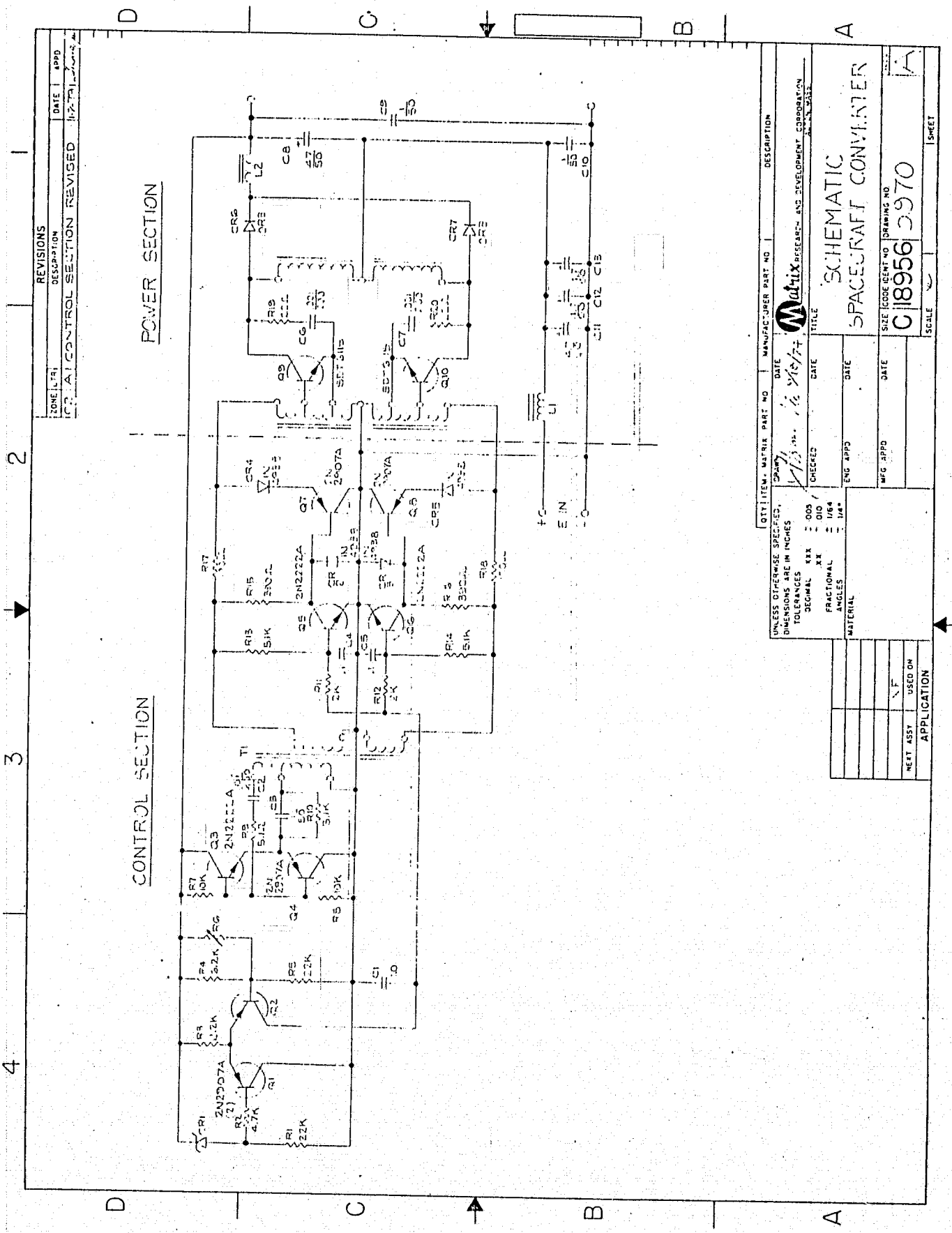

POWER SECTION
CONTROL SECTION
SCHEMATIC
SPACECRAFT CONVERTER
C18956 3970
Matrix RESEARCH AND DEVELOPMENT CORPORATION
REVISIONS
DESCRIPTION
DATE
APPD
IC'S A1 CONTROL SECTION REVISED
DESCRIPTION
MANUFACTURER PART NO
ITEM
QTY
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMAL XXX ± .005
XX ± .010
FRACTIONAL ± 1/64
ANGLES ± 1/4°
CHECKED
ENG APPD
MFG APPD
MATERIAL
NEXT ASSY
USED ON
APPLICATION
SIZE
CODE IDENT NO
DRAWING NO
SCALE
SHEET
+IN
-IN
+OUT
-OUT

Figure 7

were inadvertently saturated due to unbalanced drive to the converter transistors. The output is taken from the collectors of the converter transistors and rectified by a pair of ion implanted rectifier devices. These devices have a lower drop and faster recovery times than conventional devices and have sufficient voltage rating for the application. This full wave rectified output is then averaged by the output filter L2-C8 in order to produce the required 28 V output.

Drive for the converter is produced by a duty cycle modulator of the ramp and comparator type, the ramp being generated by R13, C4 on the one side and R14, C5 on the other. The comparator consists of a two stage amplifier with the second PNP stage connected as an emitter follower. It should be noted that the comparator portion of the circuit is not regenerative but is simply an amplifier whose action is to shunt the drive from the current transformer at the time when it is desired to turn off the particular converter transistor. The turn on of the transistor is initiated by the oscillator voltage applied through a series resistor. A typical sequence begins with a positive waveform appearing at the output of the oscillator transformer, in this case, the side connected to R17. This produces drive to the current transformer which in conjunction with converter transistor Q9 is a regenerative circuit; that is, there is voltage gain due to the step up in the current transformer. This sharpens the turn on of Q9 in response to the drive waveform. During this time the voltage at the base of Q5 is rising in ramp fashion and the DC level of the ramp at that point is controlled by the output of the error amplifier. When the combined voltage reaches the turn-on point of Q5, it draws current through the base emitter of Q7 turning it on and drawing current from the current transformer. This current reduces the drive to Q9 and, the process being regenerative, results in turn-off of Q9. Q9 is held off by the action of the comparator throughout the remainder of the portion of the cycle when the drive waveform is positive and is held off by the drive waveform during the portion of the cycle when it is negative. The process is symmetrical and an identical sequence is then applied to the other side.

The drive waveform for the duty cycle modulator is provided by an oscillator circuit which is essentially identical to that described in the previous section for the instrument converter. The duty cycle of the duty cycle modulator is controlled by the output of an error amplifier which, in this case, is configured as a simple differential amplifier. The output current from Q2 increases with increasing output voltage, raising the average DC level of the ramp voltage applied to the comparators and causing an earlier turn-on of the comparator and the consequent reduction in duty cycle of the converter transistors. A dominant lag is used at the output of the error amplifier to stabilize the loop. As stated in the discussion of the instrument converter, more elaborate control amplifiers, loop stabilization networks, and RFI filtering would be required for converters for actual use.

The detailed design would be based upon the detailed specifications for the converters in question. Due to their importance to the overall operation of the circuitry, the construction of the current transformer and the output transformer require some additional discussion. The primary requirements for the current transformer are that it have extremely tight coupling, that it have reasonably low magnetizing currents, and that it have minimum resistance in series with the main load current. The relatively small size of the core utilized and the relatively low voltage minimize the core loss and the capacitive currents. As such, the transformer is wound for maximum coupling or, stated another way, minimum leakage inductance. The current transformer is wound on a 1/4 mil Supermalloy tape wound bobbin core. The bobbin is divided into two halves with the windings on one side of the center tap being applied to each half. The main or primary winding consists of two turns consisting of four parallel #20 wires spread evenly over that section of the core. The second or base drive winding is formed by winding #22 wire evenly over the half core on top of the distributed two turn winding. The main control winding is formed by progressively sector winding #28 wire over the previous two layers. The other half of the transformer is formed in identical fashion. This results in maximum coupling between the windings having to do with a particular converter transistor, and in particular, maximum coupling between the primary and base drive windings which is the most singly important ingredient. The choice of a tape wound Supermalloy core results from the desire to insure that the current transformer saturates prior to the main power transformer as a function of asymmetry of the applied drive waveform, and secondly, that the magnetizing current be as small as possible.

The output transformer is wound on an 1811 size ferrite pot core of 3D3 material from Ferroxcube Corporation. Four identical layers are placed one on top of the other consisting of eight turns of #22 wire wound evenly once across the bobbin. Layers one and three are connected in parallel and two and four are connected in parallel. The parallel groups are then connected in series to form a center tapped winding. Due to the required power level, the desire to minimize stray capacity is sacrificed somewhat in lieu of providing the maximum coupling between the halves of the winding since the main output power is coupled in this fashion.

Typical performance data for the spacecraft converter is included and indicates that performance of the converter is satisfactory in many respects in that reasonably high efficiency is obtained over a relatively wide range of output power levels. The primary difficulties involved obtaining sufficient control range to remain in regulation over the full input voltage range with currents at the output varying from essentially 0 to the desired maximum loads. Secondly, the devices used as switches limited truly useful operation more in the order of 100 watts as opposed

TABLE 4

TYPICAL SPACECRAFT REGULATOR DATA

Po(W)	28 (1a)			56 (2a)			84 (3a)			112 (4a)			140 (5a)		
Vin	Iin	Pin	Eff.	Iin	Pin	Eff.	Iin	Pin	Eff.	Iin	Pin	Eff.	Iin	Pin	Eff.
16	1.95	31.2	89.7	3.75	60	93.5	5.60	89.5	94	7.40	118.5	94.5			
20	1.60	32	87.5	3.10	62	90.3	4.52	90.4	93	6.10	122	92	7.6	152	92
26	1.30	32.5	86.2	2.45	61.3	91.5	3.60	90	93.5	4.85	121.3	92.5			

to the desired 200 watt level. It is felt that the problem area of control range would be circumvented by a more limited range of output currents required of a normal spacecraft busline converter, and that the capability of stacking output sections would allow any reasonable power level to be obtained from the basic technique without excessive additional complexity.

The design difficulties centered around the relatively low current gain and consequent high drive requirements of the high speed converter transistors and the fact that the relatively large amplitude high speed current waveforms produced make it necessary to exercise extreme care in layout in order that they do not interact with the control circuitry causing erratic operation.

Conclusions

Conclusions that can be drawn from the preceeding are that converters operating at both high and low power with frequencies in excess of 200 KHz for the high power and 1 MHz for the low power converter can be produced. The efficiencies of the lower power version will probably fall somewhat below the levels obtainable at lower frequencies due to the higher contribution of the switching losses. At the higher power level the efficiency numbers could well approach those obtainable at lower frequencies due to the fact that the resistive losses, especially those within the magnetic components, are reduced over those obtained in the lower frequency case if converter size is a limitation. Most of the circuits utilized are not drastically different from those used at low frequencies but are tailored in subtle but important ways to better suit them for the high frequency requirement.

Use of certain techniques such as current transformer drive for the converters is made more feasible due to the relatively smaller size and simpler and less expensive windings required. This is due simply to the fact that a relatively small core and relatively few windings are required to support the normal voltages at high frequencies.

Operation at the higher frequencies requires an added measure of care in choice of components and most importantly in layout and construction techniques. The high frequency high amplitude currents generated can readily produce interference between the power and control sections of a given converter if not properly controlled.

On the positive side, the size reduction of the reactive components allowed by operation at these frequencies can result in a reduction of the overall size of the converter especially at the higher power levels. The loop response or regulating speed capability of the switching regulator is also increased allowing better transient regulation characteristics.

Since the majority of this work was accomplished, a significant time has elapsed and there are, of course, many newer components some of which would be applicable to the high frequency converter area. These are the improved Schottky Barrier diodes, the power FET devices, and the improved conventional diodes and switching transistors. All of these would make the operation of power converters at the higher frequencies more feasible.

It is felt that performance in excess of that actually obtained with the demonstration converters could be obtained with additional work, primarily in the area of optimizing the magnetic components for the lower power converter.

The higher frequency techniques would seem to lend themselves most optimally to the higher power converters having a small number of outputs. The advantages of reduced IR losses and smaller size tend to offset the somewhat reduced efficiency and the increased difficulty in design and fabrication. At the lower power levels, it should be pointed out that the somewhat reduced efficiency becomes less important in inverse proportion to the total output power being drawn. That is to say that, while the percentage losses may be higher, if the total output power is relatively low then the total power loss becomes relatively less important in the overall power considerations. As such, the higher frequency operation may be useful in specific situations even at relatively low power levels.

Recommendations

Due to the lapse of time between the majority of the work and the final report, it is, of course, true that a number of things have changed in this interim period. Should the requirement for high frequency conversion arise, it is deeded advisable to review the entire area of active component selection in light of the new components available. It is felt that, in general, the availability of these newer components makes the use of the somewhat standard switching techniques more feasible at present than they were at the time that the majority of the previous work was performed. As such, the most important improvements to the high frequency converter area would be produced by searching the available components for those which could significantly improve performance in each of the component areas.