NASA CR-151866

SOLAR POWER SATELLITE RECTENNA DESIGN STUDY: DIRECTIONAL RECEIVING ELEMENTS AND PARALLEL-SERIES COMBINING ANALYSIS

RONALD J. GUTMANN
JOSE M. BORREGO

ELECTRICAL AND SYSTEMS ENGINEERING DEPARTMENT
RENSSELAER POLYTECHNIC INSTITUTE
TROY, NEW YORK 12181

CONTRACT NAS 9-15453 WITH
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
LYNDON B. JOHNSON SPACE CENTER

FINAL REPORT
DECEMBER 1978

TABLE OF CONTENTS

Acknowledgments

Numerous students at Rensselaer contributed to the successful completion of this program. In particular, R. Gworek contributed significantly in the area of Yagi-Uda design and cost evaluation, R. Seymour and M. Van Slyke in the printed circuit implementation feasibility evaluation and J. Faricelli and M. Mackiw in the computer simulation effort.

We would also like to acknowledge the support and technical interaction with numerous JSC personnel. In particular, the suggestions and feedback from J. S. Kelley and R. H. Dietz throughout the program and the conversations with F. Stebbins on rectenna structure deserve special recognition.

Finally, the assistance of Ms. M. Jadlos in preparing the final report is gratefully acknowledged.

R. J. Gutmann

J. M. Borrego

LIST OF FIGURES

LIST OF TABLES

1.0 PROGRAM OVERVIEW

The solar power satellite (SPS) baseline rectenna has been developed over a period of years by Raytheon Company. To date rectenna conversion efficiencies (RF to DC) ~85% have been demonstrated on a small scale clearly indicating the feasibility and potential of efficient conversion of microwave power to DC.[1-3] However numerous technology issues remain to be resolved before an operational SPS rectenna can be designed. In addition, overall SPS cost estimates indicate that the baseline rectenna subsystem will be between 25% and 40% of the system cost.[4] Clearly further work exploring other rectenna design approaches and further analysis of the baseline rectenna is needed. This program was originally proposed to initiate an ongoing effort to pursue these tasks. This document is the final report on the first phase of such a program.

Of the many possible rectenna related tasks, two were selected for study. One emphasized an investigation into alternative rectenna concepts, focusing on the possibility of more directional, higher gain receiving elements to reduce rectenna cost (while maintaining or even improving conversion efficiency). The second task emphasized an evaluation of power combining inefficiencies inherent when many conversion circuits share a common DC load, focusing on the effect of individual receiving elements operating at different power levels.

In this program overview chapter, these tasks are described in more detail, followed by a description of the approach used in addressing these tasks including a discussion of key assumptions. Finally we list briefly a list of key accomplishments of our program, items which are thoroughly presented in the body of the report.

1.1 TASK DEFINITION

As a result of system studies performed at Johnson Space Center (JSC), it appears that the baseline half-wave dipole receiving element is more nondirectional than necessary. With an orbit eccentricity of .01 and small inclination, the rectenna must tolerate azimuth angle variations of $\pm 1\ 1/2^{\circ}$ and elevation angle variations of $\pm 1/2^{\circ}$, assuming a rigid and perfectly aligned rectenna.[5] Present rectenna elements can tolerate an angular beam variation of $\pm 6^{\circ}$ with a tolerable 0.5% reduction in received power. Besides this over-nondirectionality, the rectenna cost is a significant percentage

of the system cost and there is a large uncertainity in the conversion circuitry cost (in particular the GaAs Schottky diodes). Therefore, it is desirable to reduce the number of rectenna elements (15 billion in the baseline rectenna)[6] by designing a more directional, higher gain receiving element.

Task A in this program emphasized selection, design and comparison of more directional receiving elements. Specific tasks originally delineated are given below:

- Develop a detailed list of characteristics required for a more directional receiving element with relative weights for each category.
- Perform a preliminary investigation of basic antenna elements in order to delineate a small number (perhaps 3) of the most promising alternatives.
- Perform a detailed comparison of the more promising antenna elements for a more directional SPS rectenna.
- Perform a preliminary evaluation of rectenna element production techniques with the more promising elements.
- Project a production cost comparison of the more promising elements and compare to the baseline rectenna element including performance factors.

A second major task focused on a previously unexamined, fundamental issue with the baseline rectenna. In order to provide reasonably sized power modules (perhaps 10 kW to 300 kW), it is necessary to combine outputs of numerous (10,000 to 300,000) rectenna elements and operate into a common DC load. Elements are combined in parallel and/or series to increase the current and/or voltage level. Rectenna testing to date stressed similar units operating at the same power density. In fact rectifier outputs were combined to insure operation at identical power levels.[7] Since edge elements in the rectenna will nominally operate at different power densities and central elements will operate at different levels due to diffraction from the serrated rectenna, the effect on overall conversion efficiency must be considered.

Since this issue had not been evaluated previously (either analytically or experimentally) and was inherent in SPS operation, Task B emphasized on evaluation of power combining inefficiency in the baseline rectenna. Particular tasks delineated are listed below:

- Develop basic fundamentals for parallel-series combining of DC power from rectenna elements (into basic 10 kW to 300 kW power modules).
- Develop a model of rectenna element operation that can be used to calculate effect on power density spatial variations on parallel-

series combining efficiency.

- Perform a preliminary evaluation of SPS power module size constraints for baseline rectenna.
- Delineate areas for further work to quantify the power combining degradation with power density fluctuations and to alleviate this degradation.

1.2 APPROACH TAKEN WITH UNDERLYING ASSUMPTIONS

In performing these tasks with the resources available, certain assumptions were needed to bound the program. In this section of the report these are delineated and discussed briefly. Generally these assumptions were based upon the status of SPS rectenna development, the needs of SPS system planning in the near future and the technical literature in relevant areas. Emphasis was placed upon arriving at quantitatively based conclusions at the end of the program, while providing a fundamental foundation for future work.

Task A, design and comparison of more directional receiving elements, initially followed two parallel paths: consideration of rectenna requirements for SPS operation, focusing on critical technology feasibility areas and areas of previously projected large and/or uncertain cost, and consideration of alternative receiving antenna concepts that could be feasible. This is discussed in some depth in Section 2.1, but we decided to investigate further three alternatives (individually and in combination) to the baseline rectenna, namely printed circuit receiving element and RF to DC conversion circuitry implementation, Yagi-Uda type receiving elements and a hogline rectenna.

At various times these had been proposed (with various degrees of detail) by W.C. Brown of Raytheon and R.M. Dickinson of JPL, O.K. Garriott of JSC, and Boeing Company respectively. Except for some detail on the hogline reported by Boeing in the middle of this program,[7] there was little quantifitative design information available about these options. Because of the ongoing Boeing effort, the hogline was not considered in as much detail as the printed circuit implementation and Yagi-Uda antenna element. However, some basic hogline electrical considerations are discussed in Section 2.2.3. The remainder of Chapter 2, Sections 2.2.1, 2.2.2, and 2.3, contain the emphasis of our work in this task, a detailed evaluation of printed circuit element and Yagi-Uda receiving element feasibility.

The principal factor limiting printed circuit implementation of the receiving element and RF to DC conversion circuitry is increased RF circuit losses due to smaller conductor cross section. In addition spacing constraints dictate that a lumped element (rather than distributed/lumped element) filter would be desirable with a printed circuit design. Appreciable design effort was expended in evaluating low pass filter designs suitable for the input harmonic rejection filter. Inductor loss was assumed to be the fundamental limiting factor on circuit loss and state of the art, printed circuit inductor Q's were assumed in evaluating insertion loss of the input filter. Results of our evaluation of printed circuit element feasibility are presented in Section 2.2.1.

Yagi-Uda receiving element electrical design factors are presented in Section 2.2.2. Since arrays of Yagi-Uda antennas are not widely reported, we emphasized a design comparison based upon isolated receiving elements. While the element gain is slightly smaller in an array, we believe the results obtained can be used as a reasonable first order design, and are a valid indicator of achievable performance. This approach allowed us to use optimized designs from the literature and to compare performance with long and short Yagi-Uda elements in some detail.

In a Yagi-Uda antenna the front-to-back (F/B) ratio is often an important factor. We estimate that if a F/B ratio above 25 dB is obtained, the ground plane of the baseline rectenna is not needed, while if a F/B ratio below 15 dB is used the electrical requirements on the ground plane mesh can be relaxed. Since forward gain is reduced to achieve high F/B ratio, both moderate and high F/B ratios were considered. The validity of these critical values of F/B ratio depend upon multiple land use considerations and polarization rotation in the ionosphere and need further specification.

Because of the possible synergistic effects between printed circuit versus baseline type construction, Yagis with moderate versus high F/B ratio, and long versus short Yagi-Uda elements, eight receiving elements were considered in some depth. Electrical, structural and economic factors were evaluated, and are reported in Section 2.3. The approach taken was to select optimum electrical designs based upon the assumptions above, develop a structural design and arrive at a production cost per square meter of rectenna area. No detailed structural engineering was performed, that is detailed wind and snow loading was not explicitly included, although qualitative structural requirements were considered in the design and cost evaluation.

Cost estimates similar to those reported in latest rectenna studies[7] were made, although not in as much detail. We believe the results indicate which designs are most promising and worthy of further detailed investigation, although detailed comparison with the baseline requires further work.

Task B, parallel-series combining analysis, focused initially on the methodology of performing the analysis and development of appropriate RF to DC conversion circuit models. A principal requirement for any combining analysis is a valid circuit model of the RF to DC conversion circuitry. In our work two parallel paths were followed: namely development of both a detailed computer model and an approximate closed form model. The latter was developed to gain insight into circuit operation, to help delineate filtering requirements, and to aid in understanding fundamental combining inefficiency tradeoffs. This closed form model is described in detail in Section 3.1.2, emphasizing the importance of various functional parts of the conversion circuitry. The computer simulation model does not duplicate the baseline rectenna element directly, but includes lumped element L-C input and output filters for reduced running time on the computer and to more accurately evaluate printed circuit implementation designs. Reasonable diode parameters, mounting parasitics, and loss parameters were incorporated in arriving at a model agreeing with actual rectifier performance. In order to achieve 80-90% efficiency, an input harmonic-phasing transmission line was necessary, as described in Section 3.1.1 (along with detailed assumptions about the model). Our computer model is not as extensive as previously developed,[8] but it has a key advantage, namely that a general computer program widely available is used. Thus, both computer and closed form models could be easily used and even extended in future rectenna development programs.

The power combining methodology was to obtain the output equivalent circuit of the RF to DC conversion circuitry by varying the load impedance at each RF power level of interest. Incident power was varied over a 20:1 range, compatible to the range expected in SPS operation. This load line analysis provided a simple power dependent output equivalent circuit that was used with a circuit analysis developed recently for solar cells[9] to compare series and parallel combining inefficiencies. The load line analysis is described in Section 3.2, followed by the power combining analysis in Section 3.3.

The power combining analysis developed calculates the combining inefficiency (percentage reduction in DC output power for operation into a common load) for series or parallel combining for an arbitrary distribution of incident power level. This allows accurate determination of the effect of power density variations to be determined for the first time. The effect of series/parallel combining compared to parallel/series combining has not been evaluated in similar detail but is discussed in Section 3.4, which relates our analytical results to SPS power module size constraints.

1.3 SUMMARY OF KEY ACCOMPLISHMENTS

As a result of this program we have made some key contributions toward evolution of the rectenna design for SPS operation. These are concisely summarized as follows:

- The fundamental limitation of printed circuit implementation, RF circuit losses, was evaluated by detailed consideration of the RF to DC conversion circuitry input filter and supported by the detailed computer simulation model (Sec. 2.2.1).
- Electrical design of isolated Yagi-Uda receiving elements has provided an understanding of the tradeoff between gain, F/B ratio and number of directors, while providing an electrical design for preliminary structural design and Yagi-Uda rectenna costing (Sec. 2.2.2).
- A comparison of half-wave dipoles and various length Yagis, as well as printed circuit implementation and baseline type construction, indicates that more directional receiving elements are technically feasible and can lead to significantly lower rectenna costs (Sec. 2.3).
- A detailed RF to DC conversion circuitry computer simulation model was developed using a transient analysis program (Spice 2) in order to obtain an accurate output equivalent circuit (Sec. 3.1.1). Results obtained with this model are in general agreement with rectenna experimental results, so that we have confidence in our analysis using this model.
- Various simplified closed form models of the conversion circuitry were developed, to enhance understanding of circuit operation, to provide design guidelines and for use in first order calculations where a computer simulation model is not warranted (Sec. 3.1.2).

- Power combining inefficiencies were obtained for both series and parallel combining circuits, assuming identical conversion circuitry operating with a variety of input power distributions. A load line analysis was used to obtain the output equivalent circuit for various input power levels using both computer simulation and closed form models (Sec. 3.3).
- The impact of the power combining inefficiencies on the buss bar design and power module size was analyzed in a preliminary fashion, sufficient to get an order of magnitude understanding and to give guidelines for future investigations (Sec. 3.4).

2.0 MORE DIRECTIONAL RECEIVING ELEMENTS

In this chapter of the report results obtained on our evaluation of alternative rectenna concepts are presented. While the baseline rectenna has demonstrated the feasibility of efficient RF to DC conversion, the high projected cost in SPS system studies indicated that different approaches to rectenna implementation be considered. Previous system studies of orbit considerations, beam pointing accuracy and rectenna alignment and settling factors[5,6] indicate that a more directional receiving element is feasible.

Since the number of conversion circuits will be reduced as a more directional, higher gain receiving element is utilized, lower overall cost would be expected. In addition GaAs Schottky diode conversion efficiency is increased when operated at higher powers resulting with a more directional receiving element (at least until voltage breakdown or thermal considerations become limiting). From updated orbit information, we concluded that a 0.5% power beamwidth (power reduction by 0.5%) can be as low as $\pm$ 1-1/2% in the azimuth plane and $\pm$ 1/2° in elevation, compared to a $\pm$ 6° beamwidth (0.5% power beamwidth) with the baseline rectenna.

We concluded that a 5 to 10 dB increase in effective element gain would be desirable, resulting in a factor of 3 to 10 decrease in number of receiving elements and a similar increase in power incident on the conversion circuitry. While a larger factor (~ 50 or 17 dB) could be obtained with an optimally shaped fan beam and perfect alignment except for orbit considerations, it seemed prudent to allocate similar angular variations to rectenna alignment and settling and power beam phase control errors. In addition with power level increases greater than 10, diode breakdown considerations could be a problem and diode thermal considerations for long life operation need to be evaluated. An overall listing of advantages and disadvantages on going to higher gain, more directional receiving elements is shown in Fig. 2-1.

2.1 RECTENNA ALTERNATIVES COMPARED WITH OVERVIEW COMPARISON

Because of the variety of alternative antenna elements and the variety of factors to consider, a list of desirable characteristics for the SPS rectenna was developed. This list of 17 characteristics is presented in Table 2-1, along with the relative weight of each characteristic. While this list is not unique nor all encompassing, it does indicate the factors

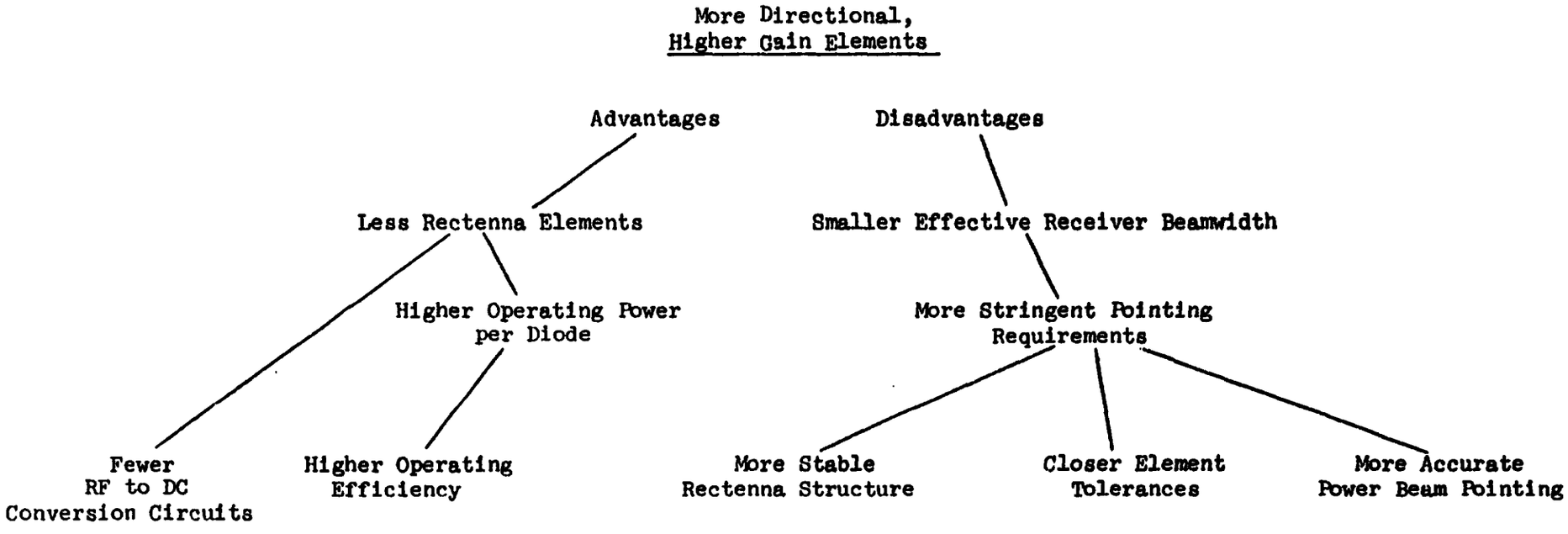


Fig. 2-1 Advantages and disadvantages of a higher gain, more directional receiving element

considered explicitly in our work and our evaluation of the relative importance of each factor.

As indicated in Table 2-1, most of our emphasis was on electrical evaluation of alternative receiving elements. We utilized isolated element performance as a first order indicator of performance in an array environment. Principal emphasis is placed on collection and conversion efficiency, with secondary weighting on flexibility in antenna parameters (namely directivity, radiation impedance and harmonic characteristics) to permit final conversion circuitry optimization. In the characteristics categorized under "electrical emphasis", relative weights were assigned to get a spread between 1 and 5, with "5" indicating most important.

Non-electrical characteristics were grouped into "manufacturing emphasis" and "system considerations", as shown in Table 2-1. Emphasis is placed upon potential low cost manufacturability, with secondary emphasis on related factors such as terrain tolerance, maintenance and multiple land use. In particular, structural implications of the various designs need further work to properly evaluate requirements for different environments and, as described in Sec. 2.3.3, to permit more accurate cost estimation. Note the relative weights in these latter categories have been made compatible with the weights under "electrical emphasis" characteristics. Since these latter areas were not evaluated in as much detail, less critical areas (weights 1 and 2) were not explicitly considered in our work.

During the initial phases of the program a variety of conventional receiving elements were considered briefly. These included horns, corner reflectors, rhombic antennas and microstrip antennas. Most suffered from either (or many) of the following fundamental limitations: could not be expected to obtain 100% aperture efficiency, high raw material usage, manufacturing complexity, inherent structural problems, incompatibility with high efficient power conversion circuitry or high optical blockage (to make multiple land use infeasible in many cases). As a result such elements were only briefly considered.

Our early evaluation indicated that Yagi-Uda antenna elements were promising. Analytical and experimental results[10-12] indicated that

Table 2-1 Characteristics for SPS Rectenna Element

Characteristic	Relative Weight (1 to 5 with 5 most important)
Electrical Emphasis	
capable of efficient reception	5
controllable directivity	3
overall conversion efficiency with Schottky rectifier	5
controllable radiation impedance	2
combining network compatibility	4
amenable to analysis and modeling	2
harmonic radiation characteristics	3
cross polarization considerations	1
Manufacturing Emphasis	
low cost raw material usage	5
low manufacturing complexity	4
lack of manufacturing tolerances	3
structural implications	4
terrain tolerance	3
single building block feasibility	2
System Considerations	
maintenance implications	2
environmental protection	3
multiple land use feasibility	4

isolated Yagi-Uda receiving elements could provide desired electrical characteristics, although some type of folded dipole would be needed in the driven element to provide a sufficiently high radiation resistance. The possibility of eliminating the ground plane also appeared to be attractive, although this depends upon obtainable front-to-back (F/B) ratio, polarization rotation in the ionosphere (Faraday rotation) and multiple land usage.

In addition the possibility of printed circuit implementation appeared attractive as a means of lowering raw material cost[5]. While RF circuit losses could be a limiting factor in this application, possible manufacturing advantages warranted a careful investigation. Possible synergistic effects between Yagi-Uda elements and printed circuit implementation were not obvious so that all possibilities were eventually considered explicitly.

During this time, the hogline rectenna proposed by Boeing[6] came to our attention. While concerned about the capability of achieving near 100% aperture efficiency, we considered the hogline to some intermediate detail. In particular we considered some electrical design problems, without a detailed look at manufacturing and structural factors.

Our overall evaluation of four alternative rectennas using the criterion of Table 2-1 is given in Table 2-2. Weights indicate a relative order between the alternate choices, with 5 "most favorable" and 1 "least possible". If values of 4 or 5 are given, we have concluded that satisfactory performance can be obtained. Low ratings of 1 or 2 indicate a deficiency in the area or a basic uncertainty about obtaining desirable performance.

Although there is no obvious best element derived from Table 2-2, some conclusions can be drawn. First the baseline rectenna element has good electrical characteristics. However, the alternatives do have some significant advantages that indicated further investigation was warranted. Most of our effort was on Yagi-Uda elements and printed circuit implementation, to avoid duplication of the work at Boeing on the hogline.

Table 2-2 Alternative Rectenna Overall Comparison

Characteristic	Relative Weight (1 to 5 with 5 most important)	Baseline Dipole Rectenna	Printed Circuit Dipole Implementation	Yagi Printed Circuit	Yagi with Baseline Construction	Hogline
Electrical Emphasis						
capable of efficient reception	5	5	5	4	4	3
conversion efficiency with Schottky rectifier	5	5	3	4	5	4
controllable directivity	3	2	2	3	3	4
controllable radiation impedance	2	2	4	3	2	4
amenable to analysis and modeling	2	4	4	3	3	3
harmonic radiation characteristics	3	3	3	2	2	4
cross polarization considerations	1	4	4	2 or 4**	2 or 4**	3
combining network compatibility	4	5	4	4	4	3 or 5*
Manufacturing Emphasis						
low cost raw material usage	5	3	4	4	3	4
low manufacturing complexity	4	4	5	5	4	4
lack of manufacturing tolerances	3	5	5	4	4	3
structural implications	4	3	3	3	3	3
single building block for rectenna	2	2	2	2	2	2
terrain tolerance	3	3	3	3	3	2
System Considerations						
multiple land use feasibility	4	3	3	4	4	2
maintenance implications	2	2	4	4	2	3
environmental protection	3	3	3	3	3	4

* polarization dependent

** ground plane dependent

1 to 5 with 5 most favorable

2.2 PRINCIPAL ELECTRICAL CONSIDERATIONS

In this section of the report principal electrical considerations evaluated in some depth during the program are presented. Three isolated subjects are treated: an analysis of printed circuit implementation feasibility with detailed evaluation of RF circuit loss in the input filter (Section 2.2.1); a comparison of the electrical performance of short, i.e. 3 element (1 active element, 1 reflector and 1 director), and long, i.e. 6 element (1 active element, 1 reflector and 4 directors), Yagi-Uda receiving elements designed for both high (> 25 dB) moderate (~ 15 dB) and low (~ 5 dB) F/B ratio; and a discussion of fundamental electrical considerations in the Boeing-proposed hogline rectenna.

2.2.1 Printed Circuit Implementation

In exploring alternative rectenna concepts, printed circuit implementation of the receiving elements and RF to DC conversion circuitry was considered. A basic half-wave dipole type receiving element in printed circuit form is depicted in Fig. 2-2. A key difference apparent in this conceptual drawing is the elimination of the baseline two plane construction, and substitution of the collection buss in closer proximity to the ground plane mesh. This approximates the configuration used in the Goldstone demonstration tests,[2] except that we consider extending the conversion circuitry through the ground plane to be quite undesirable. Therefore our designs emphasized using lumped elements wherever possible, thereby keeping the physical length of the conversion circuitry less than .2λ. This would permit the DC collection buss to be located on the antenna side of the ground plane mesh.

While the printed circuit implementation is clearly feasible, the penalty in conversion efficiency needed to be evaluated. In considering the various parts of conversion circuit, we decided to focus our attention on the input low-pass filter. This filter allows the 2.45 GHz received signal to propagate to the diode rectifier while trapping harmonics generated by the diode. The effect of the filter in the conversion process is discussed in Section 3.1.2.

We evaluated the input filter assuming that the antenna radiation impedance was 75+j0 ohms and that no impedance transformation was needed

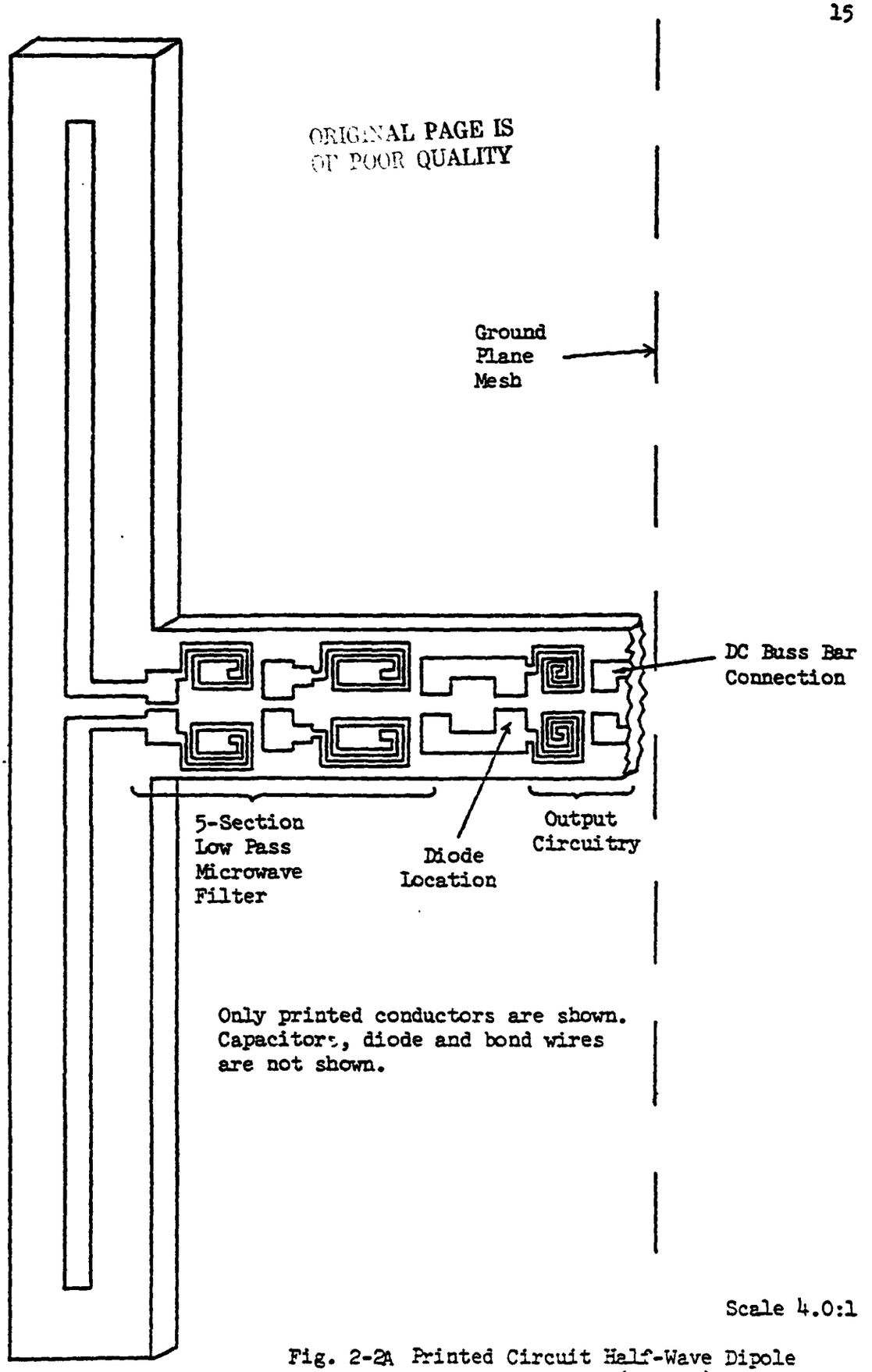


Fig. 2-2A Printed Circuit Half-Wave Dipole Rectenna Element (Ref. 5)

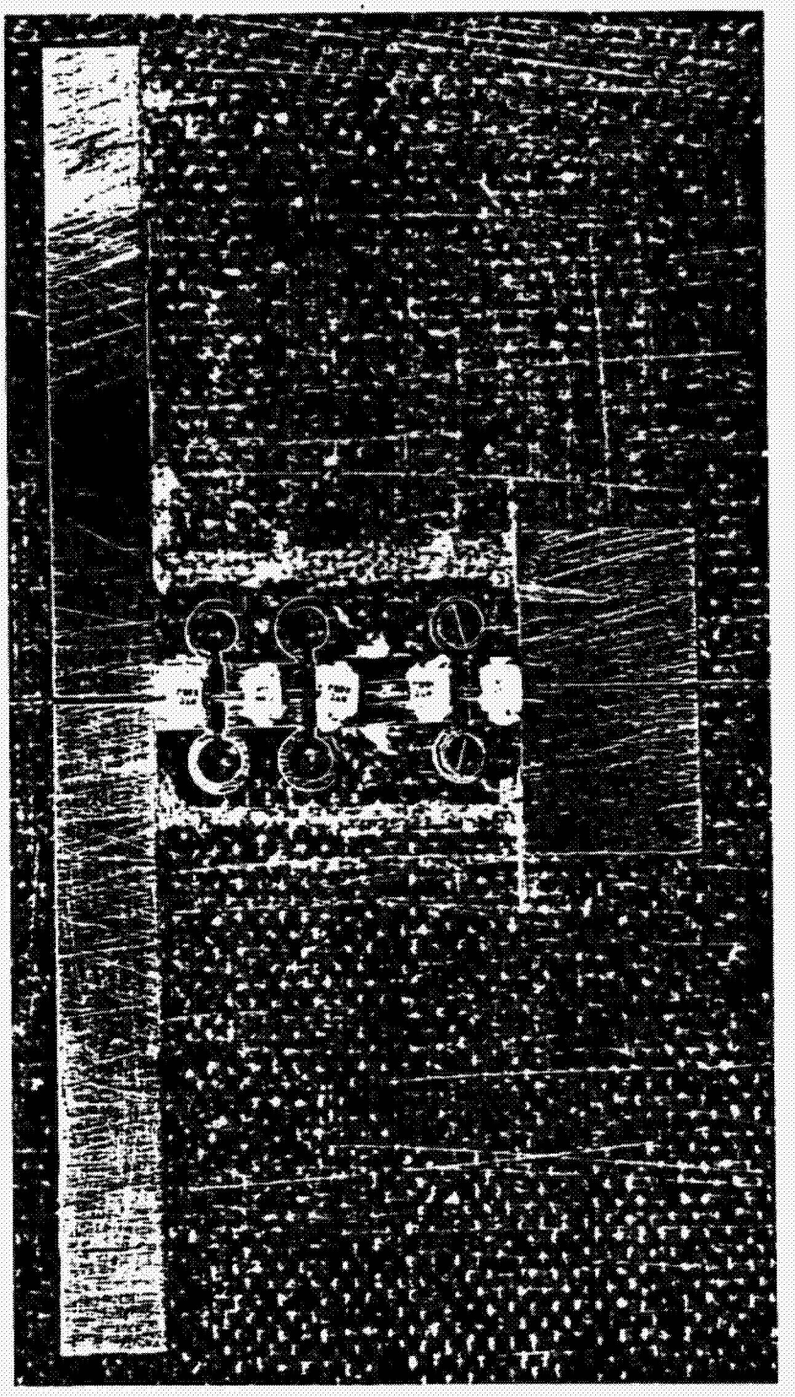


Fig. 2-2B Printed Circuit Half-Wave Dipole Rectenna Element (Scale ~ 3.5:1)

between input and output. While the actual requirements depend upon rectifying diode selection and circuit optimization, this impedance is convenient for evaluation purposes and has been shown in our work to be consistent with high conversion efficiency (Sec. 3.1.1). An n=5 low pass filter was selected, comparable to the baseline design. The filter was a straightforward shunt C-series L-shunt C-series L-shunt C design. Minimum loss was assumed to be limited by inductor Q due to finite conductor losses. Thus inductor Q's of 300 to 450 were selected, comparable to the better values measured experimentally and calculated analytically for inductors of the magnitude required at S band.

The filter design concept is depicted in Fig. 2-3.[13] A Chebyshev design was selected to permit high harmonic rejection. In addition 2.45 GHz was selected to be in the highest frequency null of the lossless filter response to minimize insertion loss. Initially we anticipated using a high ripple factor to enhance harmonic rejection, but as indicated in Fig. 2-3 the insertion loss at 2.45 GHz (i.e. 0.951 f_c) increases as the ripple factor increases when finite Q elements are introduced.

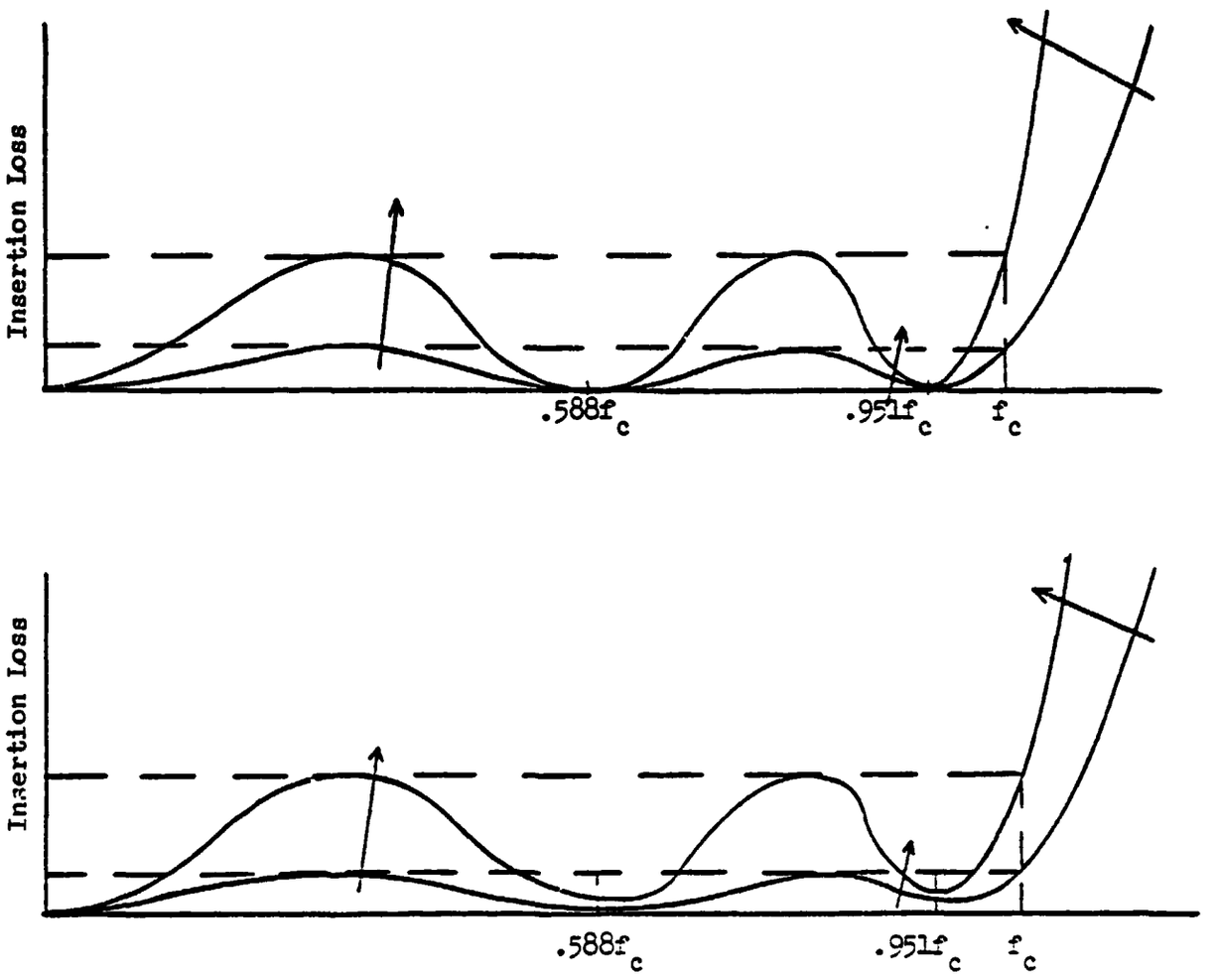
The tradeoff in harmonic rejection versus loss at the fundamental is indicated in Table 2-3 for 0.1 dB, 0.5 dB, and 3.0 dB ripple designs. Note that insertion loss at 2.45 GHz increases from .078 to .116 to .235 dB and second harmonic rejection increases from 32 to 39 to 48 dB with the increasing ripple factor. Interesting enough, near DC (.3 MHz) the insertion loss decreases with increasing ripple factor, so that DC loss approximations for finite Q elements are not useful in evaluating loss characteristics at 2.45 GHz. From these results we selected the 0.5 dB ripple design as the best compromise for further study.

Next we focused attention on design of the printed circuit spiral inductors. The inductance and unloaded Q of such inductors can be approximated (~ 20% accuracy) by the following relationships:[14]

$$L = \frac{a^2 n^2}{8a+11c}$$

and

$$Q = \frac{2LW}{an} \left(\frac{f}{\pi \mu_o \rho}\right)^{1/2}$$



Insertion Loss vs. Frequency for N=5 Chebyshev Filters. Arrows in direction of increasing ripple factor.

(A) Lossless Elements (B) Finite Q Elements

Note: .951 f_c=2.45 GHz or f_c=2.576 GHz

Fig. 2-3 Concept of Chebyshev Input Filter Design

Table 2-3 Printed Circuit, Chebyshev Input Filter Characteristics

Ripple Factor (dB)	Design Parameters (from Ref. 13)					I.L. (dB) with inductor Q=300						
	C_1 (pF)	L_2 (nH)	C_3 (pF)	L_4 (nH)	C_5 (pF)	.3MHz	.80GHz	1.52GHz	2.10GHz	2.45GHz	4.90GHz	7.35GHz
0.1	.94	6.30	3.25	6.30	.94	.036	.147	.053	.156	.078	32.	52.
0.5	1.38	5.70	2.09	5.70	1.38	.032	.541	.065	.554	.116	39.	58.
3.0	2.87	3.50	3.74	3.50	2.87	.020	3.058	.102	3.071	.235	48.	68.

Note: $f_c = 2.576$ GHz

$.951f_c = 2.450$ GHz

$.588f_c = 1.515$ GHz

where $a = \frac{(r_i+r_o)}{2}$ the mean radius of the spiral, $c = r_o - r_i$, r_i the inner radius of the spiral in mils, r_o the outer radius of the spiral in mils, L the inductance of spiral in nanohenries, n number of turns, W the line width in mils, f the frequency, ρ the resistivity (for copper 1.7×10^{-8} ohm-m), and μ_o the permeability of free space. Dimensions and resultant Q's for the 0.5 dB ripple design ($L_2/2$ or 2.85 nH) are given in Table 2-4. From the designs considered in detail the one turn coils of high Q (designs 2 and 3) were selected. With the higher Q inductors possible, the .116 dB insertion loss given in Table 2-3 can be reduced to above .065 dB, a significant reduction.

The resultant input filter is shown in Fig. 2-4, a photograph of a filter prototype using the design values above. The tabs at the ends are compatible with spring connections on baluns used to interface to standard microwave test equipment. While we attempted to evaluate experimentally the filter design, poor balun performance prevented a meaningful evaluation with the resources available.

While these designs allow a relative comparison of filter performance, it is not sufficient for rectenna element feasibility evaluation. In our detailed computer simulation discussed in Sec. 3.1.1 this filter was used, with an extremely conservative inductor Q of 135, to compensate for the lack of inclusion of additional loss factors and to insure that calculated performance could be achieved. Results of our nominal design are indicated in Table 2-5, indicating that circuit losses with conservative inductor Q are significant. While we did not expand a large effort in optimizing a design after achieving baseline type performance (without a supportive experimental program this would not be justified in our opinion), the performance indicated is considered realistic and even somewhat conservative.

Our evaluation is that printed circuit conductor losses can be significant, but with proper RF design can be tolerable. However printed circuit implementation will only challenge baseline type construction if structural and/or cost advantages balance the resultant 2 to 4% penalty in conversion efficiency. The range in conversion efficiency penalty results from uncertainty in obtainable inductor Q and an additional contribution due to transmission line loss and finite capacitor Q. We decided that considering printed circuit implementation further was prudent, even though loss penalty is significant.

Fig. 2-4 Photograph of Prototype Lumped Element Input Filter (Scale ~ 10:1)

Table 2-4 Dimensions and Theoretical Q's for 2.85 nH Inductors

d_o(mil)	d_i(mil)	a(mil)	c(mil)	W(mil)	n	Q
100	40	35	30	10	1.19	270
100	60	40	20	20	.98	570
100	65	41.2	17.5	17.5	.94	500
100	80	45	10	10	.81	305
80	40	30	20	6	1.21	185
80	60	35	10	10	.91	35
60	40	75	10	2	1.19	170

At Nominal Power (1.04W)

Conversion Efficiency =	83.0%
Circuit Losses	7 %
Diode and Mount Res.	3 %
Mismatch Loss	1 %
Diode Drop	6 %

Efficiency Sensitivities (% change in efficiency for given parameter change)

1% per 20% change in Q_L

1% per 30% change in diode and mount res.

1% per 0.2eV change in barrier height (at 1W level)

Power Level Dependence

$P_{in(w)}$	$\eta(\%)$
1.50	84.2
1.04	83.0
.67	80.5
.38	79.0
.17	74.5

Table 2-5 Conversion Circuitry Computer Simulation Model Performance

2.2.2 Yagi-Uda Design Features

Yagi-Uda antennas have been developed over a period of 50 years, with various analytical and experimental data available. However there are many variables in such an antenna design and many previous efforts did not result in design information over a wide range of parameters. We decided to principally utilize a detailed procedure by Morris[12] as reported in a well-known book on cylindrical antennas[11]. These results allowed a comparison of short (3 element) and long (6 element) designs, as well as indicating tradeoffs between gain and front-to-back (F/B) ratio. Recent Yagi-Uda optimization techniques[15], however, have resulted in improved performance and this refinement has also been included in our design evaluation.

Representative designs considered most desirable for SPS application and indicative of design tradeoffs are indicated for 3 and 6 element designs in Tables 2-6 and 2-7 respectively. Note that the work by Morris[12] assumed .50λ driven elements and .51λ reflectors spaced .25λ from the driven element. Only the director(s) length and spacing(s), assumed equal, were varied as indicated in Fig. 2-5. With these key variable parameters, forward gain could not be increased to the degree desired (Section 2.0), the baseline antenna design having a gain of about 6.5 dB. While other information on Yagi-Uda antennas indicates higher gain should be achievable, the work is not as extensive nor thorough as the results reported here. The last two designs in Table 2-7 include variable director spacing and indicate further performance improvement. In some cases however, the overall Yagi-Uda length increases, with material cost and structural implications (discussed in Sec. 2.3). As discussed in Sec. 1-2, this performance assumes isolated elements and is only approximately indicative of array performance.

Based upon the calculated results (experimentally supported as well) listed in Table 2-7, we project that performance given in Table 2-8 can be achieved with Yagi-Uda receiving elements. The performance shown in Table 2-8 indicates that the number of rectenna elements can be reduced by a factor between 1.6 and 5.6 depending upon F/B ratio and number of elements. While longer Yagi-Uda receiving elements (more directors) are

Table 2-6 Representative 3 Element Yagi-Uda Performance (After Ref. 11)

Driven:	.50λ	.50λ	.50λ
Reflector:	.51λ Spaced .25λ	.51λ Spaced .25λ	.51λ Spaced .25λ
Director:	.44λ Spaced .12λ	.46λ Spaced .16λ	.46λ Spaced .10λ
Gain (WRT Isotropic)	7.3 dB	9.1 dB	8.1 dB
F/B Ratio:	30 dB	8 dB	17 dB
Z_{IN} (Ohms):	40 + j20	20 + j70	16 + j20
Overall Length:	.37λ	.41λ	.37λ

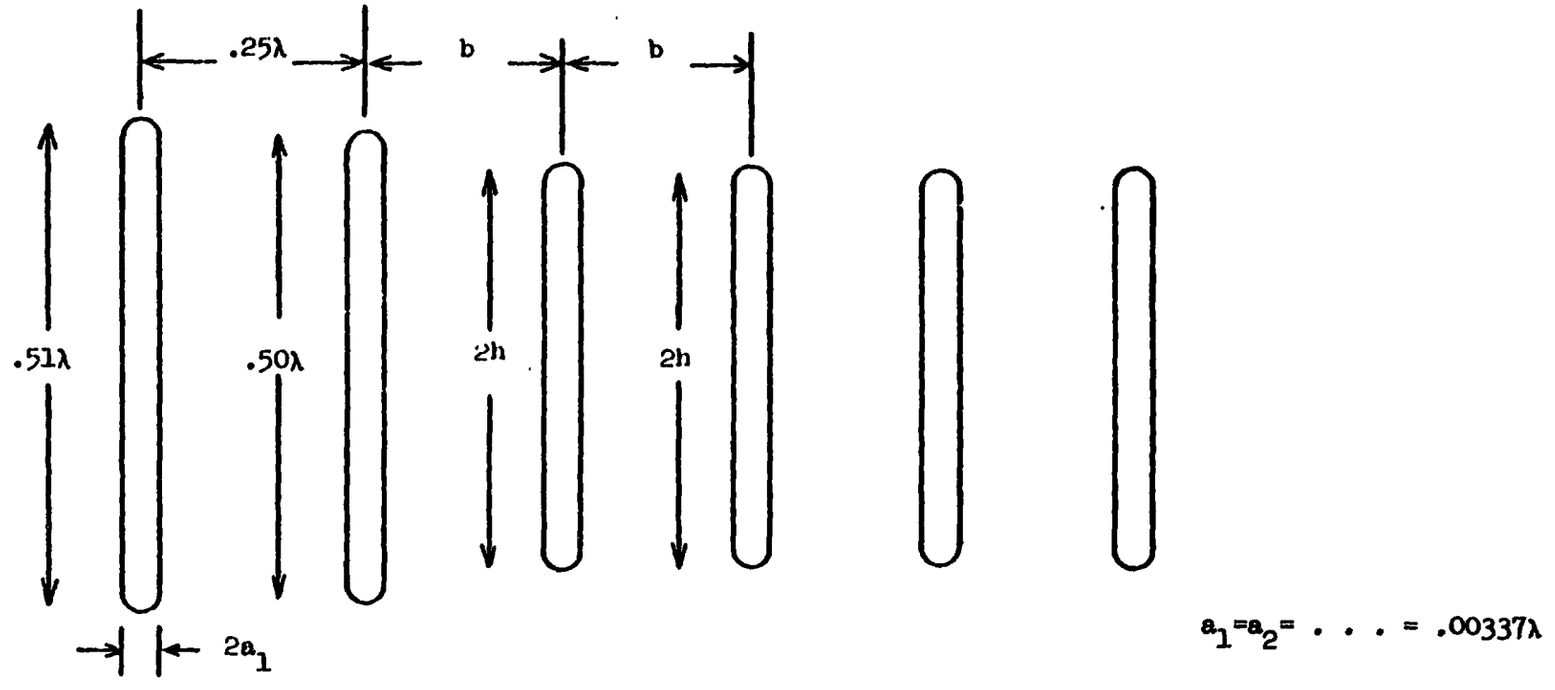


Fig. 2-5 A Yagi-Uda Array with Directors of Constant Length, Radius and Spacing (after Ref. 11)

Table 2-7 Representative 6 Element Yagi-Uda Performance (After Refs. 11 and 15)

Driven:	.50λ	.50λ	.50λ	.50λ	.45λ
Reflector:	.51λ Spaced .25λ	.51λ Spaced .25λ	.51λ Spaced .25λ	.51λ Spaced .25λ	.48λ Spaced .25λ
4 Directors:	.415λ Spaced .145λ	.423λ Spaced .25λ	.43λ Spaced .25λ	.43λ Spaced .31λ	≈ .216λ*
Gain (W.R.T. Isotropic):	10.0 dB	11.1 dB	11.6 dB	10.9 dB	13.4 dB
F/B Ratio:	30 dB	30 dB	20 dB	10 dB	10 dB
Z_{IN} (Ohms):	55 + j40	65 + j55	50 + j65	95 + j86	10 + j6
Overall Length:	.83λ	1.25λ	1.25λ	1.49λ	1.69λ

* Spaced .289λ, .406λ, .323λ and .422λ from driven element and/or preceding director (Ref. 15).

Table 2-8

Expected Optimal Performance of Yagi-Uda Receiving Elements

	Gain (wrt Isotropic) dB	F/B Ratio dB	Receiving Element Reduction Factor*
3 Element-Low F/B ratio	11	5	2.82
3 Element-Moderate F/B ratio	10	15	2.24
3 Element-High F/B ratio	8.5	25	1.58
6 Element-Low F/B ratio	14	5	5.62
6 Element-Moderate F/B ratio	13	15	4.47
6 Element-High F/B ratio	11.5	25	2.82

* Relative to 6.5 dB Baseline Half-Wave Dipole.

possible, structural considerations and diminishing returns on gain improvements indicate that longer elements are not desirable.

A key factor in the Yagi-Uda element design for the SPS would be maximizing gain for a specified F/B ratio. A high F/B ratio would eliminate the ground plane mesh in the baseline design, and possibly lead to principal structural advantages (discussed in Sec. 2.3.2). In order to eliminate the ground plane, a F/B ratio > 25 dB is probably required, in order to insure high collection efficiency and low microwave reradiation past the rectenna. Of course, quantifying the latter specification depends upon multiple land usage. However rotation of the RF field polarization in the ionosphere places a lower limit on the microwave leakage which can be obtained without a ground plane. That is, the perpendicular component would not be affected significantly by the Yagi-Uda receiving element.

If a ground plane mesh is included with lower F/B ratio designs, the electrical performance of the Yagi-Uda element is affected. The ground plane is assumed to be $\sim .25\lambda$ behind the active element, in proximity to the Yagi-Uda passive reflector. Since the "reflector" current distribution will be less spatially concentrated with a ground plane, the antenna pattern is expected to change. However, such a design has not been analyzed to date and was beyond the scope of this initial study. We have assumed that similar performance is available with a ground plane mesh, although slightly higher gain is expected.

With a ground plane included, two alternatives were considered - a 15 dB F/B ratio judged to be appropriate for relaxing electrical requirements on the ground plane mesh and 5 dB F/B ratio requiring excellent ground plane conductivity (as required in baseline rectenna with half-wave dipole receiving elements). With the proposed structural configurations[16] ground plane mesh requirements are not severe. However with (expected) lower cost structural design using mesh held in tension,[17] relaxing electrical conductivity requirements would be desirable.

Based upon this work, Table 2-8 is our best estimate of Yagi-Uda receiving element electrical capabilities and resultant reduction in number of receiving elements. While appreciable analytic and experimental work is needed to verify these particular performance characteristics

(particularly in an array environment), these parameters are sufficiently accurate to evaluate the potential of a Yagi-Uda rectenna. They have been used in the detailed rectenna work described in Section 2.3. Because of an expected significant effect of a ground plane on Yagi-Uda elements having a F/B ratio of only 5 dB, they are not included in our detailed design work in Sec. 2.3. However the larger gain indicates this to be a promising area for further work.

While our emphasis has been on maximizing gain for a specified F/B ratio, additional electrical factors affecting suitability in the SPS rectenna have been considered. Referring to Tables 2-6 and 2-7 the input or radiation impedance of the various designs are presented. In general the Yagi-Uda radiation resistance is less than the half-wave dipole (nominally 73 ohms), which is undesirable for high RF to DC conversion efficiency. The input impedance can be increased by using a folded dipole for the driven element. This is easily included with printed circuit implementation and only slightly more difficult with baseline type implementation. All Yagi-Uda designs described in Sec. 2.3 have a folded dipole as the driven (active) element.

An additional factor affecting SPS implementation of a Yagi-Uda rectenna is the dimensional tolerances involved. As director spacings vary as little as .01λ, F/B ratio can be significantly reduced with the high F/B ratio designs. Fortunately other parameters are not as sensitive to dimensional variations, but parameter tolerances need to be investigated. Certainly less sensitivity is possible if performance parameters (gain and F/B) are "backed off" to some degree. Certainly parameter sensitivity must be examined in future Yagi-Uda evaluations.

2.2.3 Hogline Considerations

During the initial stages of the program, the hogline rectenna concept was explored. However, to avoid duplication of ongoing efforts at Boeing and to allow detailed evaluation of Yagi-Uda elements and printed circuit implementation the hogline effort was curtailed after our interim presentation at JSC. This section of the report presents mostly electrical design considerations that need to be addressed and our preliminary evaluation results. While these considerations may have been evaluated by Boeing, they

are not presented in much detail in the reports available to us.[6,7] Because of our minimal effort on the hogline and incomplete design treatment, a comparison to the baseline rectenna or our alternative concepts presented elsewhere in Chapter 2 is not possible at this time. In this brief discussion familiarity with the hogline antenna concept is assumed.

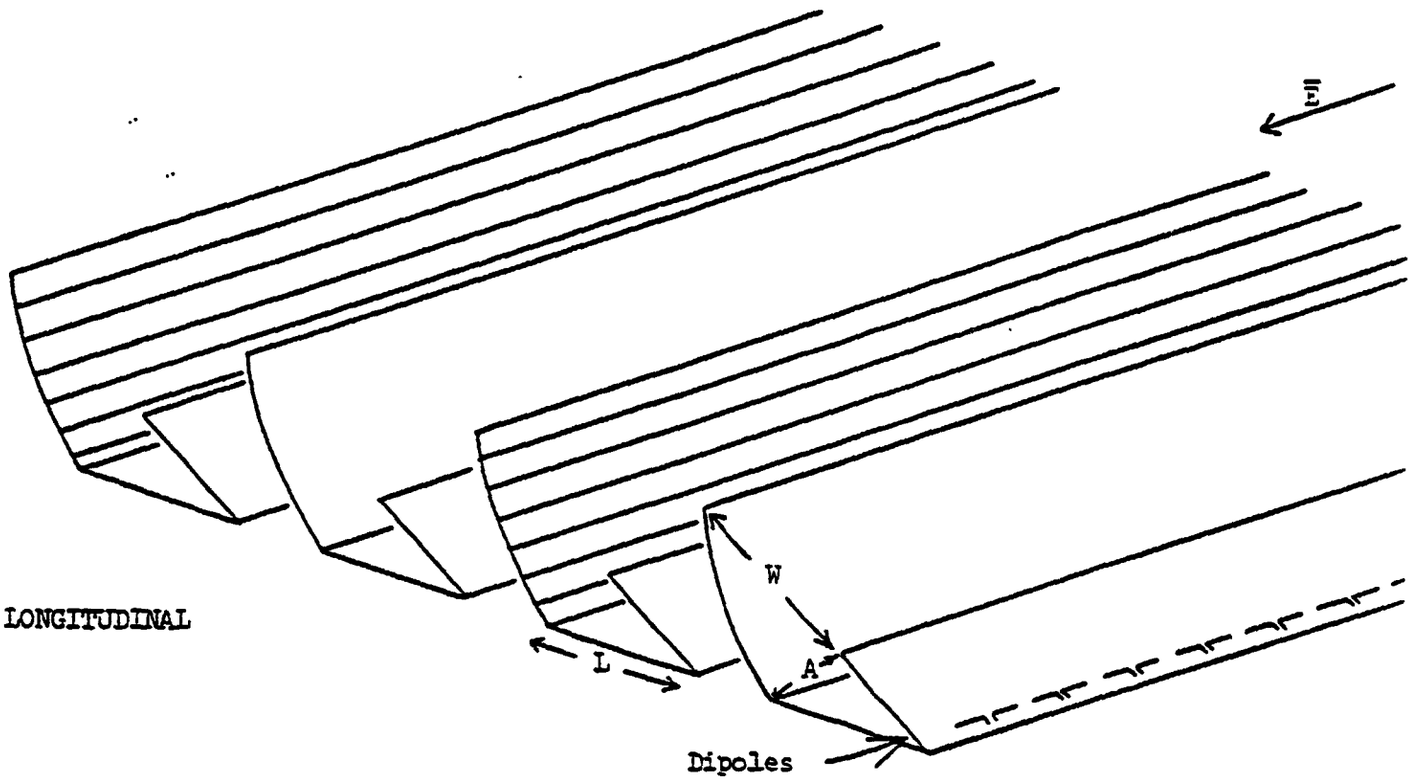
In particular, we will discuss three considerations: the effect of longitudinal versus transverse polarization, the effect of multiple diffraction, and consideration of multiple rectifying elements perpendicular to the focal line. While these factors are interrelated to some extent in the electrical design of the hogline, we find it useful to consider them separately for discussion purposes.

The hogline, a linearization of the hog-horn antenna developed for satellite reception, is depicted in Figure 2-6, in which the parabolic reflector surface is emphasized. The incident power beam can be polarized either in the longitudinal, i.e., parallel to the focal line of the parabolic cylinder, or transverse, i.e., parallel to the narrow dimension (W) of the parabolic reflector aperture plane, direction. For emphasis every other parabolic reflector depicts the conductor requirements with these incident polarizations.

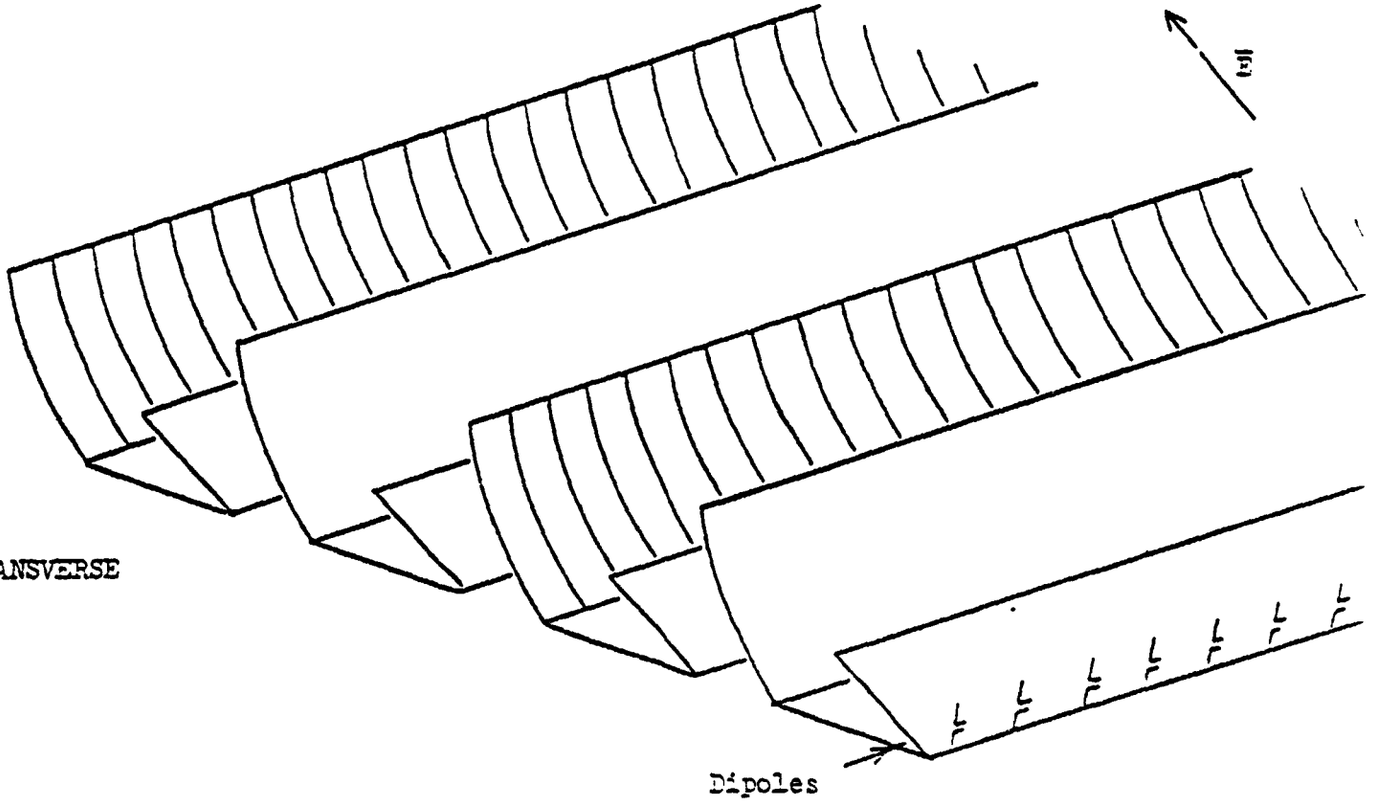
The incident polarizations affect the electrical design appreciably. For example the corner reflector design at the mouth of the inclined plane is polarization dependent.[16] With transverse polarization, the electric field will be perpendicular to the conducting surfaces in the inclined plane region. Therefore, with proper design the power density can be nearly spacially uniform across the region between the inclined planes. With longitudinal polarization the electric field is parallel to these conducting boundaries, so that a TE_{10} mode (rather than a TEM mode) becomes a fundamental mode in this region. Therefore, uniform power density across the inclined plane region is much more difficult to obtain. This uniform power density is particularly important if multiple receiving elements are placed perpendicular to the focal line. This discussion is only approximate as the inclined plane aperture A will probably be in the near field of the parabolic aperture W for high collection efficiency.

However, longitudinal polarization has a more desirable reflector conductor requirement (Fig. 2-6). Since only conductors parallel to the

Fig. 2-6 Hogline Parabolic Reflector Conductor Requirements and Dipole Alignment for Longitudinal and Transverse Polarization



LONGITUDINAL



TRANSVERSE

ground are needed, a light weight structural design with "wires" held in tension appears possible. With transverse polarization a parabolic surface must be formed, so that a conducting mesh may be desired. Naturally a mesh could also be used with longitudinal polarization as well.

A significant difficulty with the longitudinal polarization is DC collection buss requirements. Since the electric field in the inclined plane region is parallel to the focal line, the individual output terminals must be brought through the ground plane. With transverse polarization, the DC collection buss can be parallel to the focal line "inside" the inclined planes, as the electric field is perpendicular to this line. Not protruding through the ground plane is considered a significant advantage.

A fundamental consideration with the hogline is diffraction. Besides diffraction from the top surface of the parabolic cylinder aperture (similar to that from the ground plane in the baseline rectenna), there is a double diffraction from the bottom surface of this aperture (same as top surface of the inclined plane aperture). The latter near field, double diffraction is a complicated problem to analyze and is also polarization dependent. This is considered to be a significant electrical design problem that needs to be addressed in further hogline feasibility studies.

Instead of the simple linear array of receiving elements along the focal line as indicated in Fig. 2-6 , Boeing is proposing a planar array with ~ 10 elements placed across the inclined plane guide[7] (probably symmetrically located with respect to focal line). With this arrangement the field distribution across this plane is of concern. If different elements receive different powers, conversion circuitry inefficiencies can result. This nonuniformity exists even in a first order analysis of the inclined plane-cylindrical parabolic reflector configuration and is expected to be enhanced with the near field double diffraction.

It should be emphasized that none of the above factors have been evaluated in sufficient depth to indicate that efficient power beam reception and RF to DC conversion would not be possible with the hogline. However, in our brief hogline evaluation, they appeared as key electrical design factors that need to be addressed in some detail in any further hogline investigations.

Fig. 2-7A and B Baseline Half-Wave Dipole Rectenna (after Ref. 1)

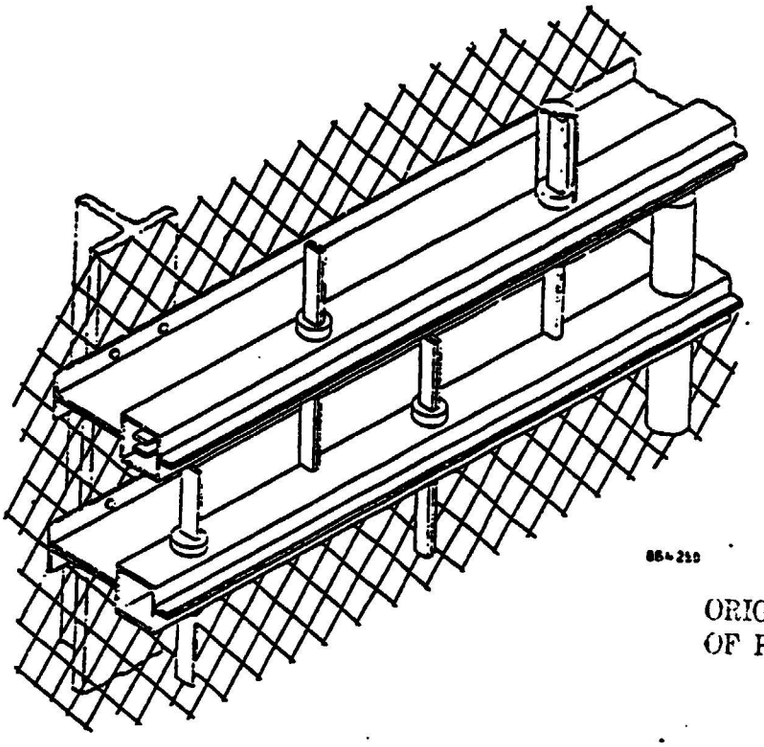


Figure 2-7A Proposed design of Rectenna motivated by environmental protection and cost considerations.

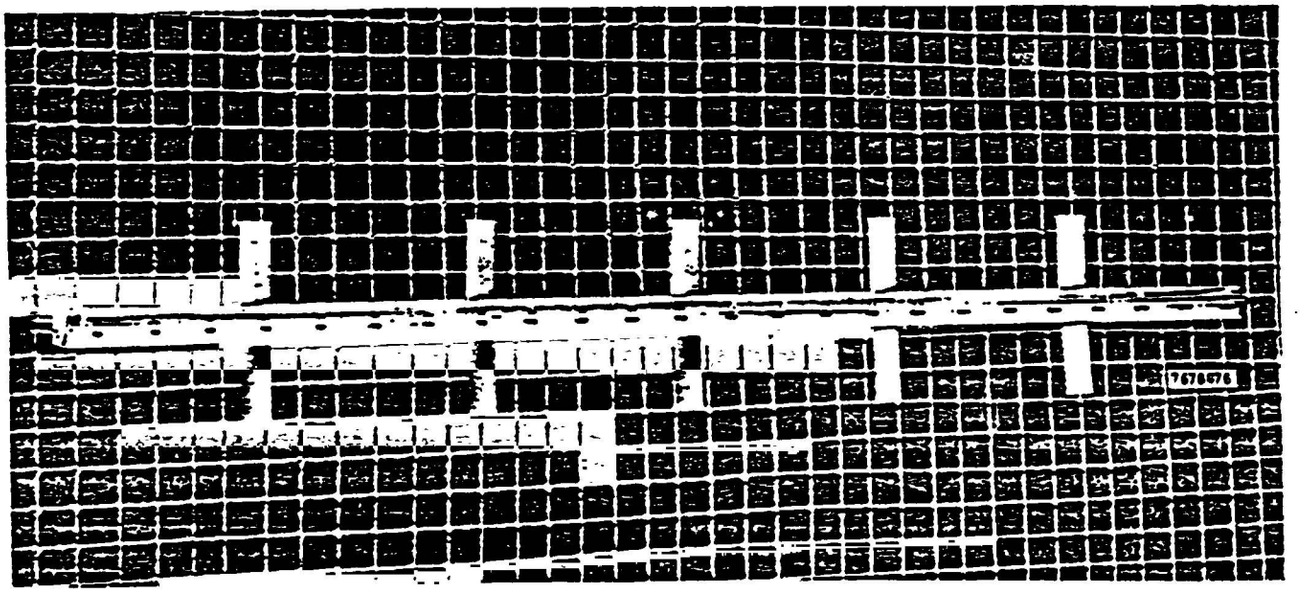


Figure 2-7B Physical construction of two-plane rectenna. With the exception of covers (white teflon sleeves in photograph) this is the same five element foreplane that was electrically tested in earlier work. Reflecting plane made from hardware cloth is representative of what could be used in SSPS rectenna.

Fig. 2-7C and D Baseline Half-Wave Dipole Rectenna (after Ref. 7)

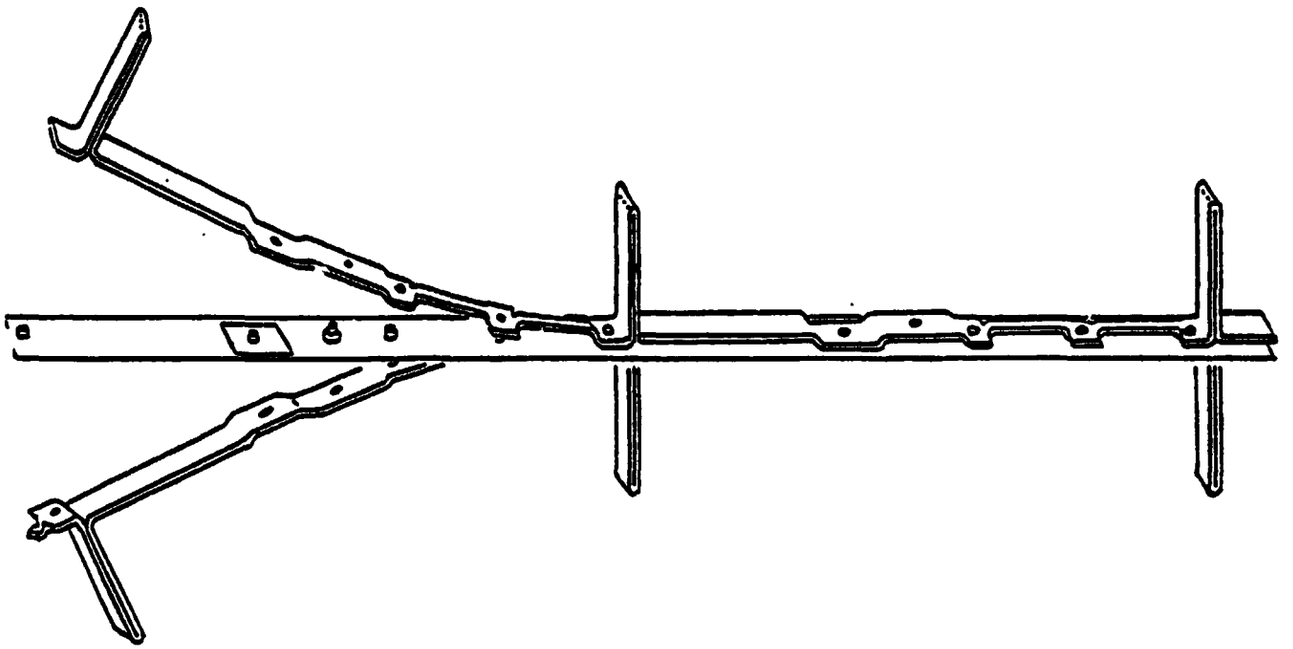


Fig. 2-7C Core Assembly Fabrication

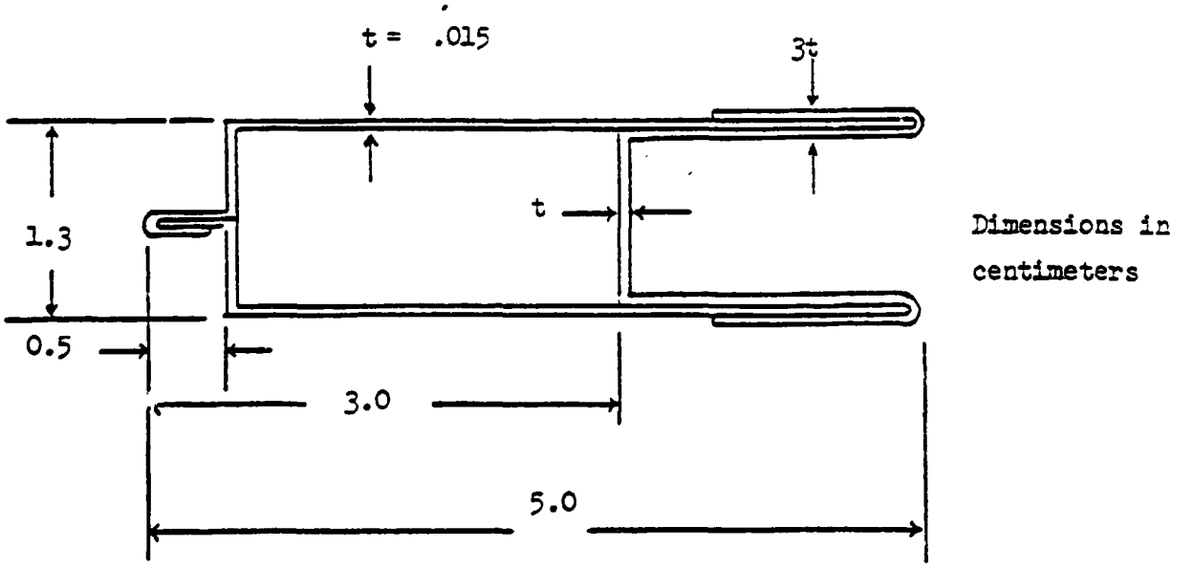
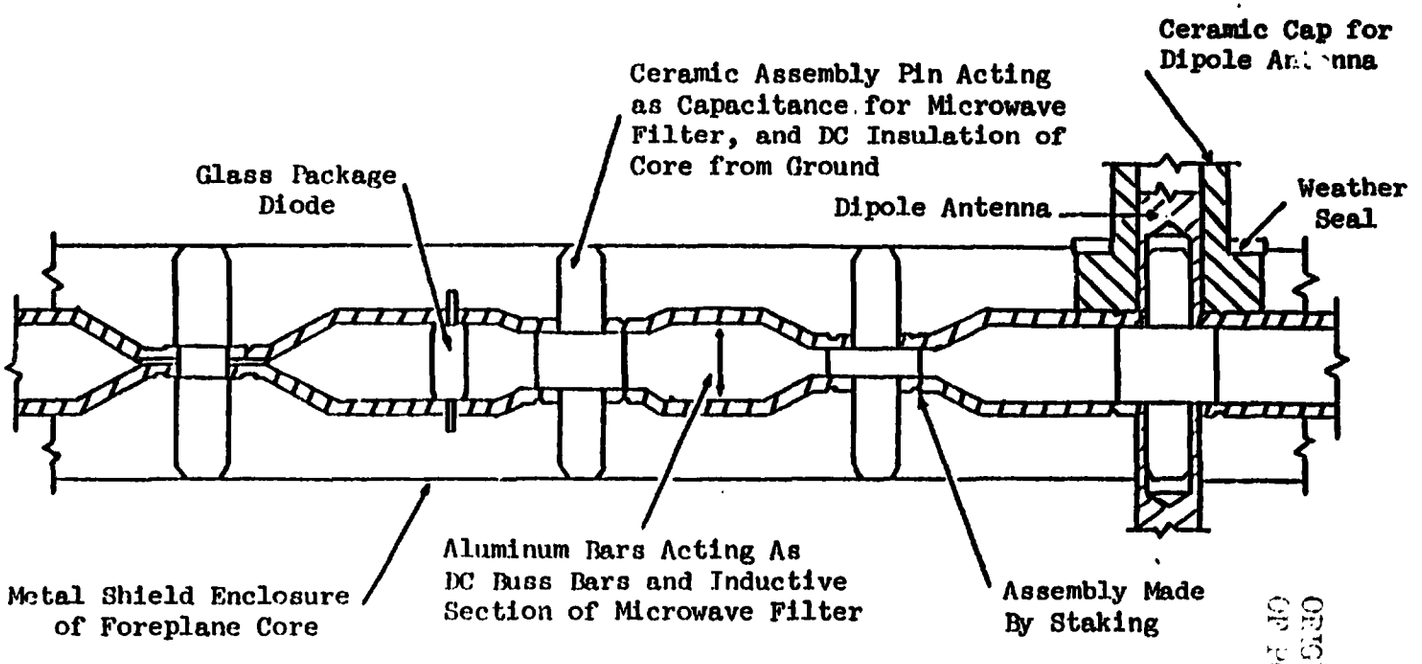


Fig. 2-7D Foreplane Assembly Shield

Fig. 2-7E Baseline Half-Wave Dipole Rectenna (after Ref. 7)

(Foreplane Assembly)



2.3 COMPARISON OF EIGHT RECTENNA ELEMENT DESIGNS

In this section we present design concepts for seven alternative rectenna elements and compare these with the baseline rectenna element. Initially the eight designs are presented with a brief description of each, followed by a general comparison of the designs. Finally cost estimates for the eight designs are discussed. It should be emphasized that the costing methodology developed by Raytheon[1,6] is followed, but resource limitations and relative lack of sufficient design refinement indicate that only tentative comparisons are possible. However more likely alternatives, and relative advantages and disadvantages, clearly appear. We believe the data presented in this section should be used in evaluating future directions of alternative SPS rectennas.

2.3.1 Designs Considered

The eight designs are grouped into half-wave dipoles, 3 element Yagi-Uda rectenna elements and 6 element Yagi-Uda rectenna elements. Our designs with a brief description of each follows:

Half-wave dipoles (baseline construction and printed circuit implementation): The SPS rectenna baseline design as developed by Raytheon consists of a half-wave dipole over a conducting ground plane. The gain of this dipole a quarter wavelength from a ground plane is 5.1 dB with respect to an $\lambda/2$ dipole radiator[17] or 7.25 dB with respect to an isotropic radiator. However, the gain of the baseline dipole in the rectenna array is about 6.45 dB, the slight decrease explained by mutual coupling among the elements in the closely spaced array.

The two plane construction depicted in Fig. 2-7 (A and B) consists of the ground plane mesh and the foreplane, which contains the dipole, circuitry and DC buss (Fig. 2-7C). The foreplane shield (Fig. 2-7D), made from aluminum sheeting, forms the major structural member and provides environmental protection. It is attached to the rectenna frame vertical members and also has the ground plane folded into the foreplane stem. Thus the ground plane has an auxiliary structural purpose besides its function as an antenna reflector.

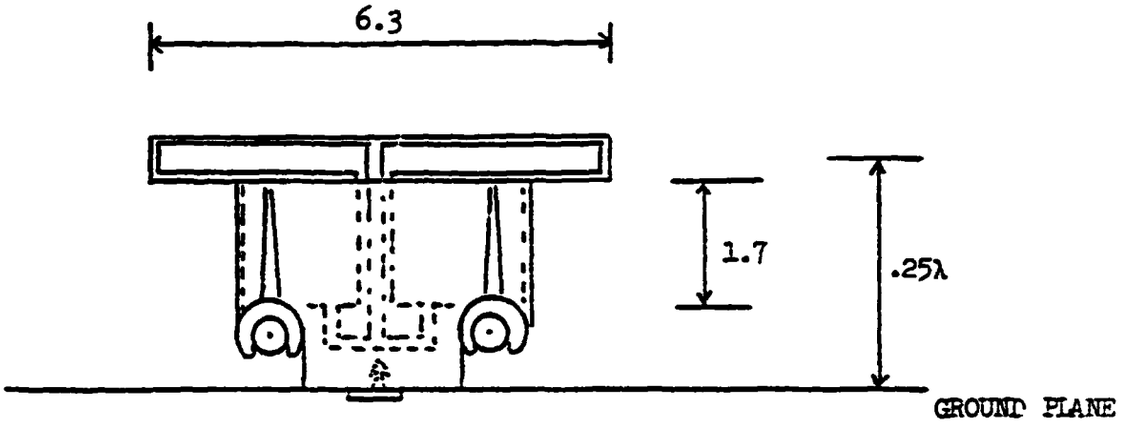
The printed circuit design should have characteristics similar to the baseline dipole since it also is a half-wave dipole over a conducting ground plane. However, because of the smaller conductors, circuit losses are increased with a resultant reduction of about 2-5% in conversion efficiency (discussed in Sec. 2.3.1), an important limitation.

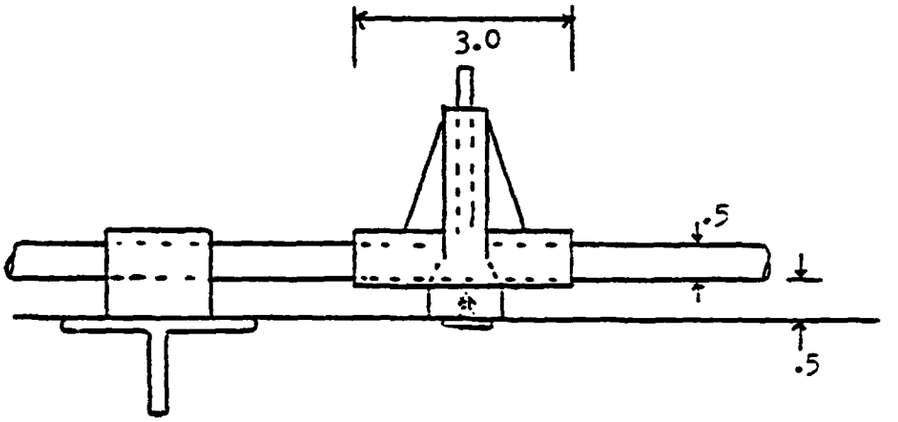
This proposed printed circuit board (PCB) implementation shown in Fig. 2-8 consists of three main parts: the PCB, the PCB socket, and the DC collection buss bars. The PCB has been previously discussed and is depicted in Fig. 2-2. The rectenna frame supports the ground plane and the DC buss bars. The socket extensions also supports the ground plane, keeping it at the one quarter wavelength distance from the dipole. The sockets are made from strong, durable plastic with embedded conducting strips to make the connection between the PCB and the buss bars. The socket clips on and holds tightly to the two aluminum buss bars which are the major structural supporting member of the rectenna element.

Three element Yagi-Uda rectenna elements (with and without ground plane as well as printed circuit and baseline type implementation): Figs. 2-9 through 2-13 depict alternative three element Yagi-Uda elements, based upon electrical design considerations presented in Section 2.2.2. In the printed circuit implementation (Figs. 2-9 and 2-10) the PCB socket with the ground plane is identical to the PCB dipole socket. However with the given dimensions the socket without a ground plane is somewhat larger, because the reflector can be above the DC buss. Recall that penetration through the ground plane is considered undesirable, so that the DC buss bar is in front of the reflector in the design with a ground plane. This extra length for the socket may be an advantage since loading on the PCB Yagi is greater than the PCB dipole. Printed circuit board implementation is shown in Fig. 2-11.

With baseline type implementation (Figs. 2-12 and 2-13) the baseline rectenna is modified in a straightforward fashion. If a ground plane is needed, the Raytheon foreplane is modified into a Yagi by attaching a two-piece plastic support mast for the director. Without a ground plane, the environmental shield is the main supporting member and is attached

Fig. 2-8 Printed Circuit Half-Wave Dipole
(all dimensions in centimeters)





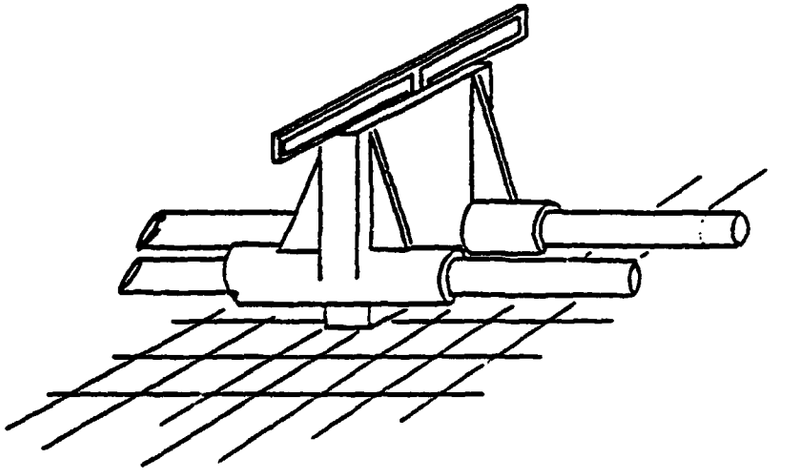


Fig. 2-9 Three Element Printed Circuit Yagi-Uda without Ground Plane (all dimensions in centimeters)

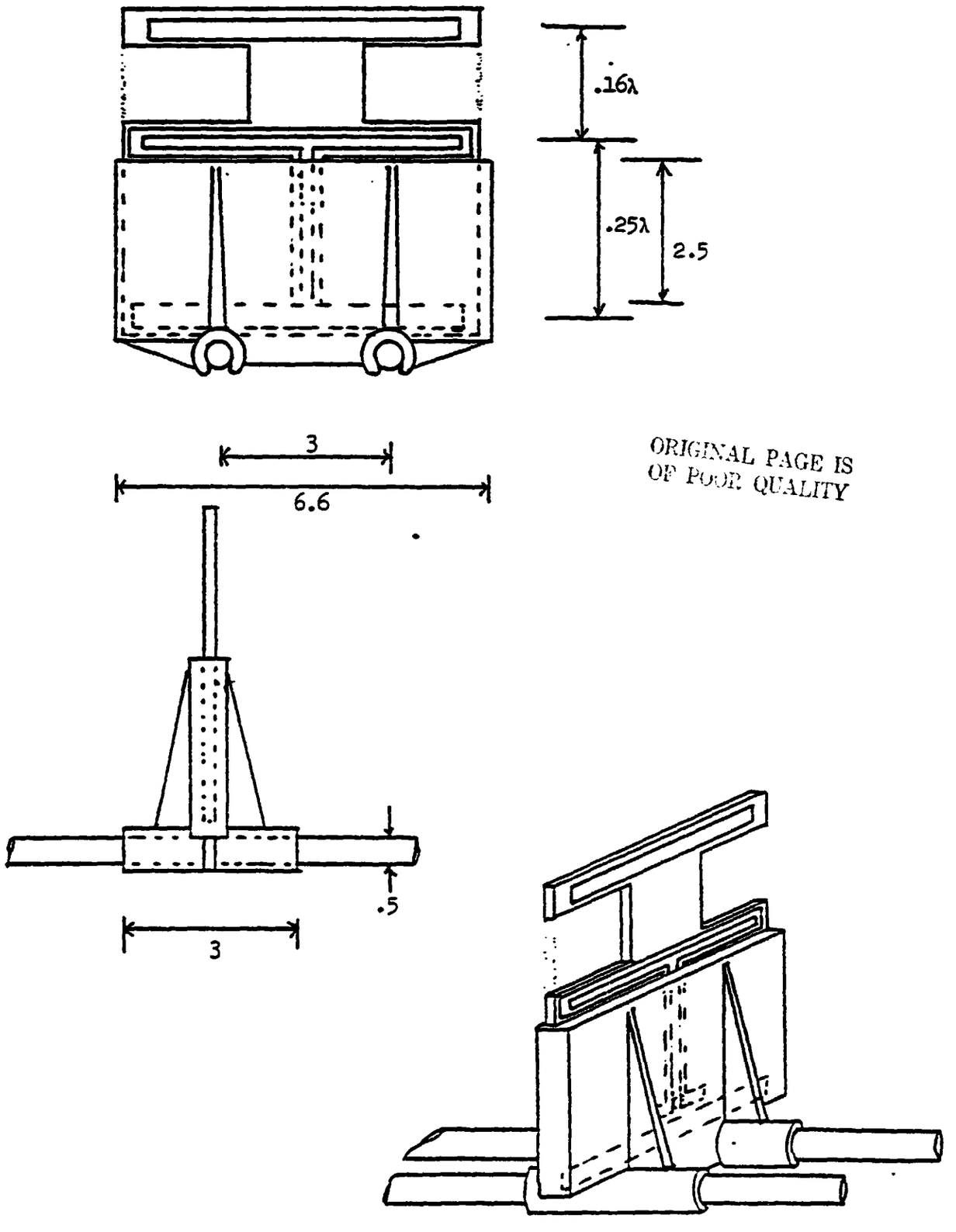
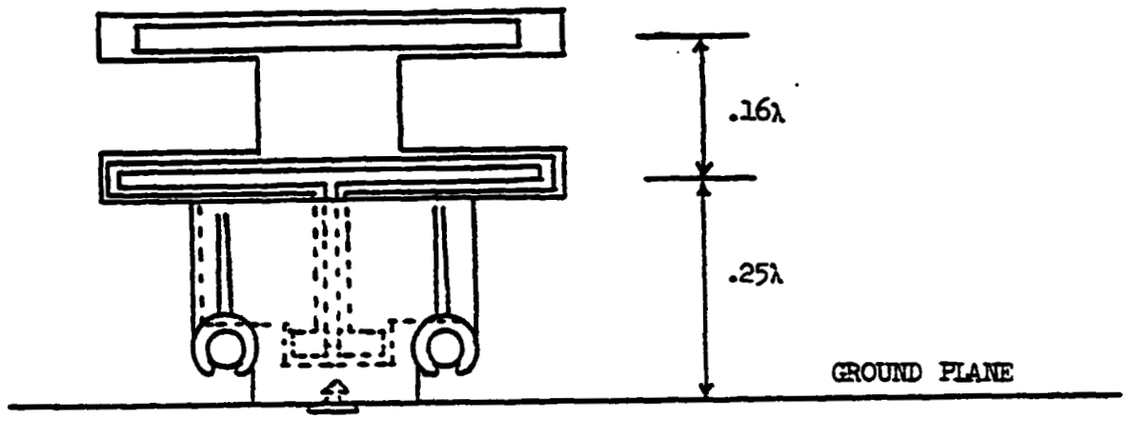
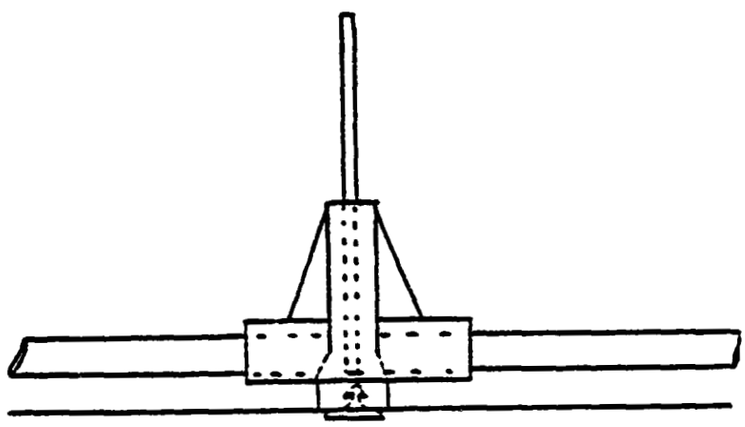


Fig. 2-10 Three Element Printed Circuit Yagi-Uda with Ground Plane





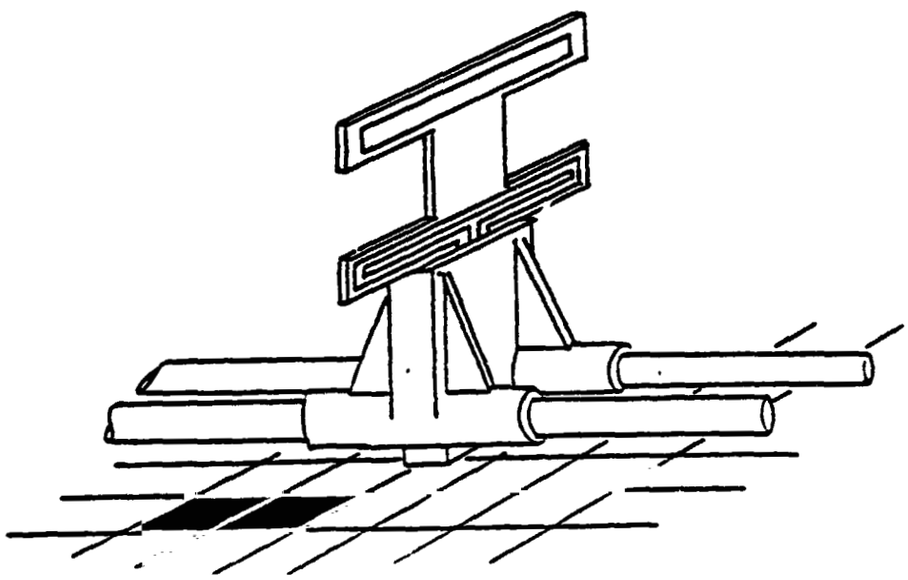
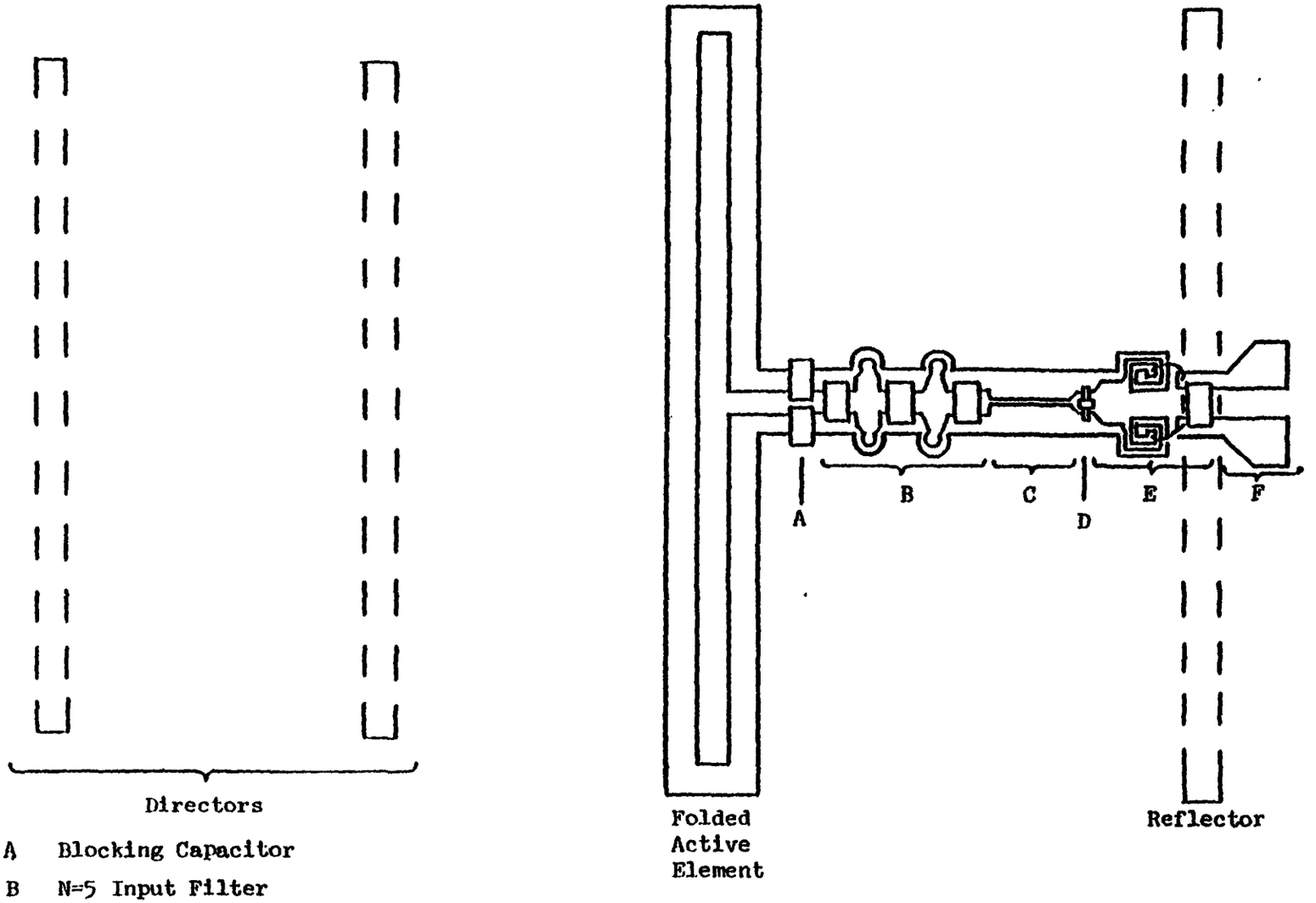


Fig. 2-1a Yagi-Uda Printed Circuit Rectenna Element



A Blocking Capacitor
B N=5 Input Filter
C Harmonic Phasing Transmission Line
D Schottky Diode Chip
E N=2 Output Filter-Transformer
F DC Buss Connector

Fig. 2-12 Three Element Baseline Construction Yagi-Uda with Ground Plane

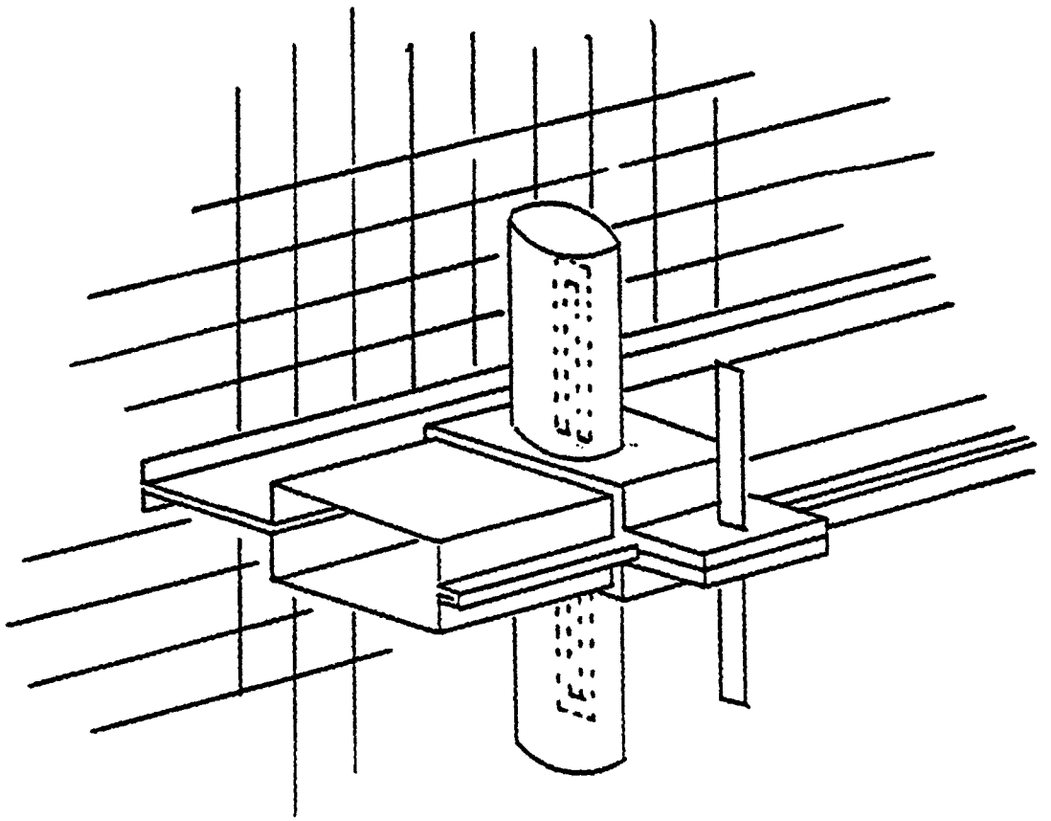
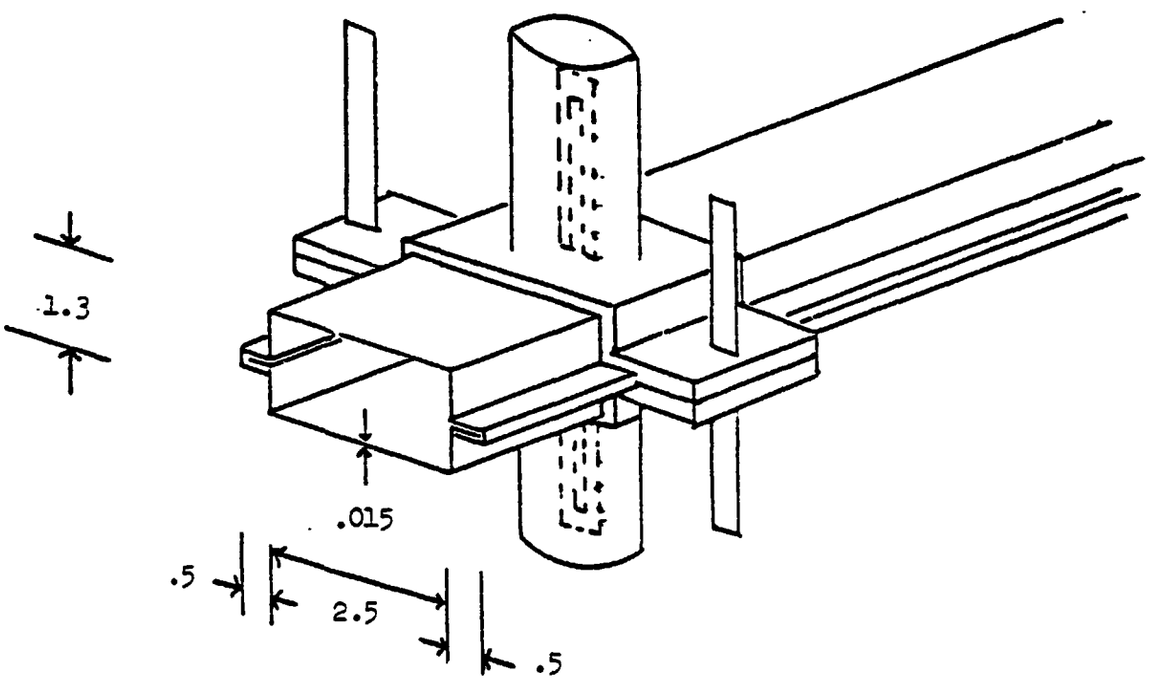


Fig. 2-13 Three Element Baseline Construction Yagi-Uda without Ground Plane (all dimensions in centimeters)



directly to the rectenna frame. The shield is similar to the foreplane shield of the baseline dipole without the stem extended to the ground plane. A two-piece plastic support mast encircling the shield snaps together clamping the passive elements of the Yagi to the active plane.

Six Element Yagi-Uda Elements: With printed circuit implementation (Fig. 2-14) the PCB socket is similar to those already presented (Fig. 2-9) with minor changes in structure to support the longer Yagi-Uda elements and perhaps other changes to accomodate a larger per element power reception (although this is not expected to be needed at this time). The baseline constructed long Yagi-Uda element is also very similar to previously described designs (Fig. 2-12) with exception of minor structural modifications. Detailed designs are given assuming no ground plane. Because of the different lengths of the six element designs (see Table 2-7), two designs are shown in Fig. 2-15 for comparison purposes.

2.3.2 Overall System Comparisons

The list of factors considered in our work and to be discussed in this section include: a summary of electrical considerations (described in detail in Secs. 2.2.1 and 2.2.2), manufacturing, construction and maintenance considerations, environmental factors and multiple land use potential. While priorities are not given explicitly here, they have been described previously in Sec. 2.1.

Because the long Yagi-Uda elements (in this section called "Yagis") are most affected by environmental loading (snow, ice, rain, wind and gravity) and because the long Yagis have the highest gain they need the strongest support and the most accurate antenna pointing. The short Yagis have both lower gain and less environmental loading thus requiring less accurate pointing and less structural support for the element. Naturally, the dipole is the easiest to support and point. Ground settling or shifting of the rectenna frame (or superstructure as it is sometimes called) may become significant as the antenna gain is increased, and satellite beam pointing accuracy must also be reconsidered. As described earlier, system studies to data indicate that higher gain rectenna receiving elements can indeed be accomodated.

Fig. 2-14 Six Element Printed Circuit Yagi-Uda without Ground Plane

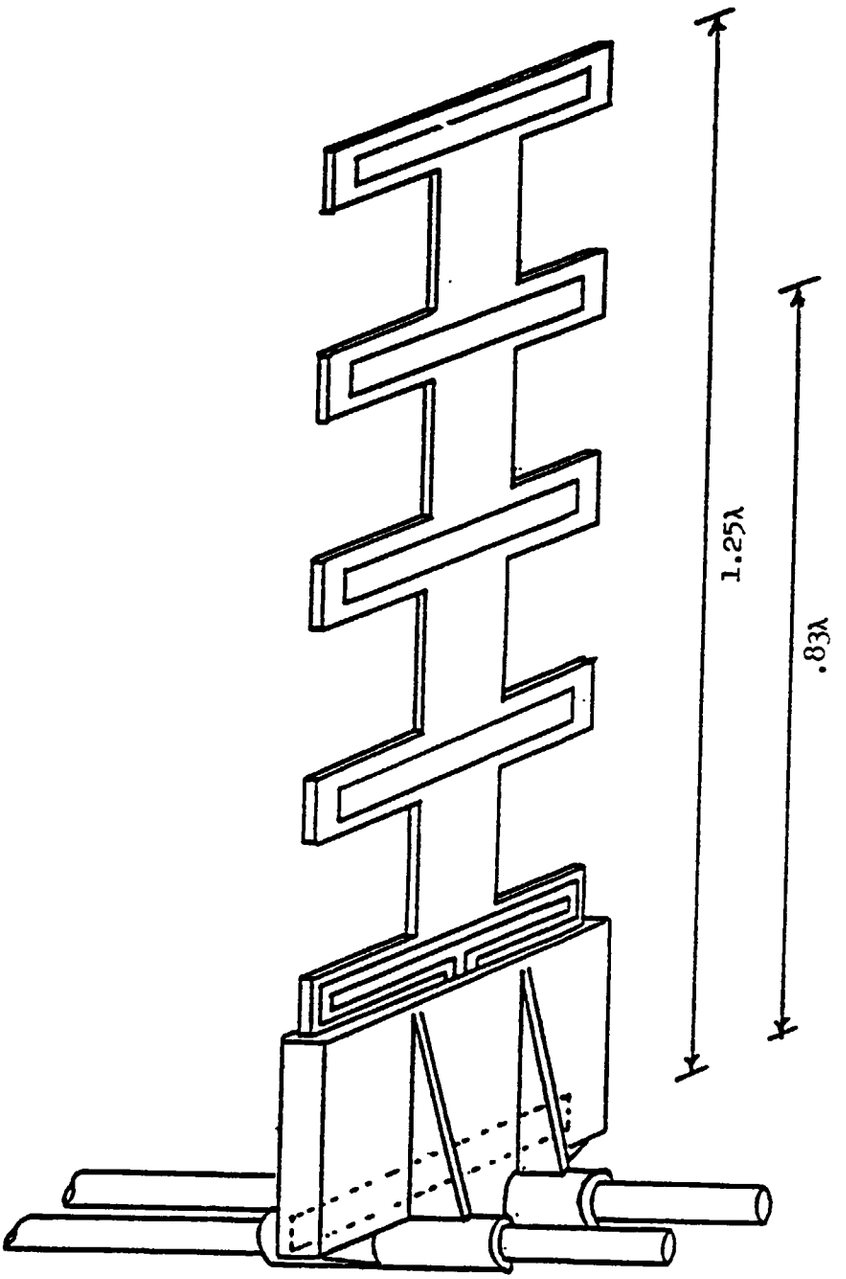
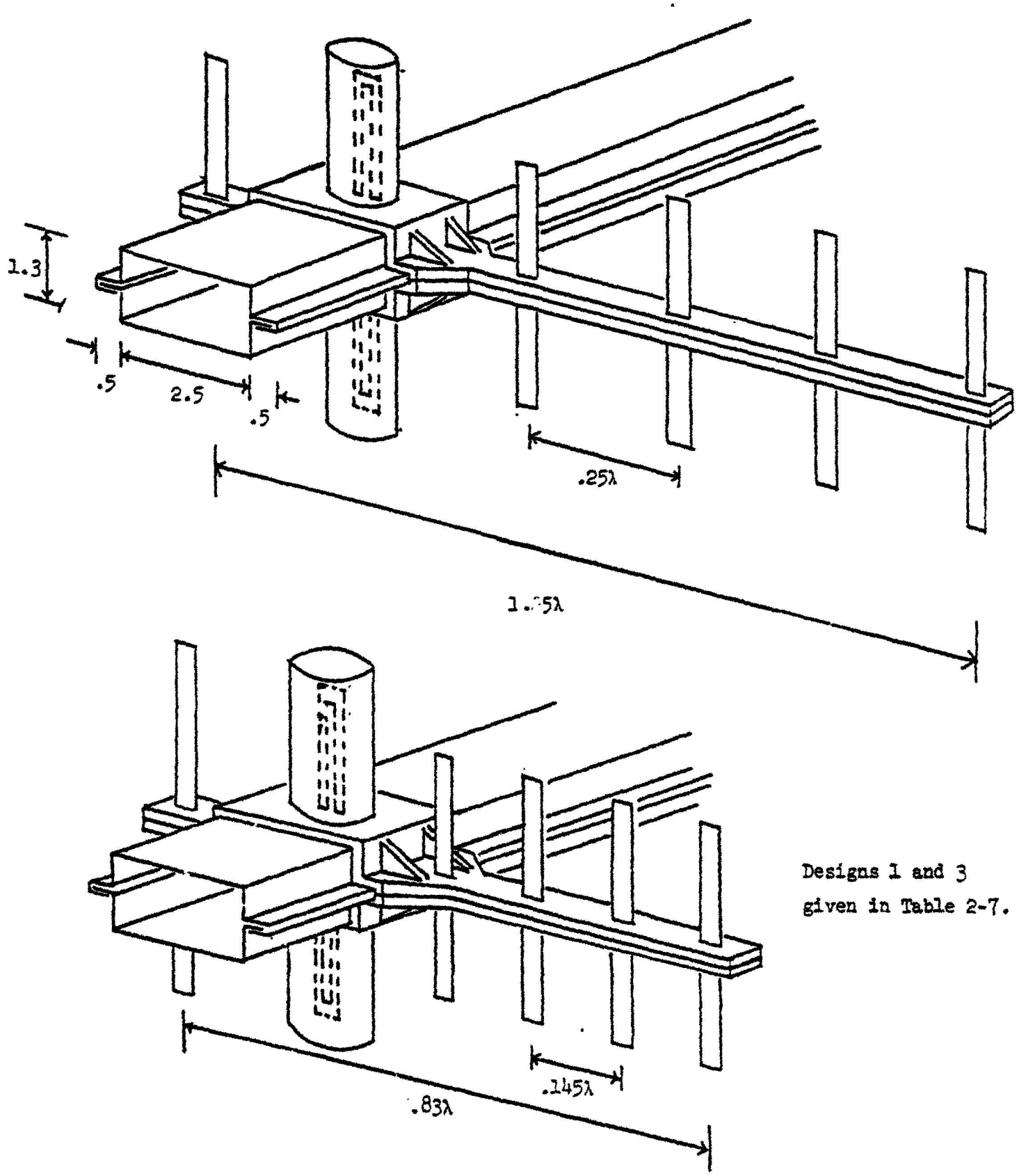


Fig. 2-15 Six Element Baseline Construction Yagi-Uda without Ground Plane (all dimensions in centimeters)



Designs 1 and 3 given in Table 2-7.

The isolated dipole radiation pattern has an F/B ratio of one (0 dB) and therefore depends on a good ground plane to allow a high collection efficiency. With a solid ground plane an infinite F/B ratio is achieved, but a solid ground plane is expensive and structurally undesirable. A mesh ground plane can have a transmission loss > 30 dB and should have a good conducting surface to keep losses in the ground plane low.

Some Yagis have high enough F/B ratios (~ 15 dB) to ease the electrical constrairts (e.g., lower conductivity) on the ground plane mesh. If one wanted to keep losses in the ground plane constant, the smaller amount of induced currents in the ground plane when using a higher F/B ratio allows the mesh material to have a higher resistance, alleviating one constraint on the mesh materials.

Some Yagis have high enough F/B ratios (~ 25 dB) to consider elimination of the ground plane (discussed in Section 2.2.2). The ground plane adds rigidity to the rectenna frame and provides structural support for the baseline constructed dipole and Yagis but it adds weight and material costs. It is also susceptible to environmental loading and a source of shading. For these reasons it might be desirable to dispense with the ground plane where adequate support can be given to the rectenna elements and, of course, the F/B ratio is high. Of course, multiple land use issues impact F/B ratio requirement and Faraday rotation in the ionosphere must be considered. The variety afforded by the wide range of gain and F/B ratio possible with Yagis (Table 2-8) allows the selection of a suitable design governed by more rigorous study of the physical and electrical limits of the rectenna structure.

The higher gain antennas have a higher microwave power input to the diode. Since the present Pt-GaAs Schottky rectifiers are capable of improved conversion efficiency at higher power levels (2 to 5 watts instead of 1 watt as in the baseline rectenna), improved performance results. If the antenna gain is increased so the rectifiers operate above 10 watts, then diode reliability and/or circuit design must be reevaluated.

In PCB antennas conductor losses are greater than in the baseline because the PCB conductors are thinner. Although the higher conductivity of copper over the aluminum (factor of 1.64) does compensate, we conclude

a 2 to 5% conversion efficiency penalty results with printed circuit implementation (Sec. 2.2.1). Because the DC buss is the main structural support in the printed circuit board implementation it will have a larger cross sectional area than its baseline buss counterpart, resulting in lower DC collection losses. The baseline dipole rectenna has a per element resistance of $1.72 \times 10^{-3}\Omega$, while the five millimeter diameter DC buss for the PCB dipole implementation has $0.22 \times 10^{-3}\Omega$ per element, indicative of possible reductions.

The higher gain antennas have larger effective areas, thereby increasing spacing between the rectenna elements. This increased distance is important for the baseline constructed designs where the conversion circuitry is positioned between the elements (two plane construction). The extra room allows additional harmonic filters to be included. In addition, the increased spacing reduces the number of rows of foreplane or DC bussing by a factor between 1.3 and 2.4 with either printed circuit or baseline type implementation (depending upon number of directors and F/B ratio).

Besides these electrical factors, manufacturing and constructing a rectenna plays a large role in overall rectenna feasibility and cost. In the following comparison between baseline construction and PCB implementation the rectenna frame (or superstructure) is assumed to be similar and is not discussed. Although we recognize that superstructure differences may exist with and without ground planes and with different type element realizations, we believe element cost differences will dominate. Therefore we stressed this evaluation. The erection of the rectenna frame is a different phase of construction and is assumed to be independent of our evaluation.

The foreplane core of the baseline constructions designs is fabricated from two continuous aluminum strips sandwiching a middle strip containing the dielectric for the capacitors and the diodes. The foreplane shield/structural member is formed around the core from three sections of sheet aluminum. The dipole caps and seals are then fitted completing the foreplane. The long strip of foreplane is attached to the rectenna frame by folding the ground plane between the open ends of the foreplane stem and then rolling and indenting the whole assembly.

The fabrication of the foreplane and its attachment to the ground plane are two separate assemblies. However, if it were possible, with the long lengths of the aluminum foreplane sheeting, to form the foreplane shield and attach it to the pre-folded ground plane far enough behind to prevent buckling there would be less time spent on each section of the rectenna. This eliminates moving and positioning completed foreplanes to be attached to the ground plane in a different phase of construction.

The printed circuit board implementation consists of three parts: PCB, PCB socket, and the DC buss bars. The PCB's and the sockets are manufactured most likely near the rectenna site and batches are sent to the moving assembly factories. Rolls of the DC buss bar material are brought to the assembly factories where they are either notched or modified to suit the assembly procedure. The whole width of one rectenna slat is constructed at the same time. The required number of horizontal buss bars is unrolled, straightened, notched at intervals of the appropriate element spacing, and perhaps the last stages of its material properties treatment is performed (e.g. cold working). Attaching the buss bars to the rectenna frame is easily done by insulating fittings. The PCB is plugged into the socket and a weather seal is fitted at the junction of the PCB and the socket entrance. With the buss firmly in place the socket/PCB is then clipped onto the buss. The notch not only guides the element spacing but prevents the socket from sliding along the bar.

The socket should be able to provide excellent support for the PCB and should grip the DC buss fairly well. Its square base makes it stable in all directions. Another function of the socket is the effective transition from the PCB contacts to the DC buss bars. This is accomplished by two copper or aluminum strips embedded in the plastic, exposed where it contacts the PCB and around the inside of the clips where the buss bars run. If keeping the diode from overheating is a problem (one that increases with a higher gain element) and the socket plastic does not have a high enough thermal conductivity a heat sink can be embedded above the diode during socket fabrication (not needed with current parameters in our opinion).

The baseline designs and the PCB implementation utilize both continuous and modular construction to varying degrees. In the baseline design a completed foreplane rolls out continuously but is modular because it has a finite length. An estimate of the foreplane lengths was 200 meters.(7) In the PCB implementation the DC buss bars can be continuous for a large distance. The modular aspect naturally is the socket and PCB units. A pure continuous construction can be made stronger and, if not too complex, is also faster. However, mistakes hold up construction and, if maintenance is ever required, pure continuous construction makes replacing parts difficult. Pure modular construction could also be difficult to replace parts by the great numbers of units. This is also its main disadvantage for assembly since large amounts of individual modules must be handled. But pure modular construction more easily effects quality control measures and corrections of machinery malfunctions before making it part of "permanent" rectenna structure.

PCB Yagis are easily made and involve no more or little effort than making a PCB dipole. For Yagis used over a ground plane only the directors and the dipole need to be etched and this can be done on the same side. This is recommended to insure that the maximum gain of the Yagi pattern is in the same direction as that in which the PCB is pointing. The four directors on the six element Yagi can be on either side of the dipole because the travelling wave follows the director plane which is parallel to the PCB. Naturally, the reflector on PCB Yagis is on the other side of the active dipole to avoid the conversion circuitry.

Baseline construction Yagis fall into two categories: with ground plane and without. Both are modifications of the Raytheon foreplane but the Yagis without the ground plane remove some of the difficulties in construction. The main difference is that the Yagi foreplane is supported in the active plane where the bulk of the weight is centered and not from the ground plane, as in the baseline dipole, which produces undesirable moments. Construction is faster because there is no ground plane to fold into the foreplane stem which is not done in line with the continuous fabrication of the foreplane. Modification is easily done by snapping on the support mast and then inserting the passive elements.

Manufacturing tolerances are more important for Yagis than dipoles (discussed in Sec. 2.2.2) since there are more dimensional variables (spacing, radii, and lengths of all the antenna elements) which have to be controlled and some quite closely. In this regard the PCB antennas are best and the baseline dipole reasonable, with three element and six element baseline constructed Yagis expected to be somewhat difficult to control. Yagi tolerances are more critical at high F/B ratio, as discussed in Sec. 2.2.2.

Besides manufacture and construction, maintenance of the rectenna of a 30 year life requirement needs to be considered. It is expected that individual failure of elements will not accumulate to a large enough number to require replacing the defective parts. However, if no precaution is taken to prevent domino effect failures or multiple catastrophic failures (such as lightning storm damage) large sections may become inoperable, in which case it might be cost effective to repair these sections. The cost of replacement is probably much greater than the initial assembly cost per element because of the special nature of the repair. Mulitple land use and RFI considerations must also be evaluated when evaluating repair options. At this stage all designs have similar maintenance features, although the two plane continuous construction may be more difficult.

Environmental factors come under two categories: structural loading and environmental protection considerations. Structural loading from the weather and environmental considerations will vary with rectenna location. In this report environmental conditions typical of Northeast United States are assumed.

From loading considerations, it is most desirable to have the heaviest member as the primary supporting structure of the elements. Extensions should be lightweight and strong to withstand loading. Thus, long Yagis in both types of construction have the most problems with loading. Therefore, the socket is made relatively stronger (or longer) in the PCB case and the support mast is made more rigid in the baseline case. PCB dielectric cut from in between the directors on the Yagis will alleviate much of the loading especially on the long Yagis. Of course, a central dielectric stem of good width is left to connect the directors. In short Yagis without ground planes, the reflector helps counterweight the directors.

The foreplane shield in the baseline constructed designs is horizontal for construction continuity but is acted on by gravity and other environmental loads. Thus environmental protection constraints require the solid construction of the baseline designs. The baseline constructed Yagis without the ground plane would withstand loading much better because the heavy foreplane is supported in the active dipole plane, where most of the weight is, instead of at the ground plane. The dipole and the three element printed circuit Yagi in the socket forms the stronger designs.

The methods for environmental isolation should protect the circuitry from weather and keep radio frequency interference (RFI) generated by the harmonics of the diode from escaping while allowing adequate cooling of the diode. Baseline construction performs all three functions reasonably well. From the discussion on PCB socket design weatherproofing and the heat sink are no problem. RFI, however, would not be stopped by the plastic. It could be reduced by using a high loss plastic in the dipole sockets and ground plane Yagi sockets or possible in the exposed reflector sockets as well. With existing dielectrics there would be too much loss at the fundamental frequency, 2.45GHz, if second and higher order harmonics were to be suppressed. However, if a dielectric could be developed with a low pass capability, low loss at the fundamental and high loss at higher frequencies, and had good structural qualities, radiation of RFI would be greatly reduced. Of course, in all cases harmonic reradiation is of spectral concern.[7]

Because of the large amount of real estate required for one rectenna the idea of multiple land use has received attention as a means of increasing the monetary output of each acre. Each different land use will have its own definition of how much microwave radiation or sun shading is tolerable. But in many cases the amount of microwave power allowed to pass through to the ground will probably be the same for ecological reasons (or for favorable biological consequences). However, some economical considerations and enough leeway in the safety standards may prove otherwise. In any case, if shadowing is important the methods used to achieve certain microwave intensity levels will affect the amount of shading (e.g. different mesh dimensions in the ground plane or going to long PCB Yagis with high F/B ratios).

Shading is a difficult factor to compare at this stage of our design. Fortunately, a good ground plane with 33 dB transmission loss has about 80% transparency.[18] The foreplane shield has a sizable amount of shading and fortunately is horizontal in an east-west orientation. Recall that the rectenna faces south toward the satellite in near zero inclination orbit. In the PCB implementation, since the DC buss runs east-west for constructional ease, the PCB's must be aligned north-south to avoid inducing time varying currents in the buss. North-south PCB's will have more shading. In general the antenna designs which contribute the most shading per element have the least number of elements. To first order these may cancel but the less bussing involved favors the more directional elements.

Clear plastic is used for the PCB socket but since the PCB is buried deep in the socket there is about 50% of the socket still opaque. The development of a clear dielectric for PCB application would alleviate this problem if it became considerable enough to justify the research and development costs. This would find most use in the long Yagis which cannot afford to have too much dielectric cut away between the directors.

2.3.3 Cost Comparison

Although appreciable design work is needed to evaluate the approximations and judgements discussed throughout Chapter 2, it is desirable to provide as accurate cost estimate as possible to serve as a guide in properly allocating future resources. This section describes the cost methodology and results with the eight rectenna elements described in Section 2.3.2.

The cost analysis followed the percent estimates provided by Raytheon for the baseline rectenna.[7] For baseline type constructed rectennas with Yagi elements, the results are expected to be of similar accuracy. Although more Yagi structural design is needed, additional material and construction costs are not expected to be too significant. However, with printed circuit implementation cost estimates are more approximate. In particular the socket costs and DC buss bar sizing requirements are difficult to quantify at this time, as structural loading requirements have not been designed. Thus our results should be considered preliminary only, with additional work certainly necessary.

However, even with these appropriate qualifications, we believe the results indicate which designs are most worthy of further investigation. In particular, the expected strong correlation between rectenna element directionality and rectenna cost is clearly indicated.

The rectenna element density used for the cost estimates are shown in Table 2-9 for the half-wave dipole and various Yagi configurations. The gain values have been discussed in Sec. 2.2.2 and are equal (except for round off differences) to the extrapolated performance given in Table 2-8. Other values in this key table can be calculated from geometric considerations, assuming elements are placed in a triangular grid as in the baseline.

The resultant costs obtained are presented in Table 2-10. The trend toward lower cost with increased rectenna element gain is clearly apparent. The comparison between baseline construction and printed circuit implementation is less apparent. The printed circuit estimates are based upon less detailed design, but these results do not indicate a substantial reduction with printed circuit implementation. Only if socket and DC buss bar cost can be reduced will a large cost advantage result. These will probably be possible only with careful structural designs requiring less material usage and low cost manufacturing.

Cost estimates for the printed circuit board, PCB sockets and related DC buss bar are given in Table 2-11 through 2-13 respectively. Note that raw material costs only are included, as manufacturing complexity and related costs are assumed low. However design refinements to reduced cost, such as elimination of gold flashing in non contact areas, reducing dielectric thickness below 1/16", and reducing buss bar diameter, are not included The feasibility of the two latter, critical factors depends on structural considerations beyond the scope of the present program.

From these cost estimates it is apparent that the DC buss bar, ground plane where needed and GaAs diodes dominate the rectenna element cost with printed circuit implementation. However the socket design and cost in particular needs additional work and the DC buss bar structural support warrants further study.

With the baseline constructed rectennas the latest Raytheon[7] estimates were used, and additions to form the Yagi-Uda elements

Table 2-9 Rectenna Element Density Used in Cost Estimates

	Half-wave Dipole	3 element Yagi		6 element Yagi	
		with ground plane	without ground plane	without ground plane smaller size	larger size
Gain with respect to isotropic (dB)	6.5	10.2	8.4	11.11	12.7
Gain ratio with respect to isotropic	4.4	10.4	6.8	12.7	18.4
Effective Area, A_e (cm^2/element)	52	123	81	150	218
Element Density (No. of elements/m^2)	192 (≈200)*	81	123	67	46
Density Reduction Factor	1	2.37	1.56	2.87	4.17
Element Spacing (cm) (on triangular grid)	7.8	11.9	9.7	13.2	15.9
Rows of DC Buss/m	14.9	9.7	11.9	8.8	7.3

$A_e = \frac{G\lambda^2}{4\pi}$ -- G is the gain ratio with respect to isotropic.
-- A_e is the effective area of the rectenna element.

The baseline had all other parameters derived from the element spacing, the reverse of what is done here for the rest of the elements.

* used in Raytheon estimates.

A. PCB Implementation

(costs are given in $\$/m^2$)

	Half-wave Dipole	3 element Yagi with ground plane	3 element Yagi without ground plane	6 element Yagi without ground plane (average size)
Element Density ($\frac{elem.}{m^2}$)	192	81	123	57
Socket	$ .92	$ .39	$1.12	$ .52
DC buss bar	2.78	1.81	2.23	1.55
PCB (less diode)	.24	.24	.42	.44
Ground Plane	1.91	1.91	.00	.00
Cost/m^2	$5.85	$4.35	$3.77	$2.51
Diodes at $.01 each*	$1.92	$ .81	$1.23	$ .57
Total Cost/m^2	$7.77	$5.16	$5.00	$3.08

B. Baseline Type Construction

(costs are given in $\$/m^2$)

	Half-wave Dipole	3 element Yagi with ground plane	3 element Yagi without ground plane	6 element Yagi without ground plane
Element Density ($\frac{elem.}{m^2}$)	192	81	123	57
Foreplane Core	$3.13	$1.47	$2.09	$1.09
Aluminum Shield/ Structural Member	2.14	1.40	.92	.64
Yagi-Uda Additions	.00	.30	.71	.76
Ground Plane	1.91	1.91	.00	.00
Cost/m^2	$7.18	$5.08	$3.72	$2.49
Diodes at $.01 each*	1.92	.81	1.23	.57
Total Cost/m^2	$9.10	$5.89	$4.95	$3.06

* Large cost uncertainty with probability of lower cost package with PCB implementation

Table 2-10 Overall Cost Estimates

Table 2-11A Cost Estimate for Printed Circuit Boards

	Half-wave Dipole	3 element Yagi with ground plane	3 element Yagi without ground plane	6 element Yagi (long) length = 1.25λ
Area ($in.^2$)	2.015	5.54	6.25	15.6
Volume ($in.^3$)	.126	.346	.391	.98
Weight (lb.)	1.483×10^{-2}	4.05×10^{-2}	4.59×10^{-2}	11.51×10^{-2}
% of Total cost of				
1. dielectrics	58.4	70.3	66.7	74.2
2. copper	1.2	0.9	1.1	0.9
3. gold	40.4	28.8	32.2	24.9
Total Cost/element	.127¢	.289¢	.343¢	.772¢

NOTES: 1. Diode cost not included.

2. Copper is small percentage of cost (assuming copper etched from P.C. boards and reused at no cost). Therefore more area on the board could be used to reduce losses if no ill effects from changing impedance levels.

3. Gold flashing may only be needed at the D.C. contacts. The dielectric coating may be adequate to protect copper from corrosion.

4. Biggest cost factor is the dielectric (thickness of 1/16" is assumed). Some cutaway is possible between the directors of Yagis, but not at the base since this region fits into socket. Cutting away of dielectric is not considered in the calculations so Yagi costs would be less. Dielectric is assumed to be recyclable.

Table 2-11B Detailed Cost Estimate for Half-wave Dipole with Printed Circuit Implementation

area: (1 cm. x 2.5) + (1.5 x 7) = 13 cm^2 = 2.015 $in.^2$

volume: (2.015 $in.^2$) (1/16 in.) = .126 $in.^3$

copper -- (.5 mils thick): (2.44 in. + 1 in.)(.050) x (.5 x 10^{-3}in.) = 8.6 x $10^{-5}$$in.^3$

gold flash -- (250 $\mathring{A}$): (2.44 in. + 1 in.) (.050) (10^{-6}) = .15 x $10^{-6}$$in.^3$

capacitors: 4 (.050 x .050 x .025) = .25 x $10^{-3}$$in.^3$

two gold bond wires (1 mil.): $2(\pi(.001)^2/4)$ (.050) = 7.85 x $10^{-8}$$in.^3$

dielectric coating: (2.015 x .005) = 10.1 x $10^{-3}$$in.^3$

Weight Calculations = (specific gravity) (density of water) (volume)

dielectrics -- 3 (62.4) $(1/12)^3$ (126 + 10.1 + .25) 10^{-3} = 1.48 x 10^{-2} lb.

copper -- 8.9 (62.4) $(1/12)^3$ (8.6 x $10^{-5}$$in.^3$) = 2.8 x 10^{-5} lbs.

gold -- 19.3 (62.4) $(1/12)^3$ (150 + 78.5) 10^{-9} = 1.6 x 10^{-7}lb.

TOTAL = 1.483 x 10^{-2}lb.

	Cost	% of total cost
dielectrics (polyethylene 5¢/lb.)	\$7.4 x 10^{-4}	58.4
copper (56¢/lb.)	1.57 x 10^{-5}	1.2
gold (\$200/ounce)	5.12 x 10^{-4}	40.4
	\$1.27 x 10^{-3}	

or 0.127¢ (per PCB without diode)

Table 2-12 Cost Estimate for PCB Socket

material - Delrin (an acetal resin) : specific gravity ≈ 1.43 (acetal plastic) ; estimated cost : $.15/lb.

	type 1 (with ground plane)	type 2 (without ground plane)
volume --	(3 x 4 x 0.6) = 7.2 cm^3	(4 x 6.5 x 0.6) = 15.6 cm^3
weight --	$1.43(62.4)(1/12)^3(\frac{1}{2.54})^3(7.2)=.02269$	(0.00315) (15.6) = 0.04914 lb.
cost --	(.02269) ($.15) = $0.0034 or .34¢	(0.04914) ($.15) = $0.00737 or .737¢

Two 1-1/2" aluminum conductor strips, 20 mils thick; specific gravity = 2.7; cost $.80/lb.

volume = (2) (1.5) (1/8) (.020) = 0.0075 $in.^3$

weight = 0.00731 lb.

cost = $0.000585 or .059¢

resistance = $1.33 \times 10^{-3} \Omega$

Weather Seal: silicone rubber; for soft commercial rubber 69 $lb./ft.^3$; cost $1.00/lb.

volume = 2 (6) (.2) (.2) = .48 cm^3

weight = 0.00117 lb.

cost = $0.00117 or .117¢ type 2
and .078¢ type 1

	type 1 (w/G.P)	type 2(w/o G.P.)
TOTAL COST	.477¢/socket	.913¢/socket

NOTES:
1. Seal may be considerably smaller if only sealed where circuitry had to pass through entrance slot of the socket.
2. Aluminum conductors could be made larger to lessen losses.
3. Heat sink, if needed, is not considered.

Table 2-13 Cost Estimate for DC Buss Bars for Printed Circuit Implementation

Two aluminum rods with 5mm diameter.

volume = $2(\pi)\ (.25)^2\ (7.77) = 3.05\ cm.^3$ (7.77 cm spacing as in half-wave dipole rectenna)

weight = 0.0185 lb. = 8.3 grams.

cost = (0.01815 lb.) ($.80/lb.) = $0.0145
or 1.45¢

resistance = $2.24 \times 10^{-4}\ \Omega$/element spacing

	Half-wave Dipole	3 element Yagi with ground plane	3 element Yagi without ground plane	6 element Yagi (average specifications)
Element Density (elem./m^2)	192	81	123	57
Element Spacing (cm.)	7.77	11.92	9.67	14.5
Cost/element of DC buss	1.45¢	2.23¢	1.81¢	2.71¢
Cost/m^2 of rectenna	$2.78	$ 1.81	$2.23	$1.55

were included. Table 2-14 summarizes data provided by Raytheon while Table 2-15 through 2-16 provided detailed information for the three elements Yagi designs. Six element designs costs were obtained in a similar fashion (although detailed calculations not presented).

As with the printed circuit element costs, the strong dependancy of cost per unit area upon element gain (or density) is apparent. Thus we conclude that

THERE IS A LARGE RECTENNA COST SAVING POSSIBLE BY FURTHER CONSIDERATION OF MORE DIRECTIONAL RECEIVING ELEMENTS.

In addition, it appears that costs are similar for printed circuit implementation and baseline type construction. Although these cost estimates are derived from a different basis, we conclude that the 2 to 4% sacrifice in conversion efficiency with printed circuit implementation does not appear to be overcome by a large cost advantage. That is, baseline type construction appears preferred over printed circuit implementation at this time. However a structural design is considered worthwhile to specify more rigorously DC buss bar and PCB socket requirements. For example, if the DC buss bar cost can be reduced by a factor of 2 (by reducing diameter below 5mm or developing an appropriate composite material), PCB implementation would be 25% below the baseline type construction cost. If this cost reduction was obtained, efficiency-cost tradeoffs would need to be considered in more detail.

Another key factor that could influence the tradeoff between printed circuit and baseline type construction is diode package cost. A large uncertainty in projecting rectenna cost is the diode estimate. Even glassed diode stand alone packages will have a non-negligible cost compared to the diode chip in the quantities needed. PCB implementation is expected to be less expensive since the chip could be directly banded in place. While more work is needed to evaluate cost factors in the quantities needed, this advantage of PCB implementation could be significant.

Table 2-14 Cost Estimate for Baseline Constructed Half-wave Dipole (192 elements/m^2)

Foreplane Core	Quantity/m^2	Cost \$/m^2
- aluminum in common buss bar and microwave circuit	418 g.	\$ .77
- aluminum in dipole antennas	142 g.	.26
- common assembly pins and capacitors mamade from AlO_2	768 units	.40
- enclosure caps for dipole made from AlO_2	384 units	.85
- seals for dipole caps	384 units	.85
	TOTAL	\$3.13
Additions		
- aluminum shield/structural member	1212 g.	\$2.14
- steel ground plane		1.91
	TOTAL	\$7.18
Diodes at \$.01 ea.	192 units	\$1.92
		\$9.10

Table 2-15 Cost Estimate for Baseline Constructed 3 Element Yagi with Ground Plane (81 element/m^2)

Foreplane Core	Quantity/m^2	Cost \$/m^2
- aluminum in common buss bar and microwave circuit	273 g. (factor = $\frac{9.7}{14.9}$ = .65)	\$ .50
- aluminum in dipole antenna	58 g. (factor = $\frac{81}{200}$ = .405)	.11
- common assembly pins and c capacitors made from AlO_2	324 units (factor = .405)	.16
- enclosure caps for dipoles made from AlO_2	162 units (factor = .405)	.35
- seals for dipole aps	162 units	.35
	TOTAL	\$1.47
Additions		
- aluminum shield/structural member	790 g. (factor = .65)	\$1.40
- aluminum directors	58 g.	.11
- Delrin support masts	81 units at 0.232¢/elem.	.19
- steel ground plane	2423 g.	1.91
	TOTAL	\$5.08
- Diodes at \$.01 ea.	81 units	.81
	TOTAL	\$5.89

Table 2-16 Cost Estimate for Baseline Constructed 3 Element Yagi without Ground Plane Cost (123 element/m^2)

Foreplane Core	Quantity/m^2	Cost \$/m^2
- aluminum in common buss bar and microwave circuit	336 g. (factor = $\frac{11.9}{14.9}$ = .80)	\$ .62
- aluminum in dipole antenna	87.3 g. (factor = $\frac{123}{200}$ = .615)	.16
- common assembly pins and capacitors made from AlO_2	492 units (factor = .615)	.25
- enclosure caps for dipole made from AlO_2	246 units (factor = .615)	.53
- seals for dipole caps	246 units	.53
	TOTAL	\$2.09
Additions		
- aluminum shield/structural member	529 g.	\$ .92
- aluminum passive elements	175 g. (factor = $2(\frac{123}{200})$ = 1.23)	.32
- Delrin support masts	123 units at \$0.320¢/element	.39
	TOTAL	\$3.72
- Diodes at \$.01 ea.	123 units	1.23
	TOTAL	\$4.95

3.0 POWER COMBINING EVALUATION

Most of the rectenna development effort to date has properly emphasized high RF to DC conversion efficiency.[1-3] As a result experimental arrangements have been somewhat idealized as far as SPS operation is concerned. For example flat rectenna arrays have been tested rather than serrated rectennas and DC combining networks have been arranged to insure, as much as possible, that devices to be combined operate at the same power level. In this part of our program, we emphasized an evaluation of the power combining inefficiencies expected when many RF to DC conversion circuits (~ 10,000 to 1,000,000) share a common load.

This consideration, inherent in SPS operation, had not been evaluated previously. While the power variations due to diffraction from a serrated antenna[7] and the power variations due to the power beam taper[5] have been quantified to some degree, the impact with DC load sharing on overall RF to DC conversion efficiency had not been evaluated. In addition the relationship between incident power variations, conversion circuitry operation and DC load sharing had been delineated as a source of SPS power output fluctuation, which in turn affects power grid interface requirements.[19] In this task we made a good first order evaluation of the resultant power combining inefficiency, while developing a methodology which can be applied directly in future work.

The principal concept of our evaluation is to utilize a power dependent output equivalent circuit of the conversion circuitry, obtainable by varying the load impedance at each RF power level, i.e. a load line analysis. To employ this technique a circuit model of the rectenna element conversion circuitry is needed. In Section 3.1 two rectifier circuit models (a computer simulation model and a closed form model) developed in this program are presented, followed by a discussion of the load line analysis in Section 3.2. These two sections contain a detailed treatment of the basics for the power combining analysis.

In Section 3.3 the power combining analysis methodology and results obtained with both computer simulation and closed form models are presented. These results focus on evaluation of series versus parallel combining inefficiency with numerous rectifiers sharing a common load. Numerous

distributions in power density are presented. In Section 3.4 the effect of these results on power module size constraints and SPS rectenna design are presented.

3.1 RECTIFIER CIRCUIT MODELS

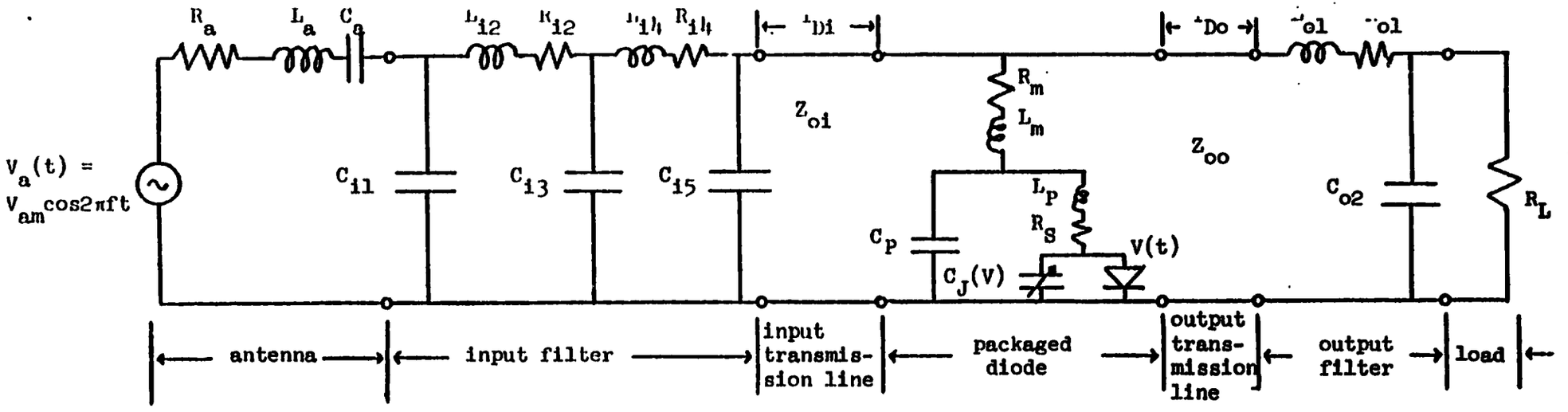
In this section two independent circuit models of the RF to DC conversion circuitry are presented, along with principal results obtained with these models. A valid model of the conversion circuitry is necessary in order to obtain a reasonably precise output equivalent circuit for the load line analysis. However accurate modeling a non-linear circuit can be a time consuming and resource absorbing undertaking.[3,8] Our approach focused on development of a detailed computer simulation model using a general non-linear circuit program (Spice 2) and a parallel development of a closed form circuit model.

The detailed computer simulation model contains 30 device and circuit parameters and closely represents an actual rectifying circuit element. It differs from previously developed computer simulation models of the rectenna element[3,8] in that a general circuit program is used rather than developing individualized code for the particular circuit. Thus resources needed in development of the model are reduced appreciably, at the expense of less efficient operation for the particular circuit. Attention was focused on obtaining baseline type efficiency performance with typical packaged diode characteristics. The results are presented in Section 3.1.1.

In addition closed form models of the conversion circuitry were investigated. Initially the purposes of this work was to aid in understanding rectifier operation and to develop preliminary output equivalent circuit models for the power combining analysis, thereby allowing a first order evaluation of our main task. However the closed form analysis results in an output equivalent circuit in excellent agreement with the computer simulation model results, indicating that valid results can be obtained with this simpler model. The model is presented in Section 3.1.2.

3.1.1 Computer Simulation Model

The baseline type rectifier computer simulation model is depicted in Fig. 3-1. Initially we selected diode parameters and associated mounting



Source Parameters

$f = 2.45 \times 10^9$ Hz (2.45 GHz)

V_{am} = 25V (1.04W input)

Input Filter Parameters

C_{i1} = 1.40 pF C_{i3} = 2.09 pF

L_{i2} = 5.70 nH L_{i4} = 5.70 nH

R_{i2} = 0.66 ohms R_{i4} = 0.66 ohms

C_{i5} = 1.40 pF

Output Filter Parameters

L_{o1} = 10.4 nH

R_{o1} = 1.20 ohms

C_{o2} = 10.75 pF

Diode Parameters (T = 300°K)

ϕ = 0.8 eV

n = 1.0

$C_J(0)$ = 0.7 pF

I_s = 10.0 nA

R_s = 0.50 ohm

Input Transmission Line

Z_{oi} = 75 ohms

T_{oi} = 51 pS

Output Transmission Line

Z_{oo} = 75 ohms

T_{oo} = 0 pS

Antenna Parameters

R_a = 75 ohms

L_a = 0 nH

C_a = 3 pF

Diode Package and Mount

L_p = 0.3 nH

C_p = 0.2 pF

L_m = 0.5 nH

R_m = 0.25 ohm

Load

R_L = 75 ohms

Fig. 3-1 Computer Simulation Model for Baseline Type RF to DC Conversion Circuitry

parasitic parameters. These were selected to be comparable to that of the baseline rectifier with the present mounting configuration[1] and were held constant throughout our investigation. Also selected was a 75 ohm antenna resistance, comparable to an isolated $\lambda/2$ dipole receiving element. For simplicity it was decided to keep a 75 ohm impedance level throughout the circuit. Although higher efficiency may be possible by impedance transforming to a higher value, detailed efficiency optimization was not within the scope of our effort.

With a 75 ohm impedance level selected, a five stage lumped filter was used at the input and two stage smoothing filter at the output. The input filter is described in detail in Sec. 2.2.1 and the output is designed similarly. Obviously the output filter has a lower frequency cutoff, with a value depending upon a tradeoff between inductance required and filter rejection at 2.45 GHz. The output filter has a 3 dB ripple, cutoff frequency of 612 MHz and provides 30 dB of fundamental frequency rejection when operated between 75 ohm impedances.

Initially results obtained with the model indicated low efficiency until input and output transmission lines were added between the mounted diode and filters. The transmission line control the phase of reflected signals and is particularly important at the input. In many simulations, a five section L-C network was used to replace the transmission line, to reduce program running time without sacrificing overall circuit performance.

With this model, the incident power is varied by changing the value of the amplitude of the voltage source. As a result, the nonlinear circuit performance changes, principally due to the diode turn-on voltage of approximately 0.8 volts. A plot of conversion efficiency versus incident power is shown in Fig. 3-2, in which no circuit or diode parameters have been varied. This decrease in efficiency with decreasing power is greater than experimentally obtained when circuit is reoptimized at each power level,[1] as described previously.[5] Because of resource constraints, optimization at each power level was not performed. However we believe that the power combining inefficiency is relatively insensitive to this further optimization.

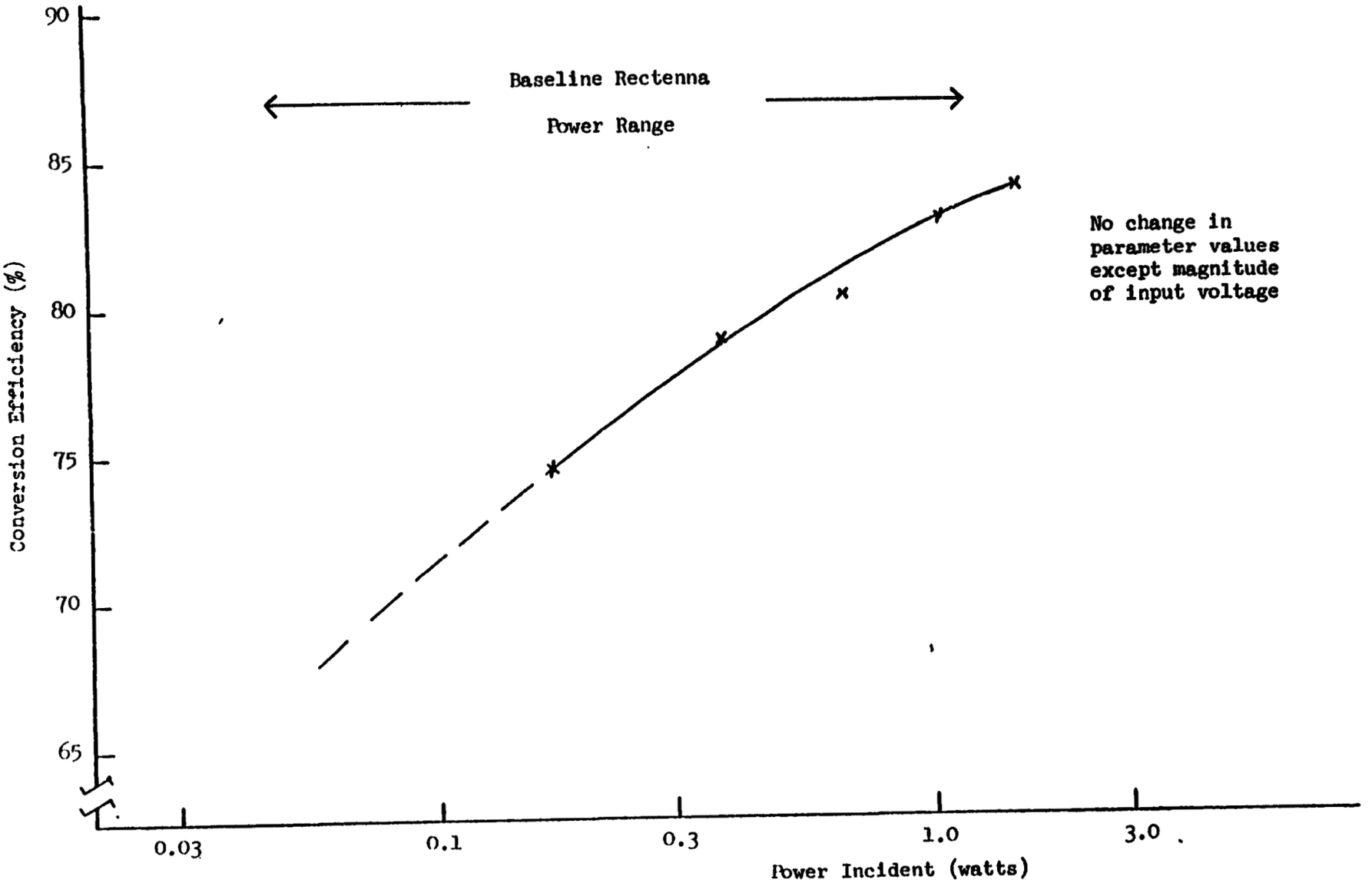


Fig. 3-2 Conversion Efficiency of Computer Simulation Model

Besides the conversion efficiency one can obtain useful voltage and current waveforms as well as Fourier analysis of these waveforms. For example Figures 3-3 and 3-4 indicates packaged diode and diode chip waveforms of voltage and current respectively at a 1W power level. The chip reverse voltage exceeds slightly the peak voltage amplitude of the source (29V compared to peak amplitude of the open circuited RF source voltage of 25V); while the chip current (conduction plus displacement) exceeds 400 mA during the middle of the 180° conduction angle (compared to peak amplitude of the shorted circuited RF source current of 333 mA). The waveforms are obviously rich in harmonic content, partly attributed to resonances from packaged diode parasitics.

Fourier analysis of three voltage waveforms, namely the output voltage, the diode package voltage and the diode chip voltage are presented in Table 3-1, along with the input current. The effectiveness of the smoothing filter is apparent as the DC voltage is similar while the fundamental component of the output voltage compared to that of the mounted package voltage is reduced by a factor of 26(12.79V to .497V) or 28 dB, with harmonics reduced still further (e.g. second harmonic 40 dB). Also the three values of DC voltage are slightly different, due to numerical approximations in the program and finite program running time. The approximation, as well as the effect of the input filter, can be seen from the input current, which contains harmonics 50 dB below the fundamental. This is about the precision of the program as used by us, as can be seen by the erroneous finite value of DC input current (should be zero).

It should be mentioned that additional investigations possible with this program such as efficiency optimization at nominal power and lower powers, effect of package and mount parasitics, sensitivity of performance to diode and circuit parameters and harmonic performance evaluations were beyond the scope of our program. Emphasis was placed upon printed circuit board implementation evaluation (Sec. 2.2.1) and developing a model that provided efficiency characteristics similar to that demonstrated experimentally (for the power combining analysis).

As a result of these and similar considerations, we concluded that the computer simulation model developed results in performance characteristics similar to the Raytheon baseline. This model was used to determine the

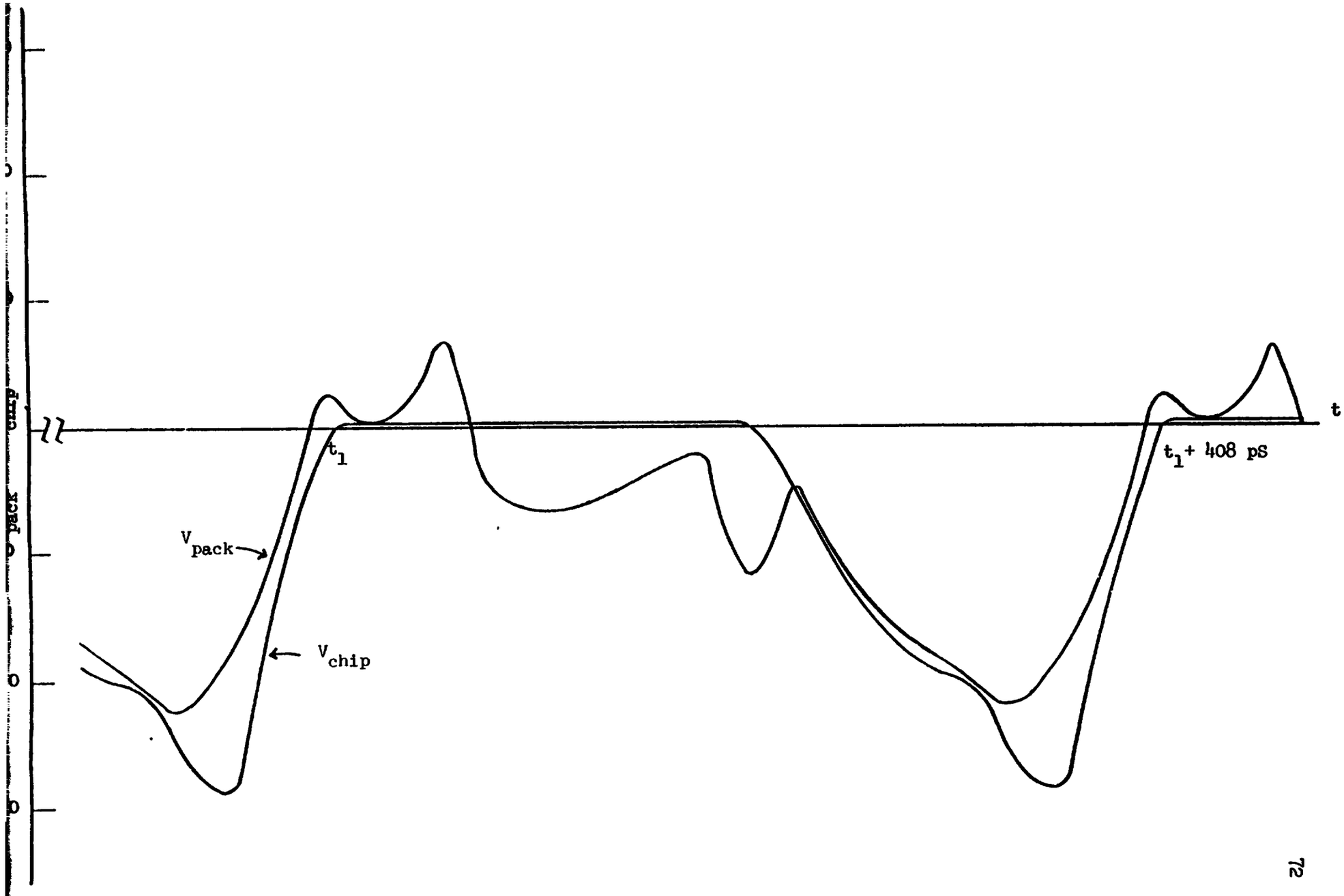


Fig. 3-3 Package and Chip Voltage Waveforms of Computer Simulation Model at 1W Level

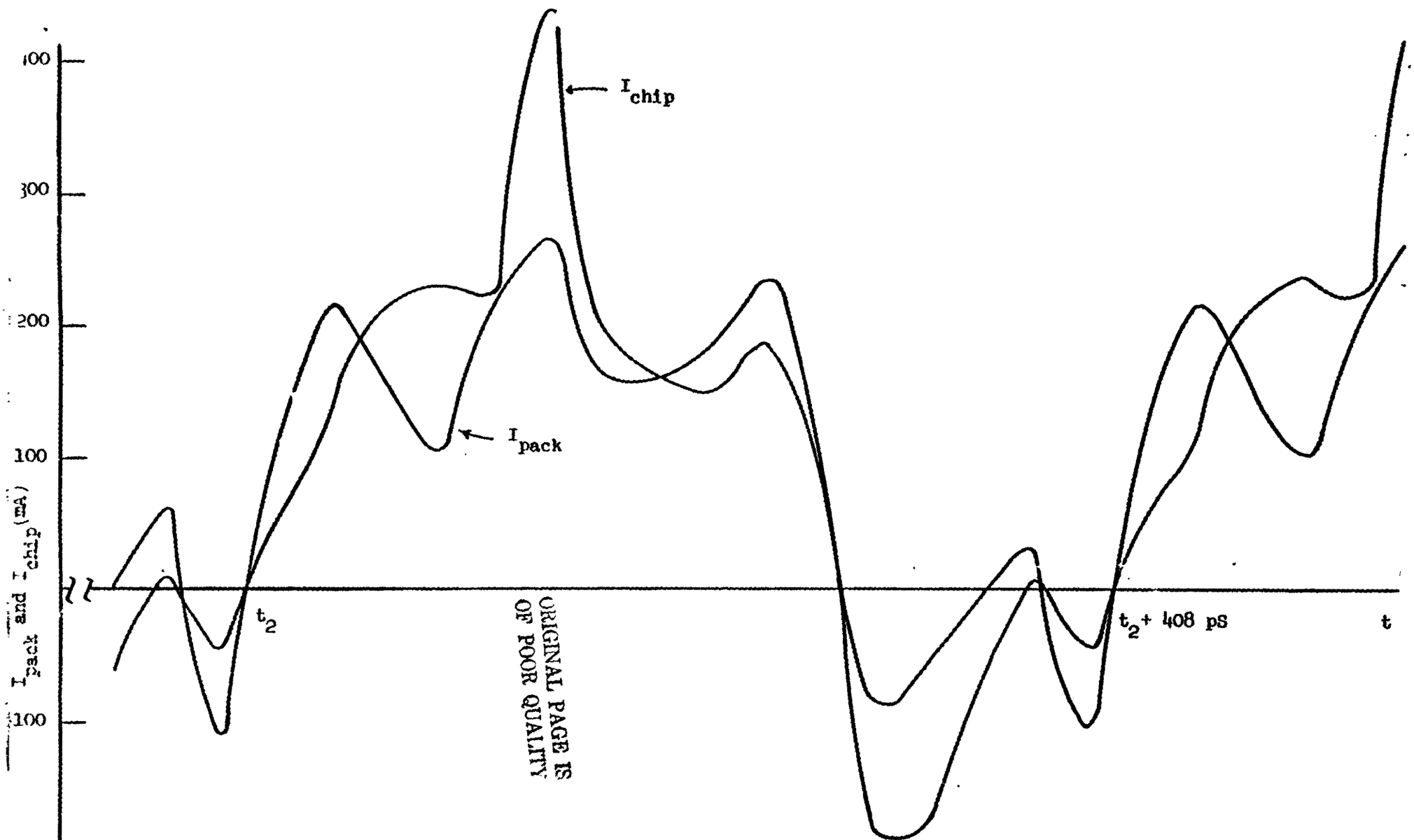


Fig. 3-4 Package and Chip Current Waveforms (including Chip Displacement Current) of Computer Simulation Model at 1W Level

Table 3-1

Computer Simulation Output for Baseline Type Rectifier (Power In = 1.04 W)

Fourier Components of Transient Response of Output Voltage - DC Component = -8.052D 00 (volts)

Harmonic No.	Frequency (HZ)	Fourier Component	Normalized Component	Phase (Deg)	Normalized Phase (Deg)
1	2.450D 09	4.971D-01	1.000000	-114.908	0.000
2	4.900D 09	5.658D-02	0.113826	9.055	123.963
3	7.350D 09	1.147D-02	0.023079	61.376	176.284
4	9.800D 09	3.714D-03	0.007472	-15.882	99.026
5	1.225D 10	2.125D-03	0.004274	-47.665	67.243
6	1.470D 10	2.115D-03	0.004255	23.977	138.886
7	1.715D 10	2.603D-03	0.005237	2.376	117.285
8	1.960D 10	6.438D-04	0.001295	14.474	129.382
9	2.205D 10	7.756D-04	0.001560	23.437	138.346

Fourier Components of Transient Response of Mounted Package Voltage - DC Component = -8.194D 00 (volts)

Harmonic No.	Frequency (HZ)	Fourier Component	Normalized Component	Phase (Deg)	Normalized Phase (Deg)
1	2.450D 09	1.279D 01	1.000000	59.228	0.000
2	4.900D 09	5.672D 00	0.443533	-173.104	-232.332
3	7.350D 09	2.533D 00	0.198123	-112.479	-171.707
4	9.800D 09	1.075D 00	0.084099	152.082	92.854
5	1.225D 10	1.162D 00	0.090878	101.244	42.015
6	1.470D 10	1.233D 00	0.096399	-147.130	-206.359
7	1.715D 10	2.458D 00	0.192248	177.288	118.059
8	1.960D 10	4.572D-02	0.003575	-11.400	-70.628
9	2.205D 10	4.473D-01	0.034980	-131.388	-190.616

Fourier Components of Transient Response of Chip Voltage - DC Component = -8.269D 00 (volts)

Harmonic No.	Frequency (HZ)	Fourier Component	Normalized Component	Phase (Deg)	Normalized Phase (Deg)
1	2.450D 09	1.396D 01	1.000000	51.526	0.000
2	4.900D 09	6.437D 00	0.460942	-173.499	-225.025
3	7.350D 09	1.623D 00	0.116224	-112.665	-164.191
4	9.800D 09	2.693D 00	0.192868	-27.354	-78.881
5	1.225D 10	1.749D 00	0.125243	100.730	49.204
6	1.470D 10	7.460D-01	0.053421	-145.123	-196.649
7	1.715D 10	4.952D-01	0.035461	-5.913	-57.440
8	1.960D 10	3.836D-01	0.027469	159.988	108.462
9	2.205D 10	1.350D-01	0.009670	-119.313	-170.839

Fourier Components of Transient Response Source Current - DC Component = -1.318D-04 (Amps)

Harmonic No.	Frequency (HZ)	Fourier Component	Normalized Component	Phase (Deg)	Normalized Phase (Deg)
1	2.450D 09	1.588D-01	1.000000	179.679	0.000
2	4.900D 09	4.186D-04	0.002635	33.824	-145.856
3	7.350D 09	1.699D-05	0.000107	74.036	-105.643
4	9.800D 09	1.084D-05	0.000068	-12.489	-192.168
5	1.225D 10	4.711D-06	0.000030	107.372	-72.307
6	1.470D 10	9.712D-07	0.000006	5.270	-174.410
7	1.715D 10	4.553D-06	0.000029	-68.767	-248.446
8	1.960D 10	7.651D-07	0.000005	174.106	-5.573
9	2.205D 10	4.034D-06	0.000025	77.587	-102.093

equivalent circuit as a function of power level in Section 3.2.2 and the power combining analysis of Sections 3.3.2.1 and 3.4.

3.1.2 Closed Form Models

In this section we describe the closed form analysis which was carried out in order to gain insight into the operation of high efficiency rectifier circuits. The final goal of the analysis was to arrive to a rectifier circuit which could give 100% rectification efficiency, assuming no losses in the diode rectifier and in the circuit elements. This circuit model, as the computer simulation model, was used for calculating power combining inefficiencies when rectenna elements, operating at different RF power levels, are connected in either series or parallel.

Our starting point was the simple rectifier circuit shown in Fig. 3-5. In that circuit V_s is the peak amplitude of the open circuit RF voltage at the antenna terminals, R_s is the antenna radiation resistance and R_L is the load connected at the rectenna element terminals. The voltage V_L at the load terminals is a half-wave rectified sine wave, shown in Fig. 3.5, with peak amplitude of:

$$(V_L)_p = V_s \frac{R_L}{R_s + R_L} \tag{3.1}$$

and rms value of:

$$(V_L)_{rms} = \frac{V_s}{2} \frac{R_L}{R_s + R_L} \tag{3.2}$$

Since the maximum RF power available at the antenna terminals is:

$$(P_{RF})_{max} = \frac{V_s^2}{8 R_s} \tag{3.3}$$

it follows that the efficiency η, ratio of power at the load to maximum RF power available, is given by:

$$\eta = \frac{2 R_s R_L}{(R_s + R_L)^2} \tag{3.4}$$

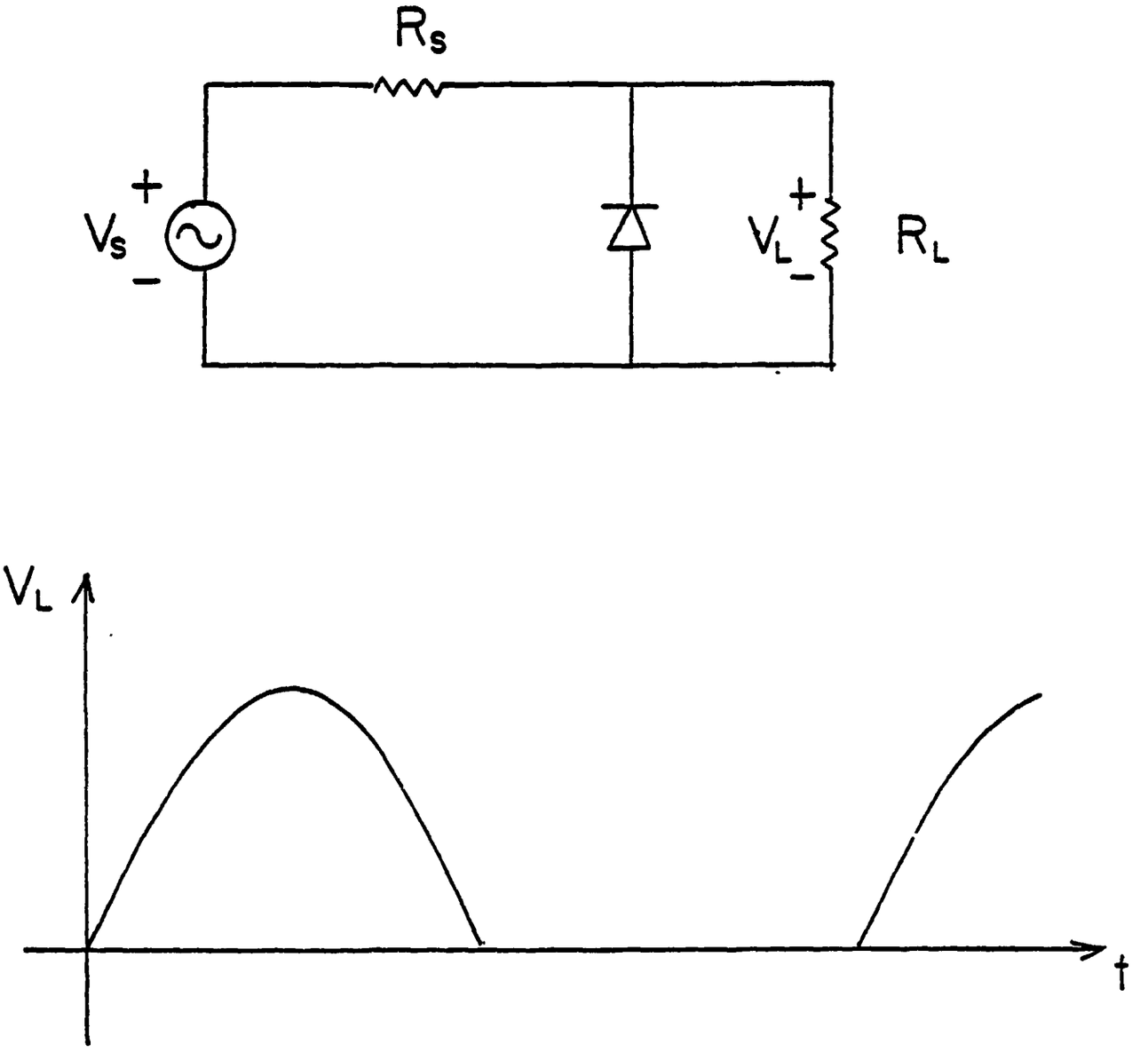


Figure 3-5 Simple Rectifier Circuit and Load Voltage Waveform.

The maximum efficiency is 50%, achieved when $R_s = R_L$. The above circuit has two drawbacks. First of all its efficiency is at the most 50% and, because of the lack of filtering, there is a large amount of the ripple in the load voltage.

The ripple in the load voltage can be reduced by incorporating a low pass filter in the output as shown in Figure 3-6, the inductance L being placed in series with the load. If the value of this inductance is sufficiently large the current flowing through the load is only DC current of magnitude I_L. Under these conditions, the rectifier is closed ($V_R = 0$) as long as $I_1 < I_L$. The waveforms of the current I_1 and rectifier voltage V_R are shown in Fig. 3-6. The angle 2θ during which the rectifier is open is determined by the equation:

$$\cos \theta = \frac{I_L}{I_s} \tag{3.5}$$

where I_s is peak amplitude of the maximum RF current which can be supplied at the antenna terminals, i.e. under short circuit conditions and is given by:

$$I_s = \frac{V_s}{R_s} \tag{3.6}$$

It follows from the above circuit that the DC value of the load voltage V_L is the average value of the rectifier voltage V_R. It can be shown that the value of V_L is:

$$\frac{V_L}{V_s} = \frac{\sin \theta - \theta \frac{I_L}{I_s}}{\pi} \tag{3.7}$$

and the rectification efficiency is given by:

$$\eta = \frac{8}{\pi} \left(\frac{\sin 2\theta}{2} - \theta \cos^2 \theta \right) \tag{3.8}$$

The efficiency is zero for $\theta = 0$ ($V_L = 0$ or short-circuited conditions) and for $\theta = \pi/2$ ($I_L = 0$ or open-circuited conditions). The conditions for maximum efficiency are achieved for $\theta \approx 67^\circ$ and for this case

$$\eta_{max} \approx 46\% \qquad \frac{R_L}{R_S} \approx 0.4 \tag{3.9}$$

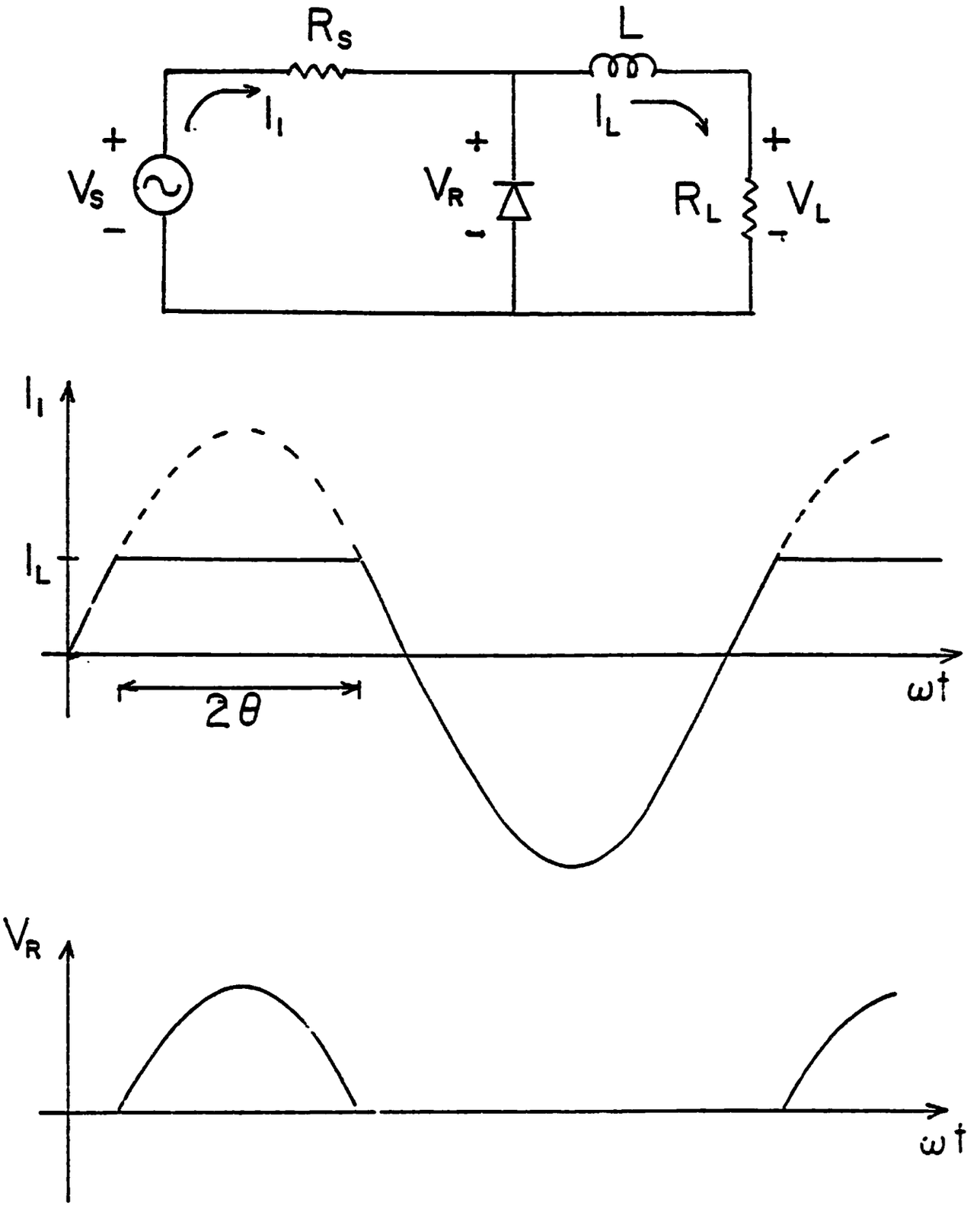


Figure 3-6 Rectifier Circuit with a Low Pass Filter in the Output and Associated Current and Voltage Waveform.

Although the above rectifier circuit provides low ripple in the load output voltage because of the filtering introduced, the efficiency is very low. The main reason is that any harmonics generated are allowed to flow through the antenna resistance R_s where their power is dissipated. It is necessary to have not only an output filter to reduce ripple in the output voltage, but also an input filter to prevent harmonic dissipation. A schematic representation of a rectenna element which contains input and output filters is depicted in Fig. 3-7. The filter at the input should prevent any of the dc current and harmonics to flow back through the antenna resistance R_s, but allow current flow at the fundamental RF frequency ω. The function of the filter at the output is not only to prevent AC components to appear across the load terminals but also to allow harmonic currents to flow. In particular, the even harmonics should be allowed to flow since they have the property of having a zero average on each half cycle. Therefore the output filter should allow the even harmonics to flow without any voltage drop, should prevent current flow at any of the odd harmonics and should allow dc current flow. The above characteristics of the input and output filters are shown in Fig. 3-7.

We will describe two possible implementations of realizing filters with the above characteristics. Input and output filters implemented using lumped circuit elements and satisfy the requirements given in Fig. 3.7 are shown in Fig. 3-8. The elements L_3, C_3, L_5, C_5, . . . , form parallel resonant circuits which are open circuited at the odd harmonics 3ω, 5ω, . . . respectively. The capacitor C_1 is used for preventing DC current flow as well as for series resonating L_3, C_3, L_5, C_5, . . . at the fundamental frequency ω. If that is the case, the current I_1 would be an AC current of fundamental frequency ω. The L_2, C_2, L_4, C_4, . . . elements in the output circuit are series resonant at the even harmonics 2ω, 4ω, . . . respectively. The inductance L_c is assumed to be large enough such that the current I_L is mainly dc current. In that way the current I_2 would consist of a dc current plus even harmonics only.

Another possible realization of the output filter is shown in Fig. 3-9. In this c. .t the output filter consists of a non-dispersive transmission line which is a quarter-wavelength long at the fundamental frequency,

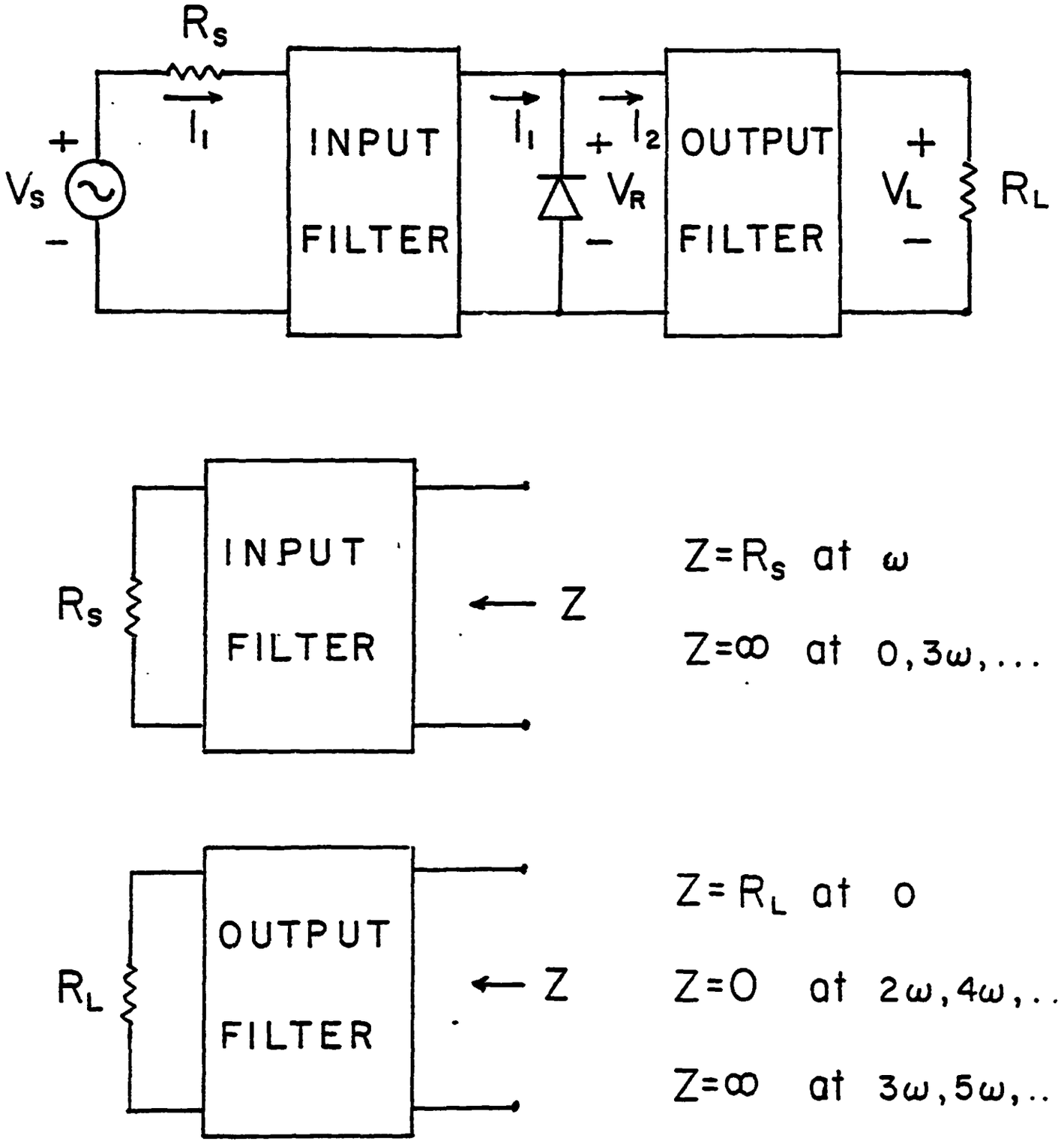


Figure 3-7 Rectifier Circuit with Input and Output Filters and their Frequency Characteristics.

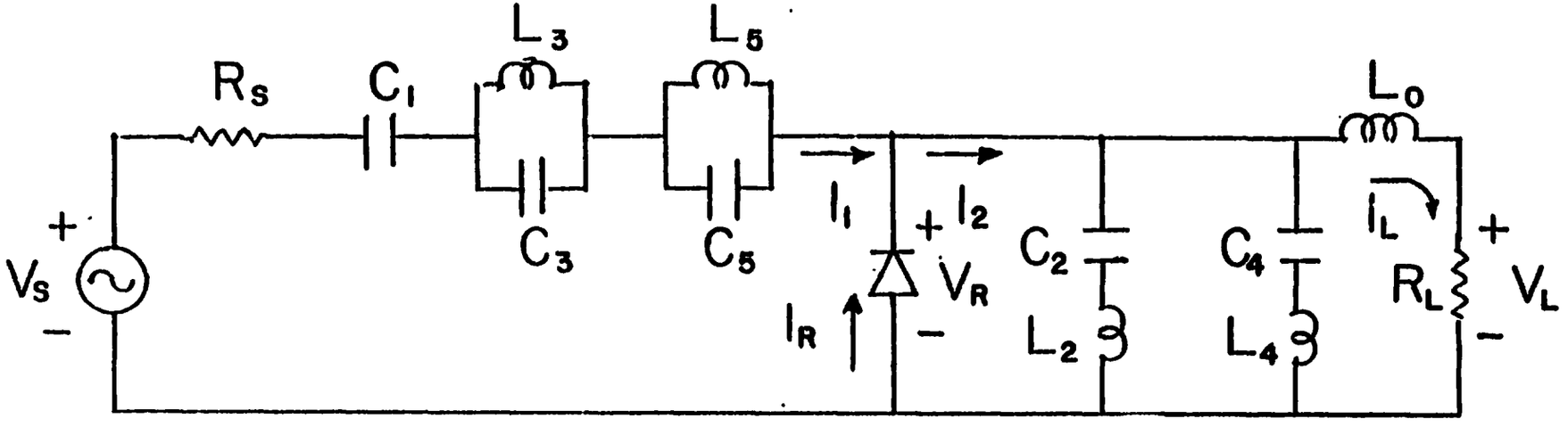


Figure 3-8 Realization of a High Efficiency Rectifier Circuit with Lumped Element Input and Output Filters.

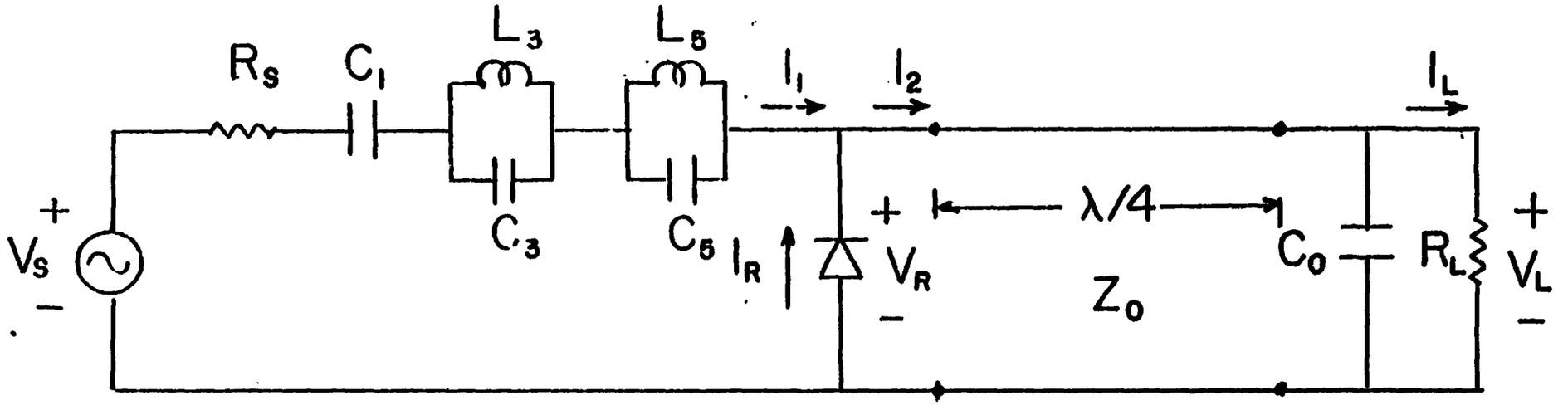


Figure 3-9 Realization of a High Efficiency Rectifier Circuit with a Transmission Line as Output Filter.

terminated in a capacitor C_o in parallel with the load R_L. If C_o is sufficiently large, the line can be considered to be shorted at the load end and will appear at the diode terminals as an open circuit at $\omega, 3\omega, 5\omega, \ldots$ and as a short circuit at $2\omega, 4\omega, \ldots$. The circuit analysis of the rectifiers circuits of Figs. 3-8 and 3-9 is identical and is presented below.

Since the current I_1 is only of the fundamental frequency, we can write:

$$I_1(t) = I_0 \sin \omega t \tag{3.10}$$

Assuming that the rectifier is open $(I_R = 0)$ in the half period $0 < \omega t < \pi$, then:

$$I_2(t) = I_0 \sin \omega t \qquad 0 < \omega t < \pi \tag{3.11}$$

Since $I_2(t)$ consists only of even harmonics it follows that:

$$I_2(\omega t + \pi) = I_2(\omega t) \tag{3.12}$$

That is, $I_2(t)$ is a full rectified sinusoud of peak amplitude I_0:

$$I_2(t) = I_o \left| \sin \omega t \right| \qquad 0 < \omega t < 2\pi \tag{3.13}$$

The rectifier current I_R is the difference between I_2 and I_1 and it is given by:

$$I_R(t) = I_o \left| \sin \omega t \right| - I_o \sin \omega t \tag{3.14}$$

which is a half-rectified sine wave of peak amplitude $2I_o$. The magnitude of the load current I_L is the average value of $I_2(t)$:

$$I_L = (I_2)_{av} = \frac{2}{\pi} I_0 \tag{3.15}$$

The rectifier voltage $V_R(t)$ is zero during the period of time when the rectifier is conducting current:

$$V_R(t) = 0 \qquad \pi < \omega t < 2\pi \tag{3.16}$$

Since the voltage across the rectifier consists only of a DC component plus odd harmonics it follows that:

$$V_R(t) = 2\,[V_R(t)]_{av} \qquad 0 < \omega t < \pi \tag{3.17}$$

where $[V_R(t)]_{av}$ is the average voltage across the rectifier and must be equal to the DC load voltage V_L:

$$V_R(t) = 2\,V_L \qquad 0 < \omega t < \pi \tag{3.18}$$

The waveforms of $I_1(t)$, $I_2(t)$ and $V_R(t)$ are shown in Fig. 3.10. Since the input filter allows the fundamental frequency to pass between the antenna terminals and the rectifier terminals, it follows that the fundamental component of $V_R(t)$ must appear across the antenna terminals. This fundamental component is determined from the Fourier series expansion of $V_R(t)$:

$$V_R(t) = 2\,V_L\left[\frac{1}{2} + \frac{2}{\pi}\sin\omega t \ldots\right] \tag{3.19}$$

It follows then that:

$$V_s = I_o R_s + \frac{4\,V_L}{\pi} \tag{3.19}$$

Substitution of Eq. (3.15) into (3.19) gives:

$$V_L = \frac{\pi}{4}\,V_S - \frac{\pi^2}{8}\,R_s I_L \tag{3.20}$$

The above equation indicates that as the dc load terminals is concerned, the rectenna elements behaves as a DC voltage source of amplitude $\pi/4\ V_s$ and internal resistance $\frac{\pi^2}{8}\,R_s$. The optimum load for maximum DC power is:

$$(R_L)_{op} = \frac{\pi^2}{8}\,R_s \tag{3.21}$$

and the maximum DC power output is

$$(P_L)_{max} = \frac{\left[\frac{\pi}{8}\,V_s\right]^2}{\frac{\pi^2}{8}R_s} = \frac{V_s^2}{8\,R_s} \tag{3.22}$$

which gives a 100% rectification efficiency. This ideal efficiency has been achieved because it was assumed no losses in any of the circuit

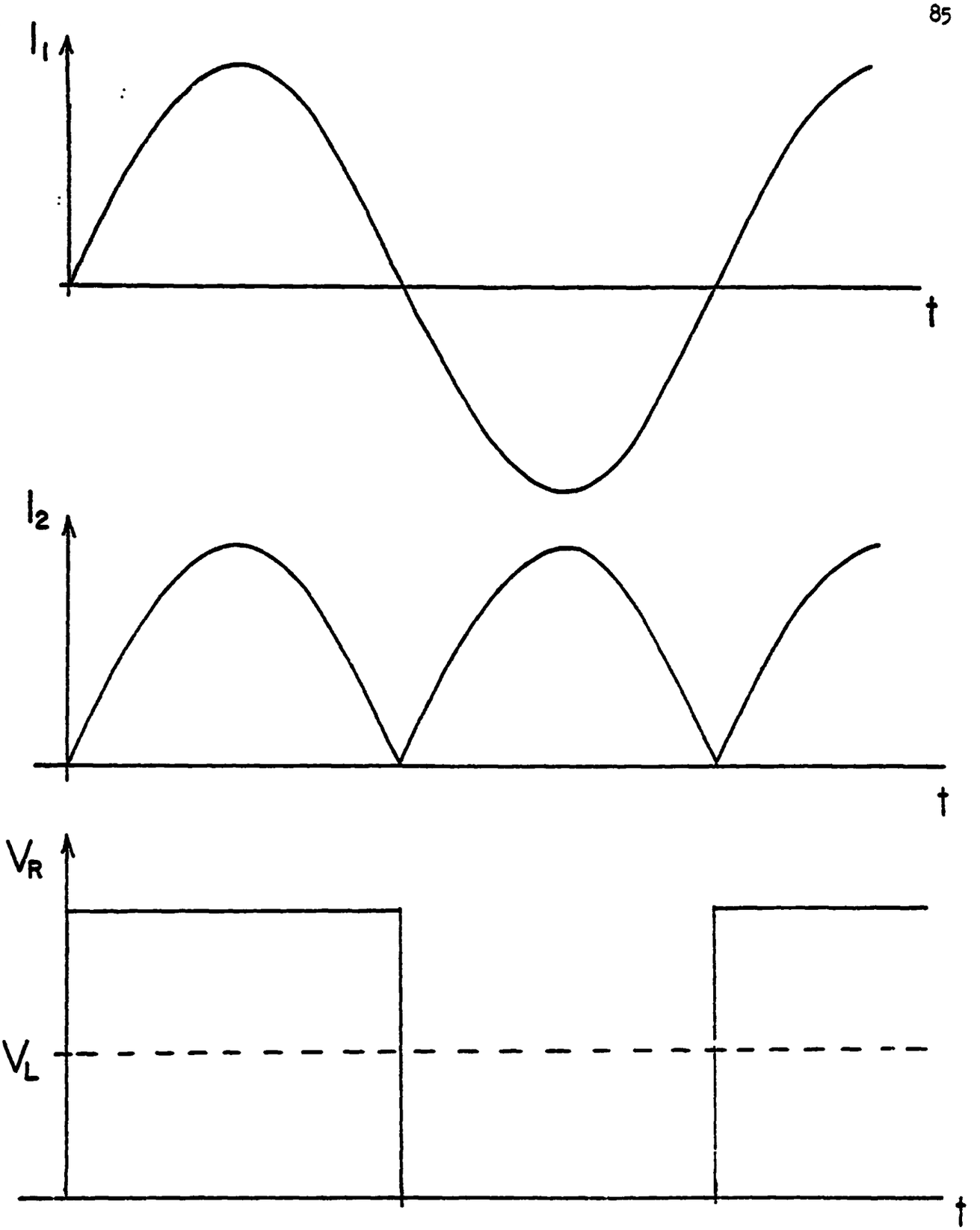


Figure 3-10 Current and Voltage Waveforms in a High Efficiency Rectifier Circuit.

components. However, since these losses can be minimized by choosing a rectifier diode with small series resistance and appropriate circuit elements, it is expected that their closed form conversion circuit model would be a good approximation to the characteristics of a high efficiency rectenna element. The principal difference would be diode depletion layer capacitance and package parasitics, accurately considered in the computer simulation model of Fig. 3-1 but ignored in the closed form, analytical model of Figures 3-8 and 3-9. However by adjusting filter parameters such parasitics can be included in the circuit design to first order. As is shown in Sec. 3.3.2, comparison with the computer simulation model of a high efficiency rectifier circuit shows the usefullness of the closed form models presented in this section.

3.2 LOAD LINE ANALYSIS

While the models presented in Section 3.1 are useful for gaining insight into the RF to DC conversion process, optimizing the circuit performance, and evaluating performance sensitivity to diode and circuit parameters, the principal use in this program was to obtain an output equivalent circuit of the rectenna element from the DC terminals. More precisely an output equivalent circuit which depends upon input power to the rectenna element (or V_s in the models of Section 3.1) is needed for Task 2 of our program.

In general an output equivalent circuit can be obtained analytically if a closed form circuit model is available or it can be obtained by evaluating the $V_L - I_L$ characteristics for various output load resistances (either by computer simulation or by measurement). These two techniques were used with our circuit models, and the results are presented in this section of the report.

The load line characteristic for the ideal, 100% efficient closed form model of Figures 3-8 and 3-9 is shown in Figure 3-11, along with the output equivalent circuit. It is obtained directly from Equation 3.20, except that in the graphical representation we have taken into account that $V_L > 0$ and $I_L > 0$, as is apparent from the actual circuits. Note that as the output load resistance is varied, all $V_L - I_L$ combinations fall

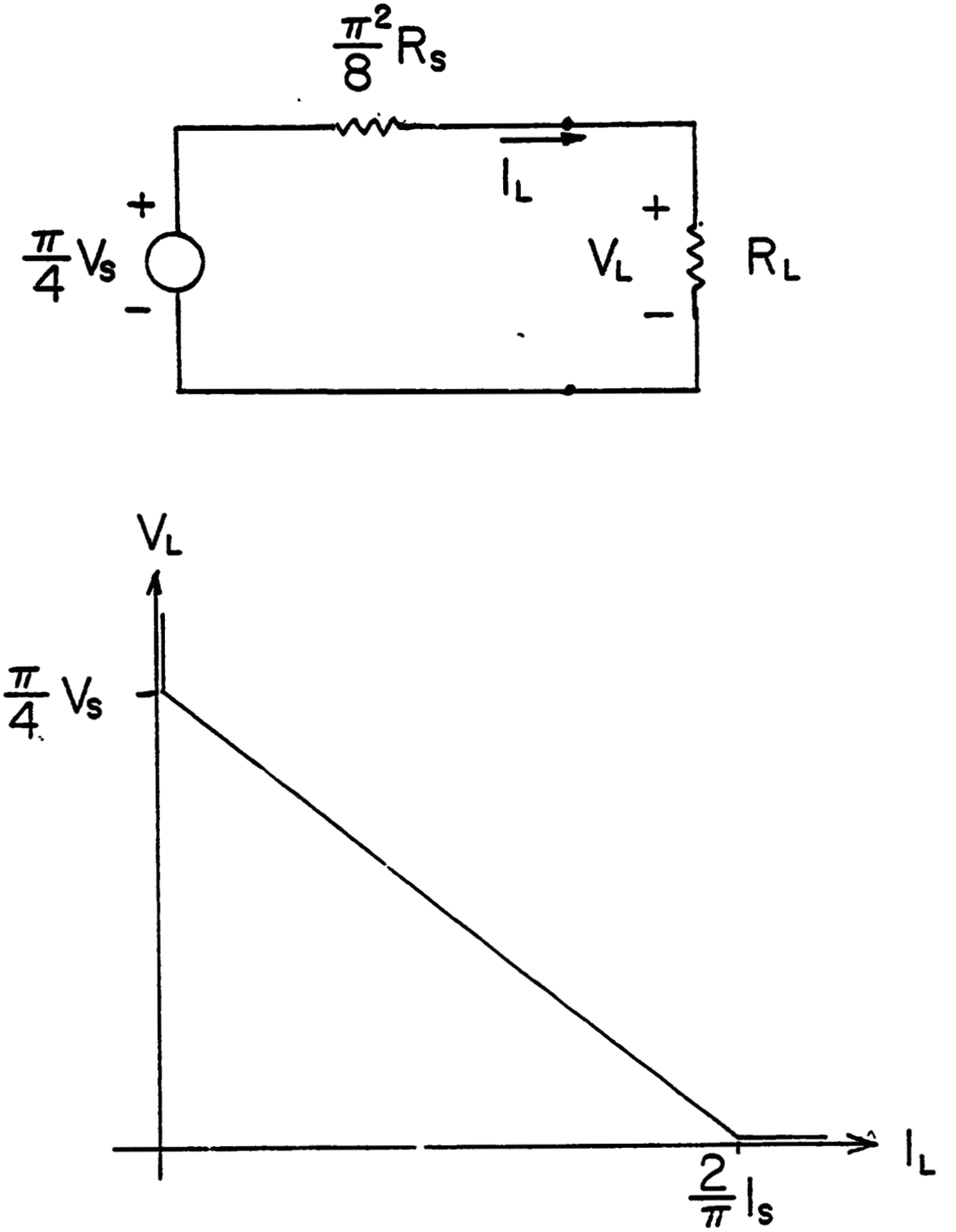


Figure 3-11 DC Equivalent Circuit and Load Line Characteristics for a High Efficiency Closed Form Rectifier Circuit.

on the straight line shown. For convenience, we find it useful to plot a normalized load line, i.e. $V_L/V_S - I_L/I_S$, where V_S is the open circuited source RF voltage and I_S is the short circuited source RF current.

The load line for the computer simulation model of Fig. 3-1 obtained by only varying the output load resistance from 5 to 1500 ohms (instead of fixed at 75 ohms), with the results shown in Figure 3-12. As required the computer model load line lies to the left of the closed form model since the latter does not contain any dissipative loss elements. Note that the computer model also results in a highly linear load line with similar characteristics to the closed form model.

With the computer simulation model a normalized load line is not identical at all power levels because of the fixed diode forward drop. The difference is shown in Fig. 3-13 for a 13 dB power range (0.10 to 2.08 watts). As expected the efficiency increases with increasing power level, and the DC output resistance varies only slightly with power level.

The dependence of output open circuited voltage V and output equivalent source resistance R on input power level is depicted in Fig. 3-14, in which the expanded scale should be noted. For comparison purposes the closed form model described earlier has V/V_S equal to .785 and R/R_S = 1.234, which is closer to the computer simulation model results at higher and lower incident power respectively. Note particularly the normalized output parameters V/V_S and R/R_S are relatively insensitive to input power.

While this program focused almost entirely on an evaluation of power combining inefficiency utilizing these load lines as described in Sections 3.3 and 3.4, the effect of circuit and diode parameter tolerances could also be included. As an aside we evaluated the effect of a ± 0.1 pF variation in the 0.7 pF nominal zero bias diode junction capacitance. A comparison of output equivalent circuit parameters and efficiency is shown in Table 3-2, and the efficiency dependence upon power level is shown in Fig. 3-15. Parameters were evaluated over a restricted 4 to 1 power range to conserve computer time. The lack of original circuit optimization is indicated by obtaining higher efficiency with 0.6 pF, the efficiency sensitivity being about -0.7%/0.1 pF over the range of interest. The output equivalent

Figure 3-12 Load Line of Computer Simulation Model at 1.04 W Compared to Closed Form Model.

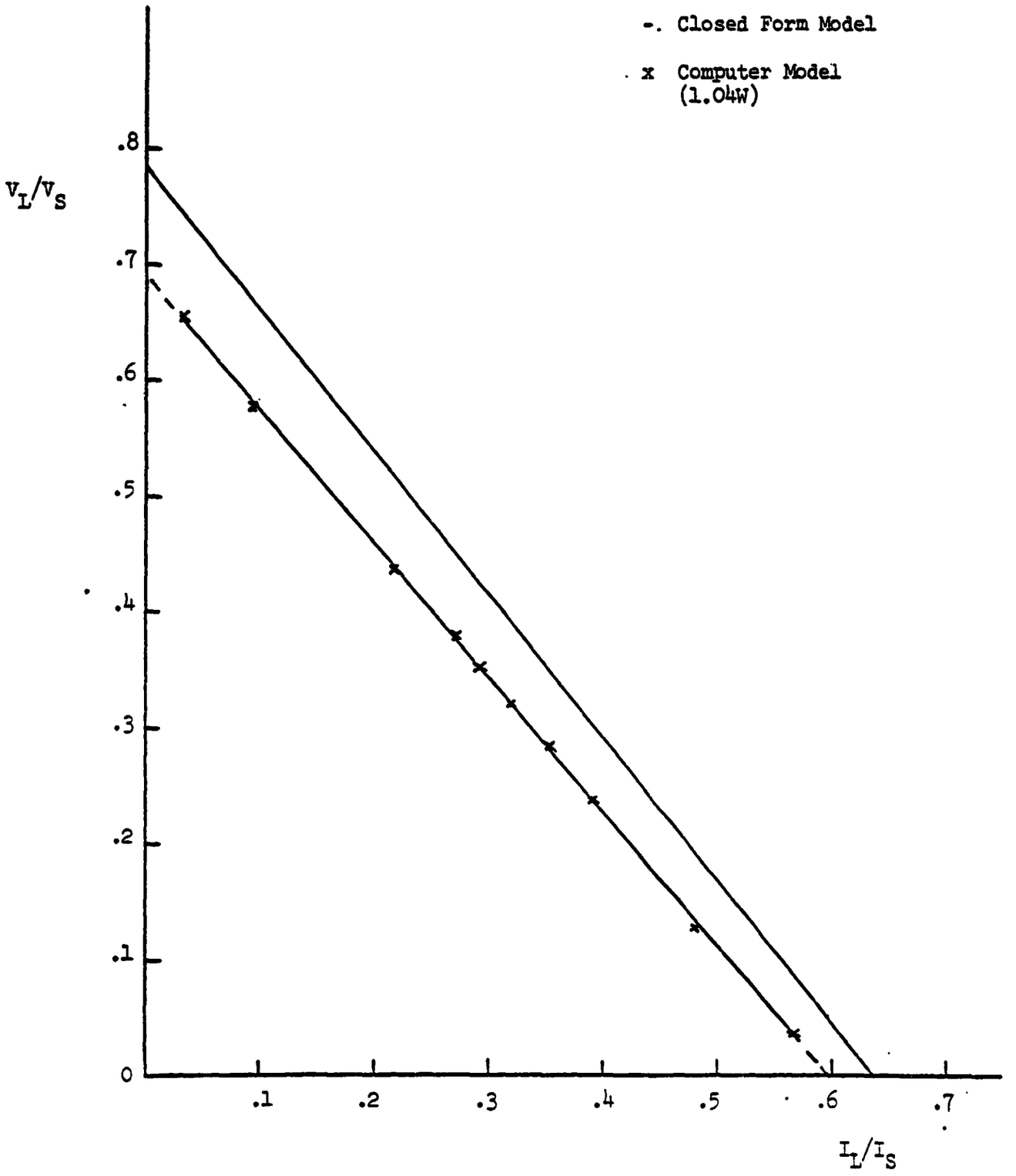


Figure 3-13 Load Line of Computer Simulation Model as a Function of Incident Power.

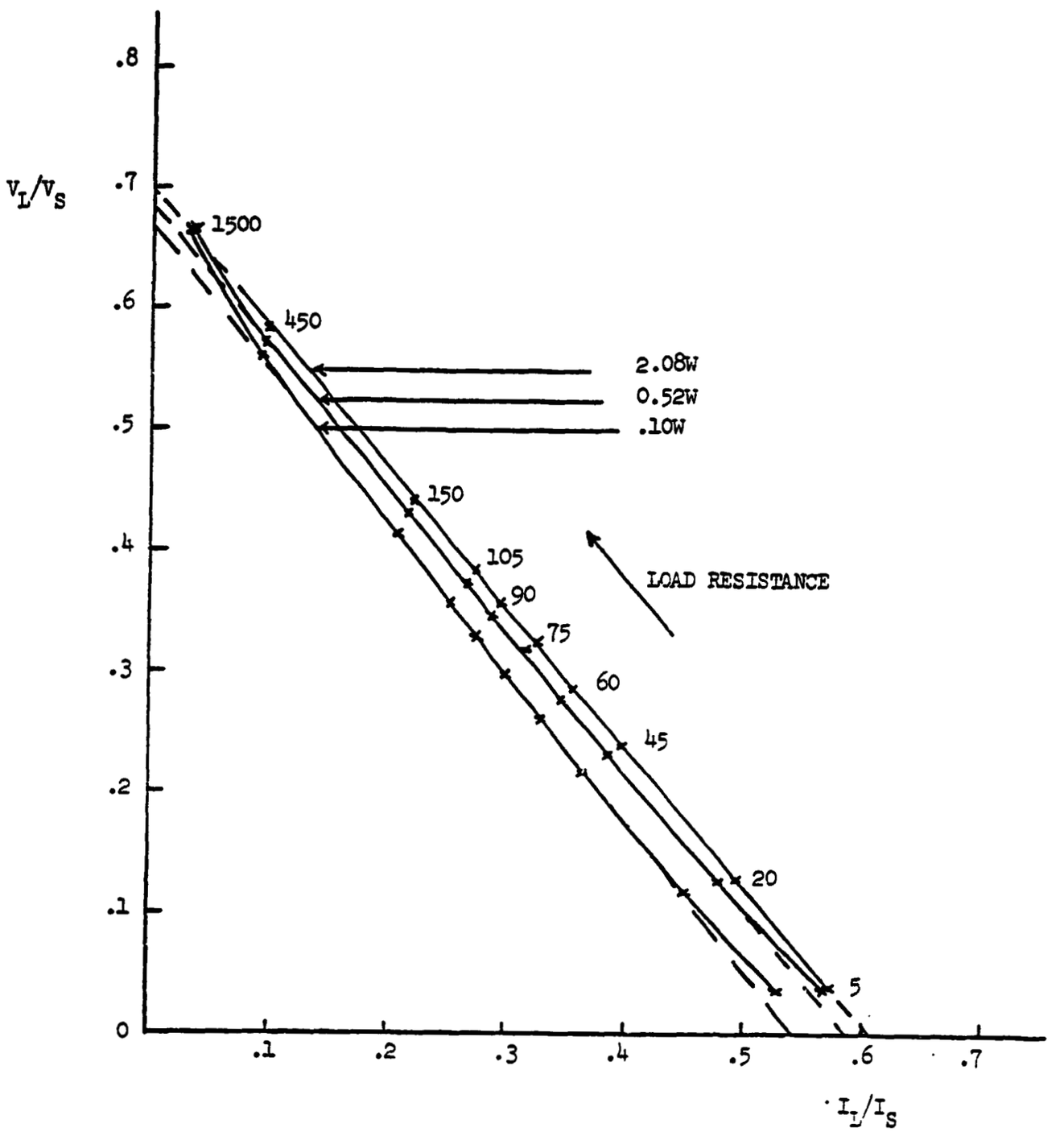
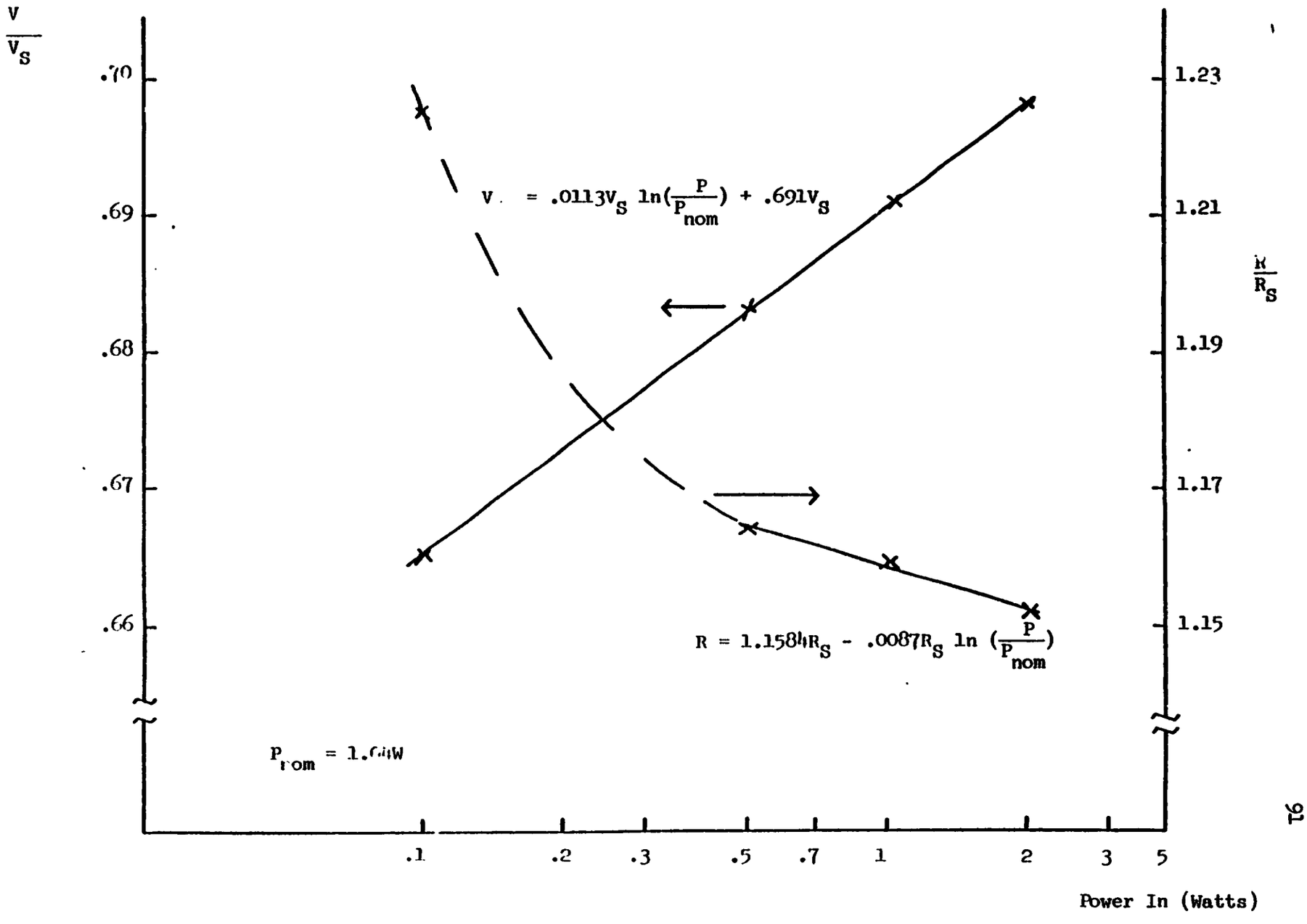


Figure 3-14 Output Equivalent Circuit Parameters of Computer Simulation Model as a Function of Incident Power.



C-2

Input Power (watts)

Diode Zero-Bias Junction Capacitance $C_j(0)$ (pF)	0.52		1.04		2.08	
	V/V_s	R/R_s	V/V_s	R/R_s	V/V_s	R/R_s
0.6	.685	1.158	.690	1.150	.702	1.149
0.7	.683	1.164	.691	1.159	.698	1.152
0.8	.688	1.184	.697	1.180	.705	1.175

Note: With closed form model $\frac{V}{V_s} = .785$ and $\frac{R}{R_s} = 1.234$

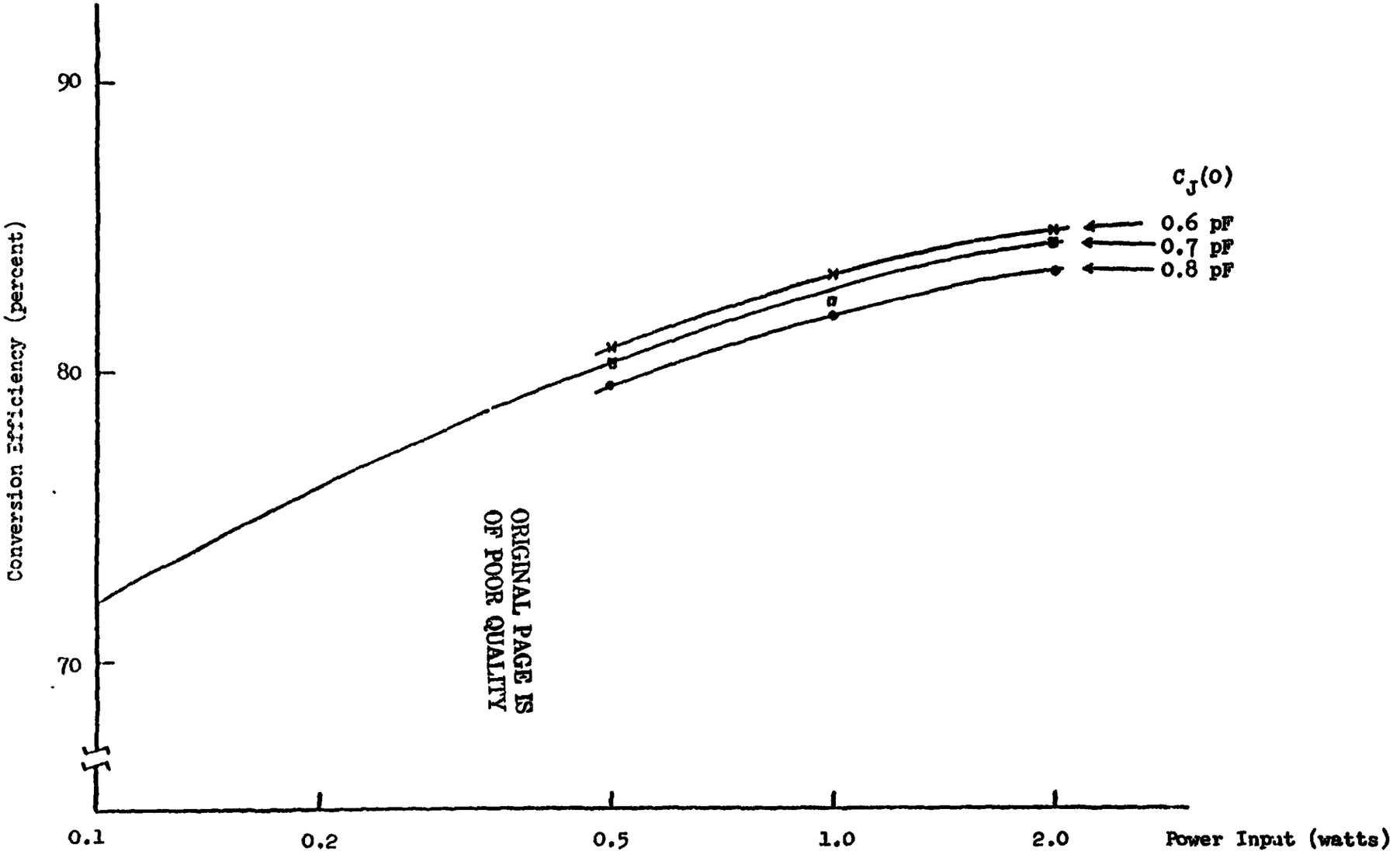
Input Power (watts)

Diode Zero-Bias Junction Capacitance $C_j(0)$ (pF)	.52	1.04	2.08
0.6	81.0	83.5	85.1
0.7	80.5	82.6	84.7
0.8	79.8	82.0	83.8

RF to DC Conversion Efficiency (percent)

Table 3-2 Output Equivalent Circuit Parameters and Conversion Efficiency as a Function of Power Level and Diode Junction Capacitance.

Fig. 3-15 Conversion Efficiency of Computer Simulation Model with Zero-Bias Junction Capacitance as a Parameter



circuit parameters changed somewhat with capacitance, in a manner considered significant. Unfortunately resource constraints did not permit a detailed evaluation of the effect on power combining inefficiency.

While the methodology of Section 3.3 and the system application in Section 3.4 is restricted to power density variations, it is important to realize that other parameters of the model can be similarly varied. This is considered a useful tool in evaluating parameter tolerances such as diode junction capacitance, necessary prior to production of a large scale, demonstration rectenna.

3.3 POWER COMBINING ANALYSIS

In this section of the report we present the method used for determining the loss in power which results when several rectenna elements, operating at different RF power levels, are connected in either series or parallel. The method used is the same as the one developed by Appelbaum et. al.[20] for determining the maximum power output of an array of non-identical electrical cells.

3.3.1 Power Combining Methodology

The method to be described assumes that output load line or volt-ampere (V-I) characteristics of each of the electrical cells to be combined are known. For the sake of discussion we show in Fig. 3.16 a general V-I characteristic of a rectenna element. This characteristic can be determined by either a circuit analysis of the rectenna element, by a computer simulation or by direct measurement of the output voltage and current for several load resistances as described in Section 3.2. It is assumed that the V-I characteristics are a function of some parameter θ of the rectenna element (for example incident RF power, diode junction capacitance, etc.). Given the V-I characteristics, then it is possible to determine the operating point for maximum power output. For example if the terminal voltage V is related to the terminal current I by:

$$V = f(I,\theta) \tag{3.24}$$

then the power output is

$$P = IV = I\,f(I,\theta) \tag{3.25}$$

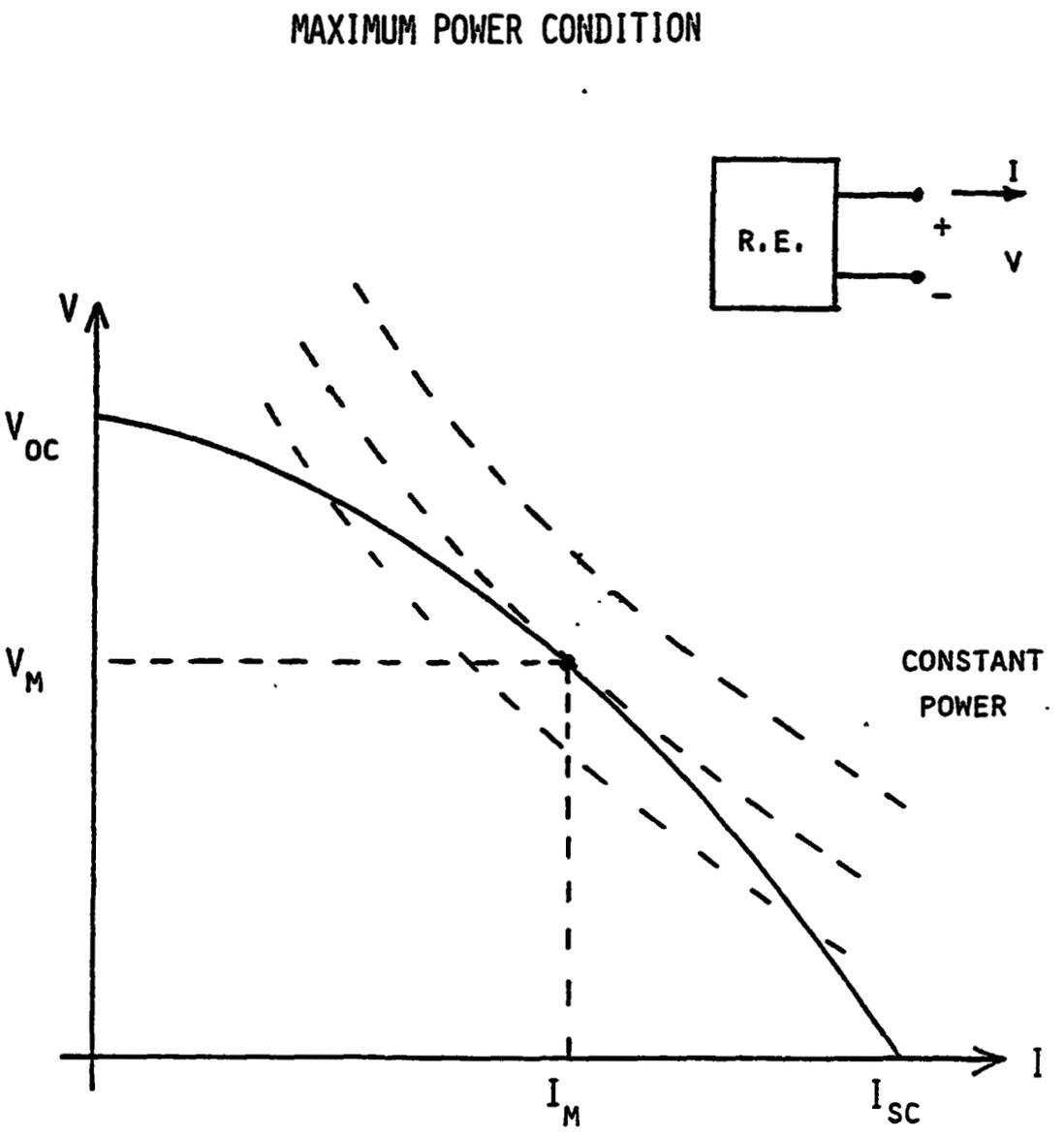


Figure 3-16 General V-I Characteristics of an Electrical Cell and Optimum Operating Point.

The current I_m at maximum power P_m is determined from the equation:

$$I_m = -\frac{f(I_m, \theta)}{f'(I_m, \theta)} = \frac{V_m}{r_m} \qquad (3.26$$

where V_m is the voltage at maximum power and $-r_m$ is the incremental or dynamic resistance at I_m. Notice that the above equation can be written as:

$$(R_L)_{op} = r_m \qquad (3.27)$$

that is at the optimum power the load resistance is equal to the incremental resistance.

In Fig. 3.17 we shown the V-I characteristics of two dissimilar rectenna elements as well as the points at which each of them deliver maximum power if operating independently. The same figure shows that if the elements are operated in parallel (common output voltage) or in series (common output current) then they will not operate at their optimum power output and their combined power output will be less than if operated independently. The difference in the maximum power of N separated single rectenna elements and the maximum power when they are interconnected can be defined as the power combining loss:

$$(\Delta P)_c = \sum_{j=1}^{N} (P_j)_{max} - (P_{max})_c \qquad (3.28)$$

and the ratio:

$$\frac{\Delta P_c}{\sum_{j=1}^{N} (P_j)_{max}} \qquad (3.29)$$

as the power combining inefficiency. The maximum power $(P_{max})_c$ when the several rectenna elements are interconnected can be determined as follows. Let

$$V = f(I, \theta_j) \qquad j = 1, 2, \ldots N \qquad (3.30)$$

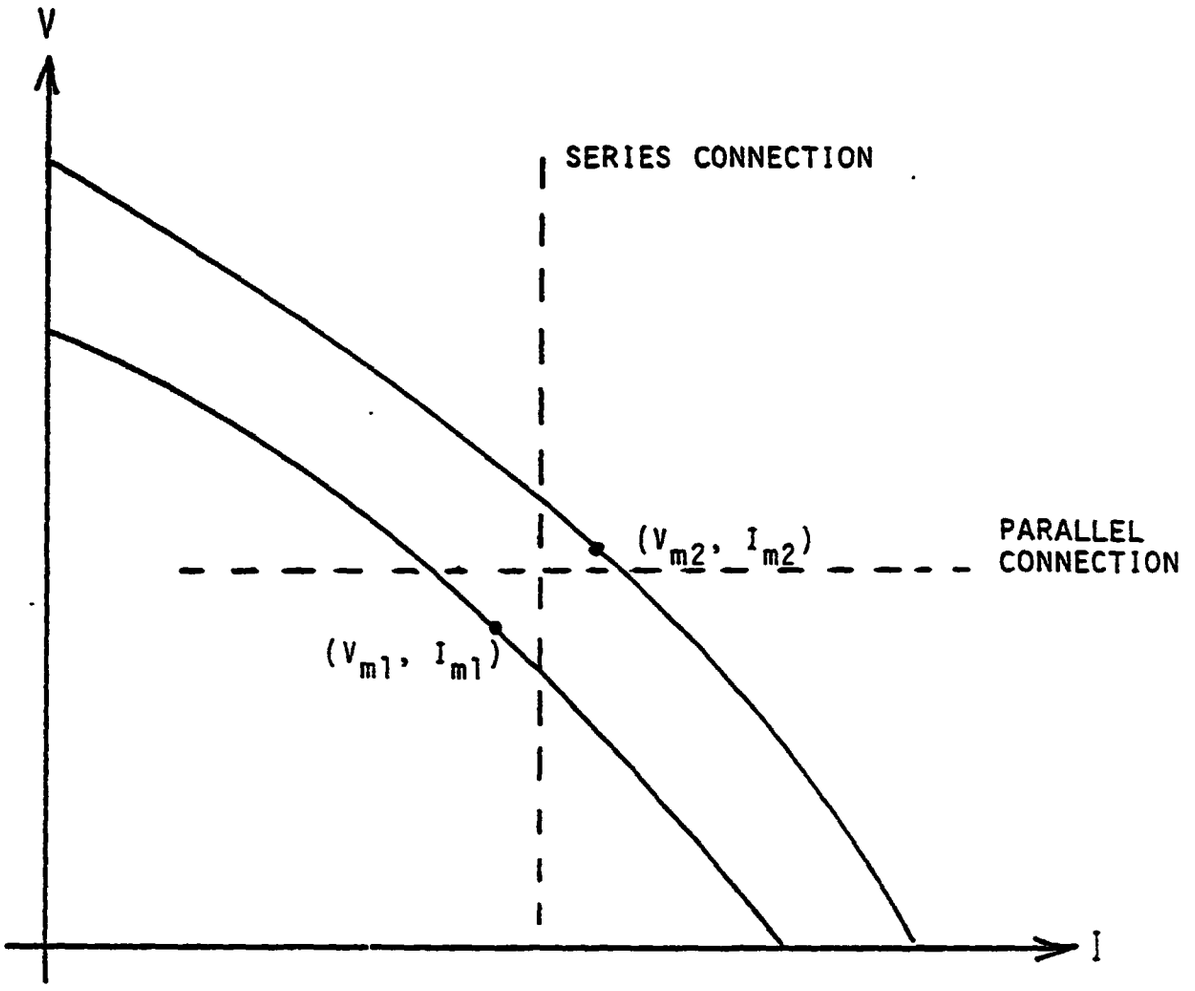


Figure 3-17 Series or Parallel Interconnection of Two Different Electrical Cells.

represent the V-I characteristics of each of the N elements. For a series connection, the voltage output is:

$$V = \sum_{j=1}^{N} f(I, \theta_j) \tag{3.31}$$

and the power output of the series connected array is:

$$P = I \sum_{j=1}^{N} f(I, \theta_j) \tag{3.32}$$

The current I_m and voltage V_m at maximum array power are given by:

$$I_m = \frac{\sum_{j=1}^{N} f(I_m, \theta_j)}{\sum_{j=1}^{N} f'(I_m, \theta_j)} \tag{3.33}$$

$$V_m = \sum_{j=1}^{N} f(I_m, \theta_j)$$

and the array maximum power is:

$$(P_{max})_s = I_m \sum_{j=1}^{N} f(I_m, \theta_j) \tag{3.34}$$

The case of parallel connected elements is treated in the same way. For this case it is more convenient to have the current expressed as a function of voltage:

$$I = h(V, \theta_j) \tag{3.35}$$

The voltage V_m and current I_m at maximum array power are given by:

$$V_m = - \frac{\sum_{j=1}^{N} h(V_m, \theta_j)}{\sum_{j=1}^{N} h'(V_m, \theta_j)} \tag{3.36}$$

$$I_m = \sum_{j=1}^{N} h(V_m, \theta_j)$$

and the array maximum power is:

$$(P_{max})_p = V_m \sum_{j=1}^{N} h(V_m, \theta_j) \tag{3.37}$$

Equations (3.31) - (3.37) are very general and it is desirable to apply them to two particular cases which are of special interest in dealing with arrays of rectenna elements. The first case is the one in which the array consists of elements in which the V-I characteristics are given by:

$$V = V_j - R_j I \tag{3.38}$$

The above case corresponds to electrical cells whose terminal behavior can be represented by an internal voltage source V_j in series with a resistance R_j as shown in Fig. 3.18. This can correspond to rectenna elements in which the V_j and R_j are both a function of the RF incident power as shown in Fig. 3-14 for the computer simulation model. In the case of an array of series connected cells, the power combining inefficiency is given by:

$$\frac{\Delta P_s}{P_{max}} = \frac{\sum_{j=1}^{N} V_j^2/R_j - \left[\sum_{j=1}^{N} V_j^2\right] \Big/ \sum_{j=1}^{N} R_j}{\sum_{j=1}^{N} V_j^2/R_j} \tag{3.39}$$

and in the case of parallel connected cells:

$$\frac{(\Delta P)_p}{P_{max}} = \frac{\sum_{j=1}^{N} V_j^2/R_j - (\sum_{j=1}^{N} 1/R_j)(\sum_{j=1}^{N} V_j/R_j \div \sum_{j=1}^{N} 1/n_j)^2}{\sum_{j=1}^{N} V_j^2/R_j} \qquad (3.40)$$

A second more restrictive case occurs if all the internal resistances are the same for the cells of the array. This case is shown in Fig. 3.19 and corresponds to the circuit model of the rectenna element derived in the closed form analysis (see Fig. 3-11). In this case the power combining inefficiency can be obtained from Eqs. (3.39) and (3.40) by making:

$$R_j = R \qquad j = 1, 2, \ldots N \qquad (3.41)$$

It can be shown that the power combining inefficiency is the same for parallel as well as for series connection and is given by:

$$\frac{\Delta P}{P_{max}} = 1 - \frac{(\sum_{j=1}^{N} V_j)^2/N}{\sum_{j=1}^{N} V_j^2} = 1 - \frac{(V_{av})^2}{(V^2)_{av}} \qquad (3.42)$$

This is an interesting result since it implies that in the first order of approximation the power combining inefficiency of an array of rectenna elements operating at different power levels is independent of the way in which they are interconnected (series or parallel). Since the output equivalent load resistances vary somewhat in the computer simulation model, the more general relationships given by Equations 3.39 and 3.40 are used for more detailed comparison. However since the output resistances vary only slightly with power level as shown in Fig. 3-14, differences between series and parallel combining would be expected to be slight, as shown in Sec. 3.3.2.

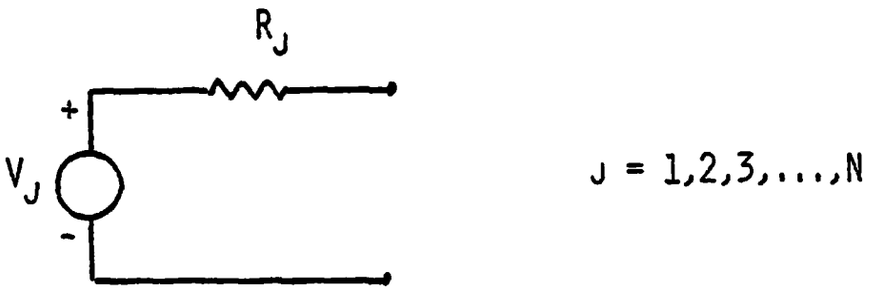


Figure 3-18 Output Equivalent Circuit of Rectenna Elements with Power Dependent Internal Parameters (appropriate for computer model).

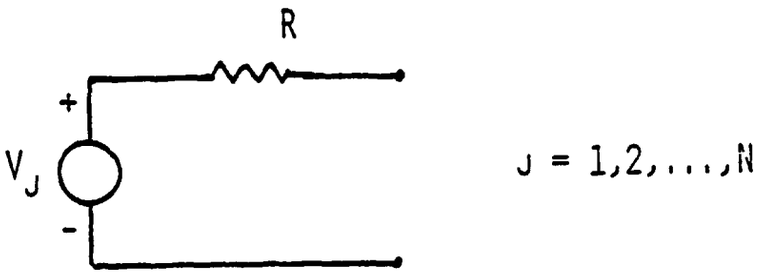


Figure 3-19 Output Equivalent Circuit of Rectenna Elements with RF Power Independent Internal Resistance (appropriate for closed form model).

3.3.2 Power Combining Results

A number of cases were calculated in detail to arrive at a comparison between parallel and series power combining inefficiency with the computer simulation model and to evaluate the usefullness of the closed form analysis. In performing these calculations discrete probability densities were used with sixteen categories of input power ranging from .52 to 2.08 watts ($.5 \leq \frac{P}{P_{nom}} \leq 2.0$) in approximately .1W steps. With the computer simulation model, the output equivalent circuit parameters were obtained at each power level using the functional form of the expressions given in Figure 3-14. Naturally the evaluation is simplified with the closed form model since the output resistance and normalized output open circuited voltage are independent of power.

Ten cases presented for illustrative purposes are shown in Table 3-3 with results presented in Table 3-4. A firm conclusion is that parallel and series power combining inefficiencies are nearly identical, and that the closed form model underestimates the power loss due to operation into a common load only slightly (by ~ 10% of the power combining inefficiency). The latter two cases shown indicate that the power combining inefficiency at the rectenna edge due to the power beam taper is very significant as discussed in detail in Section 3.4.

The effect of only one element operating at half power in a string of N total elements, N-1 operating at full power is shown in Figure 3-20. Thus if 10% of the elements in a string are at half power, a power combining inefficiency of 1.0% would occur, which drops to 0.1% if only 1% of the elements are operating at half power. Naturally the power combining inefficiency is reduced as the percentage of "unusual" elements decreases, and the calculated dependence shown in Figure 3-20 is reasonable.

The effect of the dynamic range of power variation, assuming a uniform power distribution over the dynamic range, is shown in Figure 3-21. With a 2 to 1 power range, a 1% power combining inefficiency is expected, raising rapidly to over 2.5% with a 3 to 1 power range. This curve has serious implications in DC buss design as described in Section 3-4.

While many other cases could be included, these results indicate that the power combining inefficiency will be a serious concern in SPS

Typical Power Distributions (discrete probability density functions)

$$\frac{P}{P_{nom}}$$

	.5	.6	.7	.8	.9	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7	1.8	1.9	2.0
Relative Number																
Case 1	.1	-	-	-	-	.9	-	-	-	-	-	-	-	-	-	-
Case 2	.3	-	-	-	-	.7	-	-	-	-	-	-	-	-	-	-
Case 3	.5	-	-	-	-	.5	-	-	-	-	-	-	-	-	-	-
Case 4	.1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	.9
Case 5	.3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	.7
Case 6	.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	.5
Case 7	.7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	.3
Case 8	.9	-	-	-	-	-	-	-	-	-	-	-	-	-	-	.1
Case 9	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$	$\frac{1}{16}$
Case 10	$\frac{1}{10}$	$\frac{1}{10}$	$\frac{1}{10}$	$\frac{1}{10}$	$\frac{1}{10}$	$\frac{1}{10}$	$\frac{1}{10}$	$\frac{1}{10}$	$\frac{1}{10}$	$\frac{1}{10}$	-	-	-	-	-	-

Table 3-3 Typical Power Distributions (discrete probability density functions) for Power Combining Evaluation.

	Power Combining Inefficiency (percent)		
	Computer Simulation Model		Closed Form Model
	Series Combining	Parallel Combining	(Series and Parallel)
Case 1	.88	.86	.81
Case 2	2.31	2.24	2.12
Case 3	3.13	3.04	2.86
Case 4	2.61	2.52	2.43
Case 5	7.31	7.07	6.77
Case 6	10.83	10.51	10.00
Case 7	12.05	11.75	11.05
Case 8	7.68	7.51	6.92
Case 9	3.98	3.87	3.67
Case 10	2.62	2.55	2.40

Table 3-4 Power Combining Inefficiency for Typical Cases using Computer Simulation Model and Closed Form Model.

Figure 3-20 Power Combining Inefficiency versus Number of Elements Combined with One Element at Half Power and Others at Full Power.

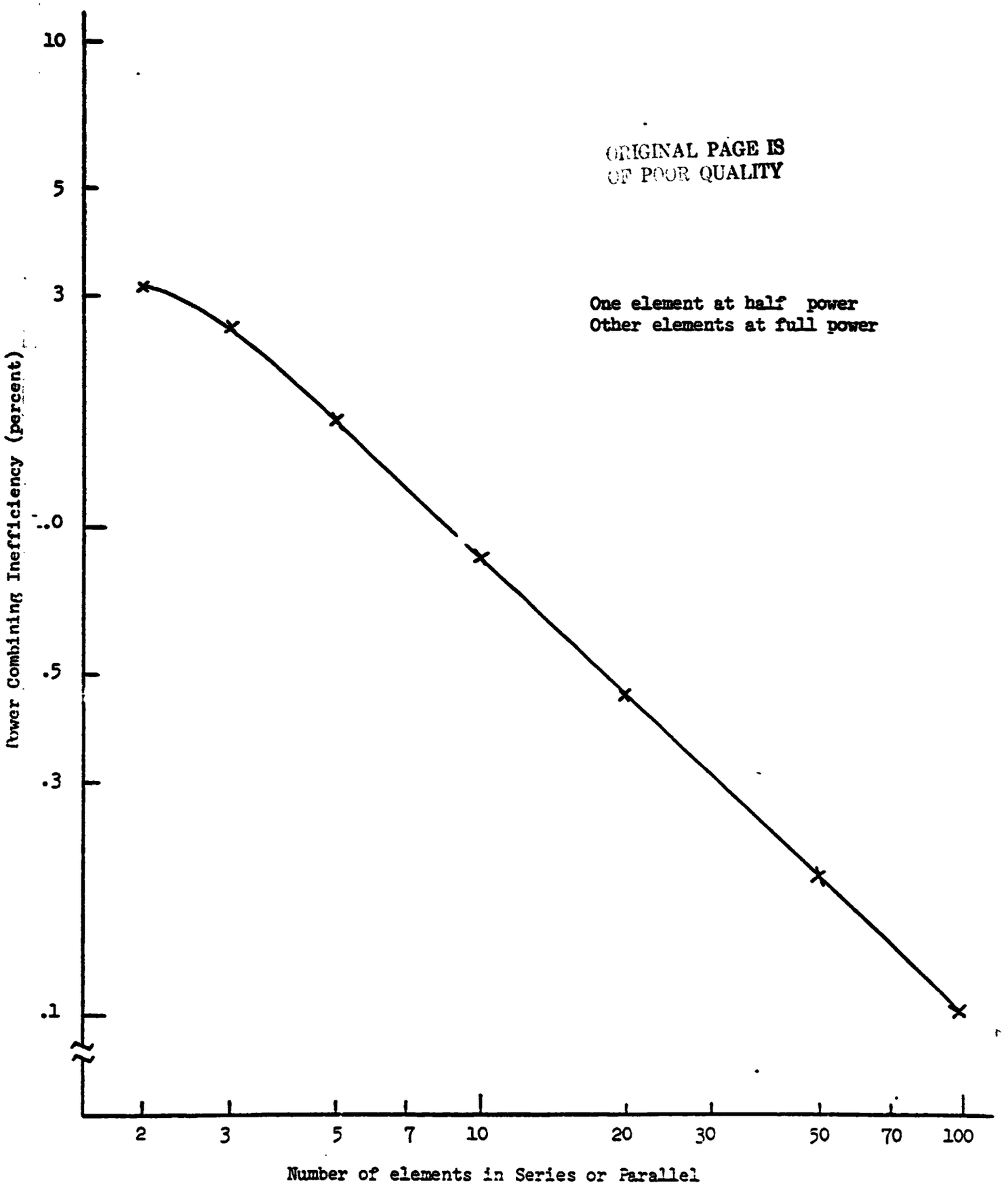
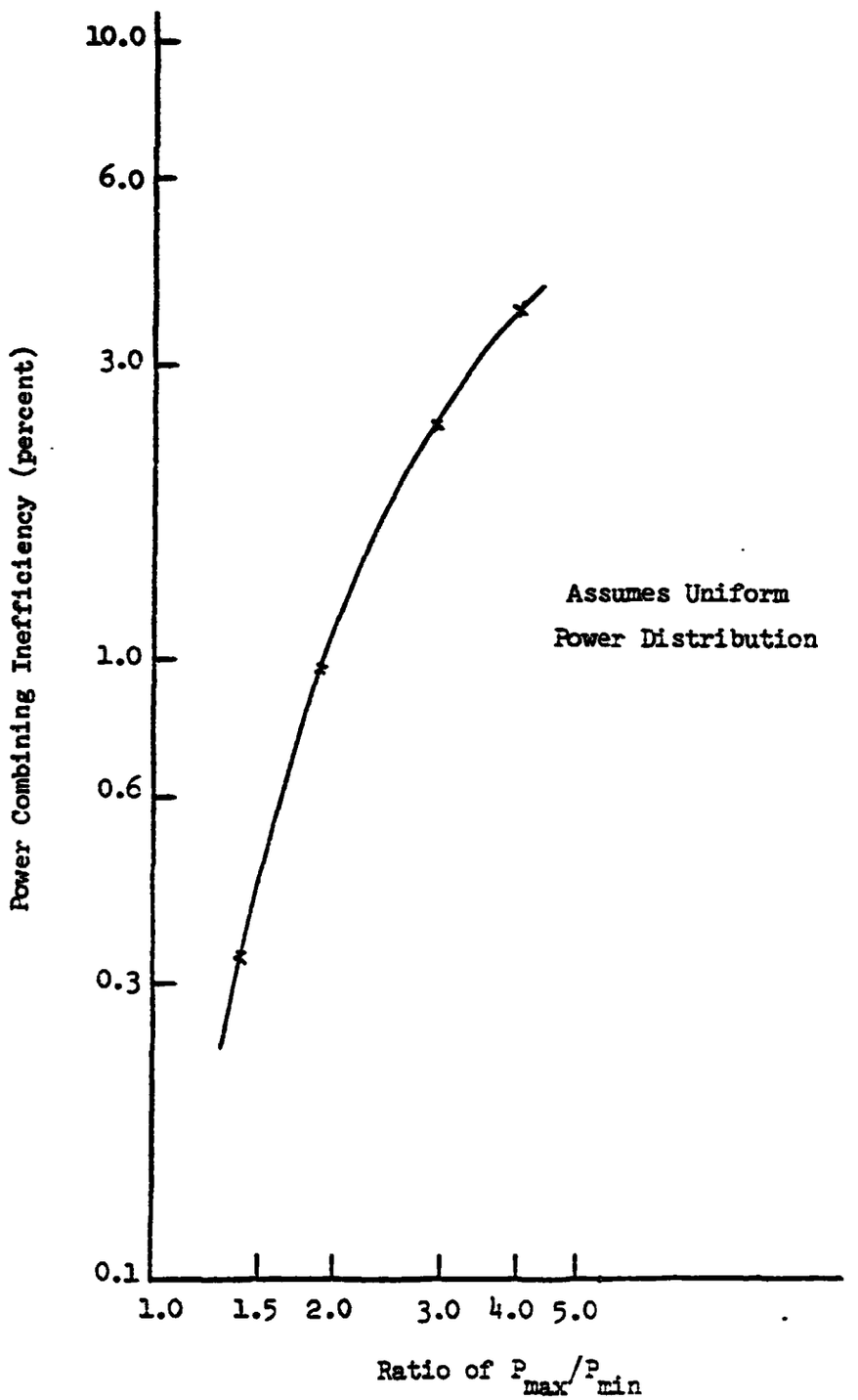


Figure 3-21 Power Combining Inefficiency versus Power Range (Ratio of P_{max}/P_{min}) assuming Uniform Power Distribution.



rectenna design and must be evaluated in detail. Two particularly significant conclusions are derived from these cases: (1) there is little difference in power combining inefficiency with series and parallel combining for the microwave power rectifier considered and (2) the closed form model results are extremely useful in evaluation of power combining inefficiency due to incident RF power differences.

3.4 POWER MODULE SIZE CONSTRAINTS

Most of the effort in this program was expended in developing the methodology of power combining, developing the necessary closed form and computer simulation models of the RF to DC conversion circuitry and in comparing series and parallel combining for a variety of power density distributions. However, we did make a preliminary evaluation of the impact of our results on SPS power efficiency and buss bar networking. These results are presented in this section, along with our simplifying assumptions.

The power density incident on each receiving element varies for three main reasons: 1. the power beam has a wide taper over the rectenna area, 2. diffraction from the top edge of the serrated rectenna results in a vertical variation of power density, 3. propagation induced variations across the 10 km power beam. The first two factors are reasonably well quantified, while the third is expected to be relatively small although not well specified to date. In this work power beam taper and diffraction considerations were taken from the JSC baseline design[4] and latest available Raytheon analysis[7] respectively.

With the baseline rectenna, simplest DC combining is along horizontal rows with element output combined in parallel and resultant "strings" combined in series. This has been always tactily assumed in Raytheon rectenna studies. In more detailed power grid interface studies, General Electric has recommended combining in circular or elliptical rings[21] (reasons not presented in resource material available to us). Although this involves numerous interconnections between rectenna "slats", the spatial density of these interconnections is probably tolerable if the power per ring is sufficiently large (50 megawatts per ring was proposed). Our results indicate that this latter approach is significantly better from a power

combining inefficiency viewpoint, although implications on manufacturing and assembly modularity, and therefore rectenna cost, needs to be considered. In addition ohmic losses in conductors connecting the slats are expected to be significant at the currents and dimensions involved.

Initially we present our evaluation of straightforward horizontal row combining, followed by a comparison with ring combining. Our discussion will be confined to power combining inefficiency comparisons only. Modularity of construction and power grid interface considerations have not been evaluated. In addition, we have not included conductor losses in this evaluation, a factor clearly limiting the baseline rectenna power module size.

Our approach has been to emphasize the effect of the power beam taper as this factor would be expensive to eliminate and is fairly well quantified from previous studies. Diffraction from the serrated antenna has been recently considered[7] but the effect depends upon row position in the slat and width of the slat. It can be minimized by making the slat wide and by combining only in rows. Of course, column combining is needed at some level to minimize the number of power grid interfaces. We have considered diffraction induced variations as a perturbation on power beam taper variations. The third factor propagation induced variations have not been adequately quantized at this time and have not been included in our work. While these effects will usually be small, during periods of atmospheric disturbances the effect could be significant (e.g. localized thundershowers). This could particularly be a concern with ring combining over geographically separated areas.

The power beam taper used in our evaluation is shown in Figure 3-22. The radial row taper (y=o) is obtained from the JSC baseline design,[4] with the non-radial row power density obtained from the assumed functional dependence i.e.,

$$PD = 23e^{-(r/2.72)^2} = 23e^{-.135(x^2 + y^2)}$$

where r, x and y are in km and PD is in mw/cm^2. Somewhat arbitrarily it is assumed that at the edge of the rectenna, rows can be combined over a

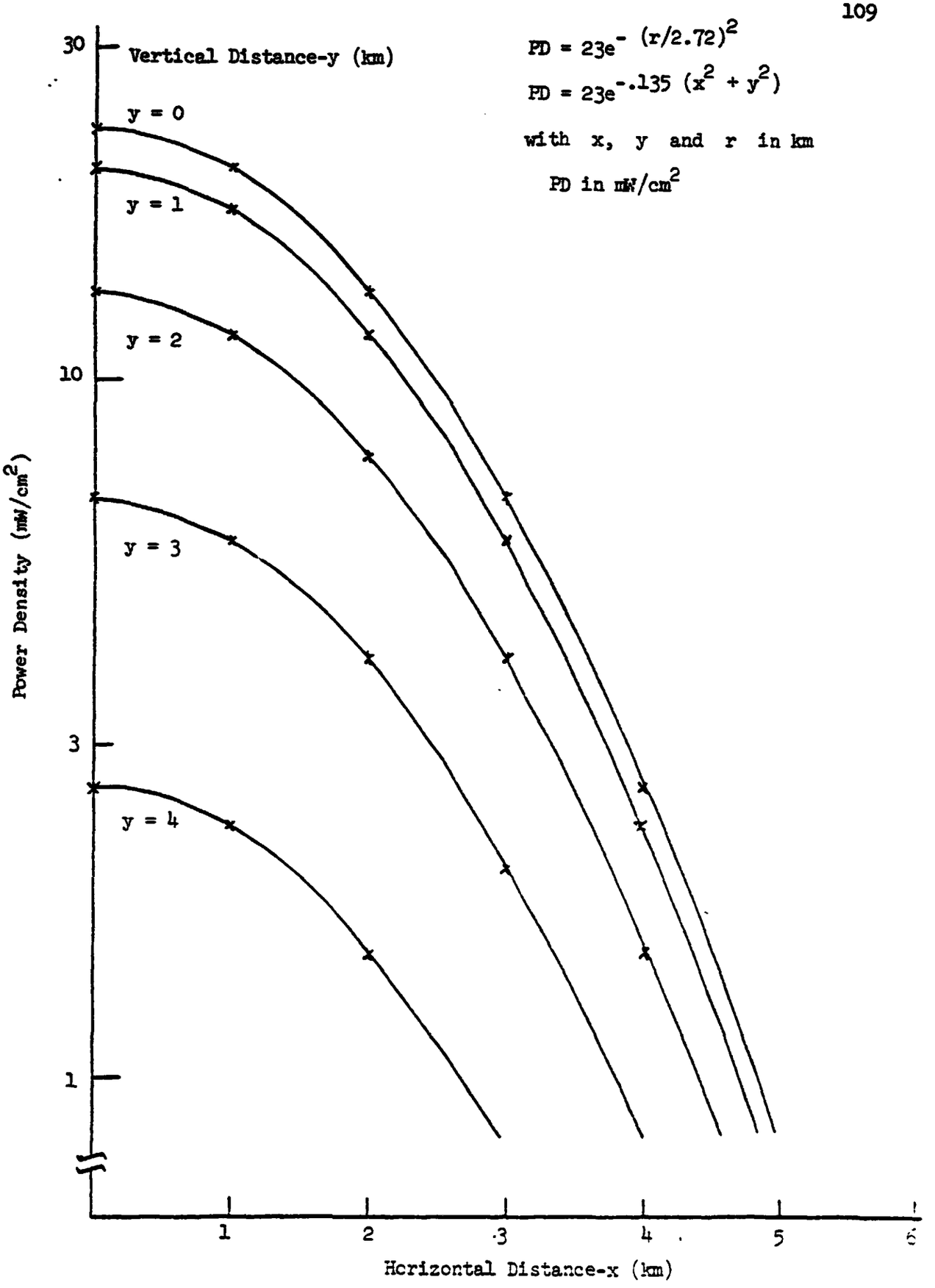


Figure 3-22 Power Beam Taper Used in Power Combining Evaluation (Horizontal Distance is Parallel to DC Combining Buss or East-West while

3:1 taper while near the middle of the rectenna combining is restricted to a 2:1 taper range. Starting from the edge of any y value, combining is performed from 1 to 3mW/cm^2, 3 to 9mW/cm^2, 9 to 18mW/cm^2 and 18mW/cm^2 to the center, as presented in the second column of Table 3-5. The range values are obtained from Figure 3-22. Using the element spacing and known power levels the number of elements in a row and power output per row are easily calculated.

By linearizing the taper over the ranges indicated one can use the power combining efficiency data presented in Figure 3-21, as the power distribution over any combining now is uniform. Note that the power loss (power combining inefficiency times power output per row) is nearly the same in power density ranges from 3 to 18mW/cm^2 and is lower near the center of the rectenna (where power taper is small) and at the edge (where power collected is small) with our assumptions. The power combining inefficiency averaged over the rectenna is about 1.3% in this case.

However, the power output per row is only 1 to 19 KW. If 1 MW power module are desired, the rectenna slat width gets prohibitively large at the edges of the rectenna ($\approx$ 50m). In addition the 1 MW power module would probably operate at $\sim$ 1 kV and 1 kA. Conductor losses are expected to be intolerable at such high current levels with the baseline elements. That is, an additional conductor buss would be required to accomodate such high currents.

It is clear that even with more modest power module sizes of 100 KW, numerous columns must be combined, so that diffraction induced variations will cause an increased power taper. While not included in our quantitative evaluation such a factor must be considered in further studies of row combining.

For combining in concentric elliptical rings, the power combining inefficiency is appreciably reduced for any sized module, at an expense of rectenna slat interconnection and decreased rectenna modularity. In fact, for any conceivable power module size, the power combining inefficiency due to power density differences becomes negligible if complete concentric ring combining is used. For example, if 50 MW modules are considered, the rectenna is divided into 100 concentric rings of average width of 50 m.

km	Radial Range for Specified Power Density Range 1-3 mW/cm^2	3-9 mW/cm^2	9-18 mW/cm^2	other	No. of Elements per Row	Power Output per Row (kW)	Power Combining Inefficiency	Size of Rectenna at for 1 MW Module (m)
10)	3.9-4.8 km	2.6-3.9 km	1.4-2.6 km	0-1.4 km (18-23 mW/cm^2)	11,500 16,700 15,400 18,000	1.2 5.0 10.4 18.9	2.5% 2.5% 1.1% 0.2%	56.3 13.5 6.5 3.6
1	3.7-4.7 km	2.4-3.7 km	0.9-2.4 km	0-0.9 km (18-20 mW/cm^2)	12,800 16,700 19,200 11,500	1.3 5.0 13.0 11.0	2.5% 2.5% 1.1% <0.1%	52.0 13.5 5.2 6.1
2	3.3-4.4 km	1.7-3.3 km		0-1.7 km (9-13 mW/cm^2)	14,100 20,500 21,800	1.4 6.2 12.0	2.5% 2.5% 0.4%	48.2 10.9 5.6
3	2.4-3.8 km			0-2.4 km (3-7 mW/cm^2)	18,000 30,800	1.8 7.7	2.5% 1.6%	37.5 8.8
4	0-2.7 km				34,600	3.5	2.5%	19.3

Table 3-5 Power Module Characteristics with Row Combining

More precisely the width of the ring varies from 260 m at the center of the rectenna, to 41 m at a 1 km radius, to 29 m at 2 km radius, to 28 m at 3 km, to 67 m at 4 km, to 260 m at the 5 km rectenna edge with the taper in Figure 3-22. The outermost ring would have a power combining inefficiency of only 0.3%, with a rapid decrease toward the center. The power loss over the rectenna would be below 0.1%. Naturally the effect would have to be reevaluated if pie sections were considered instead of complete rings.

We conclude that the power combining inefficiency is of considerable importance with row combining and will affect rectenna modularity and construction technique (continuous construction less desirable than "billboard" type construction and assembly). Ring combining is certainly preferred from the viewpoint of power combining inefficiency due to power beam taper but propagation induced variations must also be considered. In addition, conductor induced losses must be considered, from the rectenna element level to the power grid interface. It is clear that a major effort is needed to properly consider the multitude of factors involved in this area of rectenna design.

4.0 SUMMARY AND FUTURE DIRECTIONS

The list of key accomplishments of our program have been summarized in Section 1.3 of our report and described in detail in Sections 2.0 and 3.0. These accomplishments can be summarized concisely as follows:

DIRECTIONAL RECEIVING ELEMENTS

- Delineation of Desirable Characteristics for Rectenna Receiving Element with Comparison of Viable Alternatives (Sec. 2.1).
- Design and Analytical Evaluation of Printed Circuit Implementation (Sec. 2.2.1).
- First Order Electrical Design of Yagi-Uda Elements with Delineation of Tradeoff of Gain, F/B Ratio and Size (Sec. 2.2.2).
- First Order Design of Eight Rectenna Elements with Comparison of Advantages and Disadvantages (Sec. 2.3.1 and 2.3.2).
- Preliminary Cost Analysis Indicating That Directional Receiving Elements Lower Overall Rectenna Costs with Either Baseline Type or Printed Circuit Implementation (Sec. 2.3.3).

POWER COMBINING EVALUATION

- Implementation of Computer Model of Baseline Type Conversion Circuitry Using General Purpose Non-Linear Program (Sec. 3.1.1).
- Closed Form Models of Conversion Circuitry Developed (Sec. 3.1.2).
- Development of Methodology of Power Combining Inefficiency Evaluation (Sec. 3.2 and 3.3.1).
- Power Combining Inefficiencies for Series and Parallel Combining Evaluated with Comparison of Results with Computer Simulation and Closed Form Models (Sec. 3.3).
- Impact of Power Combining Inefficiencies on Power Module Sizing and DC Buss Network Evaluated (Sec. 3.4).

Although the program has been geared toward obtaining results useful for current SPS system definition, there are a number of extensions of this program which should be considered at this time. These are outlined as follows:

DIRECTIONAL RECEIVING ELEMENT EXTENSIONS

- The Yagi-Uda receiving element analysis indicates that appreciable rectenna cost savings can be expected. More design is needed to arrive at more rigorously obtained electrical parameters, thus replacing the first order parameters given in Table 2-8 and discussed in Sec. 2.2.2.
- Consideration of alternative Yagi-Uda designs besides the three and six element designs evaluated to date.
- Structural design is needed to evaluate the mechanical advantages and disadvantages of printed circuit implementation, as well as delineate the advantages of eliminating the ground plane mesh as considered feasible with Yagi-Uda elements with high F/B ratio.
- Development of a small array test structure for experimental evaluation of the Yagi-Uda rectenna element.
- Further consideration of alternative antenna elements. Backfire arrays should be considered as an alternative to the higher gain Yagi-Uda arrays.

POWER COMBINING EVALUATION EXTENSIONS

- Use of closed form model results in evaluation of alternative DC buss networking alternatives (instead of row based or complete ring based designs).
- Use of computer simulation model to optimize device characteristics for low, medium and high power levels, including performance and reliability factors.
- Extension of computer simulation model and modification of closed form analytical models to evaluate methods of reducing harmonic reradiation.
- Use of closed form and computer simulation models in evaluating effects of transient loads on the spectrum of rectenna element reradiation.
- Use of closed form and computer simulation models to evaluate effects of device and circuit parameter tolerances.

These extensions are needed to reduce projected rectenna costs with innovative electrical and structural design, to properly interface the rectenna with the power grid and to evaluate an important environmental impact of the SPS (reradiation from rectenna).

REFERENCES

1. W. C. Brown, "Electronic and Mechanical Improvement of the Receiving Terminal of a Free-Space Microwave Power Transmission System", NASA-CR-135194, August 1977.

2. R. D. Dickinson, "Evaluation of a Microwave High-Power Reception-Conversion Array for Wireless Power Transmission", JPL Tech. Memo 33-741, September 1975.

3. W. C. Brown, "Free-Space Microwave Power Transmission Study Phase III and Final Report", NASA-CR-144151, September 1975.

4. Lyndon B. Johnson Space Center - NASA, "Initial Technical, Environmental and Economic Evaluation of Space Solar Power Concepts", JSC 11568, August 1976.

5. R. J. Gutmann, "Microwave System Studies Affecting SPS Rectenna Performance", JSC Internal Report, August 1977.

6. Boeing Aerospace Company, "Solar Power Satellite, System Definition Study Part II - Vol. IV Microwave Power Transmission Systems", NASA Contract NAS9-15196, December 1977.

7. Boeing, General Electric and Raytheon, "SPS System Evaluation Phase III Study Document", June 1978, preliminary copy.

8. J. J. Nahas, "Simulation and Experimental Studies of Microwave-to-DC Energy Conversion Systems", NASA Grant No. NSG-3070, (undated but approximately January 1976).

9. J. Appelbaum, J. Bany and A. Braunstein, "Array Power Output of Non-Identical Electrical Cells", 12th Annual Intersociety Energy Conversion Engineering Conference (IECEC), 1977, pp. 1686 - 1692.

10. S. Uda and Y. Mushiake, Yagi-Uda Antenna, Sasaki Publishing Co., 1954.

11. R. W. P. King, R. B. Mack and S. S. Sandler, Arrays of Cylindrical Dipoles, Cambridge University Press, 1968.

12. I. L. Morris, "Optimization of the Yagi Array", Doctoral Thesis, Harvard University, April 1965.

13. G. L. Matthaei, L. Young and E. M. T. Jones, Microwave Filters, Impedance Matching Networks and Coupling Structures, McGraw-Hill, 1964.

14. D. A. Daly, S. P. Knight, M. Caulton and R. Ekholdt, "Lumped Elements in Microwave Integrated Circuits", IEEE Trans. Microwave Theory and Techniques, MTT-15, December 1967, pp. 713 - 721.

15. C. A. Chen and D. K. Cheng, "Optimum Element Lengths for Yagi-Uda Arrays", IEEE Trans. Antennas and Propagation, AP-23, January 1975, pp. 8-15.

16. R. W. Klopfenstein, "Corner Reflector Antennas with Arbitrary Dipole Orientation and Apex Angle", IRE Trans. on Antennas and Propagation, AP-5, July, 1957, pp. 295 - 306.

17. J. D. Kraus, Antennas, McGraw-Hill, 1950.

18. E. A. Wolff, Antenna Analysis, John Wiley, 1966.

19. R. J. Gutmann, "Output Power Variations with Solar Power Satellites", Journal of Solar Energy, 21, November 1978, pp. 323-330.

20. J. Appelbaun, J. Bany and A. Braunstein, "Array Power Output of Non-Identical Electrical Cells", 12th Annual IECEC Conference Digest, 1967, pp. 1686 - 1692.

21. Conversation with R. H. Dietz, NASA, JSC.