New Techniques In Television To Provide Research In Three-Dimensional Real-Time or Near Real-Time Imagery And Reduced Cost Systems For Teleconferencing And Educational Uses

Technical Report: Part I

Yoh-Han Pao, Paul Claspy, John Allen and Frank Merat

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NATIONAL AERONAUTICAL AND SPACE ADMINSTRATION
LEWIS RESEARCH CENTER

Grant No. NSG-3085

Period of Grant: 20 October 1975 - 20 October 1978

Department of Electrical Engineering and Applied Physics
Case Western Reserve University
Cleveland, Ohio 44106

NEW TECHNIQUES IN TELEVISION TO PROVIDE RESEARCH IN THREE-DIMENSIONAL REAL-TIME OR NEAR REAL-TIME IMAGERY AND REDUCED COST SYSTEMS FOR TELECONFERENCING AND EDUCATIONAL USES

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Chapter 1

INTRODUCTION

In recent years the rapid growth of information needs has made obvious the requirement for more efficient and cost effective use of communication channels and the necessity for optimal information content in each transmission through these channels. This report presents the results obtained to date in an extensive research and development program, which offers an important partial solution to this problem, being carried out at Case Western Reserve University.

The program involves, first, the design, development, and construction of a novel black-and white and color Variable Frame Rate Television System (VFRTS) which permits video transmission over channels having less than the standard 4.5 MHz video bandwidth and, second, a system for electronic recording, transmission, and reproducing holographic information. The VFRTS system has been successfully demonstrated and preliminary, encouraging, results have been obtained with the holographic system.

The novel feature of the VFRTS system is that it combines the large analog storage capability of a magnetic video disc as a mass memory with the reliability of digital technology for the actual time expansion and compression. The use of a magnetic disc for video frame storage makes expansion to multiple frame storage a simple matter of adding appropriate read-write electronics for each new channel rather than adding a complete new memory for each, as

required in all digital systems. In addition, the use of a novel technique for transmission of color video signals resulted in a requirement for relatively modest modifications of the original black-and-white system.

The holographic transmission system, by employing a phase modulated reference wave, enables electronic recording, transmission, and reproduction of holograms using a conventional television format, with a low resolution, nonintegrating camera and a coherent mixer. When combined with the video disc system it offers the potential capability of producing a wide perspective hologram by appropriately combining several narrow perspective holograms.

Because of the volume of material that has been generated relative to the nearly-completed VFRTS system, we have chosen to present this report in three volumes. In addition, Volume I is further subdivided, as described below:

Volume 1:
1. Technical design considerations and system operation of the black-and-white VFRTS.
2. Progress report on the electronic holography system.

Volume 2: Technical design considerations and system operation of the color video VFRTS.

Volume 3: Flow diagrams, schematics, parts lists, etc., for the black-and-white and color VFRTS systems.

In Chapter 2 of this volume each of the subsystems of the black-and-white VFRTS is discussed. In Chapter 3 the progress made to date

on the electronic holography system is discussed. While each chapter has concluding remarks about the system discussed therein, Chapter 4 presents general concluding remarks.

2. VARIABLE FRAME RATE TELEVISION SYSTEM

2.1 INTRODUCTION

2.1.1 BACKGROUND

The point-to-point transmission of visual scenes is regularly accomplished by real-time television systems. For private users the transmission channel may take the form of a coaxial cable, microwave system, or optical link. The basic requirement which must be satisfied by all these transmission techniques is that of sufficient bandwidth; the U.S. standard television signal requires a minimum of 4.2 MHz baseband response. While slight reductions are possible, picture quality deteriorates rapidly for channel bandwidths below 2 MHz. Attempts have been made to select reduced resolution real-time scan formats allowing bandwidth requirements to be relaxed to $\sim$ 1 MHz but the difficulty of realizing even this more modest requirement is immense if one is forced to use inexpensive narrowband channels such as those provided by equalized land-lines or high frequency radio links.

Wideband transmission channels present a trade-off among cost, performance and versatility. Microwave systems are probably the most cost-effective solution for point-to-point transmission in that the technology is mature and short-hop AM terminals are relatively inexpensive (<$10,000). Line of sight limitations and licensing requirements in conjunction with frequency allocation problems posed by potential adjacent-channel interference present the microwave user with a relatively limited and expensive network capability. This is especially so in crowded urban areas where channels are becoming increasingly difficult to obtain. While in principle cable

systems utilizing repeaters can be run over large distances in virtually any network configuration, the cost and time involved in the installation of such facilities renders them impractical in all but a very limited set of circumstances such as in-house video distribution or large commercial cable television systems. How then might individual interactive users separated by tens or hundreds of miles exchange visual information without entertaining the exhorbitant costs of dedicated wideband transmission facilities?

A solution of this difficulty is afforded by a system configuration known historically as slow-scan television, whose chief characteristic consists of transmitting much less information than the real-time format by means of frame-rate reduction; that is, real-time transmission is sacrificed to attain reduced bandwidth and hence an affordable and versatile transmission channel. Some systems use special cameras and monitors designed to operate at significantly reduced scan rates, but if motion occurs at the transmission site, the camera inevitably blurs the image. The received picture is built up slowly on a long retention C.R.T. monitor; these displays generally employ green or yellow phosphors, have small viewing size ($\sim$ 4" diagonal), suffer from low resolution and exhibit spatially non-uniform image brightness. These characteristics tend to make slow-scan television a psychologically unpleasant viewing medium and applicable to a relatively small class of telecommunication user needs.

If one wishes to transmit clear, stable, high-resolution

images using a reduced bandwidth format, some form of video buffer memory is needed, both at the transmission site to prevent blurring and at the receiver to allow for a stable, flicker-free image which can be processed and displayed using conventional television equipment. Conceptually the transmit buffer is loaded with a single picture or television frame at real time rates ($\sim$ 1/30 second) and unloaded at a considerably slower rate - hundreds or thousands of times more slowly to match the available channel bandwidth. At the receive site the buffer operates in reverse, i.e., it is loaded slowly from the channel and then circulated at real-time rates to continuously produce a stable full-bandwidth video signal for the monitor. Of course a picture cannot be received while one is being displayed unless two receive buffers are employed, multiplexed such that one is being loaded from the channel while the other provides the previous signal for display. In this fashion no time is lost waiting for a transmission to be received and the monitor updates at the maximum rate allowed by the channel.

2.1.2 SYSTEM OBJECTIVES

The evolution of this project has dictated certain major criteria which must be satisfied in the system specifications. This section examines those needs in the light of available technology. Necessary performance objectives include:

1) Ability to interface standard television inputs and displays.
2) Constant, steady displays at the receive site with no attendant waiting period for picture buildup.
3) Maximum frame update rates consistent with available channel bandwidth and system complexity.
4) Transmission of color stills without penalty of decreased resolution or increased transmission time over monochrome transmissions.
5) Utilization of cost-effective technical solutions to make available low-cost terminals.
6) Picture quality appropriate to home viewing standards rather than the more stringent studio quality called for in conventional microwave network transmissions.

Video buffer memories allow the first three criteria to be satisfied. Transmission of the baseband video signal in a timebase expande form, and hence bandwidth reduced, affords the fastest possible transmission speed without complex bandwidth compression algorithms, which vastly increase the cost and complexity of a terminal and

inevitably result in degradation for certain types of picture detail. A further advantage of this scheme involves system checks and maintenance - the reduced bandwidth signal is an exact duplicate of the real-time signal. Inspection of test signals present in the vertical interval can be readily made to evaluate system performance. For example, standard multiburst and sine-squared pulse signals inserted in the real-time television signal prior to transmission are thus carried through all processing steps and can be inspected in the narrow band channel as well as at the receive terminal after time-base compression.

The direct timebase expanded analog format also lends itself to NTSC color transmission without significant system electronics alterations and with no inherent penalty in resolution or transmission speed. It must be understood, however, that channel requirements, particularly in group delay flatness become more stringent and must be controlled by proper equalization procedures.

Television picture quality is necessarily subjective; it is difficult to assign an "optimum" trade-off in terms of signal-to-noise ratio, resolution, transient response, etc. Table 2.1 outlines eleven distortion parameters which can be used to characterize color picture quality; both studio and acceptable viewing standards are compared. Effort was made in constructing this table to determine a rationale for picture acceptability and the appropriate notations explain the decision criteria. The acceptable standards outlined form a basis for overall system picture quality, but are only

TABLE 2.1 (References appear on next page)

TELEVISION SIGNAL DISTORTION LIMITS

TYPE	TEST WAVEFORM	STUDIO SPEC	ACCEPTABLE SPEC
1) "K" - Factor[1]	2 T Pulse and Bar	K = 1.0 - 1.5%[2]	K = 3.0-5.0%[3]
2) Tilt	Full Field 60 Hz Squarewave	0.5-1.0%[4]	5%[5]
3) Frequency Response (dc-4.2MHz)	Multiburst	Flat ± 0.25 db[2]	6
4) Chrominance/Luminance Delay	12.5 T Modulated Sine-squared pulse	deferred[2]	100 nsec (flat)[7] 250 nsec (shaped)
5) Chrominance/Luminance Gain	"	deferred[2]	Satisfied by 3)
6) Differential Gain @ 3.58 MHz	Stairstep modulated with 20 IRE unit CW subcarrier	APL Max.[2] 10% 1.0db 50% 0.6db 90% 1.0db	± 2 db[8] (any APL)
7) Differential Phase @ 3.58 MHz	"	APL Max 10% ± 2° 50% ± 1.5° 90% ± 2.0°	± 6°[8] (any APL)
8) Chrominance into Luminance	Modulated Pedestal	No Spec	± 5IRE units
9) Luminance Nonlinearity	Stairstep	No Spec	± 5%
10) Signal to Wideband Noise Ratio	----	56db $\frac{pp}{rms}$[2] (weighted)	46db $\frac{pp}{rms}$[9] (weighted)
11) Signal to Hum Ratio	----	40 db	30 db

1 Methods of Waveform Testing, Pulse and Bar - "K" Factor, A.B.C. Laboratory Report No. 26, A. N. Thiele

2 EIA Specification RS-250A, "Electrical Performance Standards for Television Relay Facilities", Feb. 1967.

3 B.B.C. Eng. Div. Technical Instruction V5-Sine-Squared Pulse and Bar Testing Methods, Mar. 1961.

4 EIA Specifications RS-170A, "Electrical Performance Standards - Monochrome Television Studio Facilities", Nov. 1957.

5 Can be arbitrarily reduced using keyed clamping in video processing amplifiers; all 106 proc amps have this feature.

6 The most crucial factor observed by the experimenter concerns the smoothness of the roll-off, not the absolute attenuation at the band edge.

7 Lessman, "Subjective Effects of Delay Difference Between Luminance and Chrominance Information of the NTSC Color Television Signal", SMPTE Journal, Vol. 80, No. 8, Aug. 1971, pg. 624.

8 Cavanaugh, J. R., et al., "Subjective Effects of Differential Gain and Differential Phase Distortions in the NTSC Color Television Picture", SMPTE Journal, Vol. 80, No. 8, Aug. 1971, pp. 623-624. Values reflect BBC study; U.S. results using slightly different acceptability criteria are $\pm$ 1.4 db. and $\pm$ 5° respectively.

9 Consistent with available S/N of non-studio quality B & W and color television cameras.

intended as a benchmark.

In summary, the transmission system should include video buffer memories at each terminal, employ direct timebase expanded signals throughout and will seek to satisfy the picture quality levels listed in Table 2.1.

The next section explores various technologies applicable to video buffer memories and identifies the most cost/performance effective approach consistent with stated objectives.

2.1.3 VIDEO MEMORY TECHNOLOGIES

It can thus be seen that the principle sub-system needed for high quality narrowband television transmission is indeed a video buffer memory. These memories must be capable of real-time operation as well as slow access and they should not perceptably degrade the picture signal-to-noise ratio or resolution. Desirable features further include non-volatility, low initial cost, (three are required for a single simplex channel), high reliability and low maintenance costs. The technologies available for such memories are shown in Table 2.2 which includes an evaluation of pertinent characteristics.

Minimum criteria for a suitable video buffer technology include low cost, and small size, weight and power consumption consistent with acceptable technical performance. Estimates for these parameters for a hypothetical 6 frame capacity memory sufficient for a full-duplex channel appear in Table 2.3 . Inspection of Table 2.3 indicates that the magnetic video disc offers an optimum choice for a video memory for multiple frames. This advantage becomes even more pronounced if a single disc with multiple heads is configured as a buffer for a multi-channel narrowband video system. For example, a ten channel full-duplex system would require 3 x 10 or thirty frames stored at each location.

The current trend in digital memory technology shows promise in cost, size and power reduction for frame storage. For applications which require a mechanically rugged package-mobile, airborne, or space borne - digital technology would be the appropriate

TABLE 2.2 COMPARISON OF MOST COMMON VIDEO STORAGE TECHNOLOGIES

	Single Frame Store		Multiple Frame Store	Mass Store
Characteristics	Storage Tube	Digital Frame Store	Video Magnetic Disc	Quadriplex Videotape
Storage Method	Direct Video	PCM(Typ.8 bit)	Analog FM	Analog FM
Access	Random	Random	Parallel or Serial	Serial
Access Time	$\sim 10^{-4}$-10^{-3} sec	$\sim 10^{-7}$ sec	$\sim 10^{-2}$ sec	Shuttles at $\sim 10^{3}$ frames/sec
Luminance Linearity	$\sim$ 3%	< 1%	$\sim$ 1%	$\sim$ 1%
Luminance Resolution	$\sim$30-40 levels	256 levels (8 bit)	Continuous	Continuous
Volatility	10-15 minutes typ.	Non-volatile w/battery backup	Non-volatile	Non-volatile
Storage Capacity	1 Frame	1 Frame/Store	1-10^{3} Frames	10^{5}-10^{6} frames
Cost Range	$\sim$$5000-6000	$10,000-30,000	$3000 - 100,000	$100,000-200,000
Direct Color Storage Available	No	Yes	Yes	Yes
Support Complexity	Moderate	High	Moderate	High
Reliability	Moderate	High	Moderate	High
Expected Maintenance	Low	Low	Low	High

TABLE 2.2 (cont'd)

Characteristics	Storage Tube	Digital Frame Store	Video Magnetic Disc	Quadriplex Videotape
Parts Replacement Costs	High	Low	Low	Moderate
Cost/Frame Stored	High	Very High	Moderate	Very Low
Suitable as Video Buffer	Yes	Yes	Yes	No
Typical Manufacturer	Princeton Electronic Products	Quantel	Ampex	Ampex

TABLE 2.3 TRADEOFFS FOR 6 FRAME VIDEO STORE BASED UPON CURRENT COMMERCIAL PRODUCTS

Parameter	Storage Tube	Magnetic Video Disc	Digital Frame Store
Est. Cost for Basic Memory	∿$30,000	$10,000 - 20,000	∿$100,000
Memory Volume	∿ 8 cu. ft.	2-4 cu. ft.	∿ 12 cu. ft.
Weight	300 lbs.	30-50 lbs.	∿ 350 lbs.
Power Consumption	∿ 1.5 kw	0.2-0.3 kw	1-2 kw

choice despite the increase in cost. In the future it is expected that an all digital memory could become a most cost effective solution for video memories of limited capacity. It should however be emphasized that frame capacity expansion is a direct expansion of hardware in the digital memory, whereas the disc need only acquire additional tracks, which are naturally available on the continuous magnetic surface. A single moving head can access hundreds of individual frames (if one frame is recorded per track) on a single 10" disc memory. It can be clearly seen that for bulk picture storage and processing, the magnetic video disc will still occupy a respectable technical position for many years to come.

2.1.4 MONOCHROME SYSTEM

Prototype Requirements

To establish criteria for prototype construction, several basic design decisions had to be made at the outset. The target criteria were:

1) Simple point-to-point simplex operation over dedicated landline.
2) Picture quality commensurate with real-time television.
3) Choice of suitable frame refresh rate in accordance with viewer acceptability.
4) Choice of appropriate transmission format.

A transmitter unit and receiver unit were constructed, each with its own disc memory. Both can be expanded to become an actual transceive terminal by additional video heads and electronics. Timebase alteration is performed in each unit by digital sampled data systems. Thus the number of samples per line must be sufficient to resolve the required image detail. The resulting sample clock must be at least twice the highest frequency to be recovered in the video signal to avoid aliasing errors (Nyquist's Theorem). To reproduce a 4.2 MHz video upper bandlimit, a clock of approximately 10.2 MHz was chosen as it allows sufficient guard bands for realizable video low-pass filters, but yet covers virtually the entire visible television line using 512 samples, a convenient multiple of 2.

The number of actual line periods per frame is 525 in the U.S. system; not all carry visible picture detail. Of these,480 are sufficient to fill the screen and not significantly distort the aspect ratio of the picture. The resulting number of samples to be transmitted is 245,760 per frame. If these samples are PCM encoded and digitally transmitted to the receive terminal, the required minimum channel capacities can be calculated for various sample word lengths. Table 2.4 illustrates these requirements for various compression factors and quantization levels. It should be borne in mind that anything below 64 levels / pixel (6 bits) is not sufficient to produce an acceptable picture quality due to quantization noise. For color transmission 256 levels (8 bits) are required due to highly visible chroma noise.

Table 2.5 illustrates analog channel bandwidths and transmission times for various compression factors. It can be seen that a 15 KHz landline will allow a refresh in 5 seconds, which corresponds to 150-200 Kbs.

Some discussion has been devoted to digital vs. analog transmission formats, and the comparison has shown that the only technique with potential for rapid enough updates is analog transmission. At this point one may usefully ask: what refresh rates are useful? Ad hoc tests conducted in our facility revealed that real-time or very near real-time (i.e., 2 to 3 times compression) displays were psychologically identical and the latter only failed when violent picture movement occurred. The region from 10 refreshes per second

TABLE 2.4 COMPARISON OF CHANNEL CAPACITIES FOR PCM DIGITAL TRANSMISSION*

Word Length (bits)	Levels	Approx. Quant. S/N (db)	Required Bit Rate** Compression Factor 1	75	300	1500
4	16	24	29.4 Mbs	393.2 Kbs	98.3 Kbs	19.6 Kbs
5	32	30	36.8	489.1	122.8	24.5
6	64	36	44.2	589.8	147.4	29.4
7	128	42	51.6	688.1	172.0	34.4
8	256	48	58.9	786.4	196.6	39.2

* Data reflects quantization of 245,760 samples/frame.

** Actual bit rate must be higher to include word and block formatting bits for field and line identification.

TABLE 2.5 COMPARISON OF VARIOUS POTENTIAL VFRTS BANDWIDTHS

Bandwidth Compression Factor	Typical Analog Channel	Available Storage Mechanisms	Bandwidth (flat to±.25db)	Transmission Time (seconds) Field	Frame
1 (real-time)	• coaxial cable • microwave • satellite • optical	• videotape recorder • videodisc • digital frame store	4.2 MHz	1/60	1/30
75	• all of above • equalized landlines • point-to-point radio transmission	• instrumentation recorder • floppy disc	56 KHz	1-1/4	2-1/2
300	• all of above • studio-to-transmitter audio links • broadcast FM • ultrasonic links	• high quality audio tape recorder • phonograph records • optical film sound track • floppy disc	14 KHz	5	10
1500	• all of above • dial-up telephone network • voice grade channels • broadcast AM	• low quality audio • audio tape recorder • floppy disc	2.8 KHz	25	50

to about 1 refresh is an area of some interest; viewers generally agree that the jerkiness of virtually all movements creates annoying distractions. This observation is quite pivotal in the overall system/channel configuration; it indicates that beyond a certain bandwidth, additional channel capacity would only serve to irritate the viewer. Note that a 56 KHz channel (Table 2.5) provides a refresh every 1.25 seconds. This is just about the fastest update interval that can be tolerated. Any capacity beyond this should be used for time-division multiplexing groups of VFRTS channels. For instance, one real-time channel can accommodate 75 narrow-band 56 KHz channels. No alteration of any kind is required in the transmission chain because the actual signal in the channel would be identical in every way - except that sets of line pairs are extracted from different program inputs. Mixes of various refresh rates can also be accommodated in this scheme and thus some channels are near real-time and others are virtually FAX type channels, updating every few minutes.

It has been established that the useful range of frame-rate updates lies in the several second to one minute region. For most efficient transmission, analog channels should be used, requiring bandwidths from $\sim$ 60 KHz to 3 KHz, respectively. For the prototype, a 5 second refresh was chosen with a corresponding 15 KHz channel. The unit is designed however to allow any slower transmission rates to accommodate narrower transmission channels with minor filter replacements. A brief treatment of prototype operation follows.

2.1.5 PROTOTYPE CONFIGURATION

A single channel transmission system prototype was constructed to demonstrate that these concepts could be realized using video disc storage technology. Separate functions are divided into defined subsystems according to Figure 2.1 . This figure illustrates the inter-related functions of these groups for the monochrome system which was assembled and tested and demonstrated. The heart of each terminal is the Master Timing/Sync Group which provides digital reference signals for system operation. The Servo Group accepts these electronic reference signals and seeks to control the motor/disc assembly to produce uniform disc rotation synchronized to the television field. In the case of the transmit terminal (Figure 2.2), fixed video heads mounted around the periphery of the video disc write and read information from dedicated circular tracks - one head per track. The television frame is stored at the transmit terminal in the form of two sequential fields, one field per track. A standard industrial quality monochrome television camera, driven by the Timing/Sync Group, delivers video the the Mod/Demod Group which converts it to a frequency modulated carrier compatible with the disc/head transfer function. This spectrum is written upon and recovered from the disc via the magnetic heads. During read operation the FM spectrum is demodulated yielding the original video. This still frame can be displayed on a monitor and simultaneously processed for transmission by the Time Base Expander Group (TBE). The TBE receives video and parallal digital data from the Data Group. These data

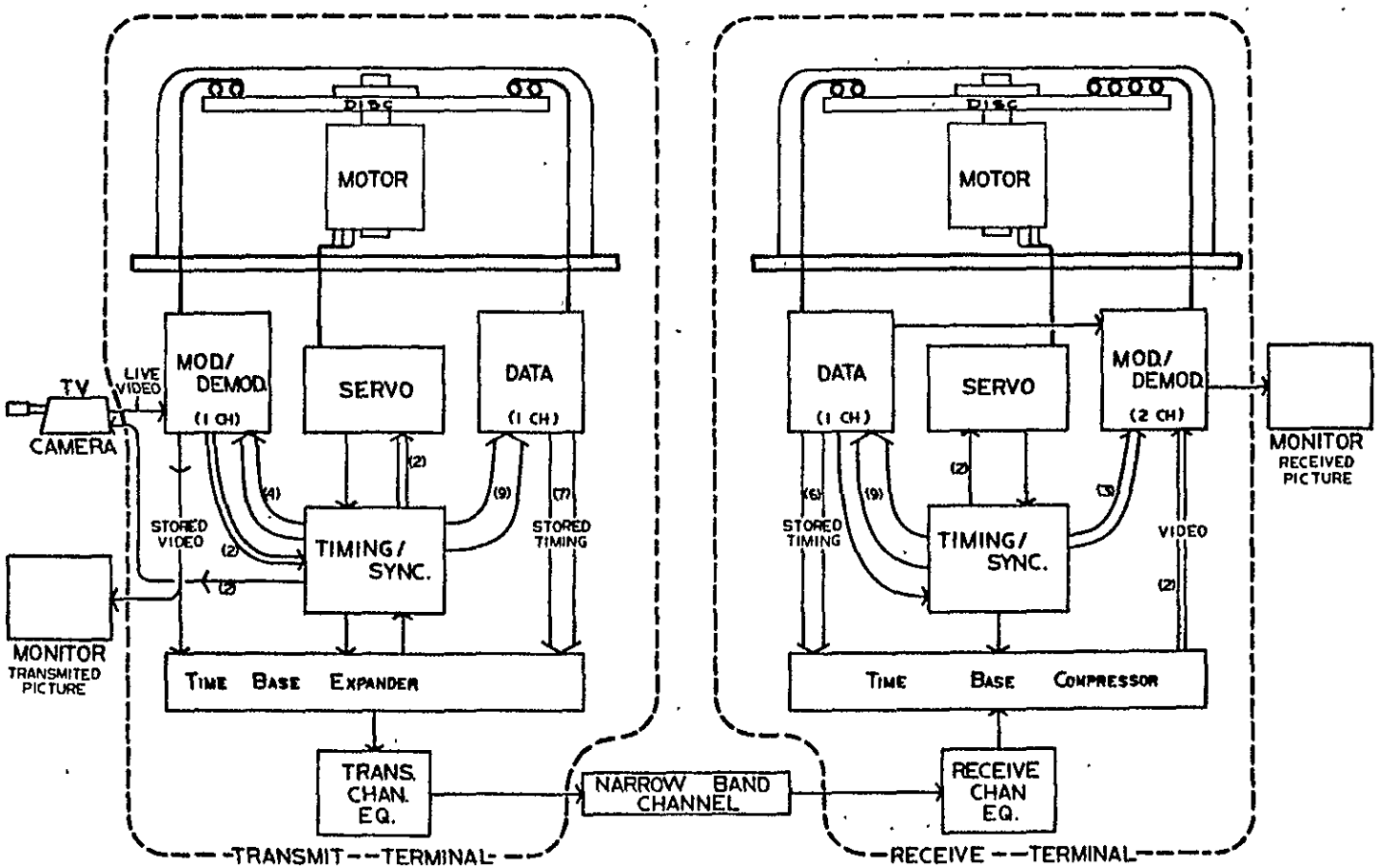


Figure 2.1. Complete VFRTS Block Diagram.

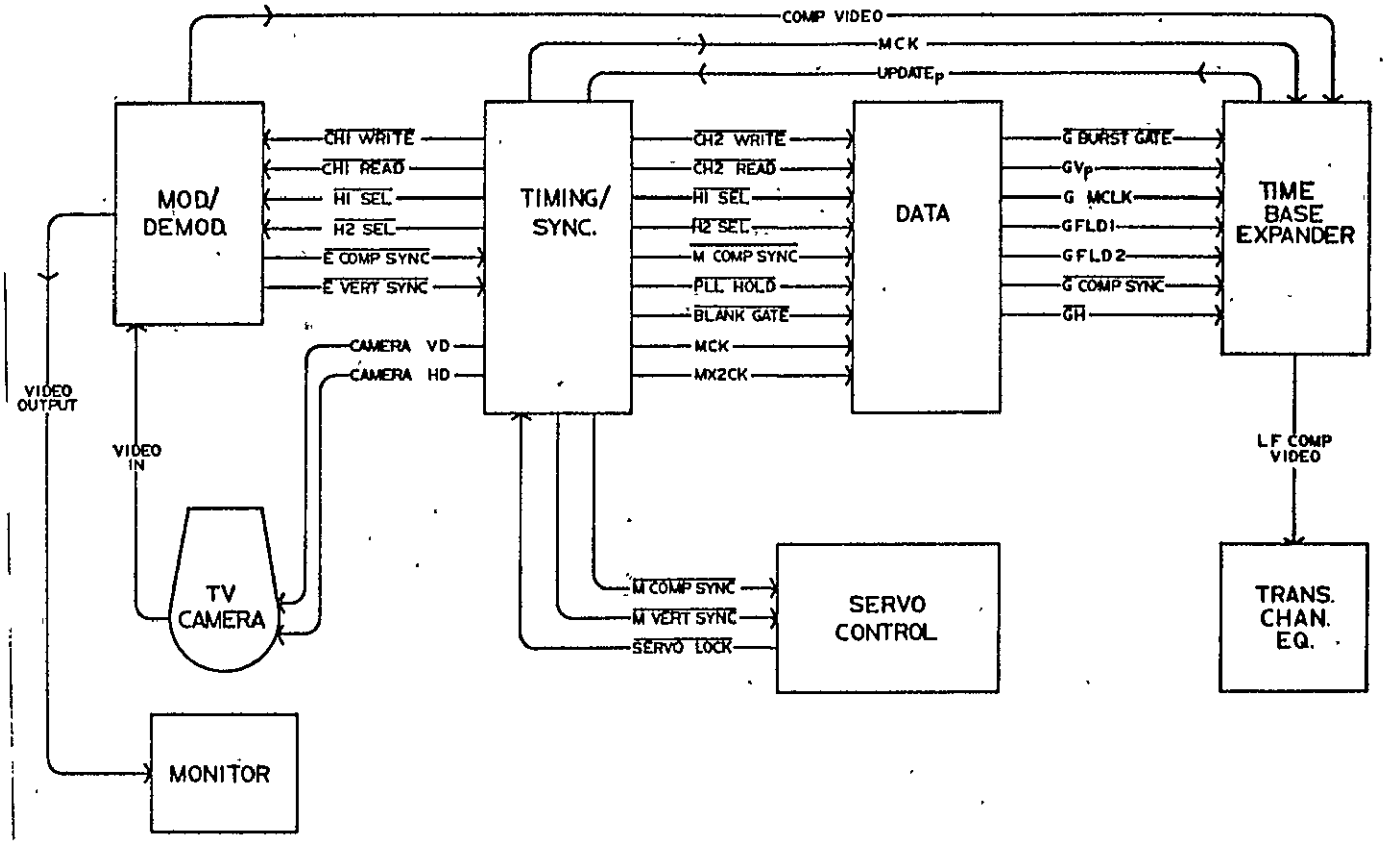


Figure 2.2. Transmit Terminal Group Block Diagram.

tracks allow precise location of lines and picture sample points within each field to be determined despite inevitable minor irregularities in disc rotational speed. A 300X expanded version of the stored analog video signal emerges from the TBE. Since the TBE is an all digital processing system, its analog output consists of a discrete "stairstep" signal exiting a sample and hold circuit. Necessary bandlimiting and channel filtering is accomplished by delay corrected filters in the Channel Equalizer Group before analog transmission.

Similar filters in the receive terminal (Figure 2.3) bandlimit the incoming low frequency video signal to remove unwanted noise introduced during transmission. The Time Base Compressor (TBC) samples active lines from the low frequency composite video and temporarily stores them in line memory. During this process, the Data Group monitors disc locations physically assigned to each video line and signals a write operation when the disc memory is in the appropriate angular position. Thus, incoming lines are transferred to the disc via timebase compression (x300) which restores original spectral content. The line-writing process continues until an entire field or frame, depending upon desired operating mode, is built up in memory. At this point the video output is switched to the most recently written picture and new data begins to be written on the undisplayed tracks. In this fasion a flicker-free display is provided to normal TV monitors.

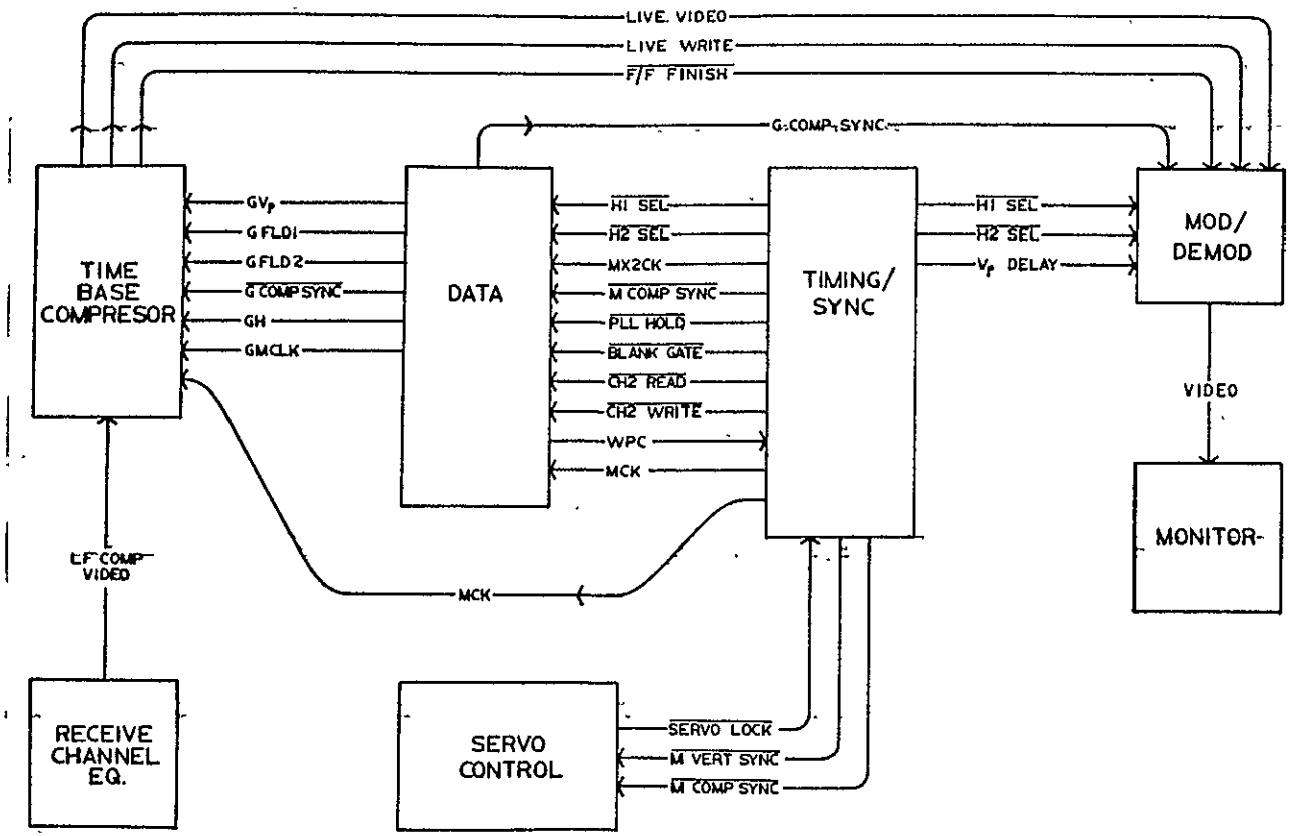


Figure 2.3. Receive Terminal Group Block Diagram.

Basic system design goals and configurations have now been established. The sections that follow will explore each major subsystem in some detail, outlining pertinent theoretical and practical design considerations. Group performance specifications will be ascertained and evaluated. The next section deals with the Master Sync/Timing Group. Subsequent sections treat the following groups: Servo, Mod/Demod, Data, TBE/TBC, and Channel Filters. An overall summary and concluding remarks will re-emphasize the primary concepts and designs; goals for the transition to full color transmission will be established.

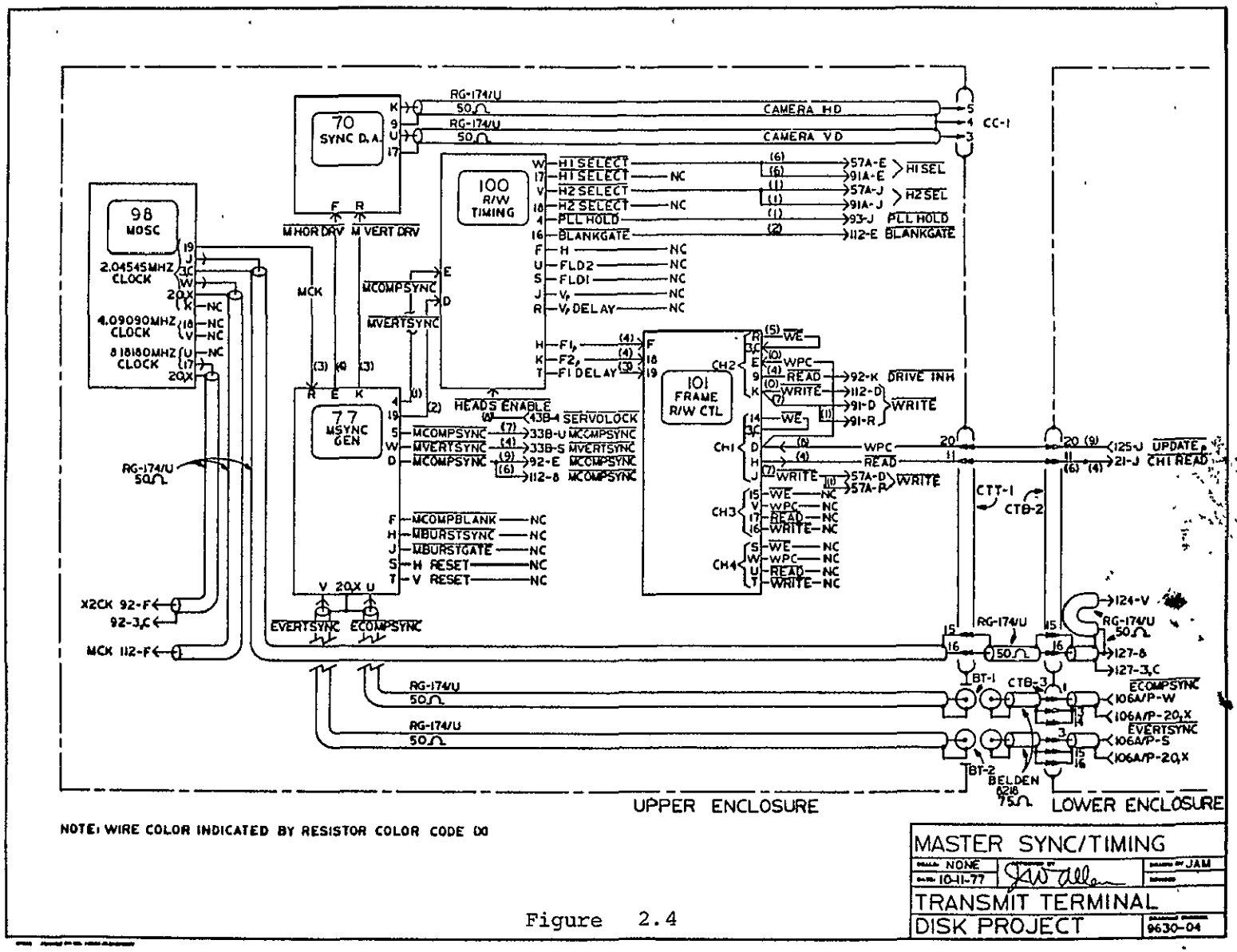
2.2 MASTER SYNC/TIMING GROUP

.2.1 INTRODUCTION

This group generates the master clocks, sync and timing signals for each terminal (see Figures 2.4 and 2,5). The crystal-controlled 16.3636 MHz oscillator on MOSC (98) serves as the reference for all subsequent signals. One clock from this card, MCK (2.04545 MHz), feeds a television sync generation chip (MM5320N) on MSYNC GEN (77); horizontal and vertical drive signals are fed directly to the transmit terminal TV camera via the SYNC D.A. (70), which raises the drive level from TTL to EIA sync standards. Composite sync is processed on the R/W TIMING (100) board, which decodes timing information within the vertical interval. The FRAME R/W CONTROL (101) contains four independent controllers that allow frame storage for an asynchronous write command; it receives vertical timing signals from (100). A block diagram of the group is shown in Figure 2.6 ; card schematics and alignment procedures are available in Appendix A2.1.

!.2.2 MOSC(98)

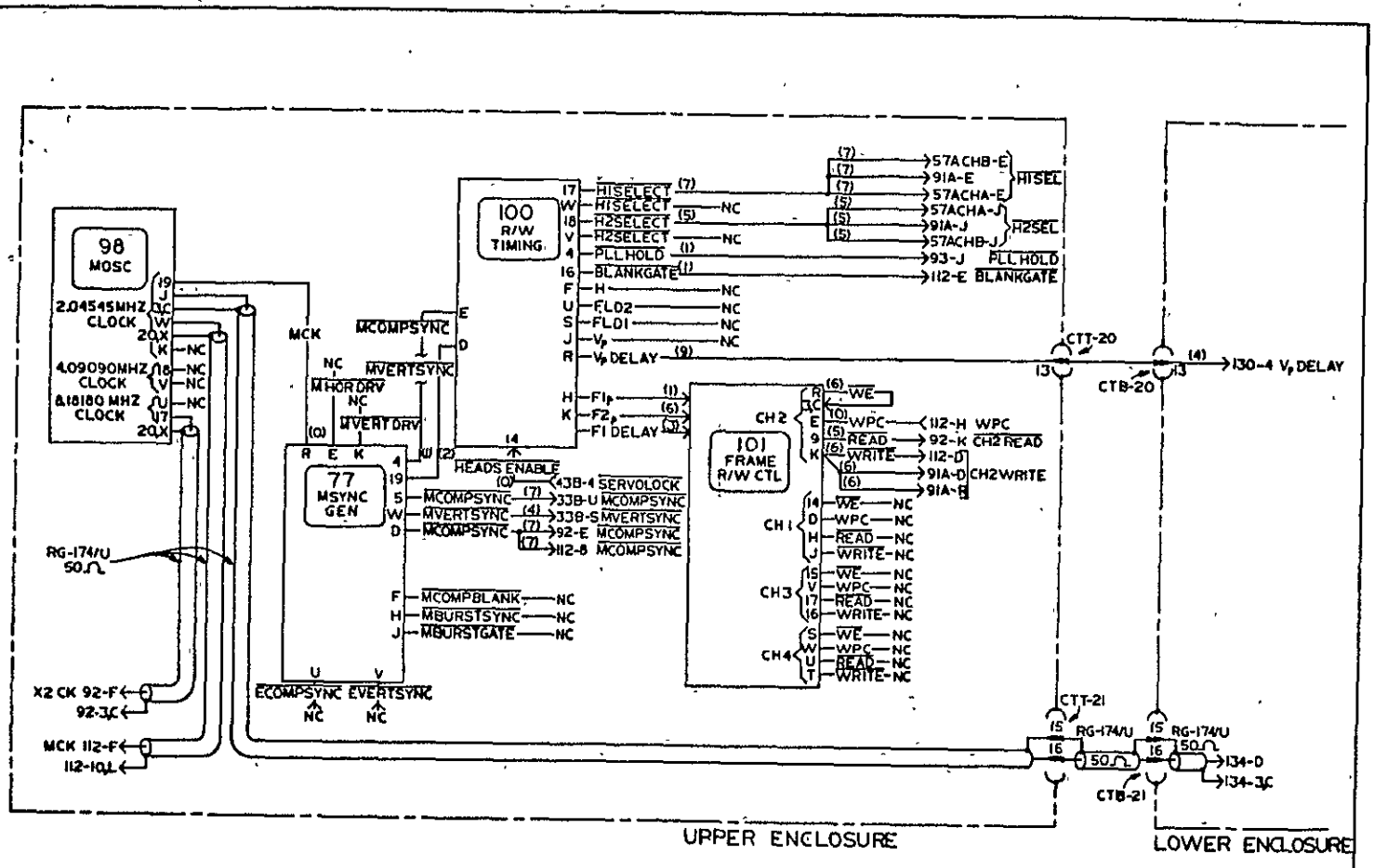
The crystal oscillator integrated circuit (MC12061P) provides a 16.3636 MHz TTL-compatible signal to a 74163N counter programmed to count from 2-9 cyclically. The Q_A, Q_B, and Q_C outputs yield square wave clocks of 8.1818 MHz, 4.0909 MHz and 2.04545 MHz respectively. Buffers are included to drive TTL and coaxial lines. Both oscillator and counter are powered by an on-card integrated circuit +5V regulator for isolation.



NOTE: WIRE COLOR INDICATED BY RESISTOR COLOR CODE DO

MASTER SYNC/TIMING
SCALE NONE
DATE 10-11-77
DRAWN BY JAM
TRANSMIT TERMINAL
DISK PROJECT
9630-04

Figure 2.4



NOTE: WIRE COLOR INDICATED BY RESISTOR COLOR CODE 00

MASTER SYNC/TIMING
RECEIVE TERMINAL
DISC PROJECT 9630-05

Figure 2.5

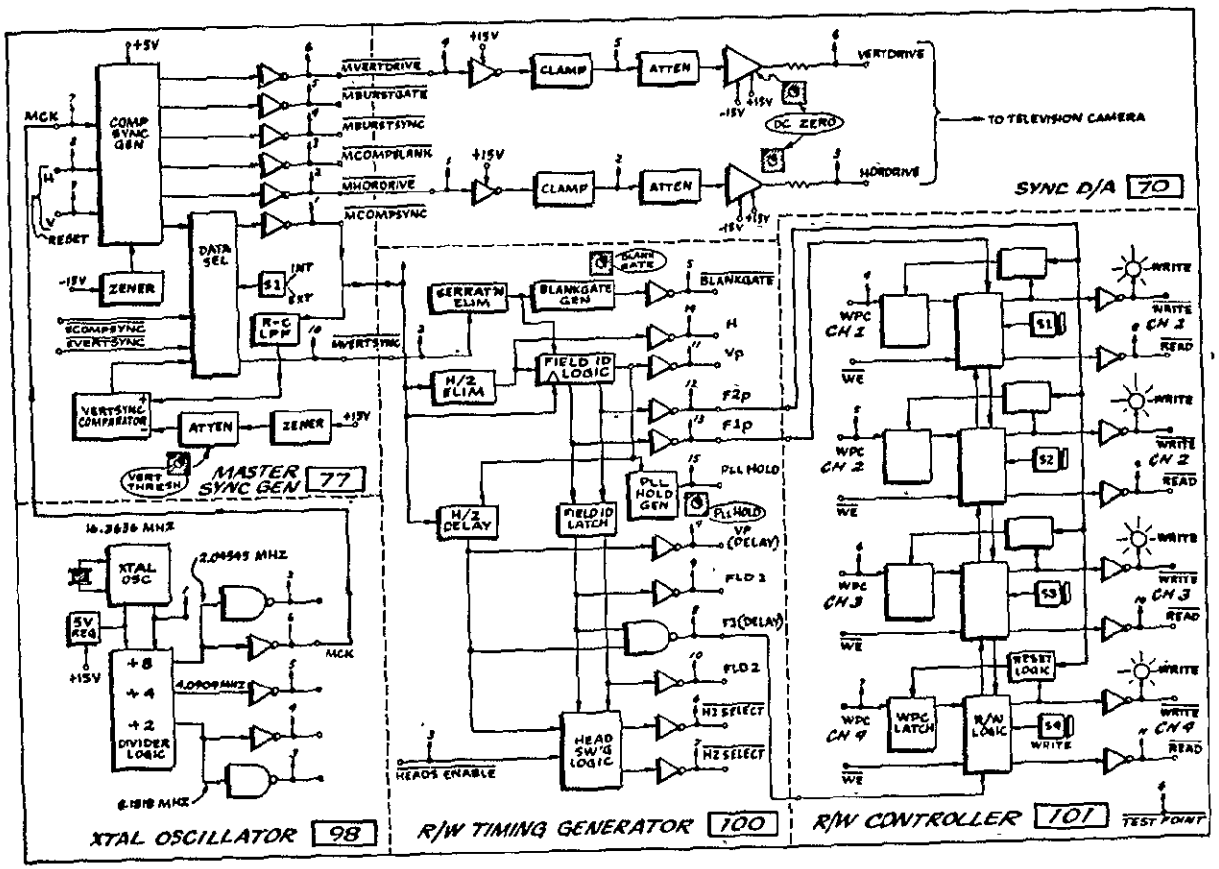


Figure 2.6. Timing/Sync Block Diagram

.2.3 MSYNC GEN (77)

The 2.04545 MHz clock feeds an integrated circuit television sync generator chip (MM5320N) which provides the following timing signals:

1) $\overline{\text{MCOMPSYNC}}$
2) $\overline{\text{MCOMPBLANK}}$
3) $\overline{\text{MBURSTGATE}}$
4) $\overline{\text{MBURSTSYNC}}$
5) $\overline{\text{MHORDRIVE}}$
6) $\overline{\text{MVERTDRIVE}}$

All signals conform to the required color timing standards prescribed by NTSC specifications (see Figure 2.7). $\overline{\text{MCOMPSYNC}}$ is processed to yield the vertical timing signal $\overline{\text{MVERTSYNC}}$; timing relations are illustrated for field 1 vertical interval in Figure 2.8 , lines 1 and 3 respectively. A data selector enables these signals to be distributed to the system either from the sync chip or from an external source, such as the PROC AMP (106 A/P) (see Mod/Demod group). In this fashion timing for the disc servo can be referenced to an incoming composite video signal, such as a test generator, for check-out and alignment.

2.2.4 SYNC D.A. (70)

The sync distribution amplifier drives the camera vertical and horizontal deflection systems with a 4 Vpp negative-going signal at 75Ω. TTL sources from MSYNC GEN (77) are inverted and passively

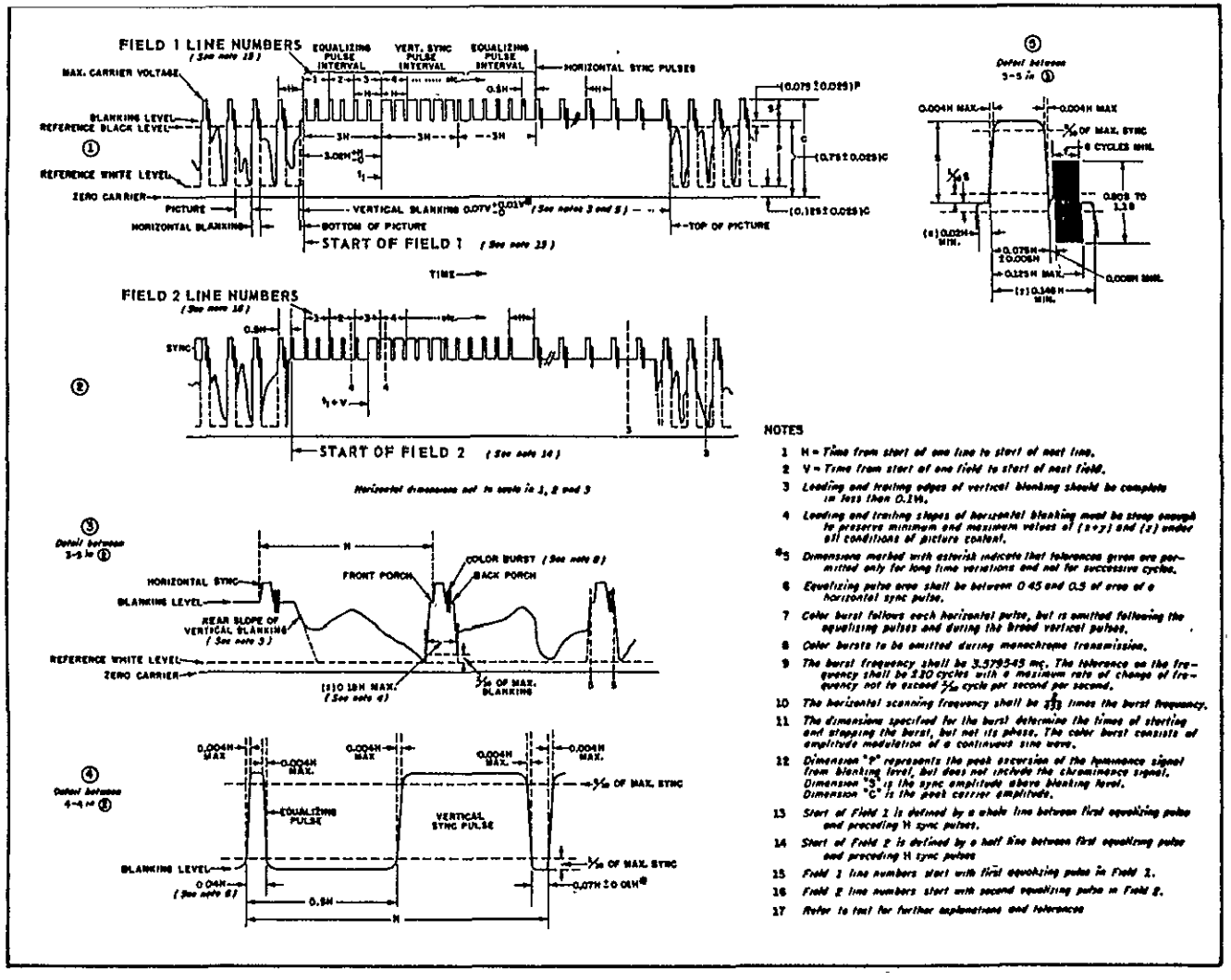


Figure 2.7 . EIA-RS-180A Television Standards

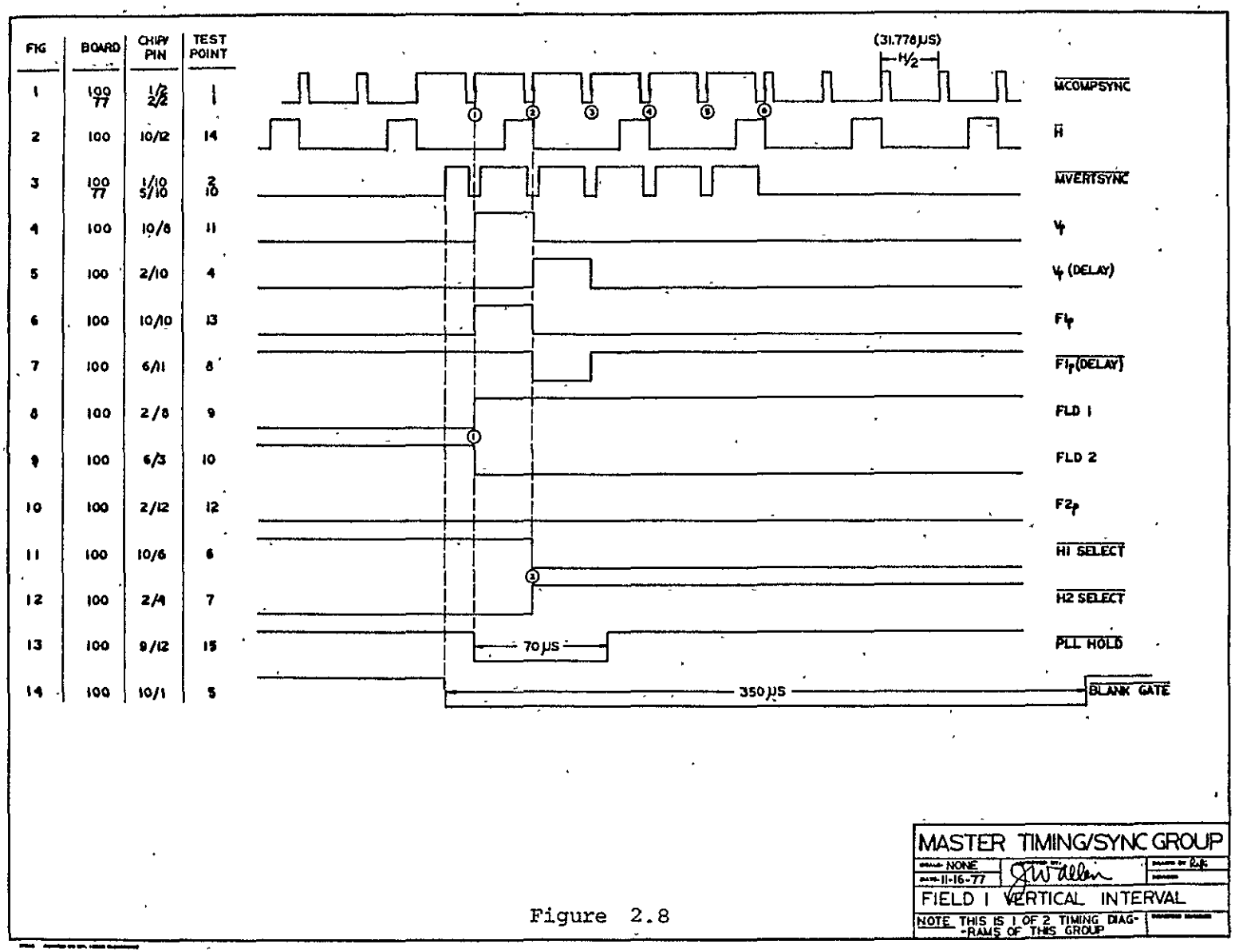


FIG
BOARD
CHIP PIN
TEST POINT
1 100/77 1/2 2/2 1
2 100 10/12 14
3 100/77 1/10 5/10 2 10
4 100 10/8 11
5 100 2/10 4
6 100 10/10 13
7 100 6/11 8
8 100 2/8 9
9 100 6/3 10
10 100 2/12 12
11 100 10/6 6
12 100 2/4 7
13 100 9/12 15
14 100 10/1 5
(31.778μS)
H/2
MCOMPSYNC
H
MVERTSYNC
Ψf
Ψf (DELAY)
F1f
F1f(DELAY)
FLD 1
FLD 2
F2f
H1 SELECT
H2 SELECT
PLL HOLD
BLANK GATE
70μS
350μS
MASTER TIMING/SYNC GROUP
NONE
11-16-77
FIELD 1 VERTICAL INTERVAL
NOTE THIS IS 1 OF 2 TIMING DIAGRAMS OF THIS GROUP

Figure 2.8

clamped; the most positive portion of the waveform is ground referenced by the clamp diode. A video buffer amplifier on each channel provides output gain and impedance matching to 75Ω coaxial cables.

2.2.5 R/W TIMING GEN (100)

Vertical interval timing and control signals are generated on (100); refer to Figures 2.6,2.8. $\overline{\text{MVERTSYNC}}$ is passed through a serration eliminator and blank gate generator. $\overline{\text{BLANKGATE}}$ (Fig. 2.8 line 14) is used to control data selection in the Data Group. $\overline{\text{MCOMPSYNC}}$, H, $\overline{\text{H}}$ and the processed $\overline{\text{MVERTSYNC}}$ feed the field I.D. logic, which generates positive-going H/2 duration pulses F1_p and F2_p at the beginning of each field between serration 1 and 2. These toggle a latch to provide FLD1 and FLD2 high-true signals. Head select (head switching command) lines are triggered at the beginning of the second serration, approximate 32 μsec later.

Phase-locked loops are used in both the Data Group and TBE for clock recovery; during head switching the input signal is temporarily disconnected. To prevent the PLL from wandering far from the correct frequency, a $\overline{\text{PLLHOLD}}$ command (Figure 2,8;13) is generated.

2.2.6 FRAME R/W CTL (101)

All four channels on 101 are identical. A negative-going write pulse command ($\overline{\text{WPC}}$) is routed to a latch which holds the state for inspection at the beginning of field one. The R/W logic switches the output lines from read to write at the beginning of the 3rd serration (see Fig. 2.8, 2.9). Write lines remain high for two

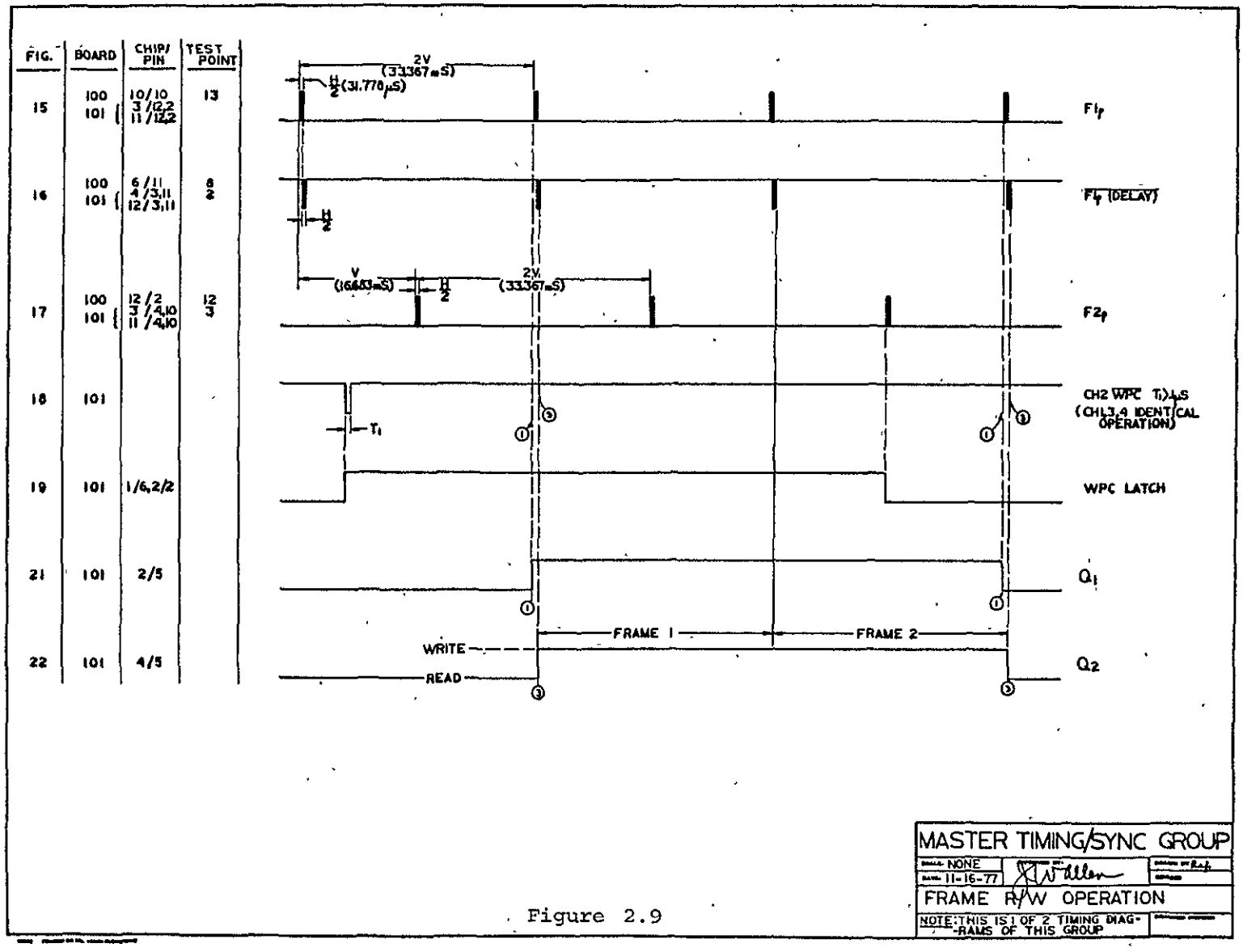


FIG.
BOARD
CHIP/ PIN
TEST POINT
15
100
101
10/10
3/12,2
11/12,2
13
16
100
101
6/11
4/3,11
12/3,11
8
2
17
100
101
12/2
3/4,10
11/4,10
12
3
18
101
19
101
1/6,2/2
21
101
2/5
22
101
4/5
2V (33367 mS)
H/2 (31.778 μS)
F1f
F1f (DELAY)
V (16683 mS)
H/2
2V (33367 mS)
F2f
CH2 WPC T1 ±1 μS (CH1,3,4 IDENTICAL OPERATION)
T1
WPC LATCH
Q1
FRAME 1
FRAME 2
WRITE
READ
Q2
MASTER TIMING/SYNC GROUP
NONE
11-16-77
FRAME R/W OPERATION
NOTE: THIS IS 1 OF 2 TIMING DIAGRAMS OF THIS GROUP

Figure 2.9

consecutive frames; the double-write process insures complete erasure of the previous picture from the disc tracks. An over-ride pushbutton allows manual writing; if the button is latched down, recording takes place continually until it is released. During the record process, the output display monitor shows the live video signal, as the demod sub-group is connected directly to the modulated RF signal supplied to the video heads. This live mode of operation is termed "E-to-E" and allows frames to be recorded without an annoying flash on the transmit monitor during frame storage.

2.3 SYSTEM DESIGN: SERVO GROUP

2.3.1 Preliminary Remarks

It has been established that a rotating magnetic video disc exhibits many desirable qualities for television image storage. The actual signal for one field is written via a tiny magnetic head which floats on an air cushion of 8-10 μinches at a fixed radius. The resulting circular track contains magnetic flux transitions which when sensed later by the same head reproduce the original image. In order to accomplish this, the disc must rotate such that it completes exactly one revolution for each television field of incoming video. Thus a separate electronic system must provide control signals to the motor which constantly maintain this absolute timing relationship. A flow diagram (Figure 2.10) illustrates the actual algorithm and system monitoring necessary to achieve suitable disc control. Subsequent sections of this chapter will explore the theoretical difficulties and demonstrate the rationale for various design decisions.

2.3.2 Principle Design Difficulties

The most difficult problem to overcome in the use of a rotating magnetic disc for video buffer memory applications is the unavoidable timebase instability due to the rotating mechanical system. This is reflected in the reproduced television signal as loss of syn-

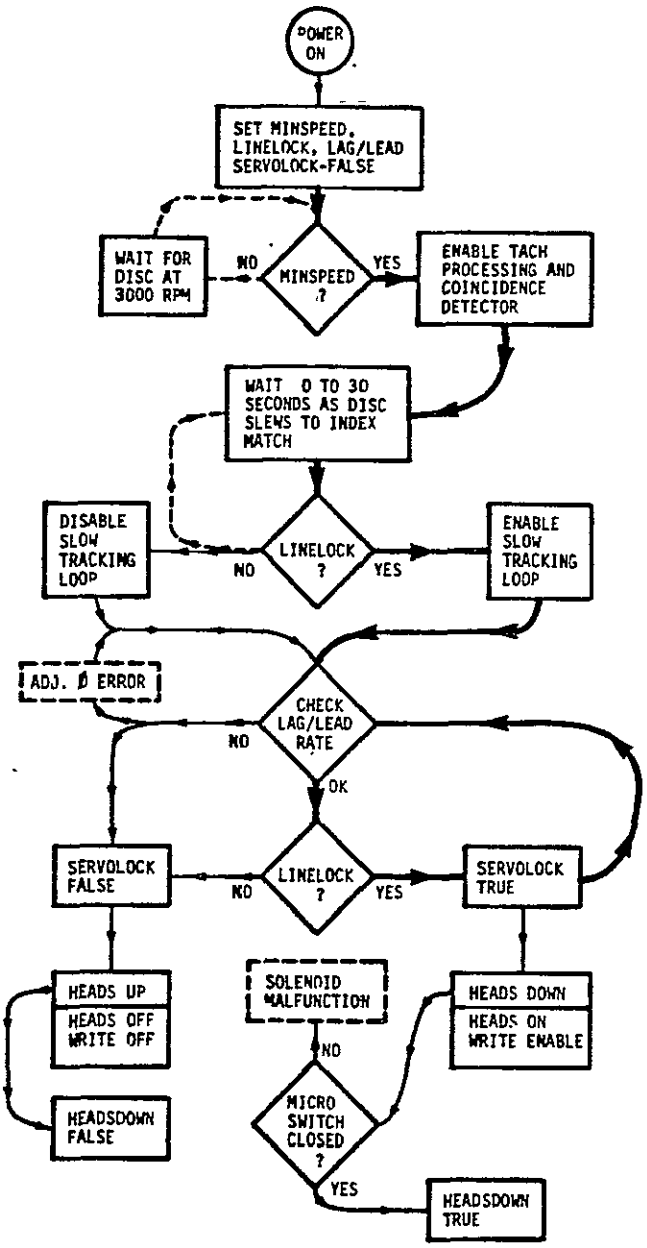


Figure 2.10 Video Disc Servo Control Algorithm.

chronization and image tearing. Since one often requires switching between "stored" and "live" channels, the timebases of the two signals should be matched sufficiently so that no erroneous synchronizing information is produced during switching.

Since we must not misidentify any of the synchronizing pulses, the required stability is determined by the narrowest pulses present in composite sync, the $\sim$ 2 μsec wide equalizing pulses, which precede and follow the vertical interval.[1] We are led to conclude that stabilities on the order of < 1 μsec per revolution would be adequate to assure "glitch-free" switching to and from the stored image. As an upper limit, it is also recognized that deviation exceeding one-half of an active line time (or $\sim$ 34 μsec) would be intolerable because an entire line of sync could be lost.

Large discs (> 12" dia) often employ synchronous motor drive to achieve constant RPM; the associated large moment of intertia ($\alpha(\text{dia})^4$) assures adequate timebase stability. Small discs (4-7"dia), however, can exhibit $\pm$ 20 μsec deviation or more when driven in this fashion - some form of feedback servo control is necessary in this case. The design of such a system usually employs a two-track glass substrate optical tachometer disc and sensor mounted on the disc drive which provides: 1) a high-frequency (10-50 KHz) signal proportional to disc speed and 2) a low frequency position index to allow precise matching of the stored and live picture signals. The high frequency feedback signal is locked to the desired reference horizontal line rate stripped from composite sync via closed loop

control of the dc-servo motor; a phase-locked loop (PLL) is ideally suited for this application. The following sections will cover the mechanical and electrical design concepts employed in achieving a low-cost, compact servo drive.

2.3.3 Disc Platform Mechanical Design

In the present work an aluminum substrate disc 0.2" thick and 6.5" in diameter was adopted for storage of 4 MHz bandwidth television signals; it is both capable of the required performance and cost effective. Design and fabrication specifications are given in Appendix 2.2 . To provide required disc/head velocities of > 1000 i.p.s., the disc is rotated at the television field rate (approx. 3600 RPM); hence, one field is recorded per revolution.

A brushless dc motor was chosen for the disc drive, primarily because of its linear torque-current characteristic and RFI free operation. The motor's rotating magnetic field is produced by a electronic commutator circuit which sequentially switches current to the four field windings. Motor dimensional drawings, detailed mechanical and electrical specifications and electronic commutator description are exhibited in Appendix 2.3.

During operation the video heads do not actually touch the disc surface, they are intended to "fly" 5-10 μin. over the magnetic coating. Consequently, wobble at the disc periphery must be held below $0.001"^2$ to avoid head "crashes" or contact with the surface. The disc drive spindle assembly serve to attach both the magnetic and

optical discs to the motor shaft, whose ball bearings support the entire mechanism. This direct drive assembly is shown in Figure 2.11 in section view. To achieve the required disc runout tolerance, final spindle machining (Figure 2.11, part 2) is performed with the piece mounted on and driven by the motor itself. This technique regularly produces a runout error (wobble) of less than .0001"/1" or ∿ .0003" total indicated runout (T.I.R.) at the disc edge.

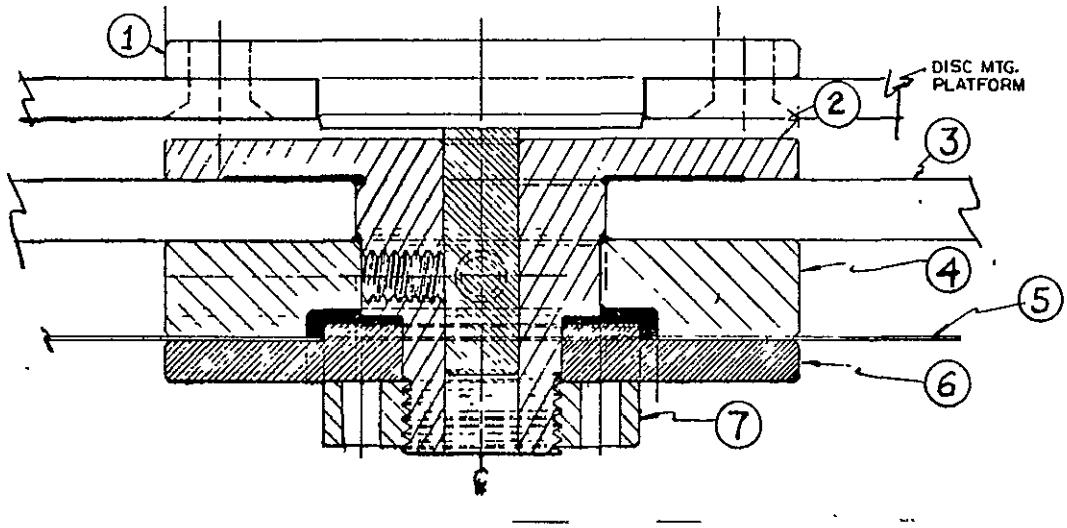


Figure 2.11 - Disc Drive Spindle Section View

1) motor
2) spindle
3) video disc
4) spacer
5) optical tach disc
6) washer
7) nut.

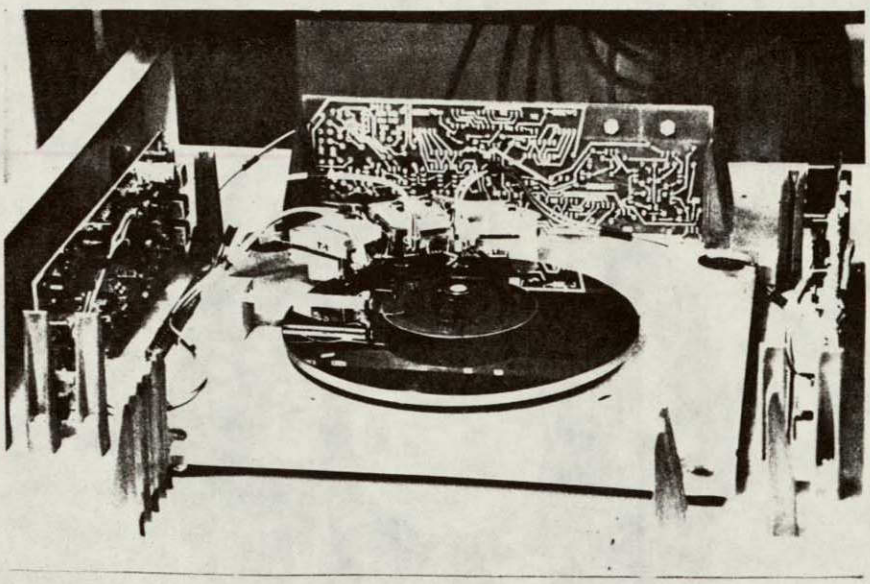
The motor flange bolts to a 10" square aluminum plate, shock mounted at the corners to isolate mechanical vibrations to the instument and to reduce the effect of external disturbances on the disc drive. Top and bottom photographs of the complete platform assembly are shown in Figure 2.12.

To reduce the complexity and expense of the usual twin-track glass optical tachometer system, an inexpensive 525 line plastic tach disc is used instead.* One transparent section is made opaque and this section is detected electronically to provide disc position information (Figure 2.13). Thus a single composite timing track serves the purpose of providing both disc speed and absolute position. Only a single tach sensor is required, eliminating the mechanical and electrical difficulties and costs associated with completely separate timing tracks.

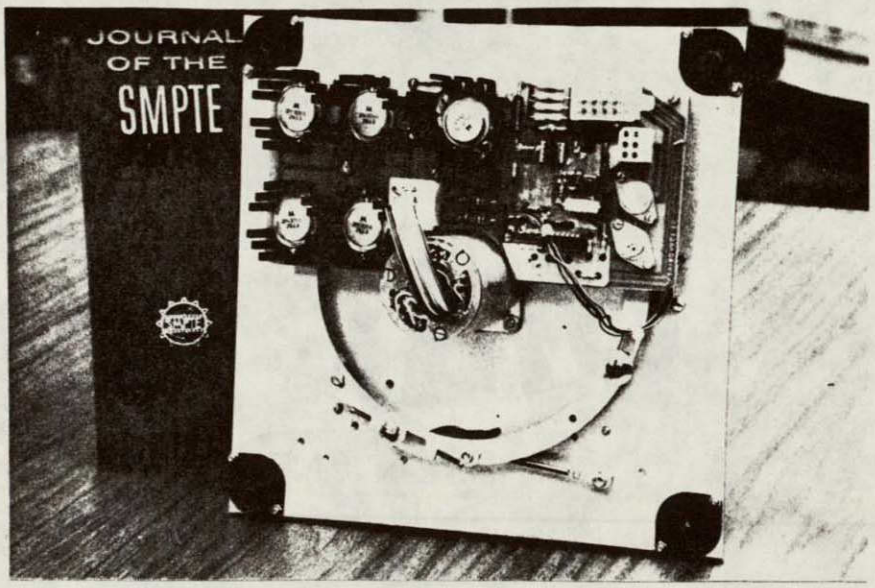
The tach sensor consists of a small lamp-photocell assembly; the lamp is operated at reduced voltage for extended life ($\sim 10^5$ hrs). As the tach rulings pass through a slot between the light source and photocell, an approximately sinusoidal voltage is produced proportional to the amount of illumination reaching the photocell. The sensor is mounted over the video disc on an extension arm which can

---

*Dynapar Corporation, 1675 Delany Rd., Gurnee, Ill. 60031. The 525 lines correspond to the number of lines in a U.S. television frame. If European CCIR specifications were required, a 625 line tach could be easily substituted, with slight servo-control time constant modifications.



Top View



Bottom View

Figure 2.12 Top and Bottom Views of Disc Platform Assembly

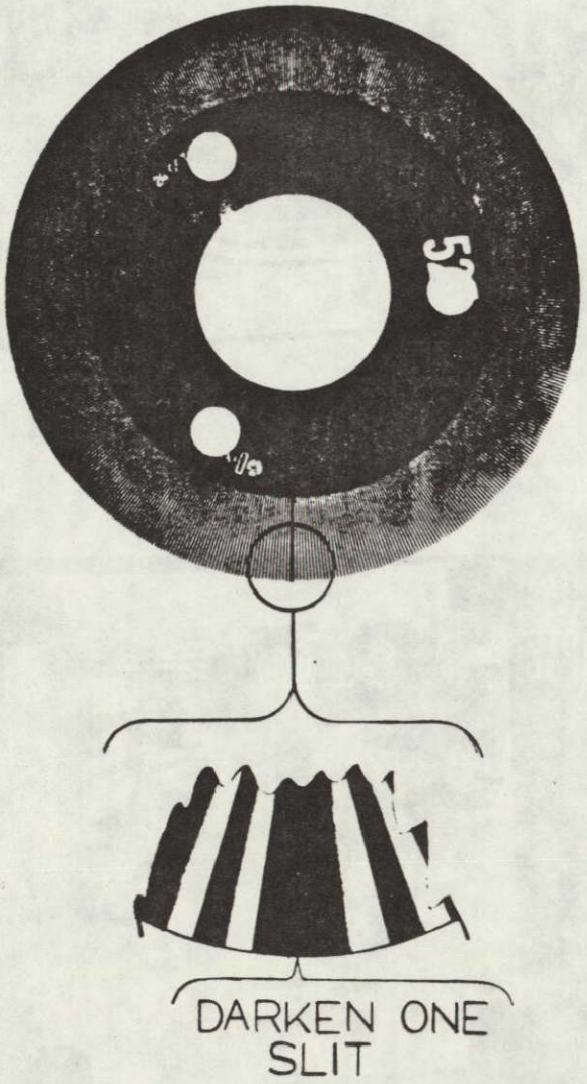


Figure 2.13 Optical Tachometer Disc.

the vertical interval of the composite TV reference; it further provides long term drift correction for changes in high frequency loop gain due to variations in components and environmental conditions such as temperature, air-loading of the disc, bearing wear, etc.

Two innovations employed by the designer provide the most constant possible drive torque to the disc assembly - 1) 180° field commutation and 2) constant current drive. If the four field windings are switched in sequence, one refers to this as 90° communtation; the resulting torque as a function of rotor position as shown in Figure 2.15. The pulsed nature of the torque is

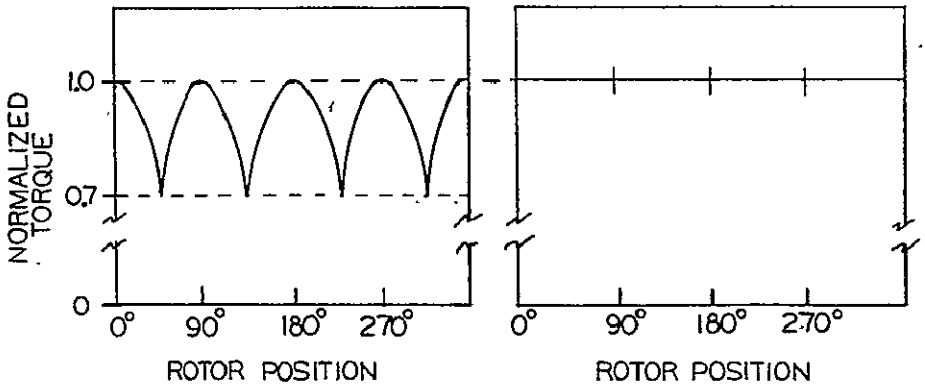


Figure 2.15 a) 90° winding commutation

b) 180° winding commutation

a typical feature of finite-pole dc machines and is termed "cogging". Often times, commercial disc drives use servo motors with printed rotors having hundreds of separate poles to reduce the torque ripple proportionately. The electronically commutated dc motor, however, offers an option of 180" commutation providing almost constant torque to the load (as shown in Figure 2.15b). The only departures from

this flat torque profile are due to non-linearities of the Hall-effect sensors and drive transistors (Appendix 2.3 contains an analysis of the 180° commutator circuit). These slight remaining variations can be reduced still further by controlling the motor drive current - since torque is linearly related to winding current for a dc machine. This combination of drive techniques makes the four-pole motor appear to have a virtually infinite number of poles and a smooth torque profile.

2.3.5 High Frequency Servo Loop Model

Figure 2.16 below is a block diagram of a conventional PLL motor controller. The motor transfer function is derived in Appendix 2.4 . Straightforward analysis yields the open loop transfer function.

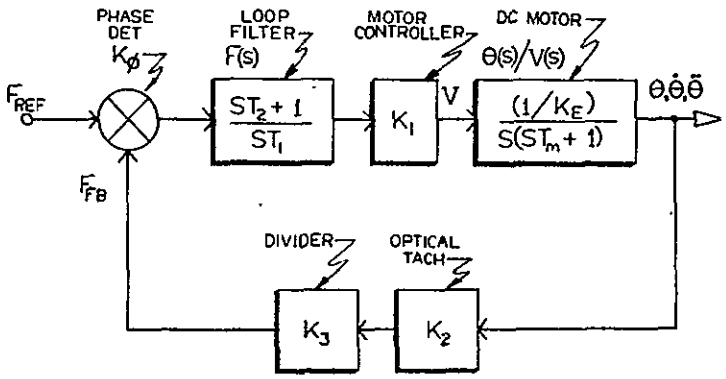


Figure 2.16 High Frequency Servo Loop

$$\text{O.L.T.F.} = K_o \left(\frac{s\tau_2 + 1}{s^2(s\tau_m + 1)} \right) \qquad (2.1)$$

$$\text{with} \qquad K_o = \frac{K_0 K_1 K_2 K_3}{K_E \tau_1} \tag{2.1a}$$

It is worthwhile to notice that when driven by a control voltage, the motor contributes a pole at:

$$\omega_m = \frac{1}{\tau_m} = \left(\frac{K_E K_T}{R \Sigma J} \right) \tag{2.2}$$

K_E = motor back EMF constant (volts/rad/sec)

K_T = motor torque constant ($Kg \cdot m^2/amp \cdot sec^2$)

R = rotor winding resistance (Ω)

ΣJ = total moment of inertia of rotor and load ($Kg \cdot m^2$)

In Appendix 2.4 , Section A, ω_m is calculated to be:

$$\omega_m = 0.385 \ \frac{rad}{sec} \tag{2.2a}$$

It is in this respect that a motor-control PLL differs from an all electric PLL - the motor can be thought of as a VCO with a preceeding low pass filter whose cutoff frequency is determined by the mechanical time constant, τ_m.

Because the order of the PLL is three, a root locus evaluation is desirable to observe stability and loop dynamics as a function of loop gain, K_o. Solving for the roots of the characteristic equation

for various values of loop gain yields the so-called root locus, whose roots "follow a locus" from the poles to the zeroes of the open loop transfer function. In this case we have three poles and three zeroes; two poles at the origin and one at $-\frac{1}{\tau_m}$, one zero at $-\frac{1}{\tau_2}$ and two at infinity. For the sake of illustration, choosing $\tau_2 = 10\tau_m$ we get the locus shown in Figure 2.17a. Notice that the two roots from the origin follow the closed circle, forming for a certain range of K_o, a dominant complex pole pair as shown in 2.17b. This low gain value yields good filtering but narrow bandwidth - consequently slow acquisition. If the loop gain is increased to a higher value, a second complex pole pair is formed (note same damping radial) influenced by the simple root on the negative real axis as shown in 2.17c. This configuration exhibits wider bandwidth, faster acquisition and poorer filtering qualities. Thus it can be seen that two distinct "regions" of operation can be had, depending upon the loop gain.

It is of further benefit to note the effect of moving the filter zero closer to the motor pole. If we choose $\tau_2 = 6\tau_m$, the locus of Figure 2.17c results. Now the circle opens and joins the asymptote without ever returning to the negative real axis. This particular form has some advantages relative to the previous one - it exhibits wider bandwidth for the same loop gains and has a region of optimum performance determined by the relative influence of the simple pole proceeding toward the jω axis with increasing gain. Figure 2.17 , parts d and e illustrate two extremes of this behavior.

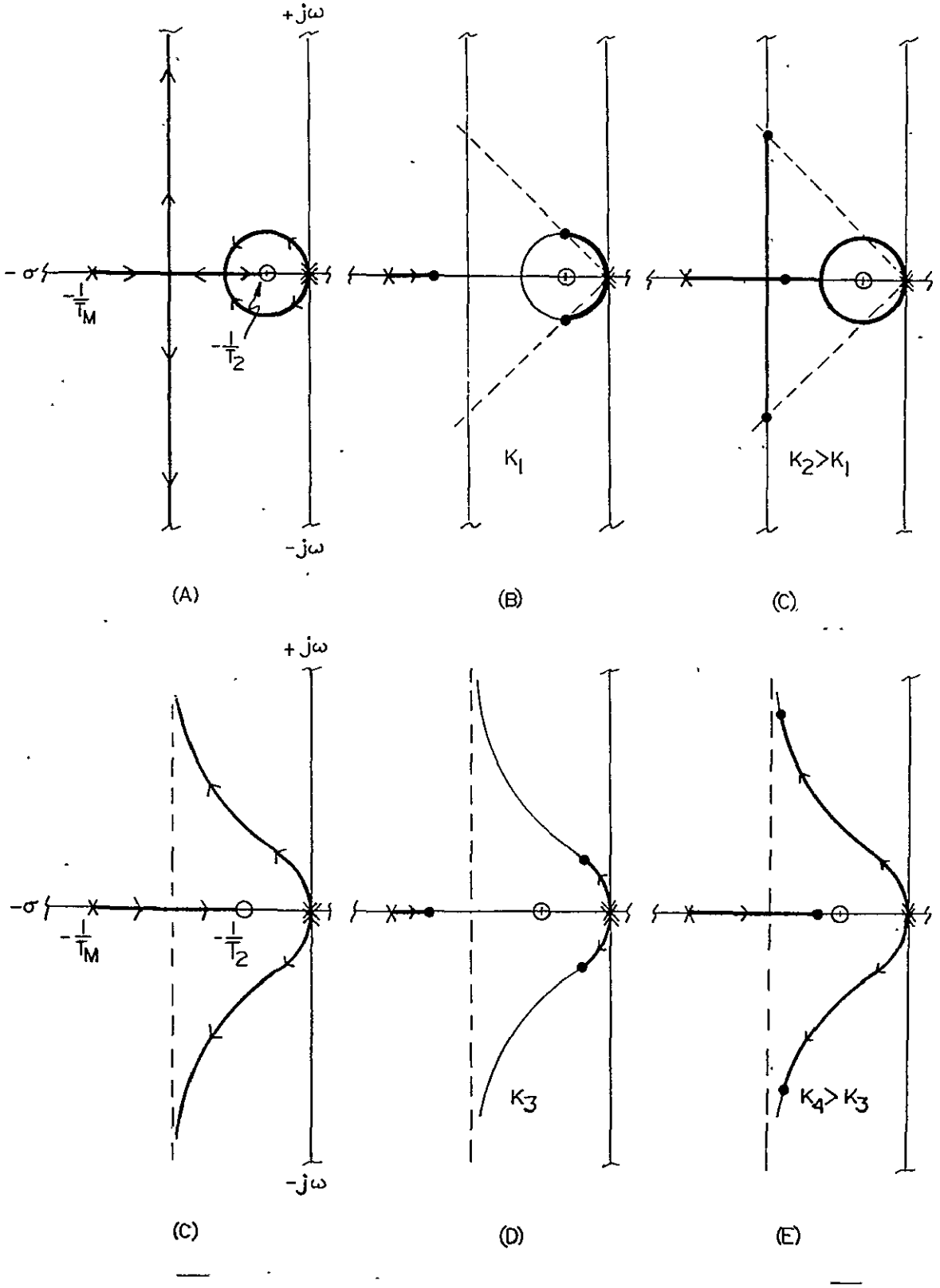


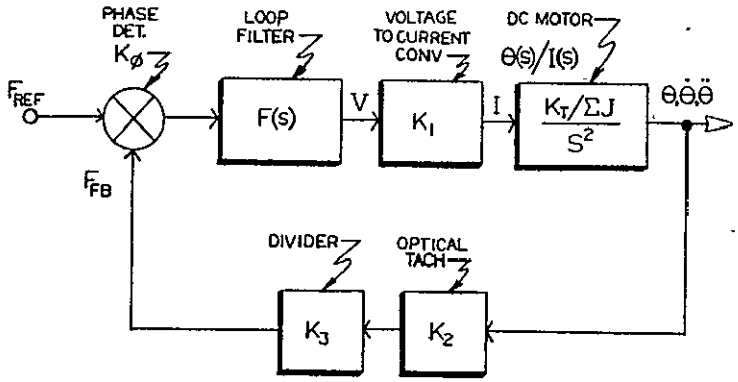
Figure 2.17 Various root loci.

Finally, it can be seen that for some regions of gain, the roots will lie on a portion of the locus proceeding radially outward from the origin - hence for some range of loop gains, the damping constant for the complex pole pair remains virtually unchanged - only ω_m changes. Thus the "form" of the loop dynamics can be held within tight tolerances relative to loop gain variations. It will later be shown that both qualities occur in the same region of the locus.

It has been mentioned before, however, that a more desirable motor control parameter is the winding current, rather than the drive voltage. The motor current transfer function is derived in Appendix 2.4 Section B and the associated servo block diagram is shown below in Figure 2.18.

The open loop transfer function for this configuration is:

$$O.L.T.F. = \left(\frac{K_0 K_1 K_2 K_3 K_T}{\Sigma J} \right) \frac{F(s)}{s^2} \qquad (2.3)$$



HIGH FREQUENCY SERVO LOOP

Figure 2.18

If we choose F(s) to have the form of a lead network (Eq. 2.4),

$$F(s) = K_4 \left[\frac{\tau_2 s+1}{\tau_1 s+1} \right] \doteq \bar{K} \left[\frac{s + \omega_2}{s + \omega_1} \right] \qquad (2.4)$$

the two O.L.T.F.'s have identical forms (same root locus) with some significant changes in parameters. Note that $(K_T/\Sigma J)$ for the current-controlled motor is lumped into the loop gain and that τ_m has been replaced by τ_1. This is a great advantage because we have complete control of τ_1 and τ_2 in the loop filter since they are determined by passive electronic components. Variations in motor parameters and motor loading are now contained in the loop gain - so all system variation will be exhibited in this parameter. By choosing the operating point appropriately on locus C of Figure 2.17, the loop dynamics are relatively unaffected by gain variations.

2.3.6 Choosing Parameters for Maximum Closed Loop Bandwidth.

The disc servo should exhibit the maximum bandwidth possible to "track out" disturbances introduced within the loop due to bearing anomalies, loading variations, etc. In order to optimize the design, the effect of the real pole upon the complex pole-pair of the closed loop transfer function must be considered; fortunately, the situation is simple enough to be treated without extensive analysis. Figure 2.19 illustrates the effect of the pole at $s = -p_r$ on the complex pole; both normalized risetime and % over-shoot are considered. If we constrain $\zeta \tilde{=} 0.7$ it can be seen that for

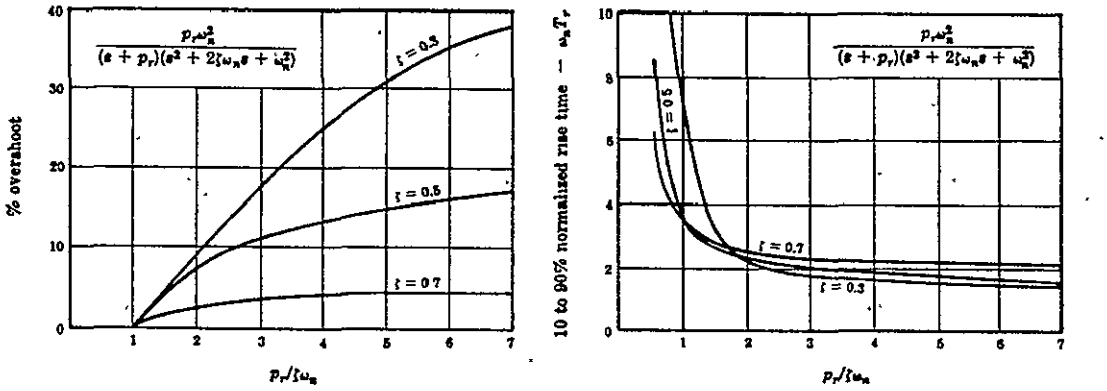


Figure 2.19 Effect of Real Root upon Complex Pole Pair.

$\frac{p_r}{\zeta\omega_n} \geq 2$, there is no significant effect upon loop dynamics, thus the real pole can approach the projection of the complex pole pair as shown in Figure 2.20 below without significant reduction in bandwidth.

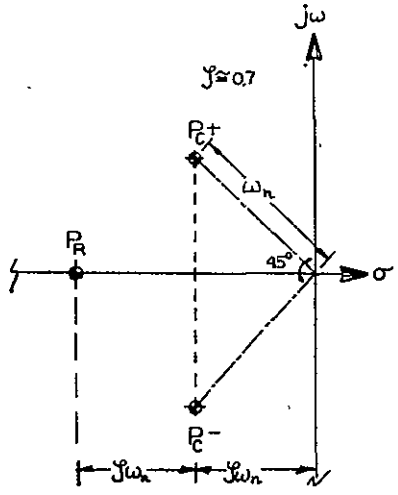


Figure 2.20 Optimum Root Placement.

The choice of controller open loop zero and pole locations is now purely a function of lead network design, given that we wish $\omega_{pole} = 6\omega_{zero}$ to yield our desired root locus. In principle, the only limiting factor on loop bandwidth is the point at which the magnetic flux within the motor ceases to increase linearly with rotor current, i.e., the magnetics begin to saturate, and K_T drops - lowering loop gain. In practice, however, it is found that non-uniformity of the optical tach rulings creates a control frequency whose instantaneous value is a function of rotor angle. For constant reference frequency, the disc rotating frequency, $\dot{\theta}$, is really a function of disc angle and can be expressed as:

$$\dot{\theta} = \dot{\theta}(2n\pi + \theta),\ n \in 1\text{, where n is a positive integer} \qquad (2.5)$$

It might first be thought that this induced rotational variance would have a disastrous effect on video luminance linearity, as the modulation process is FM. In fact, all that is required is that Eq. (2.5) holds , namely that this variation be constant for each revolution. In this fashion the signal is reproduced just as it was recorded and the speed variation is self-cancelling.

Since the optical tach disc is inexpensive, it exhibits greater ruling non-uniformities than the etched glass versions, hence, it is the dynamic range of induced control current variations which determines the upper limit on loop bandwidth if we wish the motor current to flow for a full revolution. It was found experimentally that

the maximum frequency for the controller zero was approximately 20 rad/sec to meet this criterion. The actual values used in the controller were:

$$\omega_1 = \omega_{pole} = 105 \text{ rad/sec} \tag{2.6a}$$

$$\omega_2 = \omega_{zero} = 19.25 \text{ rad/sec} \tag{2.6b}$$

The lead network can now be expressed as

$$F(s) = K_F \left(\frac{s + 19.25}{s + 105} \right) \tag{2.7}$$

where K_F is determined by the actual circuitry. It should be noted that the zero is located 19.25/0.385 = 50 times farther out on the negative real axis for the current controlled loop, a bandwidth improvement of 50. Larger bandwidths can be had by increasing the precision of the tach rulings at the price of increased expense and complexity of the tach system.

2.3.7 Root Locus Analysis

$$\text{O.L.T.F.} = \frac{K_o(s + 19.25)}{s^3 + 105\, s^2} \tag{2.8}$$

zero @ 19.25 rad/sec, ∞,∞

poles @ 105 rad/sec, 0,0

K_o = Total Loop Gain

TABLE 2.6

Roots of Characteristic Equation

K_o	p_r	Re $\{p_c^+\}$	Im $\{p_c^+\}$
100	- 104.22	- 0.39115	4.2799
500	- 100.99	- 2.0036	9.5546
1000	- 96.719	- 4.1407	13.486
2000	- 87.115	- 8.9425	19.026
4000	- 59.538	-22.730	27.867
6000	- 31.259	-36.876	48.327
8000	- 25.870	-39.565	66.238
4300	- 53.579	-25.710	29.730
4500	- 49.406	-27.797	31.315
4861	- 42.406	-31.297	35.030

Figure 2.21 shows the behavior of the locus for loop gains varying from zero to 8000. The region of optimality occurs for $4000 < K_o < 5000$. This value of gain results in the following loop dynamics:

1. $\omega_n \overset{\sim}{=} 40$ rad/sec
2. $\zeta \overset{\sim}{=} 0.7$
3. response to step in θ or $\dot{\theta}$ to within 10% error < 65 milliseconds
4. loop bandwidth, $f_n \overset{\sim}{=} 6.4$ Hz

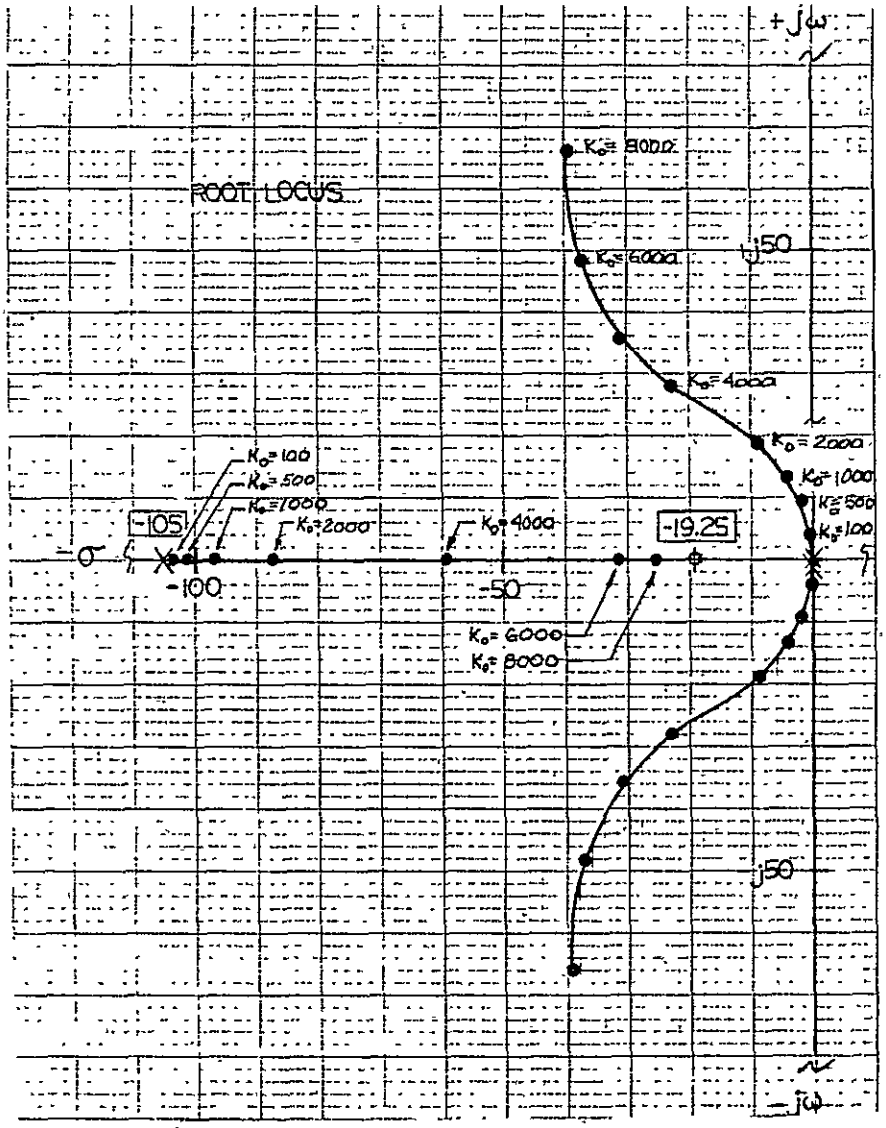
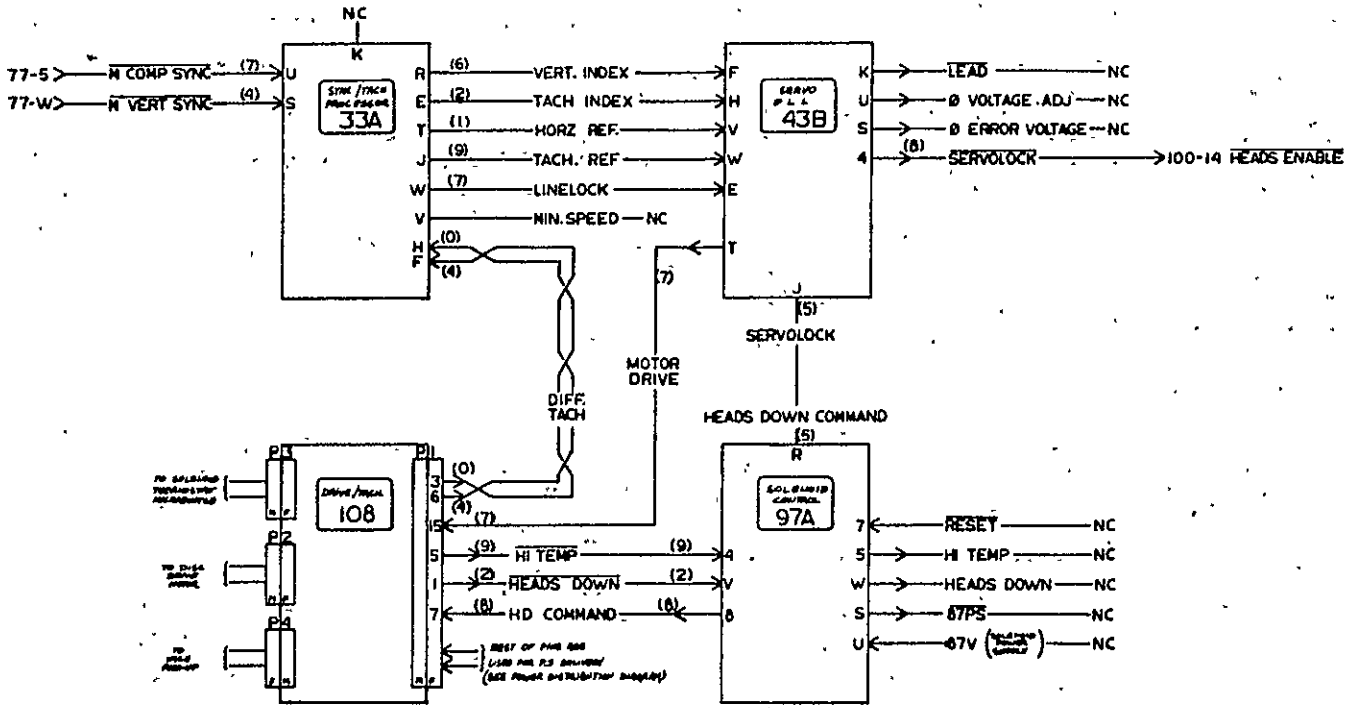


Figure 2.21 . Servo Controller Root Locus.

2.3.8 Functional Circuit Description

The Servo Control Group consists of four circuit boards whose interconnections are shown in Figure 2.22. Actual board functions are illustrated in Figure 2.23 and related timing diagrams in Figure 2.24.

Upon power-up, board 33A processes the television sync reference signals $\overline{\text{MCOMPSYNC}}$ and $\overline{\text{MVERTSYNC}}$ to yield $\overline{\text{HORREF}}$ and F2_{p} VERT INDEX respectively. These waveforms are shown in Figure 2.24, sub-figures 12 , 13, 10, and 11 . The high frequency servo loop, contained on board 43B, receives these signals and provides drive to the voltage-to-current converter and electronic commutator located on board 108 to bring the disc up to speed. The composite optical tach signal, illustrated in Figure 2.24, sub-figure 1 , passes to the tach processing electronics on 33A (see Fig. 2.23). This subsystem gives an indication when the disc reaches approximately 3000 RPM (MINSPEED, Figure 2.24;6) and enables the missing pulse detector (Fig. 2.23) to generate a phantom pulse (INSERT, Fig. 2.24;4). As the disc nears 3600 RMP, this pulse is included for 3 out of every 4 revolutions, causing the disc to slew at about 0.1% speed increase past the reference waveform, HORREF. The vertical coincidence detector provides a positive indication when the TACH INDEX (Fig. 2.24;9) aligns with the VERT INDEX. At this point the disc is locked in speed and position with the reference signals, and LINELOCK is enabled. Simultaneously, the tach processor includes the INSERT pulse in



NOTE. 1. THE SERVO GROUP IS LOCATED IN THE UPPER ENCLOSURE
2. WIRE COLOR INDICATED BY RESISTOR COLOR CODE - (X)

SERVO GROUP
SCALE NONE
DATE 10-7-77
TRANSMITER & RECEIVER

Figure 2.22

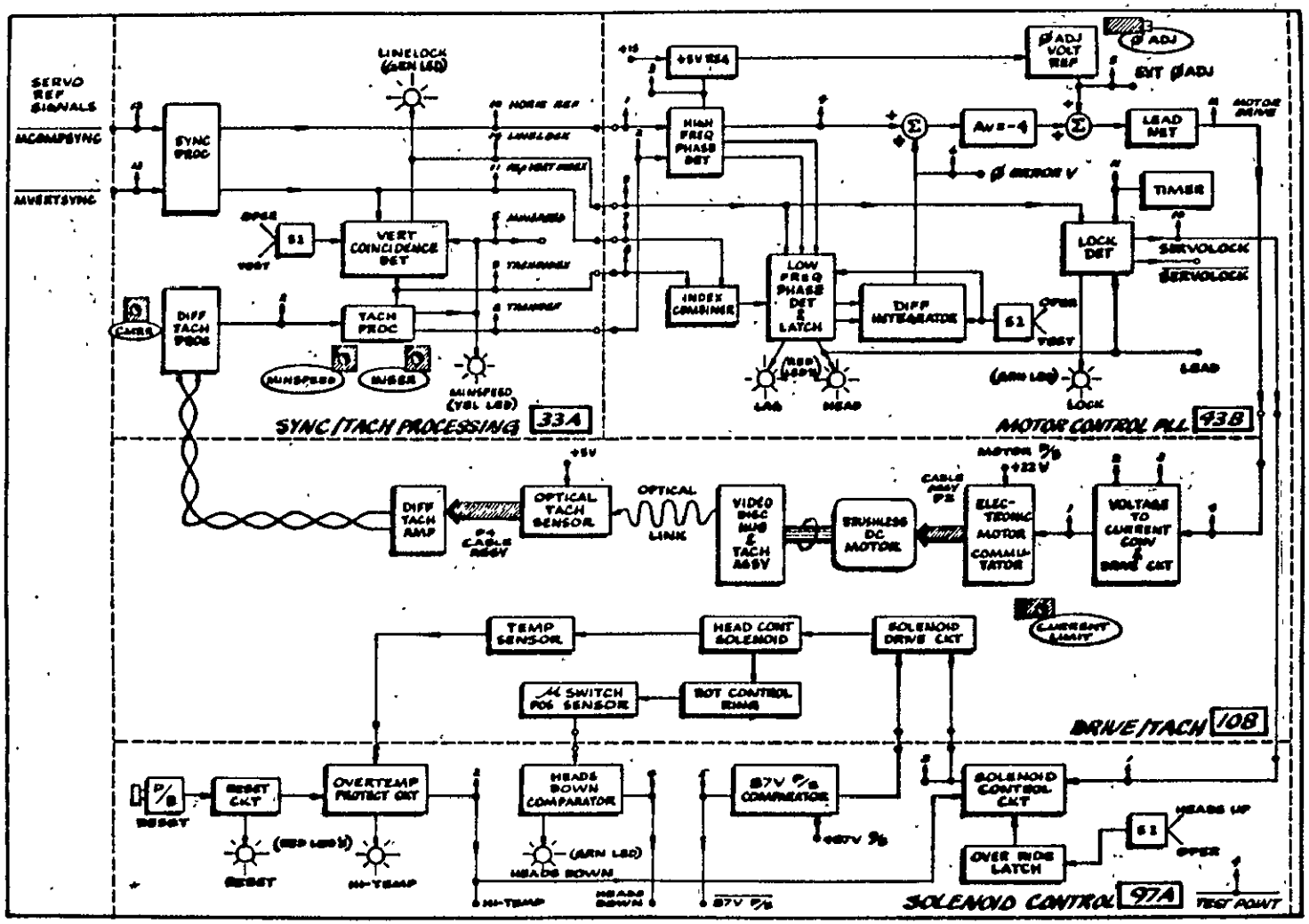


Figure 2.23 Functional Block Diagram of Servo Control Group

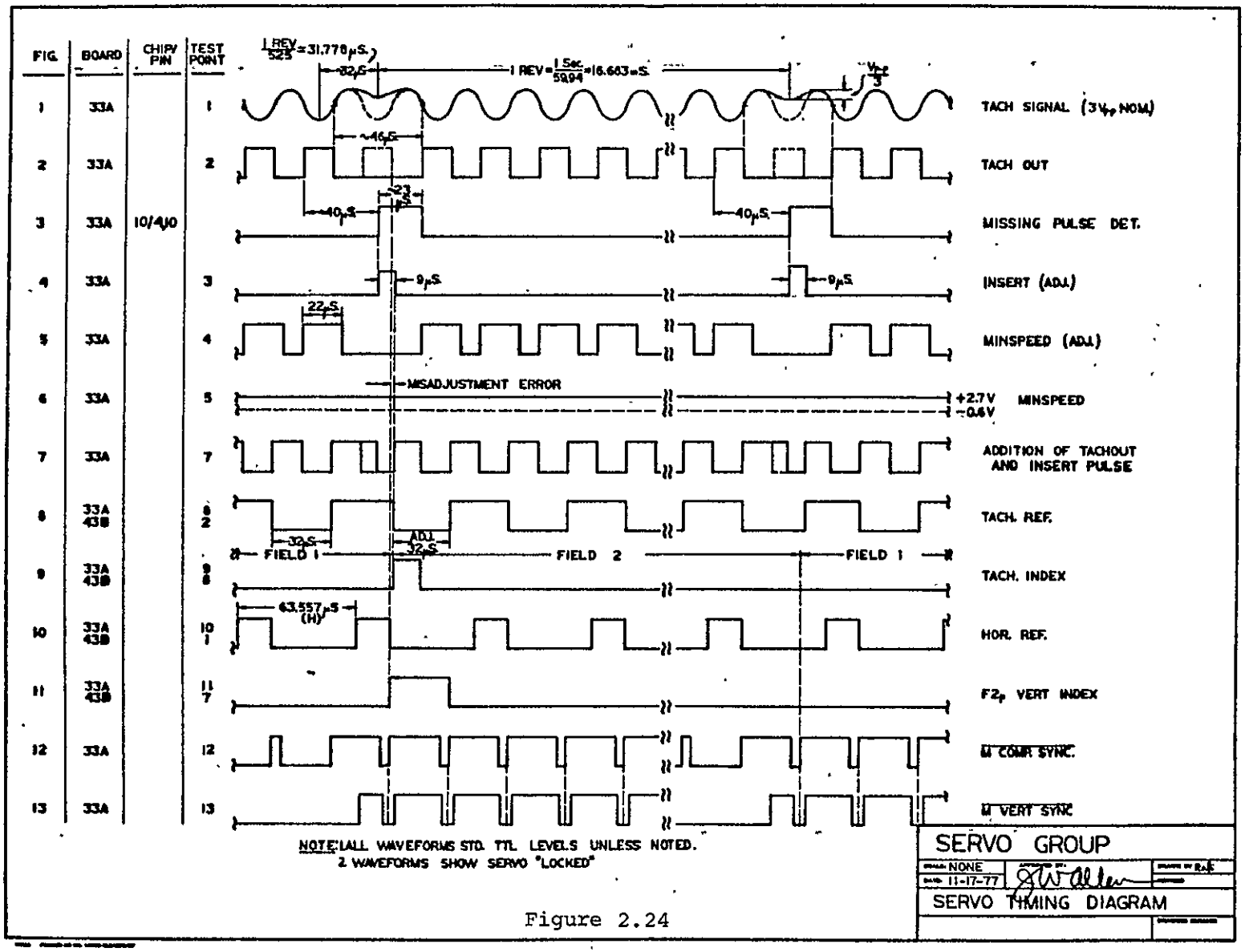


Figure 2.24

the composite tach data stream on every revolution, insuring the disc will not slew past the correct index position.

Once LINELOCK has been achieved, the low frequency phase detector, latch, and differential integrator on board 43B are activated to provide a correction signal to the main high frequency servo loop, such that rising edges of the index pulses are precisely aligned. The lock detector energizes the SERVO-LOCK line about 10 seconds after LINELOCK has been achieved, to be certain that the low frequency loop has had time to align the indices correctly. Real-time positional error of these indices is monitored every two revolutions and indicated by LAG and LEAD light emitting diodes (LED). During normal operation these flicker uniformly; this allows simple adjustment of the correct $\dot{\phi}$ ADJ offset current (located on board 43B). Measured disc jitter is on the order of $\pm$ 0.1 µsec peak to peak.

Switch S1 on 33A will disable the coincidence detection circuitry when placed in the TEST position. This feature allows recording frames from unstable timebases, such as those produced by helical-scan VTR's. Switch S1 on 43B allows the low frequency phase detector loop to be switched out when it is in TEST: this function is only needed during initial alignment when the $\dot{\phi}$ ADJ offset current must be set to place the indices in registration for no net correction by the low frequency loop.

The control range of the low-frequency loop is approximately $\pm \frac{H}{4}$ or about $\pm$ 15 µsec. Figure 2.25 illustrates the typical control

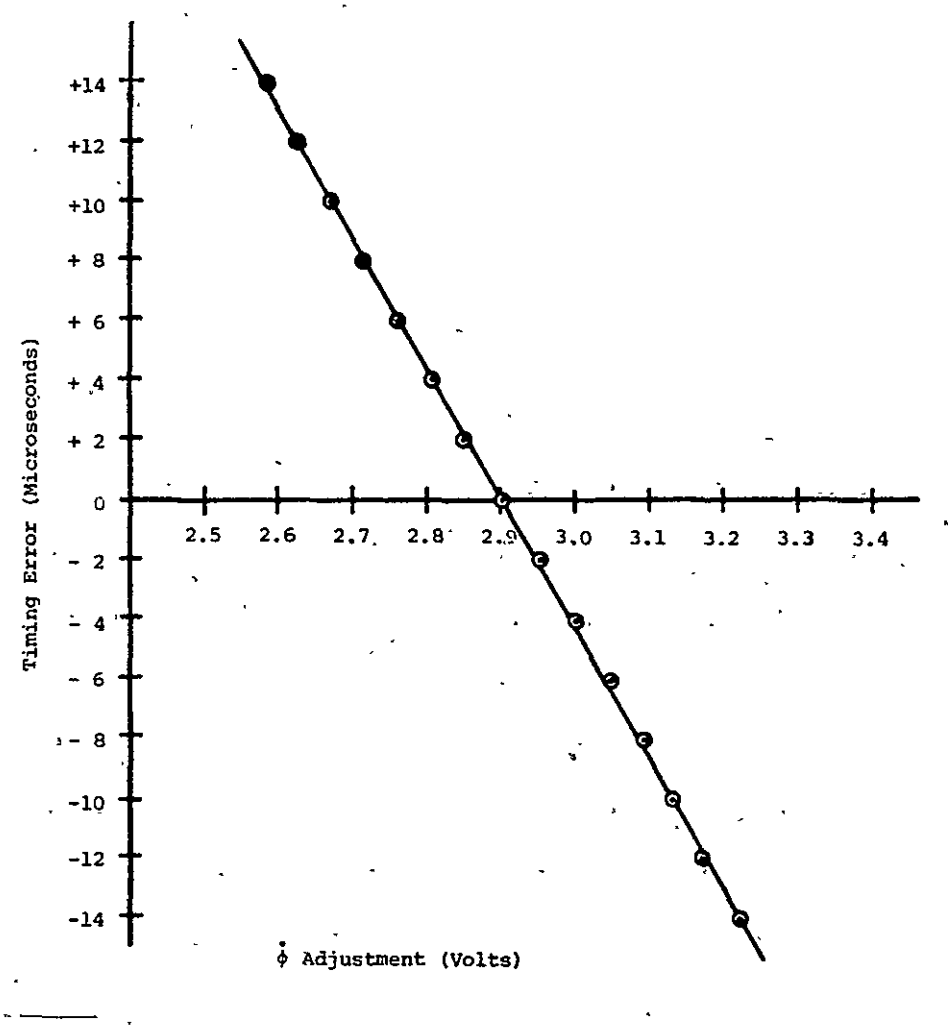


Figure 2.25 Open Loop Timing Error vs. Control Voltage

vs. $\dot{\phi}$ ADJ provided in 43B. In this case, the proper setting lies at about 2.9 VDC. Since loop gains will vary with the actual components used, this single "zero adjustment" has been provided to allow centering of the low frequency control loop at room temperature. The $\pm$ 15 µsec correction range is more than adequate to compensate for system temperature variations from 0°C to 50°C.

Complete initial alignment and checkout procedures, and schematics of the servo boards are available in Appendix 2.6.

2.3.9 Solenoid Control of Head Lifter

The video heads fly only when disc/head velocity is sufficient to "lift" them off the surface ($\sim$ 1000 i.p.s.). To prevent the heads from contacting the disc during start-up and shut-down, the head platforms are retracted and remain approximately 0.05" above the disc surface. Servo Group board 97A accepts the SERVOLOCK signal from 43B and energizes a solenoid to rotate a control ring beneath the disc platform; subsequent angular motion is transmitted to the lifter arms of each head platform to lower the video heads. This board monitors the solenoid power supply (87 VDC), as well as solenoid temperature. Should an overheat fault occur in the drive electronics or solenoid, the thermostat will automatically disconnect power and give a HITEMP indication which must be manually reset via a pushbutton. Positive heads-down indication is provided by a microswitch sensor mounted near the control ring. Both HITEMP and HEADSDOWN TTL compatible signals are provided for system monitoring.

Switch S1 allows manual lockout of the solenoid drive circuit to hold the heads in the UP position.

REFERENCES

1. EIA Standard RS-170 Electrical Performance Standards - Monochrome Television Studio Facilities, Nov: 1957, Figure 3.

2. Telephone conversation with Dr. Norm Meyers, Davis-Smith Corporation, San Diego, Ca.

2.4 VIDEO MODULATOR/DEMODULATOR SYSTEM DESIGN

2.4.1 Introduction

Characteristics of the magnetic record-reproduce process will be developed and related to video disc recording parameters in terms of required head and disc specifications. Electronics system requirements are divided into three sub-groups - Read-Write (R/W) electronics, modulator, and demodulator electronics. Design parameters, circuit configurations, and performance specifications will be developed and discussed for each sub-group. Overall system performance will be evaluated with comments for possible areas of improvement. A discussion of the FRAME R/W cycle (transmit terminal) and LINE R/W cycle (receive terminal) is given.

2.4.2 The Magnetic Record/Reproduce Process - Basics

When an electrical signal is recorded on magnetic media, the tape (or disc) must be magnetized such that a given flux amplitude and polarity as a function of tape location represent the signal as a function of time. The relative tape-head motion, which is (usually) maintained constant during the record or reproduce process causes time variations of the electrical signal to be translated into spatial magnetic flux variations within the media. The remanent flux, ϕ_r, within the media can be expressed, for a sinusoidal current in the record head as:

$$\phi_r = KI\sin\omega t \qquad 2.9$$

where: I = peak current (Amp)

ω = instantaneous angular frequency (rad/sec)

K = read/media loss factor

t = time (sec)

The record loss factor K, is in general a function of the head/tape geometry, magnetic material, and frequency. Loss mechanisms involve record head losses, media self-demagnetization, and record separation losses.[1] In general, these losses (compared with those experienced in the reproduce process) modify the record-reproduce transfer function primarily in the form slightly of decreased response at high frequencies. Naturally, they are intimately related to the choice of magnetic materials, which is not pertinent to this discussion. The interested reader should refer to a recent tutorial in magnetic recording for an in-depth treatment of these loss mechanisms.[2]

The magnetic flux at any point along the tape can be represented as:

$$\phi_r = K\ I \sin\frac{2\pi x}{\lambda} \qquad 2.10$$

where: x = linear tape coordinate

λ = recorded wavelength = $\frac{s}{f} = \left(\frac{\text{tape/head speed}}{\text{record frequency}}\right)$

Playback voltage is induced in the reproduce head by flux lines

emerging from the media which pass through the head core. The amplitude of the voltage is determined by the rate at which a given number of flux lines cut the fixed number of turns of the head windings (Faraday's Law). The flux can be represented as:

$$B = K' \frac{d\phi_r}{dt} \qquad 2.11$$

where: B = emerging flux

K' = loss factor

ϕ_r = remanent flux

The reproduce loss factor, K', is a complex function of many phenomena and will be examined in detail later. This equation may be expressed, in the tape coordinate, as:

$$B = K''I \frac{2\pi}{\lambda} \cos \frac{2\pi x}{\lambda} \qquad 2.12$$

where $t = \frac{x}{s}$, $f = s/\lambda$, $\phi_r = KI \sin\omega t$, $K'' = KK's$.

The head output voltage, e, is directly proportional to the number of flux lines cut per unit time; thus:

$$e = KI f\cos\omega t \qquad 2.13a$$

or $$e = K''Is \frac{2\pi}{\lambda} \cos \frac{2\pi x}{\lambda} \qquad 2.13b$$

where: K = composite loss factor

It is seen that 1) output voltage is proportional to record current and frequency, 2) record and reproduce frequencies are identical for constant tape/head velocity, 3) record current and

output voltage have a 90° phase difference for any location on the tape. Next, the particulars of video recording will be examined.

2.4.3 Saturated FM Video Recording

The video spectrum extends from virtually dc through several megahertz; direct recording is impossible because reproduce voltage approaches zero as frequency approaches dc. Thought of another way, the signal to be recorded covers over 20 octaves in frequency. Notwithstanding S/N limitations, the recorder would have to cover a dynamic range on the order of 120 db (6 db/octave). Fortunately, the video signal may be FM encoded such that the range of wavelengths to be occupied within the magnetic medium is reduced to less than one decade. An additional advantage of this approach is that FM reproduction depends only upon the density of zero-crossings of the readback signal rather than its amplitude. Thus, sufficient magnetic force may be applied to the medium to achieve saturated remanent flux, ϕ_r, for maximum playback S/N. The linearity of video luminance (amplitude) is only a function of the FM mod/demod linearity and group delay and is independent of the linearity of the record/reproduce process. It is necessary, however, to closely examine the reproduce losses associated with the head and disc in order to specify the FM energy distribution for optimum video performance.

2.4.4 The Magnetic Reproduce Process

Equation (2.13a) indicates that reproduce head output voltage

increases indefinitely from dc as a function of frequency at 6db/octave for constant recording current in the head windings. In fact, that is hardly the case. Various loss mechanisms considerably modify the reproduce characteristic as shown in Table 2.7 below.

TABLE 2.7

REPRODUCE LOSS MECHANISMS

Type	Frequency Region Affected
1) Finite effective head gap	
2) Head-to-tape separation	
3) Finite head permeability	
4) Head-to-tape gap azimuthal misalignment	High
5) Head magnetics losses	
6) Magnetic surface losses (dynamic head bounce)	
7) Media thickness (flux penetration)	
8) Media self-demagnetization	
9) Record loss effect	
10) $\lambda/2$ to head contact area losses	Low
11) Head "bump"	

Perhaps the most significant alteration to the reproduce function results from head gap losses (finite scanning aperture). The resulting loss factor can be expressed as a function of recorded frequency as[3,4,5]

$$\text{Gap Loss (db)} = L_g = 20\log_{10}\left[\frac{\sin K_1 f}{K_1 f}\right] \qquad 2.14$$

f = frequency (Hz)

$K = \frac{\pi g_e}{s}$

g_e = effective head gap* = 1.12g

g = actual head gap (in.)

s = head-to-disc speed (i.p.s.)

The video heads chosen for this system have a nominal gap width of 50 μin. Narrower gaps would yield higher reproduced frequency response, but exhibit readback signals of insufficient signal-to-noise ratio. Complete head specifications are shown in Appendix A2.7.

The video head need not be in direct contact with the surface of the magnetic disc. These particular heads fly in an aerodynamically stable state approximately 8-10 μinches above the surface, which eliminates the possibility of head or disc wear. In order to achieve a stable flying condition, head platforms were designed to allow virtually independent adjustment of head height, pitch, yaw, and roll (see Figure 2.26). A triangular head platform located on sub-assembly (1) in the figure is capable of accommodating three independent heads spaced on 0.100" centers. Up to 12 platforms (36 heads) can be mounted around the periphery of the disc.

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*The effective head gap varies (due to fringing) from 1.1 to 1.15 times the physical gap width, g, for various magnetic head configurations. A figure of 1.12 is often used for video ring heads such as those used on disc recorders.

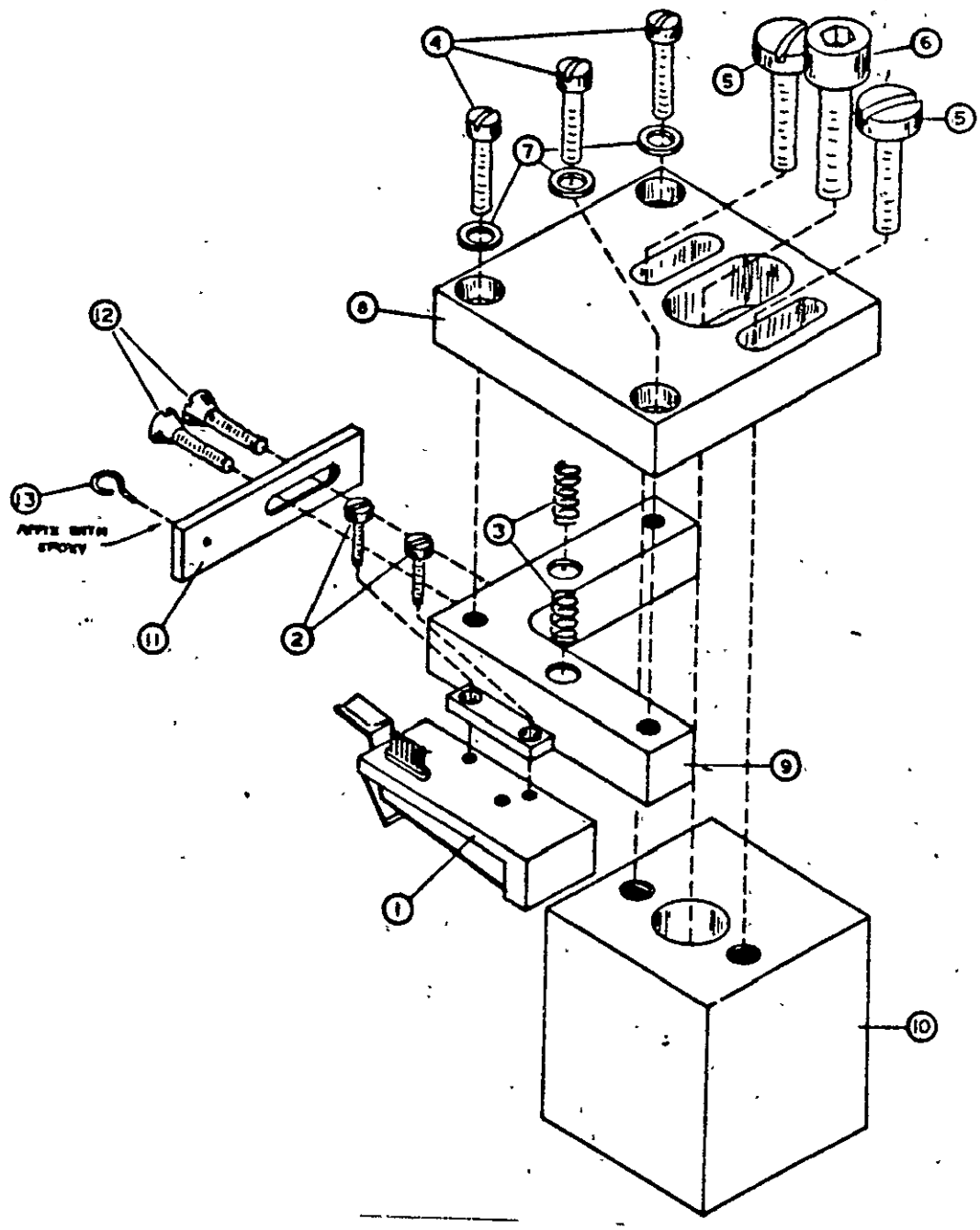

Figure 2.26. Head Mount Assembly View.

The price to be paid, however, for the advantage of eliminating head and disc wear is the associated disc/head-gap separation losses. It is intuitively clear that during the recording process the magnetic force, H, due to head winding currents, decreases as a function of increasing distance from the head gap. The number of flux lines cutting the core during the reproduce process will also be reduced as the head is moved away from the magnetic disc. Wallace[3] shows this relation to be

$$\text{Separation Loss} = L_s = 54.6 \left(\frac{d}{\lambda}\right) \text{ db} \qquad 2.15$$

d = separation of head and disc (in.)

λ = recorded wavelength (in.)

Figure 2.27 shows combined reproduce profiles accounting for gap and seapration losses for d values of 0, 10, 20 and 30 μin. It can be seen that significant losses are experienced for even 10 μin. separation. Figure 2.28 (courtesy of Davis-Smith Corporation) illustrates the relative sizes of various disc contaminants and head-to-disc separation to give the reader a better feeling for the dimensions involved.

Finite head permeability further influences the characteristics of Figure 2.27, but the effects are negligible compared to separation losses.[6] The fourth loss mechanism, head-to-tape gap azimuthal misalignment error, can contribute serious high-frequency losses, particularly for machines with interchangable media (audio and

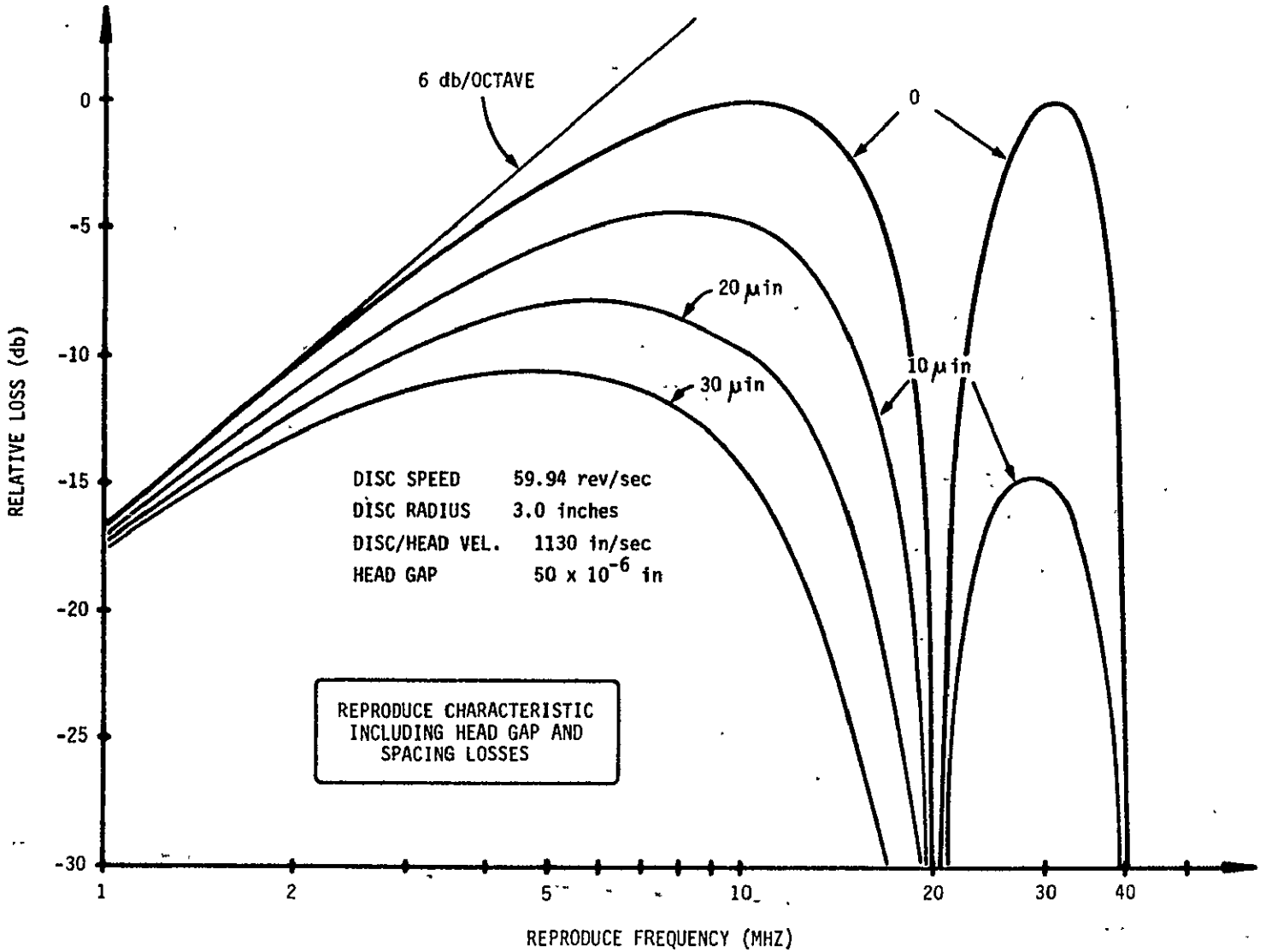

Figure 2.27. Reproduce Characteristics Including Head Gap and Spacing Losses.

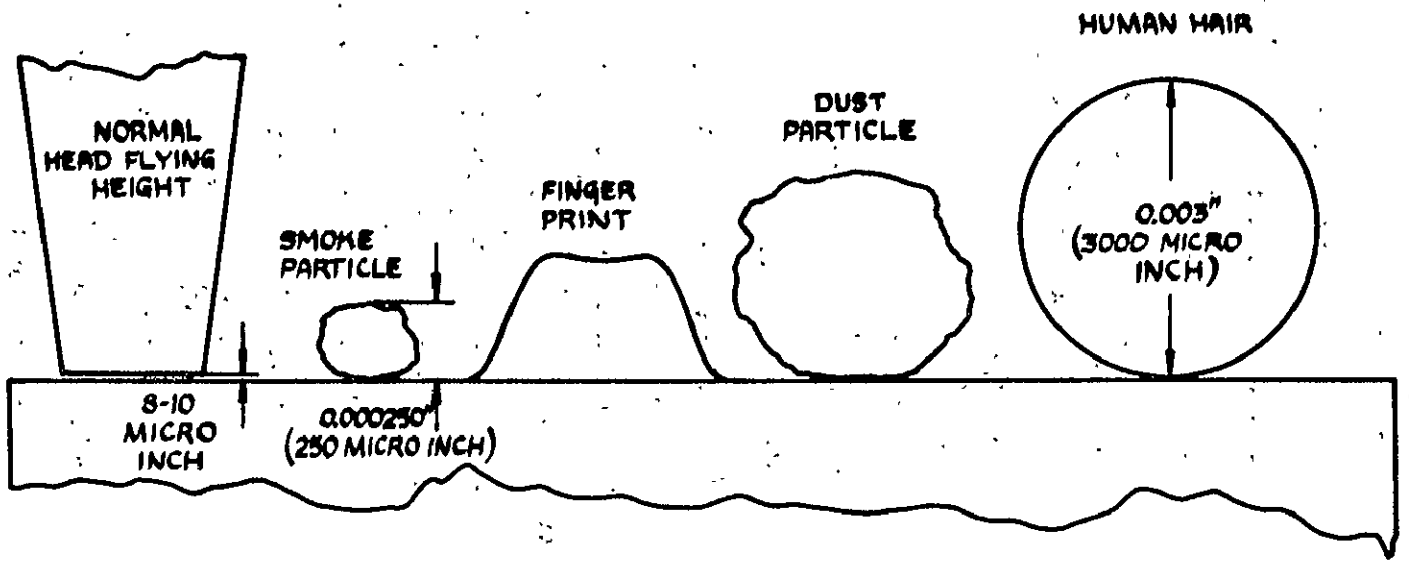

Figure 2.28. Sizes of Various Video Disc Contaminants.

video tape recorders, digital disc memories, etc.). The video disc with fixed heads is relatively immune to this effect, as the same head platform is used for both record and reproduce processes. The design of moving head arms, however, must be influenced by the tolerance requirements to be outlined.

Azimuthal alignment losses are given by:[7]

$$\text{Alignment loss (db)} = 20 \log_{10} \left\{ \frac{\sin \theta}{\theta} \right\} \qquad 2.16$$

where: $\theta = \frac{\pi W \tan\alpha}{\lambda}$

W = width of recorded track (in.)

α = angle of misalignment between record and reproduce head gaps (rad.)

λ = wavelength of recorded signal (in.)

Figure 2.29 illustrates relative losses at fixed frequency (10 MHz) as a function of alignement error, α . Figure 2.30 shows the frequency dependent losses for $\alpha = 0$, 5', 10', and 15', while Figure 2.31 shows combined gap and azimuth alignment losses.

It can be concluded that azimuthal tracking requirements for a moving head-arm dictate alignment errors less than 1/6° for associated read losses under 3 db (see Figure 2.30).

Eddy current losses and magnetic losses are purely a function of magnetic head construction. The primary loss mechanism for video reproduce heads is magnetic material losses. This loss is

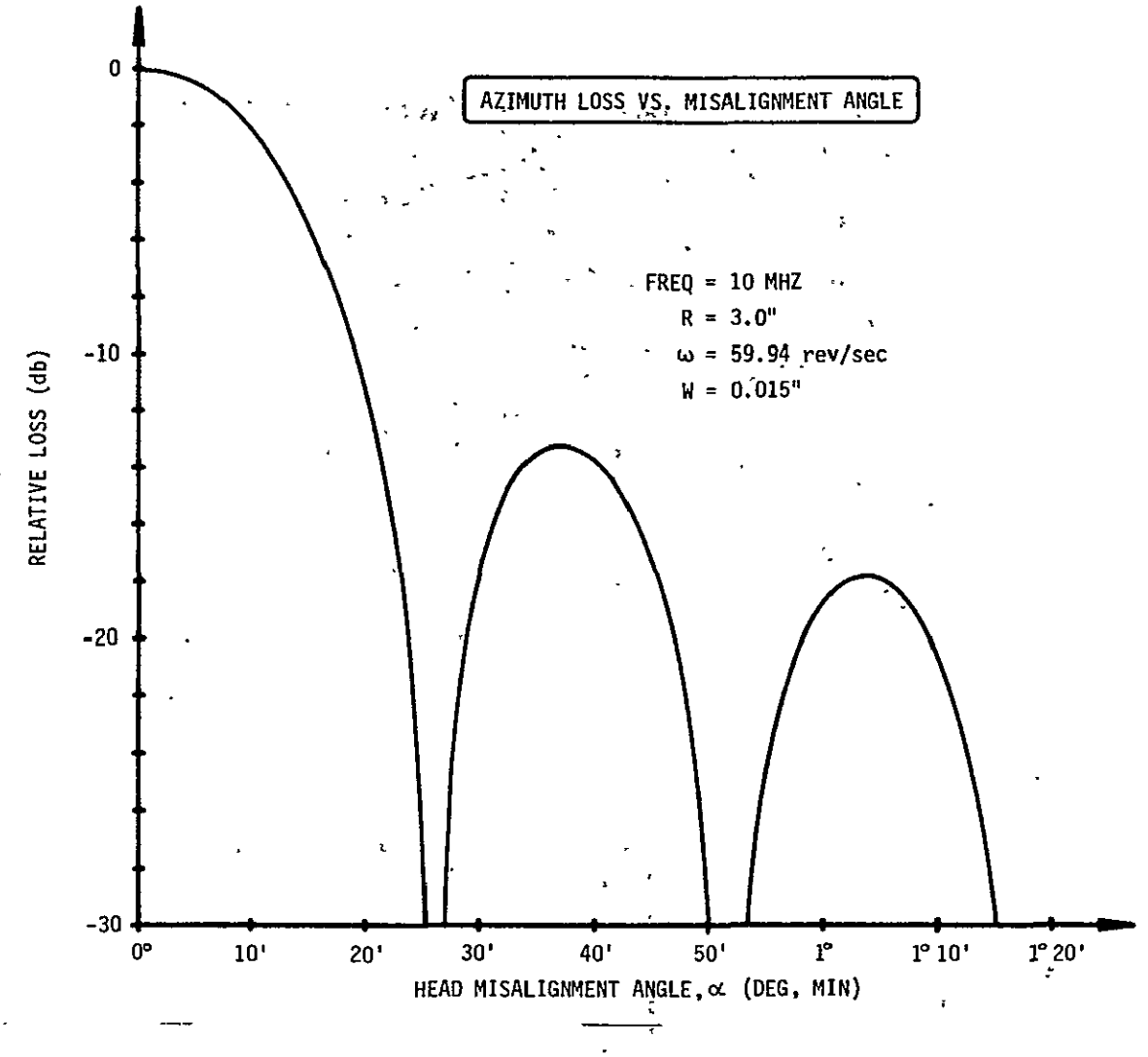

Figure 2.29 Azimuth Loss vs. Misalignment Angle.

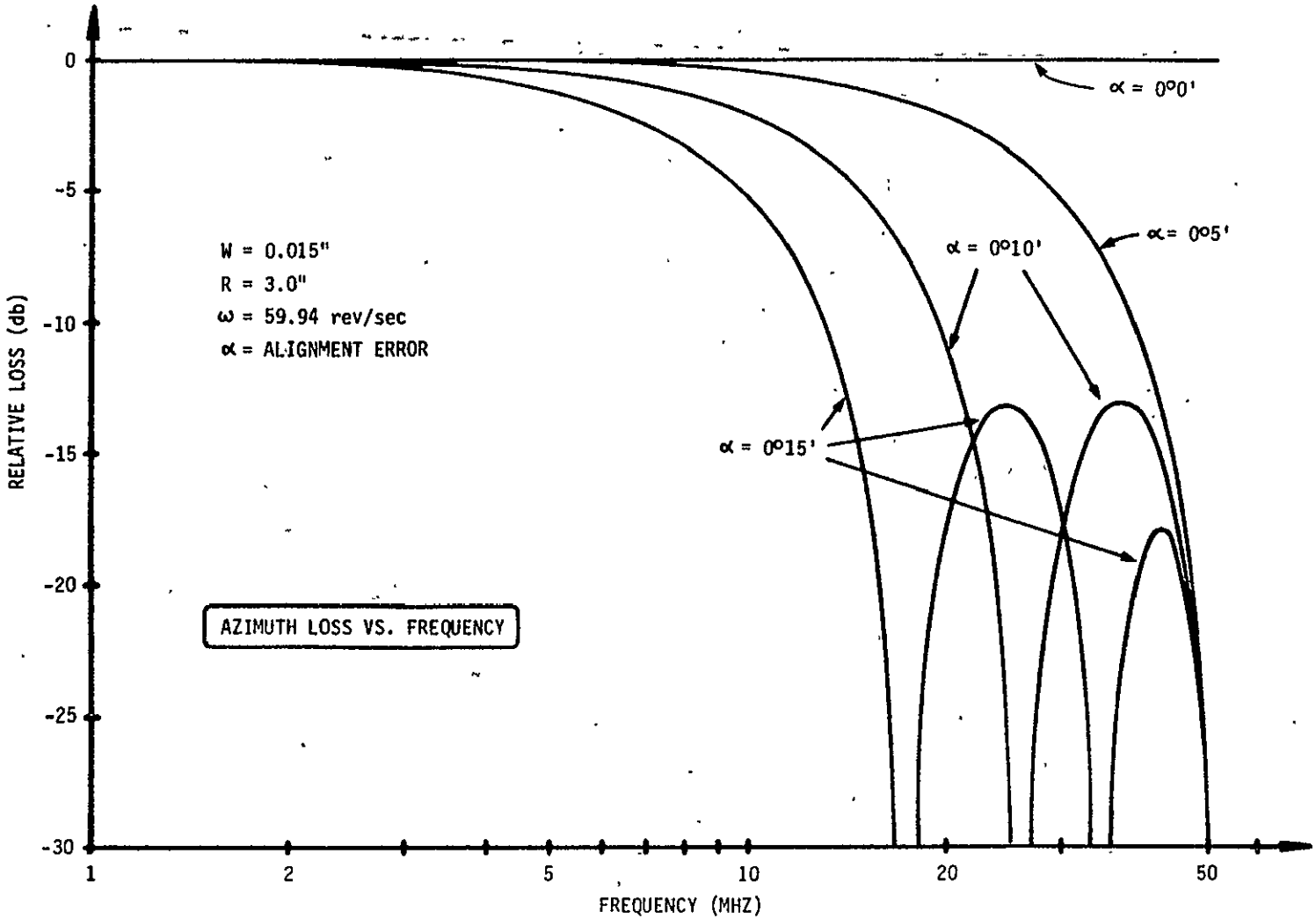

Figure 2.30. Azimuth Loss vs. Frequency.

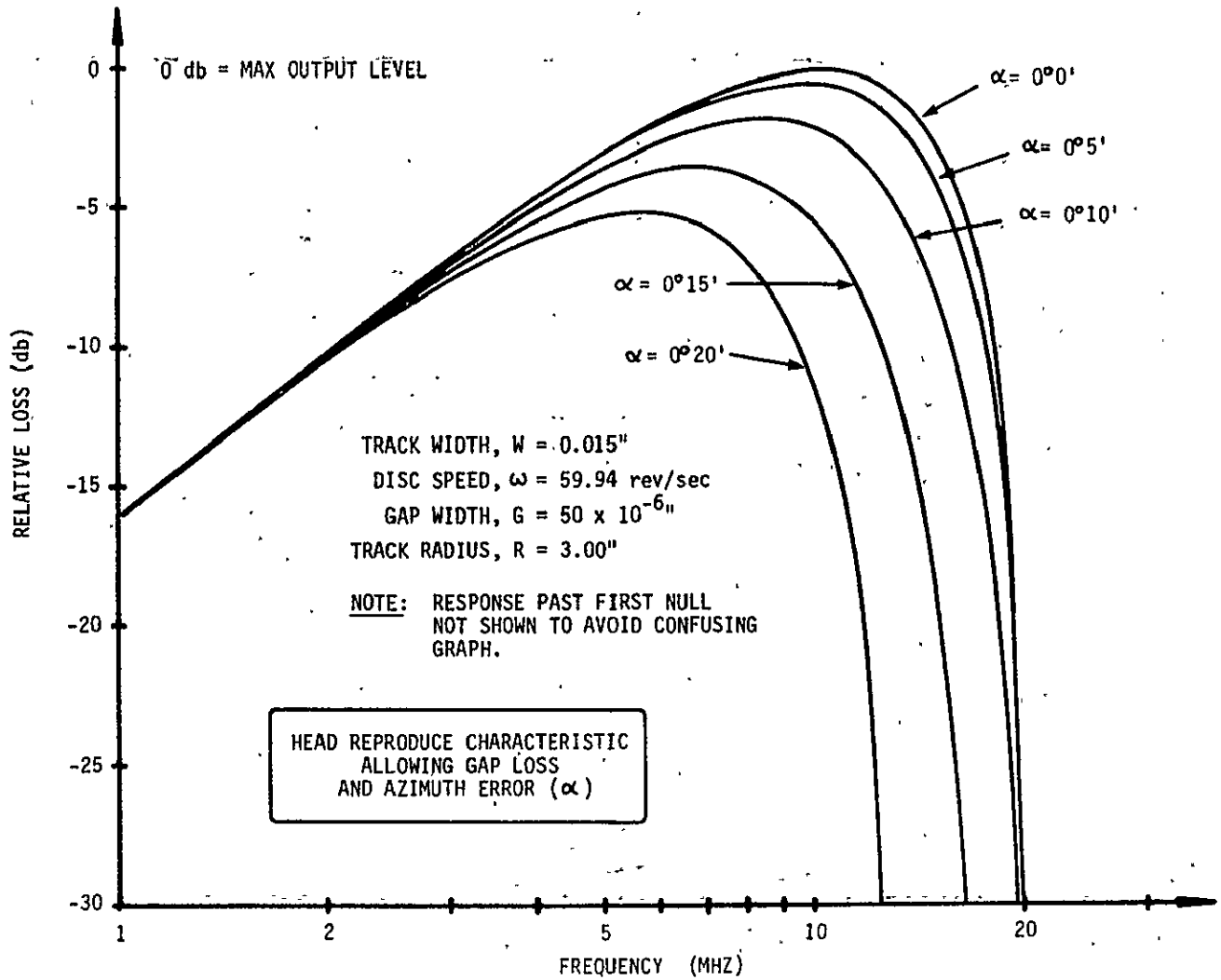

Figure 2.31. Head Reproduce Characteristic Allowing Gap Loss amd Azimuth Error.

typically measured by sending a constant current through an auxilliary head winding and measuring the open circuit voltage developed across the normal winding. Any departure from a 6 db/octave increase with frequency is due to head losses. The video heads used for the disc recorder should exhibit a loss of no more than a 1-2 db up to 10 MHz. Measurements on closed ring samples were taken and confirmed this specification.

Magnetic surface losses are due to the non-flatness of the disc - the loss mechanism is separation loss. The disc/head aerodynamics for a flying video head cause envelope variations of approximately 10-15% in the playback signal. These irregularities increase dramatically when the head and/or disc become contaminated. In severe cases the head may not fly at all. For a properly flying head, the 1-2 db envelope modulation is not a concern in saturated FM recording, but would seriously distort any directly recorded signal due to the random nature of the imposed modulation.

Since no magnetic coating can be made infinitely thin, the playback signal for low frequencies has greater amplitude than that for high frequencies. This phenomenon is due to increased flux contributions from magnetic material located beneath the disc surface.[8] Analytically this can be expressed as:

$$\text{Media Thickness Loss} = L_t = \left[\frac{1 - e^{-2\pi t/\lambda}}{2\pi t/\lambda} \right] \qquad 2.17$$

t = effective coating thickness

Table 2.8 illustrates losses associated with inner and outermost tracks of a video disc rotating at the television field rate (59.94 rev/sec) for 5 μinch effective coating thickness.

Half wavelength/head contact area and head "bump" losses[9] contribute only at low spatial flux densities. The FM'd video spectrum lies well above frequency regions for which these phenomena would effect the playback response. In the case of a direct recording process, as used in commercial audio tape machines for example, proper head design concepts must be applied to achieve adequate low frequency response.

Self-demagnetization losses in the magnetic material decrease high-frequency response. This can be accounted for qualitatively by associating small bar magnets with each local magnetic domain. At long wavelengths most bars are aligned within a given length of tape; at higher spatial frequencies more flux reversals exist within this same distance. When the magnetizing flux is removed some domains will tend to reverse polarity due to the competing effects of nearest neighbors. Naturally, the effect is more pronounced for high spatial variation of flux density. Calculations based upon a more detailed tratement[10] indicate this effect to be negligible (<-1db) up to 10 MHz in this application.

Some experimenters[11] have found high frequency losses dependent upon contact or non-contact (heads flying) recording. As might be expected, less high frequency readback signal is present for non-contact recording. The magnitude of this effect seems to be

TABLE 2.8

CALCULATED PLAYBACK LOSSES DUE TO COATING THICKNESS*

Frequency (MHz)	Inner Radius r = 2.25" Loss (db)	Outer Radius 5 = 3.00" Loss (db)
1	0.16	0.12
2	0.32	0.24
3	0.48	0.36
4	0.64	0.48
5	0.79	0.60
6	0.95	0.71
7	1.10	0.83
8	1.25	0.95
9	1.41	1.06
10	1.56	1.18
11	1.71	1.29
12	1.86	1.41
13	2.01	1.52

*Video disc speed 59.94 rev/sec, magnetic coating thickness 5µin.

approximately 2-3 db at 10 MHz for a video disc with state of the art ring heads at tape/head speeds of ∿ 1000 i.p.s. The exact mechanisms are not completely understood and are being closely investigated.

Figure 2.32 depicts the combined effects of gap, separation, magnetic material, and head losses to be expected based upon the previously examined loss mechanisms. Best (outer track) and worst (inner track) responses are illustrated. Video heads used on this machine have a nominal gap width of 50 micro inches with a production tolerance of ± 20%. For this reason, expected losses were calculated for this range of gap widths.

2.4.5 Measurement of Disc Write/Read Characteristics

Experiments were conducted to determine the actual video disc write/read transfer frequency response in order to confirm theoretical predictions. The necessary interface electronics designed for this purpose were later used as a basis for a final portion of the design and as such will be described in detail later in this chapter. A write amplifier (constant current vs. frequency) was developed to drive video heads at current levels up to 100 ma_{pp} from 3 to 13 MHz. Considerable effort was expended to achieve flat wideband gain and delay characteristics and low harmonic distortion. The same criteria were applied to read amplifier design and methods of coupling the video heads to each system. Testing the read amp was conducted by providing constant current drive to an auxilliary video head winding and measuring the resultant amplifier output

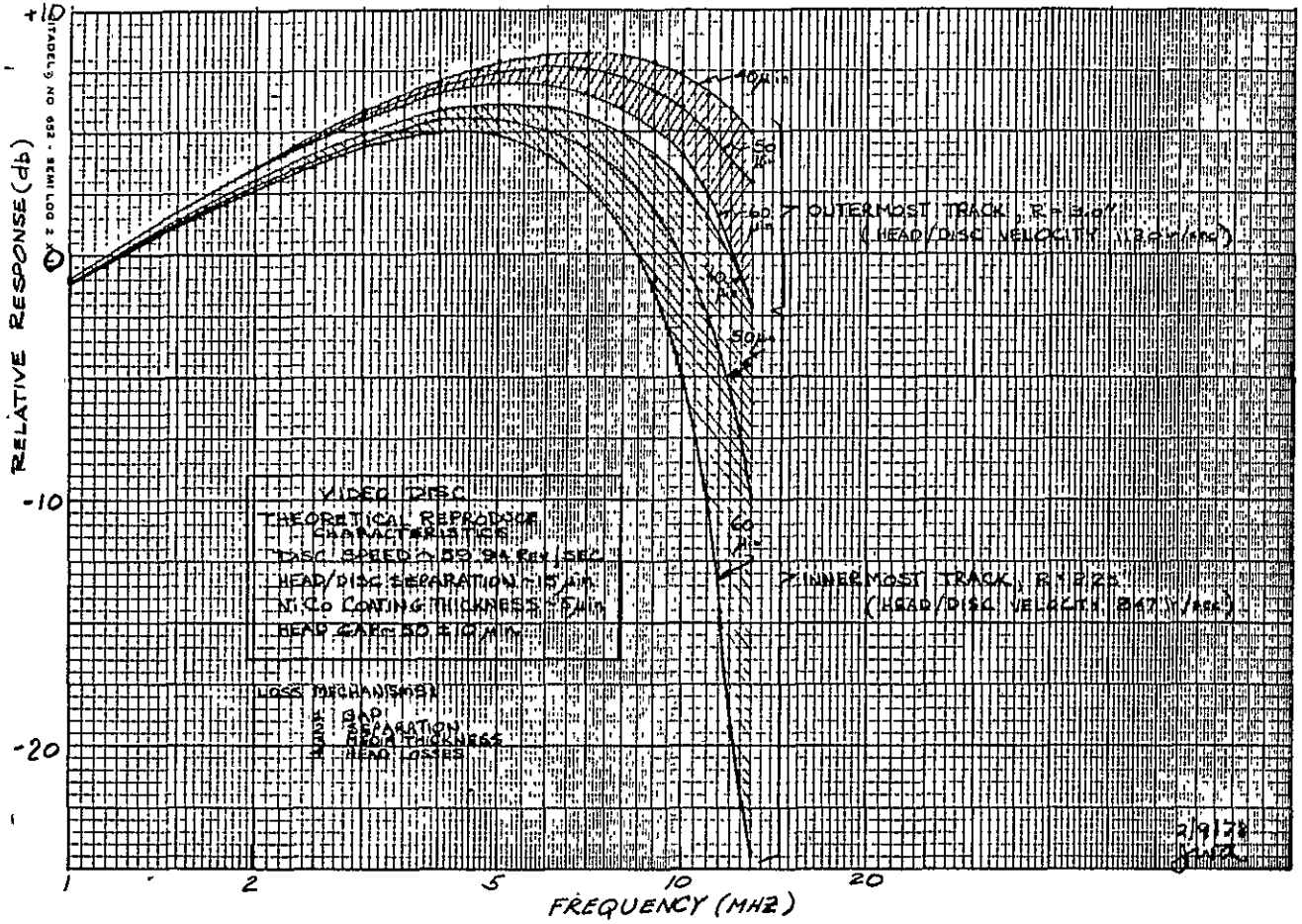

Figure 2.32 Video Disc Theoretical Reproduce Characteristic

voltage. Departures from a strict 6 db/octave increasing slope were indications of non-uniform response. After corrections for head loss and electronic imperfections, the disc transfer function was determined by successively recording single frequencies from 2 to 12 MHz. Figure 2.33 shows the experimentally determined response of the disc/head pair for the innermost track (worst case). Vertical bars indicate the range of uncertainty for experimental error and variation from head to head. In all, six individual heads of the same type were tested to assure a reasonable range of gap widths.

The experimental results, necessary for determination of the video FM spectral distribution, are in close agreement with expected results, although high frequency losses are somewhat greater. It was concluded that any further investigation and measurement of high frequency losses to reconcile this data would not be of practical importance with regard to the application.

2.4.6 R/W Electronics (57A)

The read-write (R/W) electronics contained on a single card (57A), are divided into three functional groups: 1) write amplifier, 2) head switch, and 3) read amplifier (see Fig. 2.34). The write amplifier must accept the wideband FM video spectrum and produce constant record current in the video head winding. Constant record current as a function of frequency produces the optimum trade-off between playback S/N and moire effects in the reproduced video.[4] The head switch serves to connect the write amp during record to

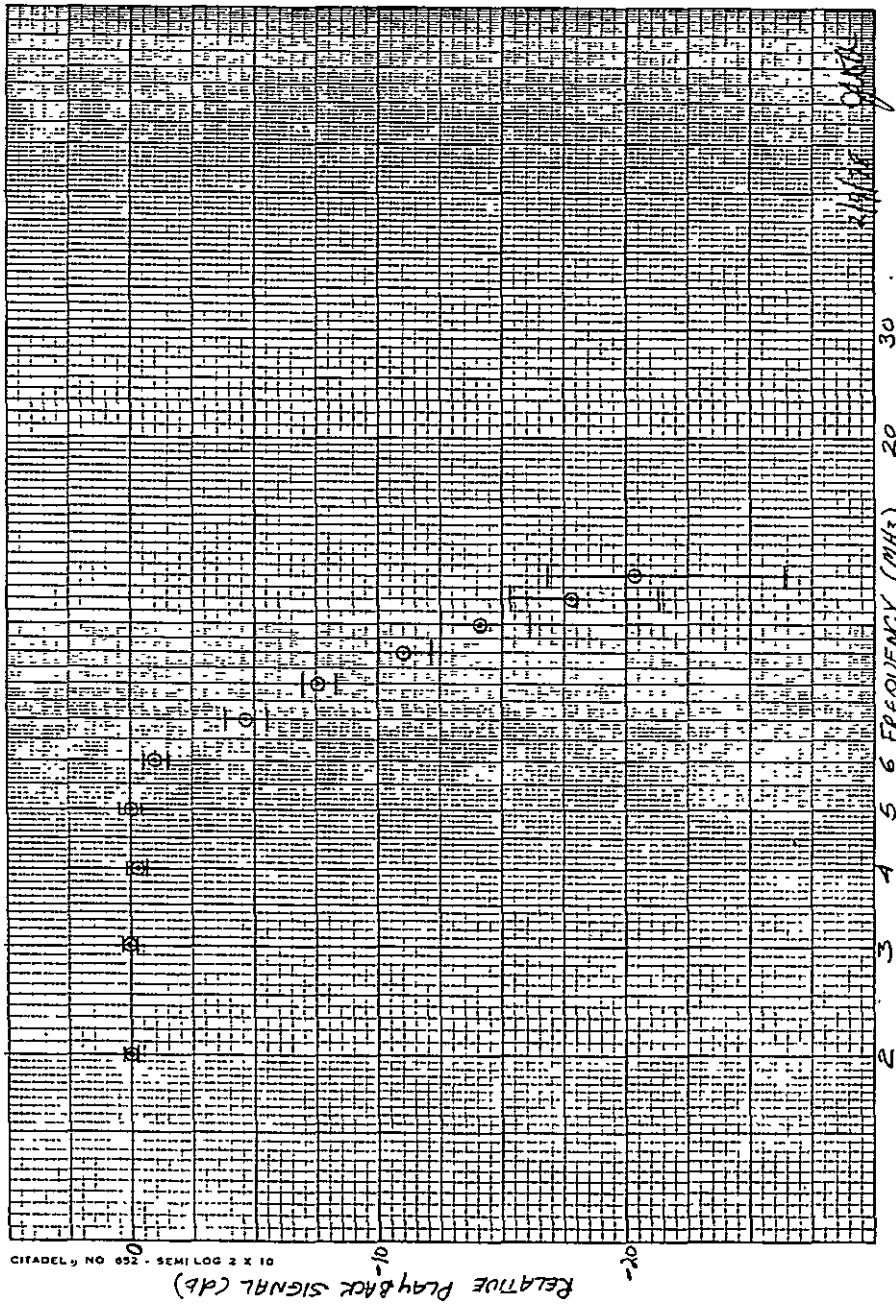

Figure 2.33 Measured Worst Case Disc Reproduce Characteristic

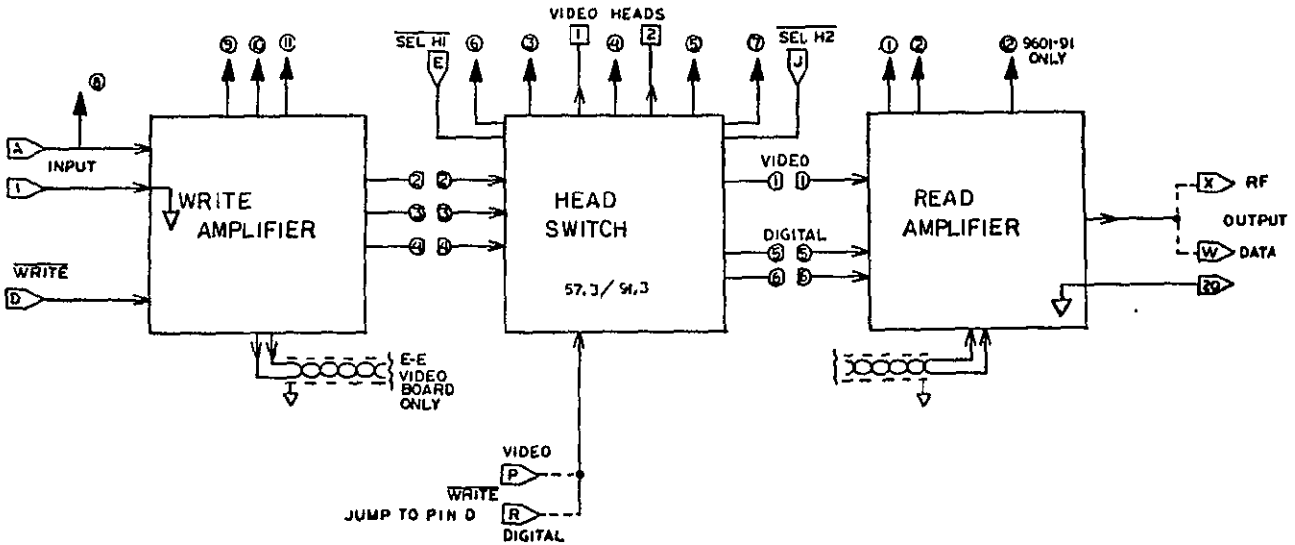

Figure 2.34. R/W Board Block Diagram.

either of two video heads; one head is assigned to each field of the television frame. During playback, these same heads are disconnected from the write amplifier output and connected to the read amplifier, which amplifies and low-pass filters the disc playback spectrum prior to FM demodulation. The input and output interface with balanced 50Ω coaxial cable.

2.4.7 Write Amplifier and Head Switch

The unbalanced write amplifier input is converted to a balanced differential signal via a miniature wideband transformer (Figure 2.35). For saturated recording, head currents ∿ 100 ma are required over a 1-10 MHz bandwidth. Constant current operation is achieved by a voltage driven differential cascode amplifier with resistive degeneration in the emitters (see Appendix A2.8 for schematic diagram). A potentiometer in the emitter legs compensates for imbalance in the differential amp. The output signal is coupled to the heads via several wideband transformers and diode arrays as shown in Figure 2.35. The diode bridge serves to isolate the read amp from the high-level record currents and couples to the diode arrays driving each video head. Heads are connected alternately on successive disc revolutions (to provide sequential field recording) by the TTL head select lines.

Initial measurements of head current vs. drive voltage were undertaken employing a wideband (∿ 100 MHz) current probe in series with the head winding. Frequency response (Figures 2.36,2.37) was

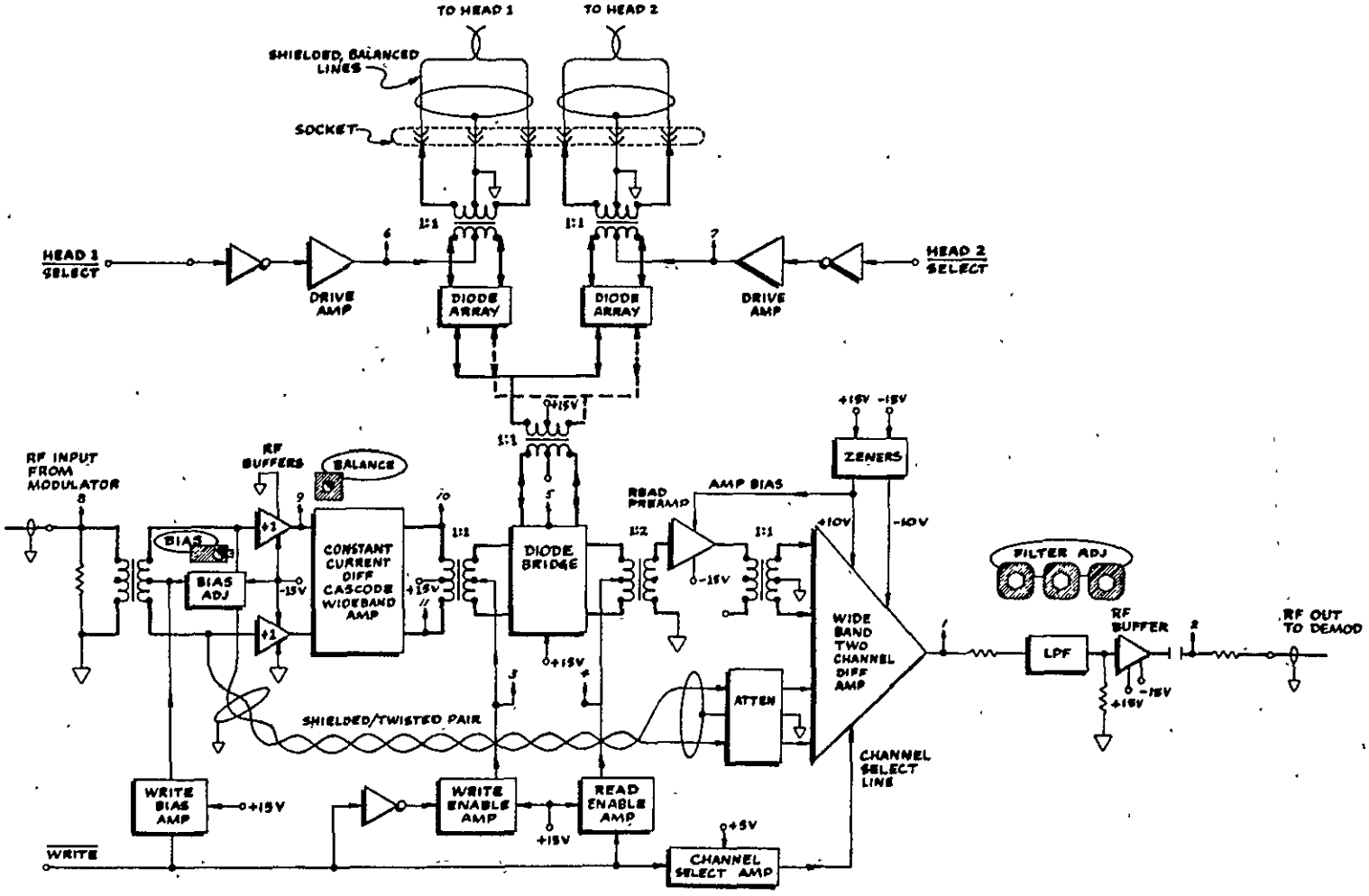

Figure 2.35. Functional Block Diagram (57A).

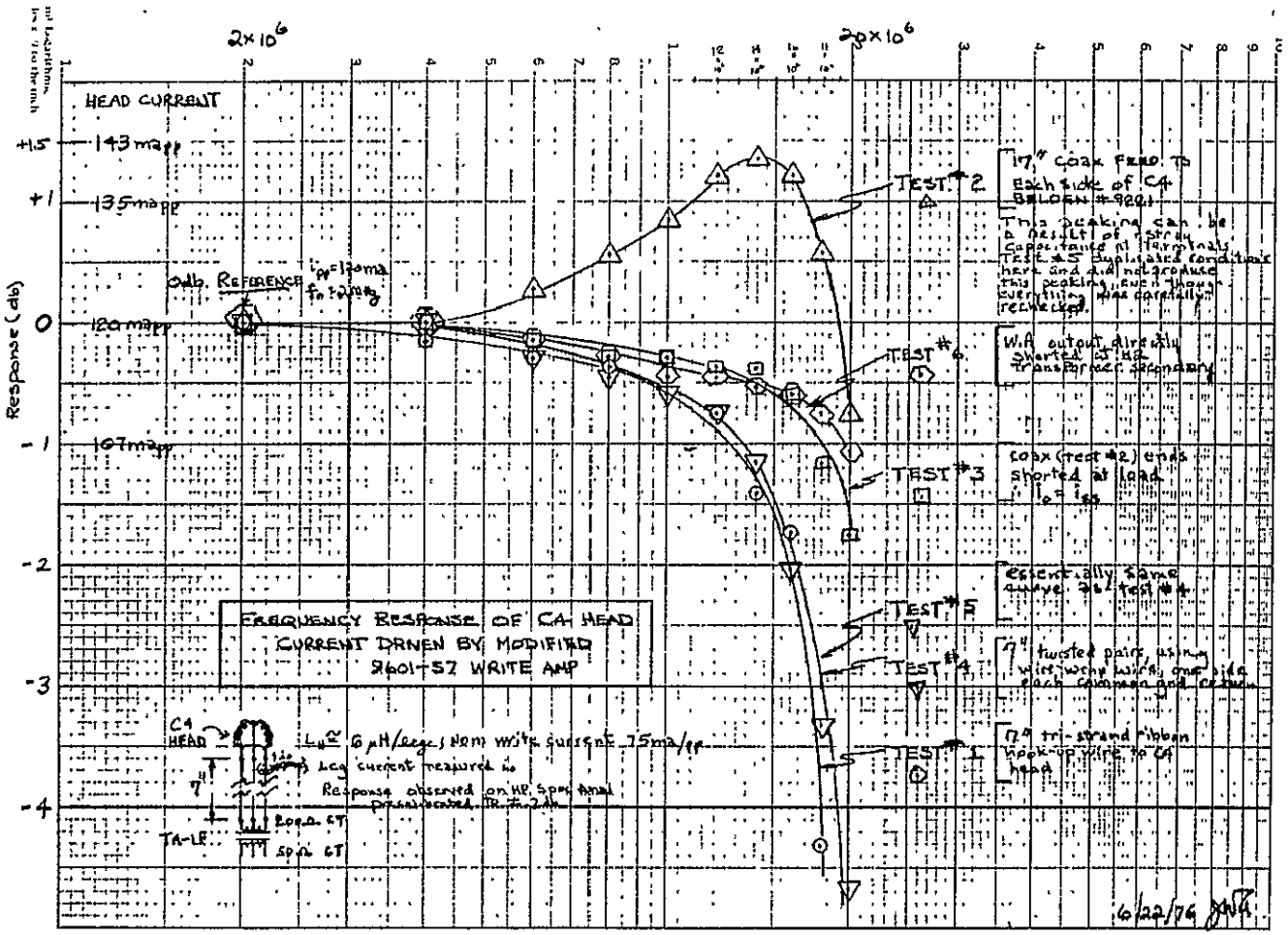

Figure 2.36. Video Head Response for Various Types of Head Cable.

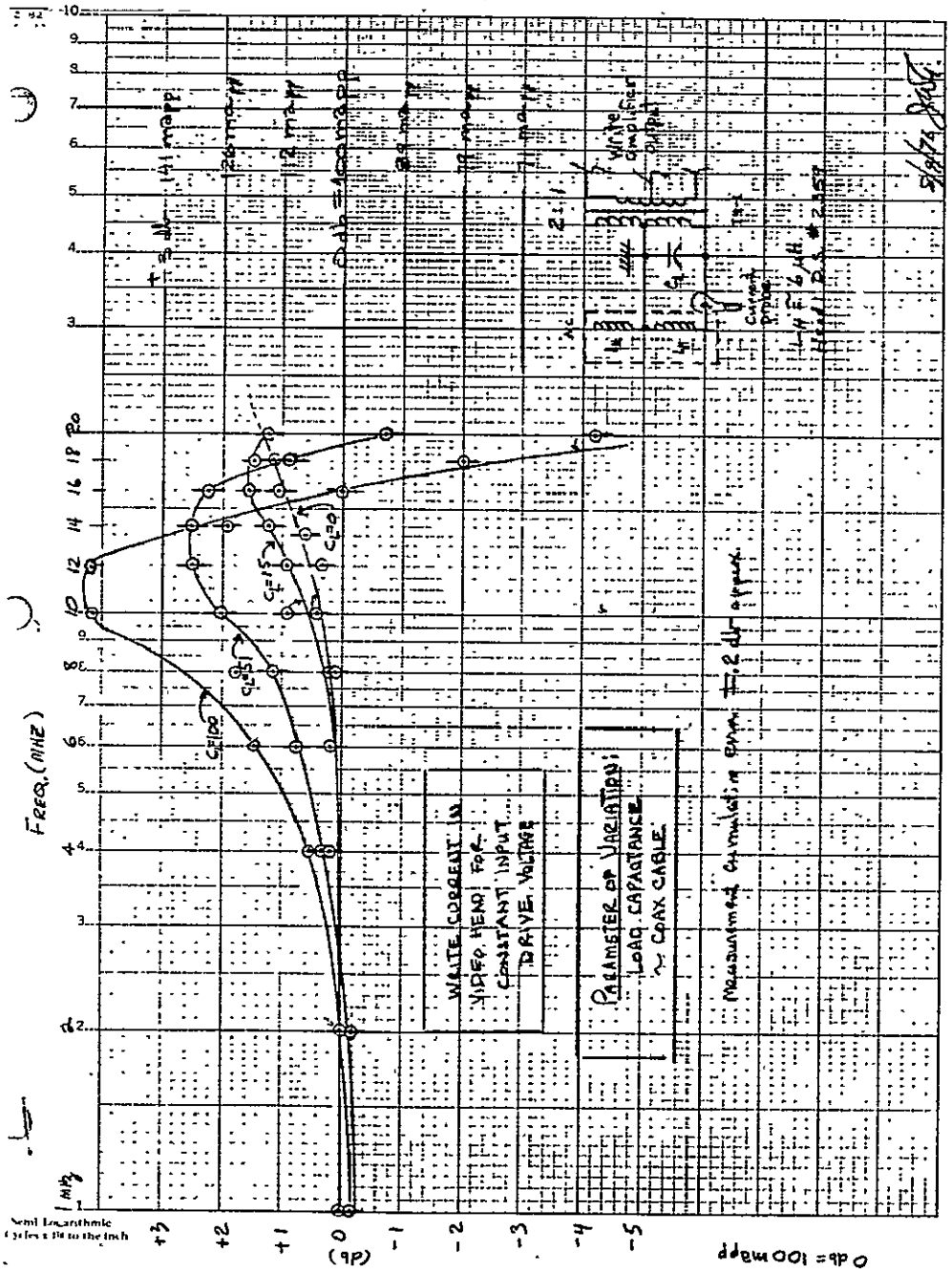

Figure 2.37. Video Head Response for Various Shunt Capacitive Loads.

recorded from DC-20 MHz for various capacitive loads as shown. It can be seen that increases in drive current occur at higher frequencies, for capacitive loading, which is quite reasonable to compensate for head losses. Since expected cable runs are less than 3 feet, a net maximum boost of 2 db is anticipated at 10 MHz. Low capacitance (13 pf/foot) shielded twisted pair cables were selected to connect the heads to the head output transformers. Figure 2.38 shows final write amp performance over a 30 db dynamic range of input signal. The write amp transfer function sensitivity is approximately 50 ma p-p/V_{p-p} input drive.

Fast switching diodes (IN914B) are used throughout the head switch diode arrays to insure flat frequency response and high reverse isolation (low reverse capacitance). Full write current is induced within < 1 μsec during a head-switching sequence, assuring very small glitches in the readback FM spectrum.

It should be noted that wideband FM systems for video recording are particularly sensitive to second-order harmonic distortion.[12] At drive levels of 120 ma_{pp} to the head winding, 2nd harmonic distortion is -55 db or better from 2-10 MHz; 3rd harmonics are down 30 db.

2.4.8 Read Amplifier

The read amplifier front end, a casode bipolar pair, is coupled to the head switch by another wideband transformer, which serves to convert the low level (∿1 mv) differential readback signal

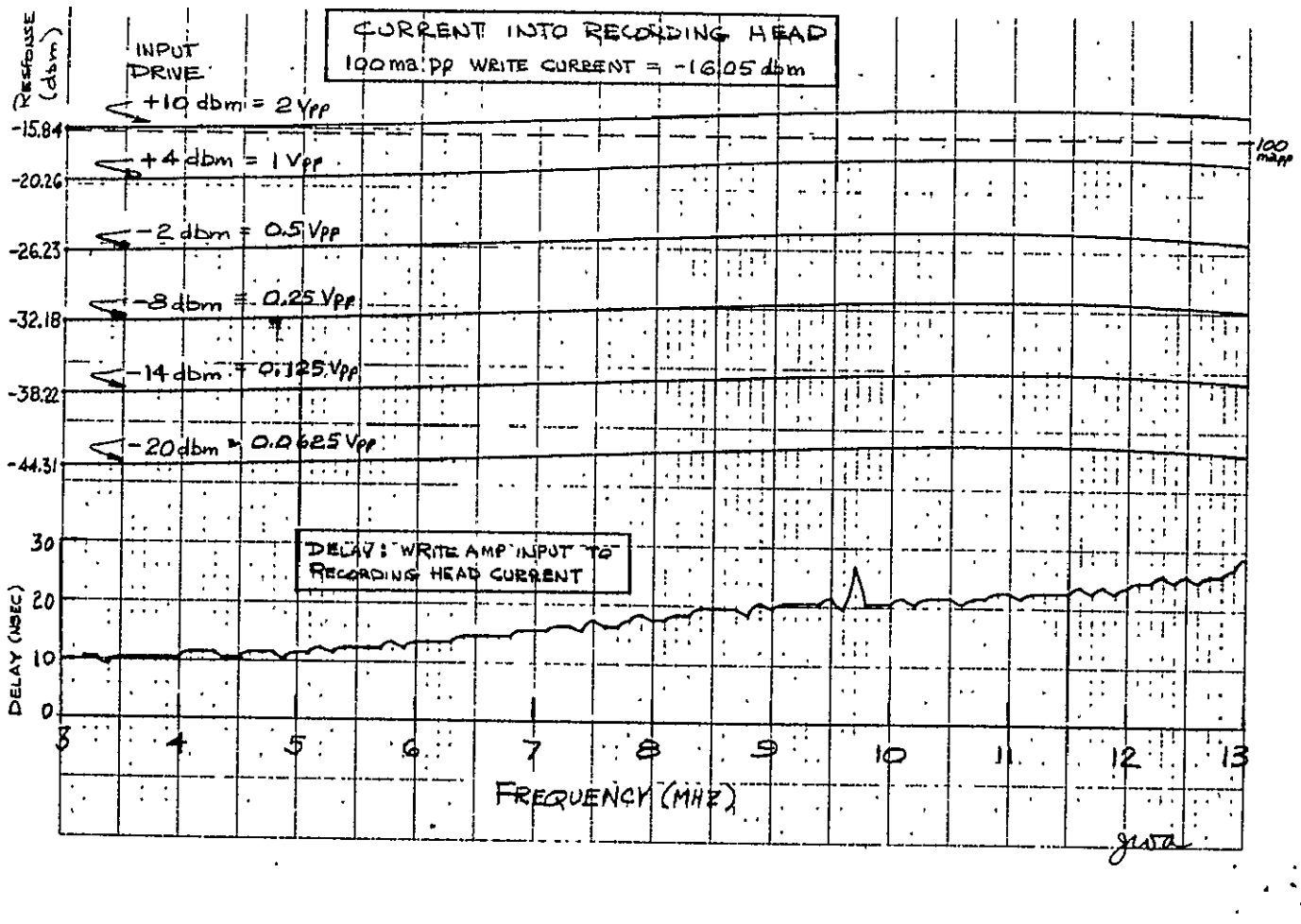

Figure 2.38 Write Amp Current Respose: Magnitude Linearity and Group Delay

to a single-ended signal to minimize input amplifier noise contributions. After preamplification the signal is fed to a wideband, two channel amplifier which serves to increase the signal level to approximately 1 volt rms. Frequency response of the amplifier was measured vs. cable loading at the heads (Figure 2.39). It can be seen that cable capacitance forms a resonant circuit with the head inductance causing slight peaking of the output voltage, which is desirable. Response is flat + 0, -0.5 db to 10 MHz for about 30 pf of loading. The - 3 db point occurs at 14 MHz for virtually any loading under 56 pf, well within the requirements for the FM spectral distribution.

The second channel of the wideband amplifier is used to route the FM signal to the demodulator circuits during recording and provides a direct connection (termed "E to E") between the modulator and demodulator processing circuits. The head switch diode bridge provides sufficient isolation of the read amplifier input circuitry to avoid damage to the front end during the record mode.

These amplifier sections arefollowed by a low pass filter to remove noise and harmonic distortion products prior to limiting and demodulation. An equiterminated transitional (Gaussian to - 6 db) sixth order loww pass filter (LPF) was designed with a cut-off (-3 db) frequency of 10 MHz[13] (see Figure 2.40 for normalized attenuation characteristic). This type of filter combines relatively steep rolloff beyond cutoff with flat delay within the pass-

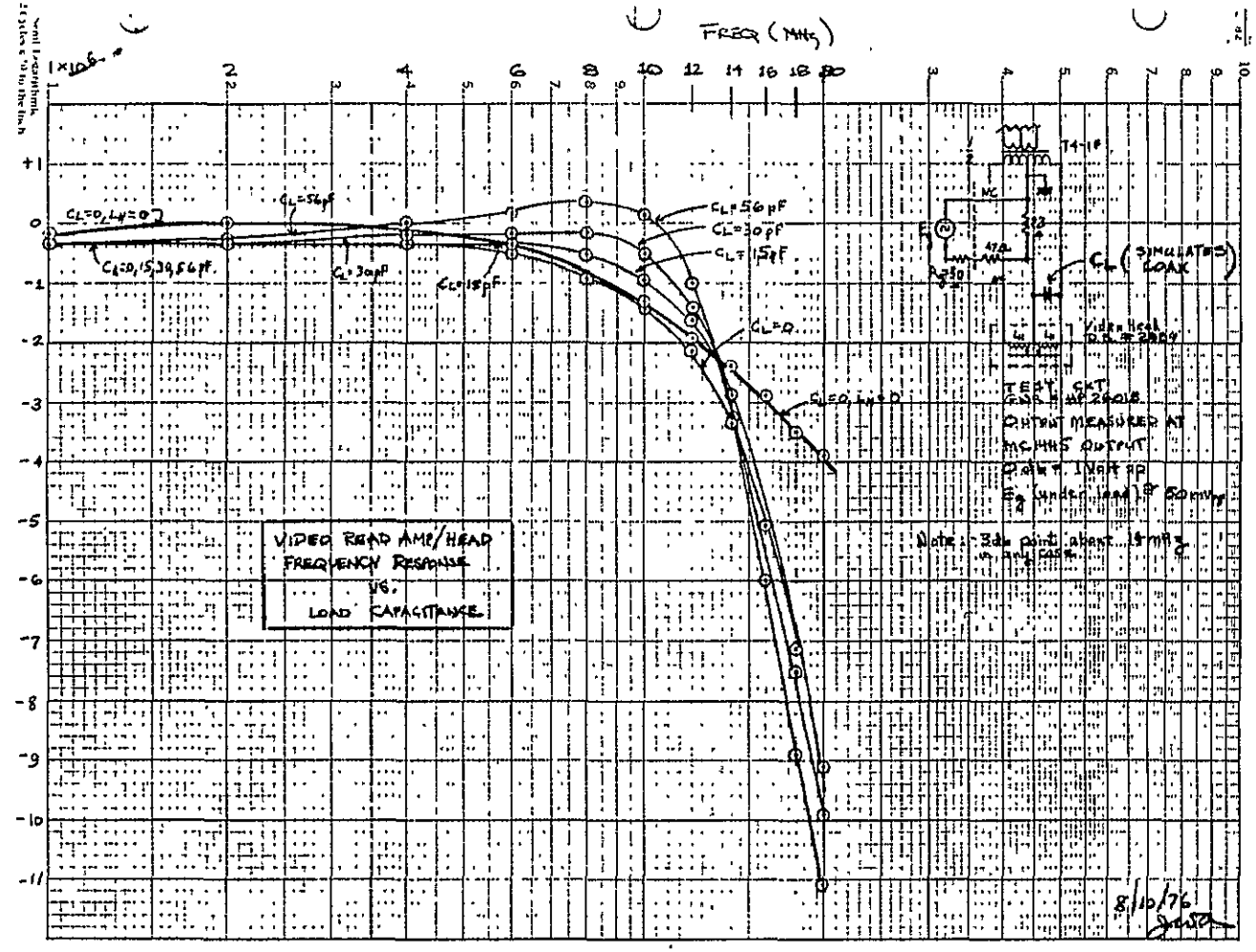

Figure 2.39. Final Read Amp/Head Response for Various Shung Capacitances.

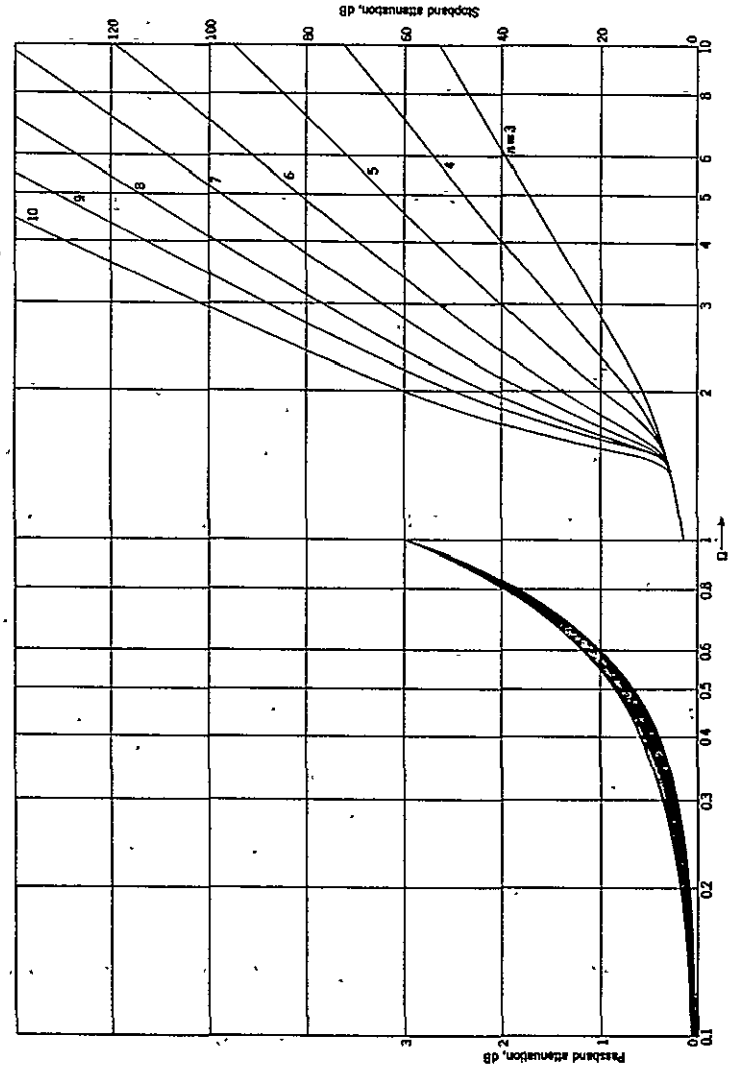

Figure 2.40. Normalized Attenuation Characteristics for Transitional Filter (Gaussian to 6 db.)

band (Figure 2.41); the maximum delay occurs well outside the passband at ∿ 15 MHz. Theoretical passband delay is 60 nsec ± 3 nsec. The filter is driven and loaded by ∿ 620Ω (equiterminated for minimum sensitivity to component variations). Gain and delay characteristics of the actual circuit were measured and are shown in Figure 2.42 . An emitter follower buffers the filtered signal and drives a coaxial cable leading to the demodulator electronics.

2.4.9 Modulator/Demodulator Electronics Configuration System Overview

Figure 2.43 illustrates the card interconnections for the video memory function of the transmit terminal. The modulator subgroup consists of boards 106 A/P, 105 A/P, and 32A, which feed wideband FM to the R/W electronics on 57A. The input board (106 A/P) is a video PROC AMP that strips synchronizing information from the baseband signal, clamps the video signal sync tips to ∿ OV and adjusts the amplitude to approximately 700 mVpp. Clamping is necessary to prevent picture luminance level variations from affecting the FM resting frequency, corresponding to video blanking. This board also has provision for pre-emphasizing the high-frequency picture content for S/N improvement after FM demodulation. The next process step is performed in the VIDEO AMP (105 A/P) which contains a delay-equalized low-pass filter, gain, and biasing controls to set the ac and dc levels of the pre-emphasized video prior to modulation. The ac signal level controls peak-to-peak FM deviation and the dc bias point sets the frequency corresponding to

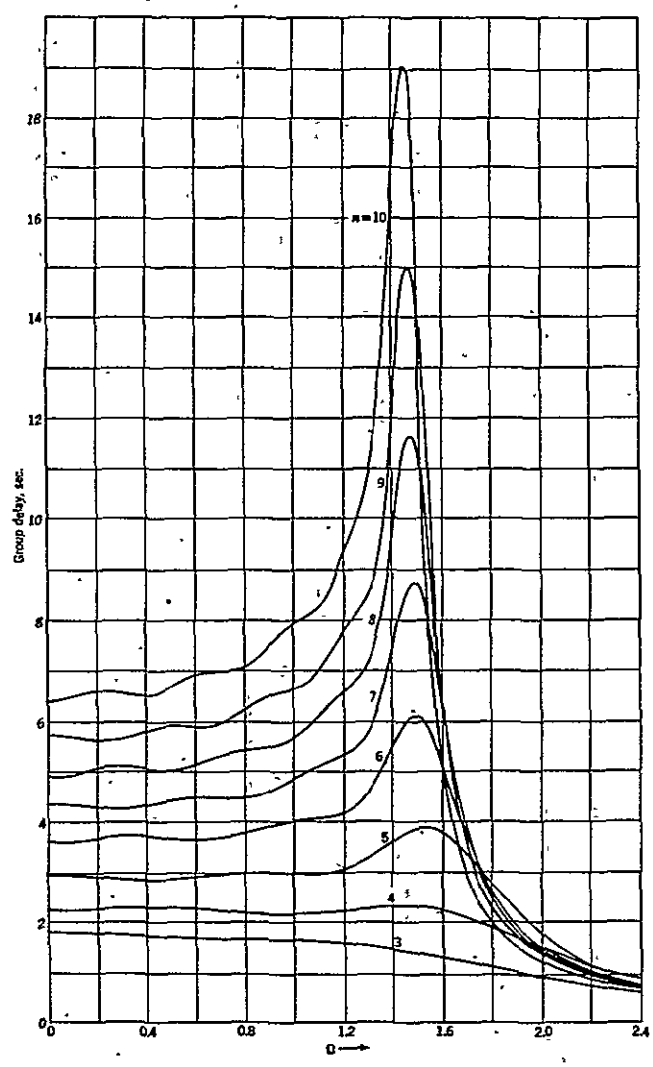

Figure 2.41. Normalized Group Delay Characteristics for Transitional Filter (Gaussian to 6 db.)

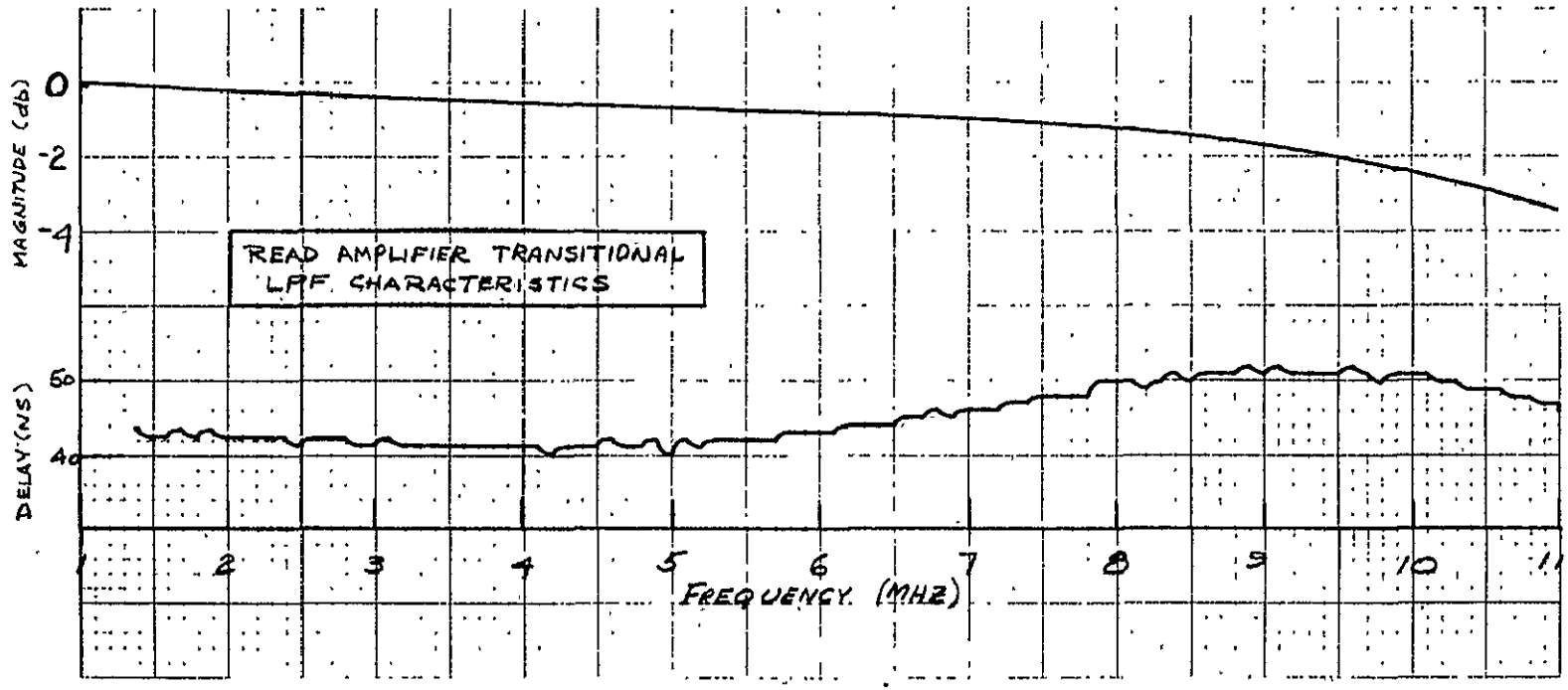

Figure 2.42 Measured Magnitude Response and Group Delay of Read Amplifier Transitional LPF

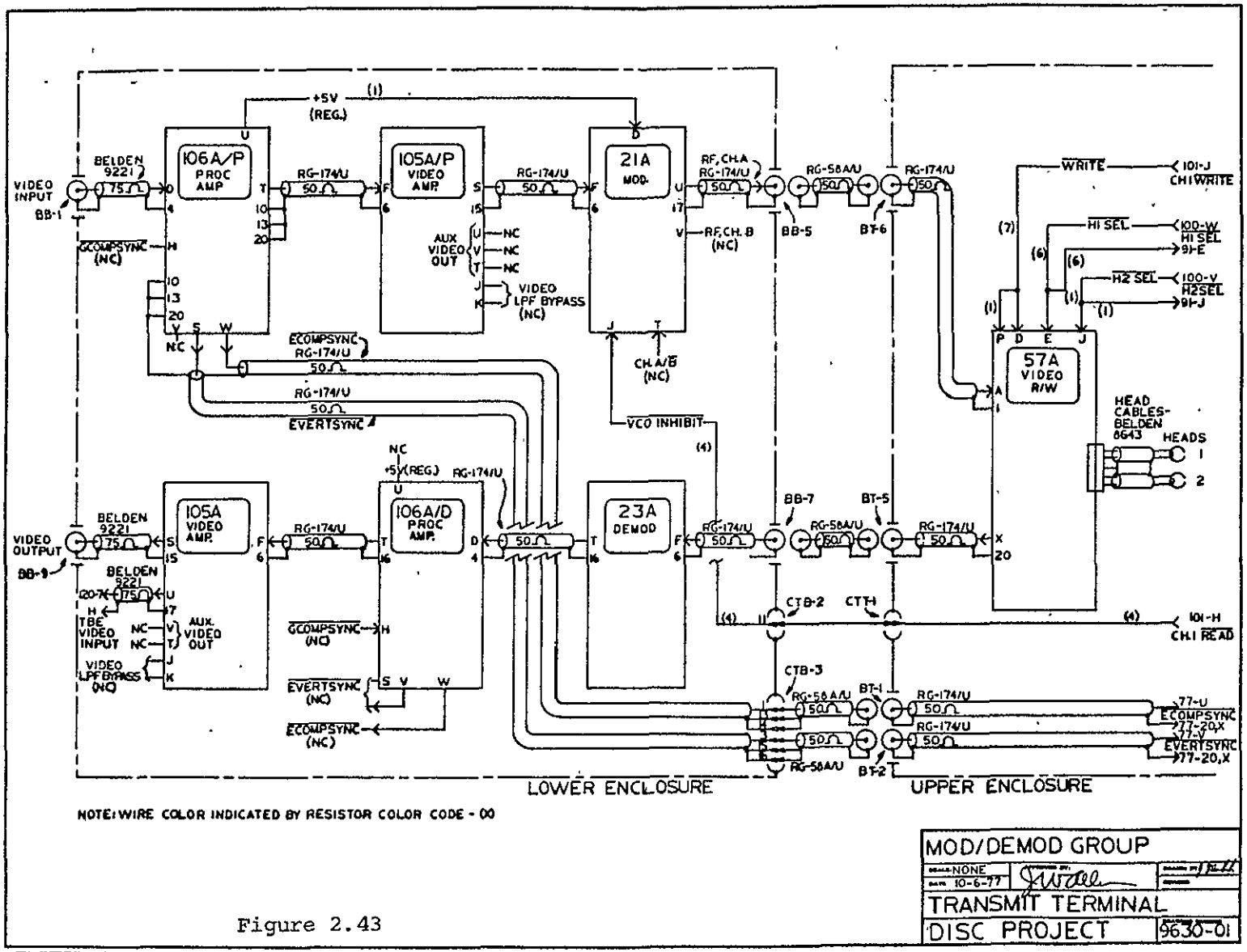

Figure 2.43

blanking, which remains fixed, independent of picture content. Low-pass filtering is necessary to prevent the production of extraneous high-frequency sidebands in the modulator. The MOD (21A) contains a voltage-controlled oscillator, linear-phase filtering circuits, an RF buffer amplifier, and channel select relay. Filtering circuits remove harmonics from the TTL-generated carrier prior to power amplification to drive the coaxial line feeding 57A. The relay allows either of two R/W amplifiers to be driven by the modulator, a feature necessary only in the receive terminal (see Figure 2.44), since it must have two independent video memories. It should be noted that the receive terminal modulator sub-group is driven directly by the high-speed D/A converter, so no signal clamping is necessary. The LINE WRITE CTL (130) performs channel selection and signal routing functions to allow "reading" one channel while the other is being written, line-by-line, into the memory as the encoded picture information arrives at the terminal.

The demodulation process is nearly identical in each terminal, consisting of a DEMOD (23A), PROC AMP (106A/D), and VIDEO AMP (105A). The DEMOD contains a balanced RF limiter, frequency doubler, high-speed one-shot, baseband LPF, and video preamplifier. Frequency doubling is necessary to translate the carrier energy to frequencies above the video baseband, which extends to approximately 4 MHz.

The high speed one-shot and LPF act as a pulse-counting discriminator,[15] providing an output voltage proportional to instantaneous frequency. Such circuits are capable of high linearity

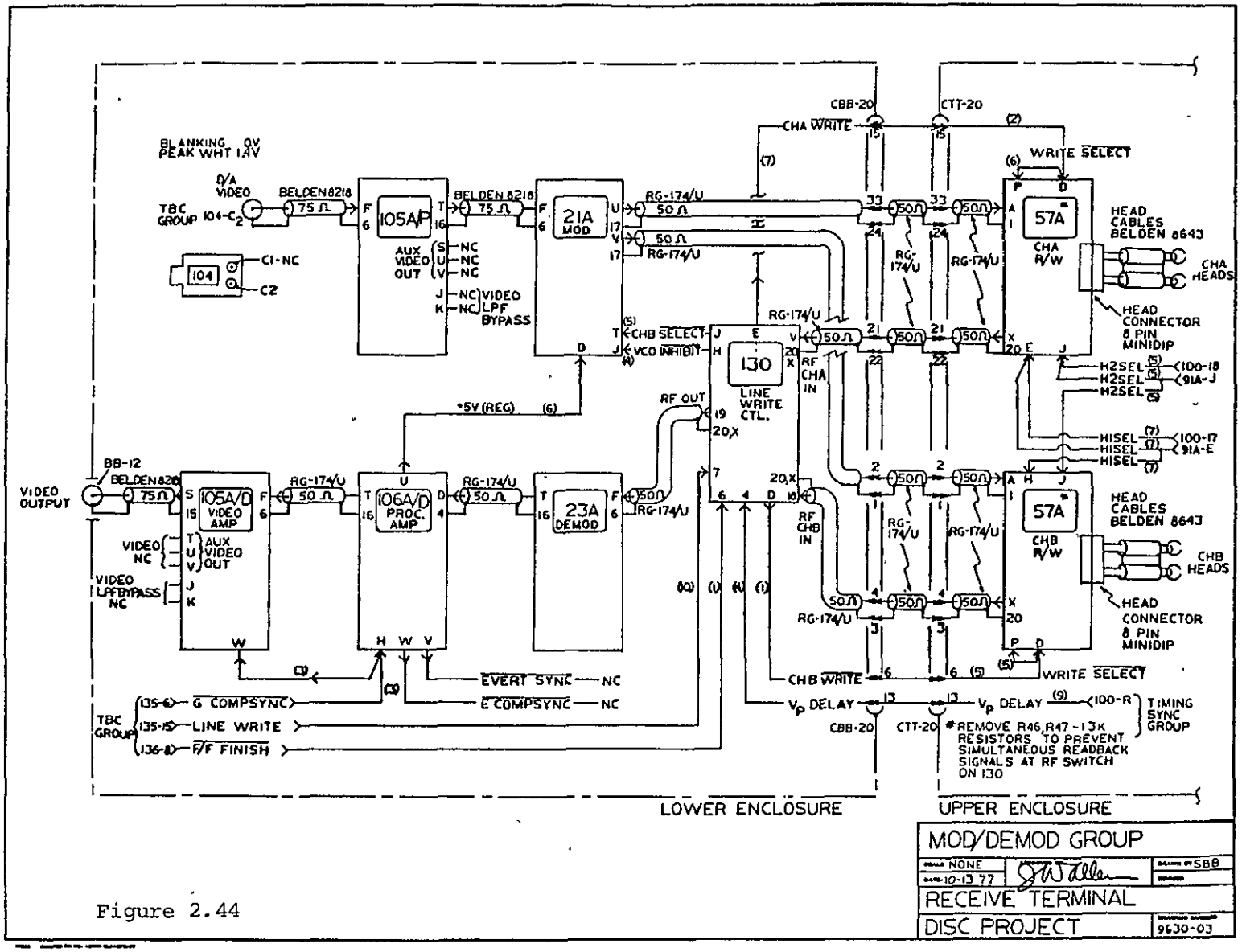

Figure 2.44

(better than 0.1%) with frequency deviations approaching the carrier frequency - a particular requirement for wideband FM video demodulation. The low-pass filter, which rejects unwanted carrier from the demodulated video, feeds a preamplifier that raises the signal level to approximately 1 Vpp. Video clamping (dc restoration) and de-emphasis are performed on the PROC AMP (106A/D) which feeds the buffer amplifiers and LPF on the VIDEO AMP (105A). Additional carrier filtering, performed on 105A, is necessary to reduce the FM carrier amplitude sufficiently to provide an output video signal/carrier ratio in excess of 60 db.

The receive terminal demodulator (Figure2.44) operates in a similar fashion with two exceptions. Because only luminance information is written into the memory, the demodulated signal contains no synchronizing information. Composite sync ($\overline{\text{GCOMPSYNC}}$): 1) activates 106A/D's clamp circuits, and, 2) is added to demodulated video on 105A to produce a standard composite video signal capable of driving a television monitor. Subsequent sections will examine board functions, design techniques, and performance specifications in greater detail as they relate to transmit and receive terminal applications.

2.4.10 PROC AMP (106 A/P, 106 A/D)

The processing amplifier card is used, with slight functional variations, in the transmit modulator and in transmit and receive demodulator sub-groups (Figures 2.45,2.46,2.47). The input video amp

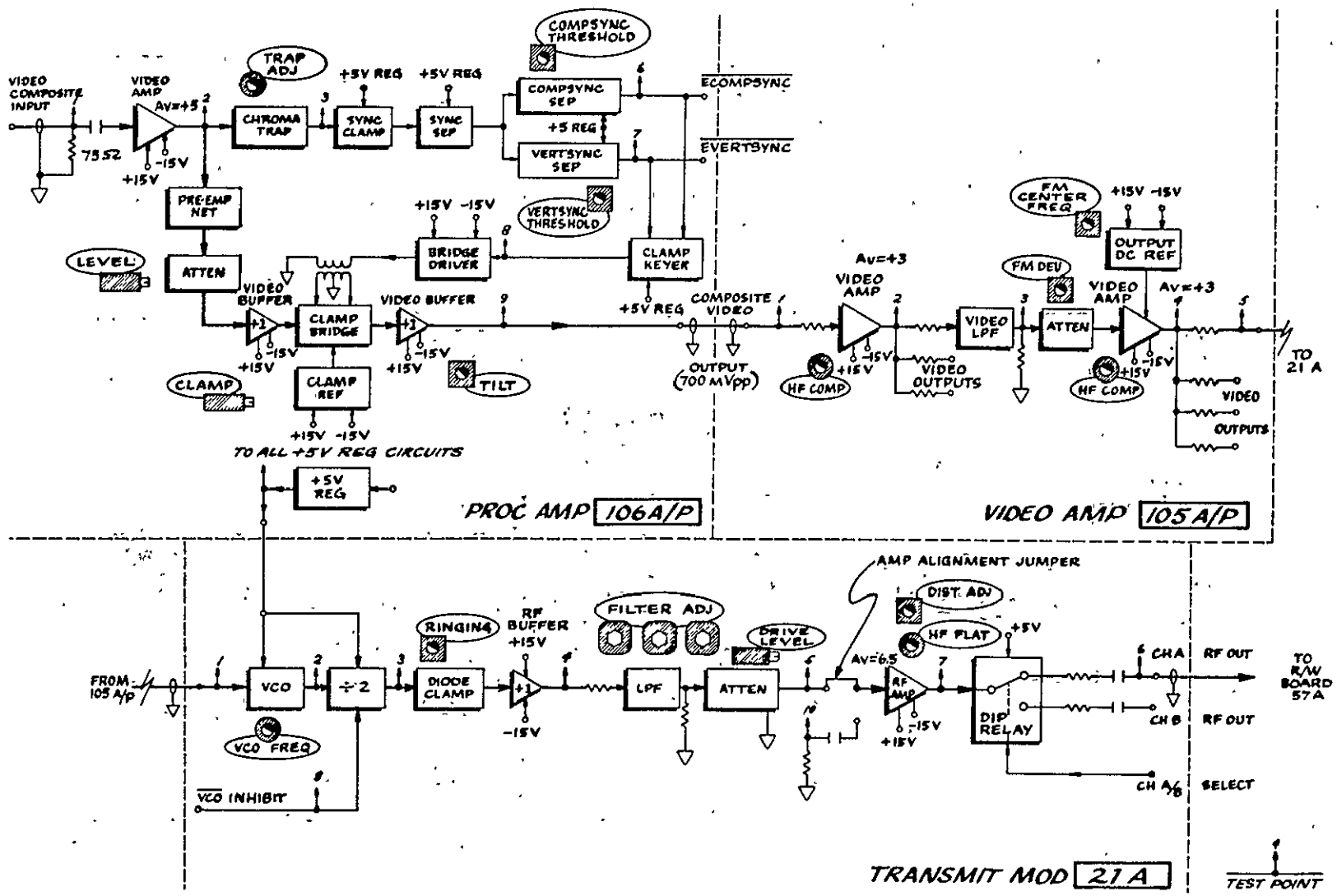

Figure 2.45. Funcational Block Diagram for Transmit Mod Group.

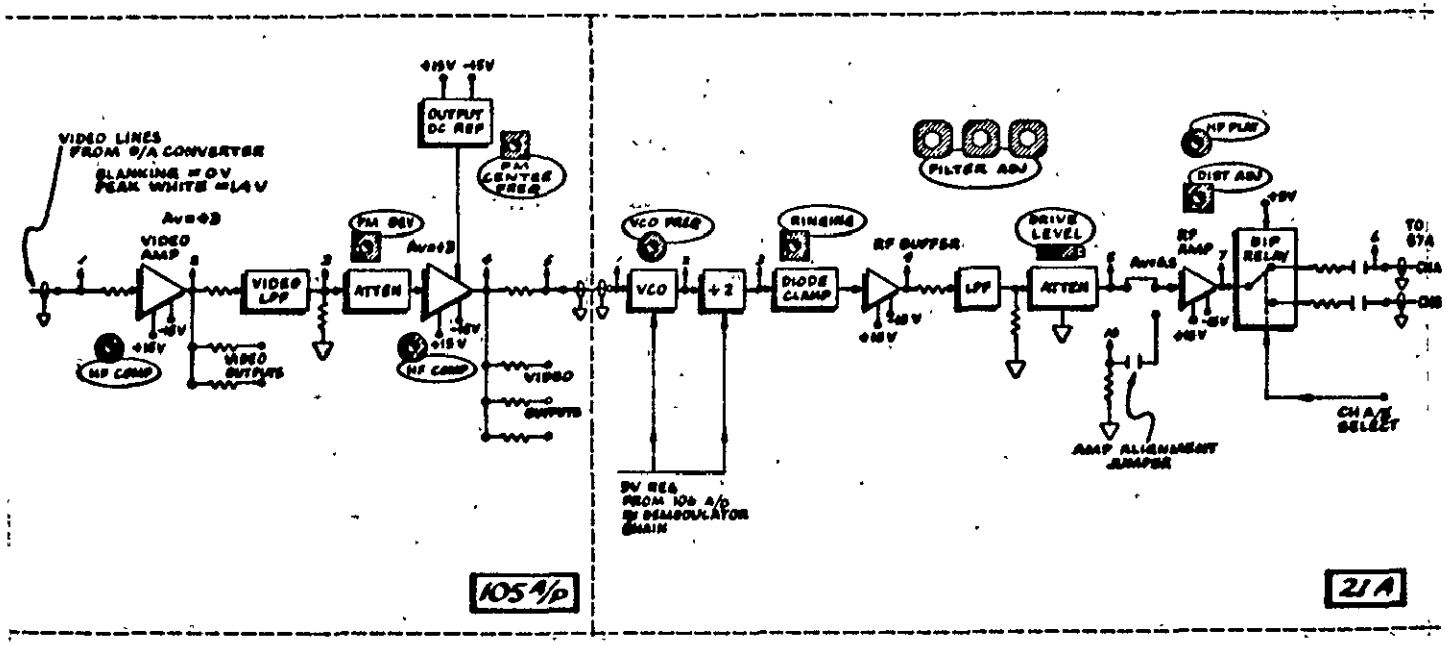

Figure 2.46 Functional Block Diagram for Receive Mod Group

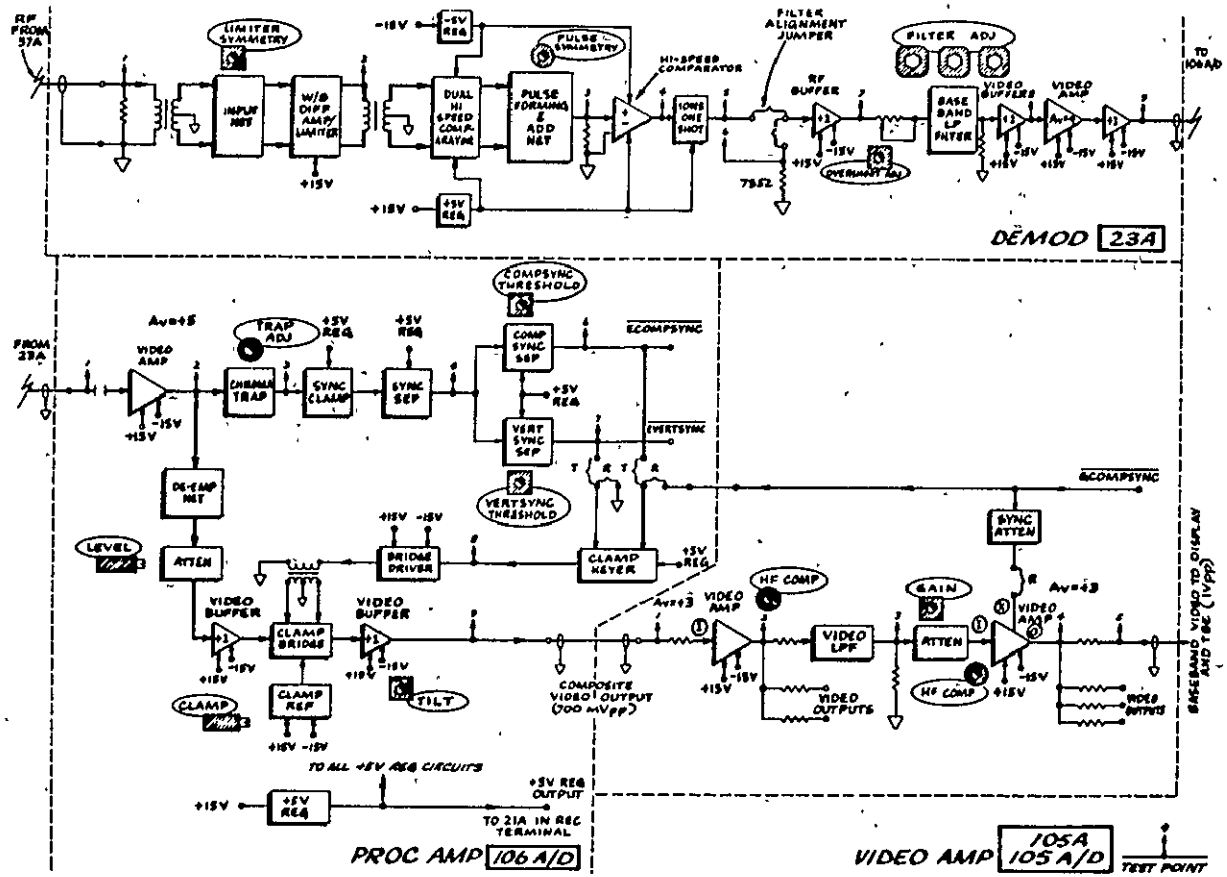

Figure 2.47. Functional Block Diagram for Demod Group.

is an ac-coupled wideband video amplifier using a high frequency transistor array (RCA 3046 or 3086) and additional discrete transistors (see Appendix A2.8 for schematic). After amplification, nominal video signal level at TP2 is 8 Vpp . This point feeds two separate paths: 1) the sync separator and 2) video clamp and output stages.

The sync separator section consists of a passive series resonant chroma trap, to remove possible color information from the sync region, an active clamp to amplify only that portion of the signal occupied by sync, and twin composite and vertical sync separators. A 5 volt TTL compatible sync-pulse train (TP4) is fed directly to the compsync separator, a fast comparator ($\frac{1}{2}$LM319). The same signal, after low-pass filtering to reject all but the vertical sync region, feeds the other comparator in the chip. Power for the sync separator circuits, comparator and comparator reference threshold circuits is derived from a separate +5v regulated supply, to insure stable operation for varying analog supply bus voltages ($\pm$ 15v nominal), and to isolate the bus from switching glitches. TTL compatible outputs are provided for external use and also key a 1.2 µsec one-shot (clamp keyer) which is fed, after amplification, to a phase-splitting transformer, providing simultaneous pulses of opposite polarity and equal amplitude. These pulses are used to turn on diodes (2-1N916) in the clamp bridge for the 1.2 µsec clamping interval. The clamp reference voltage is buffered from a resistive divider also connected to the +5V reg power bus.

Figure 2.48 shows the 1.2 μsec clamp action on the horizontal sync pulse.

Video from TP2 is ac-coupled to the pre- or de-emphasis network (suffix on board number P,D indicates which option is in use), loaded by a resistive attenuator to set the peak-to-peak output level. An emitter follower buffers this signal to the clamp capacitor - which is connected to the bridge output. Signal is extracted from the clamp via a second follower with a TILT adjustment potentiometer to compensate for finite base currents and leakage. Typical specifications follow in Table 2.9.

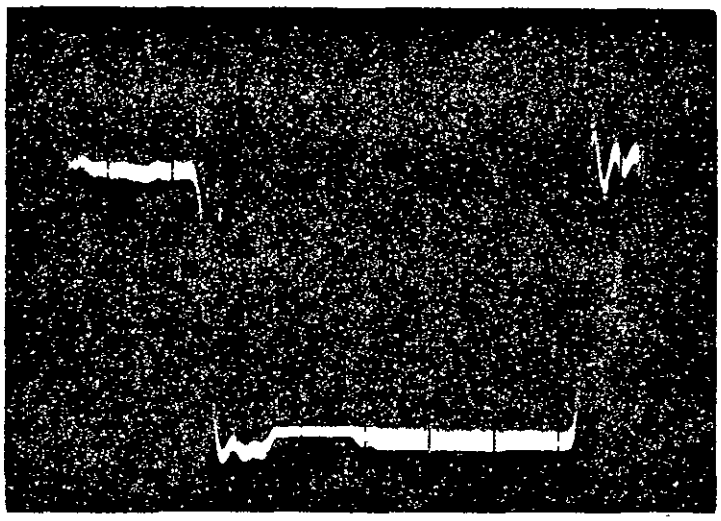

Figure 2.48 Clamp Artifact

2.4.11 VIDEO AMP (105A)

All 105 video amplifier cards consist of an input wideband video buffer amp, a 75Ω equiterminated delay-equalized LPF, and an identical output buffer (Figures 2.45,2.46,2.47). Each buffer amp

TABLE 2.9

106A PROC AMP PERFORMANCE DATA

Input impedance	75Ω ± 5% or bridging > 5KΩ
Input signal level (ac)	0.5 - 2.0 Vpp composite video
Input dc level	< ± 10 VDC
Output signal level (ac)	700 mVpp (nominal)
Output signal level (dc)	-0.5 to +4.5 Vdc (0V nominal)
Frequency response	dc to 4.2 MHz ± .2 db
Max. Diff Gain @ 3.58 MHz	1.5% (any APL)
Max Diff Phase @ 3.58 MHz	2° (any APL)
Hum Rejection	> 30 db
Tilt @ 60 Hz	< 1%
"K" rating[16]	< 1%
Power Supply Rejection	< 1% change in any parameter for ± 13 to ± 17 VDC analog supply bus variation
Linearity (stairstep)	< 1%
Pre/De-emphasis	0.5 µsec, 6 db @ 4.2 MHz
Sync separator:	
outputs	composite sync ($\overline{\text{ECOMPSYNC}}$) vertical sync ($\overline{\text{EVERTSYNC}}$)
video S/N for error - free sync (minimum)	25 db

(see Appendix A2.8 for schematic) has an open circuit voltage gain of ∿ 3 which is flat ± .1 db. to 5 MHz. A small trimmer capacitor (7-25 pf) at the inverting input allows adjustment of the compensated feedback attenuator.

The video LPF is delay-equalized to preserve transient response while retaining flat passband and steep skirt rolloff characteristics. Magnitude and delay transfer functions, measured on an HP3570A network analyzer, are shown in Figure 2.49 . Delay variation over the video passband is less than 8%, adequate to insure a "K" factor rating[16] of approximately 0.5% for either pulse or bar test waveforms.

Amplifier gains more than compensate for the fixed 6 db insertion loss of the equiterminated filter. A variable attenuator on the input of the second buffer amplifier allows overall voltage gains from 0 to 2.25 to be realized when driving a 75Ω load; the nominal gain is ∿ 1.4 to raise the 700 mVpp PROC AMP signal to 1.0 Vpp. Overall board specifications appear in Table 2.10.

2.4.12 VIDEO AMP (105 A/P)

This version of 105, found in the transmit and receive terminal modulator subgroups (Figures 2.45 and 2.46) differs from 105A in that the output buffer amplifier has a variable dc offset (+3 to +6 V) which allows biasing the VCO on the MOD board (21A). By adjusting the clamp reference on 106 A/P for blanking at 0V at TP3 on 105 A/P, the dc biasing sets the FM frequency corresponding

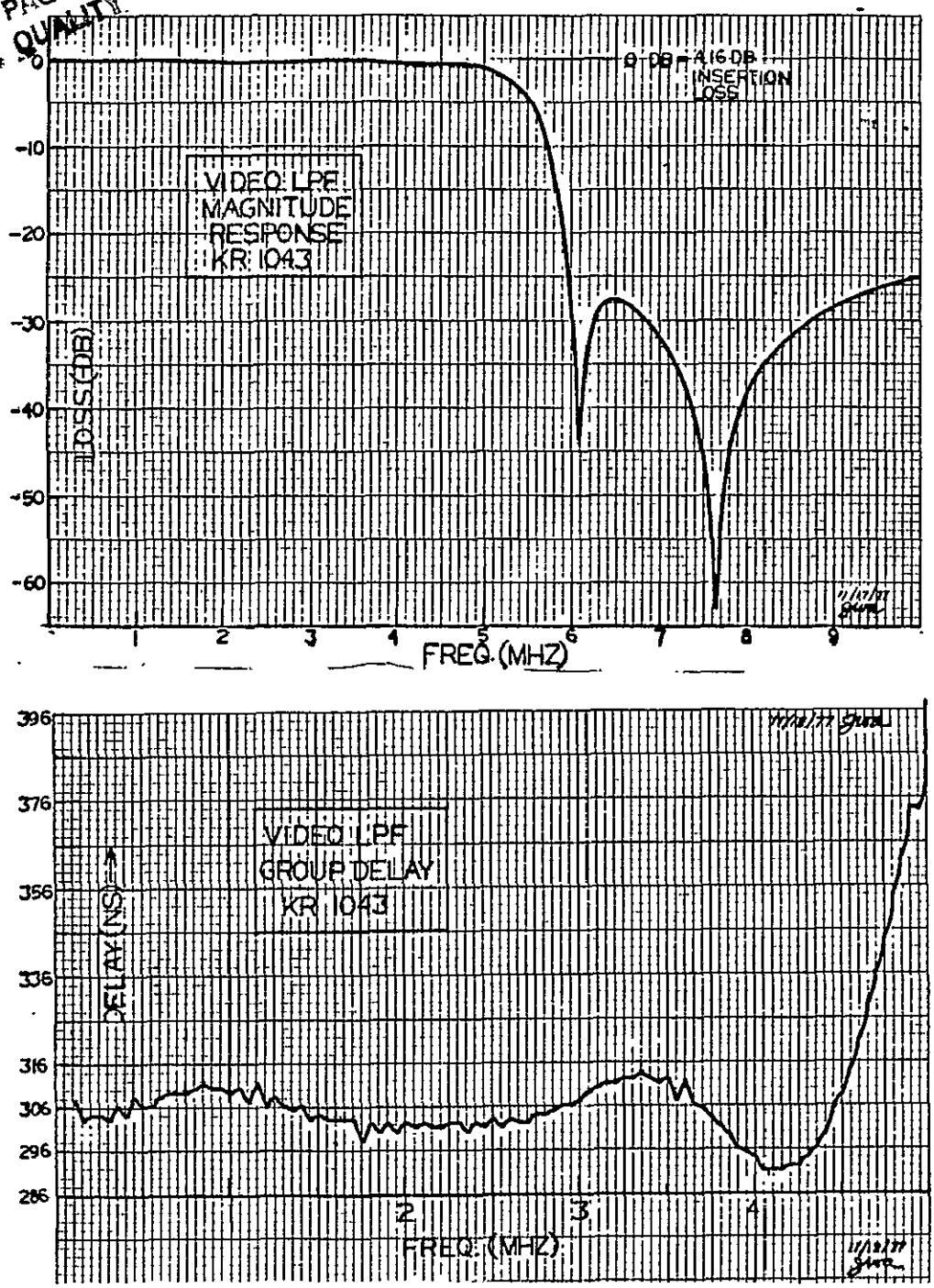

Figure 2.49. Measured Magnitude Response and Group Delay of KR1043 LPF.

TABLE 2.10

105A VIDEO AMP PERFORMANCE DATA

Input Impedance	75Ω ± 5% or bridging > 5KΩ
Input signal level (nominal)	700 mVpp composite video
Input dc level (nominal)	blanking @ 0VDC
Output Impedance	75Ω ± 5%
No. of independent filtered outputs	4
Output Blanking level	0VDC (105A, 105A/D)
	∿ 4.5 VDC (105 A/P)
Output signal level	1 Vpp composite video (105A,105A/d)
	0.8 Vpp composite video (105 A/P)
Frequency response	dc to 4.2 MHz ± 0.3 db
Max. Diff Gain @ 3.58 MHz	< 0.5% (any APL)
Max. Diff Phase @3.58 Mhz	1° (any APL)
Total Delay @ 3.58 MHz	340-355 nsec
Hum Rejection	0 db
Tilt @ 60 Hz	< 1%
"K" rating[16]	0.5% Pulse
	1.0% Bar
Linearity (stairstep)	< 0.5%
Stopband rejection (>6MHz)	25 db or better

to blanking independent of video level. Thus the bias control becomes FM CENTER FREQ and the gain control FM DEVIATION with no mutual interaction. These features are desirable for ease of initial alignment and routine maintenance.

2.4.13 VIDEO AMP (105 A/D)

The receive terminal uses this variation of 105A in the reconstruction of composite video. Composite sync ($\overline{\text{GCOMPSYNC}}$) after attenuation is added to demodulated disc video in the final buffer amp (Figure 2.47) to produce a standard composite video output. The schematic 1f 105 (see Appendix A2.8) shows all of the aforementioned circuit configurations.

2.4.14 MOD (21A)

The video input to the VCO ($\frac{1}{2}$MC4024P), an emitter-coupled multivibrator is dc-biased to yield optimum luminance linearity with sync tips at ∿ 4.0V and a peak-to-peak amplitude of approximately 800 mV. These values produce an output blanking frequency of approximately 12 MHz with peak luminance deviations of 2 MHz. Sync occupies the lower frequencies and luminance the upper regions (see Figure 2.50). The signal passes through a high speed divider ($\div 2$, $\frac{1}{2}$74S112) to suppress even order harmonics due to deviations from a 50% duty cycle in the VCO output waveform.[17] The spectrum at TP4 (Figure 2.51) now contains the desired fundamental and chiefly odd order harmonics as desired. The signal is buffered through a diode clipping circuit and emitter follower which removes frequency dependent amplitude

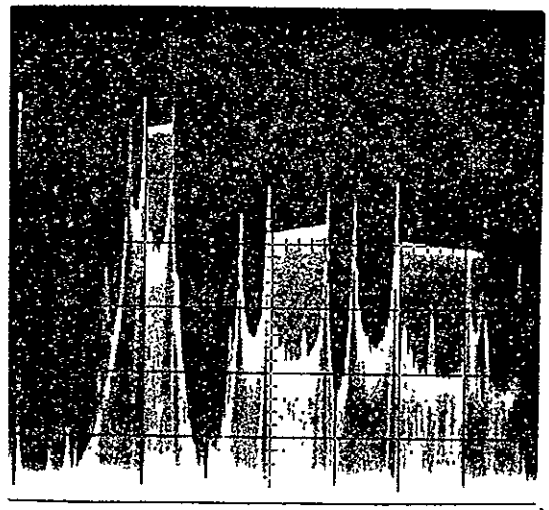

Figure 2.50 VCO Output Spectrum (TP2)
(Full-field Video Ramp Input)

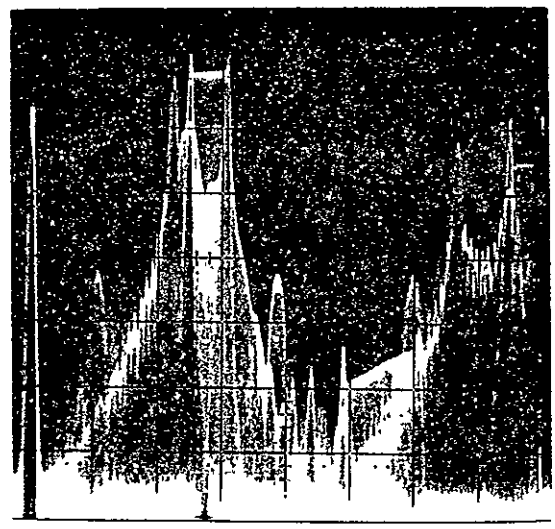

Figure 2.51 Divided VCO Spectrum (TP4)

variations and overshoot due to the extremely fast transition times (∿ 3-4 nsec) in the flip-flop output. Both chips are powered by the +5V regulated supply on the PROC AMP (106 A/P). The procedure avoids spectral contamination of the VCO due to unavoidable glitches riding the +5V TTL power bus. An override low true $\overline{\text{VCO INHIBIT}}$ line is tied to the preset input of the divider flip-flop, used to remove the drive signal to the record electronics during the playback cycle.

Filtering of the FM spectrum prior to output buffering is accomplished with an equiterminated (620Ω) 6 pole linear-phase LPF with .05° equiripple departures from phase linearity to 1.8 times the cutoff frequency of 10 MHz (-3 db).[18] Figure 2.52 shows the theoretical magnitude response and Figure 2.53 the group delay. An attenuator on the filter output sets the input drive level to the wideband RF buffer amp, which ultimately feeds the write amplifier on 57A. The buffer, similar in design to all video amps used in the system has provisions for response flatness adjustment (trimmer cap) and 2nd harmonic distortion minimization (bias pot). A test jumper is included to allow ease of initial settings of these adjustments. (Complete board alignment procedures and schematics are shown in Appendix A2.8).

2.4.15 DEMOD (23A)

The demodulator board receives an unbalanced coaxial input signal which passes via a wideband RF transformer to a balanced limiter (MC1355P). A potentiometer, LIMITER SYMMETRY ADJ, compensates for dc imbalance and nulls the even-order harmonics prior to

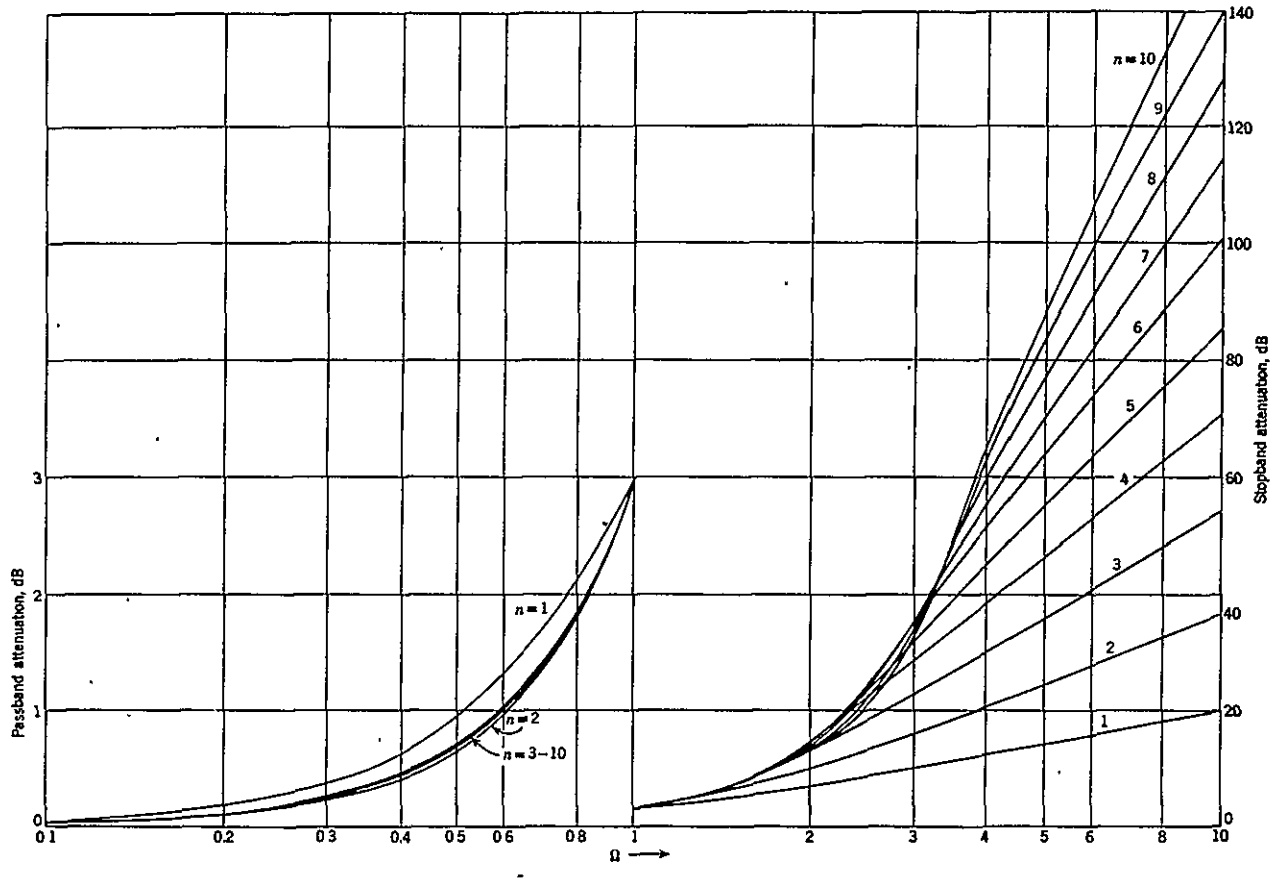

Figure 2.52. Normalized Attenuation Characteristics for Linear Phase with Equiripple Error Filter (phase error = 0.05°).

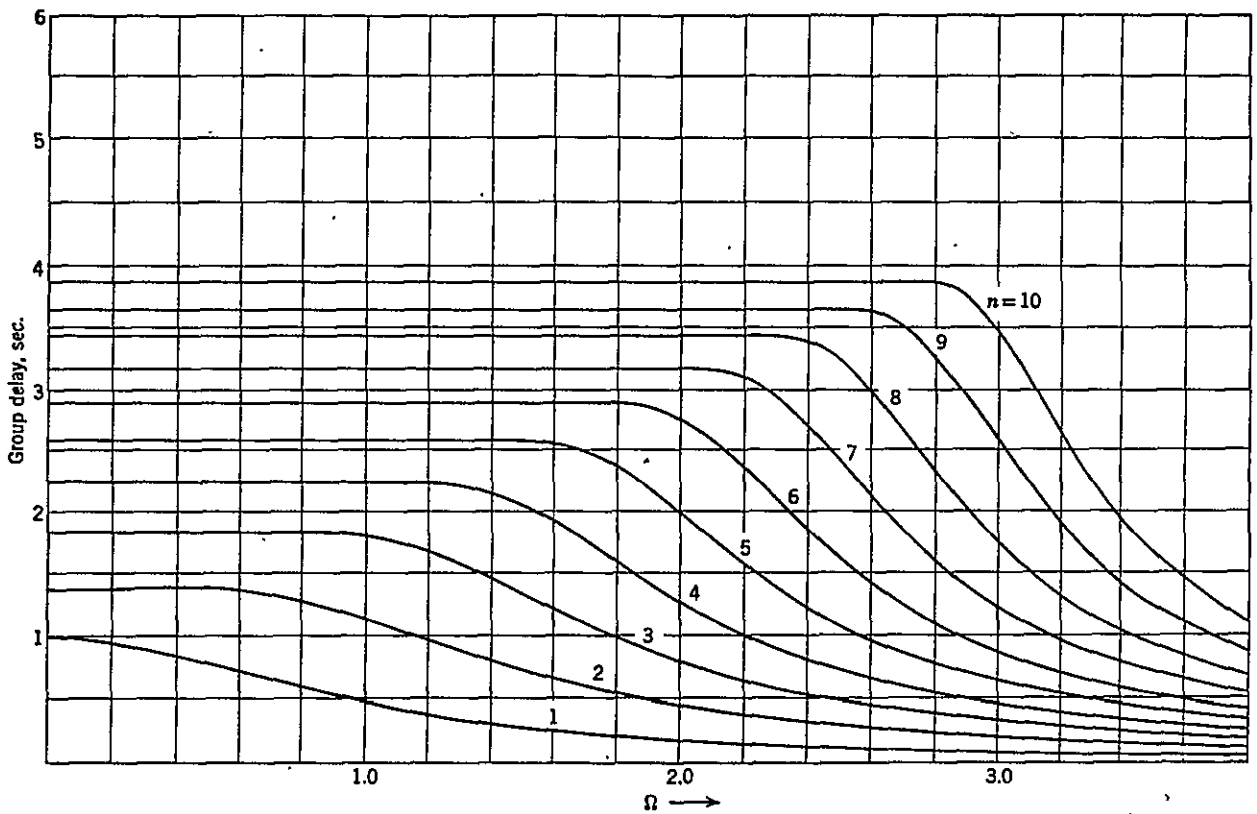

Figure 2.53. Normalized Group Delay Characteristics for Linear Phase with Equiripple Error Filter (phase error = 0.05°).

demodulation. The limited signal is fed via second wideband transformer to a frequency doubler consisting of dual hi-speed comparators, a pulse forming (differentiating) network, pulse adder, and comparator. All comparators operate from separate on-card regulated ±5 VDC supplies to avoid spectral contamination and provide analog supply bus isolation. The resulting output signal triggers a 10 nsec one-shot, which yields a fixed pulse width whose duty cycle varies with instantaneous frequency. At this point FM demodulation occurs (see Figure 2.54). Note the demodulated video baseband spectrum and the doubled carrier energy lying above it. This signal is buffered to a sharp cutoff 7-pole Cauer-Chebyshev LPF.[19] The design parameters for this filter are listed in Table 2.11. Measured magnitude and delay response of the realized filter (HP3570A Network Analyzer) are shown in Figures 2.55and 2.56 respectively. Slight

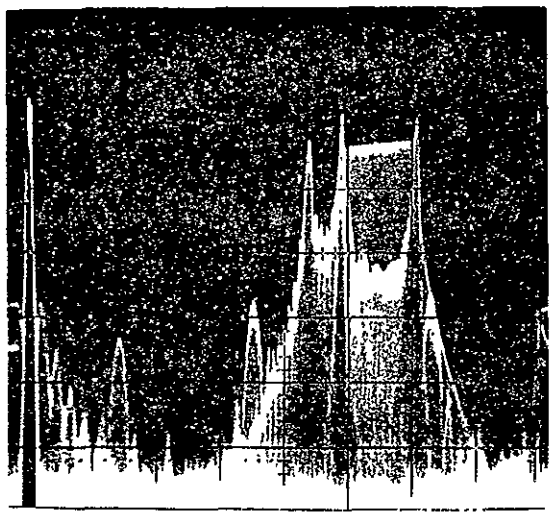

Figure 2.54 One-Shot Output Spectrum

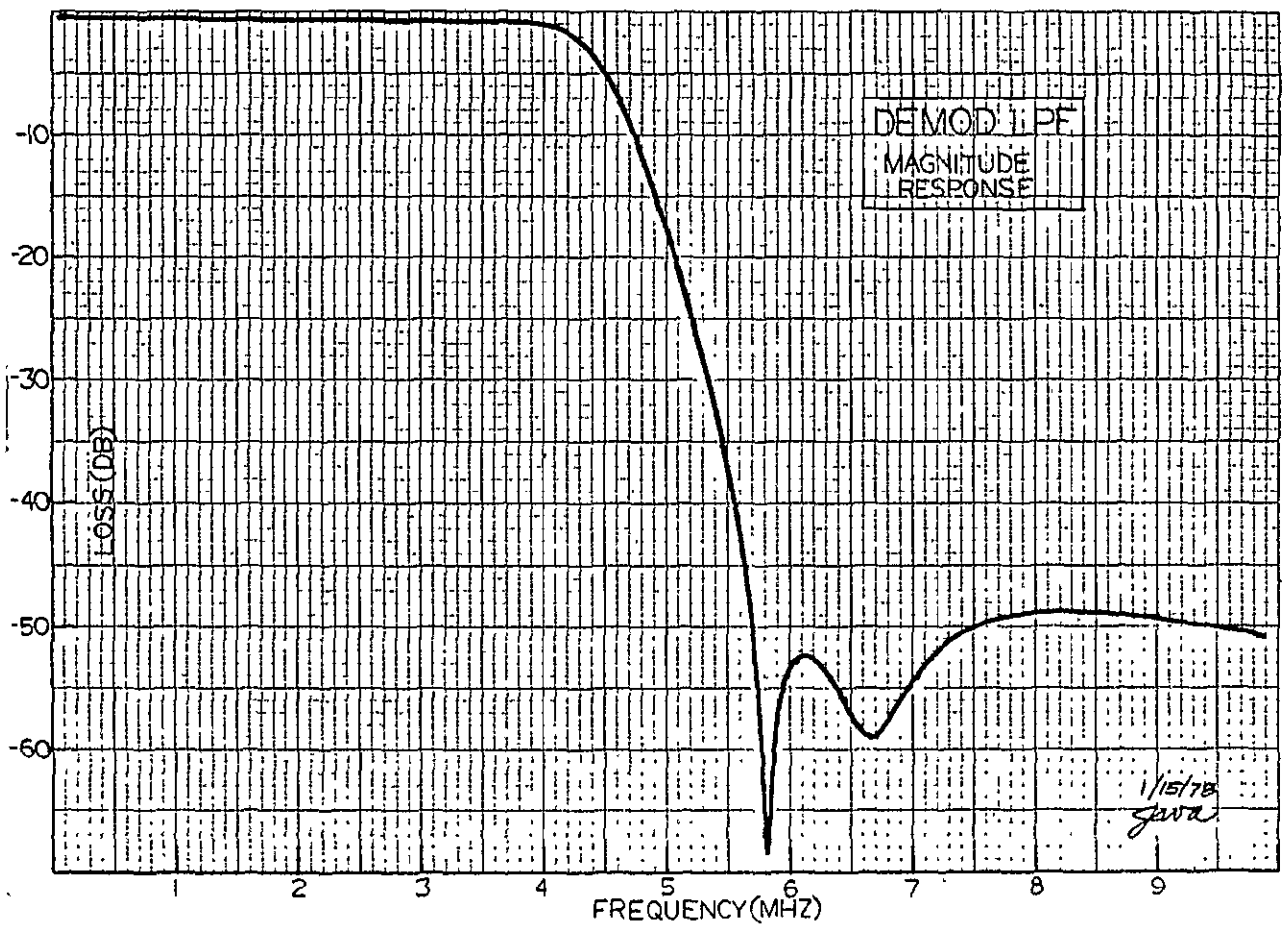

Figure 2.55 Measured Demod LPF Magnitude Response.

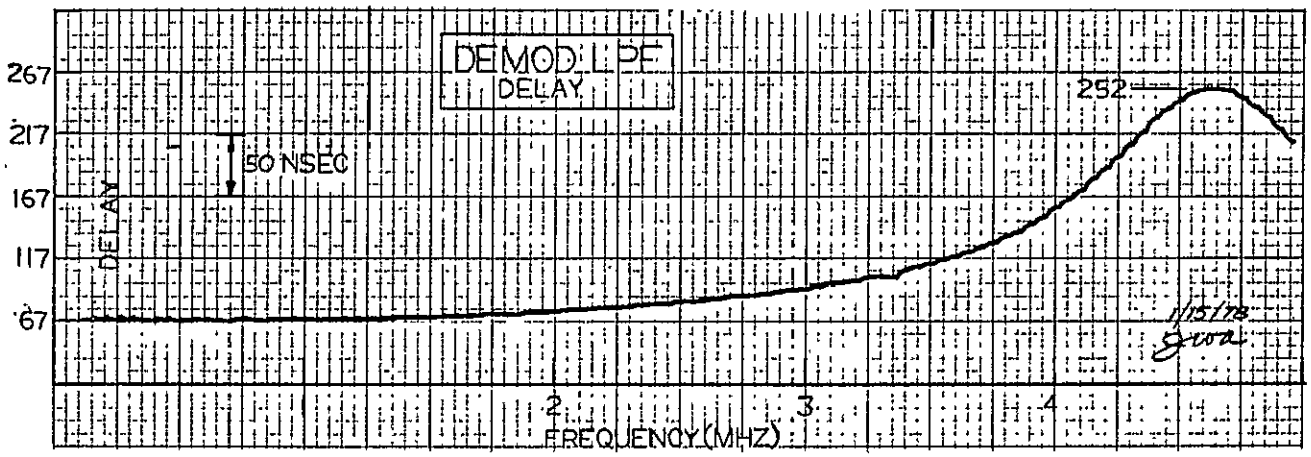

Figure 2.56. Measured Demod LPF Group Delay.

TABLE 2.11

Passband Ripple	.01 db
Passband	dc - 4.3 MHz
Stopband Rejection	50.11 db
Stopband	5.61 Mhz
Reflection Coeff	5%
Drive Impedance	270.18Ω
Load Impedance	∞

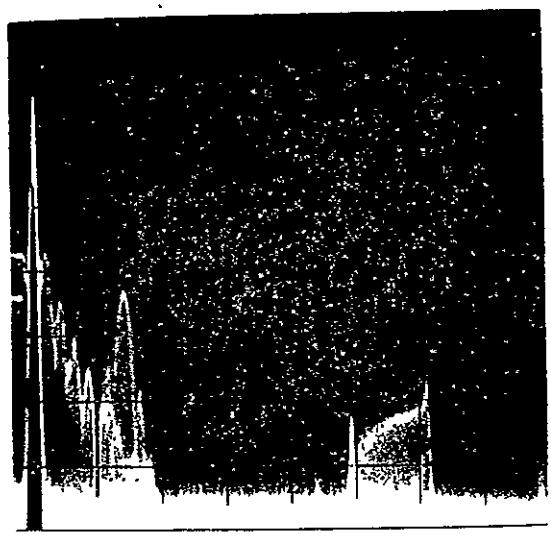

Figure 2.57. Demodulator Output Spectrum (TP9)

variations from design specifications are due to finite achievable tolerances (∿ 1-2%) on components, finite inductor "Q's" (∿ 50), inductor distributive capacitances, and small additional stray capacitances. Figure 2.57 shows the demodulator board output spectrum; note the suppression of the carrier spectrum after low-pass filtering. Circuitry is shown in Appendix A2.8 .

2.4.16 E-E Mod/Demod Performance

The MOD (21A) output was coupled via a 20db 50Ω pad to the DEMOD (23) input; a linear ramp (1 Vpp @ 75Ω) was used to generate all spectra shown for 21A and 23A. Comparison of input and output waveforms of the entire group can be seen below in Figures 2.58,2.59. Slight glitches on the horizontal sync tips are due to the action of

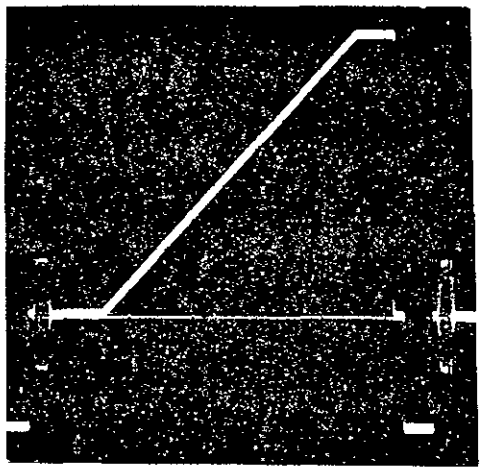

Figure 2.58

Input Ramp

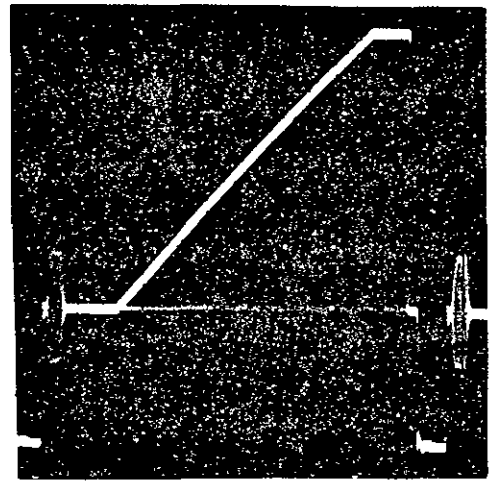

Figure 2.59

Output Ramp

10 μsec/div

1 Vpp @ 75Ω

the keyed-clamps in both PROC AMPS (106 A/P, 106 A/D). The output spectrum (Figure 2.60) is completely free of residual FM carrier due to the final LPF on the VIDEO AMP (105A).

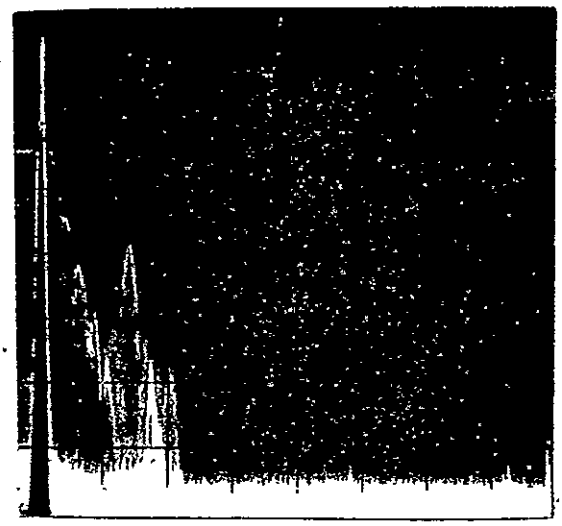

Figure 2.60 Ramp Output Spectrum

Baseband video frequency response is illustrated with a reduced amplitude multiburst test waveform; Figure 2.61 is the 1 Vpp input to the modulator subgroup and Figure 2.62 is the resulting video output from 105 A/D. Slight burst rolloff (∿ 1 db) at 4.2 MHz is primarily due to the action of the DEMOD (23A) LPF. The slow envelope build-up of the high frequency bursts is again due to: 1) band limiting action of all LPF's in the system and, 2) non-uniform group delay of the DEMOD (23A) LPF (see Figure 2.56). The latter effect is more clearly discernable when a transient response test is made; a $\sin^2$ pulse and bar test waveform is generally used (Figure 2.63). The output is shown in Figure 2.64.

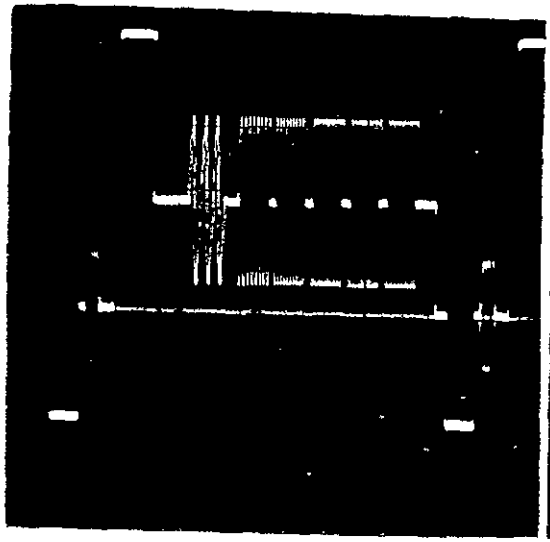

Figure 2.61
Input Multiburst

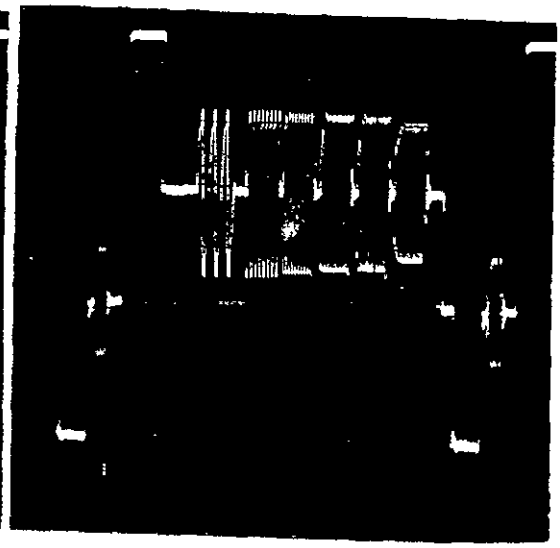

Figure 2.62
Output Multiburst

10 μs/div
1 Vpp @ 75Ω

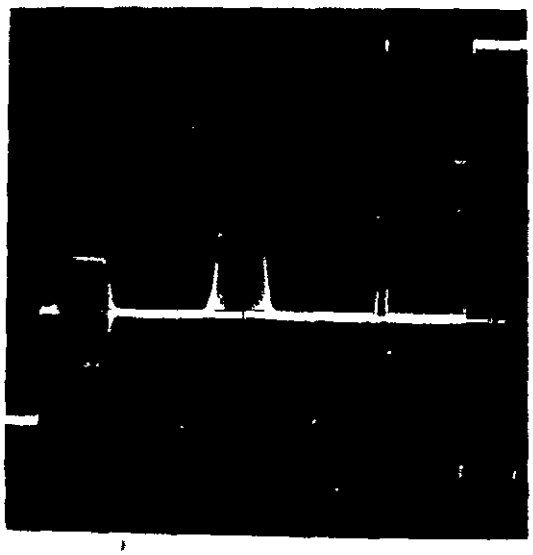

Figure 2.63
Input Sin^2 Pulse and Bar

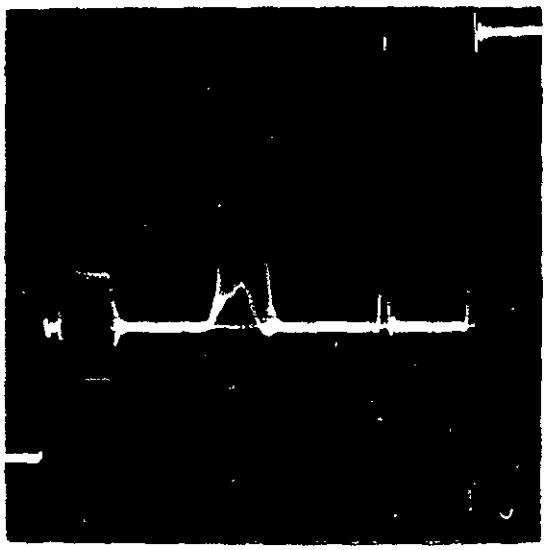

Figure 2.64
Output Sin^2 Pulse and Bar

10 μsec/div
1 Vpp @ 75Ω

Four features of the test waveform (Figure 2.64) should be noted: 1) the color burst reference following horizontal sync, 2) a 12.5T 3.58 MHz modulated $\sin^2$ pulse, 3) a 2T $\sin^2$ pulse, and finally, 4) the bar. The lift-off of the 12.5T pulse is due to two factors - the reduction of chrominance gain at 3.58 MHz as noted in the multiburst test and unequal chrominance - luminance delay. Both impairments are primarily a result of the DEMOD (23A) LPF. The overshoots and oscillations of the 2T pulse and bar waveforms are due to the same filter imperfections.

2.4.17 Conclusions and Recommendations for Improvement

The chief departures from studio quality video reproduction in the mod/demod group are due to the non-uniform group delay characteristic (Figure 2.56) of the DEMOD (23A) Cauer-Chebyshev LPF. A series all-pass equalizer cascade, suitably matched to the filter, could reduce the variation to less than 5% across the video passband, which would be adequate to correct these deficiencies. It should be pointed out, however, that the K-factor for the existing system is approximately 2% and is visually adequate for all but the most stringent applications; these picture impairments are usually only discernable to trained observers.

2.4.18 Disc Playback Performance

Distribution of spectral energy was optimized to provide the best possible picture viewing quality. The criteria chosen in order of relative importance were:

1) Signal-to-wideband noise ratio (maximize)

2) Harmonic distortion (minimize)

3) Carrier Feedthrough (minimize)

4) Transient Response ("K" rating - minimize)

5) Frequency Response (flattest)

6) Luminance linearity (maximize)

The final distribution was experimentally determined; the chosen parameters were:

1) Blanking (0 IRE) at 5.3 MHz.

2) Peak White (100 IRE) at 7.1 MHz.

3) Pre-emphasis: 0.15 μsec, 6 db @ 4.2 MHz.

Figures 2.65,2.66,2.67 illustrate the following playback signals: 1) ramp, 2) multiburst, and 3) $\sin^2$ pulse and bar. Measurements were made with a video head flying at a radius of approximately 2.25", which exhibits worst case disc frequency response (i.e., it is the innermost track by design).

Non-linearity is evidenced by close inspection of the ramp waveform; this effect is not discernable in any picture material. A peak of 1 - 1.5 db around 3 MHz can be noted in the multiburst but, again the visual effect cannot be perceived easily. The $\sin^2$ pulse and bar measurement indicates a "K" rating of 2% for the pulse and 4% for the bar. Ringing associated with the bar would be noticable as fringes around high-contrast picture transitions but

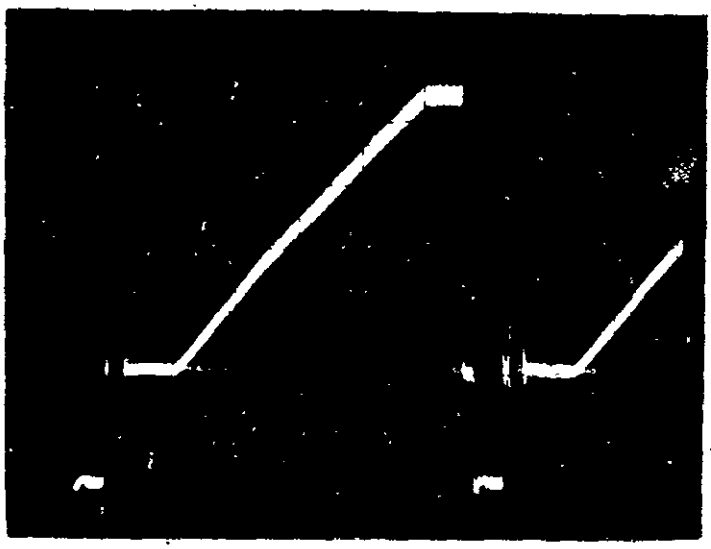

Figure 2.65 Ramp

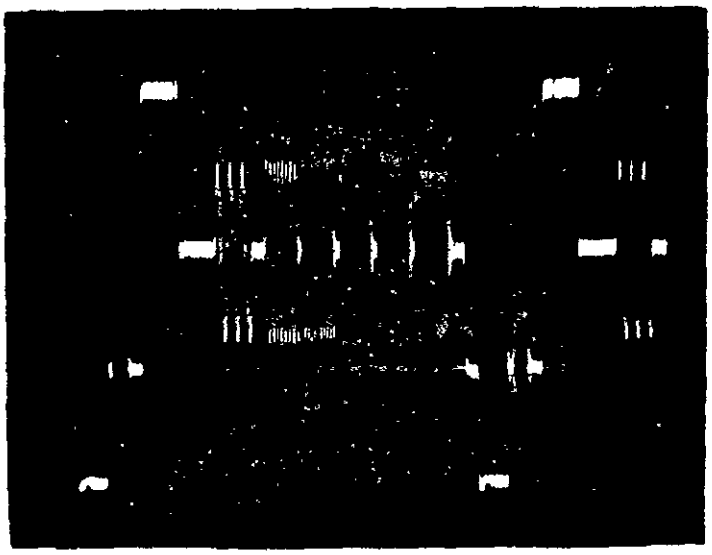

Figure 2.66 Multiburst

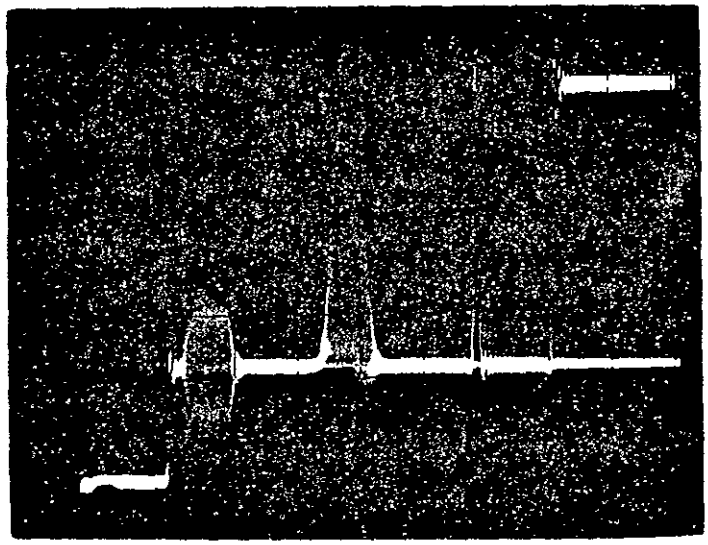

Figure 2.67 Sin^2 Pulse and Bar

the relatively high ringing frequency causes these oscillations to be barely visible.

Playback signal-to-noise ratio is 40 db ± 1 db unweighted, or 47 db ± 1 db weighted.* Further increases in FM deviation, which would directly increase the S/N, cause objectionable moire effects and luminance non-linearity.

2.4.19 Conclusions and Recommendations

It can be seen that the readback signal is a degraded version of E-to-E performance, as must be the case with FM video reproduction from tape or disc. Additional improvements could be made in the read amp circuitry to equalize head signal amplitude and group delay which would largely correct the linear distortions present (aperture corrector). Recently acquired network analyzers would allow this to be done, but present visual quality is more than adequate for the design objectives. Improvements in S/N would require careful additional analysis of the head-switch interface and read amp for optimum match to the video heads for lowest possible noise figure and/or a higher coercivity magnetic coating for the video disc. Neither of these alternatives is recommended for system use with industrial grade monochrome cameras since S/N out

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* Weighting takes into account the frequency dependent perception of noise on the television monitor; a network is used to create the weighted noise spectrum. (See EIA RS-250A, p. 16 for the schematic diagram of the random noise weighting network.)

of the vidicon preamp is on the order of 42-46 db in normal ambient lighting conditions.

In summary, an electronic system was designed to allow storage and recovery of monochrome video on a compact 6.5" multitrack video disc. The performance has been shown to be visually acceptable. The next section covers development of a data system which allows the absolute location of video information to be determined despite mechanical disc jitter.

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2.5 Data Group

2.5.1 Introduction. The timebase of the stored video at both transmit and receive terminals is not stable, but rather varies in proportion to instantaneous disc/head speed fluctuations. These perturbations are very small (∿100-200 nsec peak/revolution) for any given location on the video disc. In order to generate the low frequency reduced bandwidth video signal from the stored picture at the transmit terminal, lines from disc video must be time sampled and temporarily stored for reclocking at a lower sample rate. Likewise the receive terminal must locate incoming picture sample points precisely on its video disc, independent of disc speed fluctuations. Clearly, the resolution in each case must exceed one sample point to avoid blurring and geometric distortions in the final image.

A manner in which this may be accomplished is to write (at the transmit terminal) a data channel on separate parallel disc tracks simultaneously with each new picture stored for transmission. The data read back from these channels must contain all information necessary to sample the entire stored video frame uniformly, without being affected by disc speed variation. Similarly, the receive disc would contain permanently recorded data tracks which function in the same fashion--locating all line addresses and picture elements (pixels) within each line--so that sampled video values are always placed in registration on the disc.

How might such a data track be encoded? A suitable method for locating the beginning of each line would involve detection and

counting of the horizontal sync pulses preceeding each active line. In addition, a high frequency clock should be available to locate samples within the line. Ideally both of these digital signals would be derived from the same data stream. If this is to be the case, the generation of master sync (which contains the horizontal sync pulses needed for line number identification) must be synchronous with the high frequency pixel sample clock needed to time sample the video. The integrated circuit used to generate master sync uses an input clock reference frequency of 2.04545 MHz. The lowest multiple of this frequency satisfying the Nyquist rate is 10.227 MHz, the fifth harmonic. Thus the goals of the data system reduce to:

- regenerate a high frequency sample clock (f_s) of 10.227 MHz from disc.
- regenerate a composite sync stream synchronous with f_s.

2.5.2 Methods of Encoding Digital Data. A wide variety of encoding formats exist for transmission and/or storage of digital data. In addition to disc bandwidth and noise power there are other parameters to be considered in choosing a correct coding scheme (modulation). Reviewing the pros and cons of the various modulation schemes yields the best group of characteristics for a specific application. A useful listing of such characteristics is:

- DC Component - By eliminating all DC from the power spectrum the system may be AC coupled.

- Self Clocking - Some codes have inherent self-clocking features which eliminate the necessity of providing a clock signal to recover the transmitted data.
- Error Detection - Provides the means of detecting data errors and may allow error correction.
- Bandwidth Compression - Some codes increase efficiency of transmission by allowing, for a fixed information rate, a decreased bandwidth thus transmitting more information per unit bandwidth.

The various code groups may be classified as follows:

- Non-return-to-zero (NRZ)
- Return-to-zero (RZ)
- Phase Encoded (PE)
- Multi-level binary (MLB)

Some of the most popular codes are illustrated in Figure 2.68. Of the four basic classes, the PE codes exhibit the most desirable mix of features for digital magnetic recording.[1] They are inherently self-clocking, can eliminate any DC component, allow bandwidth compression, and provide, in addition, limited error detection capabilities.

The particular code chosen for data recording on the magnetic disc is known as Bi-ϕ-M which conforms to the following encoding rules:

1) a transition must occur at the borders of every data cell

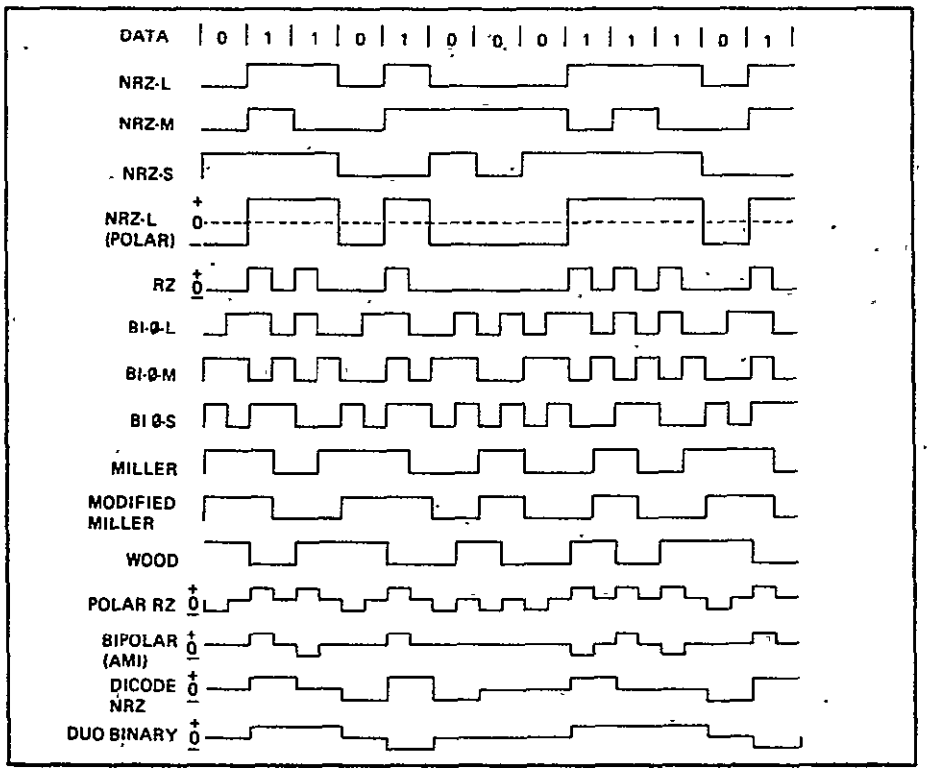

Figure 2.68 Formats for Various Common Digital Codes Used in Data Transmission and Recording

2) a "1" data state will produce a transition in the middle of a cell

3) a "0" data state will not produce a transition in the middle of a cell.

The data to be encoded consists of realtime composite sync (see Master Sync/Timing Group) coming from the sync chip. A synchronous data cell clock must be chosen to allow recovery of f_s from the data stream. Frequency response limitations of the disc/head transfer function and the Bi-ϕ-M code spectral distribution dictated a cell clock of 4.0909 MHz (twice master clock frequency). The self-clocking property of the code allows recovery of this frequency from the data stream in order to generate f_s .

2.5.3 Data System Configuration. The data group consists of four major subsystems which are:

- Digital Read/Write Amplifier
- Encoder/Decoder
- Clock-Recovery PLL
- Composite Sync Decoder

The digital R/W board accepts a digitally encoded data stream and directly interfaces to the video heads. The encoder/decoder board translates the incoming data into Bi-ϕ-M during recording and decodes the data stream during reproduction. The clock-recovery PLL accepts the incoming data stream from disc and generates the clock required to decode the data. Finally, the composite sync decoder regenerates

the same group of sync signals as the master sync system directly from recovered composite sync. All these signals are, however, locked to the disc timebase during playback.

Figure 2.69 shows the card interconnect diagram for the data group. Table 2.12 lists the various cards employed. A brief review

Table 2.12 DATA GROUP CIRCUIT BOARDS

91A	Digital R/W Board
92A	Encoder/Decoder
93A	Clock-Recovery PLL
112A	Dsync I Proc
114A	Dsync II Proc

of board functions and design features now follows.

2.5.4 Digital R/W (91A). This board is a basic modification of the video R/W board (57A), particularly in the reproduce amp section. Figure 2.70 shows a functional block diagram of the board. The disc playback signal is a differentiated version of that which is recorded. To restore the original signal, the preamplified head signal is low passed, differentiated, low-passed again and fed to a high-speed comparitor. The low-pass filters are classical flat delay filters which serve to isolate subsystems in each direction of signal flow. A line driver buffers the TTL data stream to the Bi-ϕ-M decoder board during playback. See Figure 2.71 for functional placement within entire data system.

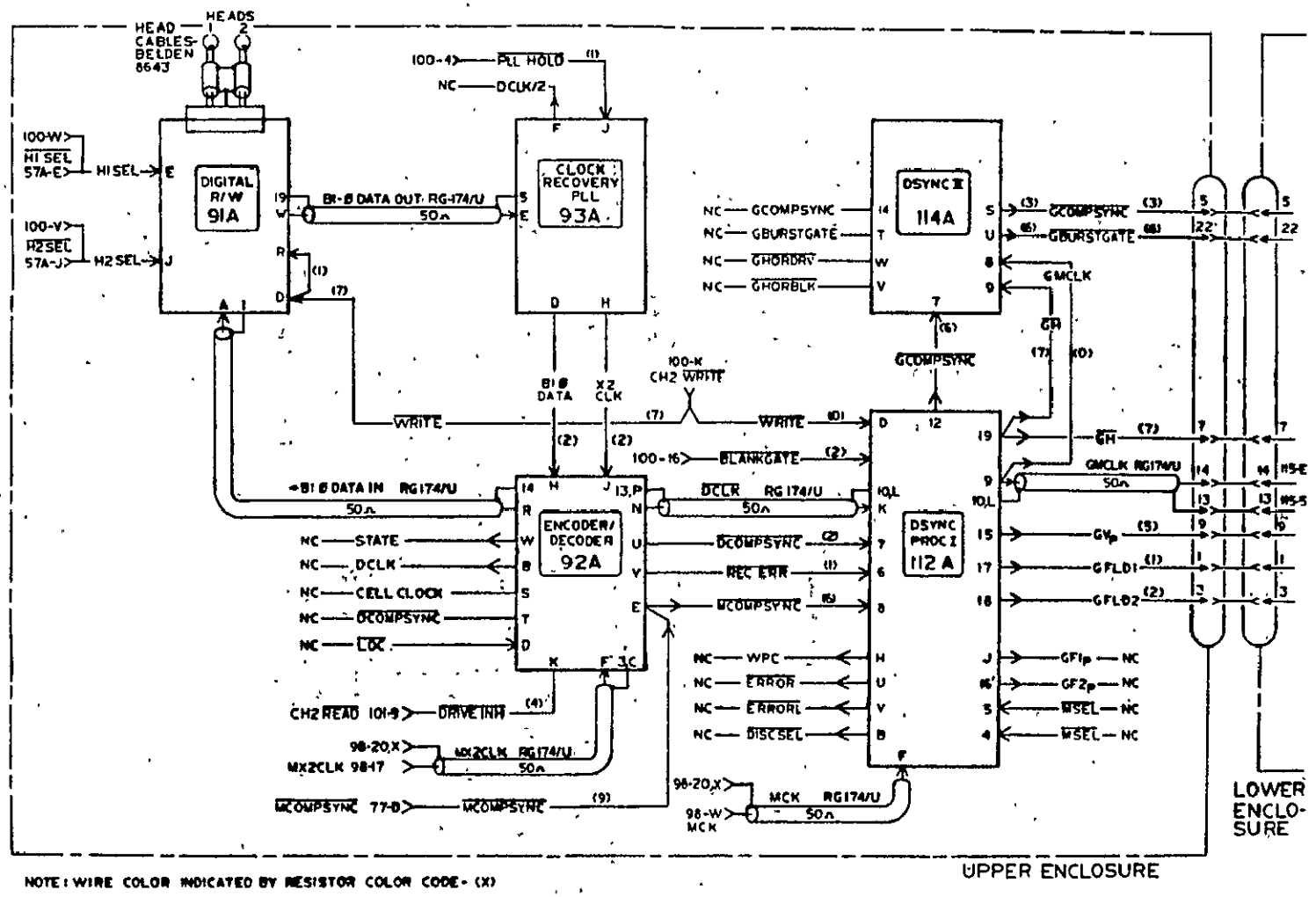

Figure 2.69 Data Group Card Interconnect Diagram

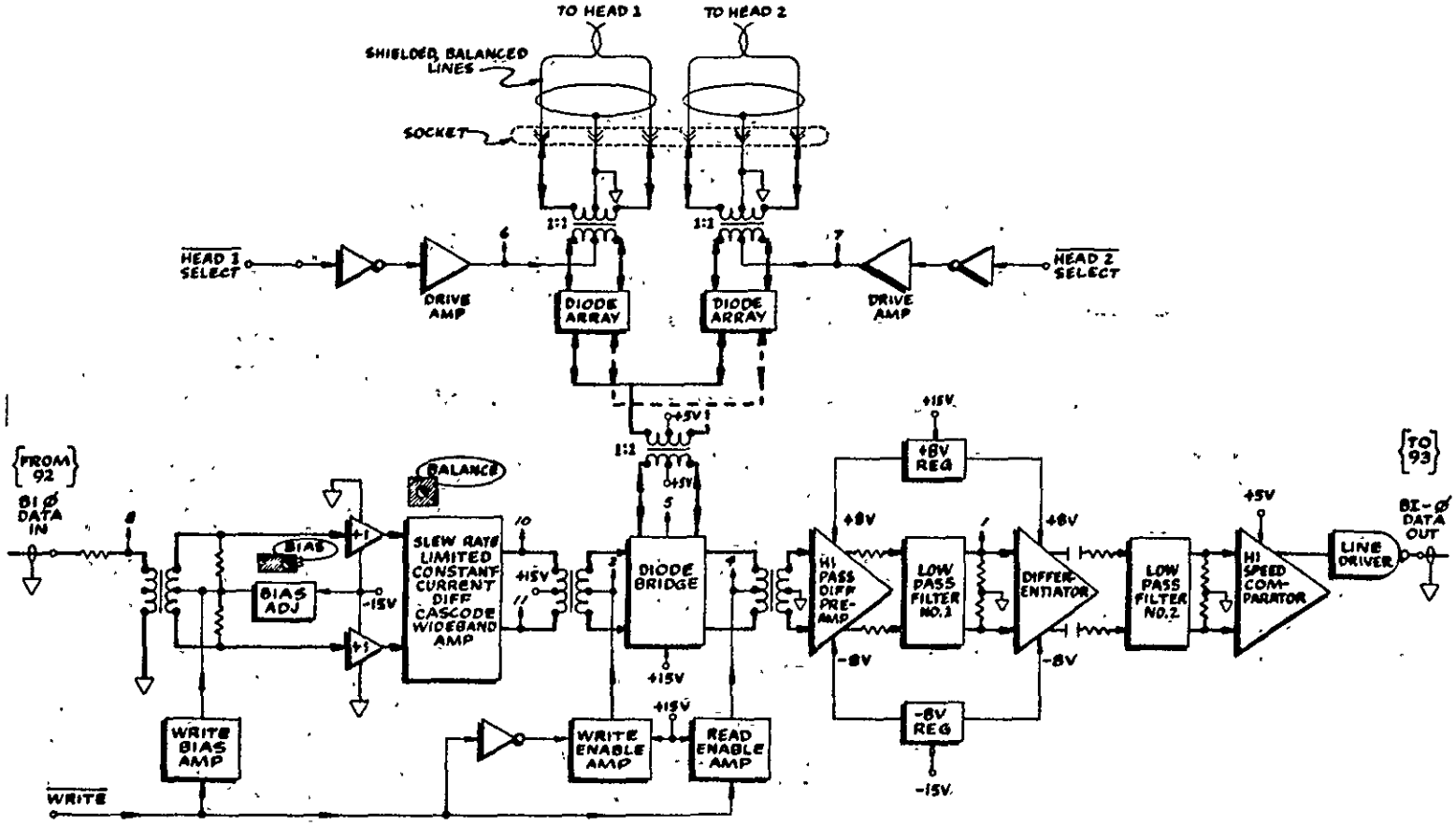

Figure 2.70 Digital R/W Board (91A) Functional Block Diagram

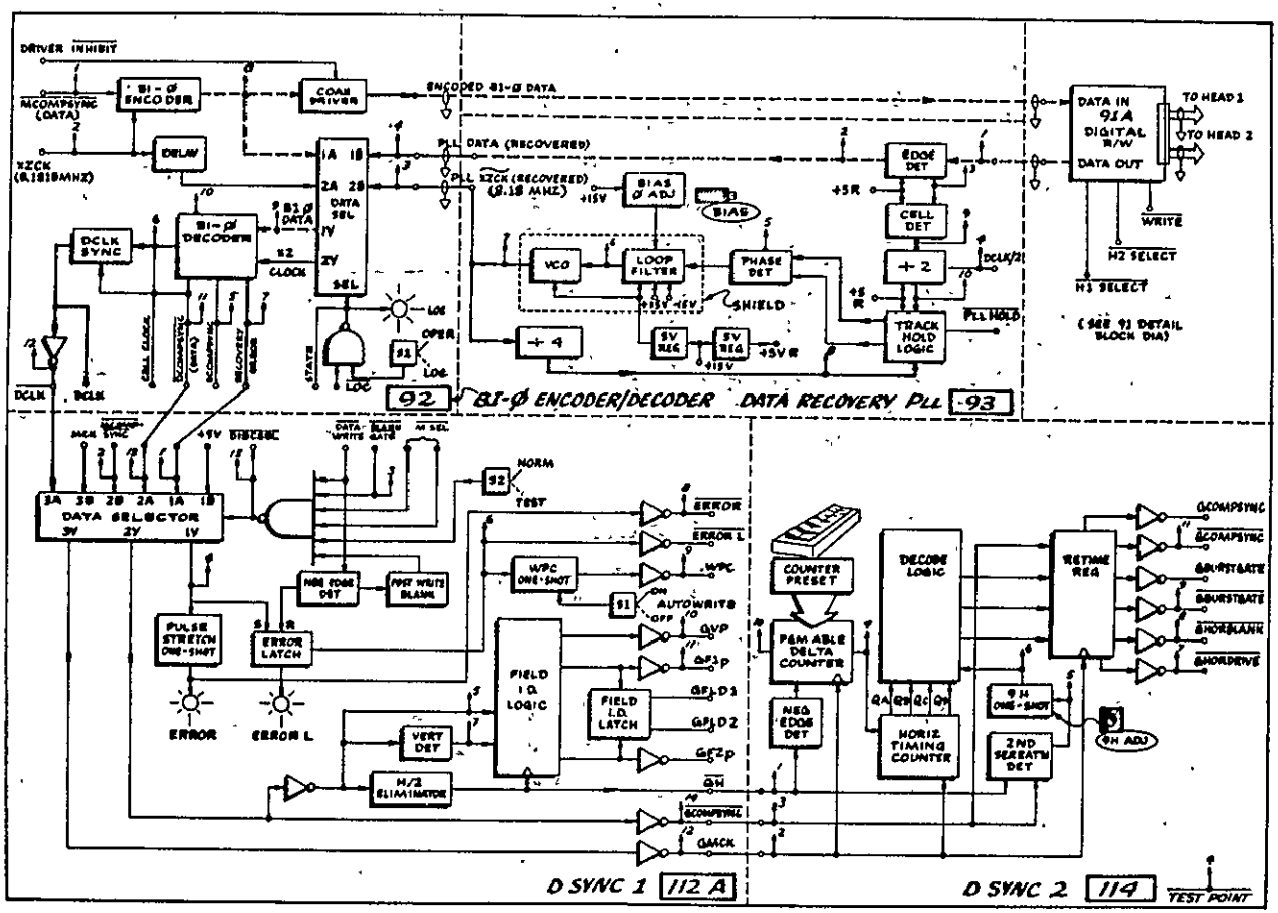

Figure 2.71 Data Group Functional Block Diagram

2.5.5 Encoder/Decoder (92A). This board (Figure 2.71) contains three subsystems; an encoder, a data selector, and a decoder. The encoder requires the data (MCOMPSYNC) and an encode clock (8.1818 MHz) and produces the Bi-ϕ-M bit stream with a cell clock of 4.0909 MHz. The data selector allows the decoder section to be fed either from disc or directly from the encoder. This allows for a) self-testing of the board and b) preservation of data output integrity during track-switching of the video disc. The decoder yields the output data stream, a recovered master clock (DCLK) at 2.04545 MHz, and a recovery error line. This last feature relies upon the coding rules and produces a low output if these rules are violated, and is particularly useful in disc/head alignment procedures. Further subsystems monitor the output and automatically rewrite the data track (in the case of the receive terminal) should even a single cell error occur.

2.5.6 Data Recovery PLL (93A). This board processes the disc data stream and detects the individual cell boundaries. Edge information is fed to a PLL which generates the required 8.18 MHz clock to decode the Bi-ϕ-M data. Track-hold logic is embodied to keep the loop near lock during disc track switching so that rapid aquisition occurs once the signal is again available. A phase bias control allows adjustment of clock edge time relative to the data stream to eliminate possible errors induced by jitter in either clock or data signals.

2.5.7 D Sync I (112A). The disc clock (DCLK) and data (DCOMPSYNC) signals decoded by (92A) are processed by this board. An input data selector allows either crystal-referenced clock (MCK) and sync (MCOMPSYNC) or disc referenced signals to be processed. Two functions are performed: 1) Vertical interval and field identification and 2) readback error processing and automatic re-writing of the data track. The clock and data signals are buffered off (112A) to (114A) and are respectively called (GMCK) and (GCOMPSYNC).

2.5.8 D Sync II (114A). All horizonal (line-related) timing signals are generated on this board. The input (GMCK) is processed by digital counters and combinational logic in conjunction with (GCOMPSYNC) to produce horizonal drive (GHORDRIVE), blanking (GHORBLANK), and burst gate (GBURSTGATE). These signals, together with (GCOMPSYNC), are retimed with (GMCK) in a quad "D" register to insure that all transitions are synchronous with the pixel clock reference.

All schematics, timing diagrams, and adjustment procedures are exhibited in Appendix A2.9.

2.5.9 Conclusions. A solution to the line and picture element location problem was proposed and verified by design. An entire set of real-time sync signals are produced by the Data Group electronics which are locked to the video disc timebase. These signals enable the Timebase Expander Group (TBE) and Timebase Compressor Group (TBC) to operate on disc-video as if it had a stable timebase. The TBE/TBC Groups will be explored in the next section.

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2.6 TBE/TBC Group

2.6.1 Introduction

These systems enable the stored video information to be transmitted over a narrowband channel and reconstructed for real-time display. The timebase expander (TBE) performs bandwidth compression at the transmit terminal and the timebase compressor (TBC) reverses the operation at the receiver. This section shall develop the fundamental concepts, theoretical and practical constraints and functional block diagrams of each system. A description of system operation and specifications will follow. Detailed card interconnection diagrams will be introduced, but no attempt will be made to cover every aspect of system control and data handling. This information will be available in the near future as part of a complete VFRTV operating manual.

2.6.2 Fundamental Concepts

The TBE/TBC groups are essentially data handling systems that slowly transfer blocks of data from one mass memory to another over a suitable transmission channel. For reasons examined earlier, the mass memories are video magnetic discs; a television frame recorded upon these discs is repeated continuously in real-time on the viewer's monitor. This "snapshot" is a direct recording of the output of any conventional video source such as a camera, VTR, etc. Each television line can be considered a discrete block of data. The visible or "active" portion of this line is a continuous analog

signal of approximately 50 μsec duration. The total picture is composed of about 500 of these horizontal lines sequentially scanned across the face of the television monitor. More exactly, each frame consists of two consecutive scans or fields consisting of exactly one half of the total number of horizontal lines. The scans are arranged to allow the alternate sets of lines to fall between each other; this technique is termed "interlacing" and is necessary to eliminate visual flicker and jerkiness during motion sequences. A stored frame repeats every 1/30 second; the video disc can thus be thought of as a large shift register file circulating every 1/30 second.

The register contains in analog form about 500, 50 μsec data records which are identified by their sequence in the register. It is these records which must be bandwidth compressed, transmitted, and restored to real-time to be entered in a similar "register" at the receive site. To accomplish the required timebase change, the analog record must be time sampled. These samples are then used to create a corresponding low frequency signal for transmission. The sampling process, together with intermediate short-term storage is done by the digital processor in the TBE. A discussion of the sampling process now follows.

2.6.3 Discrete Time Sampling

The choice of sampling frequency, f_s, is dependent upon satisfactory signal recovery and realizable filter technologies. The upper baseband frequency required for television is approximately

4 MHz. Suitable bandlimiting filters can assure that spectral energy drops rapidly beyond this frequency (> 50 db down @ 5 MHz). Consideration must be given to realizability of bandlimiting (anti-aliasing) and reconstruction filters; that is to say, the sampling frequency must be sufficiently high to accommodate the transition regions of the video filters. A frequency of 10.2 MHz was chosen for the sample rate; this allows reconstitution of a 4 MHz baseband signal without aliasing errors.

A block diagram (Fig. 2.72) illustrates the format for signal timebase alteration employing discrete time sampling. Low pass filter #1 bandlimits the input signal to well below the Nyquist limit prior to sampling at f_s. A fixed record length of N samples is stored in analog shift register memory. A reconstruction clock resamples the memory at a faster (or slower) rate feeding low pass filter #2 which regenerates the analog signal at the new timebase. Bandwidth compression or expansion is directly proportional to the ratio of f_s and f_R. In the case of timebase expansion (bandwidth compression) the mass memory supplies upon demand N-sample records of the real-time signal at suitable intervals to construct the low frequency version (see Figure 2.73).

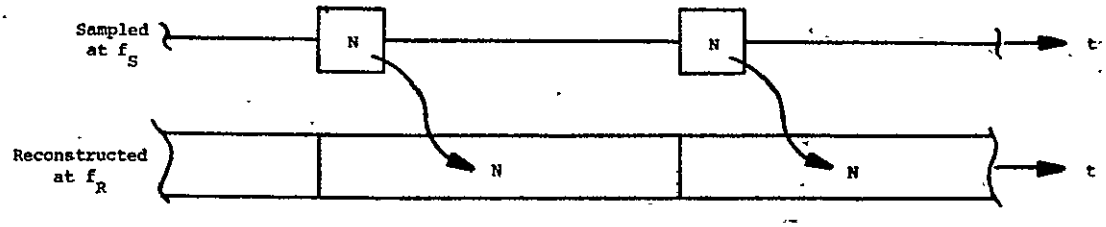


Figure 2.73. Signal Timebase Expansion

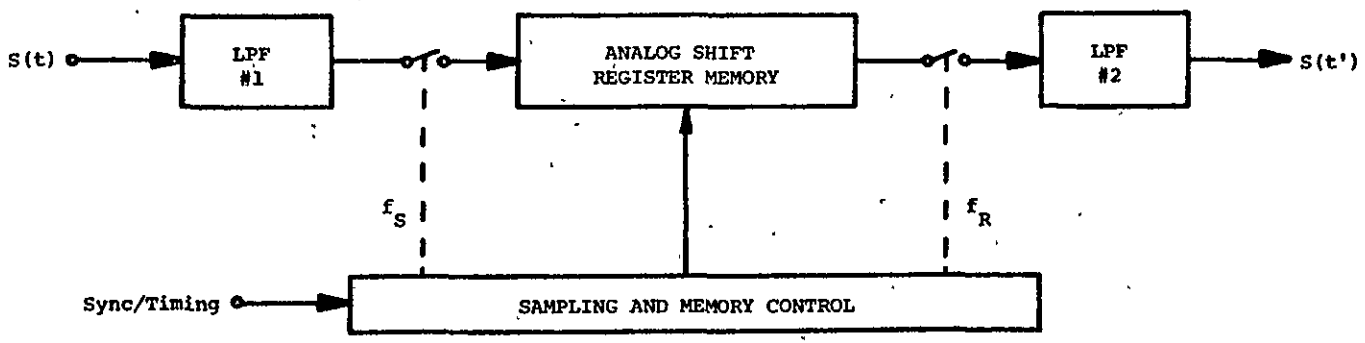


Figure 2.72. Basic Format for Signal Timebase Alteration

The timebase alteration procedure de:
possible embodiment of the concept. Unfortunately, analog memories suffer from deficiencies due to limitation of charge transfer device technologies. These problems were encountered and analyzed during evaluation of a 512 sample analog memory constructed from 8 chips of 64 samples each, multiplexed with an 8 phase clock to achieve the 10.2 MHz high speed sampling rate. It was found that each device tended to impose a characteristic amplitude variation due to charge site capacitance variations. The degree of variation exceeded 10% in some cases rendering the system unsuitable for high SNR applications. An additional limiting factor encountered involved the low frequency shift rate - these devices cannot operate at an arbitrarily low sample rate due to charge leakage. This characteristic is further aggravated by high temperatures which may be encountered in real systems. This constrains the bandwidth compression factor, which is undesirable.

2.6.4 Digital Timebase Alteration

After examination of the difficulties encountered in an all analog processing scheme, it was concluded that a digital system would be required for temporary storage of signal samples. Since the samples must be represented by a finite number of levels (quantized), a further complication is introduced.

Conceptually, discrete time samples and quantized amplitude are not the same. Quantization describes the process of assigning

to a range of voltages a single value, whereas discrete implies that only certain values for the continuous time variable are utilized; changes in the analog signal between sampling instants are ignored. If this signal is bandlimited relative to the sampling rate (Nyquist rate), the sampled analog values contain information identical to the continuous signal - no information is lost. Time sampling can be a lossless process, but amplitude quantization always destroys information.

Digital word length dictates the overall quality of reproduction in terms of signal-to-quantization error ratio. If quantization error is random from sample to sample, (which is a valid assumption for high-level complex input signals such as video having essentially independent and uncorrelated quantization errors) the quantization noise can be modeled as white additive noise. The resulting SNR is expressed by the well known formula:

$$SNR(db) = 6.02n + 1.76 \qquad 2.18$$

where n = no. of bits/word.

An eight bit word was selected for the digital processor providing a theoretical upper limit of ∿ 50 db SNR which is sufficient to be masked by video disc playback noise. Compact A/D converters can be had in the $500-$1000 price range which operate at the required 10.2 MHz sampling frequency. Figure 2.74 illustrates the configuration employed and the functional placement of A/D, memory, and D/A systems.

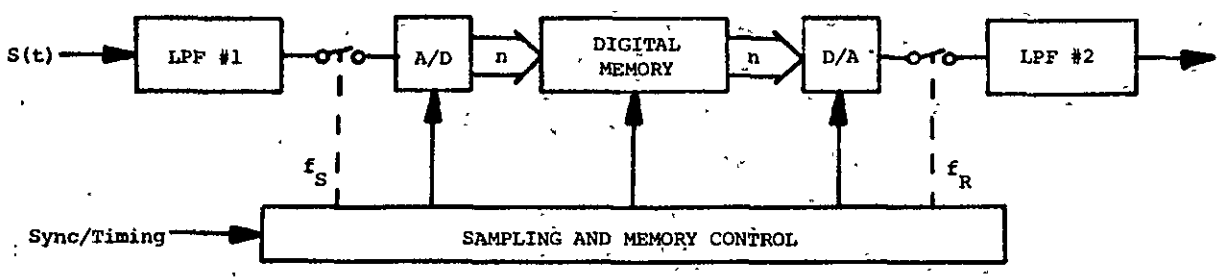


Figure 2.74. Basic Format for Digital Timebase Alteration

2.6.5 Digital TBE/TBC Operation

Figure 2.75 illustrates the most basic functional block diagram of the digital TBE. A single video frame, stored on disc, is available to the processor in real-time form. Suitable parallel sync information, recorded on an additional disc track is utilized to control high frequency sampling and locate individual lines in each recorded field of the picture to be time-base expanded. The TBE is configured for an expansion/compression ratio of 300; a convenient record length used is 512 samples per line which allows virtually complete conversion of an active line at the required 10.2 MHz sample rate. To allow for sufficient time to expand the signal in temporary storage, two lines are loaded into memory #1 directly from the disc. This memory immediately transfers its contents to memory #2 provided the second memory is empty. Memory 2 is reclocked at the much lower sampling rate f_R. Meanwhile memory #1 is available for loading the next line pair from disc. This interleaving procedure is necessary to 1) allow continuous reconstruction at the low frequency clock rate, and 2) provide sufficient time to locate the next 2 lines on the disc. Note that only active video information is passed through the system. All low frequency synchronizing signals are generated in the TBE control logic and added to the output waveform prior to filtering. The resulting expanded video signal after low-pass filtering is a virtually exact duplicate of the normal real-time counterpart except for the timebase change.

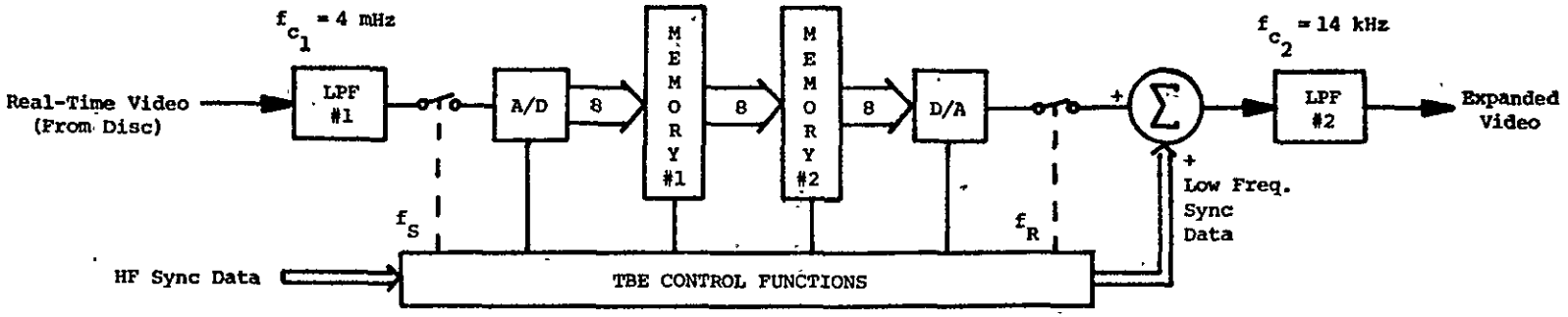


Figure 2.75. Functional Block Diagram of Digital Timebase Expander (TBE)

An inband burst (see Figure 2.76) is also added to the expanded video signal on the back porch of horizontal sync to provide a reference frequency for the TBC at the receive terminal to resample the incoming video for timebase compression. The TBC (see Figure 2.77)

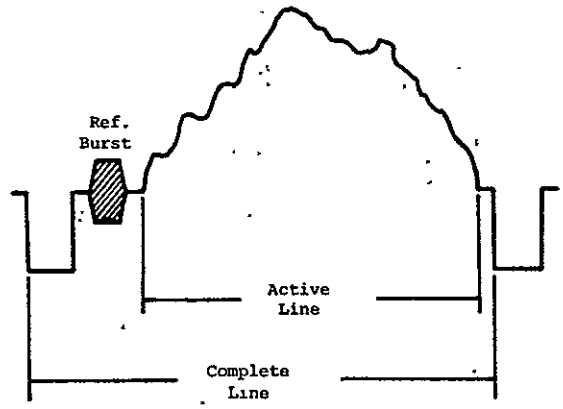


Figure 2.76. Low Frequency Video Line Showing Burst

extracts sync and f_R from this signal and uses this information to essentially invert the expansion operation performed at the transmitter. Information is written on disc 2 lines at a time. Line location and pixel location are controlled by a data track which is permanently written on the receive disc. Thus, the high-frequency resampling clock f_s is constructed from magnetic information on the disc itself, avoiding the problems encountered due to minor fluctuations in disc speed. A detailed description of the system employed is given in the Data Group Section.

2.6.6 TBE System Configuration

The card interconnect block diagram (see Figure 2.78) shows the individual card functions utilized in the TBE and all associated

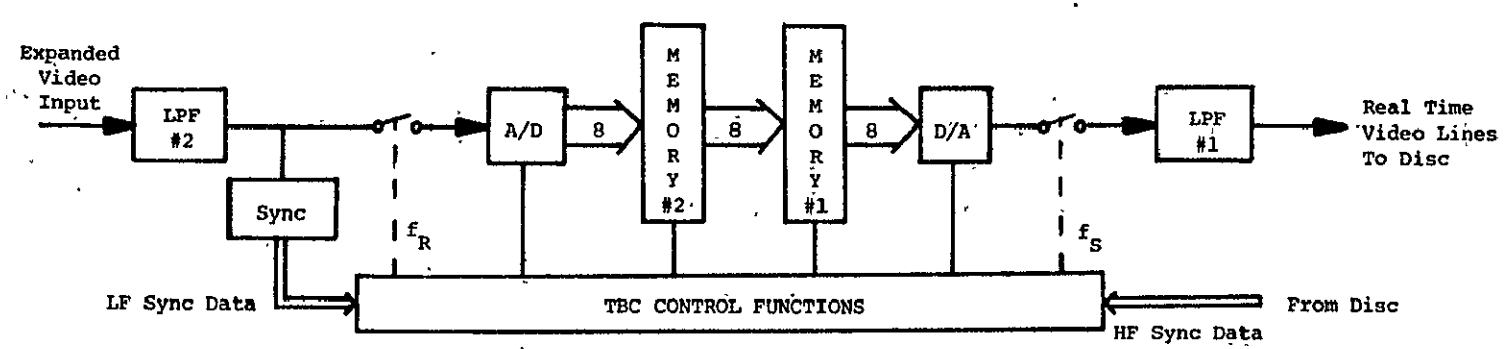


Figure 2.77. Functional Block Diagram of Digital Timebase Compressor (TBC).

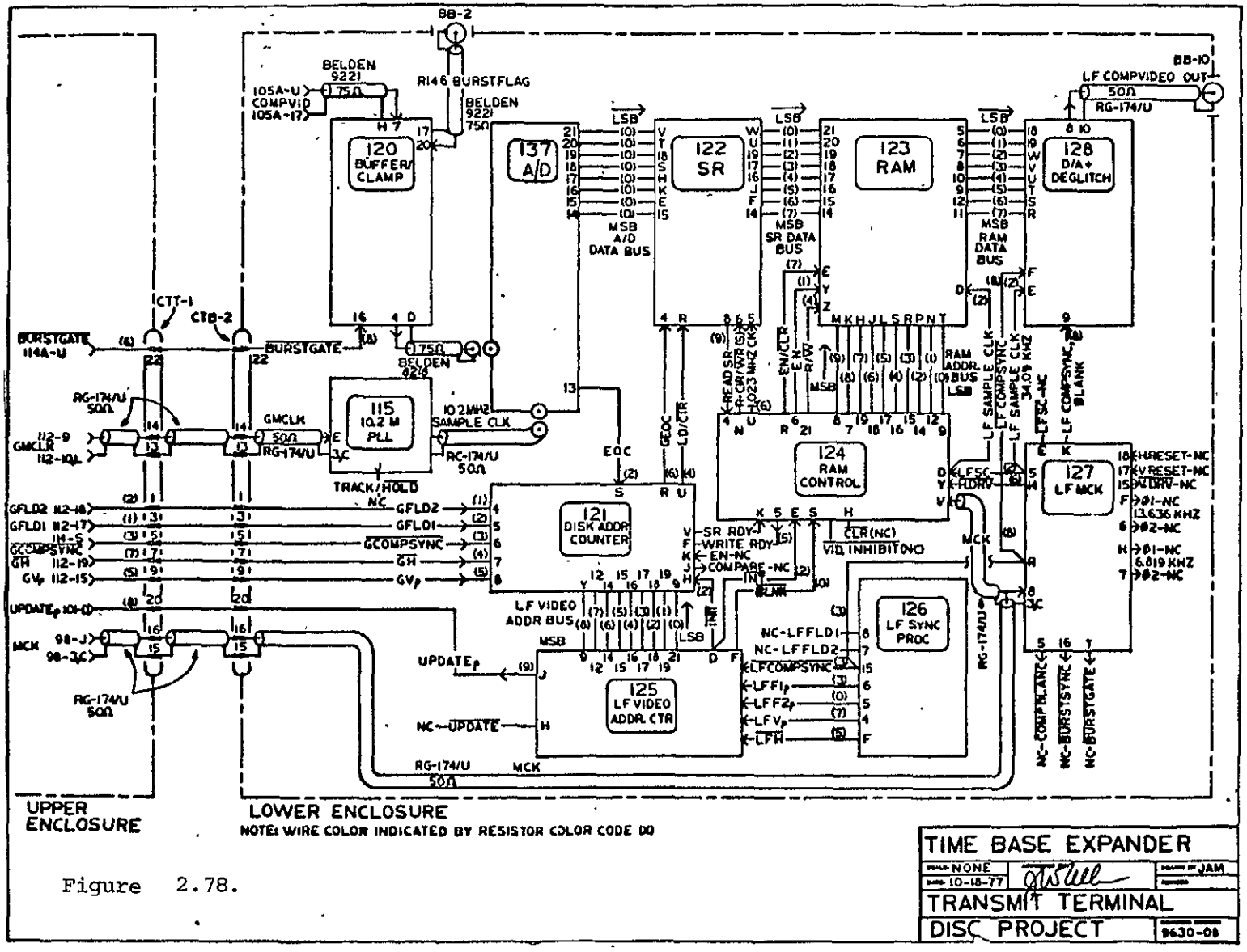


Figure 2.78.

internal control and data busses as well as I/O ports. A list of board names and numbers appears below in Table 2.13.

TABLE 2.13

Timebase Expander Circuit Boards

Board No.	Name
115	10.2 MHz PLL
120	Buffer/clamp
121	Disc Address Counter
122	Shift Register
123	RAM
124	RAM Control
125	LF Video Address Counter
126	LF Sync. Processor
127	LF Master Clock (LFMCK)
128	D/A and Deglitch
137	High Speed A/D

The low frequency composite video transmitted between terminals is generated on board (128) by combining expanded picture information, line by line, with a composite sync signal. This composite signal contains sync, blanking, and burst in the same relative proportions as real-time composite sync. These components of the signal serve to provide the necessary information for the receive terminal to assign line and picture element locations on its video disc memory. This LF compsync signal is processed by boards (125) and (126) to

produce the additional control signals for TBE operation. It should be noted that system control is entirely executed by the internal low frequency signals.

Board (125) enables data transfer to the output during the active line time of low frequency sync. This transfer is timed using the low frequency reconstruction clock, f_R, and LF sync to identify the required line pair to be accessed from the disc. The required line numbers are transferred to the Disc Address Counter (121) via the low frequency video address bus. The method of accessing the line memories #1 and #2 will be developed next.

Two types of memory are used in the expander. Each is configured as a 1Kx8 shift register. Memory #1 is constructed of high speed MOS dynamic shift register integrated circuits which read data at the video sampling rate (f_s = 10.2 MHz) and transfer to memory #2 at 1.02 MHz. This second memory is built of static RAM whose address space is controlled to allow emulation of a shift register. The RAM control board (124) loads two lines from the shift register (122) only during a LF horizontal blanking period. These two different technologies were required at the time when this portion of the system was designed due to the high cost of fast static RAM. Present availability of such technology dictates that both memories could be combined into a single larger RAM which would enable reduction in physical circuit complexity and the necessity of memory transfer. The recommended embodiment would be alternate

parallel access to two identical RAM's. Address space would be divided equally for memories #1 and #2.

The nature of transfer from disc to LF video can be understood by consideration of the following basic premise. The disc address counter on board (121) holds the number identifying the current video lines which are available at the expander's high-speed A/D converter output data bus. A line address comparator enables transfer of this picture data only for the requested line pair generated by the low frequency address bus. Transfer timing constraints take into account worse case access times for any given line pair needed from disc. This process is shown in abbreviated form in Figure 2.79. It should be noted that once the S.R. has been loaded, it will continuously circulate until the RAM is empty (the preceeding lines have been clocked out at f_R) and RAM control takes over for the intermediate transfer.

Only a subset of the entire video frame is actually transmitted. Some initial lines bearing no picture information can be ignored. Similarly the amount of each line to be expanded is somewhat less than the entire active portion to allow for a more simple digital system architecture. In each case, incremental counters termed delta (Δ) counters, provide digitally controlled delays to accomplish this. These serve to locate the sampled picture information in the approximate center of the visual field (see Figure 2.80). The amount of reduction experienced does not significantly effect picture content.

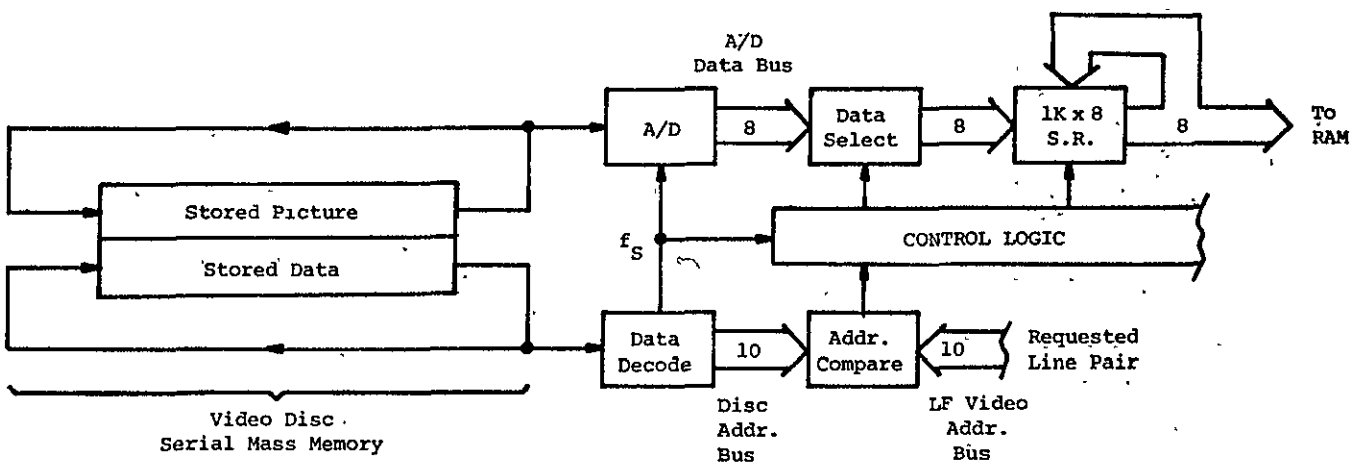


Figure 2.79 Block Diagram of Video Transfer from Disc to Shift Register Memory.

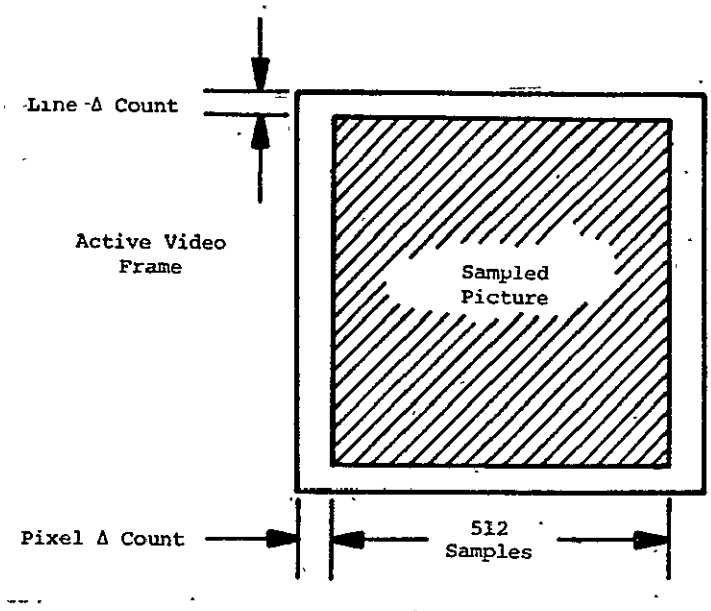


Figure 2.80 Picture Sampling Format

2.6.7 TBC System Configuration

The TBC system serves to reverse the process effected on picture samples and utilizes much of the physical circuitry developed for the TBE. Table 2.14 shows the board names and numbers employed in this system. The associated card interconnect diagram is shown in Figure 2.81 . The TBC derives its low frequency timing from the incoming bandwidth-compressed VFRTV signal via sync and burst as explained earlier. Memory transfer is less complex because RAM may load the SR immediately. Sufficient time is allowed (2 LF lines) to insure that the appropriate disc address can be accessed for unloading the SR to disc. Minor variations in system control functions and timing will be covered in the system manual.

TABLE 2.14

Timebase Compressor Circuit Boards

Board No.	Name
104	High Speed D/A and Deglitch
115	10.2 MHz PLL
122	Shift Register
123	RAM
131	LF Timing
132	Sample Clock Recovery PLL
133	LF A/D
134	RAM Control
135	Disc. Address Counter
136	LF Address Counter

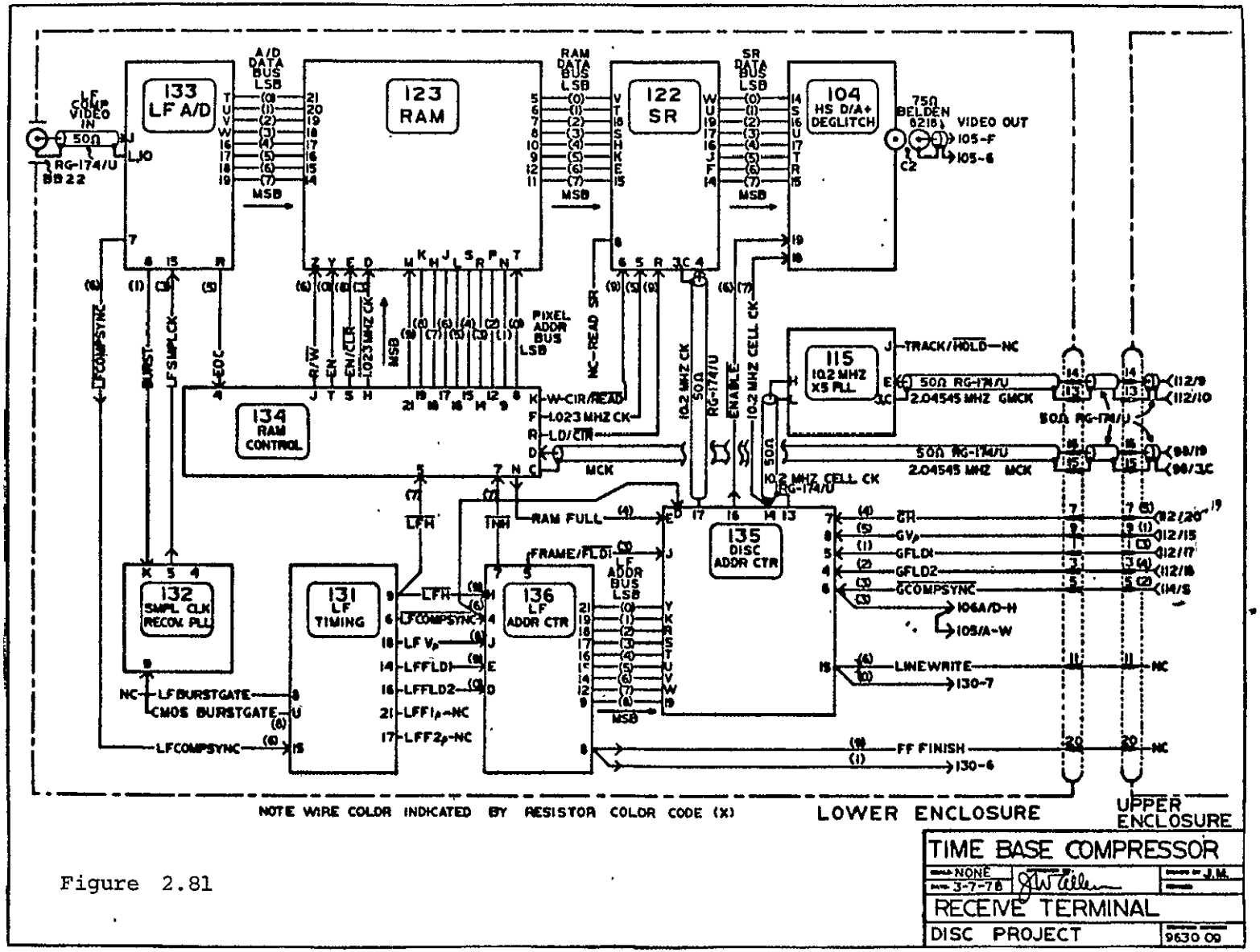


Figure 2.81

2.6.8 System Specifications and Performance

The following tables specify various operating parameters for the TBE/TBC system. Table 2.15 lists input signal requirements for the TBE. Table 2.16 details the internal parameters relevant to both TBE and TBC, while Table 2.17 specifies the characteristics of the low frequency narrowband video signal. It should be noted that the Data Group, which provides reference markers for the video disc read/write operations is treated in detail in another section. Similarly, the design considerations and actual circuitry employed in the low pass filters for the LF video signal will be covered in a separate section.

TABLE 2.15

INPUT SIGNAL REQUIREMENTS

Television Standard	U.S. (EIA-RS-180A)
Lines/frame	525
Fields/frame	2, interlaced
Field rate	59.94 Hz.
Line rate	15734 Hz.
Field Time	16.683 msec.
Line time	63.557 μsec.
Input amplitude	1.0 Volt (nominal)
Blanking reference	0.0 Volt (nominal)

TABLE 2.16

Sampling and Quantization	
No. of quantization levels	256 (8-bit word)
No. of lines transmitted	240/field 480/frame
No. of samples/line	512
High speed sample clock frequency	10.22725 MHz
High speed sample interval	97.778 nsec.
Sampled active line time	50.062 μsec.
Data Track	
Time base correction method	Parallel digital data track
Data encoded	Composite sync.
Encode method	Bi-phase, M
Encode clock frequency	4.0909 MHz.
Pixel reference clock recovery	Phase-lock loop
Pixel reference frequency	2.04545 MHz.
Memories	
Fast 2 line buffer memory	MOS shift register (S.R.)
Capacity	1024x8 bits
Write clock-from Hi-speed A/D	10.22725 MHz.
Read clock - to RAM	1.002725 MHz.

Memories (cont'd)	
Slow 2 line buffer memory	MOS RAM
Capacity	1024x8 bits
Write clock - from S.R.	1.022725 MHz.
Read clock - to D/A converter	34.0908 KHz.
Timebase Expansion/ Compression factor	300

TABLE 2.1

Low Frequency Video Characteristics

No. of lines/frame	525
No. of active lines/frame	480
No. of fields/frame	2, interlaced
Field rate	0.199 Hz.
Field time	5.005 sec.
Line rate	52.4467 Hz.
Line time	19.067 msec.
Signal amplitude	1.0 V_{pp} (nominal)
Receive terminal pixel clock reference	Burst on backporch of blanking for each active line
Burst frequency	13.63632 KHz.
No. of cycles/burst	10
Burst duration	0.733 msec.
CW regeneration technique	Sample/hold PLL

Table 2.17(cont'd)

LF video maximum in band frequency	14.0 KHz.
Out-of-band energy	Function of equalized channel filters.

Various laboratory transmissions have been run to evaluate picture quality. Initially direct digital data was transferred between transmit and receive terminals to verify the video memories and hi-speed digital subsystems. Later tests transferred unfiltered analog samples of the low frequency video signal. Final tests employed bandlimiting filters to achieve an actual 14 KHz. channel. A demonstration of this system was conducted at NASA Lewis Research Center for various members of the technical staff. Picture viewability was found to be acceptable in each of two transmission modes: 1) full frame update in 10 seconds, and 2) single field transmission every 5 seconds. In the latter mode the single field which is transferred to the receive terminal is written into both field memories on the video disc. This trick produces a fully scanned video image with a sacrifice only in vertical resolution and was found to be surprisingly viewable - little degradation is perceptable.

2.6.9 Recommendations and Conclusions

The prototype TBE/TBC digital system was designed, constructed and tested over a period of approximately one year. Individual printed circuit cards were assigned to various subsystems for

use in trouble shooting and modification. Card interconnection and isolation of transients from the low-level wideband electronics elsewhere in the VFRTV system was however, a continuing difficulty. It is felt that a significant improvement in SNR ($\sim$ 6-10 db) could be achieved if all functions were now implemented on a large wirewrap board specially designed for Schottky TTL logic. Certain major simplifications would also result from the use of one large fast RAM, as mentioned earlier in this section, rather than separate technologies for each memory.

2.7 Channel Filters

In the design of classical sharp cutoff low-pass filters (Butterworth, Chebychev and elliptic, for example) the designer may completely control the magnitude response of the filter by proper choice of parameters to achieve any desired response in the passband, transition region, and stop-band. Once the magnitude response is determined, the phase response (and thus the delay characteristic) of the filter is fixed.

Frequently, a non-linear phase response poses no significant problem and may be ignored. In the processing of video signals, however, phase response is important, since delay non-uniformities produce undesirable overshoots at high-contrast picture transitions which are visually manifest as ghosts and fringing. It is therefore necessary to modify the phase response of these filters by the addition of a series delay correction network whose presence will not degrade the filter's magnitude characteristic. Any additional series network cannot decrease the overall phase shift; thus the corrector should be designed in such a way that its phase response, when cascaded with the low pass filter, will produce an over-all piece-wise linear phase response, i.e., constant group delay (see Figure 2.82).

Delay corrected audio low pass filters are not available commercially unless specially designed. It was therefore decided to develop a computer program to determine the optimum pole-zero locations for second order all pass filter sections to realize any

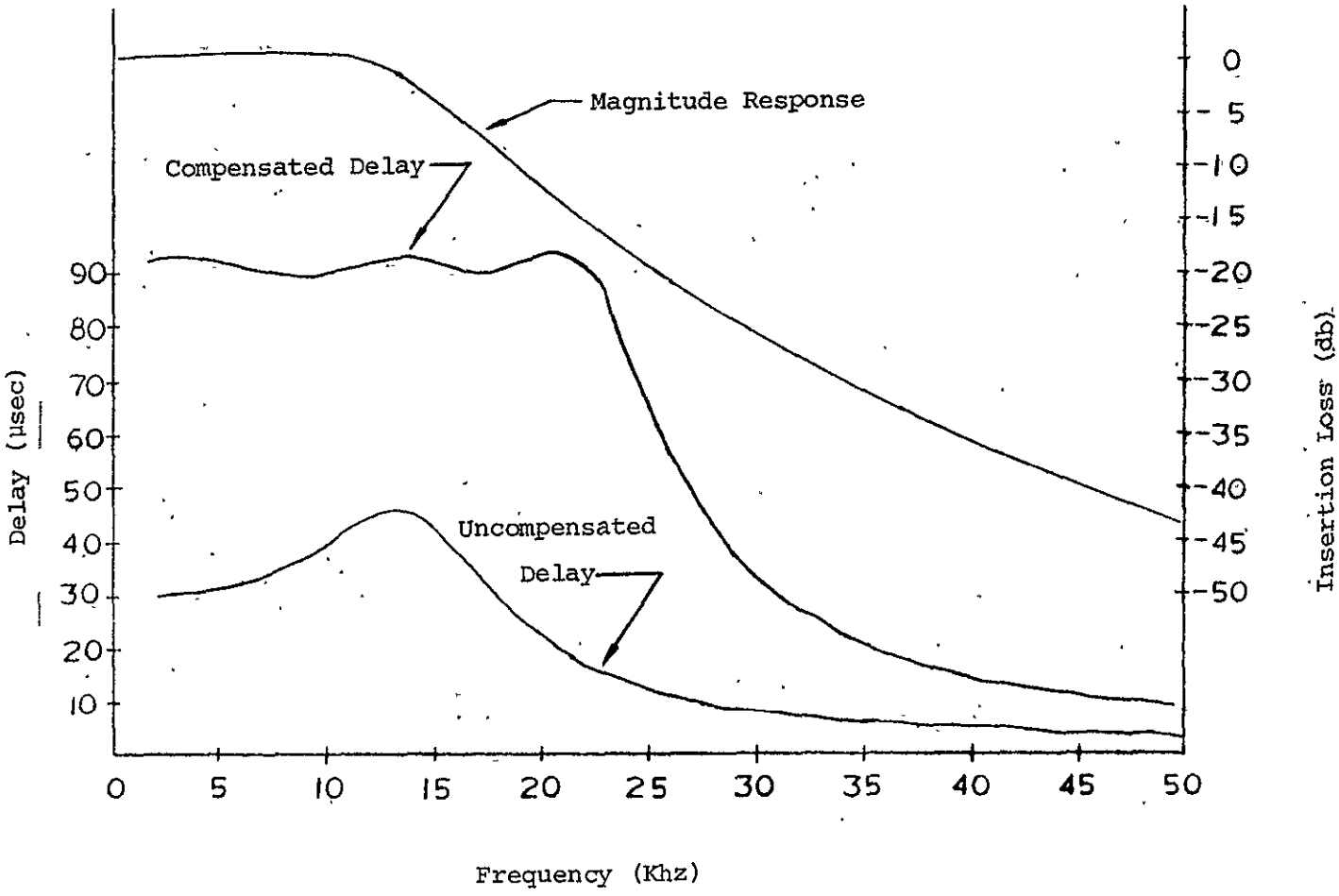


Figure 2.82 Fourth Order Butterworth LPF

needed delay correction networks for filter or channel equalization. This program allows the designer to enter data for a given low pass filter either in the form of an ideal transfer function or as measured group delay from a network analyzer. In the latter case, the delay may be corrected to any desired frequency beyond the cut-off frequency of the low pass filter. The user may specify a range of orders for the corrector network and whether the network is to be active or passive. The program determines if a realizable network exists for each even order configuration within that range, prints out the pole-zero values and component values. The magnitude and delay response of the overall filter, its impulse response (corrected and uncorrected), and its response to a bandlimited sine-squared pulse input are also computed. The flow chart in Figure 2.83 shows the basic steps carried out by the program.

Results for a 4-th order Butterworth filter (f_c = 14 KHz) delay compensated with a 4-th order all pass section (f_c = 22 KHz) now follow. This particular filter is needed to implement the VFRTS prototype for 14 KHz wide channels. The resulting circuitry for the filter and equalizer are shown in Figures 2.84, 2.85 respectively. Note that the realization of the needed pole-zero locations is accomplished using the Bi-Quad op-amp configuration which is very tolerant of slight component irregularities. The calculated response to a sine-squared pulse bandlimited to 14 KHz is shown in Figure 2.86 ; the equalized response (Figure 2.87) results in an acceptable "k-factor" of $\sim$ 1%. Actual measurements were taken

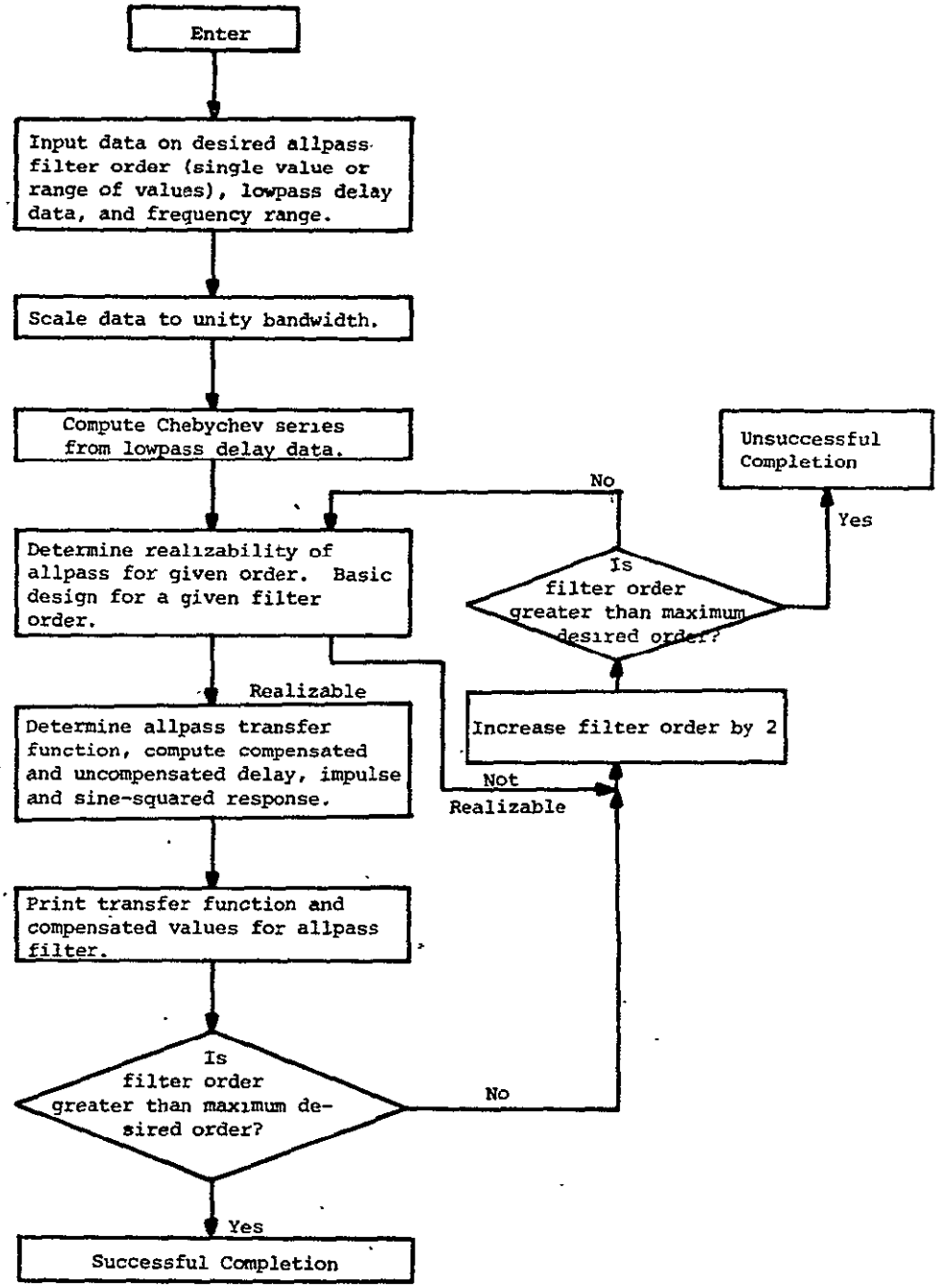


Figure 2.83 Basic Flowchart of Allpass Equalizer Program

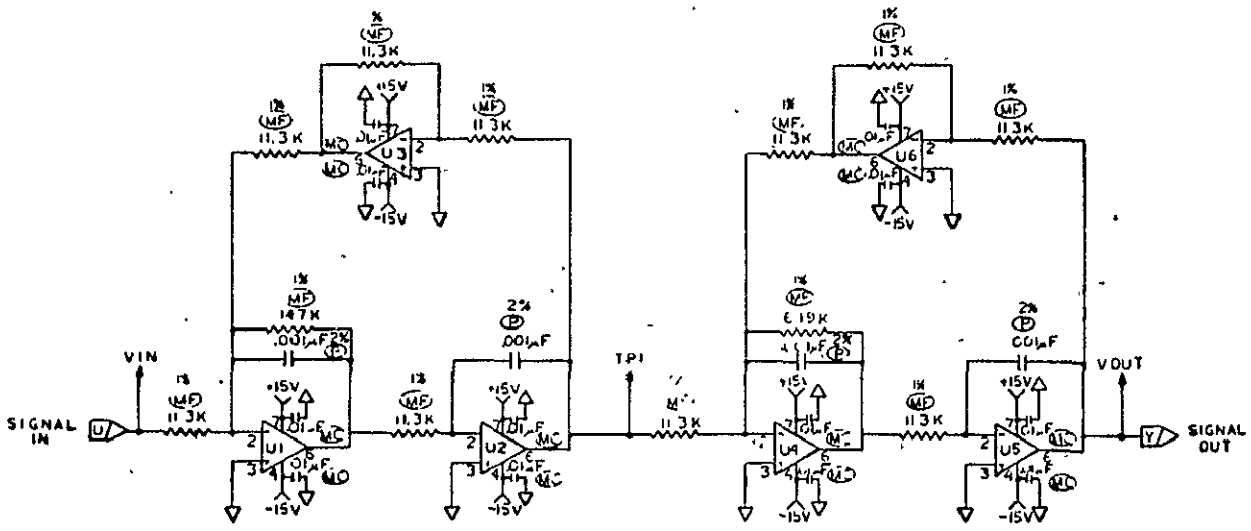


Figure 2.84 Four-pole Butterworth Low Pass Filter (f_c = 14 KHz)

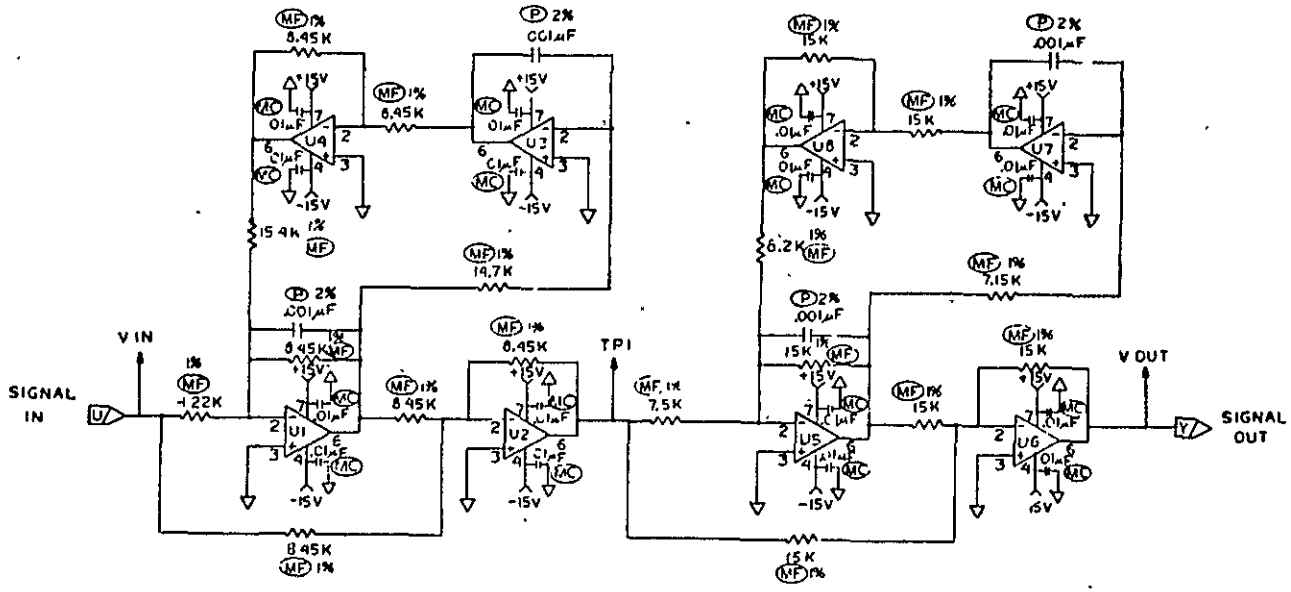


Figure 2.85 Optimum Four-pole Delay Corrector (f_c = 22 KHz)

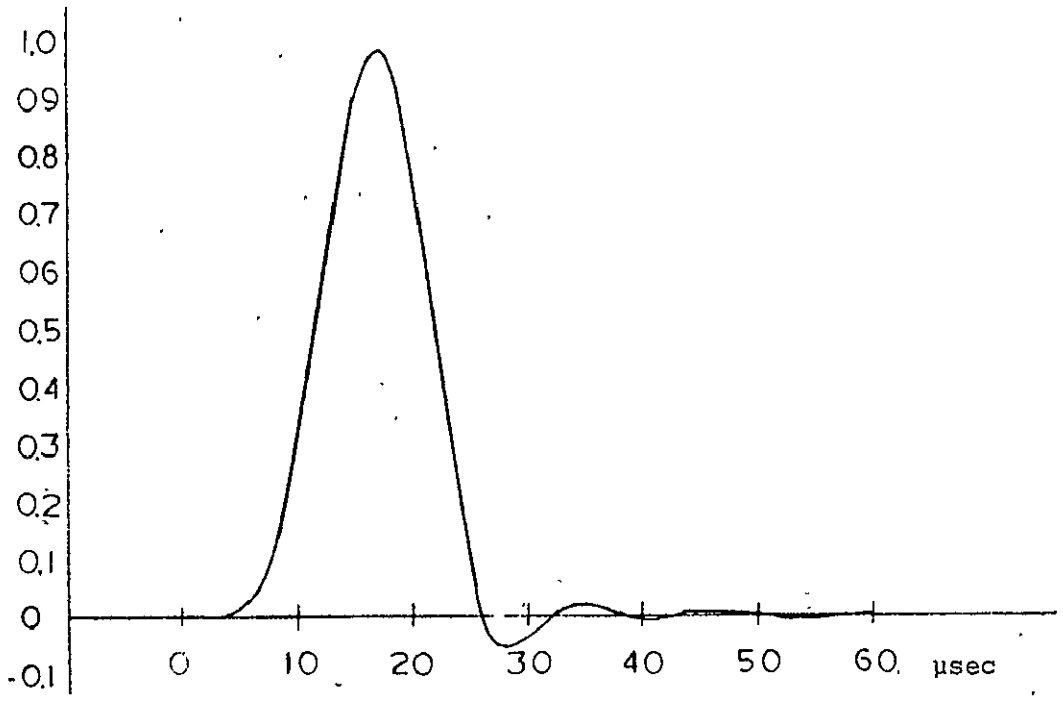


Figure 2.86 Computed Uncompensated Response to a Sine-Squared Pulse Input.

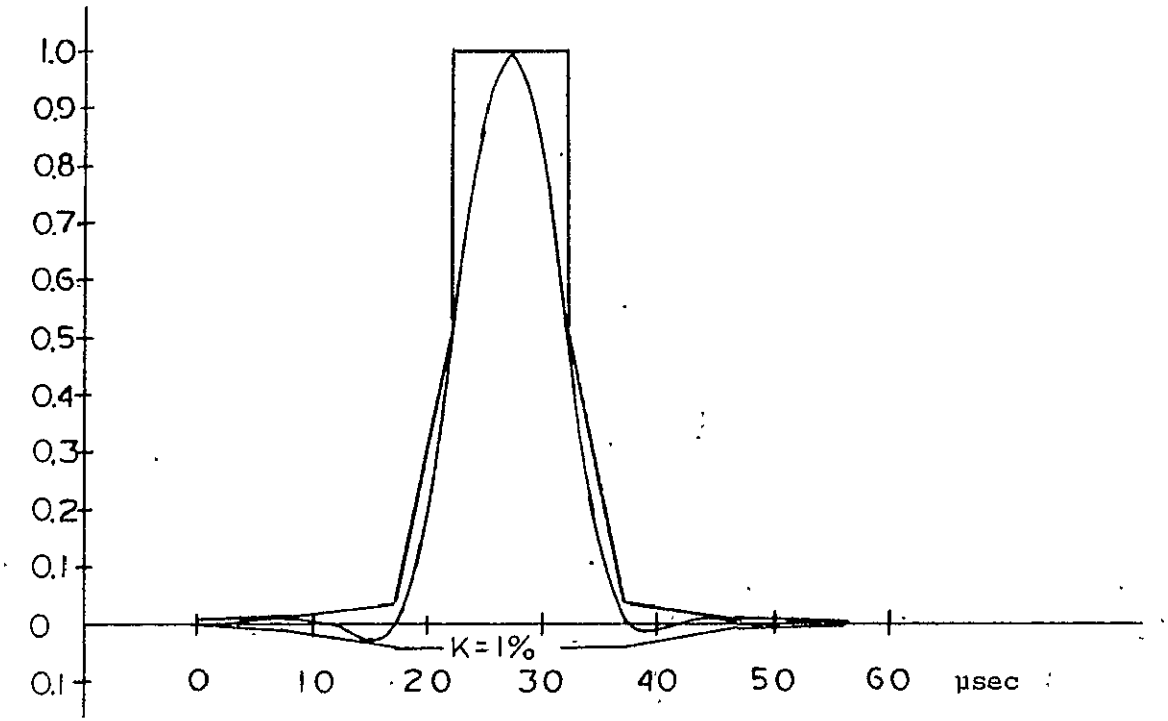
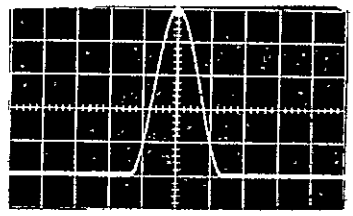
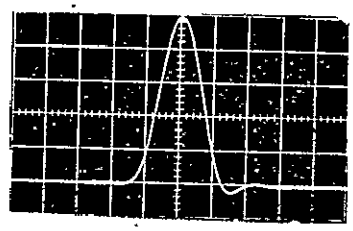


Figure 2.87 Computed Compensated Response to a Sine-Squared Pulse Input. (Note that response lies within K = 1% boundary.)



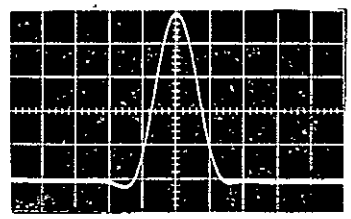
Vertical Scale - 0.2V/cm
Horizontal Scale - 10 μsec/cm

Figure 2.88 Synthesized Sine-Squared Pulse



Vertical Scale - 0.2V/cm
Horizontal Scale - 10 μsec/cm

Figure 2.89 Uncompensated Response



Vertical Scale - 0.2V/cm
Horitontal Scale - 10 μsec/cm

Figure 2.90 Compensated Response

using the digitally synthesized sine-squared pulse shown in Figure 2.88 . The measured uncompensated and compensated response are shown in Figures 2.89 and 2.90 respectively. Note the excellent agreement between predicted and actual responses.

The results obtained with actual VFRTS signals now follow. Figure 2.91 shows the method of synthesis of low frequency burst from the digital reference signals generated in the TBE. The lower oscilloscope trace is the input to the filter—horizonal sync followed by a burst of the reference frequency. Above is the filtered output ready for introduction to the narrowband channel. The second photograph (Fig. 2.92) shows an actual sine-squared pulse. A composite real-time television full field test signal (containing a sine-squared pulse) was recorded on disc, expanded, and stepped out at the low frequency reconstruction clock rate. The D/A converter output is shown in the lower trace; the delayed, filtered output is shown directly above. Note the excellent symmetry and lack of overshort in the sine-squared pulse.

The techniques employed for creating suitable equalized low pass filters have been shown to be effective in synthzing 24 db/octave VFRTS channel filters with "K-factors" of $\sim$ 1%. Performance has been verified by computer simulation and actual circuits realized using the generated specifications. These methods may be used to delay-correct any linear system whose initial delay profile is known analytically or by measurement. Further improvement of the entire system could be achieved by the application of delay correctors to

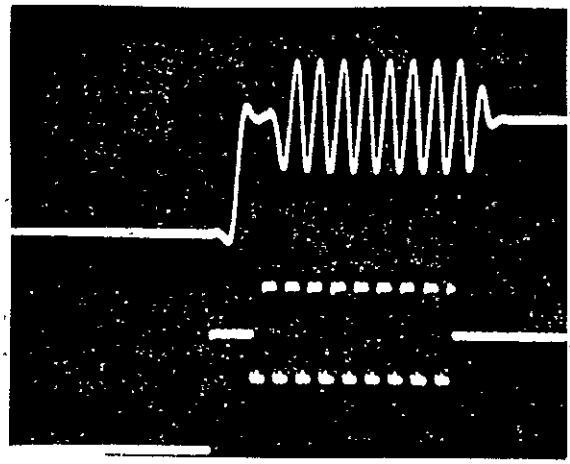


Figure 2.91 Low Frequency Horizontal Sync and Burst

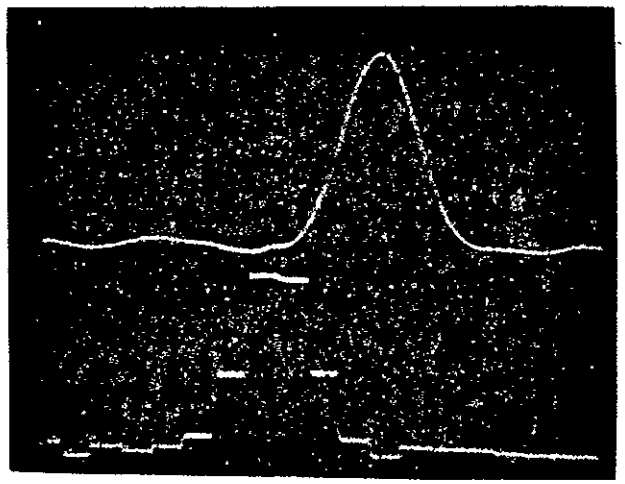


Figure 2.92 Timebase Expanded Sine-Squared Pulse

various subsystems in the Mod/Demod, TBE and TBC.

The next section will summarize the results of this chapter and outline the direction of effort in obtaining color transmission using the principles and techniques of the monochrome VFRTS system.

2.8 Conclusions

2.8.1 Monochrome System Summary. A simplex VFRTS transmitter/receiver was designed and constructed using a 6.5" video magnetic disc as a mass store for real-time television display. The inputs and outputs are completely compatible with real-time U.S. television standards.

The construction employed modular plug-in circuit cards for prototype development and alteration. Two separate enclosures are used for each terminal--one for the video disc and servo and one electronics bay containing the remaining processing circuitry.

Documentation of the system consists of block diagrams, schematic diagrams, and adjustment procedures where appropriate. A complete documentation package (manual) will be forthcoming including any remaining circuit diagrams not exhibited in the Appendices of this report.

The system has been tested and demonstrated using a simulated 14 KHz baseband channel with refresh rates of 5 seconds/field. Picture quality was judged to be consistent with design goals.

2.8.2 Adaptation of Color Transmission. A goal initially outlined included transmission of color images utilizing the same channel bandwidths and refresh times as the monochrome system (if possible). At present an operational system in the laboratory is capable of these transmissions. No alteration in channel capacity or penalty in update time was necessary. The design alternatives,

system reconfigurations and modification made will be the subject of Volume 2 of this report.

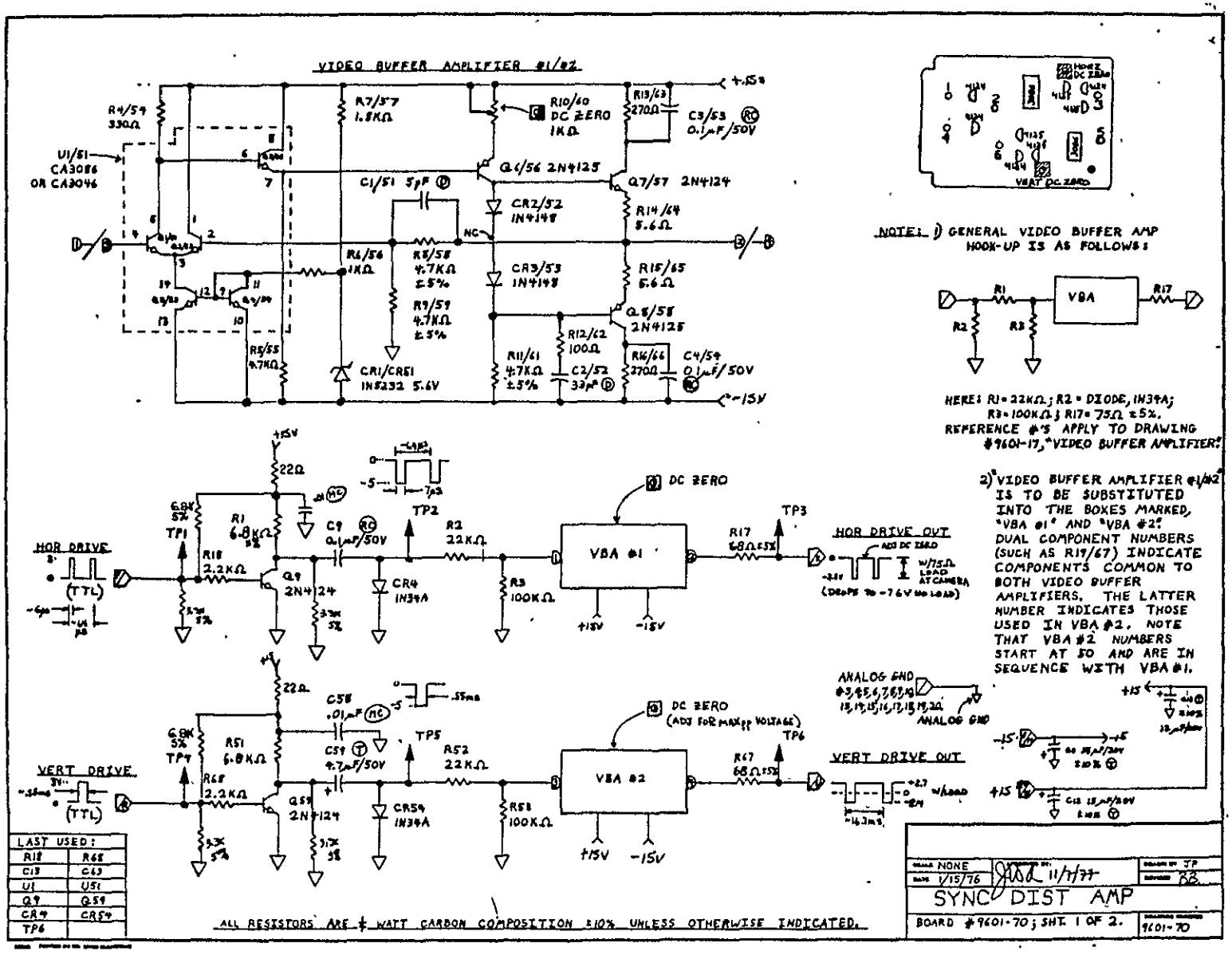
APPENDIX 2.1

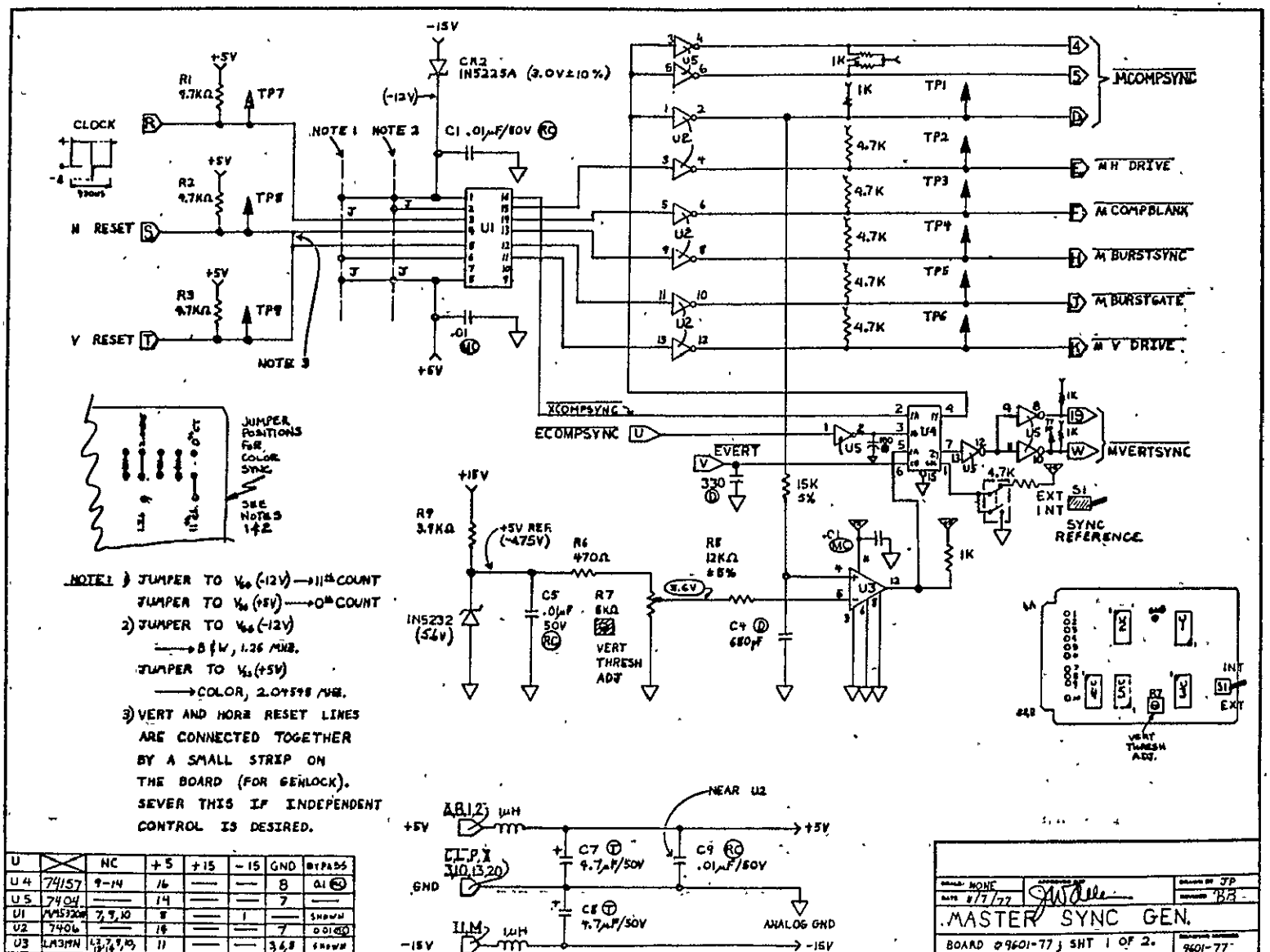
Master Timing/Sync Group Adjustment
Procedure and Schematic Diagram

Contents

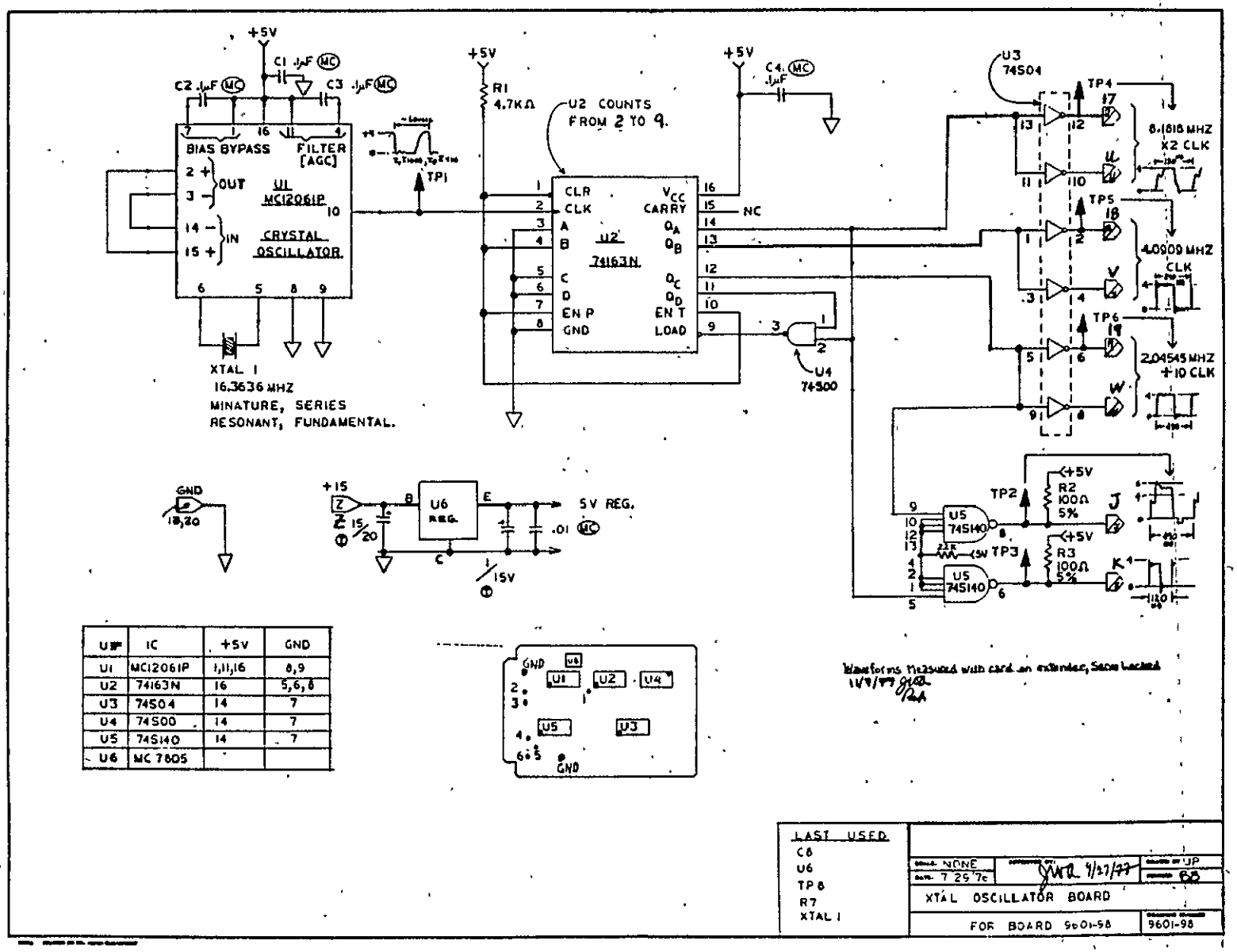
MASTER TIMING/SYNC GROUP ALIGNMENT PROCEDURE (Transmit/Receive)

Step	Board	Adjustment	
1	77	Vertical Threshold Adjustment	With 98 feeding MCK to 77, trigger CH1 of scope on TP6 $\overline{\text{MVDRIVE}}$ and display on CH2 TP10, MVERTSYNC. Rotate VERT THRESH ADJ. pot. until waveform on CH2 appears as in Fig. 3. Check voltage on pot wiper arm (via R8, 12K 5% resistor) and verify that it is about 3.6 VDC. This completes adjustment for board 77.
2	100	$\overline{\text{PLL HOLD}}$ Pulse Width Adjustment	Now insert board 100 into rack and trigger CH1 on negative going edge of pulse at TP15, $\overline{\text{PLL HOLD}}$. Rotate PLL HOLD pot. until pulse is 70μsec wide as in Fig. 13.
3	100	$\overline{\text{BLANKGATE}}$ Pulse Width Adjustment	Transfer probe to TP5, $\overline{\text{BLANKGATE}}$ and rotate BLANKGATE pot. for a pulse width of 350μsec as in Fig. 14. This completes adjustments for board 100
This completes adjustments for the Receive			Group. Continue to steps (4) - (6) for Transmit Group.
4	70	DC Zero; Horizontal Drive. (Sync to Camera)	Plug in board 70 and trigger CH1 on rising edge of HOR DRIVE signal at TP1; display several pulses. Display TP3 on CH2. With camera disconnected, a - 7.6V negative going pulse train should be present. Rotate HOR DC ZERO pot to place top of waveform at ∿0VDC.
5	70	DC Zero; Vertical Drive. (Sync to Camera)	Trigger scope CH1 on VERT DRIVE signal at TP4. Display TP6 on CH2; Clip a 75Ω resistive load from TP6 to ground. Adjust VERT DC ZERO pot for maximum peak to peak square wave (period ∿17 ms) at TP6. Top of waveform should be ∿ +2.7 VDC, bottom should be ∿ -2.3 VDC. Remove 75Ω resistor.
6	70	Camera Drive Signal Check Under Load	Plug in camera drive cable and verify 0 to -3.8 V pulse at TP3, and +2.7 to -2.4 Vdc pulse at TP6. This completes all group adjustments.


VIDEO BUFFER AMPLIFIER #1/#2
U1/51 CA3086 OR CA3046
R4/54 330Ω
R7/57 1.8KΩ
R10/60 DC ZERO 1KΩ
R13/63 270Ω
C3/53 0.1μF/50V
+15V
Q6/56 2N4125
Q7/57 2N4124
C1/51 5pF
CR2/52 IN4148
R14/64 5.6Ω
R6/56 1KΩ
R5/58 4.7KΩ ±5%
R9/59 4.7KΩ ±5%
CR3/53 IN4148
R15/65 5.6Ω
Q8/58 2N4125
R8/55 4.7KΩ
CR1/CR51 IN5232 5.6V
R11/61 4.7KΩ ±5%
R12/62 100Ω
C2/52 33pF
R16/66 270Ω
C4/54 0.1μF/50V
-15V
NOTE: 1) GENERAL VIDEO BUFFER AMP HOOK-UP IS AS FOLLOWS:
R1
R2
R3
VBA
R17
HERE: R1 = 22KΩ; R2 = DIODE, IN39A; R3 = 100KΩ; R17 = 75Ω ±5%.
REFERENCE #'S APPLY TO DRAWING #9601-17, "VIDEO BUFFER AMPLIFIER".
2) "VIDEO BUFFER AMPLIFIER #1/#2" IS TO BE SUBSTITUTED INTO THE BOXES MARKED, "VBA #1" AND "VBA #2". DUAL COMPONENT NUMBERS (SUCH AS R19/67) INDICATE COMPONENTS COMMON TO BOTH VIDEO BUFFER AMPLIFIERS. THE LATTER NUMBER INDICATES THOSE USED IN VBA #2. NOTE THAT VBA #2 NUMBERS START AT 50 AND ARE IN SEQUENCE WITH VBA #1.
+15V
22Ω
HOR DRIVE
(TTL)
TP1
R18 2.2KΩ
R1 6.8KΩ
C9 0.1μF/50V
TP2
R2 22KΩ
CR4 IN39A
R3 100KΩ
DC ZERO
VBA #1
R17 68Ω ±5%
TP3
HOR DRIVE OUT
ADJ DC ZERO
W/75Ω LOAD AT CAMERA
-15V
VERT DRIVE
(TTL)
TP4
R68 2.2KΩ
R51 6.8KΩ
C58 .01μF
C59 4.7μF/50V
TP5
R52 22KΩ
CR54 IN39A
R53 100KΩ
DC ZERO (ADJ FOR MAX p-p VOLTAGE)
VBA #2
R67 68Ω ±5%
TP6
VERT DRIVE OUT
w/load
ANALOG GND
#3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20
ANALOG GND
+15
-15
LAST USED:
R18 R68
C13 C63
U1 U51
Q9 Q59
CR4 CR54
TP6
ALL RESISTORS ARE ¼ WATT CARBON COMPOSITION ±10% UNLESS OTHERWISE INDICATED.
NONE
1/15/76
11/7/77
SYNC DIST AMP
BOARD #9601-70; SHT. 1 OF 2.
9601-70



U		NC	+5	+15	-15	GND	BYPASS
U4	74157	9-14	16	—	—	8	.01
U5	7404	—	14	—	—	7	—
U1	AM9330B	7,9,10	8	—	1	—	SHOWN
U2	7406	—	14	—	—	7	.01
U3	LM311N	1,2,7,9,10,12,13,14	11	—	—	3,6,8	SHOWN

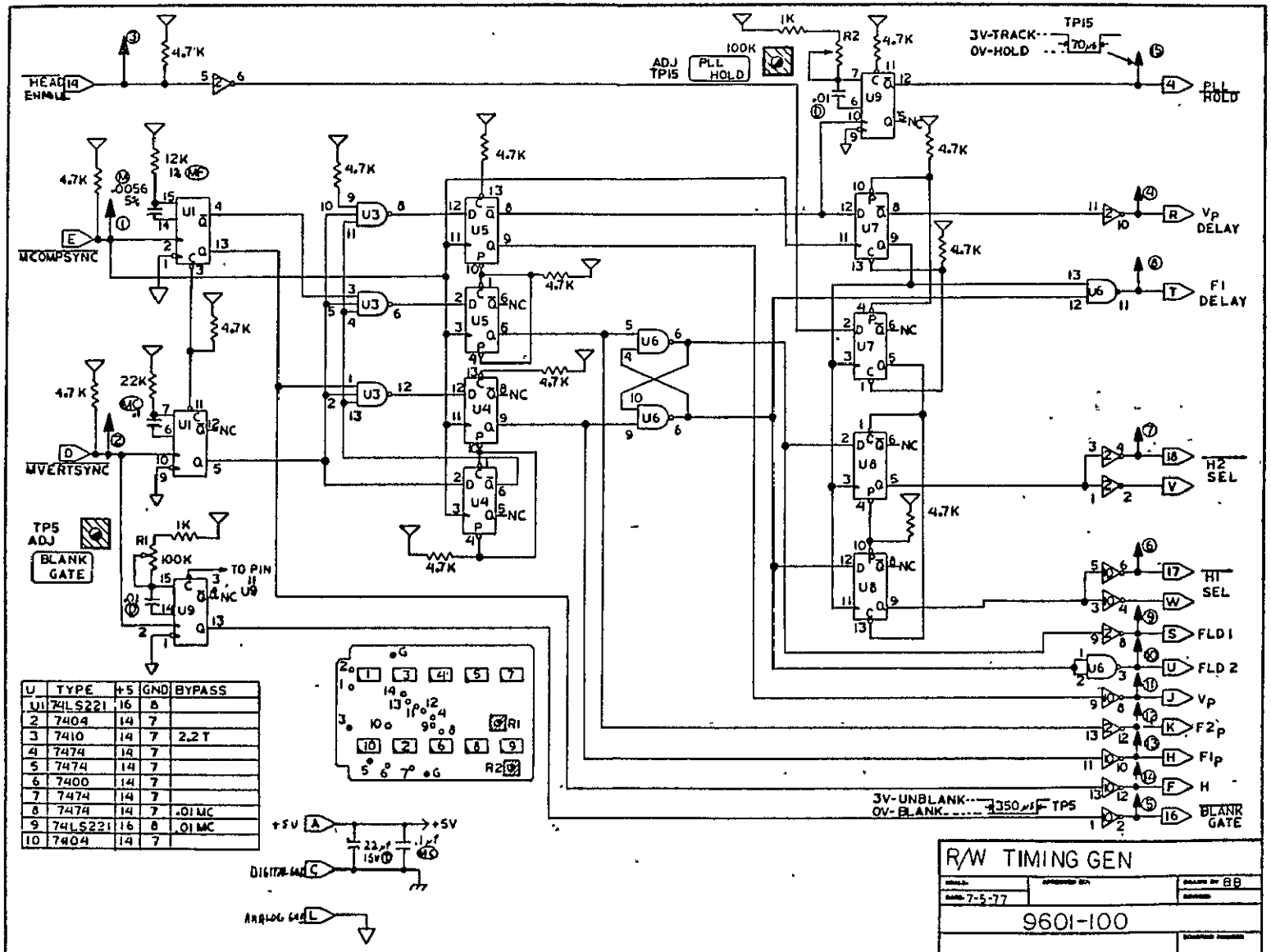


U#	IC	+5V	GND
U1	MC12061P	1,11,16	8,9
U2	74163N	16	5,6,8
U3	74S04	14	7
U4	74S00	14	7
U5	74S140	14	7
U6	MC 7805		

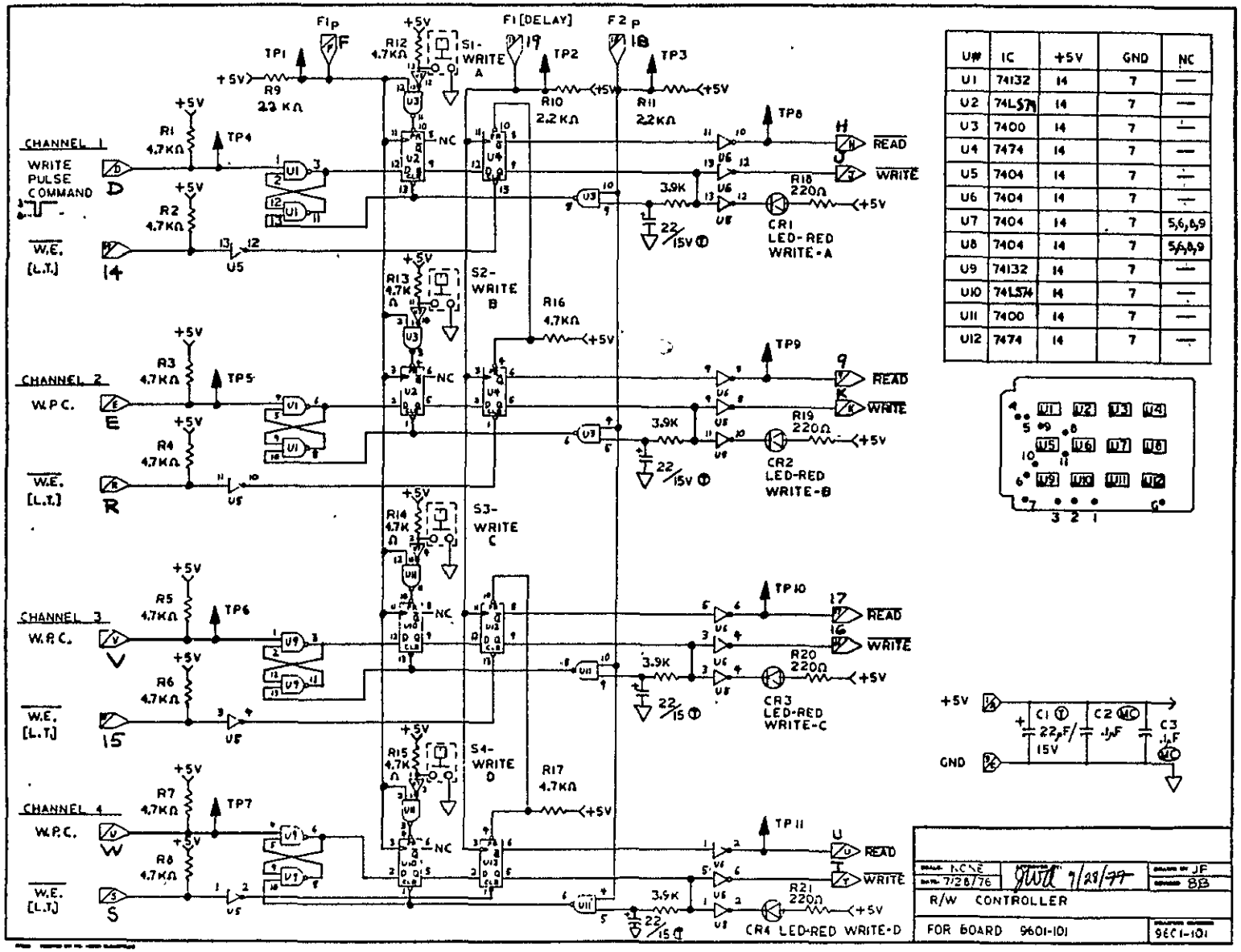
Waveforms measured with card on extender, Scope locked
11/9/77

LAST USED
C8
U6
TP8
R7
XTAL 1

NONE	9/27/77	UP
7 25 '7c		88
XTAL OSCILLATOR BOARD		
FOR BOARD 9601-98		9601-98



U	TYPE	+5	GND	BYPASS
U1	74LS221	16	8	
2	7404	14	7	
3	7410	14	7	2,2 T
4	7474	14	7	
5	7474	14	7	
6	7400	14	7	
7	7474	14	7	
8	7474	14	7	.01 MC
9	74LS221	16	8	.01 MC
10	7404	14	7	



U#	IC	+5V	GND	NC
U1	74132	14	7	—
U2	74LS74	14	7	—
U3	7400	14	7	—
U4	7474	14	7	—
U5	7404	14	7	—
U6	7404	14	7	—
U7	7404	14	7	5,6,8,9
U8	7404	14	7	5,6,8,9
U9	74132	14	7	—
U10	74LS74	14	7	—
U11	7400	14	7	—
U12	7474	14	7	—

APPENDIX 2.2

VIDEO MAGNETIC DISC SPECIFICATIONS

Outer Diameter	6.5" ± 030"
Inner Diameter	0.789" ± .001"
Thickness	0.2" ± .005"
Concentricity	< 0.001"
Flatness (each side)	< 0.001" TIR
Coplanarity	< 0.001"
Base Material	Aluminum
Magnetic Coating	Nickel-Cobalt, 6 micro-inches nominal thickness
Overcoat	Nickel oxide
Coercivity	600 Oersteds
Surface Finish	0.5 micro-inch aa or better
Surface Defects	Each surface shall be free of defects over a range of radii extending to within 1/4" of O.D. and 1/2" of I.D.

APPENDIX 2.3

BRUSHLESS DC SERVO MOTOR

APPENDIX

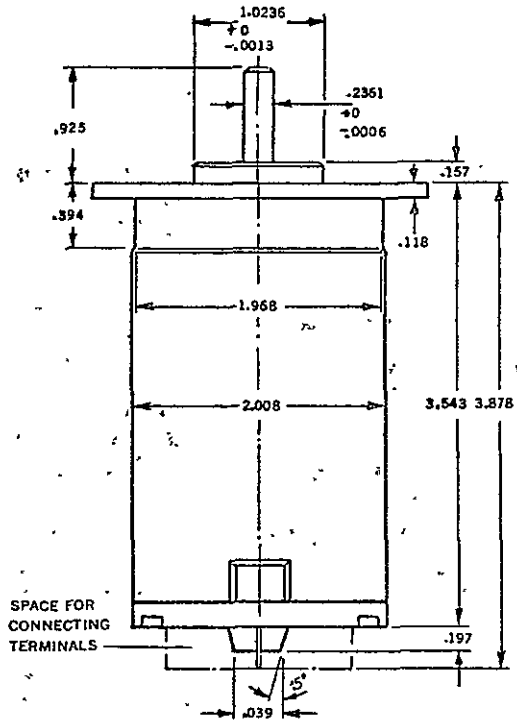
BRUSHLESS DC MOTOR SPECIFICATIONS

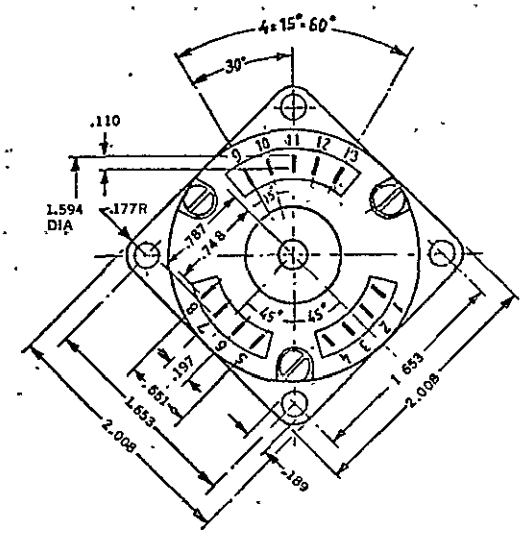
1.	Motor Type	Siemens 1AD5000-0B
2.	Dimensions	See Dwg. No. BDCM 100277
3.	Enclosure	Dust and drop-resistant
4.	Acoustical Noise	< 30 db
5.	R.F. Interference	None
6.	Bearings	Ball
7.	Lubrication	Lifetime
8.	Unattended life	> 10,000 Hrs.
9.	Weight	26 oz.
10.	Voltage Range	20.4 to 26.5 V
11.	Speed Range	600 to 6000 RPM
12.	Efficiency	50% or better
13.	Temp (°C minimum)	-10°
14.	Temp (°C maximum	+55°
15.	Temp (°C rise)	5°
16.	Duty	Continuous
17.	Starting torque	12 oz. in.
18.	Max. Cont. running torque	7 oz. in.
19.	Max. Cont. motor current	2.5 amp.
20.	Torque Constant	2.8 oz. in./amp.
21.	Winding Resistance	4 x 1 ohm

22.	Winding Inductance	4 x 0.3 millihenry
23.	Electrical time constant	0.3 millisec
24.	EMF constant	2.18 VDC/1000 RPM
25.	Mechanical time constant	90 millisec
26.	Rotor Interia	5.8×10^{-3} oz. in. sec^2
26	Shaft axial play	0.0039 to 0.0118"

Source: Siemens Corp.

Dwg. No. BDCM 100281



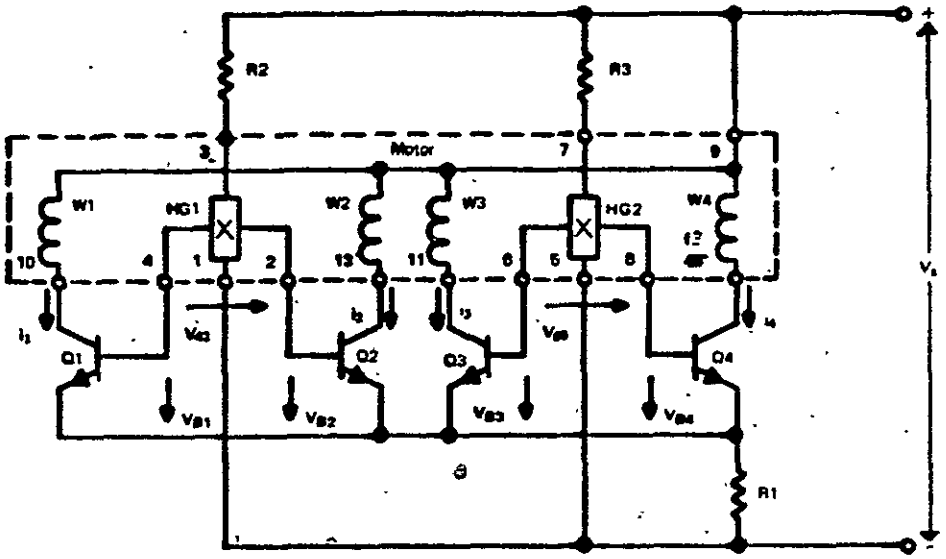


WHEN TOLERANCES ARE NOT SHOWN THESE TOLERANCES WILL APPLY SRN7168 OR 114						
.039 TO 118	.118 TO .393	.393 TO .708	708 TO 1 181	1 181 TO 1 968	1 968 TO 3 149	3 149 TO 4 724
± 004	± 006	± 008	± 010	± 012	± 014	± 016

SIEMENS	SIEMENS CORPORATION POWER EQUIPMENT DIVISION 186 Wood Avenue South, Iselin, New Jersey 08830.
BRUSHLESS D C MOTOR	1AD50. .–OB

TKB 99 61 173 REV. B	SIZE A	DRAWING NO. BDCM 100 277	ISSUE 6 28 73
SCALE·	UNIT WT. ≈27 oz.	SHEET 1	OF 1

Figure 7



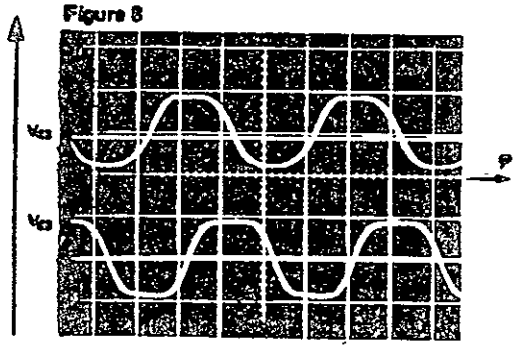
Electronic Motor with 180 Degree Commutator Circuit

180 Degree Commutator

A complete 180 degree circuit diagram is shown in Figure 7. The Hall generators are supplied with a constant control current from the supply voltage through the resistors R2 and R3. With the permanent magnet rotor running the Hall generators are exposed to a sinusoidal magnetic field. Therefore, the Hall signal voltage also is a sine wave. Typical wave shape and phase relationship of the Hall generator signals is shown in Figure 8. The Hall generator output signal terminals are directly connected to the base of its respective commutator transistor. By operating the commutator transistors in their linear region, it can be assumed that the base voltages and therefore, also the collector currents and winding currents, maintain the same sine wave shape. Figure 9 shows the typical base voltage wave shapes and Figure 10 shows the typical winding currents of the 180 degree commutator. Each winding conducts current for 180 degrees. At the same time, there are always two windings conducting current.

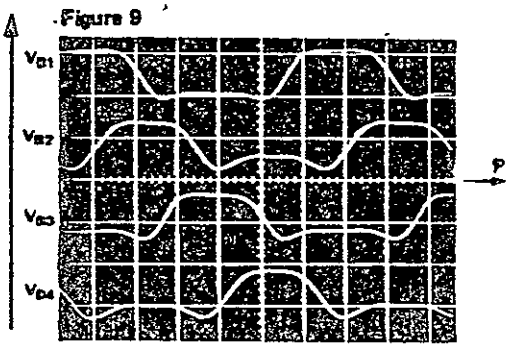
Since the winding current is a sine wave, the winding flux is also a sine wave. In Figure 11 the north pole of the rotor is in position I under the Hall generator HG1. The Hall voltages of HG1 therefore have the maximum amplitudes. The amplitude is positive at the base of commutator transistor Q1 and negative at the base of Q2. This means that Q1 is turned on at a collector current corresponding to the maximum amplitude of the sine wave current of winding W1, and Q2 is turned off. Q3 and Q4 are also turned off since HG2 is in a neutral magnetic position.

Figure 8



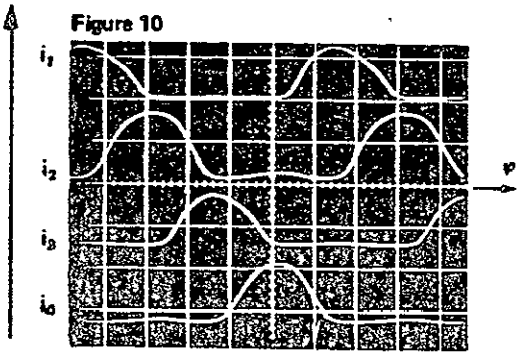
Typical Hall Generator output signal voltages

Figure 9



Typical Base Voltages of Commutator Transistors in 180 Degree Commutator

Figure 10



Typical Winding Currents for 180 Degree Commutation

At this moment the rotor flux Φ_R and the flux Φ_W of winding W1 are at an angle of 90 degrees. The rotor torque is given therefore by

$$T = C \Phi_R \Phi_W \sin 90^\circ = C \Phi_R \Phi_W$$

After the rotor has moved over the angle θ to position II, HG2 also is exposed to the rotor flux. Since the Hall voltage is a projection of the rotor flux, the winding flux of W1 follows a cosine function. Because of the physical separation of the Hall generators by 90 degrees, Q3 is turned on according to a sine function. The winding flux of W3 therefore is $\Phi_W \sin \theta$. In rotor position II, the two windings W1 and W3 are energized and developing a rotor torque. The torque from W1 follows the function

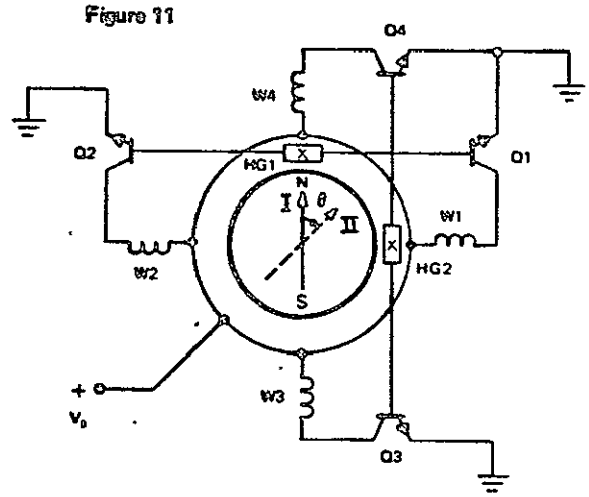
$$T_1 = C \Phi_R \Phi_W \cos^2 \theta$$

The torque from W3 follows the function

$$T_2 = C \Phi_R \Phi_W \sin^2 \theta$$

The sum of the torques from both energized winding circuits is therefore constant and equal to $C \Phi_W \Phi_R$ for any rotor position over the range of $0^\circ \leq \theta \leq 90^\circ$. After a rotation over 90 degrees winding W3 takes over from W1 and W2 from W3, etc., so that the torque over a full rotation is always constant. The angle between the rotor flux and the resulting flux of the windings is always 90 degrees. The advantage of the 180 degree commutator is that the cogging is reduced to a minimum. Only minor deviations from this ideal situation are experienced due to nonlinearities in the characteristics of the Hall generators and transistors.

Figure 11

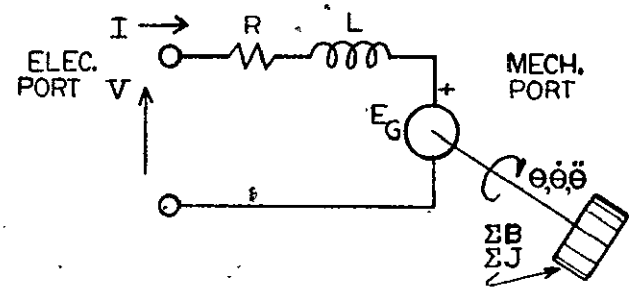


Layout of Winding Circuits and Hall Generators

APPENDIX 2.4

DERIVATION OF MOTOR VOLTAGE AND CURRENT TRANSFER FUNCTIONS

A. $\frac{\theta(s)}{V(s)}$ Voltage Transfer Function



DC MOTOR MODEL

Figure A2.4.1

R = winding resistance

L = winding inductance

ΣB = total rotational viscous damping

ΣJ = total moment of inertia (motor and load)

E_g = back EMF developed by motor

K_E = motor electrical constant (volts/rad/sec)

K_T = motor torque constant (oz.-in./amp)

$$\Sigma \text{ Torques} = \Sigma J \ddot{\theta} + \Sigma B \dot{\theta} \qquad (1$$

$$= T_{electrical} + T_{mech}$$

But $T_{mech} = 0$

$$T_{elec} = \Sigma J \ddot{\theta} + \Sigma B \dot{\theta} = K_T I \quad (2)$$

and $$E_g = K_E \dot{\theta} \quad (3)$$

Now

$$V = RE + L\dot{I} + K_E \dot{\theta} \quad (4)$$

Solving (2) for I we get

$$I = \left(\frac{\Sigma J}{K_T} \right) \ddot{\theta} + \left(\frac{\Sigma B}{K_T} \right) \dot{\theta} \quad (5)$$

and substituting in (4) for I yields

$$V(t) = R \left[\left(\frac{\Sigma J}{K_T} \right) \ddot{\theta} + \left(\frac{\Sigma J}{K_T} \right) \dot{\theta} \right] + L \left[\left(\frac{\Sigma J}{K_T} \right) \theta + \left(\frac{\Sigma B}{K_T} \right) \ddot{\theta} \right] + K_E \dot{\theta} \quad (6)$$

Taking the LaPlace Transform and regrouping terms gives

$$V(s) = \left(\frac{L\Sigma J}{K_T} \right) s^3 \theta(s) + \left(\frac{R\Sigma J + L\Sigma B}{K_T} \right) s^2 \theta(s) + \left(\frac{R\Sigma B}{K_T} + K_E \right) s\theta(s) \quad (7)$$

$$\frac{\theta(s)}{V(s)} = \frac{1}{s\left[\left(\frac{L\Sigma J}{K_T} \right) s^2 + \left(\frac{R\Sigma J + L\Sigma B}{K_T} \right) s + \left(\frac{R\Sigma B}{K_T} + K_E \right) \right.} \quad (8)$$

$$\frac{\Sigma(s)}{V(s)} = \frac{\left(\frac{K_T}{L\Sigma J}\right)}{s\left[s^2 + \left(\frac{R}{L} + \frac{\Sigma B}{\Sigma J}\right)s + \left(\frac{R\Sigma B}{L\Sigma J} + \frac{K_E K_T}{L\Sigma J}\right)\right]} \tag{9}$$

Neglecting the terms due to damping (which is a reasonable assumption) yields:

$$\frac{\theta(s)}{V(s)} = \frac{(K_T/L\Sigma J)}{s\left(s^2 + (R/L)s + \frac{K_E K_T}{L\Sigma J}\right)} \tag{10}$$

Now define $\tau_e = \frac{L}{R}$, $\tau_m = \frac{R\Sigma J}{K_E K_T}$

For motor without any inertial load

$$90 \text{ msec} = \tau_m >> \tau_e = 0.3 \text{ millisec}$$

so that

$$\frac{R}{L} \simeq \frac{R}{L} + \frac{K_E K_T}{R\Sigma J}$$

Thus we may write

$$\frac{\theta(s)}{V(s)} = \frac{K_T/L\Sigma J}{s\left(s^2 + \left(\frac{R}{L} + \frac{K_E K_T}{R\Sigma J}\right)S + \left(\frac{K_E K_T}{L\Sigma J}\right)\right.} \tag{11}$$

$$\frac{\theta(s)}{V(s)} = \frac{K_T/L\Sigma J}{s\left(s + \frac{1}{\tau_m}\right)\left(s + \frac{1}{\tau_e}\right)} \tag{12}$$

$$\frac{\theta(s)}{V(s)} = \frac{(1/K_E)}{s(s\,\tau_m + 1)(s\,\tau_e + 1)} \qquad (13)$$

and in general since $\tau_m >> \tau_e$ we get

$$\frac{\theta(s)}{V(s)} = \frac{(1/K_E)}{s(s\,\tau_m + 1)}$$

The actual transfer function may now be calculated as follows:

$$1/K_E = \{(2.18\ \frac{V}{1000RPM}) \cdot (\frac{60}{2\pi \cdot 1000}\ \frac{RPM}{RAD/SEC})\}^{-1}$$

$$1/K_E = \{\ 20.82\ \frac{V \cdot SEC}{RAD}\ \}^{-1}$$

$$1/K_E = \underline{0.048\ \frac{RAD}{VOLT \cdot SEC}}$$

$$\omega_m = \frac{K_E\ K_T}{R(\Sigma J)} \qquad (\Sigma J \text{ calc: see App. 2.5})$$

$$\omega_m = \{\ \frac{(20.82 \times 10^{-3}\ \frac{VOLT \cdot SEC}{RAD})(2.05 \times 10^{-2}\ \frac{Kg\ m^2}{Amp\ sec^2})}{(1\ \frac{Volt}{Amp})\ (111 \times 10^{-5}\ Kgm^2)}\ \}$$

$$\omega_m = \underline{0.385\ \frac{RAD}{SEC}}$$

$$\underline{\tau_m = (\omega_m)^{-1} = 2.60\ sec}$$

$$\frac{\theta(s)}{V(s)} = \frac{0.048}{s\{s(2.6) + 1\}} \tag{14a}$$

2. B. $\frac{\theta(s)}{I(s)}$ Current Transfer Function

$$T_{elec} = I K_T = \Sigma J \ddot{\theta} + \Sigma B \dot{\theta} \tag{15}$$

$$I(s)K_T = (\Sigma J)\, s^2\theta(s) + (\Sigma B)s\theta(s) \tag{16}$$

$$\frac{(s)}{I(s)} = \frac{(K_T/\Sigma J)}{s(s + \Sigma B/\Sigma J)} \tag{17}$$

Note the simplicity which results when the current transfer function is considered (R, L, and K_E do not appear). A pole is contributed by the root due to finite rotational damping B_T; if no losses were present, then the denominator would reduce to s^2.

Now

$$\omega_B = \left(\frac{\Sigma B}{\Sigma J}\right) \tag{18}$$

From (15) at constant RPM,

$$I K_T = \Sigma J \overset{0}{\ddot{\theta}} + \Sigma B \dot{\theta} \tag{19}$$

$$\Sigma B = \frac{I K_T}{\dot{\theta}} \tag{19a}$$

Hence

$$\omega_B = \frac{I K_T}{\dot{\theta}\Sigma J} \tag{20}$$

Using a 4" diameter disc, data were taken to determine a value for ω_B.

TABLE A2.4.1

Tach Freq (KHz)	Motor Voltage (Volts)	Motor Current (Amp)	RPM*
22.64	0.500	0.200	2592
35.74	0.600	0.240	4092
44.70	0.700	0.280	5118
54.86	0.800	0.320	6282

*524 counts/rev from tach disc

Fig. A2.4.2 fits a straight line through the data points and yields an estimated value for ΣB as 2.34×10^{-8} (nt.m.sec) or 2.34×10^{-8} ($Kg.m^2.sec^{-1}$).

Thus, $\omega_B = \frac{2.34 \times 10^{-8} \ Kgm^2/sec}{47 \times 10^{-5} \ Kgm^2} = 4.98 \times 10^{-5}$ Rad/sec or

7.92×10^{-6} Hz

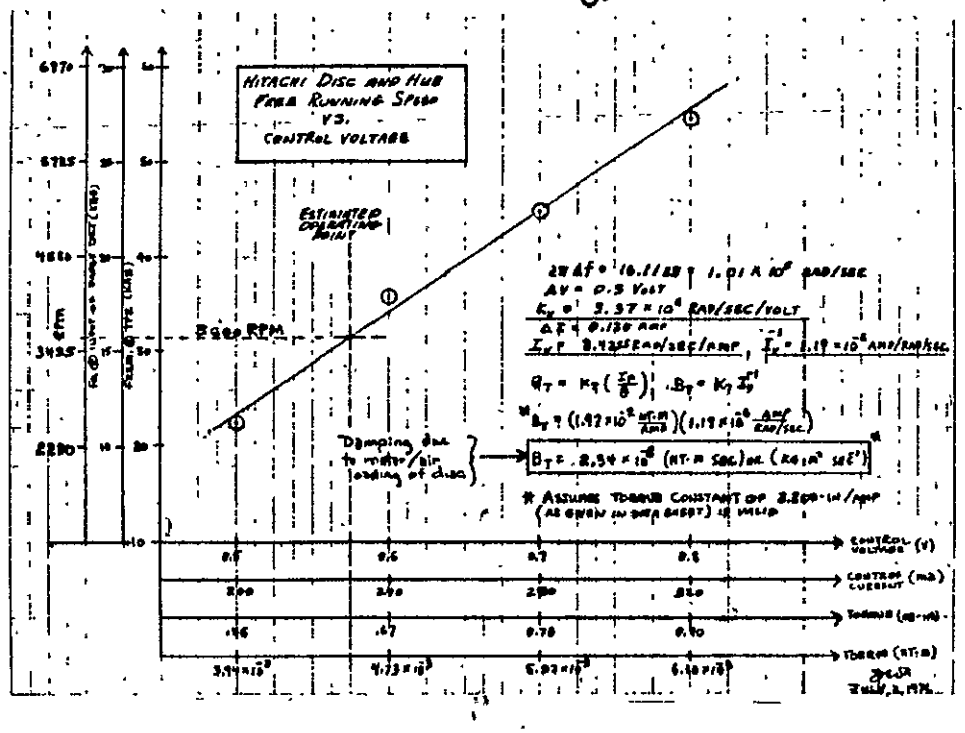


Figure A2.4.2

In general, ω_B can be scaled to any diameter disc if it is recognized that B is proportional to the area and steam velocity (see Fig. A2.4.3).

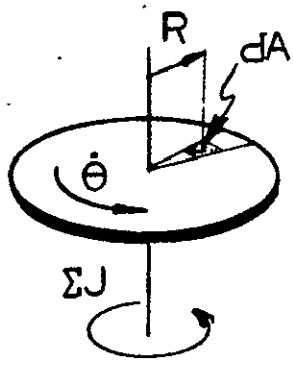


Figure A2.4.3

$$dA = drd\theta$$

$V \propto r$ at constant $\dot{\theta}$

$$dB \propto VdA \propto rdA$$

$$B \propto \int_0^{2\pi} \int_0^{R} rdrd\theta \propto r^2 \qquad (21)$$

But $\Sigma J \propto r^4$ (assuming density and thickness remain essentially the same).

Thus, $\omega_B \propto r^2/r^4 \propto 1/r^2$

Hence for a 6.5" diameter disc

$$\omega_B = \left(\frac{2}{3.25}\right)^2 \omega_{B_{4"}} = 0.38\ \omega_{B_{4"}} \qquad (22)$$

which still yields a value of approximately 3×10^{-6} Hz. This frequency is so low that the pole will be assumed to lie at the origin and the motor transfer function to be:

$$\frac{\theta(s)}{I(s)} = \frac{(K_T/\Sigma J)}{s^2} \qquad (23)$$

We now calculate the exact transfer function.

$$(K_T/\Sigma J) = \left\{ \frac{(2.05\times10^{-2}\ \frac{\text{Kg m}^2}{\text{Amp sec}^2})}{111 \times 10^{-5}\ \text{Kg m}^2} \right\}$$

$$(K_T/\Sigma J) = \underline{18.47\ \text{sec}^{-2}\ \text{amp}}$$

or

$$\frac{\theta(s)}{I(s)} = \frac{18.47}{s^2} \qquad (23a)$$

APPENDIX 2.5

MOMENT OF INERTIA CALCULATION ($J_{zz}=\Sigma J$)

See Fig. A2.5.1 for configuration.

$$T_1 = 0.200'' = 5.08 \times 10^{-3}\ M$$

$$T_2 = 0.915'' = 2.32 \times 10^{-2}\ M$$

$$R_1 = 3.25'' = 8.25 \times 10^{-2}\ M$$

$$R_2 = 1.00'' = 2.54 \times 10^{-2}\ M$$

Spindle and Disc Mat'l Alum , $\rho \cong 2.8\ gm/cm^3$

$$\cong 2.8 \times 10^3\ K_g/M^3$$

$$J_{Spindle} = \frac{\rho\pi R_2^4}{2}(T_2-T_1) = 3.32 \times 10^{-5}\ K_gM^2$$

$$J_{Disc} = \frac{\rho\pi R_1^4}{2}(T_1) = 103.5 \times 10^{-5}\ K_gM^2$$

$$J_{Rotor/Shaft} = 5.8 \times 10^{-3}\ oz.in.sec^2 = 4.18 \times 10^{-5}\ K_gM^2$$

$$J_{zz} = J_{Spindle} + J_{Disc} + J_{Rotor/Shaft} = 111 \times 10^{-5}\ K_gM^2$$

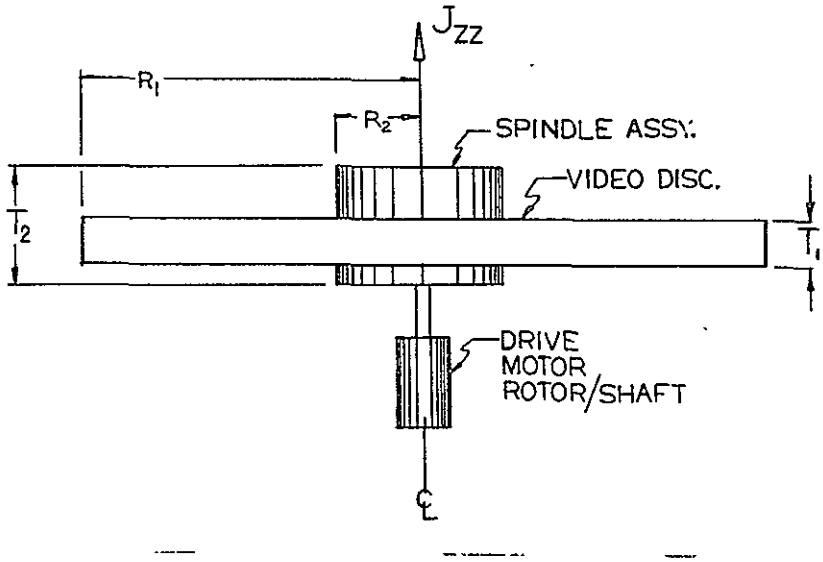


Figure A2.5.1 Video Disc, Spindle and Rotor Configuration for J_{zz} Calculation

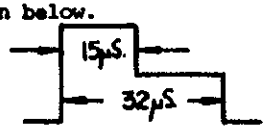
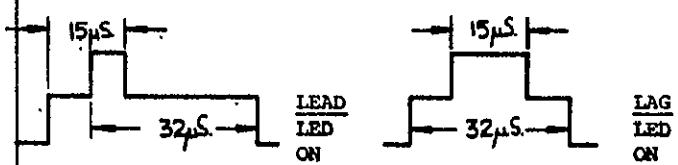
APPENDIX 2.6

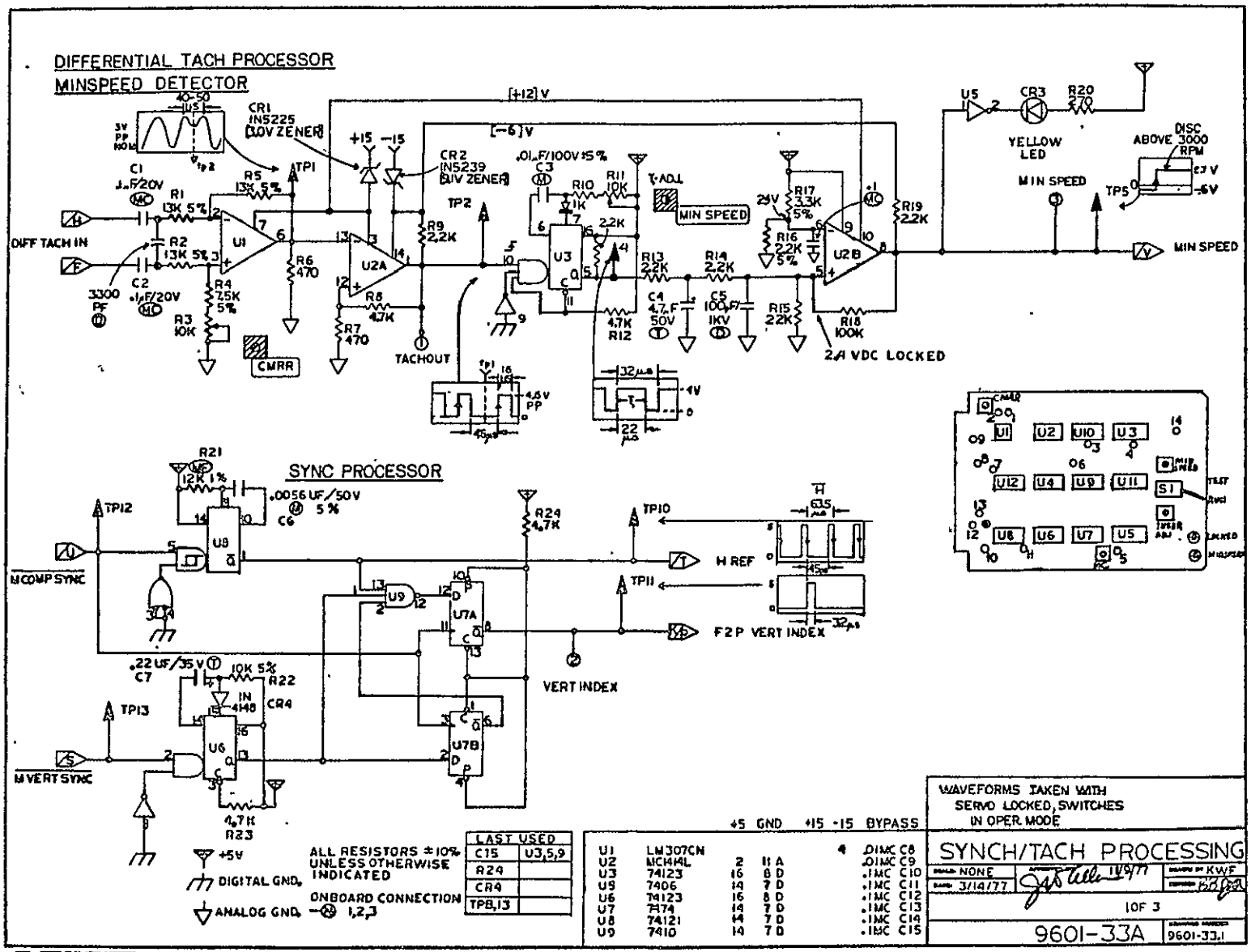
Adjustment Procedure and Schematic Diagrams for Servo System

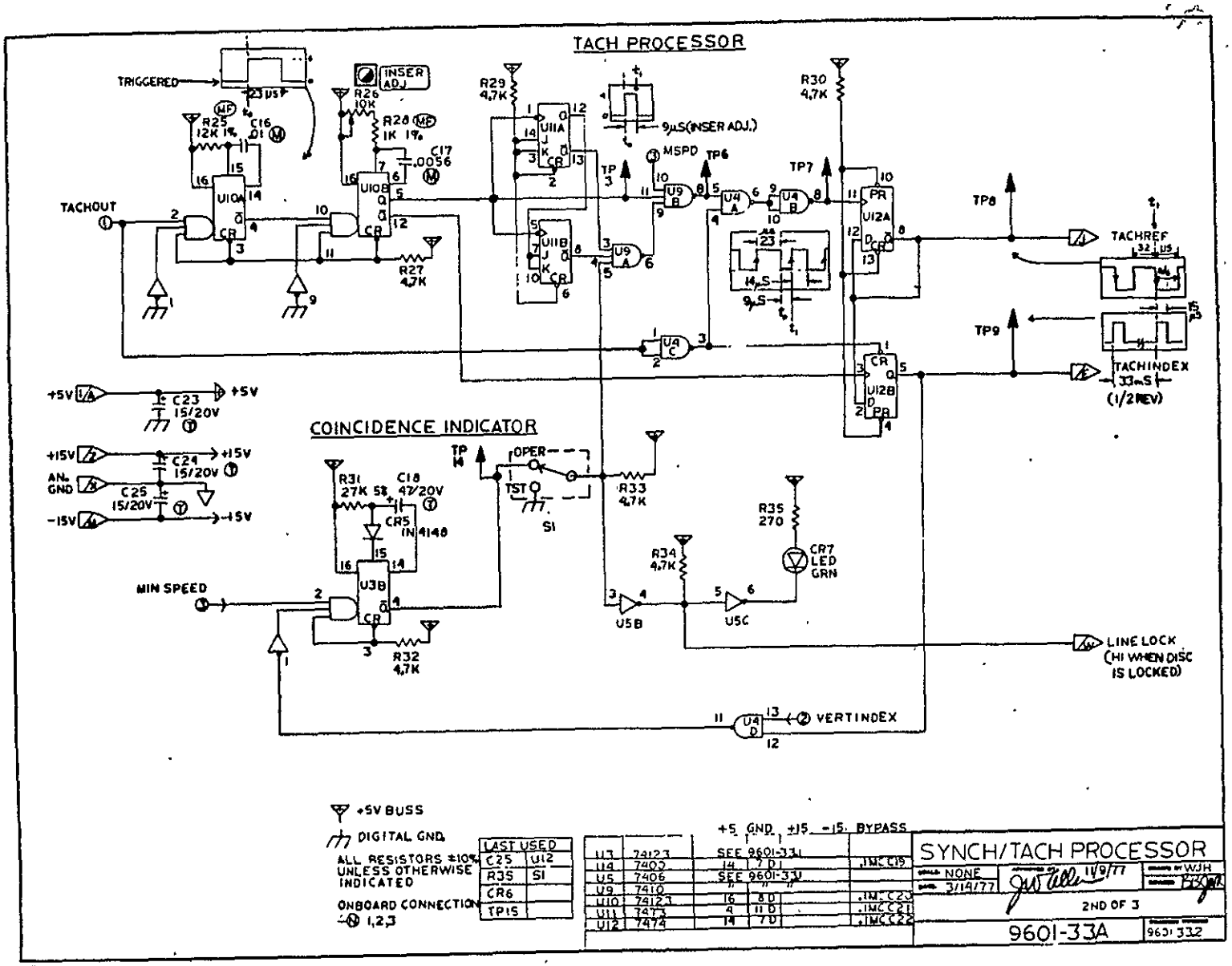
Contents

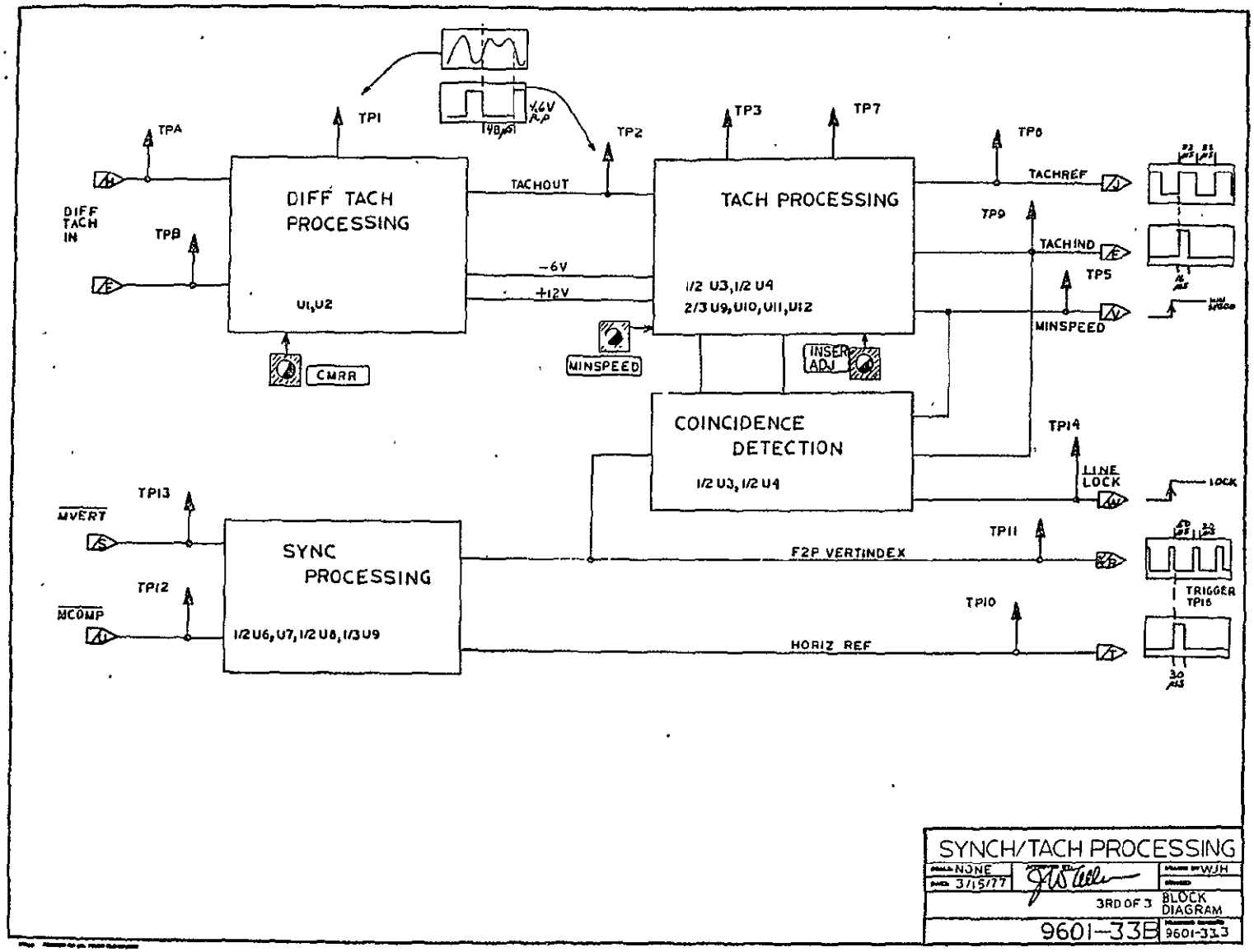
SERVO GROUP ALIGNMENT PROCEDURE (Transmit/Receive)

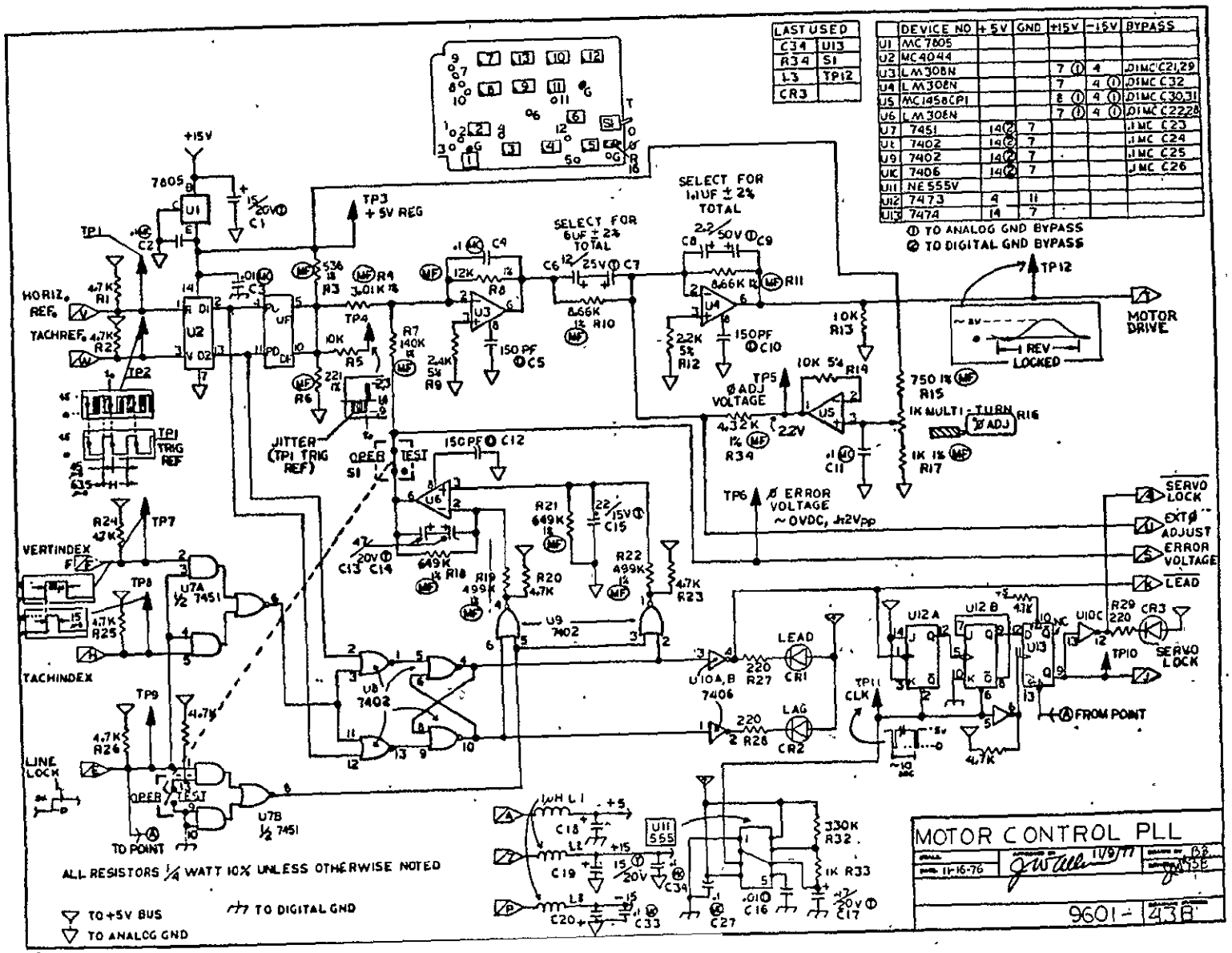
Step	Board	Adjustment	
1	108	Motor Current Limit	With 43B out of system, jump 108, TP4 to +15V while differentially monitoring the voltage between 108/TP2,3. Adjust Current Lim pot. for 2.5V at the TP's which equals 1 A of motor current. Leave on.
2	108	Optical Tach Check	With motor running, check each Output (pins 7,8) of MC1733CL on 108 for approx $2V_{pp}$ tach signal (should look sinusoidal). Adjust tack pickup arm angle if necessary to produce required signal. Turn off motor by removing jumper to TP4
3	33A	Sync Processor Check	Trigger Scope CH1 at TP13 on 33A and observe $\overline{\text{MVERTSYNC}}$ (Fig. 13). Serrated pulse should last ∿180μs and occur every vertical interval. Now display on CH2 TP12, MCOMPSYNC and check relationship shown in Fig's. 12, 13.
			Now transfer CH1 to TP13 and observe $F2_p$ vertindex, Fig. 11, which should occur every ∿33msec, Place TP13 on EXT trigger and siplay TP12 (MCOMPSYNC) and TP10 (HREF) on CH's 1 and 2 respectively. Verify timing shown in Fig's 10, 12. This completes check of sync processor section of 33A.
4	33A	CMRR Adjust	Insure that P1 of 108 is not connected. Apply $4V_{pp}$ 15KHZ sine wave to TPA and TPB of 33A. Adjust CMRR pot for minimum output at TP1 on 33A. Replace P1 of 108.
5	108, 33A	Minspeed	Attach a variable DC power supply (0-15V) to TP4 of 108 with 43B out of system; set to 0Vdc', Motor should be stationary. Slowly increase voltage while monitoring TP1 of 33A; Verify ∿$3V_{pp}$. Now go to TP2, triggering on rising edge. Adjust DC supply voltage until period of square wave is about 32μs (See Fig. 2). Place TP4 on CH2 and adjust MINSPEED pot for 22μsec wide positive-going pulse. Yellow minspeed LED should be on. Verify ∿2.4 Vdc at pin 5 of U2B on 33A and ∿2.7 Vdc at TP5 (Fig. 6). Now turn DC power supply down to 0V and check to see that as disc slows and LED goes off verifying that minspeed had dropped out. Reset supply to previous voltage and note acquisition of minspeed again. Record DC setting to produce the TACHOUT signal shown in Fig. 2. DCP.S._____ Vdc
6	33A	Inner Pulse Adjustment	With disc running at speed under control of DCP.S. in previous step monitor U10 of 33A, pin 4 or 10 and check for missing pulse det. output as shown in Fig. 3. If pulse is absent, carefully adjust tach pickup arm angle until pulse appears. This pulse identifies the once-around index on the optical tach. disc.

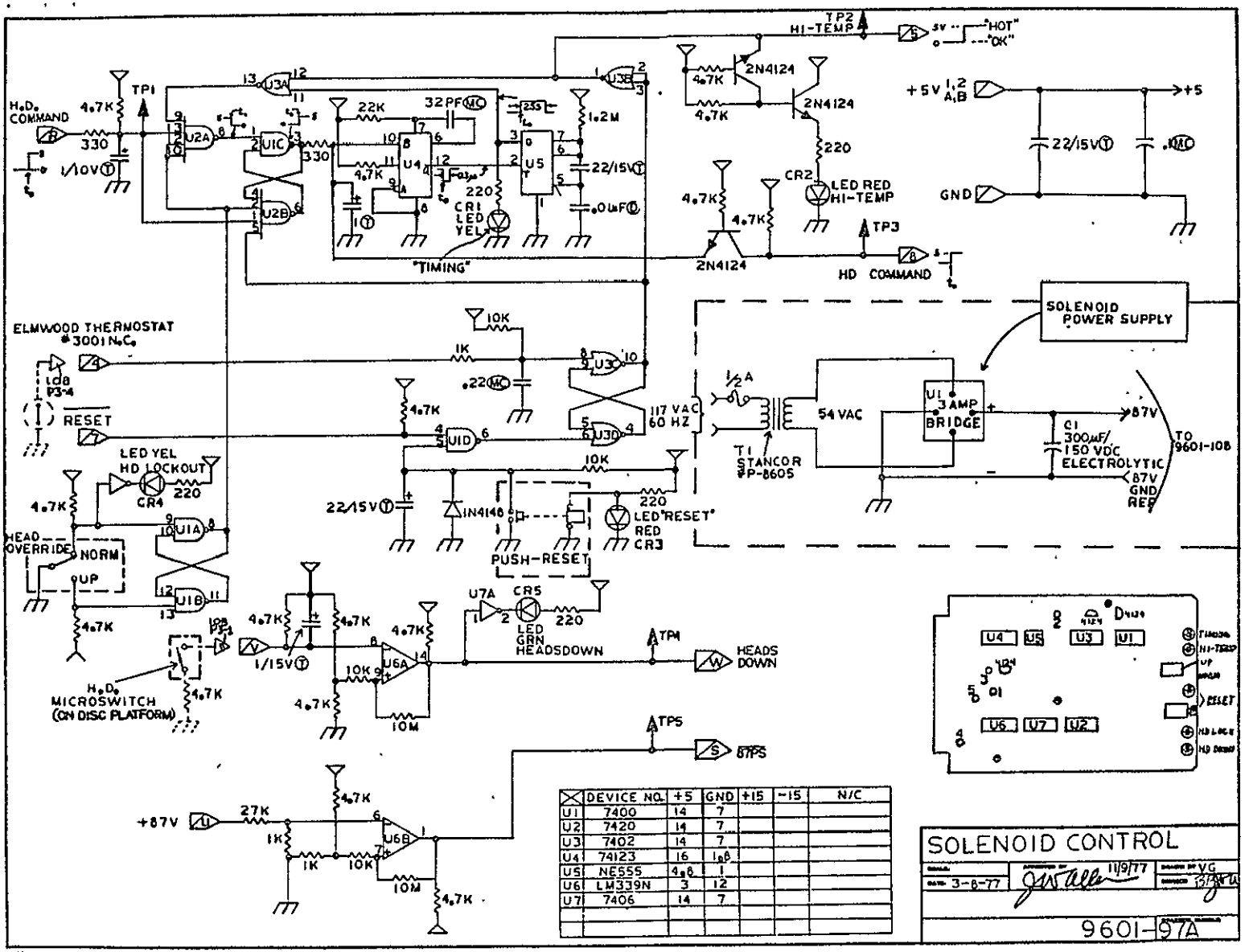
Step	Board	Adjustment	
			Trigger CH1 on pulse of Fig. 3 and display TP3 on CH2. Rotate INSER ADJ. pot until pulse width on CH2 is ∿9μs (see Fig. 4). Interpulse period should be 15 to 20msec (∿17 ideally).
7	43B	Initial Calibration of 43B	Plug 43B into an unconnected slot in rack so that it receives bus power. Check TP3 for 5V ±5%. Set pot R16 ϕADJ for 2.2VDC at TP5. Check TP11 for narrow negative-going pulse with interval of about 10sec. This completes initial check of 43B.
8	33A, 43B 108	High Freq PLL servo control lock check, ϕADJ open loop calibration	Remove DC P. S. from 108 and replace P1. Set switches on 33A and 43B to TEST position. Connect CH1 of scope to 43B, TP7 (trig ref) and CH2 to 43B, TP8. Energize system. When HF lock is achieved, pulse on CH2 should stop moving with respect to CH1. Now move switch on 33A to OPER position and note that CH2 pulse, the TACH INDEX is slowing moving. It should stop when it lines up with the VERTINDEX pulse displayed on CH1. Put scope into Add mode and adjust R16 on 43B for a display as shown below. 
9	43B	Low Freq Phase Detector Check	Note the following behavior; with R16 as an adjustment, verify the following two operating conditions.
10	43B	ϕ Corrector Loop Adjustment	Adj R16 until LAG/LEAD LED's trigger equally; this places timing relationship of VERTINDEX and TACHINDEX as shown at end of step (8). Place S1 on 43B into OPER mode. LAG/LEAD LED's should now flicker automatically indicating that compensating loop is in operation. Observe waveform at TP6 on 43B and trim R16 to place average value of voltage at 0V. This completes servo alignment procedure.
			




TACH PROCESSOR
TRIGGERED
23 µS
INSER ADJ
R26 10K
R25 12K 1%
C16 .01
R28 1K 1%
C17 .0056
TACHOUT
U10A
U10B
R27 4.7K
R29 4.7K
U11A
U11B
9µS(INSER ADJ.)
MSPD
TP6
TP7
TP8
TP9
R30 4.7K
U12A
U12B
TACHREF
TACHINDEX
33mS
(1/2 REV)
+5V
C23 15/20V
+15V
C24 15/20V
ANL GND
C25 15/20V
-15V
COINCIDENCE INDICATOR
R31 27K 5%
C18 47/20V
CR5 IN 4148
MIN SPEED
U3B
R32 4.7K
TP 14
OPER
TST
S1
R33 4.7K
R34 4.7K
R35 270
CR7 LED GRN
U5B
U5C
LINE LOCK (HI WHEN DISC IS LOCKED)
VERTINDEX
+5V BUSS
DIGITAL GND
ALL RESISTORS ±10% UNLESS OTHERWISE INDICATED
ONBOARD CONNECTION 1,2,3
LAST USED
C25 U12
R35 S1
CR6
TP15
+5 GND +15 -15 BYPASS
U3 74123 SEE 9601-331
U4 7402 14 7 0
U5 7406 SEE 9601-331
U9 7410
U10 74123 16 8 0
U11 7474 4 11 0
U12 7474 14 7 0
.1MC C15
.1MC C23
.1MC C21
.1MC C22
SYNCH/TACH PROCESSOR
NONE
3/14/77
11/9/77
WJH
2ND OF 3
9601-33A
9601 332




LAST USED
C34 U13
R34 S1
L3 TP12
CR3
DEVICE NO +5V GND +15V -15V BYPASS
U1 MC7805
U2 MC4044
U3 LM308N
U4 LM308N
U5 MC1458CP1
U6 LM308N
U7 7451
U8 7402
U9 7402
U10 7406
U11 NE555V
U12 7473
U13 7474
① TO ANALOG GND BYPASS
② TO DIGITAL GND BYPASS
+15V
7805
TP1
TP2
TP3 +5V REG
TP4
TP5 ØADJ VOLTAGE
TP6 Ø ERROR VOLTAGE ~0VDC, .4V2Vpp
TP7
TP8
TP9
TP10
TP11 CLK
TP12
HORIZ. REF.
TACHREF.
TACHINDEX
VERTINDEX
LINE LOCK
JITTER (TP1 TRIG REF)
TP1 TRIG REF
OPER
TEST
S1
SELECT FOR 1.1UF ± 2% TOTAL
SELECT FOR 6UF ± 2% TOTAL
150PF C5
150PF C10
150PF C12
22V
REV LOCKED
MOTOR DRIVE
10K 5% R14
750 1% R15
1K MULTI-TURN R16
ØADJ
1K 1% R17
LEAD
LAG
SERVO LOCK
EXT Ø ADJUST
ERROR VOLTAGE
LEAD
FROM POINT
TO POINT
ALL RESISTORS 1/4 WATT 10% UNLESS OTHERWISE NOTED
TO +5V BUS
TO ANALOG GND
TO DIGITAL GND
MOTOR CONTROL PLL
11-16-76
9601-438

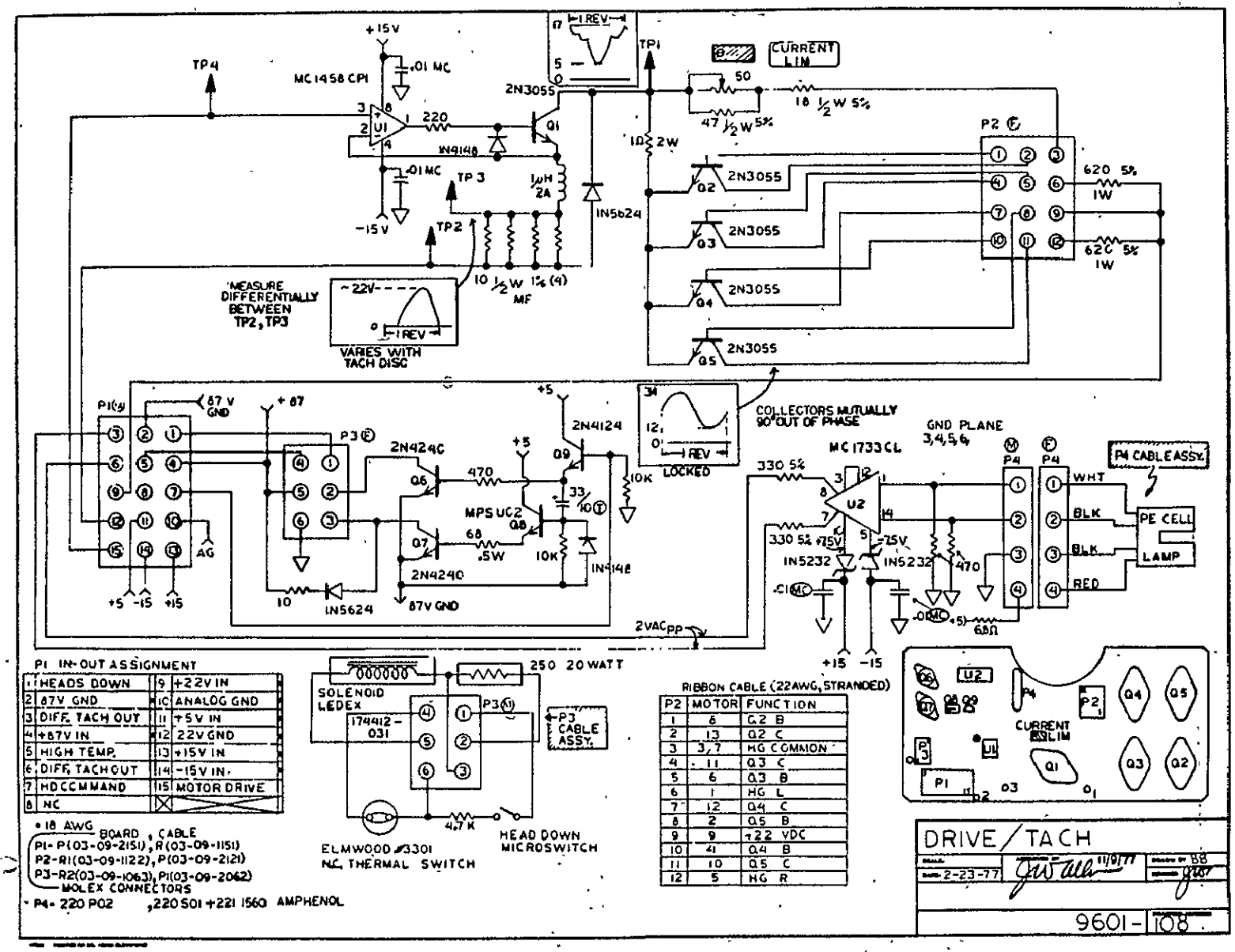


	DEVICE NO.	+5	GND	+15	-15	N/C
U1	7400	14	7			
U2	7420	14	7			
U3	7402	14	7			
U4	74123	16	8			
U5	NE555	8	1			
U6	LM339N	3	12			
U7	7406	14	7			

SOLENOID CONTROL

DRAWN 3-8-77 APPROVED 11/9/77 DESIGNED VG

9601-97A


+15V
TP4
MC1458CPI
.01 MC
U1
220
Q1
2N3055
1N914B
.01MC
-15V
TP3
TP2
1µH 2A
1N5624
TP1
CURRENT LIM
50
47 ½W 5%
18 ½W 5%
1Ω 2W
Q2 2N3055
Q3 2N3055
Q4 2N3055
Q5 2N3055
P2
620 5% 1W
620 5% 1W
MEASURE DIFFERENTIALLY BETWEEN TP2, TP3
~22V
1 REV
VARIES WITH TACH DISC
10 ½W 1% (4) MF
COLLECTORS MUTUALLY 90° OUT OF PHASE
LOCKED
GND PLANE 3,4,5,6
MC1733CL
U2
330 5%
330 5% ±75V
IN5232
±75V
470
.01MC
.01MC
68Ω
+15 -15
2VACPP
P1
87V GND
+87
P3
2N4240
2N4124
Q6
Q7
Q8
Q9
470
MPS UC2
68 .5W
10K
33 10T
10K
IN914B
10
IN5624
87V GND
+5 -15 +15
AG
P4
P4 CABLE ASSY.
WHT
BLK
BLK
RED
PE CELL
LAMP
P1 IN-OUT ASSIGNMENT
1 HEADS DOWN
2 87V GND
3 DIFF. TACH OUT
4 +87V IN
5 HIGH TEMP.
6 DIFF. TACH OUT
7 HD COMMAND
8 NC
9 +22V IN
10 ANALOG GND
11 +5V IN
12 22V GND
13 +15V IN
14 -15V IN
15 MOTOR DRIVE
• 18 AWG
BOARD ; CABLE
P1- P(03-09-2151), R(03-09-1151)
P2- R1(03-09-1122), P(03-09-2121)
P3- R2(03-09-1063), P1(03-09-2062)
MOLEX CONNECTORS
• P4- 220 P02 ,220 501 +221 1560 AMPHENOL
SOLENOID LEDEX
174412-031
250 20 WATT
P3
P3 CABLE ASSY.
4.7K
ELMWOOD #3301
N.C. THERMAL SWITCH
HEAD DOWN MICROSWITCH
RIBBON CABLE (22AWG, STRANDED)
P2 1 MOTOR 6 FUNCTION Q2 B
2 13 Q2 C
3 3,7 HG COMMON
4 11 Q3 C
5 6 Q3 B
6 1 HG L
7 12 Q4 C
8 2 Q5 B
9 9 +22 VDC
10 41 Q4 B
11 10 Q5 C
12 5 HG R
CURRENT LIM
DRIVE / TACH
2-23-77
9601-108

Appendix 2.7

VIDEO HEAD SPECIFICATIONS

Mechanical:

Track Width	.014 ± .001 inch
Gap Length	50 ± 10 microinches
Minimum Gap Depth	.0015 inch
Load Force	Adjustable, 4 to 10 grams
Winding	16 turns nominal

Electrical:

A. Record	
Maximum inductance (end-end at 140 KHz)	13 microHenrys
Maximum Resistance (end-end, DC)	4 Ohms
Maximum p-p Record Current (end-end)	75 milliamperes
B. Reproduce	
Minimum p-p Output (end-end)	
a) 1000 ips and 7 MHz	7 millivolts
b) 2000 ips and 10 MHz	20 millivolts

Appendix 2.8

MOD/DEMOD GROUP ADJUSTMENT PROCEDURE AND SCHEMATIC DIAGRAMS

Contents

MOD/DEMOD GROUP ALIGNMENT
(FRAME WRITE-TRANSMIT TERMINAL)

BOARDS:

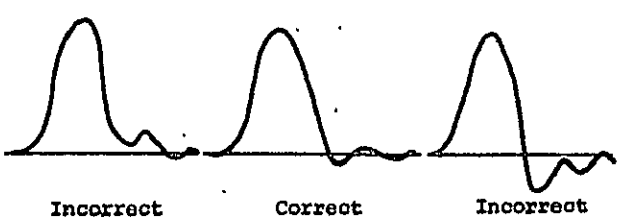
106 A/P	Proc Amp
105 A/P	Video Amp
21 A	MOD
57 A	Video R/W
23 A	DEMOD
106 A/D	Proc Amp
105 A	Video Amp

Section # 1

Preliminary Board Alignments:

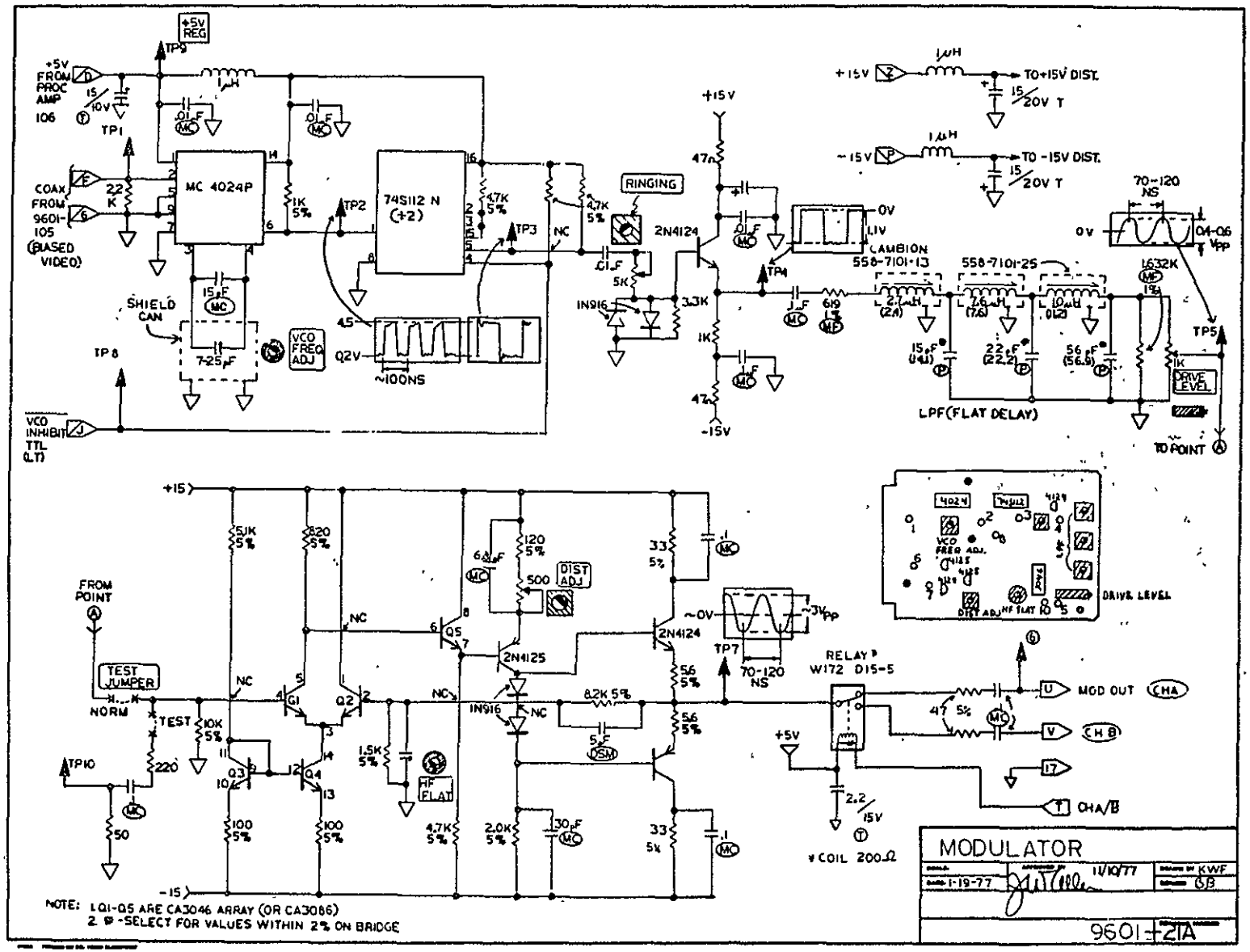
Step	Board	Adjustment	
1	106A/P,D	Video Preamp. Check	Using TEK R147 test generator, inject IV$_{pp}$ multiburst (reduced burst amplitude) at TP1; be sure 75Ω termination is in. Check TP2 for ∿6V$_{pp}$ with blanking at +0.5V. Multiburst amplitudes should be constant ±0.5 db.
2	106A/P,D	Burst Trap Adjustment	Trigger scope CH1 at TP2 to display back porch ω/color burst. Display on CH2 TP3 and rotate TRAP ADJ trimmer capacitor to minimize burst amplitude at TP3.
3	106A/P,D	Sync. Sep. Check	Move CH2 probe to TP4 and check for a 0 to +5V 3-5μs positive-going pulse delayed from horizontal sync by 0.3 to 0.5μsec.
4	106A/P,D	Vert. Sync. Sep. Adjust.	Using vertical sync. separator triggering on Tek 465 scope, trigger CH1 from TP1 and display two vertical intervals. Place CH2 on TP7, EVERTSYNC, and adjust VERT SYNC THRESHOLD pot. for clean sync (refer to master Timing/Sync Group timing diagram, Fig. 3 for correct appearance). It is necessary to use expanded sweep for this display.
5	106A/P,D	Comp. Sync. Sep. Adjust.	Remove CH2 probe and place on TP6, $\overline{\text{ECOMPSYNC}}$, and view slightly larger region of vertical interval. Adjust COMPSYNC THRESHOLD pot. for clean sync. (refer to Fig. 1 of same timing diagram). Make certain all equalization pulses are present.
6	106A/P,D	Clamp Keyer Check	Before proceeding, check to see that jumper from LM319, pin 7 to 74121N, pins 3, 4 is connected; also check for jumper from 74121N pin 5 to LM319, pin 12. (This insures that local stripped sync. is driving the keyer). Now place CH2 probe on TP8 and observe a 0 to 3V positive-going 1.2μsec pulse rising approx. 0.3-0.5μsec after the falling edge of horizontal sync. pulses. The pulses should be present for all equalizing pulses in the vertical interval section.

Step	Boards	Adjustment	
7	106A/P,D	Tilt. Adjust.	Place CH2 probe on TP9, composite video output. Change triggering of CH1 to display one line of video and expand the time-base and vertical sensitivity of CH2 to observe the bottom of the horizontal sync. pulse. Note the presence of the clamp artifact due to keying; adjust TILT pot. as shown below Horizontal Sync. Pulse 
8	106A/P,D	Clamp Level Adjustment	With same display on CH2, rotate card edge mounted CLAMP REF pot. to place blanking at approx. 0Vdc.
9	106A/P,D	Video Output Level Cal.	Now reduce vertical sensitivity of CH2 and adjust card edge mounted LEVEL pot. to produce a peak-to-peak of 600mV between sync. tip and 100 IRE reference in multiburst. (It may be necessary to disconnect, in the case of 106A/P, the pu emphasis cap. which is a 32pF, dipped silver mica located directly above the LEVEL pot.) Recheck TILT adjustment, Step 1. This completes preliminary alignment of board 106/P,D.
10	105A/P/D	Video Amp. #1, High Freq. Compensation.	Make sure 75Ω terminating resistor is in. Inject 1V_{pp} multiburst (reduced amplitude) at TP1; trigger scope CH1 on TP1 and view one line of video. Display TP2 on CH2 and rotate HF COMP #1 trimmer for flattest multiburst (should be ±.25 db or better).
11	105A/P/D	Filter Check	Move CH2 probe to TP3 and check for ~1V_{pp} multiburst; burst flatness should be essentially the same.
12	For 105A 105A/D only.	Preset Gain Adjust, Video Amp #2	Jump a 75Ω ±5% resistor from TP5 to ground. Rotate GAIN pot. to produce 1V_{pp} signal at TP5. Verify 2V_{pp} at TP4.
13	For 105A/P	Preset Gain Adjust.	With TP5 open circuited, rotate GAIN pot to produce 0.75V_{pp} at TP5.
14	105A/P/D	Video Amp #2 High Freq. Compensation.	Observe TP5 under conditions of Step 13 or 14 as appropriate and rotate HF COMP #2 trimmer for flattest multiburst at TP5.

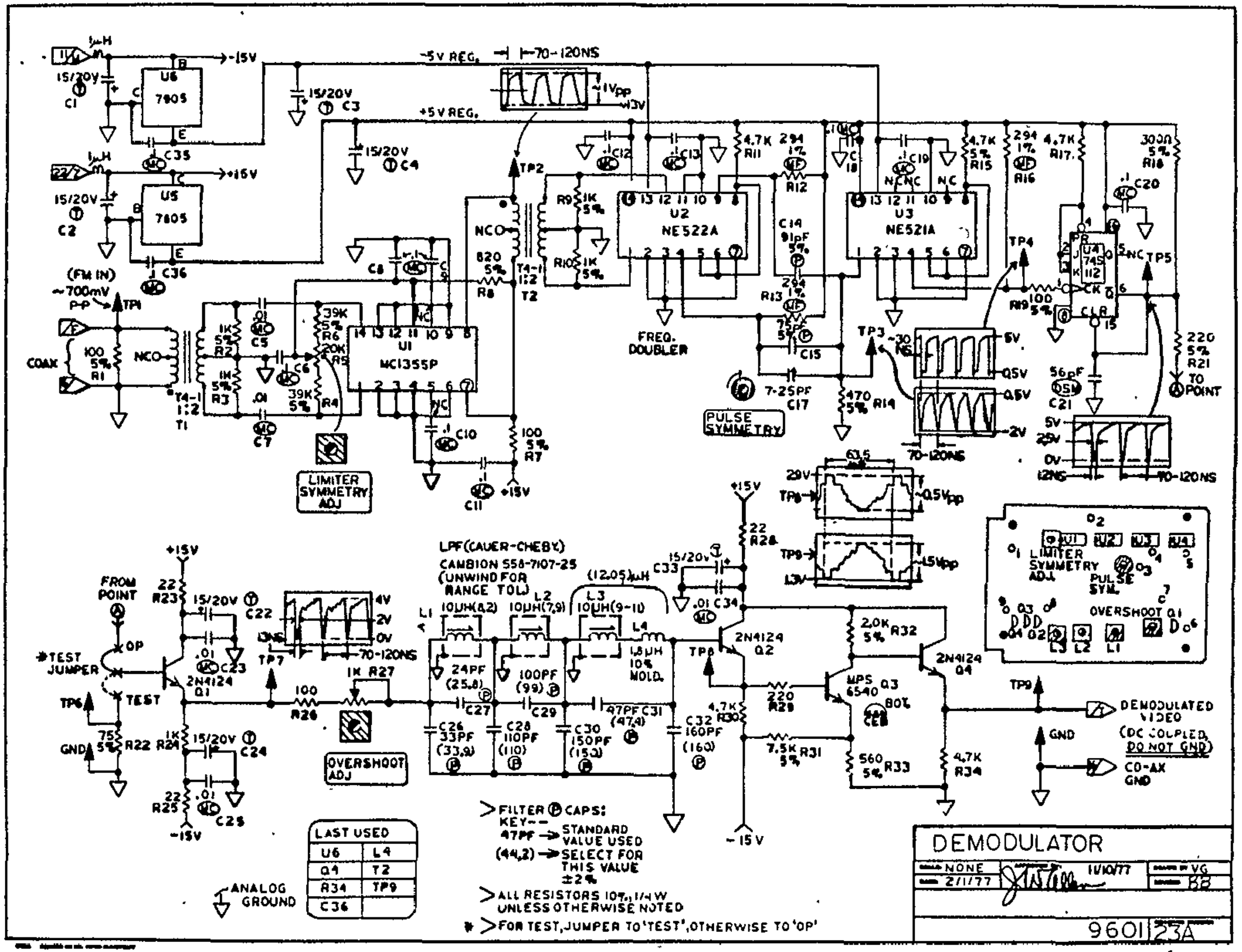
Step	Board	Adjustment	
15	For 105A/P Only	Video Output Bias Voltage Adjust.	With TP5 open circuited, rotate FM CENTER FREQ pot. to place sync. tip at +4VDC at TP5.
16	105A/P/D	Test Completion	Remove 75Ω input termination. This completes preliminary alignment of 105A/P/D boards.
17	21A	Test Set-Up	Move jumper to TEST position. Couple channel A output, pin v to a 50Ω 20 db pad and then to input of RF spectrum analyser using 50Ω coax cable.
18	21A	Harmonic Distortion Minimization	Inject (via 50Ω coax) a 6 MHZ 500 mV_{pp} sinewave at TP10 and trim generator output for 1.5V_{pp} at TP6. Rotate DIST ADJ pot. for minimum 2ND harmonic (12 MHZ) on spectrum analyser.
19	21A	High Freq. Compensation	Adjust HF FLAT trimmer cap for equal gains at 3 and 10 MHZ on analyser. This will interact with adjustment of step 18. Trim both for best results with uniform roll-off approx. 1 db down at 10 MHZ. Replace jumper to NORM position when finished. This completes preliminary alignment of 21A.
20	23A	Reg. Check	Plug in board and check ±5 and -5V regulator outputs for proper voltages, (±5V ±0.5V).
21	23A	Freq. Doubler Alignment	Inject a 6 MHZ 30 mV_{pp} sinewave into TP1 via 50Ω coax. Connect CH1 scope output to spectrum analyser input via 50Ω BNC coax cable. Observe pulse train at TP5 on CH1 and it's spectrum. Rotate LIMTER SYMMETRY pot. to null fundametnal @ 6 MHZ on analyser. Now rotate PULSE SYMMETRY trimmer capacitor for further improvement. The pot. has the dominant effect. Trim both alternately for best results.
22	23A	Demod. LPF Overshoot Adjustment	Move jumper to TEST position. Inject a "$\sin^2$ Pulse and Bar" test waveform from Tek R147 generator via 75Ω coax. at TP6. Place CH1 probe on TP8 and display the "pulse" portion of the test signal. Rotate OVERSHOOT ADJ pot for correct waveform as shown below 

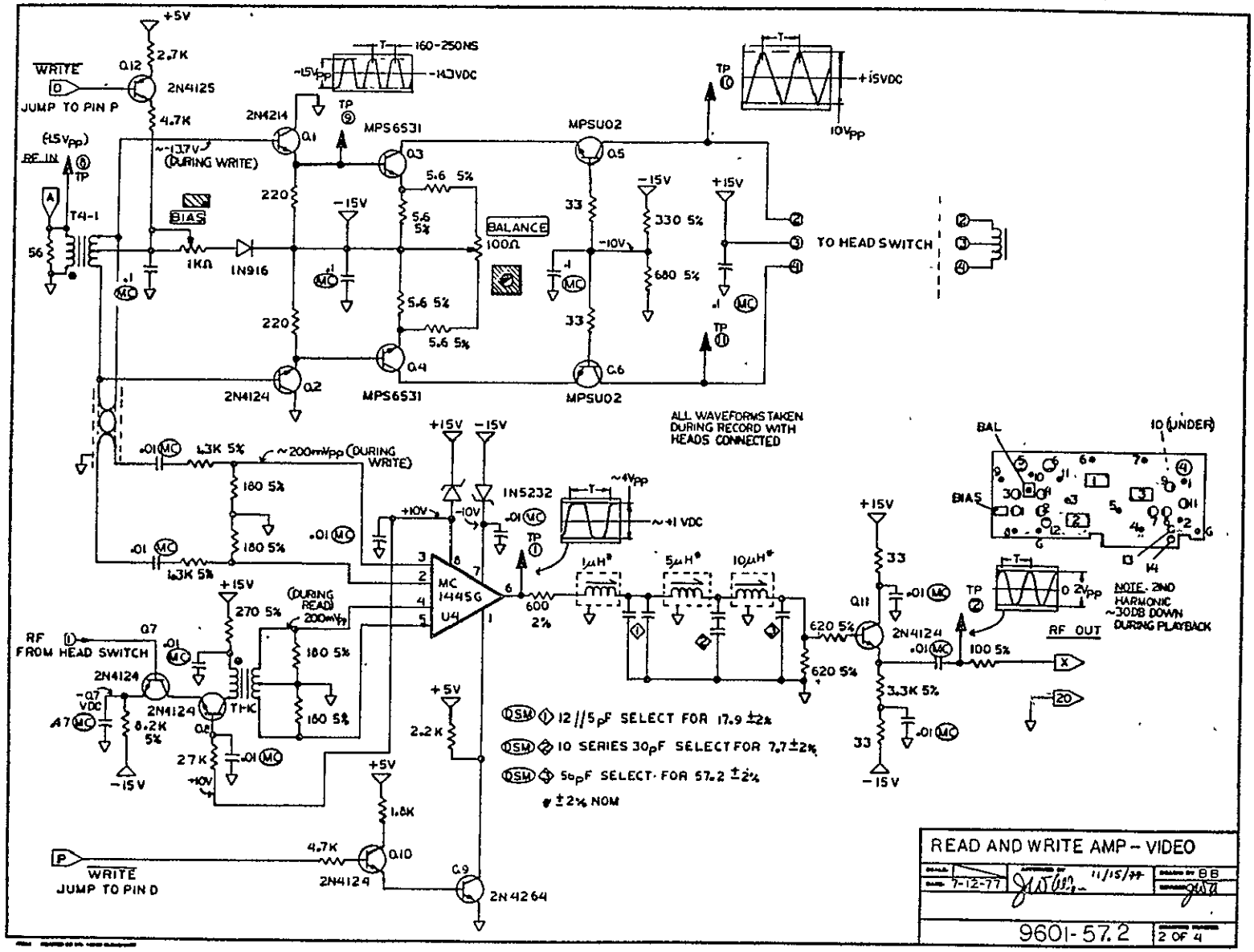
Step	Board	Adjustment	
23	23A	LPF Freq. Response Calibration	Switch test signal to "Multi-burst". Adjust coils L1, L2, L3 for flattest multi-burst with slow rolloff toward highest frequencies. Now connect RF sweep generator in place of Tek 147 test signal and check for nulls at ∿6 and ∿7 MHZ with stop band rejection of 50 db or better from 6-20 MHZ. Return jumper to OP position when finished.

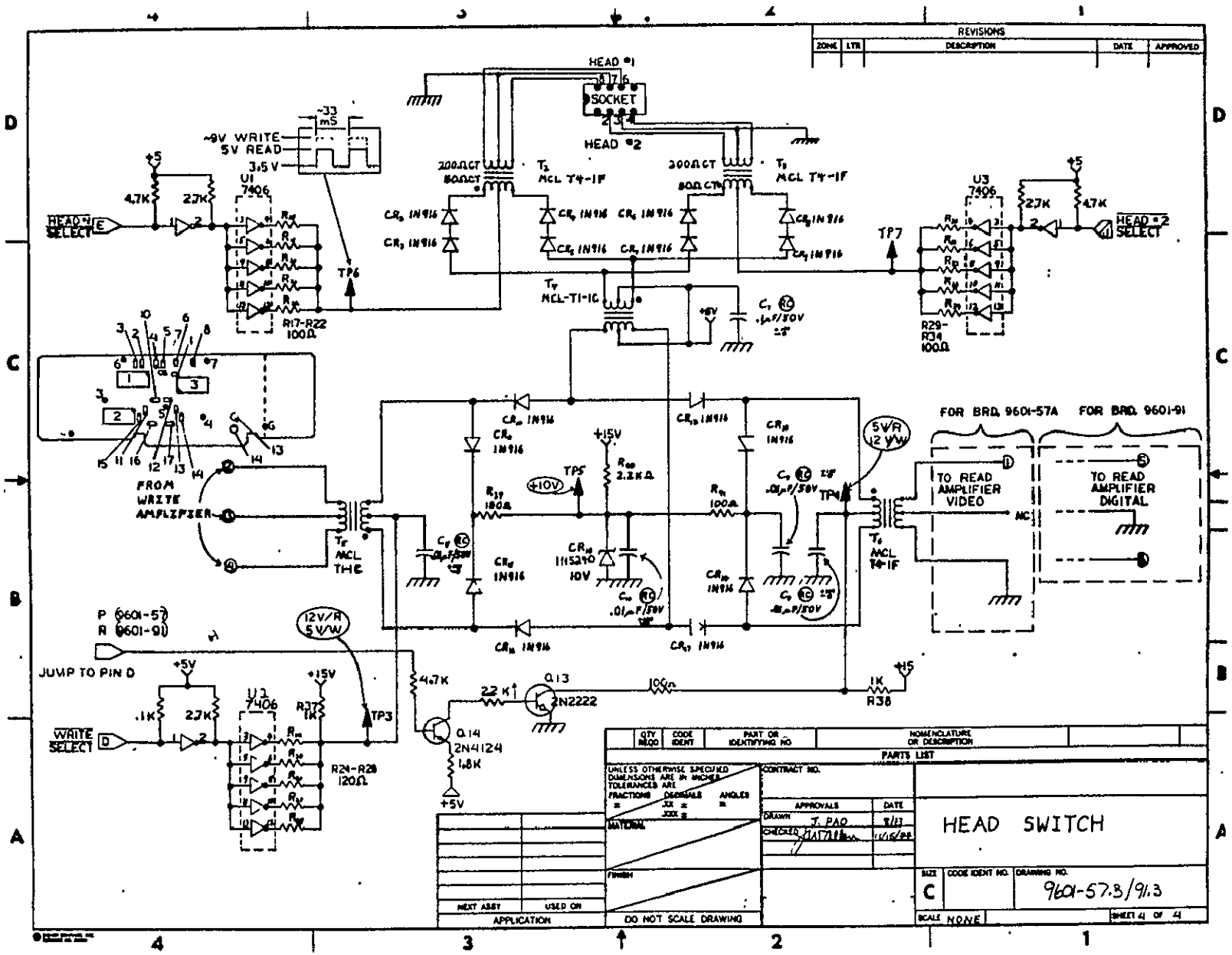
This completes preliminary alignment of the MOD and DEMOD cards.

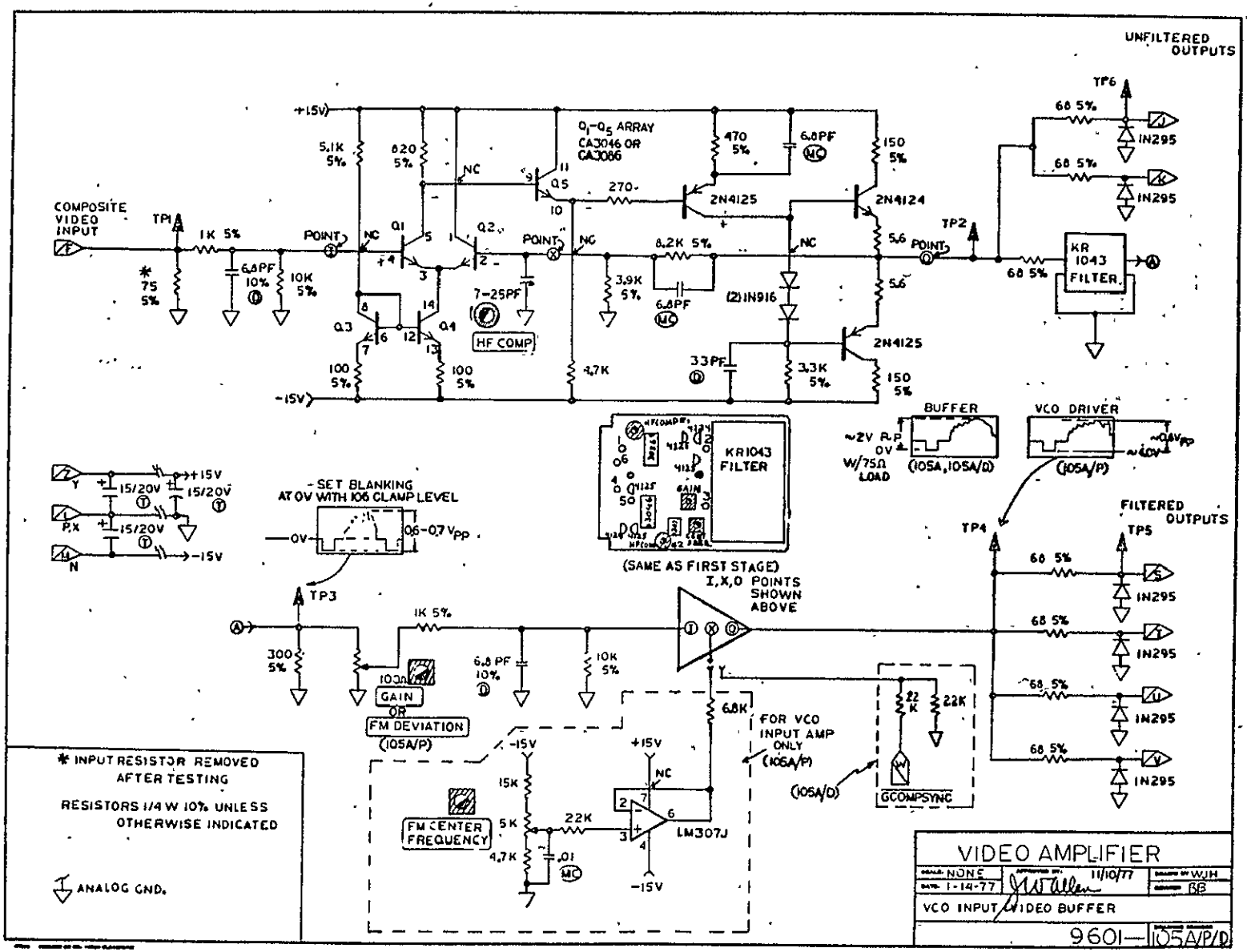


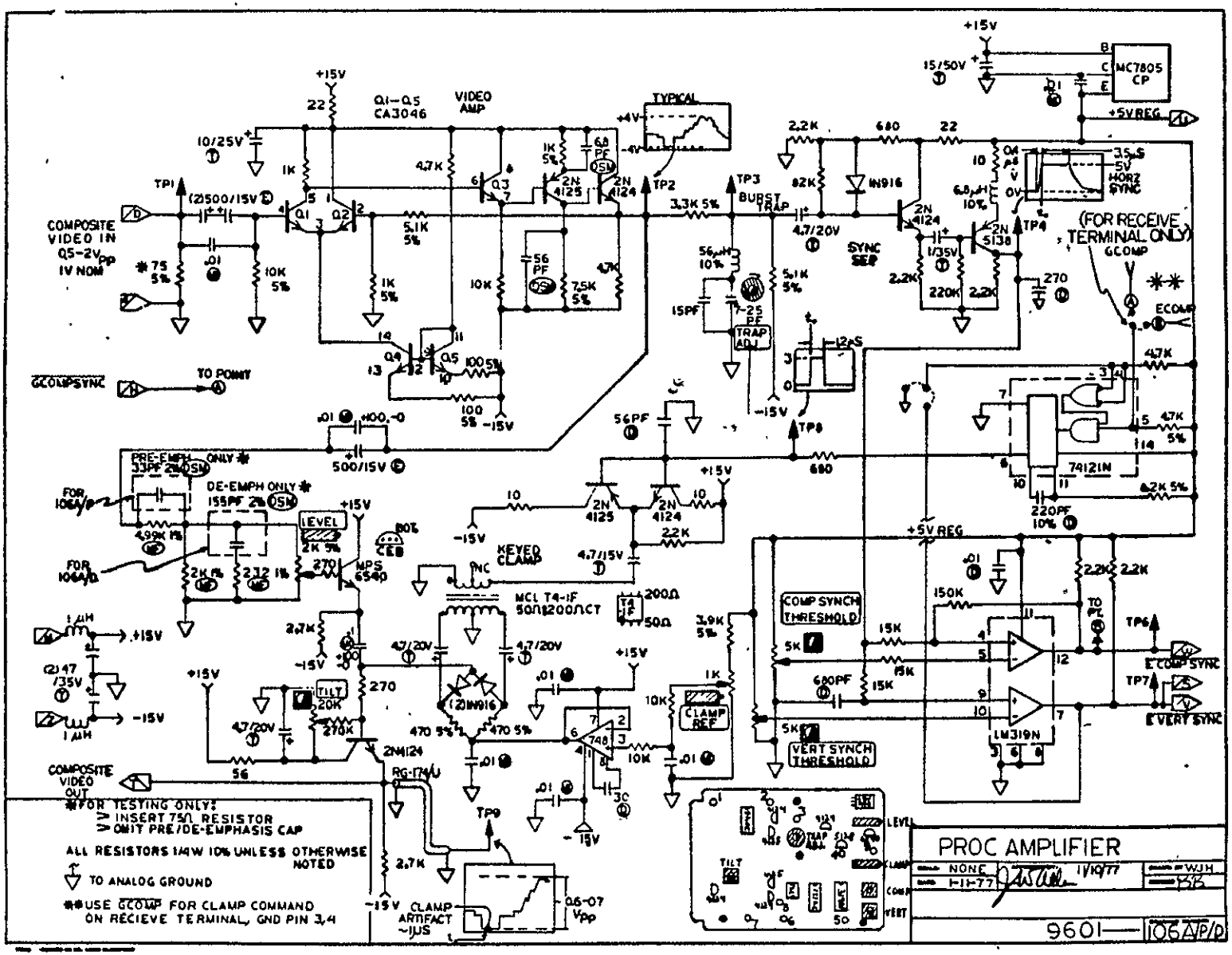
NOTE: 1. Q1-Q5 ARE CA3046 ARRAY (OR CA3086)
2. ⊕ -SELECT FOR VALUES WITHIN 2% ON BRIDGE

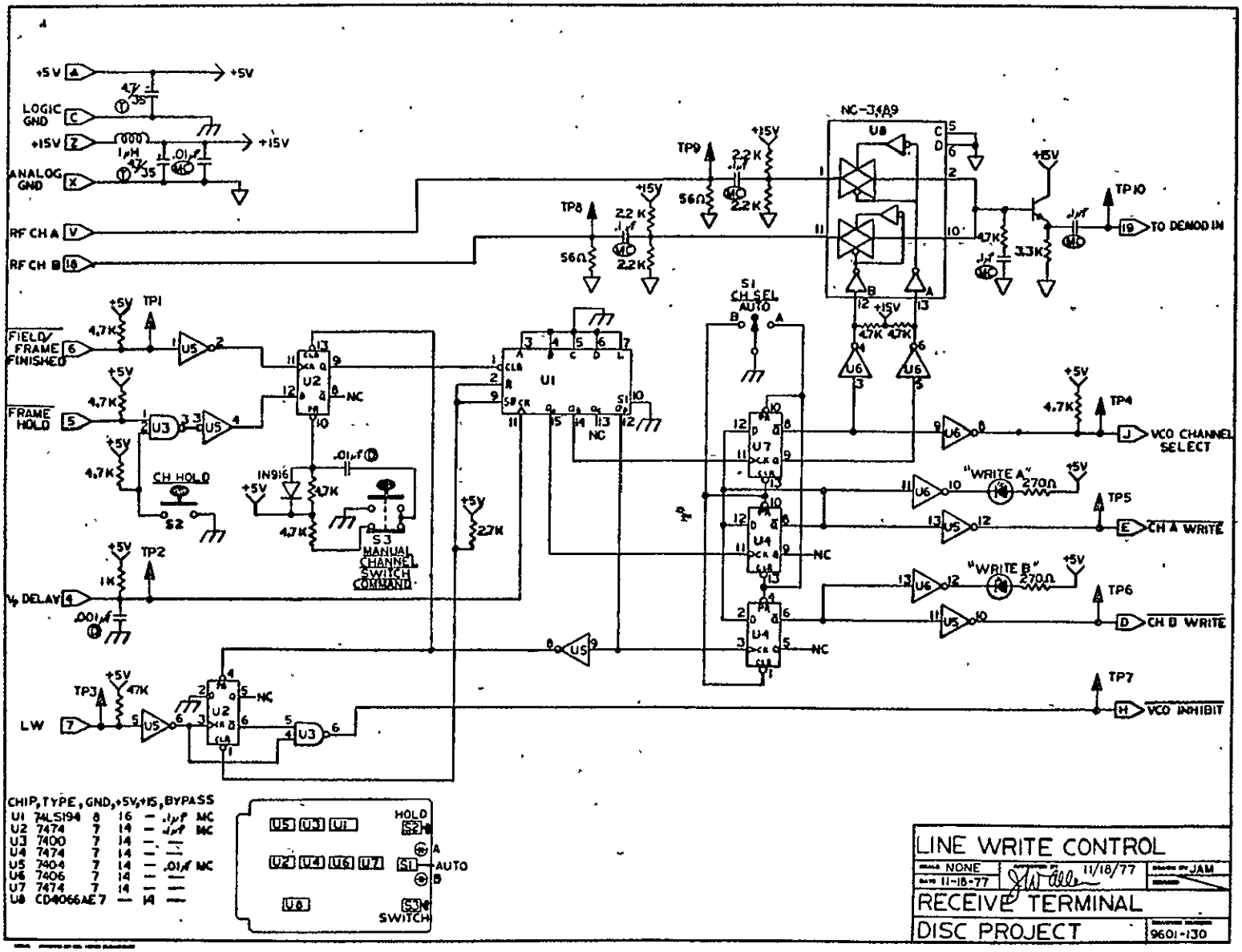

DEMODULATOR
NONE
2/1/77
11/10/77
VG
BB
9601123A
-5V REG.
+5V REG.
70-120NS
U6 7805
U5 7805
U1 MC1355P
U2 NE522A
U3 NE521A
U4 74S112
FREQ. DOUBLER
PULSE SYMMETRY
LIMITER SYMMETRY ADJ
OVERSHOOT ADJ
(FM IN) ~700mV P-P
COAX
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TO POINT
FROM POINT
*TEST JUMPER
OP
TEST
LPF (CAUER-CHEBY.)
CAMBION 558-7107-25 (UNWIND FOR RANGE TOL)
2N4124 Q1
2N4124 Q2
MPS 6540 Q3
2N4124 Q4
DEMODULATED VIDEO (DC COUPLED, DO NOT GND)
CO-AX GND
GND
+15V
-15V
LAST USED
U6 L4
Q4 T2
R34 TP9
C36
ANALOG GROUND
FILTER (F) CAPS: KEY--
47PF → STANDARD VALUE USED
(44.2) → SELECT FOR THIS VALUE ±2%
ALL RESISTORS 10%, 1/4 W UNLESS OTHERWISE NOTED
* FOR TEST, JUMPER TO 'TEST', OTHERWISE TO 'OP'
LIMITER SYMMETRY ADJ.
PULSE SYM.
OVERSHOOT




REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
HEAD #1
SOCKET
HEAD #2
~33 mS
~9V WRITE
5V READ
3.5 V
+5
4.7K
2.7K
U1 7406
HEAD #1 SELECT
R17-R22 100Ω
TP6
200Ω CT
80Ω CT
T1 MCL T4-1F
T2 MCL T4-1F
CR1 IN916
CR2 IN916
CR3 IN916
CR4 IN916
CR5 IN916
CR6 IN916
CR7 IN916
CR8 IN916
T7 MCL-T1-1C
+8V
C1 .1μF/50V
TP7
U3 7406
R29-R34 100Ω
HEAD #2 SELECT
FOR BRD. 9601-57A
FOR BRD. 9601-91
TO READ AMPLIFIER VIDEO
TO READ AMPLIFIER DIGITAL
FROM WRITE AMPLIFIER
T5 MCL T4-1C
CR9 IN916
CR10 IN916
CR11 IN916
CR12 IN916
CR13 IN916
CR14 IN916
CR15 IN916
CR16 1N5240 10V
+15V
+10V
TP5
TP4
R39 180Ω
R40 2.2KΩ
R41 100Ω
C2 .01μF/50V
C3 .01μF/50V
C4 .01μF/50V
C5 .01μF/50V
C6 .01μF/50V
5V/R 12 V/W
T6 MCL T4-1F
P 9601-57
R 9601-91
12V/R 5V/W
JUMP TO PIN D
WRITE SELECT
U2 7406
.1K
2.7K
R37 1K
TP3
R24-R28 120Ω
4.7K
22 K
Q13 2N2222
Q14 2N4124
1.8K
1K R38
+15
PARTS LIST
QTY REQD | CODE IDENT | PART OR IDENTIFYING NO | NOMENCLATURE OR DESCRIPTION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
MATERIAL
FINISH
NEXT ASSY | USED ON
APPLICATION
DO NOT SCALE DRAWING
CONTRACT NO.
APPROVALS | DATE
DRAWN J. PAO 9/13
CHECKED 10/15/84
HEAD SWITCH
SIZE C | CODE IDENT NO. | DRAWING NO. 9601-57.8/91.3
SCALE NONE
SHEET 41 OF 41


UNFILTERED OUTPUTS
TP6
68 5%
IN295
68 5%
IN295
+15V
5.1K 5%
820 5%
Q1-Q5 ARRAY CA3046 OR CA3086
470 5%
6.8PF MC
150 5%
NC
Q5
270
2N4125
2N4124
COMPOSITE VIDEO INPUT
TP1
1K 5%
POINT
NC
Q1
Q2
POINT
NC
8.2K 5%
NC
5.6
POINT
TP2
* 75 5%
6.8PF 10% D
10K 5%
7-25PF
HF COMP
3.9K 5%
6.8PF MC
(2) IN916
5.6
68 5%
KR 1043 FILTER
Q3
Q4
2N4125
100 5%
100 5%
4.7K
33PF D
3.3K 5%
150 5%
-15V
BUFFER
~2V P-P 0V W/75Ω LOAD
(105A, 105A/D)
VCO DRIVER
~0.4V P-P ~0V
(105A/P)
KR1043 FILTER
(SAME AS FIRST STAGE)
I, X, O POINTS SHOWN ABOVE
Y
P.S
N
+15V
15/20V T
15/20V T
15/20V T
-15V
SET BLANKING AT 0V WITH 106 CLAMP LEVEL
0V
.06-0.7 V P-P
TP3
TP4
TP5
FILTERED OUTPUTS
68 5%
IN295
68 5%
IN295
68 5%
IN295
68 5%
IN295
A
1K 5%
300 5%
10K GAIN OR FM DEVIATION (105A/P)
6.8 PF 10% D
10K 5%
6.8K
FOR VCO INPUT AMP ONLY (105A/P)
22K
22K
(105A/D)
GCOMPSYNC
-15V
+15V
15K
5K
FM CENTER FREQUENCY
22K
NC
LM307J
4.7K
.01 MC
-15V
* INPUT RESISTOR REMOVED AFTER TESTING
RESISTORS 1/4 W 10% UNLESS OTHERWISE INDICATED
ANALOG GND.
VIDEO AMPLIFIER
SCALE NONE
DATE 1-14-77
APPROVED BY 11/10/77
DRAWN BY WJH
CHECKED BB
VCO INPUT VIDEO BUFFER
9601—105A/P/D


PROC AMPLIFIER
9601—106AP/D
COMPOSITE VIDEO IN
COMPOSITE VIDEO OUT
GCOMPSYNC
TO POINT
FOR RECEIVE TERMINAL ONLY
GCOMP
ECOMP
E COMP SYNC
E VERT SYNC
COMP SYNCH THRESHOLD
VERT SYNCH THRESHOLD
KEYED CLAMP
CLAMP REF
TRAP ADJ
SYNC SEP
BURST TRAP
VIDEO AMP
Q1-Q5 CA3046
MC7805 CP
+5V REG
74121N
LM319N
MCL T4-1F
CLAMP ARTIFACT ~1µS
0.6-0.7 Vpp
*FOR TESTING ONLY:
=> INSERT 75Ω RESISTOR
=> OMIT PRE/DE-EMPHASIS CAP
ALL RESISTORS 1/4W 10% UNLESS OTHERWISE NOTED
TO ANALOG GROUND
**USE GCOMP FOR CLAMP COMMAND ON RECIEVE TERMINAL, GND PIN 3,4



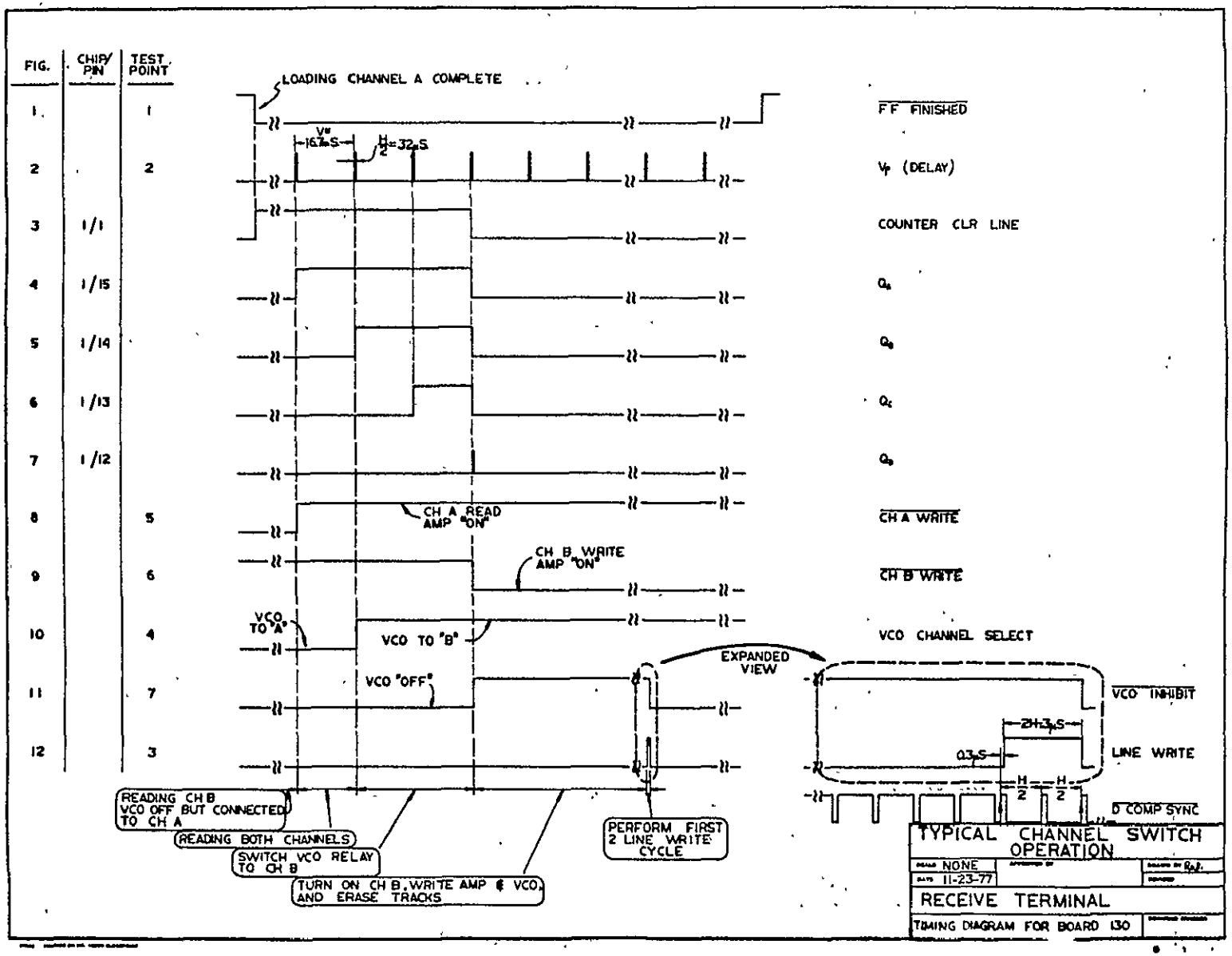


FIG.
CHIP/PIN
TEST POINT
1
2
3
1/1
4
1/15
5
1/14
6
1/13
7
1/12
8
5
9
6
10
4
11
7
12
3
LOADING CHANNEL A COMPLETE
V" 16.7μS
H/2 = 32μS
FF FINISHED
Vp (DELAY)
COUNTER CLR LINE
Qa
Qb
Qc
Qd
CH A READ AMP "ON"
CH A WRITE
CH B WRITE AMP "ON"
CH B WRITE
VCO TO "A"
VCO TO "B"
VCO CHANNEL SELECT
VCO "OFF"
EXPANDED VIEW
VCO INHIBIT
2H-3μS
0.3μS
LINE WRITE
H/2
H/2
D COMP SYNC
READING CH B VCO OFF BUT CONNECTED TO CH A
READING BOTH CHANNELS
SWITCH VCO RELAY TO CH B
TURN ON CH B WRITE AMP & VCO, AND ERASE TRACKS
PERFORM FIRST 2 LINE WRITE CYCLE
TYPICAL CHANNEL SWITCH OPERATION
SCALE NONE
DATE 11-23-77
RECEIVE TERMINAL
TIMING DIAGRAM FOR BOARD 130

Appendix 2.9

DATA GROUP ADJUSTMENT PROCEDURE AND SCHEMATIC DIAGRAMS

DATA GROUP ALIGNMENT PROCEDURE

BOARDS: 91A Digital R/W
92A Encoder/Decoder
93A Clock Recovery PLL
112A DSYNC Proc. I
114A DSYNC Proc. II

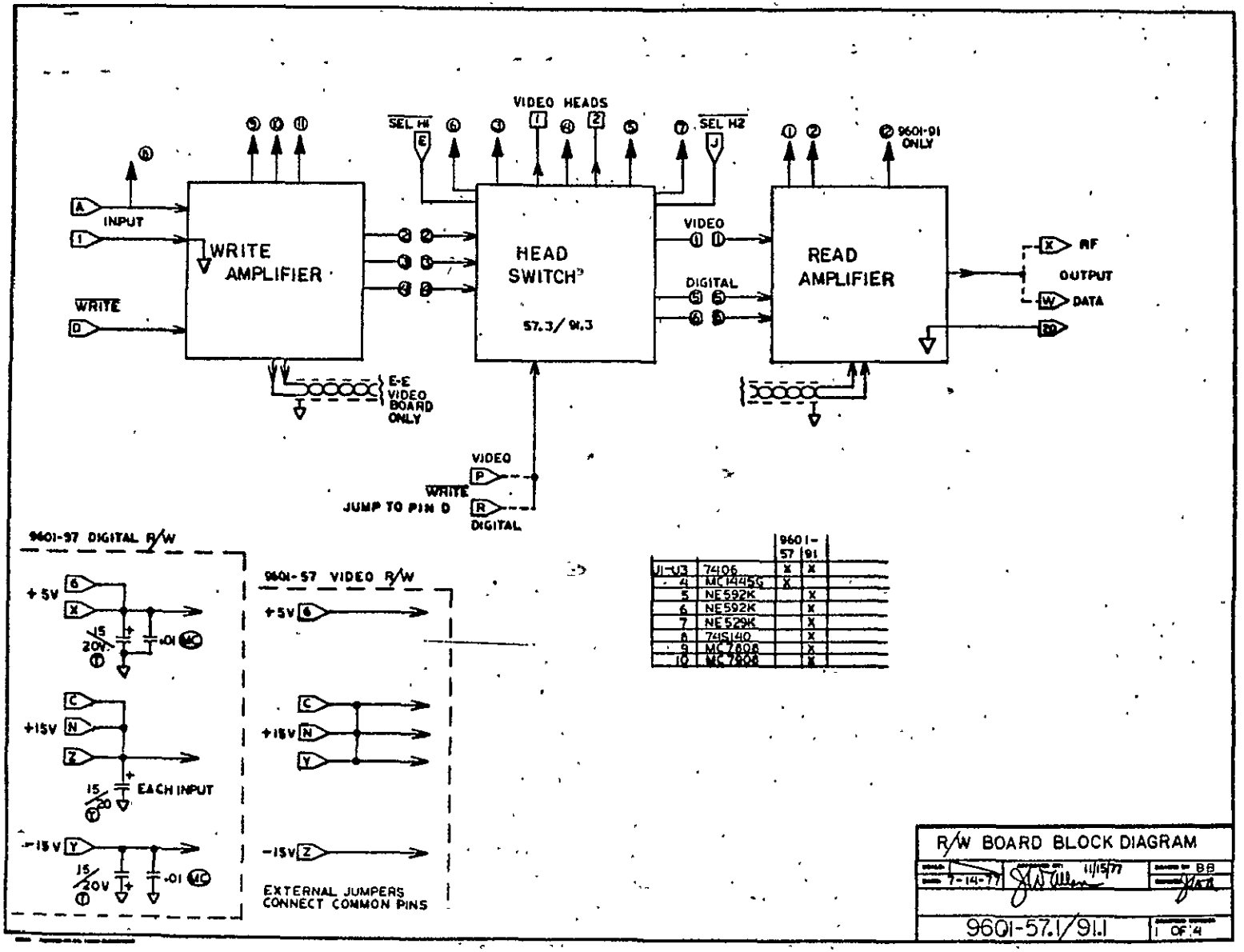
Step	Board	Adjustment	
1	92A	Test Setup	Insert only 92A in it's slot in the card cage. Place S1 in LOC mode. (This connects the encoder directly to the decoder). Note that red LED should be on. Determine that MCOMPSYNC is available at TP1 and that X2CK (8.1818 MHz) is present at TP2.
2	92A	Encoder Check	Trigger CH1 of scope (Hi-speed such as HP 1741A or Tek 454, 465, or 475) on the rising edge of one of the horizontal sync pulses from TP1. Display one additional sync pulse on screen. Using CH2, attach probe to TP8 and, employing expanded sweep, examine the area around the second sync pulse. Note that square wave is ∿ 2 MHz when MCOMPSYNC is low and ∿ 4 MHz during pulse.
3	92A	Decoder Check	Leave CH1 connected and triggered as in step (2) . Attack CH2 to TP11 and observe the same waveform as MCOMPSYNC except delayed (see timing diagram for exact relationships). Check TP5 for the inverted version.
4	92A	Recovery Error Check	Using CH2 probe, check to see that TP7, $\overline{\text{RECOVERY ERROR}}$ is in high state, as it should be.
5	92A	DCLK Syncronizer Check	Now move probe (CH1) to TP11, triggering off decoded data signal in same fashion as before. Expand the main sweep to display the falling edge of horizontal sync pulse about in the cetner of screen. Place CH2 probe on TP12 and observe a ∿2MHz (2.04545 MHz) square wave which is stable with respect to sync pulse (no polarity-flipping). See the timing diagrams for exact time relationships. This completes the checkout of 92A.
6	91A	Test Set-up	Now plug in the digital R/W board, 91A, and attach the head cable; leave the data head up, i.e. not flying. Verify that the board is receiving the encoded data stream by observing TP8. Use CH1 and trigger on rising edge with a sweep speed of 100 nsec/div. Note waveform and compare to Figure on schematic 9601-91.2, TP8. Overshoot should not exceed that shown or grounding problems exist.

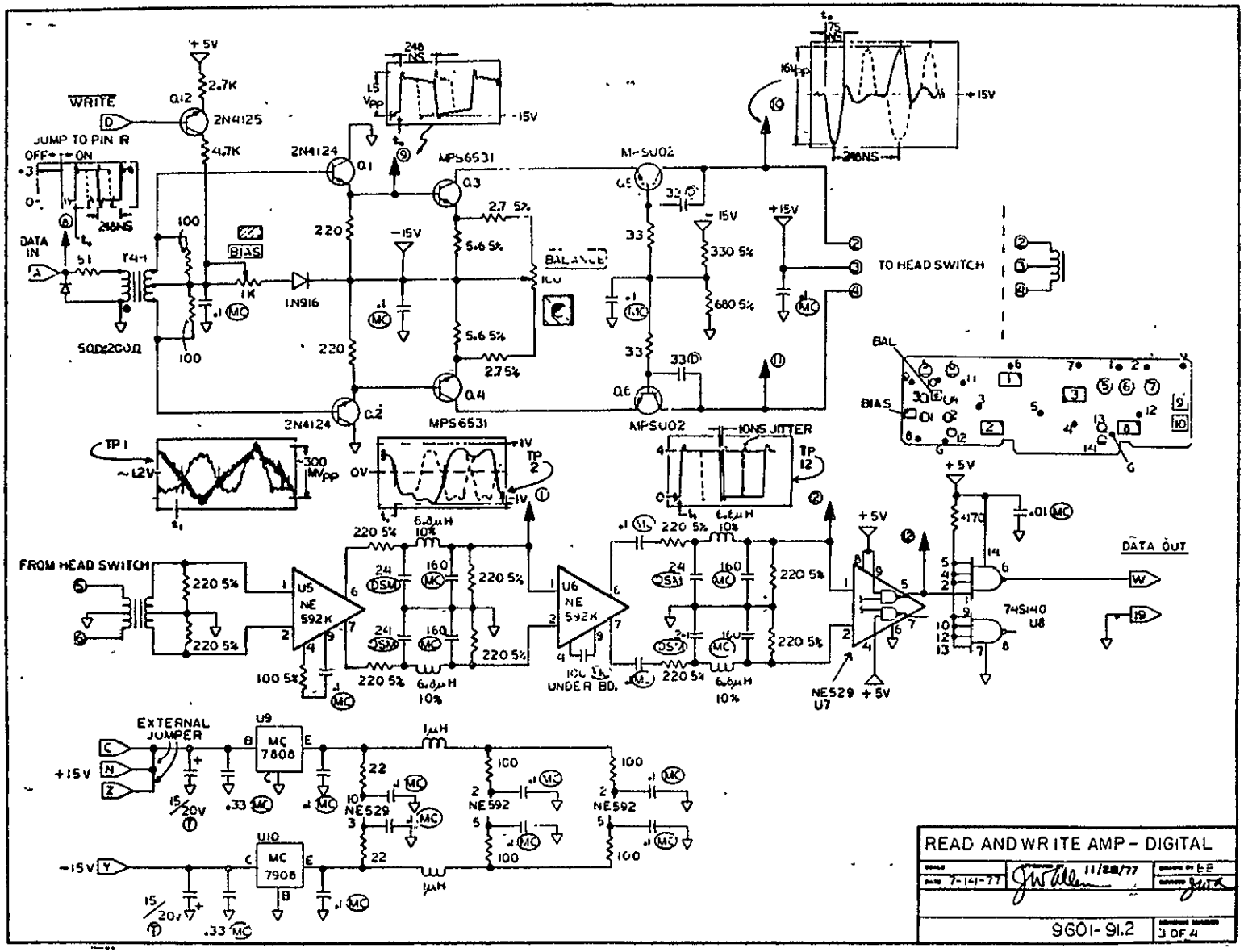
Step	Board	Adjustment	
7 —	91A	Write Amp Alignment; Bias Adjustment	Leaving CH1 probe on TP8, verify waveform on print, TP9 using CH2 probe. The signal should be ∿1.5 V_{pp} with slight tilt due to transformer coupling losses at low frequencies. Now set CH2 input sensitivity to 2V/div and place probe on TP10. Adjust BIAS pot for 16 V_{pp} dual polarity pulses as shown on the schematic. (Note: 91A must be given a WRITE command during these tests).
8	91A	Balance Pot Preset	Leave CH2 probe setup and change triggering mode to CH2. Now set CH1 to same vertical sensitivity, switch to differential display mode and rotate BALANCE pot for minimum display amplitude. (This adjustment is preliminary since it is a differential voltage measurement and is not an exact reflection of the differential current balance at the head).
9	91A	Read Amp Check	Remove probes and lower the data head. Using R/W controller pushbuttons, write data onto disc and release button. Place CH1 probe at TP1 and check for relatively noisy 300 mV_{pp} readback signal as shown on schematic. Most intense portion of waveform should be triangular in appearance. Move to TP2 and again verify waveform. Finally check output signal at TP12. Trigger on rising edge and set up scope display to mach figure on schematic. Note jitter on falling edge of data signal; ten nanoseconds is acceptable. If jitter is much greater don't be alarmed yet, it could be due to write-amp imbalance, which will be trimmed next.
10	93A	Edge Detector Check, Write Amp Balance Adjustment	Plug in the DATA CLOCK RECOVERY PLL, board 93A. Check for a clean data signal at TP1, using same probe as was used in step (9) . The waveform should be virtually identical. Now move probe to TP3, and trigger on falling edge. Observe train of negative-going pulses about 10 nsec wide as shown in figure on the schematic. Carefully note the jitter on the middle pulse. While watching this, write data onto disc while slowly varying the BALANCE pot on 91A. A pot position will be found that procedures the minimum jitter in this pulse. The jitter should be approximately 10 ns or less.
11	93A	Cell Detector Adjustment	Place probe just used on TP4 and rotate 100 NS ADJ pot. to produce a clean square wave at ∿2MHz. The rising edge jitter should be ∿10 nsec. (Waveform will have a small irregularity due to track-switching.
12	93A	Clock Phase Calibration	Set up scope for 2 channel display of TTL waveforms. Trigger CH1 on falling edge of TP10 and display TP8 on CH2. If PLL is locked, CH2 display will appear stationary w.r.t. CH1, but will not necessarily be in-phase. Rotate BIAS pot on card edge to produce ∿60 nsec lag in signal on TP8 as shown on schematic. This completes the adjustments of 93A.

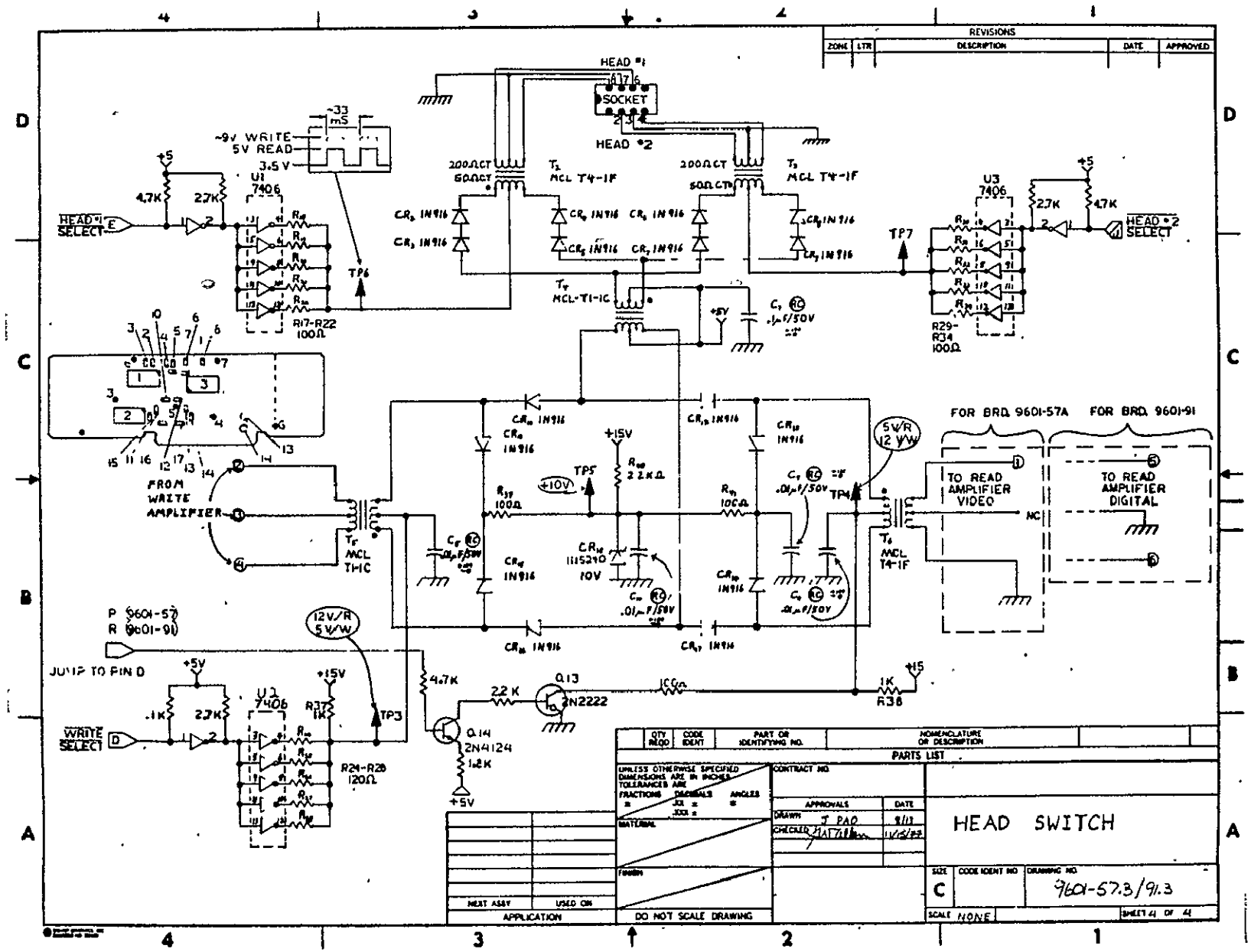
Step	Board	Adjustment	
13	92A	Readback DATA Check	Switch S1 to OPR. Trigger scope CH1 on TP1 and use sync separator to display sweep triggered on vertical interval. Check TP7 with CH2 and verify that negative-going pulses only appear during region of vertical interval (while data tracks are being switched). Now move probe to TP11 and carefully compare both COMP SYNC signals. One should find discrepancies only during the vertical interval.
14	112A	Preliminary Check	Plug in 112A and place S1 (Autowrite) in OFF position, S2 in TEST positin. ERROR LED should be OFF and ERRORL LED may be in either state. Check TP's 4, 15 for HI state, TP3 for MCOMPSYNC, TP12 for 2.04545 MHz clock signal.
15	112A	Vertsync Processor Check	Trigger scope CH1 on TP7 and note pulse as shown on schematic once each vertical interval; display two pulses on screen. Using CH2, check TP10 for GV_p each vertical interval and TP11 for GPl_p every other vertical interval. If these are present, processor is OK.
16	112A	Error Processing	Flip S2 to NORM position; this supplies clock, data, and error signals from the disc to 112A's processing circuits. If data stream is error-file, ERROR LED should be OFF. (Flashing behavior indicates problems in read-back signal which may be associated with 1) physical disc surface problems, 2) head flying improperly, or 3) sub-optimal PLL clock recovering and/or phase alignment. Carefully recheck system to determine the cause(s)). Assuming everything is OK proceed to touch the back of the socket to which the data head is connected. The ERROR LED should flash momentarily, indicating that errors are present. In order to make the ERRORL LED go out, write data (manually) onto disc. Both LED's should now be out. If AUTOWRITE is being used (in Receive terminl only), flip S1 to AUTO position. Now, touching socket with finger will cause BOTH LED's to flash on and subsequently go out, indicating that the data has automatically been re-written. If this is not the case, check one shots on 112A for proper time constants, as shown on schematic.
17	114A	Set-up	Plug in final board DSYNC PROC2, 114A. (Note: this board may be checked with either XTAL-referenced or DISC-referenced signals as selected on 112A). Check TP's 1, 2, 3 for GH, GMCK, and GCOMPSYNC respectively (see timing diagram). (These are the only input signals to the board).
18	114A	Burstgate Lockout Pulse Width Adjustment	Place probe on TP6 and rotate 9H ADJUST pot to provide a negative-going pulse of ~572 μsec duration, present every vertical interval. Using delayed sweep, check falling edge to verify that it is stable in time (i.e., not jumping ±H/2).

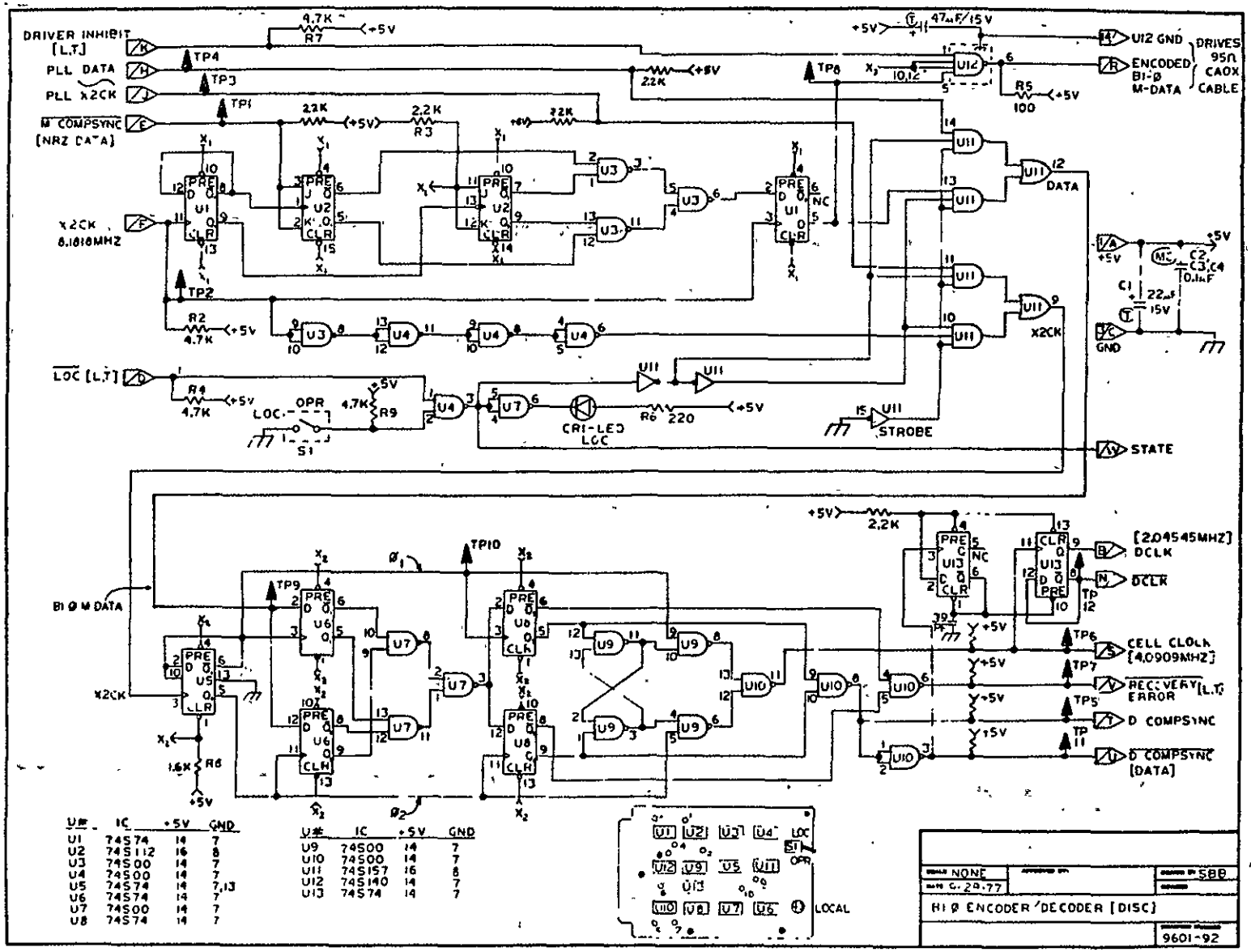
Step	Board	Adjustment	
19	114A	Delta Counter Check	Place CH1 probe on TP10 and trigger on rising edge (the HI state enables the counter). Place proper preset on DIPSWITCH, U15 as shown on schematic 9601-114. TP10 should fall low at end of Δ count; note that pulse should be of constant duration and have a stable falling edge. Erratic behavior indicates fault in Δ count subsystem or noise entering on either TP's 1 or 2.
20	114A	HORZ Counter Check	The falling edge of signal on TP4 (Δ count) enables the HORZ counter. Subsequent combinational logic (U7-U11) decodes the three horizontal sync signals, which are reclocked in register U12 to provide stable, glitch-free signals synchronous with GMCK. Check the timing relationships for GHORDRIVE (TP7), GHORBLANK (TP8) and GBURSTGATE (TP9) on timing diagram. GBURSTGATE should appear to flicker, indicating its absence for 572μsec in the vertical interval.
21	114A	Δ Counter Final Verification	Trigger CH1 with TP11, $\overline{\text{GCOMPSYNC}}$ and display two horizontal sync pulses. Using expanded sweep, place the second pulse in view so that the leading and trailing edges fill the screen. Now display TP7, GHORDRIVE on CH2. Preset dipswitch code to 10001110 = 113. The rising edge of TP7 should precede the rising edge of TP11 by 1.4667μsec. Once observed, return preset to proper code.

This completes the DATA GROUP alignment.


VIDEO HEADS
SEL H1
SEL H2
9601-91 ONLY
INPUT
WRITE AMPLIFIER
WRITE
HEAD SWITCH
57.3/91.3
VIDEO
DIGITAL
READ AMPLIFIER
RF OUTPUT
DATA
E-E VIDEO BOARD ONLY
VIDEO
WRITE
JUMP TO PIN D
DIGITAL
9601-57 DIGITAL R/W
+5V
+15V
EACH INPUT
-15V
9601-57 VIDEO R/W
EXTERNAL JUMPERS CONNECT COMMON PINS
9601-57 9601-91
U1-U3 7406 X X
4 MC1445G X
5 NE592K X
6 NE592K X
7 NE529K X
8 74S140 X
9 MC7808 X
10 MC7908 X
R/W BOARD BLOCK DIAGRAM
7-14-77
11/15/77
BB
9601-57.1/91.1
1 OF 4

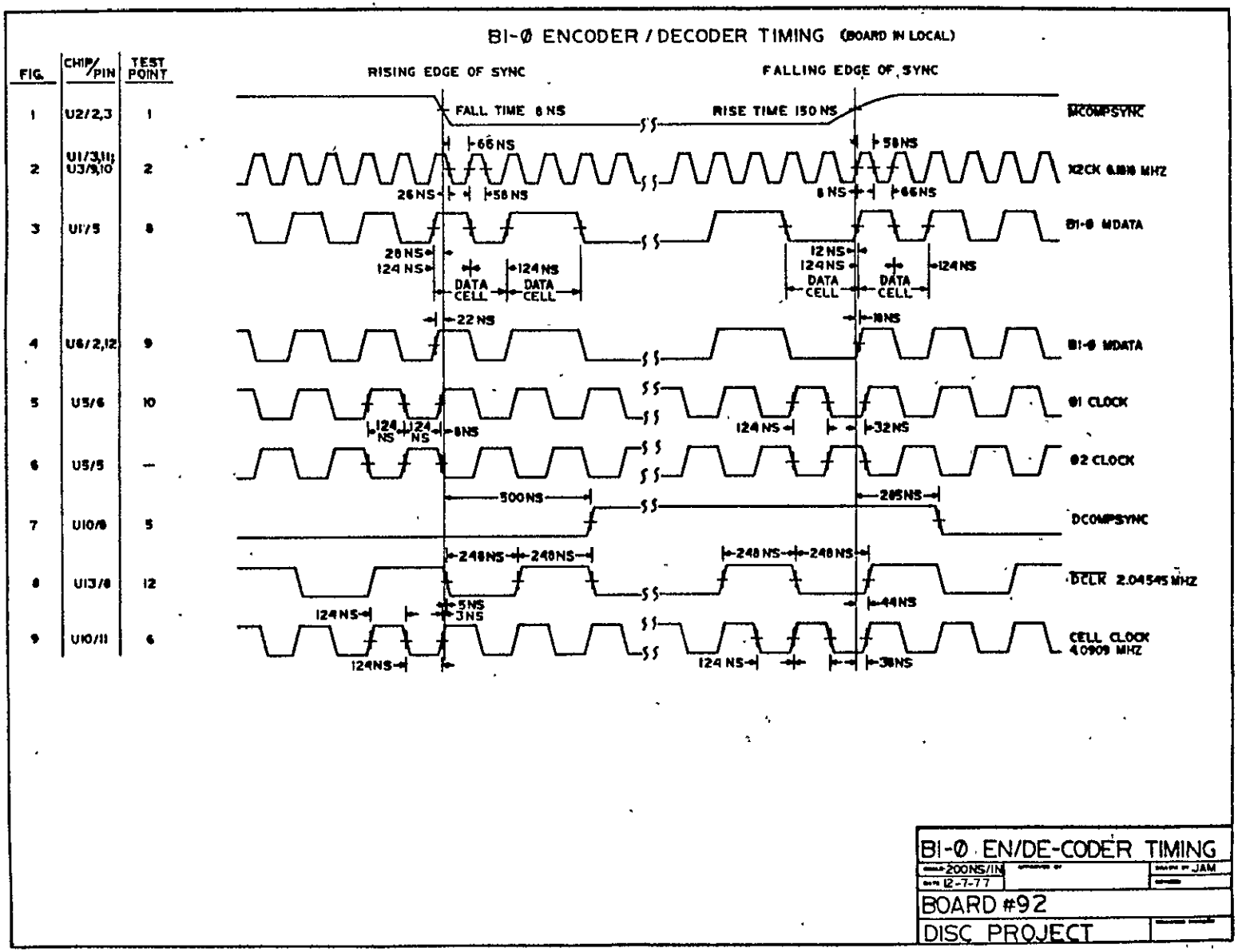


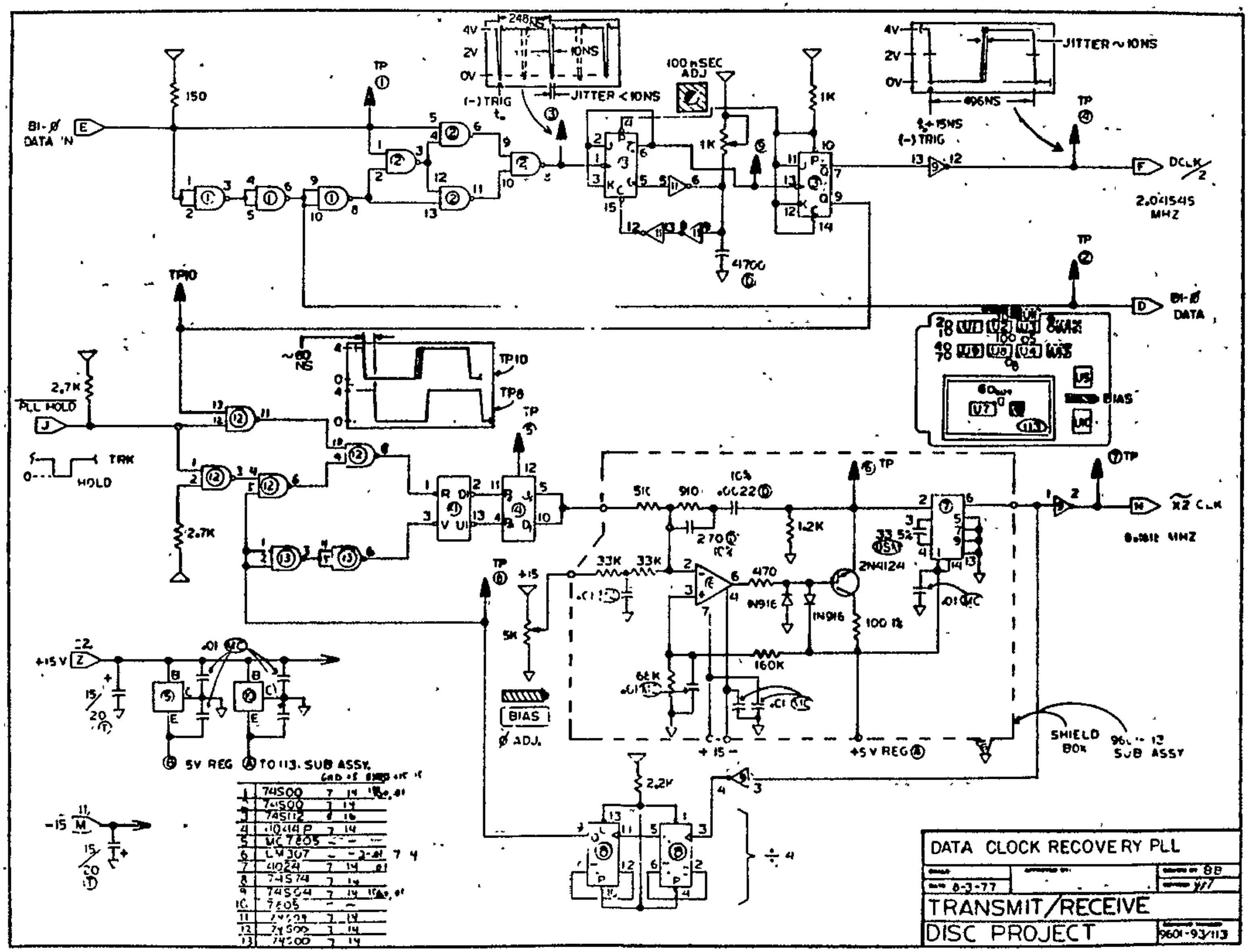

REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
HEAD #1
HEAD #2
SOCKET
~33 mS
~9V WRITE
5V READ
3.5 V
U1 7406
U2 7406
U3 7406
4.7K
2.7K
.1K
1K
HEAD #1 SELECT
HEAD #2 SELECT
WRITE SELECT
R17-R22 100Ω
R24-R28 120Ω
R29-R34 100Ω
200Ω CT
50Ω CT
T1 MCL T4-1F
T2 MCL T4-1F
T3 MCL T4-1F
T4 MCL T1-1C
T5 MCL T1-1C
T6 MCL T4-1F
CR1 IN916
CR2 IN916
CR3 IN916
CR4 IN916
CR5 IN916
CR6 IN916
CR7 IN916
CR8 IN916
CR9 IN916
CR10 IN916
CR11 IN916
CR12 IN916
CR13 IN5240 10V
+5V
+15V
+10V
TP3
TP4
TP5
TP6
TP7
FROM WRITE AMPLIFIER
JUMP TO PIN D
P 9601-57
R 9601-91
12V/R 5V/W
5V/R 12 V/W
FOR BRD 9601-57A
FOR BRD 9601-91
TO READ AMPLIFIER VIDEO
TO READ AMPLIFIER DIGITAL
NC
Q13 2N2222
Q14 2N4124
22 K
1.2K
R38
R37
R35 100Ω
R39 100Ω
R40 2.2KΩ
.01μF/50V
.1μF/50V
PARTS LIST
QTY REQD | CODE IDENT | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
CONTRACT NO.
APPROVALS DATE
DRAWN J PAO 9/13
CHECKED MATT 11/5/82
MATERIAL
FINISH
NEXT ASSY USED ON
APPLICATION
DO NOT SCALE DRAWING
HEAD SWITCH
SIZE C
CODE IDENT NO
DRAWING NO. 9601-57.3/91.3
SCALE NONE
SHEET 41 OF 41

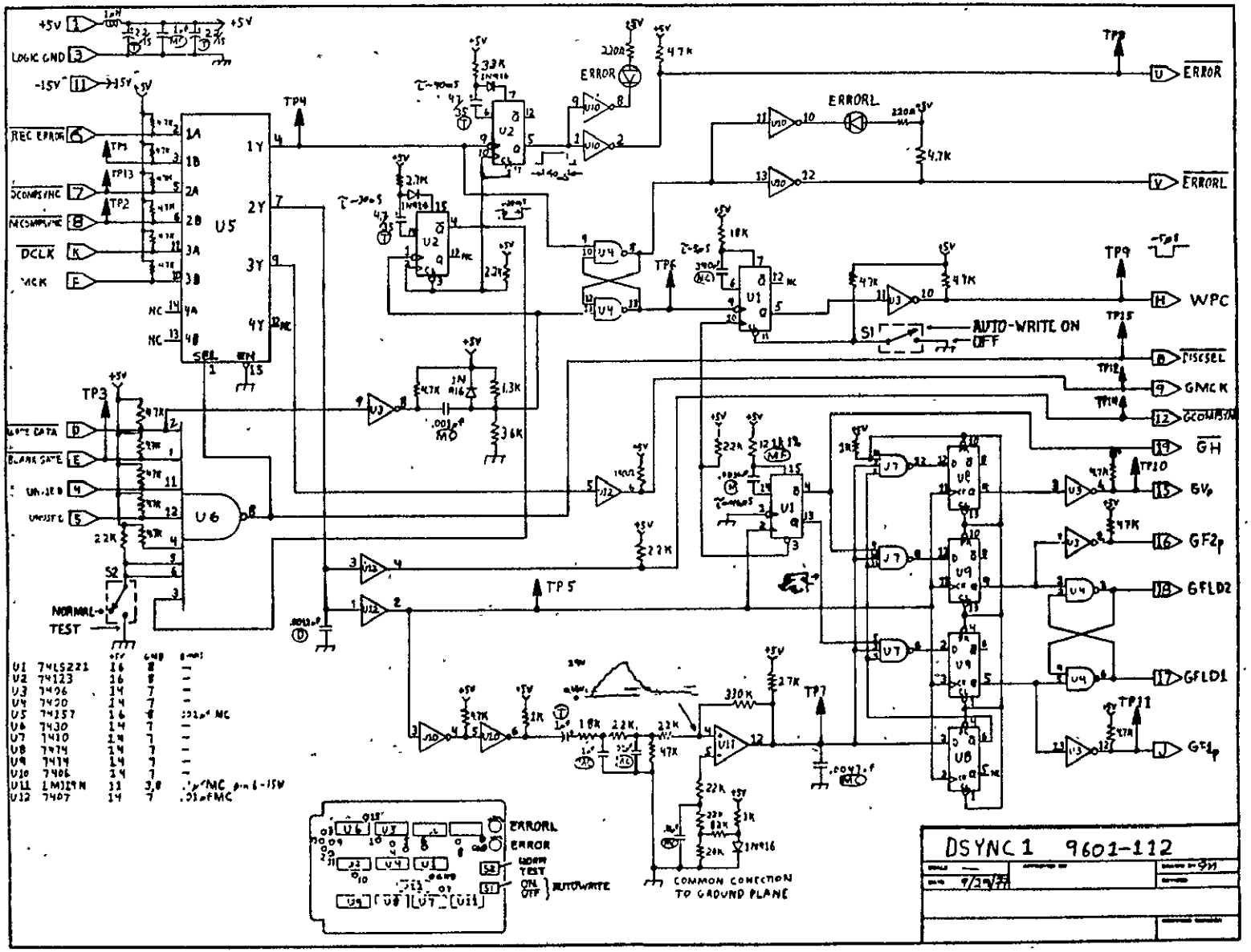


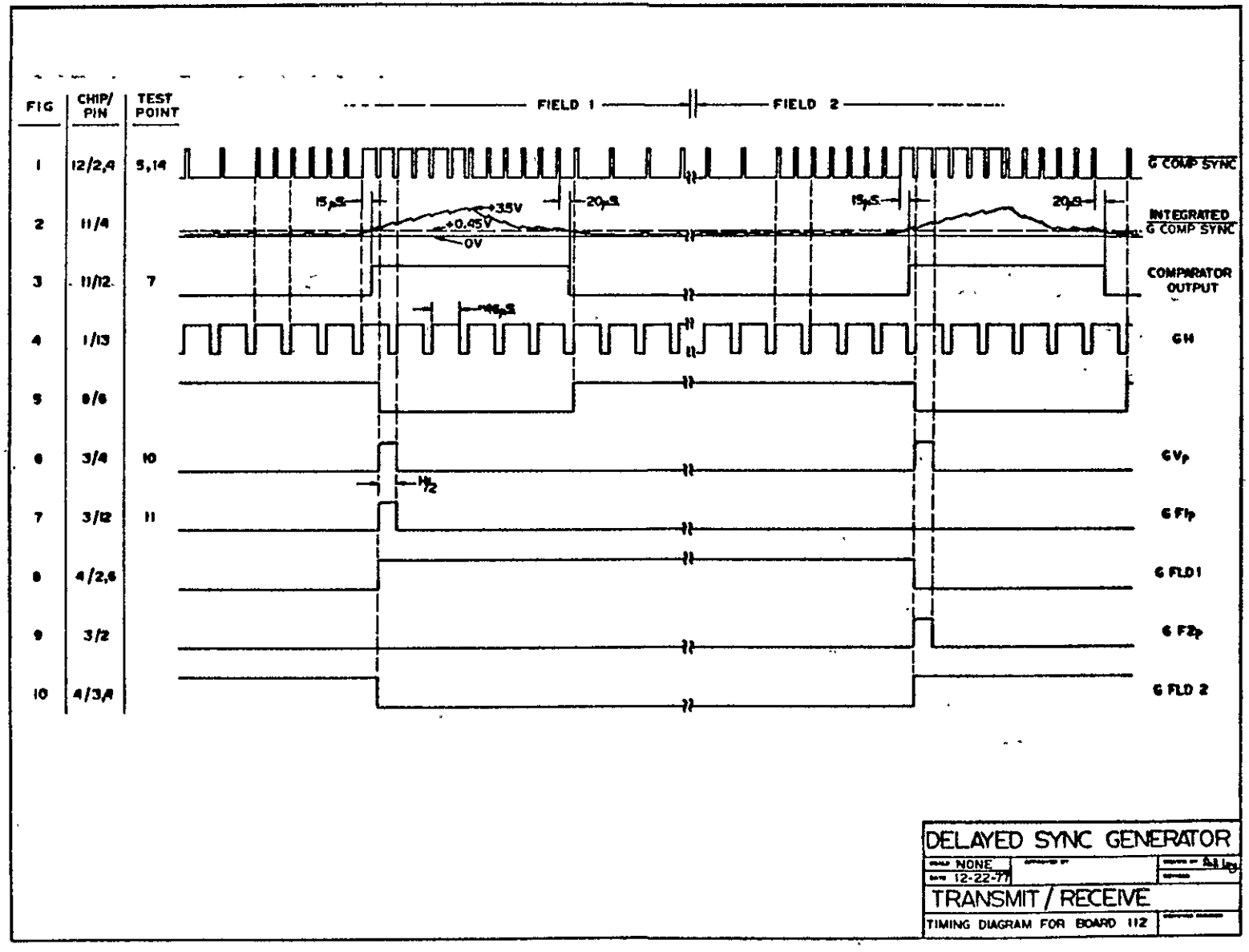
U#	IC	+5V	GND
U1	74S74	14	7
U2	74S112	16	8
U3	74S00	14	7
U4	74S00	14	7
U5	74S74	14	7,13
U6	74S74	14	7
U7	74S00	14	7
U8	74S74	14	7

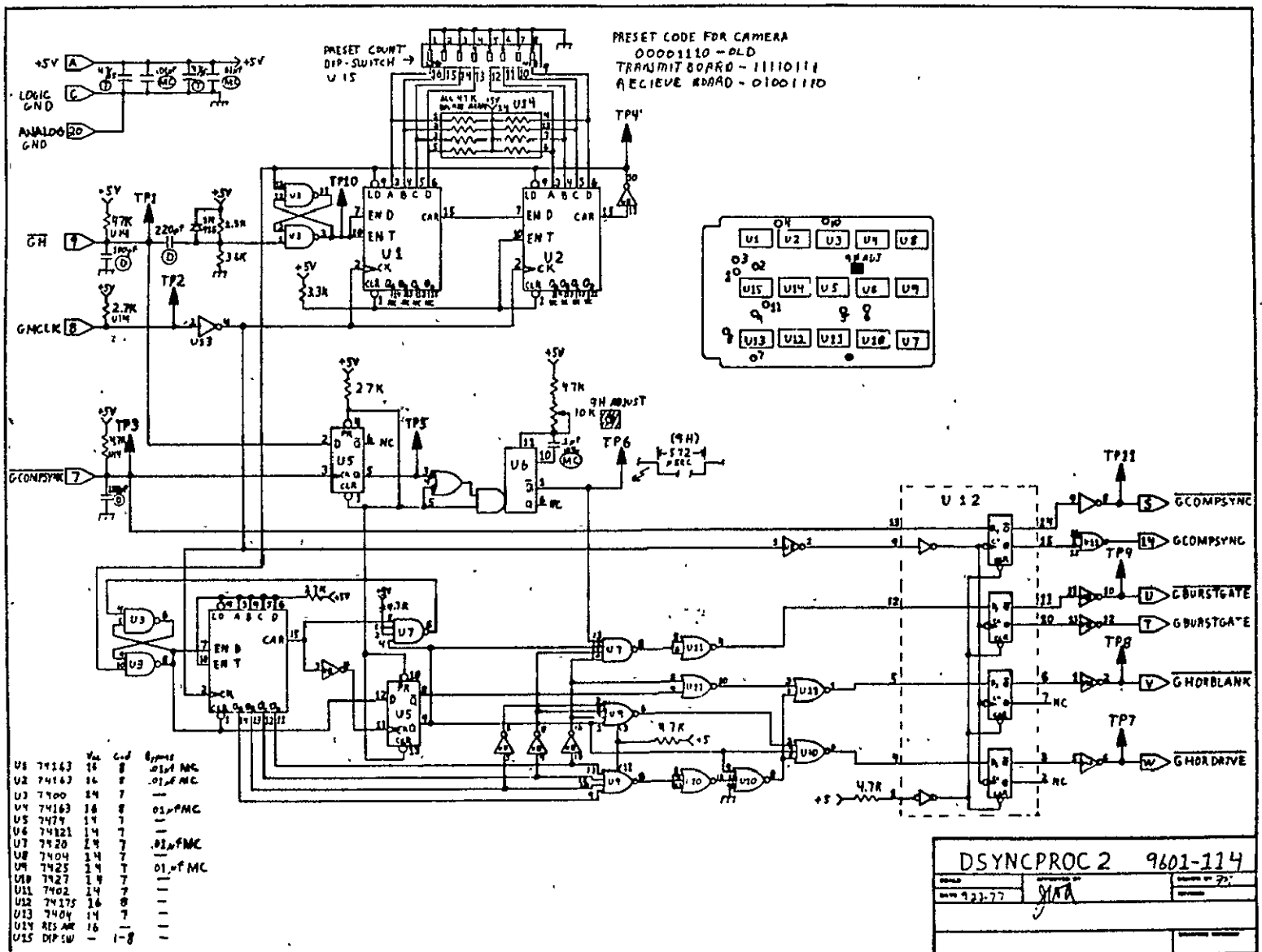
U#	IC	+5V	GND
U9	74S00	14	7
U10	74S00	14	7
U11	74S157	16	8
U12	74S140	14	7
U13	74S74	14	7

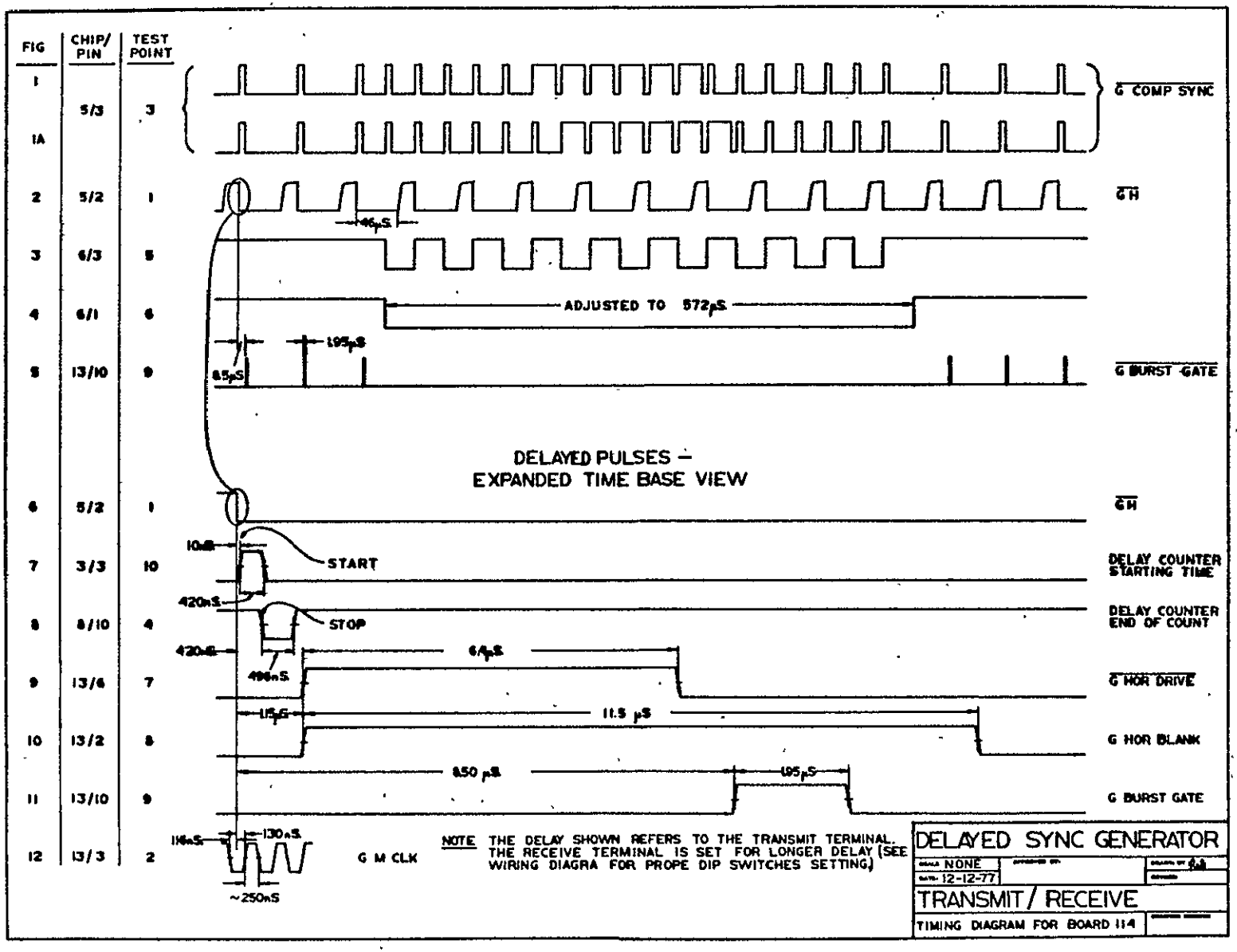

BI-Ø ENCODER / DECODER TIMING (BOARD IN LOCAL)
FIG.
CHIP/PIN
TEST POINT
1 U2/2,3 1
2 U1/3,11; U3/9,10 2
3 U1/5 8
4 U6/2,12 9
5 U5/6 10
6 U5/5 —
7 U10/8 5
8 U13/8 12
9 U10/11 6
RISING EDGE OF SYNC
FALLING EDGE OF SYNC
FALL TIME 6 NS
RISE TIME 150 NS
66NS
58NS
26NS
8 NS
28NS
124 NS
DATA CELL
12NS
22 NS
18NS
500NS
285NS
248NS
5NS
3NS
44NS
32NS
8NS
38NS
DCOMPSYNC
X2CK 6.816 MHZ
BI-Ø MDATA
Ø1 CLOCK
Ø2 CLOCK
DCLK 2.04545 MHZ
CELL CLOCK 4.0909 MHZ
BI-Ø EN/DE-CODER TIMING
200NS/IN
12-7-77
JAM
BOARD #92
DISC PROJECT


BI-Ø DATA IN
TP 1
TP 2
TP 3
TP 4
TP 5
TP 6
TP 7
TP 8
TP10
JITTER < 10NS
JITTER ~ 10NS
(-) TRIG
100 nSEC ADJ
496NS
DCLK/2
2.041545 MHZ
BI-Ø DATA
PLL HOLD
TRK
HOLD
2N4124
1N916
160K
BIAS
Ø ADJ.
+15 V
5V REG
A TO 113. SUB ASSY.
SHIELD BOX
96... - 13 SUB ASSY
+5 V REG
X2 CLK
74S00
74S00
74S112
10414P
MC7805
LM307
4024
74S74
74S04
7805
74S00
74S00
74S00
DATA CLOCK RECOVERY PLL
8-3-77
TRANSMIT/RECEIVE
DISC PROJECT
9601-93/113


+5V
LOGIC GND
-15V
REC ERROR
DCOMPSYNC
MCOMPSYNC
DCLK
MCLK
U5
U6
U1
U2
U3
U4
U7
U8
U9
U10
U11
U12
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
TP14
TP15
S1
S2
AUTO-WRITE ON
OFF
NORMAL
TEST
ERROR
ERRORL
WPC
GMCK
GH
GV
GF2
GFLD2
GFLD1
GF1
DSYNC1 9601-112
COMMON CONNECTION TO GROUND PLANE
AUTOWRITE




PRESET CODE FOR CAMERA
00001110 - OLD
TRANSMIT BOARD - 11110111
RECIEVE BOARD - 01001110
PRESET COUNT DIP-SWITCH → U15
+5V
LOGIC GND
ANALOG GND
GH
GHCLK
GCOMPSYNC
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
9H ADJUST
GCOMPSYNC
GCOMPSYNC
GBURSTGATE
GBURSTGATE
GHORBLANK
GHORDRIVE
NC
DSYNCPROC 2 9601-114



3. ELECTRONIC HETERODYNE HOLOGRAPHY

3.1 Introduction

A system that records optical holograms electronically using a phase modulated reference wave has been developed and is described in this report. Application of phase modulation to the reference wave enables the use of a low resolution camera to record the hologram while still providing separation of the desired object wave information from the undesired self interference terms in the reconstruction process.

The basis of optical holography is the formation and recording of an intereference pattern between an object wave and a reference wave.[1] One component of this interference pattern is an intensity distribution which is proportional to the complex amplitude of the object wave. It is this component which, when recorded and illuminated with a duplicate of the reference wave, permits exact reconstruction of the object wave. Unfortunately, however, the interference pattern also contains information resulting from self interference of the reference wave and of the object wave. These latter components, when recorded and reconstructed, can produce undesired waves which severely degrade the reconstructed object wave unless measures are taken to avoid this. The usual procedure used here is to design the recording geometry such that the reconstructed object wave is physically separated from the undesired waves. This is accomplished by use of an off axis reference wave, the effect of

which is to produce a high spatial frequency "carrier" in the interference term. The cross-interference term then appears as an amplitude modulation of this carrier frequency, while the self-interference terms remain as a base band signal. The net result of this spatial frequency shifting operation is that on reconstruction the object wave is separated in angle from the reconstructed self interference and no degradation occurs. The cost of the off-axis recording geometry is that the recording medium now must have a high resolution (1000 to 2000 lines/mm). While this is straightforward when the recording medium is photographic film, it is impossible with available television cameras, and therefore a new method of separation is necessary. The use of a television camera for electronically recording a hologram is, in principle, possible, because the maximum spatial frequency in the cross interference term is determined largely by the amount of parallax required, although the spatial frequency spectrum of the object will also have some effect. Thus if the self-interference terms can be eliminated, the necessary cross-interference terms can be recorded on a television camera with only a loss of perspective and perhaps some degradation of resolution of object detail. The latter will in fact occur only if the camera cannot resolve object detail in a conventional direct imaging system.

The system described in this report uses heterodyne modulation of the reference beam to eventually eliminate the self interference terms from the hologram. Since the function of a television

camera--in this case a video image dissector--is to convert a spatially varying intensity pattern into a time varying electrical signal, the net result of phase modulation of the reference wave is to produce a time frequency analog of the spatial frequency shift resulting from use of an off-axis reference beam. As a consequence, the various components of the original hologram appear as separated, band-limited signals in the time frequency domain. This enables, by use of coherent mixing and filtering, production at the display device of a hologram containing only information relevant to reconstruction of the real and virtual images, albeit with limited parallax.

A theoretical analysis of the system, including a scheme for production of large parallax views by superposition of a number of limited parallax holograms, is given in Section 3.2. Section 3.3 contains a description of the present system and results obtained to date. Section 3.4 contains a summary of results and a discussion of work to be performed during the next year.

3.2 Electronic Heterodyne Holography-Theory

A means of electronically recording optical holograms using a phase modulated reference wave has been developed. The feasibility of recording holograms via television techniques was first examined by Enloe et al.,[2] who determined the key problem to be the low resolution of the television camera tube (approximately 40 lines/mm). Typical off-axis optical holograms requre a

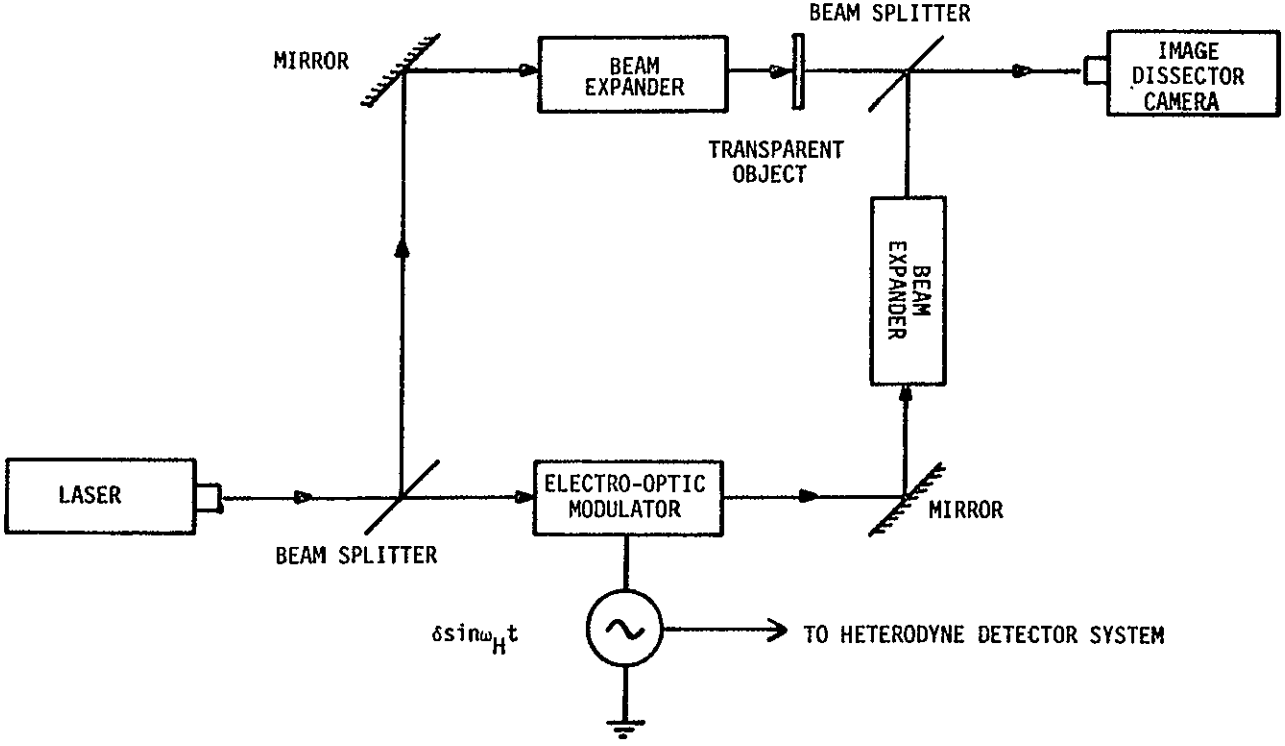
recording medium with resolution of 1000-2000 lines/mm.

To overcome this resolution problem an in-line Gabor recording geometry is used in the system described here to produce a hologram on the photocathode of a television camera tube. This geometry produces spatially overlapping self-and cross-interference terms all of which may lie within the resolution capabilities of the camera but are not spatially separable. However, these terms are separable (temporally) if the hologram reference wave is phase modulated.

Phase modulation of the reference wave temporally modulates the hologram (interference pattern), shifting the cross-interference term to harmonics of the phase modulation frequency. Such a hologram may be recorded with a non-integrating television camera and processed by a heterodyne detector to select only the cross-interference term for subsequent electronic processing and/or display.

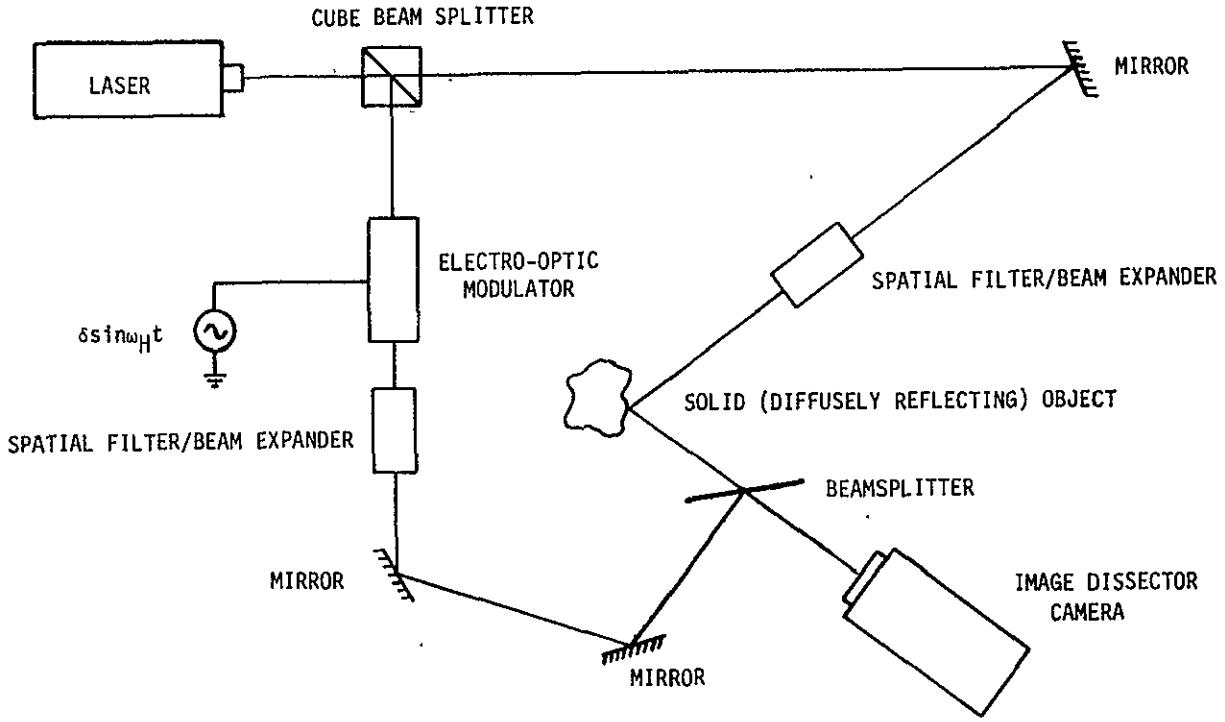
This process of electronic heterodyne holography will be theoretically examined for the recording geometry of Fig. 3.1 in the following sections.

3.2.1 Electronic Recording of Single View Holograms. Consider the recording geometry of Fig. 3.1. The hologram is formed on the photocathode of an image dissector camera (or any other non-integrating type photodetector). The reference wave is phase modulated by an electro-optic modulator and the resulting time-dependent interference pattern is electronically acquired and processed.



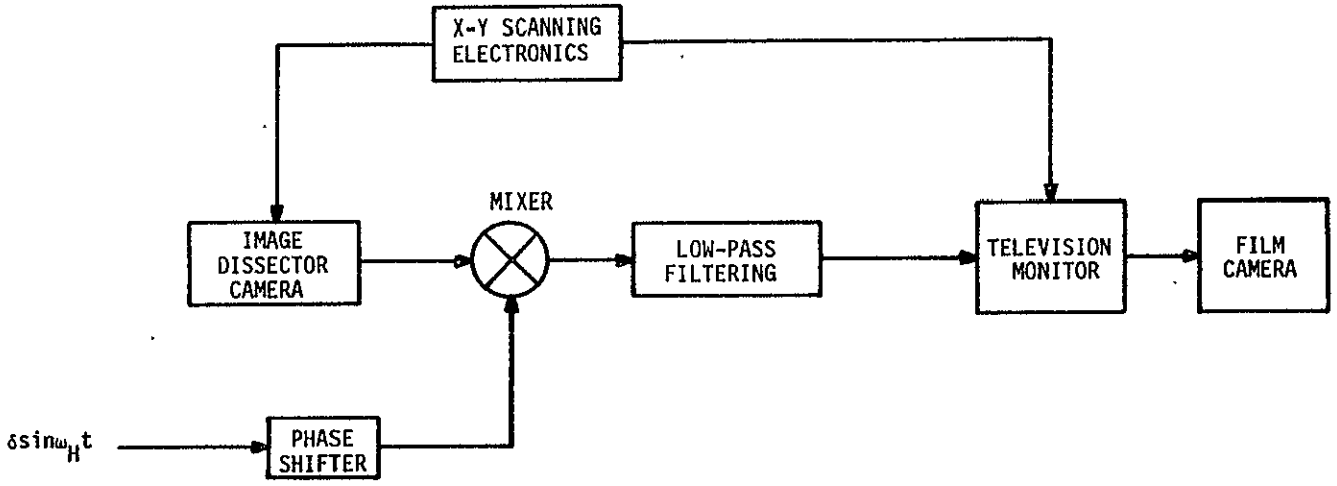
(a) Optical Recording Geometry For Transparent Objects

Figure 3-1. Electronic Heterodyne Recording of Holograms Using A Phase Modulated Reference Wave



(b) Optical Recording Geometry For Opaque, Diffuse Reflecting Objects

Figure 3-1. (Cont.)



(c) Phase Sensitive Detector And Non-Real Time Hologram Recorder

Figure 3-1. (Cont.)

Let the object wave be described by the plane wave expansion

$$U_o(x,y) = \sum_i O_i(x,y) \cos[\omega t - \Omega_i x] \quad , \tag{3.1a}$$

where

$$\Omega_i = (2\pi \sin\theta_i)/\lambda \quad ,$$

λ is the wavelength of the recording light, and ω is its circular frequency. Note that this is an expansion of an optical wavefront in terms of its angular spectrum.[3]

The reference wave may be similarly written as

$$U_R(x,y) = R(x,y) \cos[\omega t + \delta \sin \omega_H t] \tag{3.1b}$$

which is a single plane wave normally incident upon the recording surface. The phase of this plane wave is modulated at a frequency ω_H (called the heterodyne frequency) with a modulation index δ.

If an image dissector camera, i.e., an x-y scannable photomultiplier, is used for recording, it acts as a square law detector followed by a low-pass filter.

The optical amplitude on the recording surface, the photocathode of the camera, is then

$$e(x,y) = R \cos[\omega t + \delta \sin \omega_H t] + \sum_i O_i \cos[\omega t - \Omega_i x] \quad , \tag{3.2}$$

where the explicit x,y dependence has been dropped for brevity of notation. Squaring (3.2) and recognizing that optical frequency terms will be filtered out by the camera, the camera output will be given by

$$\overline{e^2} = \frac{R^2}{2} + \frac{1}{2}\sum_i \sum_j O_i O_j \cos[(\Omega_i - \Omega_j)x] + \sum_i RO_i [\cos\Omega_i x \cos(\delta \sin\omega_H t) - \sin\Omega_i x \sin(\delta \sin\omega_H t)] \quad (3.3)$$

It is interesting to establish a physical interpretation of (3.3), i.e., the physical result of phase modulation of the holographic reference wave. Consider the sinusoidal interference pattern of Fig. 3.2. As a most general case of non-uniform background intensity $A(x)$ [to represent the presence of other images, e.g., self-interference terms] is assumed. The interference pattern intensity may be written as

$$I(x) = A(x) + B \cos kx \quad (3.4)$$

where k is the spatial frequency of the interference pattern. Assume that at any point x_o one can sinusoidally shift (phase modulate) the interference pattern δ radians about x_o at a frequency ω_H, the shift, $S(x_o)$, is given by

$$S(x_o,t) = A(x_o) + B\cos[kx_o + \delta \sin\omega_H t]$$

$$S(x_o,t) = A(x_o) + B\cos kx_o \cos[\delta \sin\omega_H t] - B \sin kx_o \sin[\delta \sin\omega_H t] \quad (3.5)$$

The result (3.5) is completely analogous to the terms in the series expansion of (3.3) indicating that these terms represent an apparent spatial shifting (modulation) of the hologram at an angular frequency ω_H.

Returning to (3.3), the holographic cross-interference terms required for reconstruction may be explicitly formed by expanding

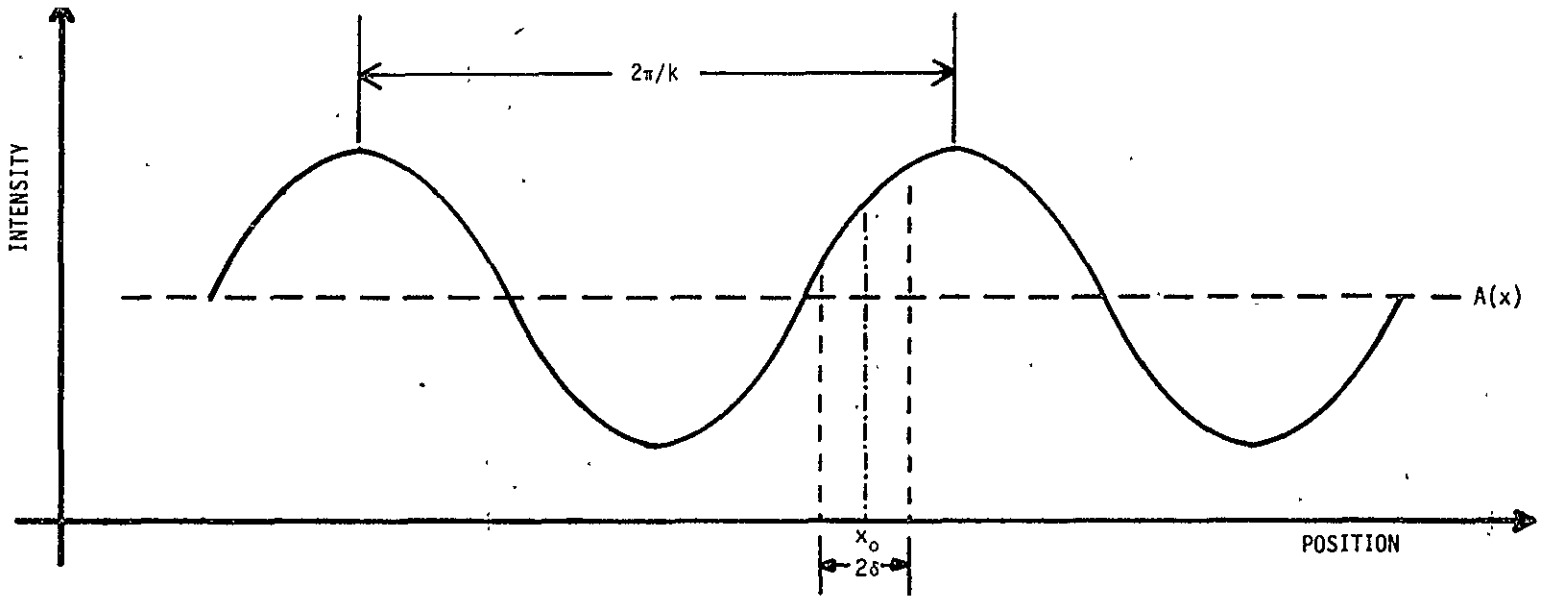


Figure 3-2. Sinusoidal Interference Pattern Phase Modulated At x_o

the expressions $\cos[\delta\sin\omega_H t]$ and $\sin[\delta\sin\omega_H t]$ in a Fourier-Bessel series, i.e.,

$$\cos(\delta\sin\omega_H t) = J_o(\delta) + 2\sum_{\ell=1}^{\infty} J_{2\ell}(\delta)\cos(2\ell\,\omega_H t)$$

$$\sin(\delta\sin\omega_H t) = 2\sum_{\ell=o}^{\infty} J_{2\ell+1}(\delta)\sin[(2\ell+1)\,\omega_H t] \qquad (3.6)$$

Using (3.6) in (3.3) and rearranging terms

$$\overline{e^2} = \frac{R^2}{2} + \frac{1}{2}\sum_i\sum_j O_i O_j \cos[(\Omega_j-\Omega_i)x] + RJ_o(\delta)\sum_i O_i \cos\Omega_i x$$

$$+ 2R\sum_{\ell=1}^{\infty} J_{2\ell}(\delta)\left[\sum_i O_i \cos\Omega_i x\right]\cos(2\ell\,\omega_H t)$$

$$- 2R\sum_{\ell=o}^{\infty} J_{2\ell+1}(\delta)\left[\sum_i O_i \sin\Omega_i x\right]\sin(\{2\ell+1\}\,\omega_H t) \qquad (3.7)$$

The terms $2RJ_{2\ell}(\delta)\sum_i O_i\cos\Omega_i x$ and $-2RJ_{2\ell+1}(\delta)\sum_i O_i\sin\Omega_i x$ represent the cross-interference terms required for holographic reconstruction of $U_o(x,y)$. All other terms are self-interference terms.

3.2.2 Separation of Cross- and Self-Interference Terms. In conventional optical holography the cross-interference terms, i.e., the real and conjugate terms, are separated from the self-interference terms by recording with an off-axis reference wave. The off-axis reference is manifested on the hologram as a high spatial frequency carrier (1000-2000 lines/mm) onto which the image

terms are modulated by the interference process. As a consequence only high resolution recording media can be used to record an off-axis hologram. This high frequency recording medium requirement has been the major obstacle to television recording of holograms. In general, television cameras have maximum resolutions on the order of 40-60 lines/mm. This is over an order of magnitude less than the resolutions required to record an off-axis hologram. Only when a Gabor configuration is used to record a hologram is the response of the television camera adequate--however, the self- and cross-interference terms spatially overlap and the resulting images are not optically separable.

A close examination of (3.7) shows that phase modulation of the optical reference wave allows separation of the self- and cross-interference terms in an in-line geometry. The cross-interference terms lie at multiples of the heterodyne frequency f_H and may be selectively detected by filtering and/or heterodyne detection.

The criterion for selecting which harmonic is to be detected depends upon the relationship among the heterodyne frequency, camera scan rate, and spatial frequency spectrum of the object wave. Consider, for example, the first harmonic term. From (3.7)

$$S_1 = -2RJ_1(\delta)\left(\sum_i O_i \sin\Omega_i x\right) \sin\omega_H t \qquad (3.8)$$

If (3.8) is scanned horizontally at a velocity v_x, each component of the summation will give rise to a temporal frequency component

$$f_i = v_x \frac{2\pi \sin\theta_i}{\lambda} = v_x \Omega_i$$

The effects of vertical scanning may be neglected since horizontal scan velocities are much higher than vertical scan velocities for television-type raster scan formats.

Note that if the angular spectrum of U_o is limited to a maximum angle θ_{max}, i.e., the maximum angular field of view is θ_{max}, it follows that the recorded hologram will be temporally band-limited to the frequency interval $[0,f_{max}]$ where

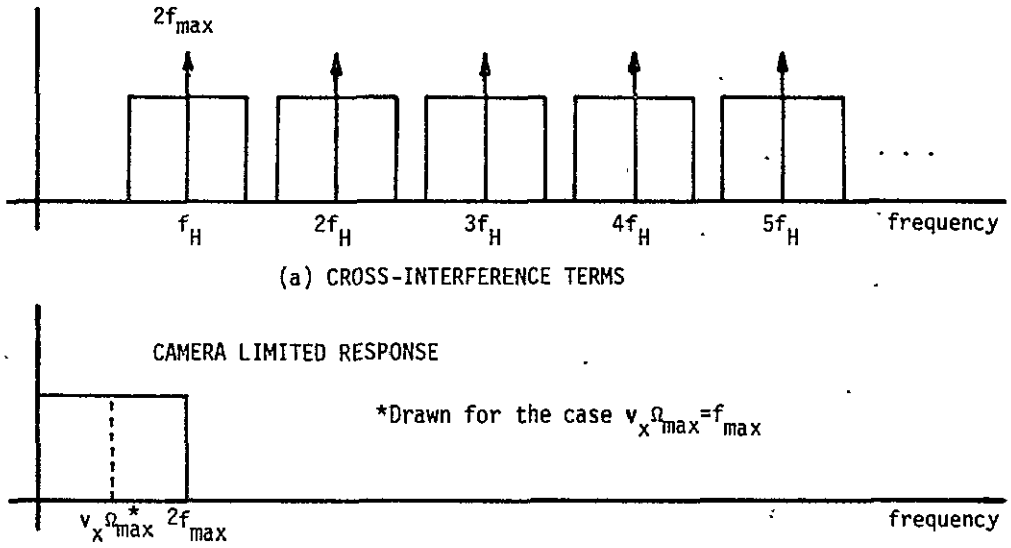
$$f_{max} = \frac{v_x 2\pi \sin\theta_{max}}{\lambda} = v_x \Omega_{max} \tag{3.9}$$

The object term may then be viewed as a signal of bandwidth f_{max} modulated onto the carrier f_H.

Because the reference wave is modulated at a single sinusoidal frequency ω_H, the spectral width of the reference wave is negligible. As a result the temporal frequency spectrum of (3.7) is much like a picket fence (Fig. 3.3). The self-interference terms

$$\frac{R^2}{2} + \frac{1}{2}\sum_i \sum_j O_i O_j \cos[(\Omega_i - \Omega_j)x] + RJ_o(\delta) \sum_i O_i \cos\Omega_i x$$

are temporally band-limited to $2f_{max}$, however, the camera response bandlimits the self-interference terms to f_{max}. This assumes that the camera resolution determines f_{max} since from (3.9) $f_{max} = v_x \Omega_{max}$ where Ω_{max} is the maximum resolution of the camera. If



Legend: f_{max} - maximum temporal frequency content of scanned hologram

v_x - camera scan velocity

Ω_{max} - maximum camera spatial frequency response

f_H - heterodyne frequency

Selection criteria: $f_H > 2f_{max}$

Figure 3-3. Frequency Spectrum of Camera Output For Electronic Heterodyne Recording of A Hologram

the camera's resolution is limited by Ω_{max} the self-interference terms occupy the spectral region $[0, v_x\Omega_{max}]$ as shown in Fig. 3.3. (In most cases the camera resolution will determine f_{max}.) This gives rise to the criterion

$$f_H \geq 2\, v_x \Omega_{max} \tag{3.10}$$

for separation of the cross-interference terms in the camera output spectra. Assuming that this criterion is satisfied, the harmonics of ω_H in (3.7) are individually separable by bandpass filtering or heterodyne detection. For purposes of illustration assume that (3.7) is bandpass filtered to obtain the term centered at ω_H. Let S_1 denote this term

$$S_1(t) = -2J_1(\delta)R(v_x t, y)\left(\sum_i O_i(v_x t, y)\right)\sin\Omega_i v_x t \sin\omega_H t \tag{3.11}$$

3.2.3 Display of Recorded Holograms. Once the cross-interference term has been recorded, an optical display must be produced. One method of producing a display is to write the cross-interference term onto a display device (CRT, etc.) and photograph the resultant two-dimensional image. If the film is properly exposed, the amplitude transmittance of the resulting photograph, using (3.11) as the signal to be recorded, is

$$T(x,y) = I_B - \gamma 2J_1(\delta)R(x,y)\left(\sum_i O_i(x,y)\right)\sin\Omega_i x \sin\left(\frac{\omega_H x}{v_x}\right) \tag{3.12}$$

where I_B is an optical bias level and γ is a proportionality

constant. Note that it is assumed that no scale transformations take place in the recording process. The factor $\sin(\omega_H x/v_x)$ in (3.12) is the result of retaining the carrier frequency term $\sin\omega_H t$ in the recording process; the temporal frequency ω_H is translated into a spatial frequency ω_H/v_x in the recorded hologram. The hologram (3.12) is identical to the hologram resulting from optically recording an off-axis hologram at an angle θ where

$$\sin\theta = \frac{f_H}{v_x}\lambda \tag{3.13}$$

and λ is the wavelength of the light used to record and reconstruct the hologram. The result of reconstructing such a hologram is shown in Fig. 3.4.

In practice, band-pass filtering cannot be used to select the cross-interference term if a two-dimensional display is to be generated. The term $\sin(\omega_H x/v_x)$ must maintain the same relative phase from line to line in the display. This is not possible unless the horizontal scan and the heterodyne oscillator are phase locked. A simpler alternative is to heterodyne detect the desired holographic term--a process which removes the carrier frequency term. The carrier may then be reinserted before writing the hologram onto a display by modulating the detected signal with a triggered oscillator. In this manner any off-axis reference wave within the resolution capability of the display may be generated. It is not necessary that an off-axis reference wave be reintroduced prior to

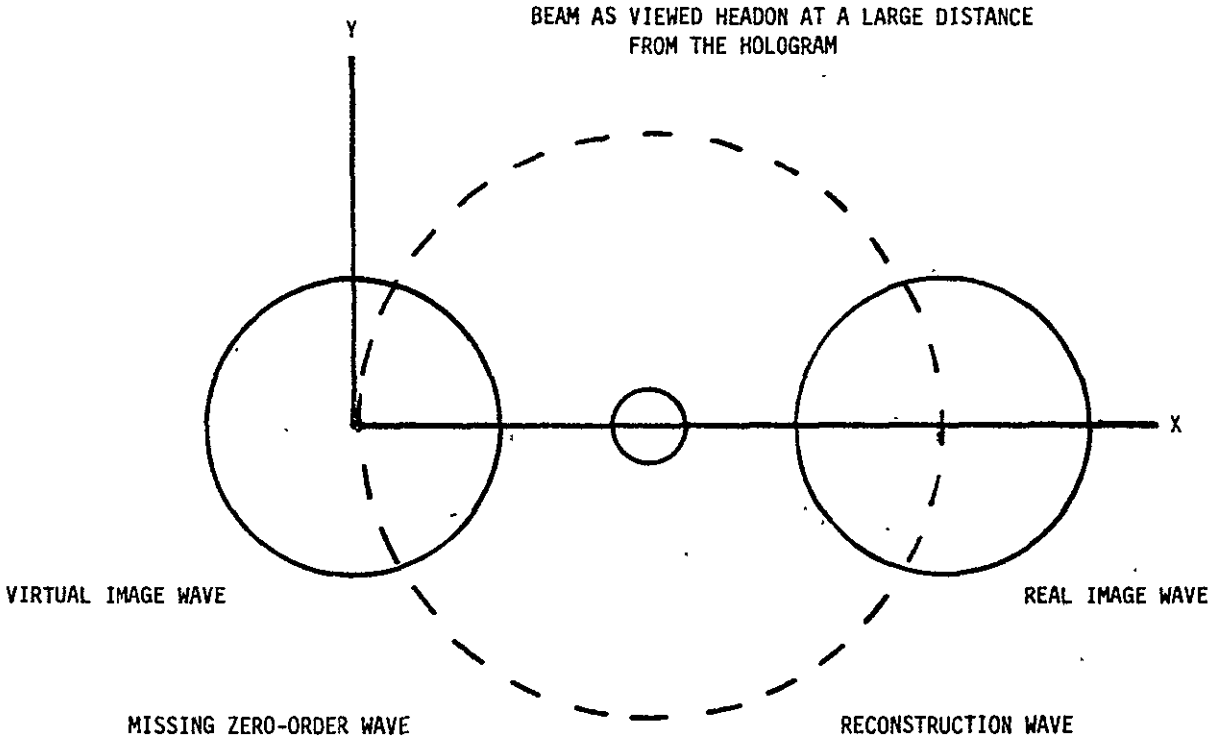


Figure 3-4. Result of Reconstructing Electronic Heterodyne Hologram

writing the display; (3.11) may be written onto the display without carrier insertion to yield an in-line hologram.

3.2.4 Multi-View (Wide Perspective) Holograms. In principle, it is possible to replicate a higher resolution hologram than can be resolved by the camera. The resolution of the camera limits the resolution of the recorded hologram to 40-60 lines/mm. However, the display device will often have a higher resolution. Even if it does not, the effective resolution may be increased by using a large display device with a sufficient number of resolution elements for writing and photographically reducing the replicated hologram. Any extra resolution of the display may be used to advantage to synthesize single wide-perspective holograms from several narrower perspective holograms.

In such a hologram each view corresponds to a different direction, or angle, of the phase modulated reference with respect to the normal to the recording plane. The direction of the reference wave may be shifted by rotating the final beam splitter in Fig. 3.1.

Each view (hologram) is assigned a unique off-axis reference wave incident at an angle which may be written in the manner of (3.1b) as

$$(U_R)_n = R_n \cos[\omega t + \delta \sin\omega_H t - \Omega_n x] \tag{3.14}$$

where the subscript indicates an unique off-axis reference. The object wave will remain the same as (3.1a). For this choice of object and reference wave the camera output will be

$$\overline{e_n^2} = \frac{1}{2} R_n^2 + \frac{1}{2} \sum_i \sum_j O_i O_j \cos[(\Omega_j - \Omega_i)x] \tag{3.15}$$

$$+ \sum_i R_n O_i \{\cos\Omega_i x \cos(\delta \sin\omega_H t - \Omega_n x) - \sin\Omega_i x \sin(\delta \sin\omega_H t - \Omega_n x)\}$$

Expanding (3.15) in a Fourier-Bessel series and collecting terms

$$\overline{e_n^2} = \frac{1}{2} R_n^2 + \frac{1}{2} \sum_i \sum_j \cos[(\Omega_j - \Omega_i)x] + J_o(\delta)\, R_n \sum_i O_i \cos(\Omega_i - \Omega_n x)$$

$$+ 2R_n [\sum_i O_i \cos\{(\Omega_i - \Omega_n)x\}] \sum_{\ell=1}^{\infty} J_{2\ell}(\delta) \cos 2\ell\omega_H t$$

$$- 2R_n [\sum_i O_i \sin\{(\Omega_i - \Omega_n)x\}] \sum_{\ell=o}^{\infty} J_{2\ell+1}(\delta) \sin[(2\ell+1)\omega_H t] \tag{3.16}$$

If a heterodyne detector is used to selectively detect the first harmonic output of the camera, the detector output will be

$$S_n = -2R_n J_1(\delta) [\sum_i O_i \sin\{(\Omega_i - \Omega_n)x\}] \tag{3.17}$$

Note that this term is low-pass filtered by the camera to the frequency interval $[O, f_{max}]$.

The corresponding term for an on-axis reference wave was

$$S_1 = -2R\, J_1(\delta) \sum_i O_i \sin\Omega_i x \tag{3.18}$$

A comparison of (3.17) and (3.18) reveals that the effect of an off-axis reference wave is to linearly shift the spatial frequency spectrum of the object wave by an amount $\Delta\Omega$. A particularly useful choice of $\Delta\Omega$ is

$$\Omega_n = n\Delta\Omega = n\Omega_{max} \qquad n = 0, 1, 2, \ldots, N \qquad (3.19)$$

If (3.19) is satisfied, each view will be a different segment of the total spectrum of the object wave. These views can be combined on a suitable high-resolution display to recreate the total spectrum of the object wave (see Fig. 3.5 and Fig. 3.6).

Because each view has a bandwidth of $\Delta\Omega$ the views may be frequency multiplexed together before the recording process to yield a higher frequency spectrum of the object than the camera can record. The recording process then translates this temporal frequency multiplexing into spatial frequency multiplexing of the individual holograms to create a wide-view, high resolution hologram.

To model this concept, let N views of an object be acquired in the manner of (3.17) and stored in a suitable video memory device (such as a video disc). Each view S_n is recorded with an off-axis reference wave at an angle θ_n defined by

$$\sin\theta = n\lambda\Omega_{max} \qquad (3.20)$$

Prior to being written onto the display, each image S_n is modulated by a sinusoidal signal of frequency f_n, defined by

$$f_n = nv_x\Omega_{max} \; . \qquad (3.21)$$

Assume that each view, S_n, is read out from the memory device and written onto the display at a scan velocity so that the explicit substitution $x = v_x t$ may be made in (3.17). If the resulting

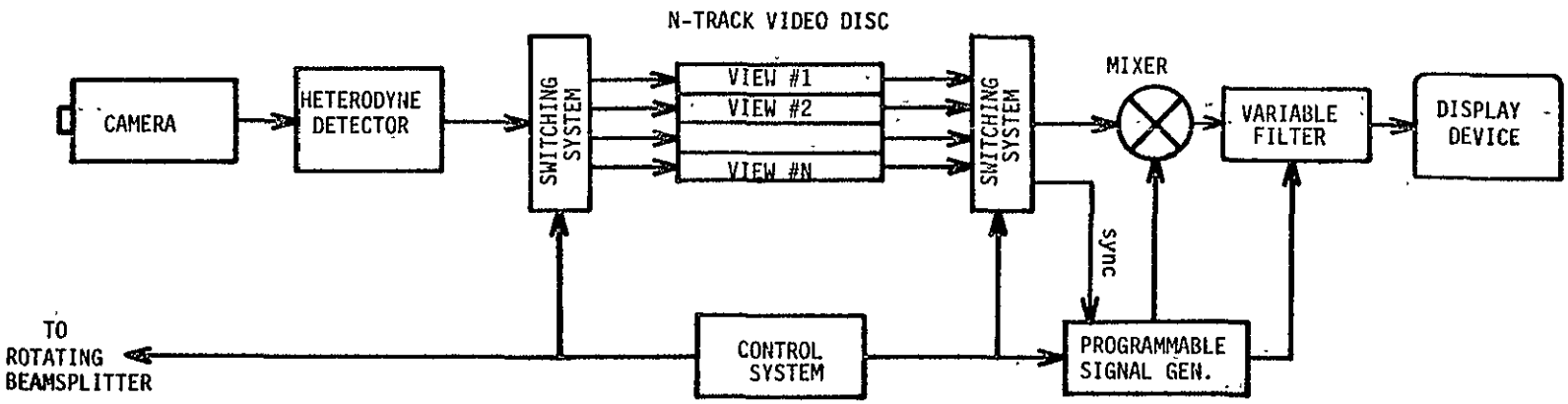
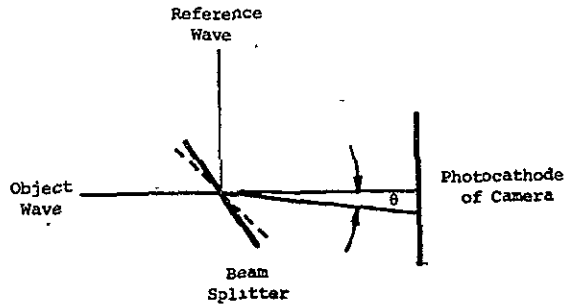
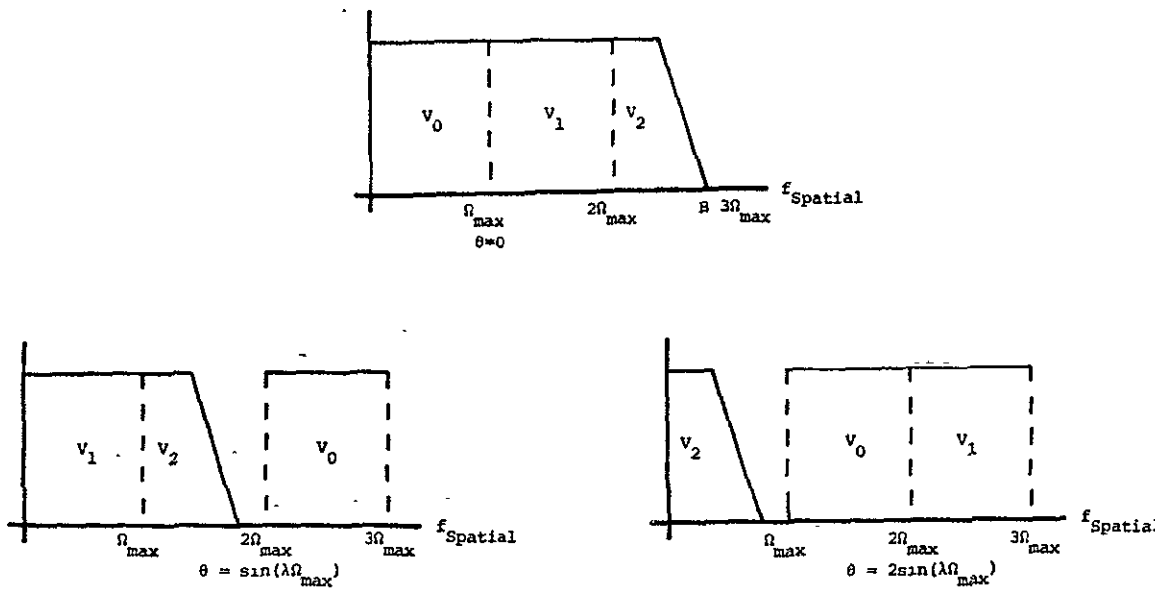


Figure 3-5. Schematic Diagram of System to Synthesize Wide Perspective Holograms From Narrow View Holograms Using A Multi-Track Video Disc Electronic Memory



Recording Wavelength-λ
Maximum Spatial Frequency Response of Camera - Ω_{max}

(a) Recording geometry for recording holograms via heterodyne method.



B = maximum spatial frequency of hologram

(b) Spatial frequency spectrum of hologram (cross-interference term) for different recording angles.

Figure 3-6. Wide-Perspective, Multi-View Hologram Concept.

Recording Angle, θ	0	$\sin^{-1}(\lambda\Omega_{max})$	$2\sin^{-1}(\lambda\Omega_{max})$
View within Camera Response	$V_o(x)$	$V_1(x)$	$V_2(x)$
Camera Output ($x = Vt$)	$V_o(t)$	$V_1(t)$	$V_2(t)$
Frequency Shift Camera Output and High-Pass Filter	$V_o(t)$	$V_1(t)\cos\omega_1 t$; $\omega_1 = V\Omega_{max}$	$V_2(t)\cos\omega_2 t$; $\omega_2 = 2V\Omega_{max}$
Record onto Film at Velocity V ($t = \frac{x}{V}$) Develop & Expose Film	$c_o + \gamma V_o(x)$	$c_1 + \gamma V_o(x)$	$c_2 + \gamma V_2(x)$
Spectrum of Transparancy	$[0, \Omega_{max}]$	$[\Omega_{max}, 2\Omega_{max}]$	$[2\Omega_{max}, 3\Omega_{max}]$

c_o, c_1, c_2 = background transparancy

γ = film constant

(c) Process and record single views onto film.

$$T = \sum_i c_i + \gamma \sum_i V_i$$

Uniform Background Wide-Perspective Hologram

(d) Superimpose views to achieve a wide perspective hologram.

Figure 3-6. Continued.

expression is modulated by a sinusoidal signal of frequency Ω_n defined by (3.21), each view becomes

$$S'_n = R_n J_1(\delta)\left[\sum_i O_i \cos\Omega_i v_x t\right]_n + R_1 J_1(\delta) \sum_{n=1}^{N} O_i \cos(\Omega_i v_x t - 2\Omega_n v_x t) \quad . \tag{3.22}$$

Equation (3.22) may be high-pass filtered to remove the second term. Such filtered terms may be combined, either electronically or optically, onto a display of sufficiently high resolution to yield a display transmittance

$$T(x,y) = I_B + \gamma \sum_{n=1}^{N} R_n J_1(\delta)\left[\sum_i O_i \cos\Omega_i v_x t\right]_n \quad , \tag{3.23}$$

where each view has been reinserted into its proper frequency slot to recreate the original wide perspective object wave (see Fig. 3.6). Note that the maximum optical density of the display medium will determine the contrast of the individual holograms if many holograms are to be combined. If n such holograms are to be displayed at one time each hologram can only utilize $1/n$ of the usable optical density range if the resultant display is to have a linear display of intensity.

A schematic diagram of a system capable of recording and displaying wide-perspective electronic holograms is shown in Fig. 3.5. Note that heterodyne detection is necessary to this concept--the individual holograms are band limited to $\Delta\omega$ to allow maximum utilization of the bandwidth of the video disc buffer memory. Baseband recording onto a video disc provides simple, low-cost storage

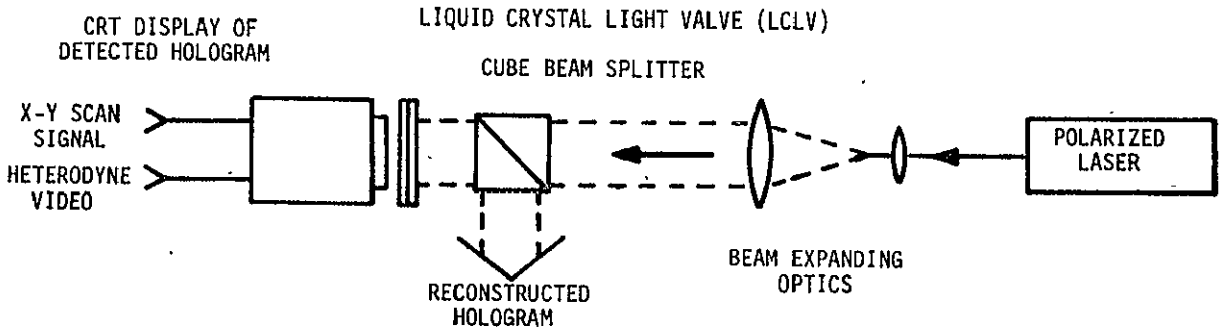
for a large number of electronic holograms with the carriers being reinserted prior to the display process.

It is significant that several devices which appear capable of synthesizing multi-view holographic displays have recently become commercially available. Hughes Aircraft has developed a liquid crystal light valve which may be written with a CRT and can be used to modulate the phase of light reflected from it. A display system concept based upon this device is shown in Fig. 3.7(a). Itek Corporation has developed the Pockels Read Out Modulator which phase modulates light transmitted through it. This device must be written by a laser operating in the blue-green portion of the spectrum. A display concept using this device is shown in Fig. 3.7(b). Future theoretical work on the synthesis of multi-view holograms will be coordinated with an analysis of available technology to determine achievable goals.

3.3 Experimental Confirmation of Electronic Heterodyne Recording

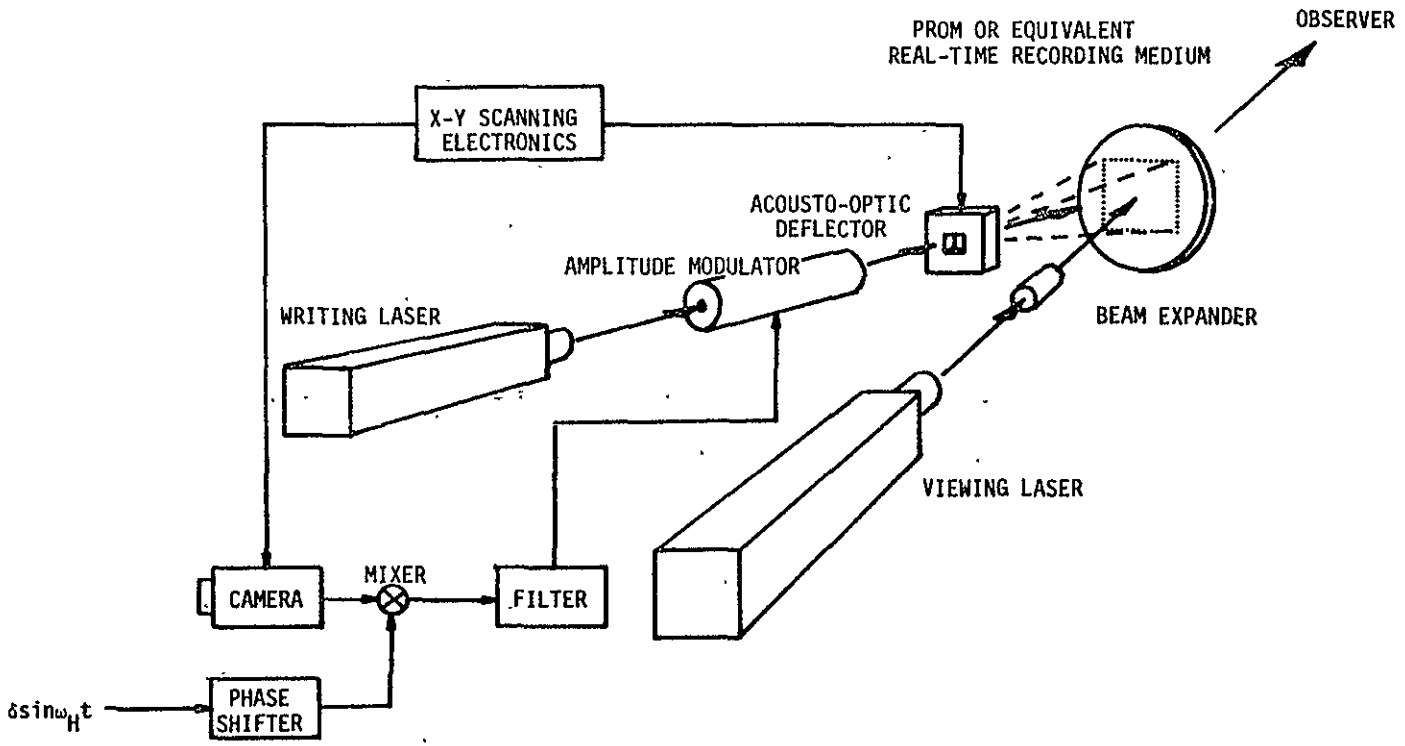
In the previous section the theory underlying the electronic heterodyne recording of holograms was developed; in this section experimental investigation of electronic heterodyne recording principles will be reported.

3.3.1 The Experimental System. The optical arrangement used for testing the heterodyne detection concept is shown in Fig. 3.8. The configuration is essentially that of a Mach-Zehnder interferometer and is used to generate simple interference patterns from the



(a) Real-Time Holographic Display Using CRT Controlled Liquid Crystal Light Valve

Figure 3-7. Real-Time Holographic Display Concepts



(b) Real-Time Holographic Display Using PROM

Figure 3-7. (Cont.)

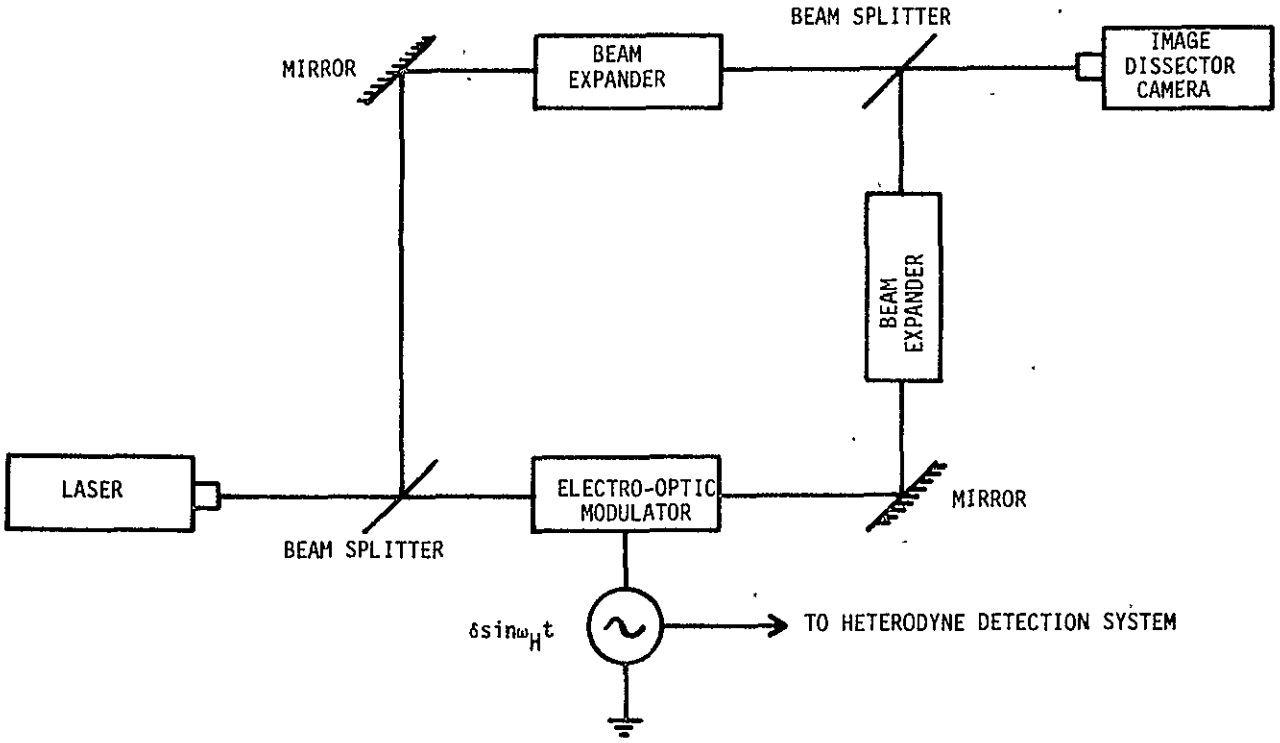


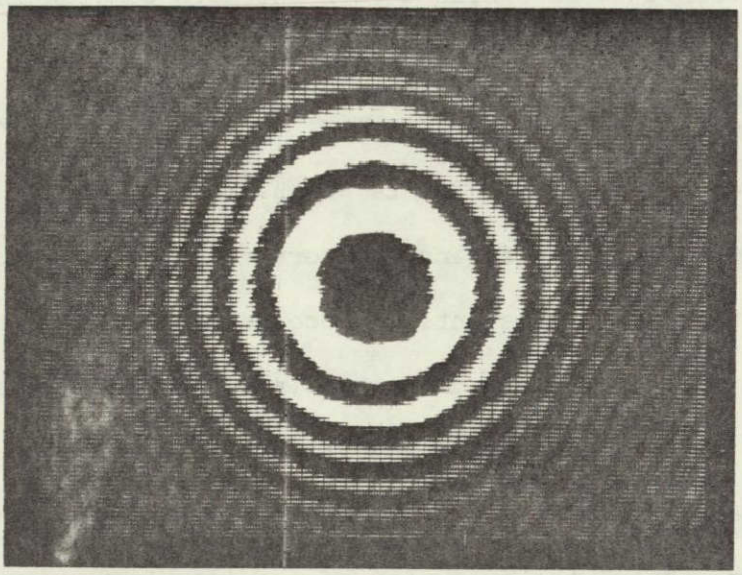
Figure 3-8. Optical Configuration For Testing Electronic Heterodyne Holography Concept

interference of plane or spherical waves. Such simple interference patterns are not to be confused with the more complex interference patterns associated with optical holograms of objects.

In the system diagrammed in Fig. 3.8, beam expanders are used to generate spherical wave fronts which are combined at the beam splitter to create interference patterns similar to that shown in Fig. 3.9. Note that this interference pattern is circularly symmetric and does not have a uniform fringe spacing. This pattern was originally chosen to test the spatial frequency response of the camera/detector/CRT recording system. However, to measure spatial frequency response, the intensity of the interference pattern must be uniform over the apeture of the camera--a feature which was found to be impossible to accomplish with the small beam expanders available. Although the interference pattern was not suitable to measure spatial frequency response it did prove satisfactory to demonstrate the principle of electronic heterodyne detection and replication as well as to establish the basic parameters of the detection electronics.

3.3.2 Spectral Analysis of the Detector Output. A spectrum analyzer was used to examine the output of the image dissector camera (see Specifications, Appendix I) used in the optical configuration of Fig. 3.8.

The spectrum analyzer was first used to establish the noise levels of the equipment. With the optical components securely fastened to a massive vibration isolated optical bench and a glass case



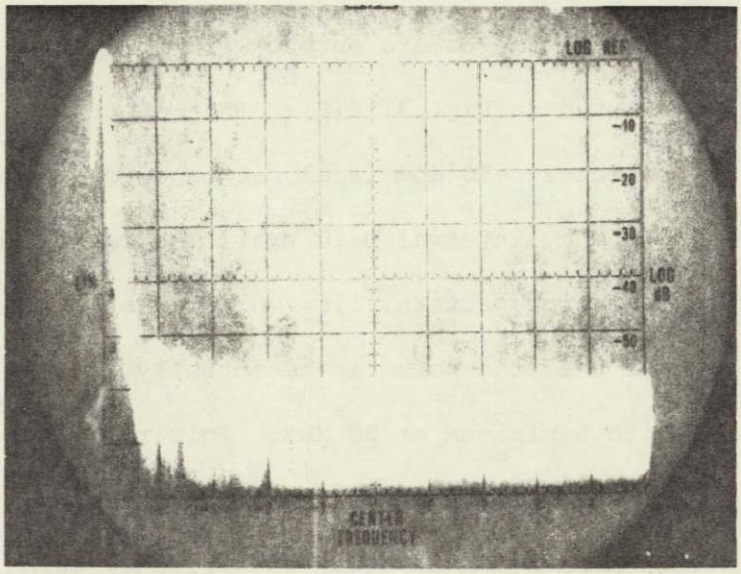
Experimental Data:
PAR 5202 Lock-In Amplifier, 100 Hz Bandwidth
Heterodyne Frequency = 100 kHz
Electro-Optic Modulator Drive = 200 volts p-p

Figure 3-9. Typical Interference Pattern Recorded In Test Configuration of Figure 3-8.

enclosing the experiment, interference patterns remained stable over periods in excess of ten minutes. (Ten minutes was simply the longest time period examined and it is probable that the interference pattern is stable over much longer periods.)

The noise level of the camera output with no optical input to the camera is presented in Fig. 3.10(a). This electronic noise was found to be approximately -70 dbm (analyzer bandwidth = 10 kHz) throughout the frequency interval 0-10 MHz. The camera response to a stationary interference pattern, i.e., no modulation, is shown in Fig. 3.10(b). Note that the noise is essentially flat to 10 MHz and quickly decreases to a minimum at 20 MHz. This roll off corresponds with the frequency response characteristics of the camera.

The frequency separation of cross-interference terms may be observed by examining the camera output in the frequency domain when the reference wave is phase modulated and the camera is not scanned. The spectrum of the camera output for this situation is shown in Fig. 3.11. Using a phase modulation frequency of 100 kHz the first and second harmonics are easily discernable above the camera noise. The first harmonic is approximately 30 db above the noise level; the second harmonic, 15 db. This information by itself is not sufficient to predict the quality of the hologram as recorded on film. Film recordings of interference patterns were made from the first and second harmonic signals and, although the signal levels did differ considerably, the recorded interference patterns were similar (see Fig. 3.12). This experiment will be reported upon in more detail



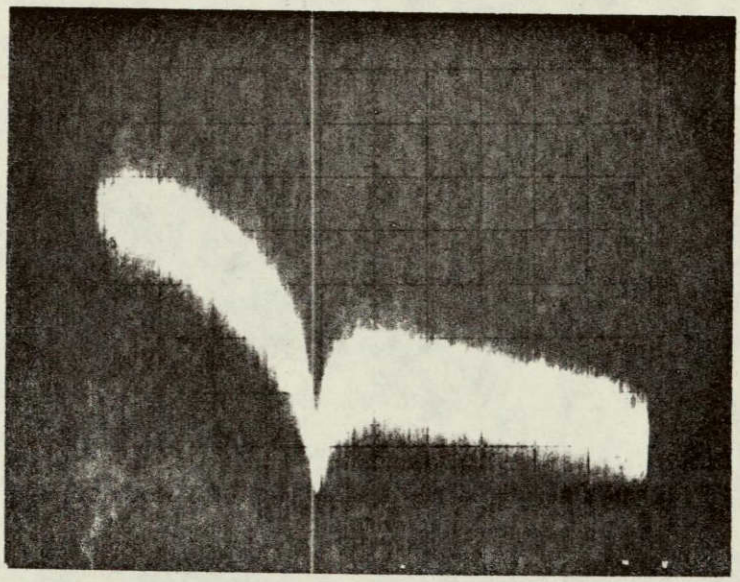
Spectrum Analyzer:
- 100 kHz/horizontal division
- Reference level = -20 dbm
- Bandwidth = 10 kHz
- Horizontal Scan Rate = 0.1 sec/division

Optical Input:
- None

Image Dissector Camera:
- Not Scanned, Spectrum Analysis at a Single Point

(a) Camera Noise Spectrum For No Optical Input

Figure 3-10. Noise Spectrum Analysis of Image Dissector Camera Output in the Test Configuration of Fig. 3-8.

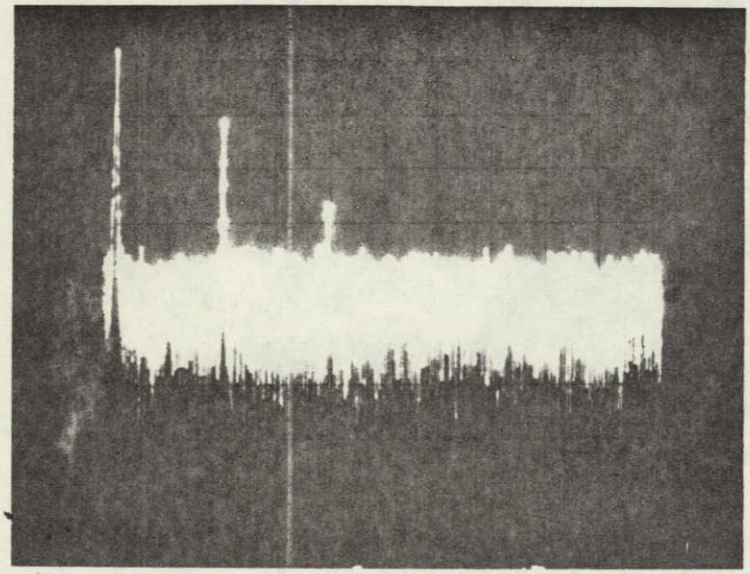


Spectrum Analyzer:
5 MHz/horizontal division
Reference Level = -20 dbm
Bandwidth = 30 kHz
Horizontal Scan Rate = 50 msec/division
Optical Input:
Unmodulated Laser Beam
Image Dissector Camera:
Not Scanned, Spectrum Analysis at a Single Point

(b) Camera Noise Spectrum With Optical Input

Figure 3-10. (Continued)

C-1



Spectrum analyzer:
50 kHz/horizontal division
Reference level = -20 dbm
Bandwidth = 1 kHz
Horizontal Scan Rate = 0.1 sec/division
Optical Input:
Reference Wave Modulated at 100 kHz
Electro-Optical Modulator Drive = 200 volts p-p
Image Dissector Camera:
Not Scanned, Spectrum Analysis of a Single Point

Figure 3-11. Spectrum Analysis of Camera Output For A 100 kHz Heterodyne Frequency in the Test Configuration of Fig. 3-8.

later in Section 3.3.3.1.

In all experiments using a spectrum analyzer the camera was not scanned either horizontally or vertically. Only extremely slow scan rates were usable with the heterodyne detectors investigated and, as a consequence, the modulated signals were very narrow band and not significantly different than the unmodulated waveforms shown in Fig. 3.10.

3.3.3 Heterodyne Detection of the Camera Output. As seen in the previous section, phase modulation of the reference wave creates a spectrum of harmonics of the modulation frequency. This is in accord with the theory of Section 3.2 which predicts an infinite number of harmonics each of which is, in principle, capable of being used to create a three-dimensional hologram. The current research program is not yet sufficiently advanced to demonstrate the actual recording of a complex hologram; however, heterodyne detection of interference patterns has been demonstrated and the effects of various sytem parameters have been investigated.

Commercial instruments capable of performing heterodyne detection are called lock-in amplifiers and have been used in electro-optic instrumentation. A block diagram of a lock-in amplifier is shown in Fig. 3.12. The major subsystems are a mixer (which may be preceeded by a bandpass filter), a low pass filter following the mixer to remove unwanted signals, and a local oscillator. The modulation (heterodyne) signal serves as the local oscillator for the

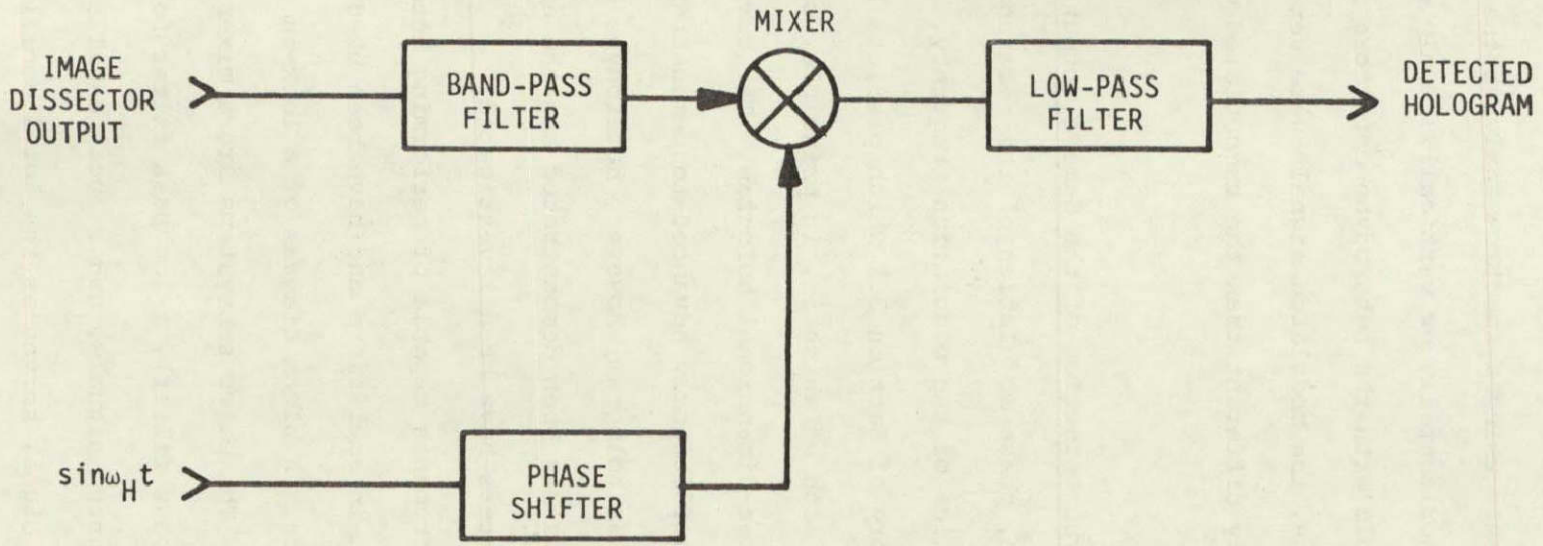


Figure 3-12. Schematic Diagram of Lock-In Amplifier (Phase Sensitive Detector)

detection of phase modulated holograms. A phase shifter is used to maximize the amplitude of the detected signal. Newer lock-in amplifiers have eliminated the phase shifter and measure magnitude and phase directly. This is accomplished by using quandrature mixers (local oscillators 90 degrees out of phase) and vectorially combining their outputs to yield the signal magnitude. The phase may be similarily derived.

In general, lock-in amplifiers can be used only at reference (heterodyne) frequencies less than 1 MHz. This immediately precludes use of such instruments for real-time holography (the heterodyne frequency must be at least 5 MHz to permit adequate signal bandwidth). The only lock-in amplifier which can operate above 1 MHz has such a small maximum signal bandwidth (100 Hz) that it is completely unsuitable for hologram acquisition. The technical specfications of some commercially available lock-in amplifiers are tabulated in Appendix 3.1. Because of the lack of suitable commercial heterodyne detectors a detector capable of operating in the frequency range 5-20 MHz with signal bandwidths up to 5 MHz is under development.

3.3.3.1 Detecting interference patterns with a PAR HR-8. The HR-8 is a commercial lock-in amplifier manufactured by the Princeton Applied Research Corporation. It can be operated at a maximum heterodyne frequency of 150 kHz with a maximum signal bandwidth of 10 kHz. The resulting performance is too restrictive for the

Figure 3-13. Interference Patterns Recorded With A PAR HR-8
In The Test Configuration of Figure 3-8 (f_c =100 kHz)

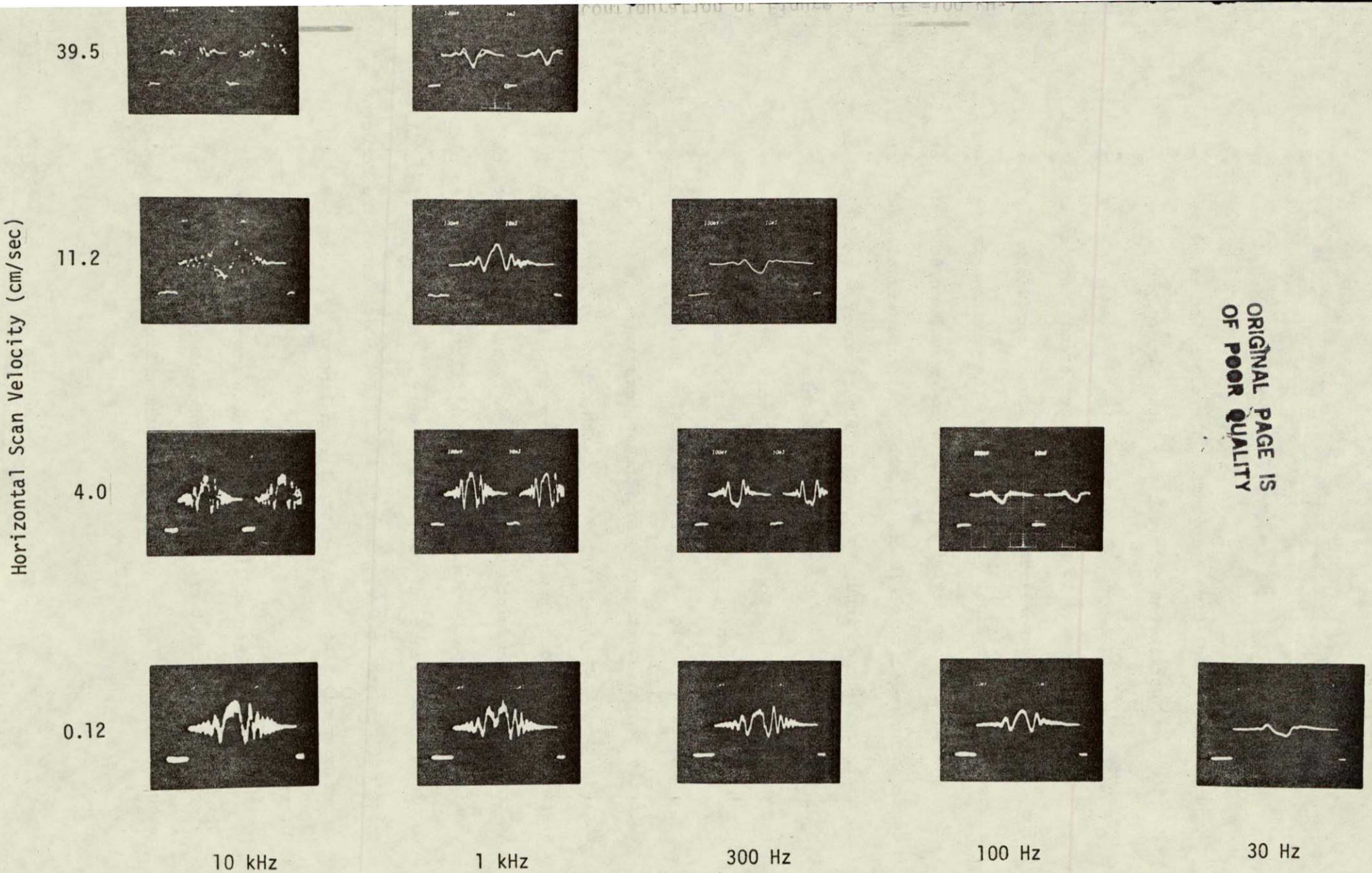


Figure 3-14. Single Line Scans of Interference Patterns Detected By A PAR HR-8 Lock-In In The Test Configuration Of Figure 3-8. (f_H=100 kHz)

acquisition of real-time holograms. The capabilities of the HR-8 do, however, permit the examination of the heterodyne holography concept.

The HR-8 was used to record the interference pattern of Fig. 3.9 for a variety of camera scan rates and signal bandwidths. The results are shown in Figs. 3.13 and 3.14. The phase shifter of the HR-8 was adjusted to maximize the detected signal/noise ratio for a camera scan velocity of 12 cm/sec and a detector signal bandwidth of 10 kHz. The signal input to the CRT film recorder was adjusted to 1 volt p-p to keep the beam intensity within the linear range of the CRT (H-P 1333A). No further adjustments were made as the camera recorder scan velocity and HR-8 bandwidth were varied.

Referring to Fig. 3.13, it can be seen that as the camera scan velocity decreases, the spot brightness increases. This results in the recorded film being overexposed with attending loss of detail. A similar result occurs when the detector bandwidth is decreased. As the detector bandwidth decreases, high frequency components of the interference pattern are lost through filtering and the resulting recorded interference pattern appears smeared, as shown in Fig. 3.13. These effects are more apparent in Fig. 3.14, which shows the detector output corresponding to the central scan line of the recorded interference pattern.

The HR-8 lock-in amplifier was used to compare heterodyne detection at the first and second harmonics of the modulation frequency. From (3. 7) the expressions for the first and second harmoic

signals in an in-line geometry are, respectively,

$$S_1 = -2\,RJ_1(\delta) \sum_i \sin \Omega_i x \qquad (3.24)$$

and

$$S_2 = -2\,RJ_2(\delta) \sum_i \sin \Omega_i x \quad , \qquad (3.25)$$

where the reference wave amplitude R is assumed to be constant. Neglecting the spectrum of the scene, i.e., the summation over i, the first and second harmonic signal amplitudes are simply related to the circular Bessel functions $J_1(\delta)$ and $J_2(\delta)$. The ratio will depend upon the value of the modulation index δ. The values of $J_1(\delta)$ and $J_2(\delta)$ are plotted on a relative scale in Fig. 3.15. The first harmonic is more interesting from an engineering viewpoint because it provides a greater S/N (signal-to-noise ratio) for a given modulation index.

Results for the experimental configuration of Fig. 3.8 are presented in Fig. 3.16. The camera was scanned across a single horizontal line (at the center of the camera apeture) and the peak signal recorded. Comparing Figs. 3.15 and 3.16, it can be seen that the behavior of the detected first harmonic agrees reasonably well with its predicted behavior; however, there is significant disagreement between the theoretical and experimental behavior of the second harmonic term. This is attributed to the upper 3 db point of the lock-in amplifier being the same as the heterodyne frequency used for these experiments--150 kHz .

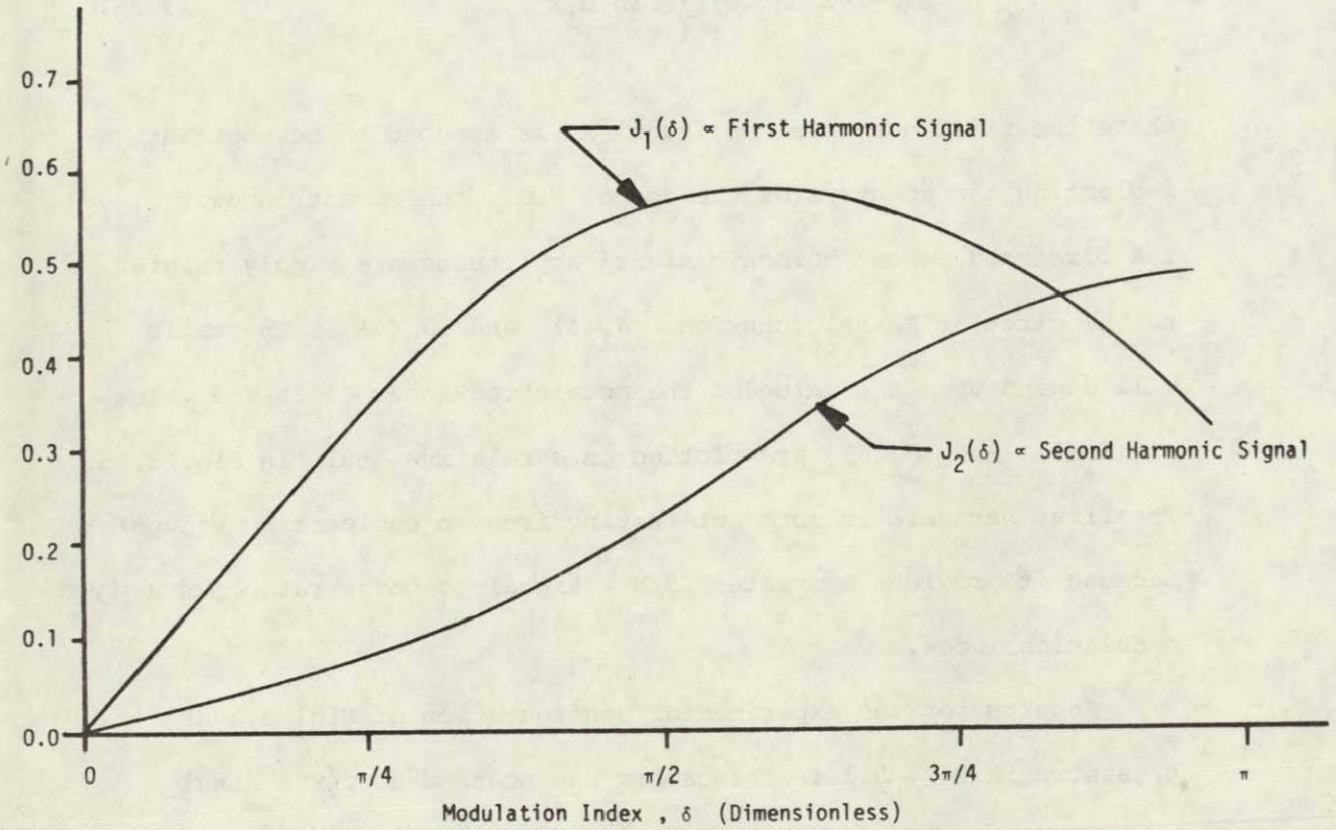


Figure 3-15. J_1 and J_2 Vs. Modulation Depth δ

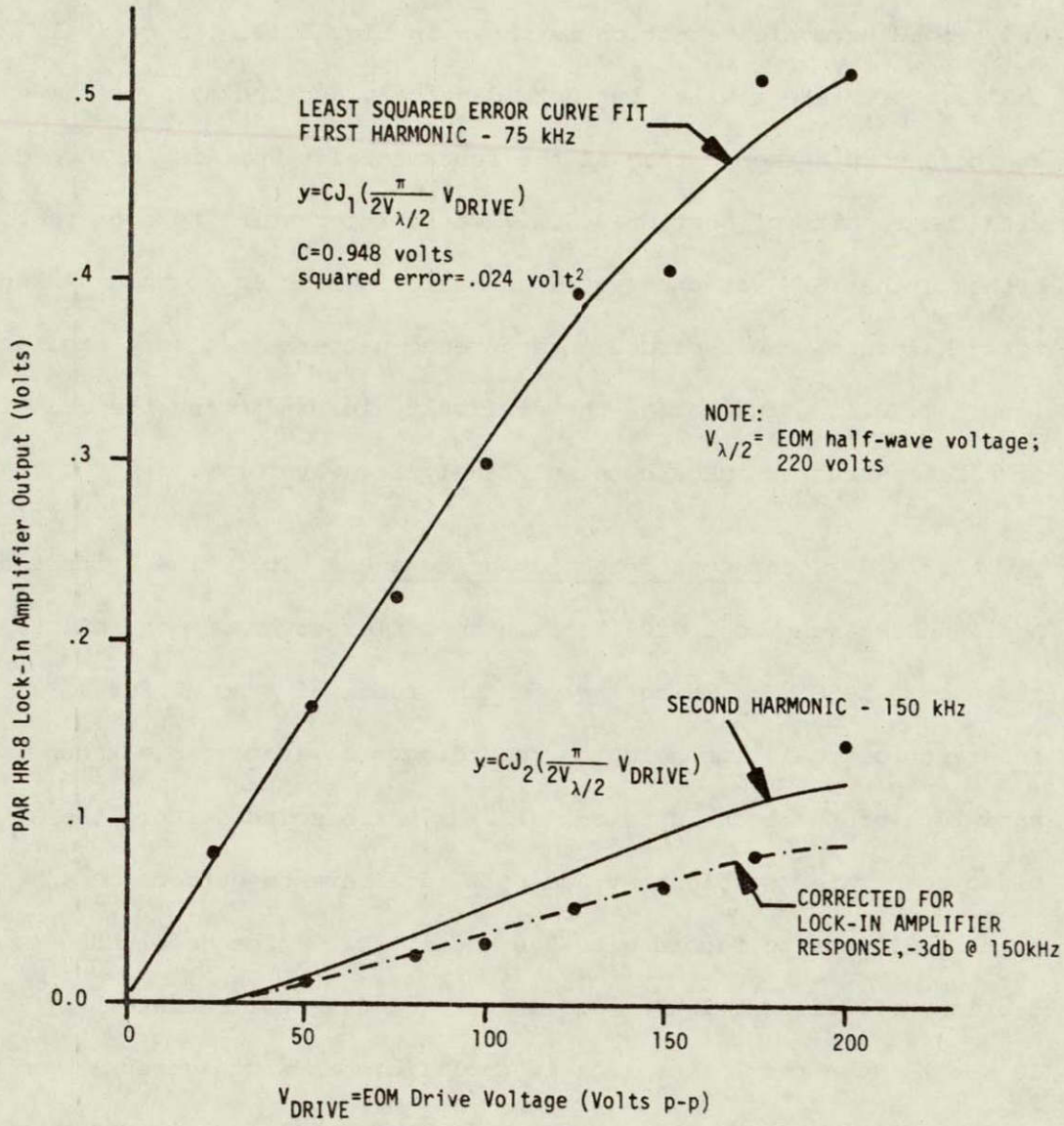


Figure 3-16. First and Second Harmonic Signal Amplitudes Vs. EOM Drive Voltage, f_H=75 kHz.

A direct comparison of the heterodyne detector output for first and second harmonic detection is shown in Fig. 3.17. In general, the waveforms are similar but not identical, and the S/N is lower at the second harmonic than at the fundamental. This is in accord with the results of Section 3.3.2. It is interesting to note that although the S/N at the second harmonic is much lower than at the first harmonic, the recorded interference patterns are very similar (see Fig. 3.11), indicating the difficulty in predicting the quality of a reconstructed image by simply analyzing waveforms.

3.3.3.2 Heterodyne detection using a PAR 5202. The Princeton Applied Research Model 5202 lock-in amplifier covers an operating range of 0.1-50 MHz, which includes the range of frequencies of interest for real-time hologram recording. However, the maximum bandwidth of the lock-in is only 100 Hz which so restricted the video scan rates usable that a single interference pattern took over 10 minutes to record with the Model 5202. (The Model HR-8 of Section 3.3.3.1 took 10-30 seconds using a detector bandwidth of 10 kHz.) As a result the lock-in amplifier bandwidth versus scan rate performance was not examined. Instead, this lock-in was used to examine the detected interference pattern as a function of heterodyne frequency. Results for heterodyne frequencies up to 5 MHz are reported in Fig. 3.18. In general, the detected interference pattern did not change significantly except for a frequency dependent d.c. offset in the lock-in output. This d.c. offset was nulled

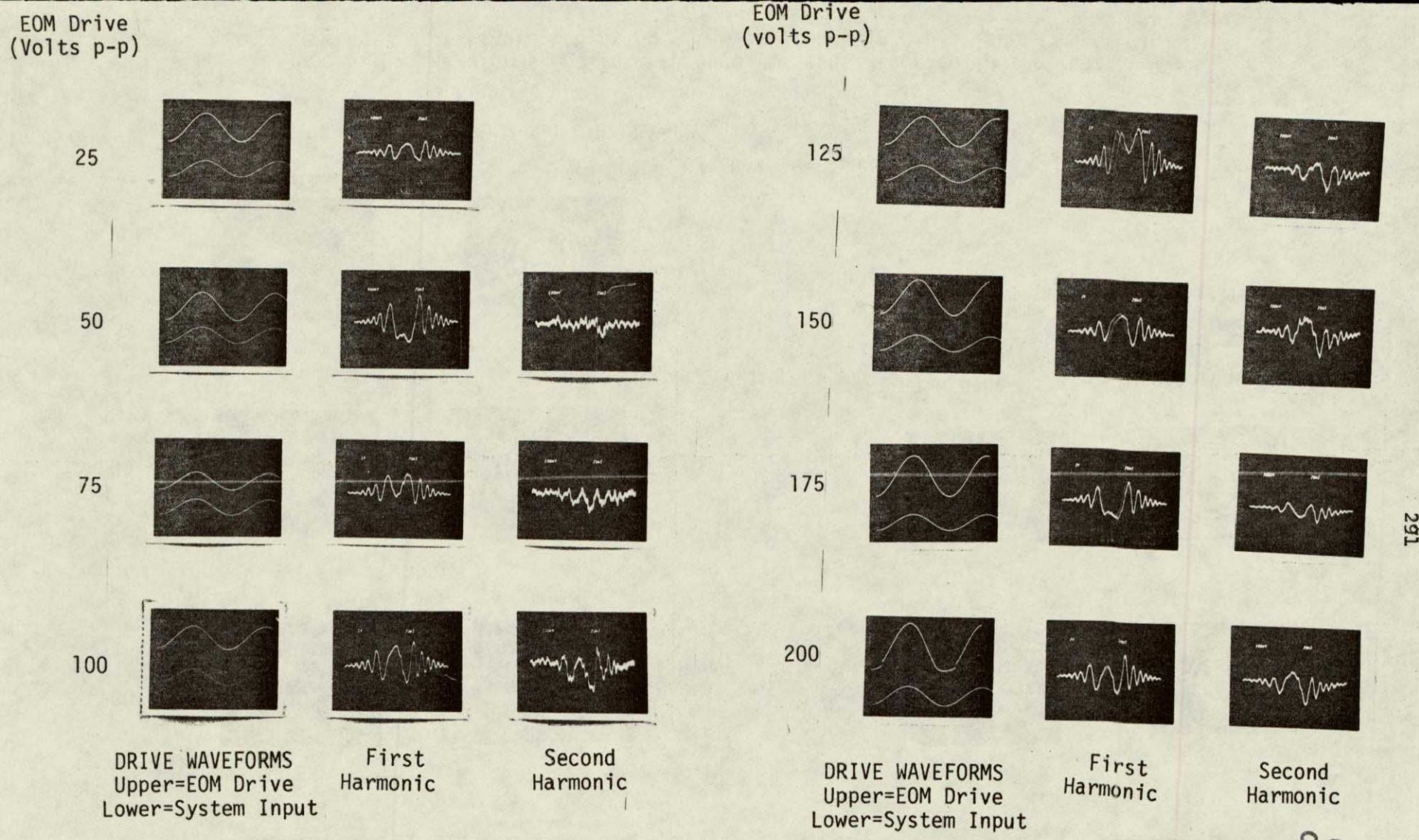


Figure 3-17. Single Line Scans of Interference Patterns For First And Second Harmonic Detection Using a PAR HR-8 Lock-In Amplifier (f_H=75 kHz).

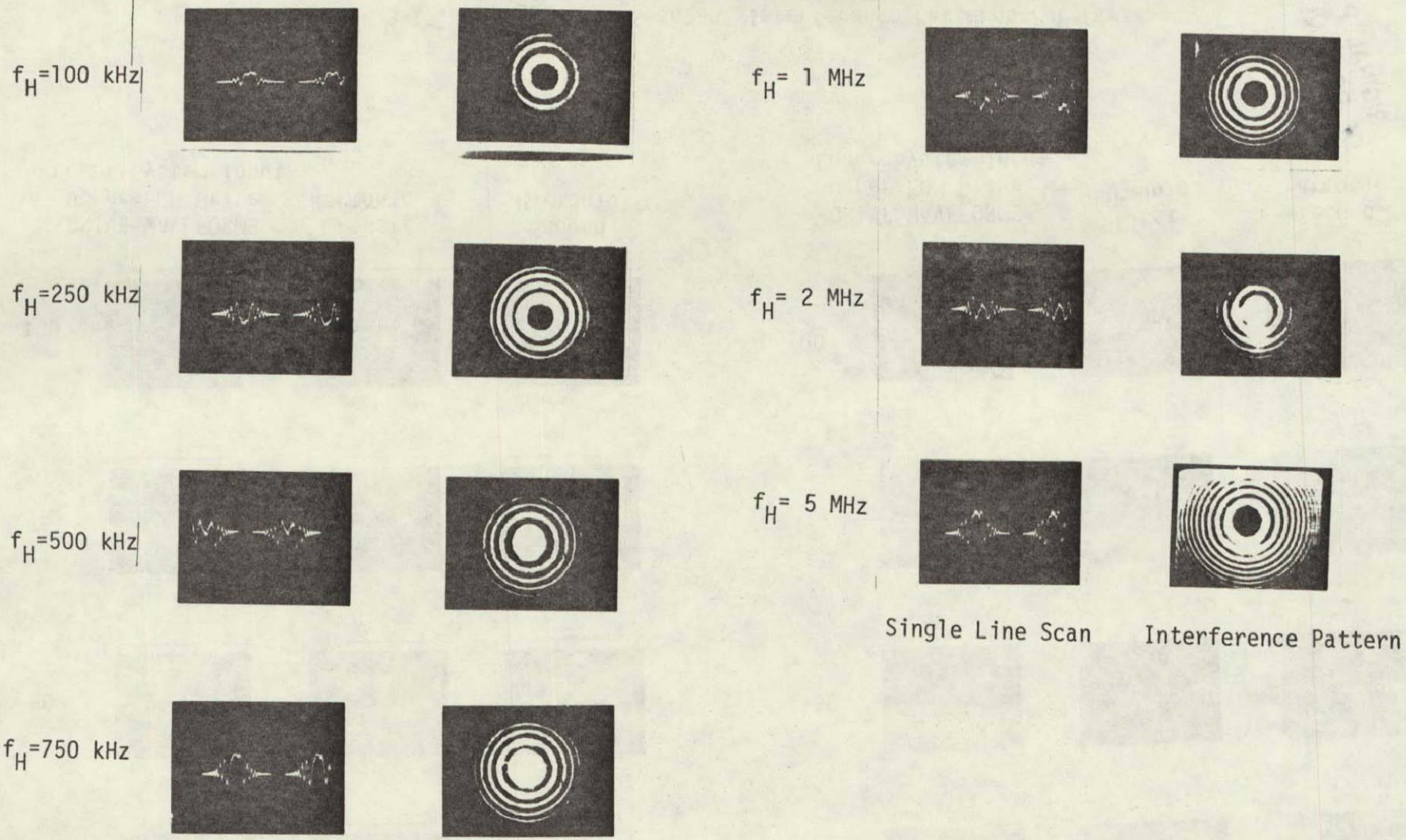


Figure 3-18. Waveforms And Interference Patterns Recorded In the Test System of Figure 3.8 Using A PAR 5202 Lock-In Amplifier

out and the a.c. waveform recorded to produce Fig. 3.18.

The uniformity of the detected interference patterns for heterodyne frequencies up to 5 MHz is in accord with the noise spectral analysis of Section 3.3.2. The more interesting heterodyne frequencies above 10 MHz, where the system noise is decreasing, were not measured due to frequency limitations of the electro-optic modulator drive electronics.

3.4 Summary and Remarks

A theory of electronic recording of optical holograms that is compatable with existing television technology has been developed and preliminary experimental evaluations have been performed. This concept, known as electronic heterodyne holography, utilizes phase modulation of the hologram reference wave to produce a time-dependent holographic interference pattern. This interference pattern is created in an in-line (Gabor) geometry so as to place the image terms within the resolution capabilities of the camera. Creating a hologram in this manner results in spatially overlapping self- and cross-interference terms; however, these terms are separable in the frequency domain because of the phase modulation. A non-integrating camera and heterodyne detection may be used to select only the cross-interference term which may be electronically processed and converted back into an optical image by an appropriate display device.

Experimental verification of electronic heterodyne holography

has been undertaken. A ITT Image Dissector camera has been used with commercial lock-in amplifiers to record simple interference patterns in typical hologram recording geometries. Detection of first and second harmonic signals was done to provide confirmation of the separation of self- and cross-interference terms via phase modulation of the spatial reference wave.

This experimental work will be continued to the actual recording of a hologram of a three-dimensional solid object in the geometry of Fig. 3.1(b). This experiment is currently being assembled and results are expected within several months. Concurrently, a specialized instrument for real-time acquisition of holograms is under development (Appendix II).

The possibility of real-time recording of holograms will be the basis for additional theoretical work. In particular, two avenues of research are anticipated: One, electronic processing of recorded holograms; and, two, real-time holographic display of recorded holograms. The electronic processing of holograms will concentrate upon the synthesis of wide-perspective holograms from several narrower perspective electronically recorded holograms. Recent developments in spatial light modulators make the real-time display of holograms a definite possibility. Commercially available spatial light modulators will be examined with regard to their potential use as real-time displays for electronically recorded holograms.

In conclusion, electronic heterodyne holography appears to be a viable technique offering unique opportunities for electronic processing and display of three-dimensional images in a television-like format.

References

1. For a detailed discussion of conventional holography see, e.g., Goodman, J. W., Introduction to Fourier Optics, McGraw-Hill Book Co., New York (1968).

2. Enloe, L. H., J. A. Murphy, and C. B. Rubenstein, "Hologram Transmission Via Television," Bell System Tech. J. 45, 335 (1966).

3. See, e.g., Goodman, J. W., op. cit., pp. 48-54.

Appendix 3.1

EQUIPMENT SPECIFICATIONS

A3.1.1 Image Dissector Camera

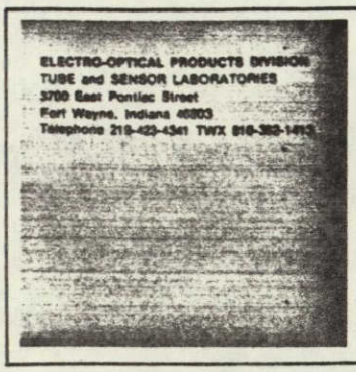
The Image Dissector camera used in the hetrodyne holography experiments reported in Chapter 3 is a type F5005 manufactured by ITT Electro-Optical Products Division. The F5005 camera uses a F4011 magnetically focused, magnetically deflected photomultiplier tube having a S20 spectral response. The F4011 tube is essentially a X-Y scannable photomultiplier tube with a 1.0 inch diameter photocathode.

The anode photocurrent is converted into an output voltage by an internal amplifier with a bandwidth of 250 kHz. For hetrodyne holography applications this integral amplifier was replaced by a wide-bandwidth amplifier. It is the response of this amplifier (-4db @ 10 MHz) that limits the camera's overall frequency response as the F4011 tube is usuable to approximately 25 MHz.

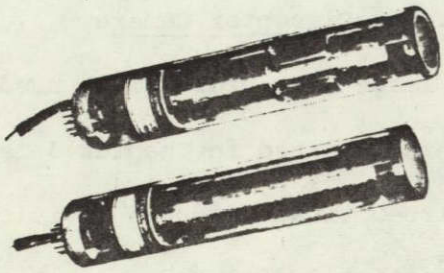
The excellent high frequency response of this tube combined with the wide bandwidth video amplifier allow the camera to be used at hetrodyne frequencies greater than 5 MHz, a prerequisite for real-time recording of holograms (using NTSC scan formats and rates). The spatial resolution of the F4011 is extremely good (-3db @ 40 line pairs/mm) and is usable to 70 line pairs/mm.

The manufacturer's specifications for a typical F4011/F5005 are reproduced in Table A3.1.

Table A3.1 SPECIFICATION OF ITT F4011 IMAGE DISSECTOR TUBE



F4011/F4011RP



VIDISSECTOR®
IMAGE DISSECTOR

- High Resolution
  65–75 Lp/mm Limiting
- High Photocathode Quantum Efficiency
- Non-Storage
- Low Dark Current
  Typically 10^{-10} Amperes at
  5×10^5 Gain
- Wide Dynamic Range
  10^{-9} Amperes
  $> 10^{-5}$ Amperes
- Low Power Requirements
- Rugged Construction
- Electron Counting Capability

GENERAL DESCRIPTION

The F4011 and F4011RP are 1-1/2 inch diameter, magnetically focused, magnetically deflected image dissectors. These image dissectors are available with a wide variety of aperture shapes and sizes having dimensions from 0.0005 inch to 0.30 inches. Photocathodes of the S1, S11, S20, and S25 types can be provided. Each tube is supplied with an individually measured absolute spectral response curve.

The F4011 RP is used in applications which require very low dark rates as in pulse counting, or whenever faceplates other than clear glass are required such as fiber optics, quartz, or MgF_2.

The salient features of the Vidissector image dissector are its inherently high resolution, determined primarily by the size and shape of the aperture; nonstorage, allowing random or variable scan rates without changes in the signal amplitude, reliable operation because of simple rugged construction and lack of a thermionic cathode. The Vidissector camera tube also has a linear dynamic range of several orders of magnitude, and a Poisson–like pulse height distribution in the single photoelectron counting mode.

F4011/F4011RP 9–70

ELECTRO-OPTICAL PRODUCTS DIVISION ITT

Table A3.1 (continued)

MECHANICAL CHARACTERISTICS

Aperture Size
- Standard (Note 1) ....0.001 Inch ± 0.0001 Inch Round
- Minimum ..... 0.0005 Inch
- Maximum (Note 2) ..... 0.300 Inch

Faceplate ..... Flat, Surfaces Parallel ± 0.001 Inch
- Material (Note 3) .....Borosilicate Glass, Corning 7056 or Equivalent
- Thickness
  - F4011 .....0.080 ± 0.005 Inch
  - F4011RP .....0.125 ± 0.005 Inch

Physical Dimensions
- Overall Length ..... 8.20 Inch
- Bulb Diameter .....1.500 Inch Max. OD
- Maximum Diameter (Note 4)
  - F4011 ..... 1.54 Inch
  - F4011RP ..... 1.56 Inch
- Weight (Approximate) .....5.5 Ounces
- Base ..... 14 Pin – See Figure
- Base Connector (Note 5) ..... ITT – 4711619 (Teflon) Burroughs – SK112 Mica-phenolic
- Operating Position ..... Any

TYPICAL OPERATING CONDITIONS
(Voltages With Respect to Drift Tube)

Photocathode .....–600 Volts
Dynode 1 (Notes 13, 14) .....0 to –40 Volts
Dynode 2 (Note 14) ..... 0 to +140 Volts
Anode (Note 16) ..... 1400 Volts
Anode with Respect to
- Dynode 10 (Note 15) ..... +30 to +200 Volts

Focus field strength (Note 17) .....40 Gauss

GENERAL CHARACTERISTICS

Photocathode .....Semitransparent
- Spectral Response (Note 6)
  - F4011 .....S11
  - F4011RP ..... S20 (High Conductivity)
- Diameter .....1.03 ± 0.03 Inch
- Quality Diameter (Note 7) 0.825

Aperture Collection Efficiency (Approximate) (Note 8) . 65%
Focusing Method .....Magnetic
Deflection Method .....Magnetic

Multiplier
- Structure ..... Box and Grid
- Stages (Note 9) 10
- Internal Divider
  - Resistors (Note 10) .....7 – 2.5 Megohm 1/8 Watt, 1%
- Material .....Ag–Mg

Interelectrode Capacitance
- Anode in all Electrodes ..... 2.5 pF
- Anode to Dynode 10 ..... 1.4 pF

MAXIMUM RATINGS (ABSOLUTE MAXIMUM VALUES)

Average Photocathode current density (Note 11) ..... –
Peak anode current (Note 12) .....0.5 mA
Average anode current (Note 12) .....0.3 mA
Photocathode to anode voltage .....3000 Volts
Drift tube to photocathode .....1000 Volts
Drift tube to dynode 1 ..... ± 100 Volts
Between any pair of dynodes .....250 Volts
Dynode 10 to anode .....500 Volts
Temperature .....70° C

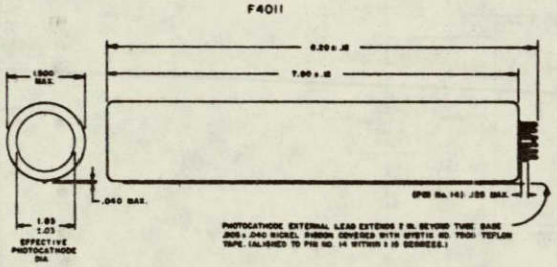


Figure 1a

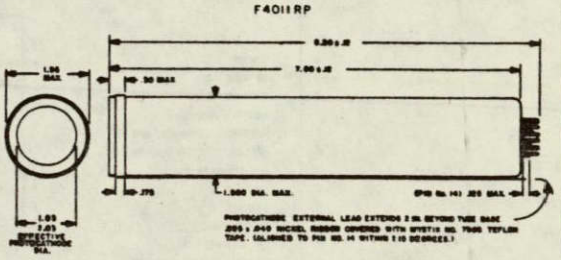


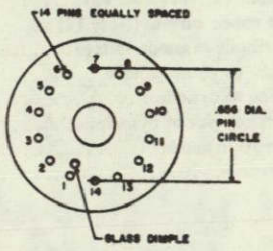
Figure 1b

Table A3.1 (continued)

PERFORMANCE CHARACTERISTICS AT 5×10^5 GAIN FOR A 0.001 INCH APERTURE TUBE (NOTE 18)

	NOTES	MINIMUM	TYPICAL	MAXIMUM
Electron multiplier voltage required for specified gain	19	1000	1400	2000 Volts
Dark current at specified gain		–	10^{-10}	5×10^{-9} Amperes
Multiplier bandwidth (–3 db)	20	–	22 MHz	–
Noise factor			–	4.0
Photocathode luminous sensitivity	21, 22			
S-11		30	40 μA/lumen	–
S-20 (high conductivity)		120	150 μA/lumen	–
Photocathode radiant sensitivity	22			
S-11 at 440 nm		–	32 mA/Watt	–
S-20 (high conductivity) at 420 nm		–	55 mA/Watt	–
Resolution (Percent Modulation)	23			
1000 TVL/inch center		–	60	–
1000 TVL/inch edge		–	40	–
1600 TVL/inch center		–	20	–
1600 TVL/inch edge		–	10	–
Uniformity	7, 24			
Photocathode (quality diameter)			95 ± 5%	
Output (quality diameter)	13	85 ± 15%	90 ± 10%	–

F4011, F4011RP



PIN	ELEMENT
1	ANODE
2	DYNODE 10
3	DYNODE 9
4	DRIFT TUBE
5	INTERNAL CONNECTION
6	INTERNAL CONNECTION
7	NO CONNECTION
8	DYNODE 1
9	DYNODE 2
10	DRIFT TUBE
11	NO CONNECTION
12	ANODE GUARD RING
13	NO CONNECTION
14	KEY PIN (CLIPPED)

FLYING LEAD - PHOTOCATHODE

Figure 2

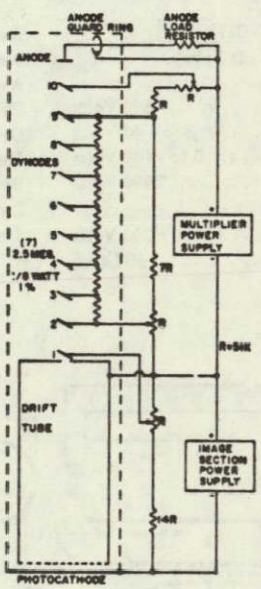


Figure 3

Table A3.1 (continued)

NOTES

1. The F4011 and F4011RP are available with aperture sizes and shapes varying within the dimensional limits of 0.0005 inch and 0.300 inch. Most round apertures are available in 0.001 inch increments up to 0.020 inch and 0.01 inch increments up to 0.100 inch. One time artwork and tooling costs may be involved if specialized sizes or shapes are required.

2. For aperture sizes greater than 0.060 inch the multiplier output may vary as much as ± 25% when a 0.001 inch spot of photoelectrons scans inside the aperture.

3. The F4011RP is also available with fiber optic, quartz and MgF_2 faceplates.

4. Includes the photocathode contact and flying lead.

5. A teflon socket, ITT P/N 4711619 is normally supplied with each tube. The Borroughs SK112 (modified) can also be supplied if requested.

6. The F4011 is also available with an S1 photocathode. The F4011RP is also available with an S25 photocathode. Use of MgF_2 or quartz faceplates and S20 or S25 photocathodes can provide as much as 20–30% Q.E. at 254 nm. For details, please consult ITT-ETD Tube and Sensor Laboratory.

7. This is a convenient diameter over which resolution, uniformity, and geometrical distortions will be specified.

8. This is the approximate transmission factor of the photoelectron accelerator mesh. Higher transmission meshes, up to 80 or 90%, can be provided in large aperture tubes with an accompanying loss in definition of the aperture edge.

9. Fewer number of dynodes can be supplied on special order. See Note 10.

10. Because of the limited number of pins in the tube base, it is necessary to include a portion of the electron multiplier voltage divider inside of the tube. The standard configuration is 7, 2.5 megohm, 1/8 watt carbon film resistors. A 9 stage electron multiplier can be provided without internal resistors.

11. The maximum recommended photocathode current densities averaged over the entire photocathode area for 1 second are:

S-1	1 $\mu A/cm^2$
S-11	3 $\mu A/cm^2$
S-20 (high conductivity)	5–10 $\mu A/cm^2$
S-25	5–10 $\mu A/cm^2$

12. For a maximum of 10% departure from linearity of output current vs input flux the dynode voltage divider has ratios of 1:1:1: . . . 1:1:5:3. The last two dynodes are bypassed or connected to power supplies. This limit is achievable only in tubes with a maximum of 4 internal resistors and all resistors located before dynode 6.

13. A negative potential on dynode 1 prevents secondary electrons formed inside the drift tube from entering the aperture and striking dynode 1. If allowed to enter the aperture and strike dynode 1, these secondaries appear at the anode as a non-zero signal in the black portions of the image.

14. Provision should be made to allow static adjustment of dynode 1 and 2 potentials over the range indicated in order to minimize the output shading.

15. Adjusted for maximum multiplier gain. In general, lower dynode 10 voltages favor increased multiplier gain. The limit in dynode 10 voltage reduction is set by the linearity requirements at high signal currents.

16. For a nominal 5×10^5 gain.

17. First loop focus. Use of second loop focus (~ 80 Gauss) results in improved resolution off axis, reduced astigmatism, and better geometrical scan accuracy with increased power requirements.

18. Using ITT F4533 or F4534 Deflection Assembly.

19. Using dynode voltage divider shown.

20. By frequency spectrum analysis of the photocurrent shot noise at 100 volts/stage. The last three dynodes are bypassed by 0.05 μf. This measurement was made on tubes having two internal resistors between dynodes 4, 5 and 6.

21. For this test, the light incident upon and normal to the plane of the photocathode is 2854°K color temperature tungsten lamp radiation, generally 0.1 lumen.

	Minimum	Typical
S-1	12 μA/lumen	20 μA/lumen
S-25	150 μA/lumen	200 μA/lumen

22. Each F4011 and F4011RP sold by ITT is supplied with an individual measurement of photocathode sensitivity in mA/watt vs wavelength and μA/lumen, each traceable to the National Bureau of Standards.

23. Measured using a square wave bar chart.

24. The 100% region usually occurs in the central portion of the scanned area and the 70% occurs around the periphery. The curvature of the shading is usually of one sign. Output uniformity includes cathode uniformity.

The F5005 camera contains a F4011 tube with all necessary focusing and deflection electronics. Low level signals (±10 volts) are sufficient to scan the camera tube over its entire apeture. For the experiments described in Chapter 3 the camera was scanned over a non-interlaced grid of 256x256 picture elements. The appropriate scanning signals as well as blanking were digitally produced and applied to the camera control inputs via digital/analog converters. The conversion time of the presently used digital/analog converters limits the camera's recording speed to approximately ten 256x256 picture element holograms/second.

A3.1.2 The Hetrodyne Detector (Lock-In Amplifier)

Two hetrodyne detectors, or lock-in amplifiers, have been used to record simple interference patterns as described in Chapter 3. These particular lock-in amplifiers are the Princeton Applied Research Models 5202 and HR-8. To be usuable for NTSC format recording of holograms at television rates a lock-in amplifier would be required to have a frequency range of 5-15 MHz with a bandwidth of 4.5 MHz (0.22 micro second time constant). Such a lock-in amplifier is also desirable for reducing hologram recording time minimizing susceptibility to acoustic noise and mechanical vibrations. Referring to Table A3.2, a tabulation of the performance specifications of commercially available lock-in amplifiers, no lock-in amplifier meets these particular performance specifications. The Princeton Applied Research Model 5202 can operate at frequencies as high as 50 MHz but has a bandwidth of only 100 Hz (time constant = 0.01 second). This

Table A3.2 SPECIFICATIONS OF COMMERCIAL LOCK-IN AMPLIFIERS*

Company and Model	Input sensitivity range (V)	Input modes	Frequency range (Hz)	Ref. modes	Time-constant range (s)	Computer control	Price	Options	Special features
Keithley									
840	10^{-9}-1	+, −, differential, tuned, wideband	10-10^5	+, −, 2f, external phase	0.003-100	No	$1595	Bandpass prefilter, fine-notch filter	Frequency monitor
Brookdeal									
9503	10^{-9}-0.5	high- and low-pass filters	2-10^5	normal, 2f, internal	2.5×10^{-4}-100	No	$2395	Specialty preamps, ratiometer	Stability-resolution tradeoff, multiple correlation modes
9505	10^{-9}-0.5	normal, fundamental only, analog or digital correlation, high- and low-pass filters	0.2-2×10^5	normal, 2f, internal	2×10^{-4}-100	No	$5795	Preamps, filters, ratiometer, oscillators, autoranging, more	Stability-resolution tradeoff, transient suppression, 2-phase
North Coast									
854	10^{-9}-1	ac, dc, bandpass	0.5-5×10^4	ac/dc, f, 2f	0.1-100	Yes	$1695	Computer interfaces, 2:1 frequency-range cards	Complete programmability
Itheco									
395	10^{-9}-1	differential	10-10^4	10-300Hz, 0.3-10kHz	0.0025-8	No	$1695	Preamps, ratio computer	Heterodyne detection
391A	10^{-7}-1	normal, low drift, high dynamic range, "noise"	0.1-10^5	internal, external, 2f	1.25×10^{-4}-125	No	$2289	Frequency range plugins, ratio computer	Heterdyne, tunable oscillator, floating input
397EO	10^{-7}-1 V 100 pA-10 A I (current) 10 nA-1 mA I × 1000	voltage	10-10^5	normal	0.0025-25	Yes	$2495	Ratio computer	Heterodyne, 2-phase detection, continuous gain control, digital panel meter
393	10^{-7}-3	normal high Q, max stability, normal low Q, max noise rejection	0.1-2×10^{-5}	internal, external, 2f	1.25×10^{-3}-125	No	$3435	Ratio computer, noise measurement, phase measurement	Heterodyne, stability-resolution tradeoff
Princeton Applied									
5101	10^{-9}-0.25	normal	5-10^5	normal, 2f	0.001-30	No	$1375	Tuned signal channel, internal oscillator, rear BNCs	Output postfilter
128A	10^{-9}-0.25	flat, low pass, high pass, differential	0.5-10^5	normal, 2f	0.001-100	No	$1850	Tuned signal channel, internal oscillator, monitor output	Basic performance
5203	10^{-9}-0.25	flat, notch filter, input × 10, differential	0.5-10^5	internal, external, f, 2f	0.003-100	No	$2295	Ratio computer, tuned amplifier,	Heterodyne detection
5204	(same as for 5203, but with 2-phase detection)						$2995	Vector/noise measurement	2-phase detection
186A	10^{-7}-0.5	low pass filters, differential	5-10^5	f, 2f	0.03-30	Yes	$2950	Internal oscillator	Stability-resolution tradeoff, heterodyne detection, phase-sensitive detector with ac output
126	plugin preamp selectable: 10^{-7}-0.5 typical	high and low filter selectable	0.2-2.1×10^5	internal, external, 2f	0.001-300	No	$3830-$3910 (including preamp)	Selection of preamps	Stability-resolution tradeoff, selectable integrate mode
5202	10^{-7}-0.25	single ended	$10^{-5} \times 10^7$	signal-type select; trigger-slope select	0.01 0.1 1 10	No	$4995	Vector phase, ratio computer	High frequency range, 2-phase detection
124A	preamp selectable	flat, notch, high pass low pass, bandpass	2-2.1×10^5	internal, external, 2f	0.001-300	Yes	$5035-$5225 (including preamp)	Selection of preamps	Stability-resolution tradeoff, tunable oscillator, tunable bandpass filter

*Reiser, Chris, "Trade off with lockins," Laser Focus, October 1978, p. 68.

instrument was used to record simple interference patterns with the results of Chapter 3 and represents the highest frequency lock-in amplifier commercially available. A complete list of its performance specifications may be found in Table A3.3.

The Princeton Applied Research Model HR-8 is no longer commercially available but has the widest bandwidth available (10 kHz with time constant=OFF). Among the lock-in amplifiers tabulated in Table A3.2 only the Ithaco 391A has a comparable bandwidth (8 kHz). The complete specifications of the Model HR-8 are presented in Table A3.4.

Table A3.3 SPECIFICATIONS OF PRINCETON APPLIED RESEARCH MODEL 5202 LOCK-IN AMPLIFIER

SIGNAL CHANNEL

FREQUENCY RESPONSE: 100 kHz to 50 MHz

GAIN BANDWIDTH LINEARITY: Flat, from 300 kHz to 10 MHz, to within ±0.5 dB

SENSITIVITY: 8 full-scale ranges from 100 μV to 250 mV in 1-2.5-10 sequence. Two output expansion ranges of X1 and X10 increase the overall sensitivity to 10 μV full scale.

INPUT: Single-ended, with auxiliary ground lug

INPUT IMPEDANCE: 50 Ω, VSWR <1.2

MAXIMUM ALLOWABLE INPUT SIGNAL: 5 V rms or 10,000X full scale (whichever is less)

MAXIMUM INPUT BEFORE OVERLOAD: 200X full scale; expandable to 2000X full scale

INTERNAL NOISE: Less than 10 nV/Hz$^{1/2}$; 100 kHz to 50 MHz

COHERENT PICKUP: Less than 5% of full scale worst case (50 MHz on the most sensitive range)

GAIN STABILITY: Better than 0.2%/ °C

REFERENCE CHANNEL

FREQUENCY RANGE: 100 kHz - 50 MHz in 9 overlapping ranges, selectable with front-panel switch.

INPUT REQUIRED: The reference channel locks to virtually any external voltage having amplitude excursions of at least 300 mV pk-pk. Front-panel reference and slope pushbutton controls enable phase lock to optimum point of the reference waveform. The front-panel REFERENCE UNLOCK lamp indicates the absence of a proper reference input.

REFERENCE INPUT IMPEDANCE: 50 Ω (nominal)

MAXIMUM INPUT LEVEL: 5 V peak

PHASE ADJUSTMENT: A calibrated ten-turn potentiometer provides 0 - 100° phase shift. The accuracy of the phase shift is ±5° with a resolution of ±0.1°. A four-position Quadrant switch provides 90° phase shift increments accurate to 5°. NOTE: Overall phase accuracy of instrument is ±15°.

PHASE NOISE: Less than 0.035° pk-pk (100 kHz to 50 MHz; 10 ms time constant)

REFERENCE ACQUISITION TIME: 0.1 s max.

PHASE-SENSITIVE DETECTORS

DESCRIPTION: The Model 5202 features two fully-independent Phase-Sensitive Detectors (PSD's) driven by orthogonal reference signals. Each PSD is provided with its own ZERO OFFSET, OUTPUT EXPAND, and TIME CONSTANT controls, allowing each to be independently optimized for the signal undergoing analysis. Wide variations between in-phase and quadrature signals can therefore be readily measured.

DYNAMIC RESERVE: Defined as the ratio, at the input of the Model 5202, of the maximum peak signal (non-coherent and outside the passband) that can be applied without overload, to the peak coherent signal required for full-scale output. The OUTPUT EXPAND switch permits output stability to be traded for overload capability, as indicated in Table II-1.

OUTPUT EXPAND SETTING	OUTPUT STABILITY (%/ °C of Output f.s.)	DYNAMIC RESERVE
X1	0.05	200X FS
X10	0.50	2000X FS

NOTE: FS = full-scale sensitivity setting divided by the output expand setting.

Table II-1. DYNAMIC RESERVE AND OUTPUT STABILITY AS A FUNCTION OF OUTPUT EXPANSION

FILTER TIME CONSTANTS: The two outputs are provided with switch-selectable choices of four time constants, 10 ms, 100 ms, 1 s, and 10 s, plus a MIN. position in which the time constant is less than 1 ms. An additional dc prefilter switch inserts a 250 ms filter after the main Time Constant filter.

DC ZERO OFFSET: Calibrated 10-turn potentiometer is provided for each channel permitting up to ±10 times full scale to be suppressed. Suppression polarity selected by front-panel pushbuttons.

OUTPUTS

METER READOUT: Two meters are provided, one for each channel. They are calibrated to provide full-scale deflection with a properly phased full-scale signal at the input. The left meter can be switched to monitor the in-phase signal, or, if the Vector Phase option has been installed, the vector magnitude. The right meter monitors either the amplitude of the quadrature signal or the phase of the input signal with respect to the applied reference (Vector phase option installed). Either meter can monitor the amplitude of a dc signal (externally derived or output of Ratio option, if installed) applied to a rear-panel connector. External Meter mode sensitivity is 1 V f.s. (100 μA movement through 10 kΩ).

RECORDER OUTPUT: Front and rear-panel I and Q OUT connectors are provided to interface to standard recorders. Output is 1 V f.s. through 600 Ω*.

*Approximately 8 kΩ in early units.

Table A3.3 (continued)

RATIO OUTPUTS: Rear-panel BNC connector outputs are also provided for the Vector Phase and Ratio Options as described under OPTIONS.

ACCESSORY INTERFACE: A rear-panel card-edge connector allows peripheral instrumentation to be powered from the Model 5202. +15 V, −15 V, and ground are provided.

GENERAL

INDICATIONS: Six front-panel indicator lights define the operating states of the lock-in amplifier.

(1) OVERLOAD: Indicates that an overload condition exists in one or more of the critical amplifier circuits.

(2) UNLOCK: Indicates lack of an adequate external reference signal as defined in the reference specifications, or that the frequency range setting is incorrect.

(3) OUTPUT EXPAND: Indicates that the input sensitivity is increased by a factor of ten. One indicator is provided for each output channel.

(4) NEGATIVE PHASE: In units equipped with Vector option, indicates that Input Signal lags Reference Signal (Phase controls to 0°) by angle in range of 0° to −180°.

(5) ERROR: Indicator lights if vector magnitude and/or phase buttons are depressed and any of the following conditions exist.

(a) In-phase and quadrature time constants are not equal.

(b) In-phase and quadrature output expansions are not equal.

(c) All Time Constant pushbuttons released (gives time constant of nominally 1 ms).

(d) Output Offset in use.

(e) Vector option board not installed.

AMBIENT TEMPERATURE RANGE: The instrument can be operated at temperatures ranging from 15°C to 45°C.

AUXILIARY POWER OUTPUT: A rear-panel connector provides ±15 V (100 mA) and ground.

POWER REQUIREMENTS: 100 to 130 or 210 to 260 V ac, 50 to 60 Hz; 50 watts.

SIZE: 17-1/2" W x 5-1/2" H x 19-1/2" D (44.5 cm W x 13.9 cm H x 49.5 cm D).

WEIGHT: 35 lbs (15.89 kg).

OPTIONS

MODEL 5202/95 VECTOR PHASE OPTION: Direct meter readout of the computed magnitude and phase angle of the input signal with respect to the reference input. Full continuous 360° phase measurement is accomplished by means of a front-panel meter and a negative phase indicator lamp. Rear-panel MAGNITUDE and PHASE output BNC connectors are provided, allowing convenient monitoring or recording. Vector Phase specifications follow.

(1) PHASE ANGLE OUTPUT VOLTAGE: 1.8 V ahead of 600 Ω for 180°; Linearity ±0.2°; accuracy ±0.2°; Transfer function of 10 mV/°.

(2) MAGNITUDE OUTPUT VOLTAGE: 1 V f.s. ahead of 600 Ω; Linearity ±0.1%; Accuracy ±1%.

MODEL 5202/96 RATIO OPTION: Option operates on dc levels (A & B) applied to rear-panel connectors and computes A/B, log A, or log A/B, as selected with a rear-panel toggle switch. Applied inputs can be I and Q outputs. Computed function is provided at rear-panel Ratio OUT connector. Ratio can also be indicated on front panel meter by making use of the EXTERNAL METER Input capability. Ratio specifications follow.

(1) Input Voltage Range: 10 mV - 1 V

(2) Input Offset (maximum): ±250 μV

(3) Input Offset Temperature Coefficients: ±15 μV/°C

(4) Output Voltage: LINEAR, +1 f.s. (unity); LOG, 0.5 V/decade with +0.5 V of offset.

(5) Log Range: 3 decades

(6) Ratio Accuracy: A function of the denominator voltage as follows. For A/B, ±0.4% from B = 0.1 V to B = 1 V; ±4% from B = 0.01 V to B = 0.1 V. For Log A, computed function is within 2 mV of correct value. For Log A/B, computed function is within 2 mV from B = 0.1 V to B = 1 V; computed function is within 10 mV from B = 0.01 V to B = 0.1 V.

ACCESSORIES

MODEL 115 HIGH FREQUENCY PREAMPLIFIER: Refer to P.A.R.C. literature T220D and TN115 for complete specifications on the Model 115 preamplifier.

Table A3.4 SPECIFICATIONS OF PRINCETON APPLIED RESEARCH MODEL HR-8 LOCK-IN AMPLIFIER

INTRODUCTION:

The PAR Model HR-8 Precision Lock-In Amplifier is essentially a detection system capable of operating with an extremely narrow equivalent noise bandwidth. Its function is to select a band of frequencies from a signal spectrum applied to its input circuit and to convert the information therein to an equivalent bandwidth at dc. The basic element of a Lock-In Amplifier is a phase-sensitive detector in which the signal voltage is mixed with a reference voltage, producing sum and difference frequencies. A low-pass filter at the output of the mixer rejects the high frequency components corresponding to sum frequencies, and passes the difference frequencies that lie within its passband. In particular, the difference frequency due to components of the signal at the reference frequency is zero or dc. Difference frequencies resulting from components of the signal spectrum at frequencies differing from the reference frequency by more than the cut-off frequency of the low-pass filter will be attenuated. Consequently, the output from the low-pass filter will be due to that portion of the signal spectrum which lies about the reference frequency within a passband determined by the low-pass filter.

MAIN FRAME SPECIFICATIONS

FREQUENCY RANGE: Continuously tunable from 1.5 Hz to 150 kHz in 5 ranges. Calibration accuracy within ±5%.

NOISE REJECTION: A signal 59 dB below ambient white noise in a 1 kHz bandwidth centered about signal frequency can be recovered with a signal-to-noise ratio of 1.

EQUIVALENT NOISE BANDWIDTH: 0.00125 Hz minimum (100 seconds maximum internal RC integrating time, 12 dB/oct.)

FILTER TIME CONSTANTS: 0, 1, 3, 10, 30, 100, 300 milliseconds; 1, 3, 10, 30, 100 seconds and EXT. position which allows capacitance to be added to rear connector to obtain any desired time constant. 6 or 12 dB/octave roll-off selectable by front panel switch.

ZERO SUPPRESS: Calibrated control permits off-setting zero by ±1000% of full scale on any range.

LINEARITY: ±0.1% of full scale.

SIGNAL CHANNEL CHARACTERISTICS: Active notch filter in negative feedback loop with nominal Q of 10. Calibrated front panel adjustment allows Q to be varied from 5 to 25 with no change in gain.

REFERENCE CHANNEL CHARACTERISTICS: The reference signal, by which the signal to be measured is demodulated, is obtained by four modes of operation.

INTERNAL: Internal oscillator drives the demodulator and presents a continuously variable 0-1 V rms (open circuit) signal at the REF. IN/OUT Connector. The source impedance is a constant 600 ohms.

EXTERNAL: Phase control not operable. Requires externally generated signal of 1 V peak-to-peak minimum level which crosses its mean value only twice each cycle with equal time between crossings.

SELECTIVE EXTERNAL: Externally generated reference signal filtered by tuned amplifier with a Q of 10, phase shifted and applied directly to demodulator. Minimum of 25 mV rms signal required.

AUTOMATIC: Any waveform which crosses its mean value only twice each cycle, and for which the smaller of the two mean-to-peak excursions is at least 500 mV. The instantaneous value of the waveform must not exceed ±100 volts.

PHASE ADJUSTMENT: Calibrated 360° phase shifter, accurate to ±5°. Differences in phase shift between signal and reference channels may be in excess of 5° on the X1 and X10⁴ frequency ranges.

DC OUTPUT STABILITY: 0.1% of full scale in 24 hours with constant ambient temperature.

OUTPUT (located on rear): Single-ended with respect to ground. Panel meter (½% mirror scale with either center or optional left-hand zero) full scale corresponds to ±10 volts at output terminal. Adjustment allows output source impedance to be varied from 7K-22K ohms which permits driving either ±½ ma recorders with internal resistance less than 10 K or ±1 ma recorders with internal resistance less than 3 K as well as servo-type recorders.

MONITOR: A five position switch allows the panel meter and monitor output terminals to be switched to SIGNAL, REFERENCE, OFF, MIXER (OUTPUT) and OUTPUT to allow monitoring and adjustment of critical points.

INTERNAL CALIBRATOR: Provides 21 square wave output levels extending from 20 nanovolts to 100 millivolts, accurate to within 1%.

NOTE: At frequencies above 50 kHz, calibrator outputs below 1 μV may be in error by more than 1%. The use of external decade attenuators is recommended for applications where this might present difficulty.

POWER REQUIREMENTS: 105-125 volts or 210-250 volts; 50-60 Hz; 25 watts.

SIZE: 19" wide x 7" high x 15¾" deep.

WEIGHT: 41 lb.

WARRANTY: 1 year.

PREAMPLIFIER SPECIFICATIONS:

GENERAL: These preamplifiers are intended for use with the Model HR-8 Lock-In Amplifier. They can be plugged directly into the Model HR-8 main frame or operated remotely (with the purchase of a remote adapter kit.) In either case, the preamplifier is powered from and controlled by the Model HR-8. The following specifications refer to the performance of the individual preamplifier when used with the Model HR-8.

TYPE A PREAMPLIFIER: The Type A Preamplifier is a high input impedance low noise front end for the Model HR-8 used to obtain optimum signal-to-noise ratios for source impedances above 3 K.

SENSITIVITY: 21 ranges, from 100 nanovolts rms full scale to 500 millivolts rms full scale, in a 1-2-5 sequence.

FREQUENCY RANGE: 1.5 Hz to 150 kHz.

INPUTS: Differential or single-ended. Common mode rejection is in excess of 60 dB at 1 kHz.

INPUT IMPEDANCE: Each input to ground, 10 megohms shunted by 20 pf.

NOISE: High sensitivity settings (100 nV to 50 μV), noise figure for either (single-ended) input shall be better than 0.5 dB for a 100 k source at 1 kHz. For low sensitivity settings (100 μV to 500 mV), the internally generated noise shall result in a meter deflection of less than 1% (RMS) of full scale with a time constant setting of 1 sec 6 dB/oct., at any operating frequency above 15 Hz. Refer to Fig. 1-1 for noise figure contours.

4. SUMMARY AND CONCLUSION

This report has presented the result of a continuing research and development program the objective of which is to develop a reduced bandwidth television system and a technique for television transmission of holograms. The result of the former is a variable frame rate television system (VFTV), the operation of which has been demonstrated for both black-and-white and color signals. This system employs a novel combination of the inexpensive mass storage capacity of a magnetic disc with the reliability of a digital system for time expansion and compression. Also reported have been the results of a theoretical analysis and preliminary feasibility experiment of an innovative system for television transmission of holograms using relatively conventional TV equipment along with a phase modulated reference wave for production of the original interference pattern. Work which is expected to lead to a capability for production of wide perspective holograms by combining several narrow perspective views is proceeding at present.

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