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High-Voltage DC Power Processing Thermal Control and Packaging Techniques

MARTIN MARIETTA

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HIGH-VOLTAGE DC POWER PROCESSING THERMAL CONTROL AND PACKAGING TECHNIQUES

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FOREWORD

This report was prepared by Martin Marietta Aerospace, Denver Division, under Contract NAS8-33078 "High Voltage DC Power Processing Thermal Control and Packaging Techniques" for the George C. Marshall Space Flight Center of the National Aeronautics and Space Administration.

ABSTRACT

This report describes the development of a conceptual packaging design for the NASA-George C. Marshall Space Flight Center Programmable Power Processor being developed for the NASA Advanced Programs 25-kW Power Module. The power processor operates in several modes, delivering up to 100 amperes of regulated electrical power, operating at input voltages to 375 volts with outputs controlled by an integral microprocessor. Several alternative packaging concepts are discussed and evaluated. High-voltage design applications, power stage interconnection and EMI considerations are also discussed. Preliminary thermal analyses were performed and the results presented for each conceptual approach with parametric study results given for the selected concept.

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I. INTRODUCTION

The programmable power processor (P^3) is a key element in NASA's 25-kilowatt power module program currently in the advanced development phase. The 25-kilowatt power module uses high-voltage solar arrays for energy collection and power processing groups of batteries, charge controllers and load bus regulators to supply 25-kilowatts of electrical power at approximately 28 volts to the Shuttle orbiter and internal housekeeping requirements.

The P^3 assembly is intended to function as a battery charge control unit or as a buck regulator with its output characteristics programmed by an internal microprocessor. Output power and voltage levels have been chosen to not only support Shuttle orbiter missions but also future large space power systems using higher voltage distribution networks. The unit can deliver up to 3 kilowatts of regulated power at 30 volts. Configured as a charge controller, the output is 120 to 180 Vdc. By developing a standardized modular power processor capable of performing a variety of functions with autonomous control, NASA expects savings of many millions of dollars compared with systems utilizing Skylab-type hardware for power processing. These savings are possible due to the reduced number of units required to satisfy the same power level.

In support of Marshall Space Flight Center's P^3 development, Martin Marietta has undertaken a design study to examine various alternatives in packaging the P^3 assembly leading toward an optimized packaging concept based on cost, performance, size and weight factors. The effort is discussed in detail in this report, with conclusions and recommendations for a P^3 packaging design. The major problems addressed in this study include thermal control, high-voltage protection and power stage interconnection.

These problem areas are paramount due to the unusually large thermal loads, high voltages and high current levels required for P^3 operation. Such design specifics as shielding configurations, material selections, circuit board layouts and structural details are not covered in this study report. They are among the numerous design problems remaining to challenge the packaging engineer in producing an optimized P^3 design.

II. PACKAGING CONCEPT DEVELOPMENT

The programmable power processor (P^3) offers a major challenge for the packaging designer in several areas. This unit is required to condition spacecraft electrical power with an input voltage as high as 375 Vdc when configured as a battery charger, and output current up to 100 amperes when configured as a bus regulator. Compared with the more typical spacecraft power regulator, the peak power, voltage stress, and current levels are up by roughly an order of magnitude. Thus the design problem is made more complex due to large components, high thermal dissipation of power switching devices, and high voltage and current levels--all of which require special packaging consideration for successful design.

The objective of this effort is to develop a packaging concept capable of satisfying the P^3 requirements for NASA's 25-kilowatt power module system resulting in minimum size, weight and cost impact while meeting all design criteria for the P^3 as they pertain to packaging. In examining various conceptual packaging approaches we have attempted to identify the more significant problems and recommend what appears to be the best solution from the viewpoint of economy, efficiency and performance. Performance of a detailed packaging design is not within the scope of this initial concept study. Tradeoff studies have been conducted with sufficient analyses to define an optimum packaging concept for the P^3 assembly. Further design refinement and optimization of the selected approach are necessary to define specific performance limits in thermal control and structural capability and to minimize weight, volume and cost factors.

A. PACKAGING CRITERIA

The overall circuit arrangement is shown in Figure 1 in simplified form. The power processor load current is supplied by three parallel power stages operating in phased sequence with each output power transistor having its own commutating diode and filter inductor. The power stages operate at 10 kHz with a variable duty cycle for conduction up to 100%. The maximum output current for each power stage is 100 amperes and maximum input voltage is 375 volts. These conditions occur under separate operating modes. The preregulator base drive circuits also operate at 10 kHz squarewave with voltages to 375 volts peak. The remaining circuits, with the exception of input and output filter banks, operate at 20 volts or less.

A partial list of circuit functions and associated parts by type is included in Appendix A and may be considered representative for preliminary packaging considerations. Other design criteria considered in this study include those discussed in the following subsections.

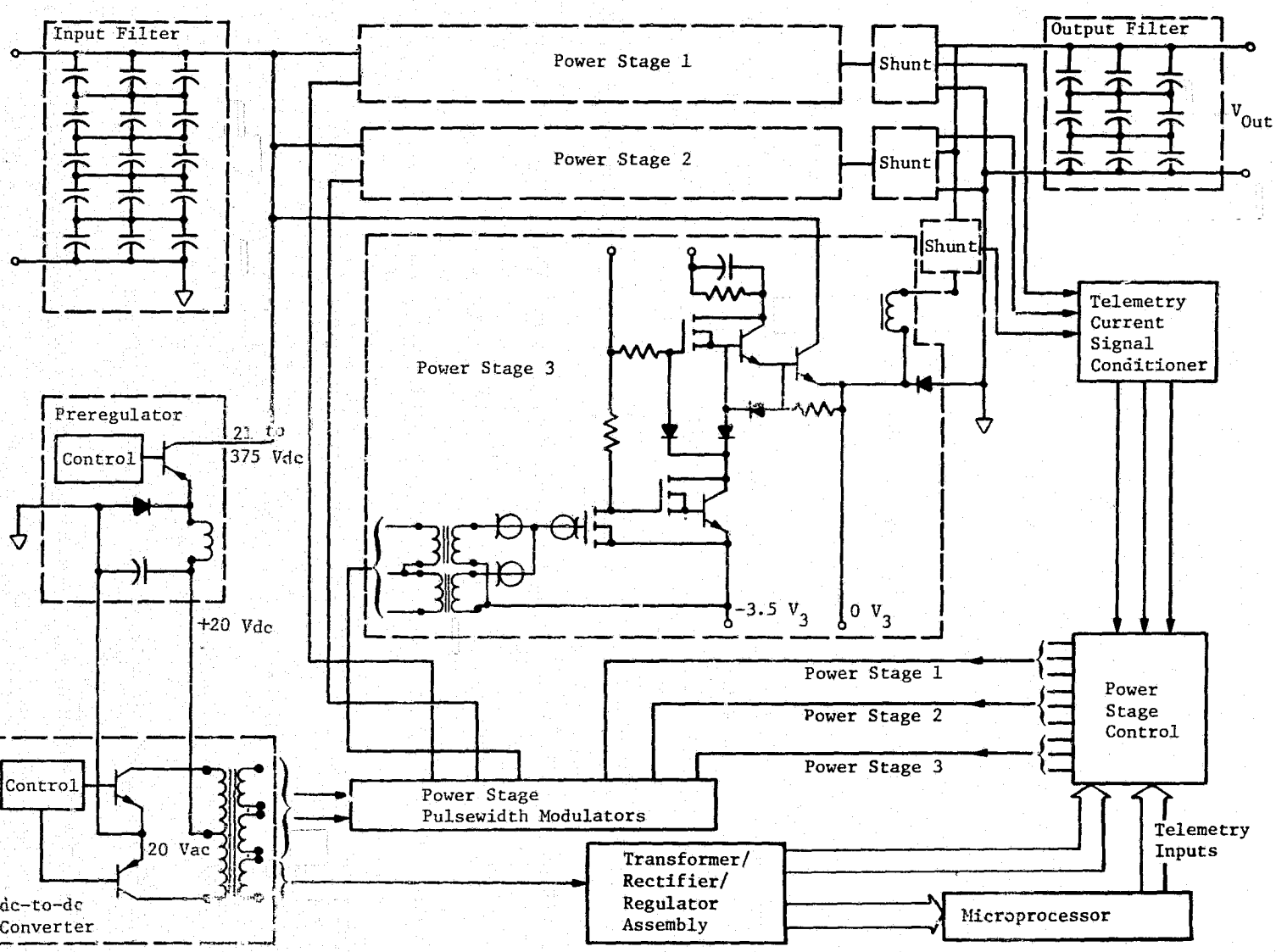


Figure 1 P^3 Simplified Block Diagram

1. EMI

The power processor operation involves current switching with high di/dt as well as high dv/dt sources. These include the input capacitor bank, power switching output transistor and commutating diode for di/dt-induced EMI. The base drive circuits for the power stages and the preregulator are sources of dv/dt-induced EMI.

2. Thermal Loads

The maximum steady-state thermal power dissipation is 608 watts total with each power stage dissipating a maximum of 155 watts. A detailed breakdown of part thermal dissipation is given in Table 3 of Section D (thermal analysis). Allowable temperature limits for semiconductor junctions is 125°C. For other electronic parts the maximum case temperature was taken to be 85°C as a conservative limit.

3. Environments

The environmental criteria are tabulated.

a.	Temperature	--	Controlled baseplate temperature from -20 to 10°C.
b.	Pressure	--	760 to 10^{-6} torr
c.	Vibration	--	Random: 0.24 g^2/Hz max, 20 to 2000 Hz, 12.5 g rms composite
		--	Sine: 3 to 10 Hz at 1-in. DA 10 to 35 Hz at 5-g peak 35 to 50 Hz at 1-g peak
d.	Acoustical Noise	--	145 dB
e.	Humidity	--	Per MIL-STD-810C, Method 507.1 Procedure 1 (Nonoperational)
f.	Storage Life	--	3 years

B. CONFIGURATION STUDIES

Several packaging approaches were examined, with changing emphasis on such factors as modularity, thermal performance, structural efficiency, cost and EMI control. Common to each of these alternative concepts was the power stage component interrelationship in which the major stud-mounted power devices associated with a single power stage were mounted closely together on a machined structure extending from the assembly base as in Figure 2.

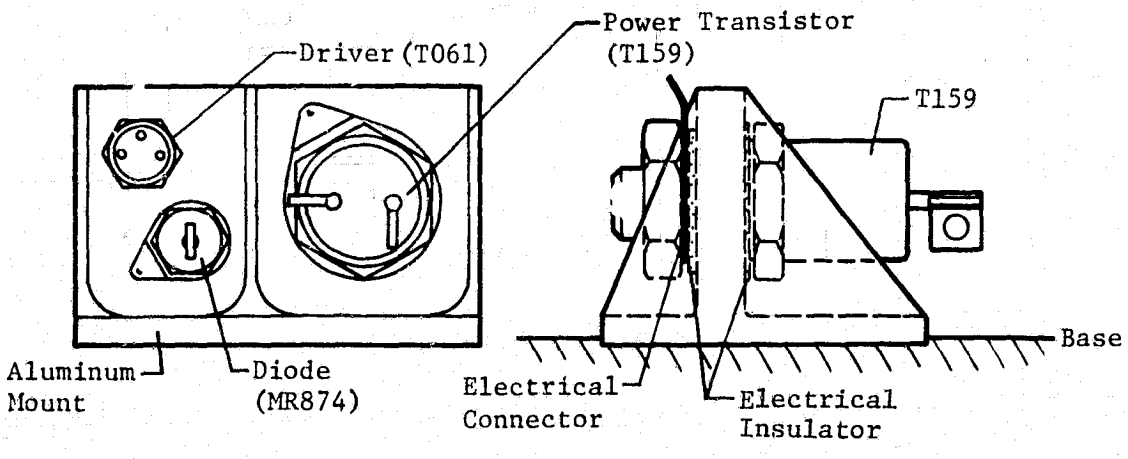


Figure 2
Power Stage Transistor and Diode Mounting

The EMI and heat transfer considerations were the primary drivers in selecting this approach. Similarly, the power stage inductor and base drive circuits were located adjacent to the power semiconductor cluster of each power stage to facilitate EMI control.

1. Alternative Approaches

Figures 3 through 7 illustrate five packaging concepts, including the overall configurations and parts arrangement for each conceptual approach.

In configuration 1 (Fig. 3) the input and output filter capacitor banks and the three power stages are integrated in a base chassis. Input and output connectors and associated filters are located at opposite ends of the chassis. The power stages are arranged so the power transistor, commutating diode and base drive transistor, the major thermal dissipators in this circuit, alternate between opposite sides of the enclosure to distribute the major heat load. Such low-power circuitry as the microporcessor, telemetry signal conditioning and control interface circuits are mounted on printed wiring boards grouped together in a secondlevel chassis that forms a cover for the base enclosure. A second group of printed wiring boards contains the housekeeping power and control circuits and is also mounted in the upper-level chassis with stud-mounted parts on machined ribs adjacent to the circuit boards. Compartments for isolating the two groups of circuits may be machined into the upper chassis for EMI control.

The upper and lower chassis are interconnected by an external harness and connectors located at the ouptut end of the assembly. External control inputs and telemetry signals are routed through a connector interface at the microprocessor end of the top chassis.

The base chassis structure consists of a machined aluminum baseplate with internal reinforcing ribs and component attachment bosses fastened to sidewalls and endplates. Primary component loads are introduced directly into the base. The second-level chassis is a single machined structure with a top cover to complete the enclosure. Primary structural and thermal load paths from the upper-level chassis are taken through the base chassis walls to the mounting base. Alternative fabrication techniques for the base chassis include a single machined (hog-out) chassis, a welded plate structure or a machined casting. The final selection of fabrication methods should be based on fabrication capabilities, cost and schedule considerations.

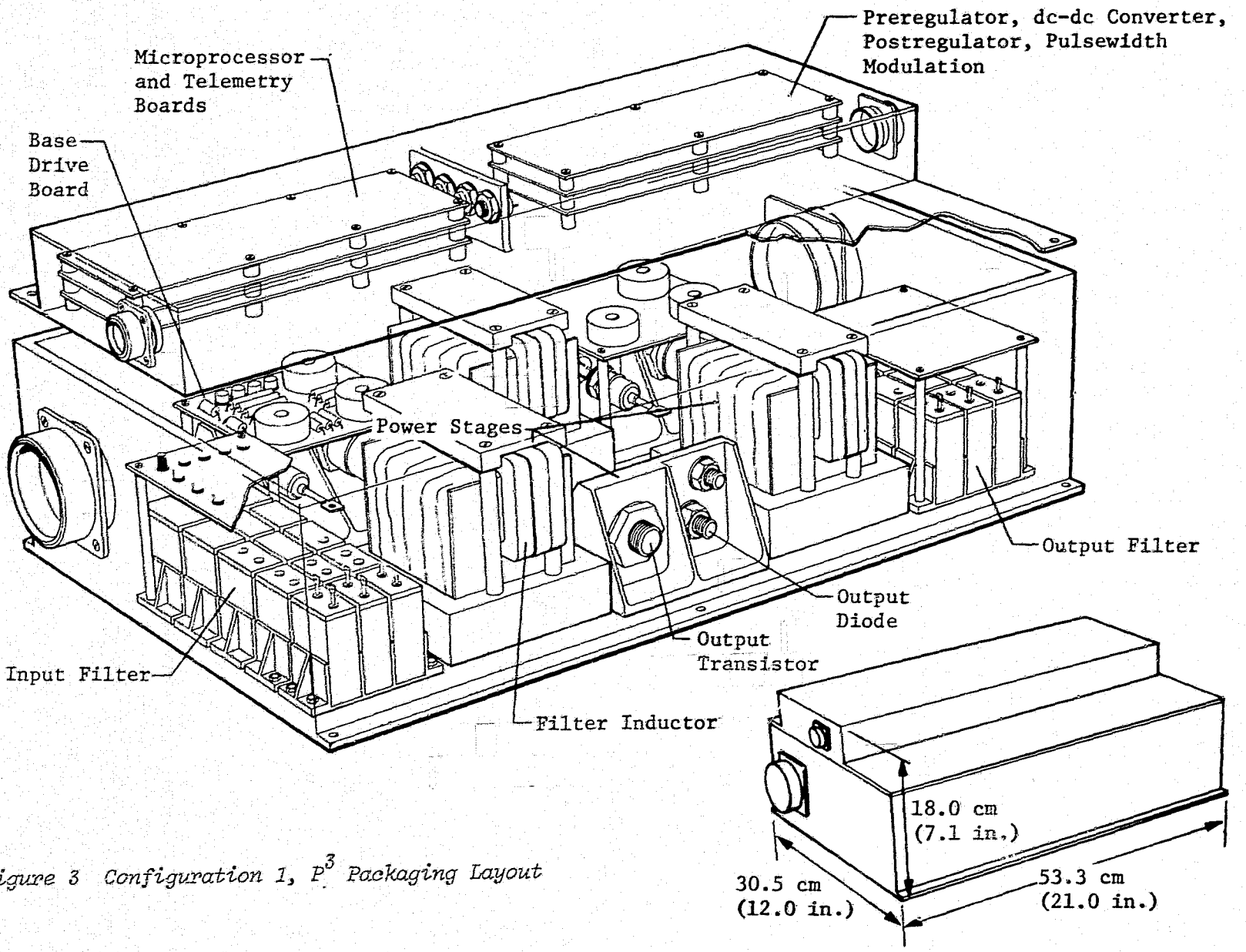


Figure 3 Configuration 1, P^3 Packaging Layout

Configuration 2 (Fig. 4) is a modular approach in which the power stages are packaged as three iednetical modules to be mounted directly on a spacecraft coldplate. The power modules are joined to a second-level compartmented chassis containing the input and output filter banks, housekeeping power and control circuits, and telemetry and microprocessor boards. The power stages and the filter bank are interconnected by harnessing and cable runs through access holes at the chassis interfaces. Low-power control and telemetry interconnection to the power modules are provided by connector interfaces and external cable runs between the upper chassis and each power module. A single power stage module can be removed from the assembly for maintenance or replacement by disconnecting the module power lines at the filter bank power bus, separating the module control connector and removing the fasteners joining the upper mainframe structure and power module. EMI is controlled by providing compartments for sensitive circuit elements, grouping and shielding cable runs and utilizing internal feedthrough filters for isolation. Structural and thermal load paths for the upper-level components are via the chassis/power module interface, through the module structure, to the module base/coldplate interface.

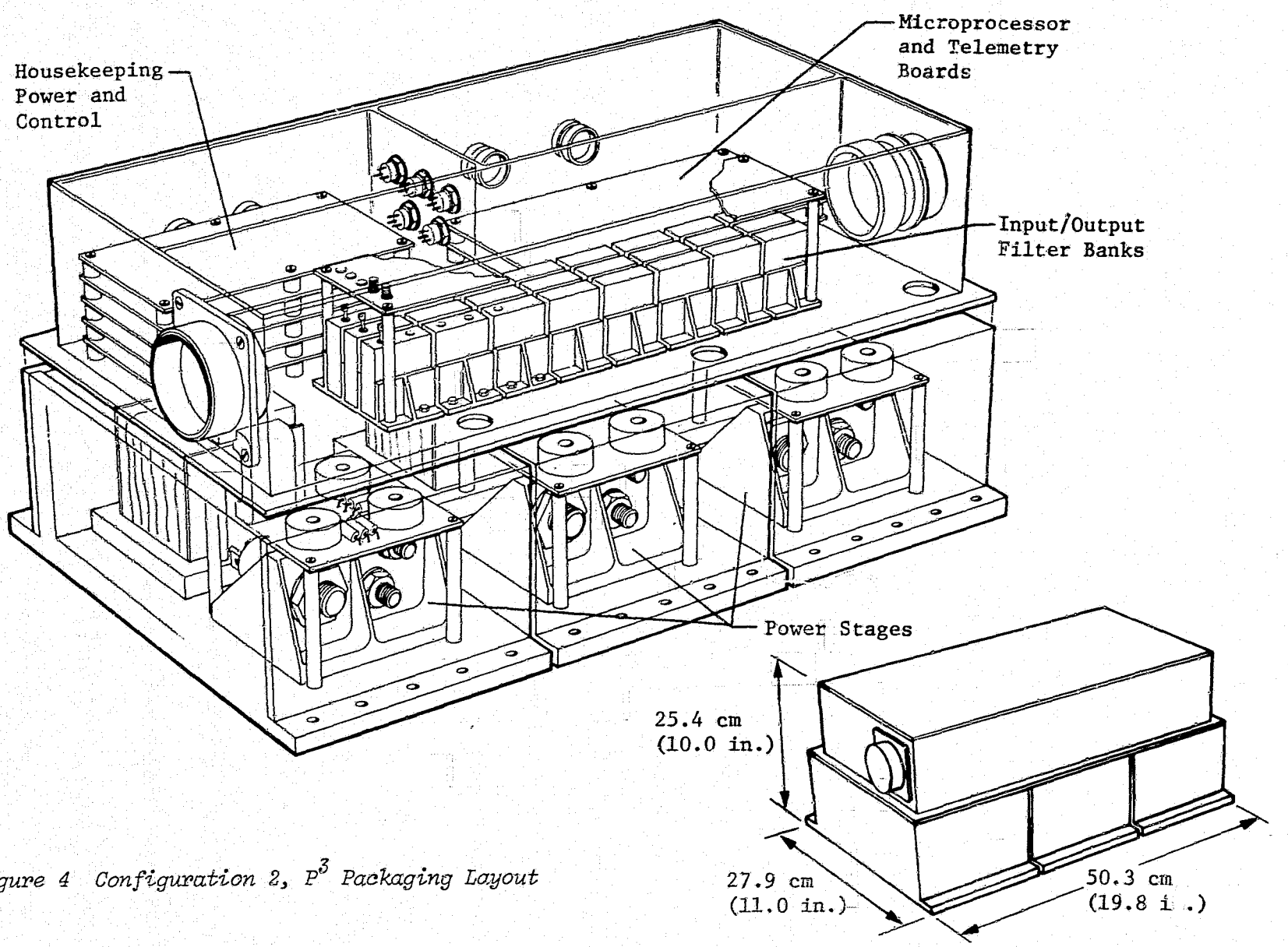


Figure 4 Configuration 2, P^3 Packaging Layout

Configuration 3 is an integrated assembly arranged as shown in Figure 5. Input and output capacitor filter banks are located at one end adjacent to both main power connectors. Three power stages are alternately arranged in the central portion of the chassis. The microprocessor, telemetry, power control and housekeeping circuits occupy the opposite end of the assembly with the microprocessor, control interface circuits and telemetry signal conditioning contained on circuit boards in a separate subchassis for EMI isolation. Access to the microprocessor is effected by removal of the assembly endplate.

The housekeeping power and control circuits are on printed wiring boards supported by the subchassis, with associated stud-mounted components located on adjacent heat sink brackets. Internal connector interfaces between the control and power stages facilitate checkout of the low-level circuits prior to installation in the main assembly and provide easy access for troubleshooting and maintenance (power bus interconnection is discussed separately under subsection 4). The major components and subassemblies are mounted directly to the assembly base structure to minimize thermal conduction and structural load paths to the coldplate mounting interface.

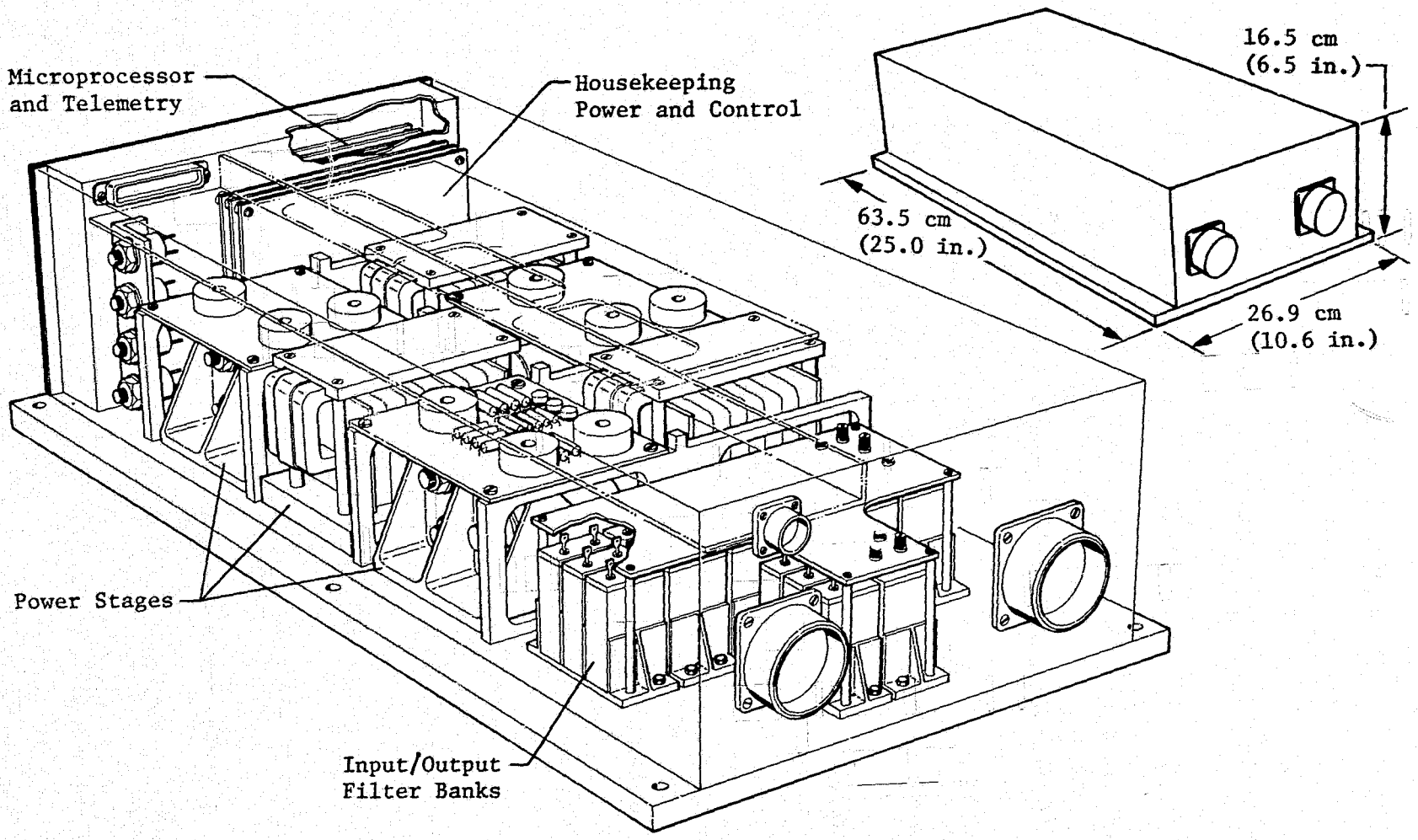


Figure 5 Configuration 3, P^3 Packaging Layout

Configuration 4 (Fig. 6) is a departure from the other approaches in that it assumes a coldrail mounting scheme as opposed to base mounting. This results in a near-center-of-gravity (cg) mounting approach with good potential for improved structural efficiency and compactness. The power stages are mounted to one side of a central support structure, with the filter capacitor banks, housekeeping power and control and microprocessor circuits mounted on the opposite side. Isolation is provided by a subchassis that encloses the microprocessor and telemetry signal conditioning boards. The two enclosures on either side of the central plate structure may be fabricated from low-cost deep-drawn aluminum parts available commercially as a standard item and attached to a flanged interface at the central support structure. A connector bracket is required to support the power connectors located above the mounting plate at one end of the assembly. Cabling from the power stages to the capacitor bank and control circuits is kept very short in this arrangement by routing cables through the central plate. Structural and thermal loads are carried directly from the central support to the rail-mounted flanges.

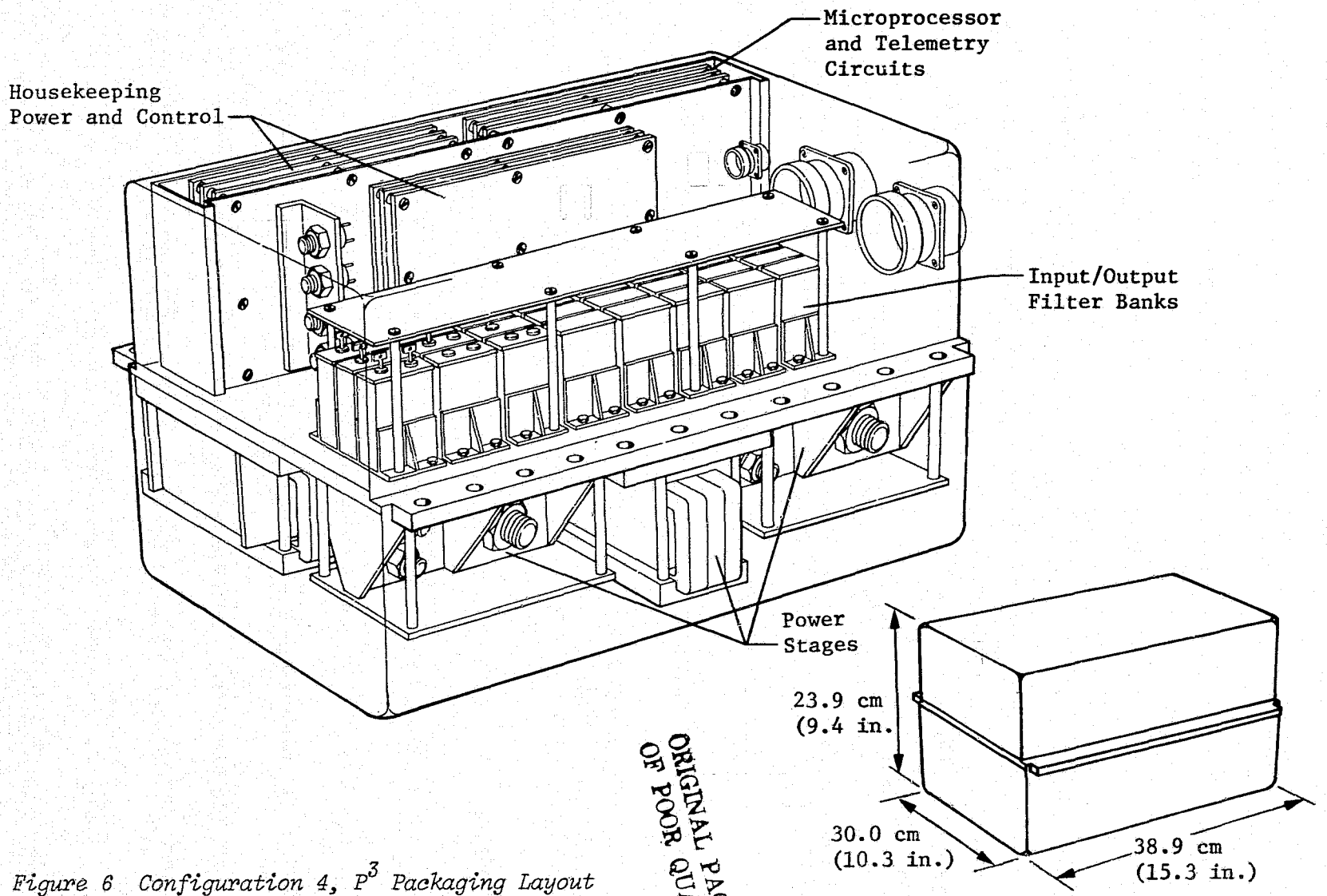


Figure 6 Configuration 4, P^3 Packaging Layout

Configuration 5 (Fig. 7) is an alternative approach in modularizing the power stages, with improved thermal conduction as compared with configuration 2. The power stages with associated pulsewidth modulation circuits are packaged in interchangeable modules and connected to a mainframe chassis containing the capacitor filter banks, housekeeping power and control circuits, and the microprocessor. The mainframe is compartmented to provide isolation for low-level circuits, cabling access and EMI control for the filter section. The power stage modules interface with the mainframe via bulkhead connectors. Access for connector installation is provided by removal of the mainframe cover plate. Input and output power connectors are located at either end of the mainframe lower compartment. Major power stage components and capacitor banks are mounted directly to the chassis base structure, minimizing the thermal conduction and structure load paths.

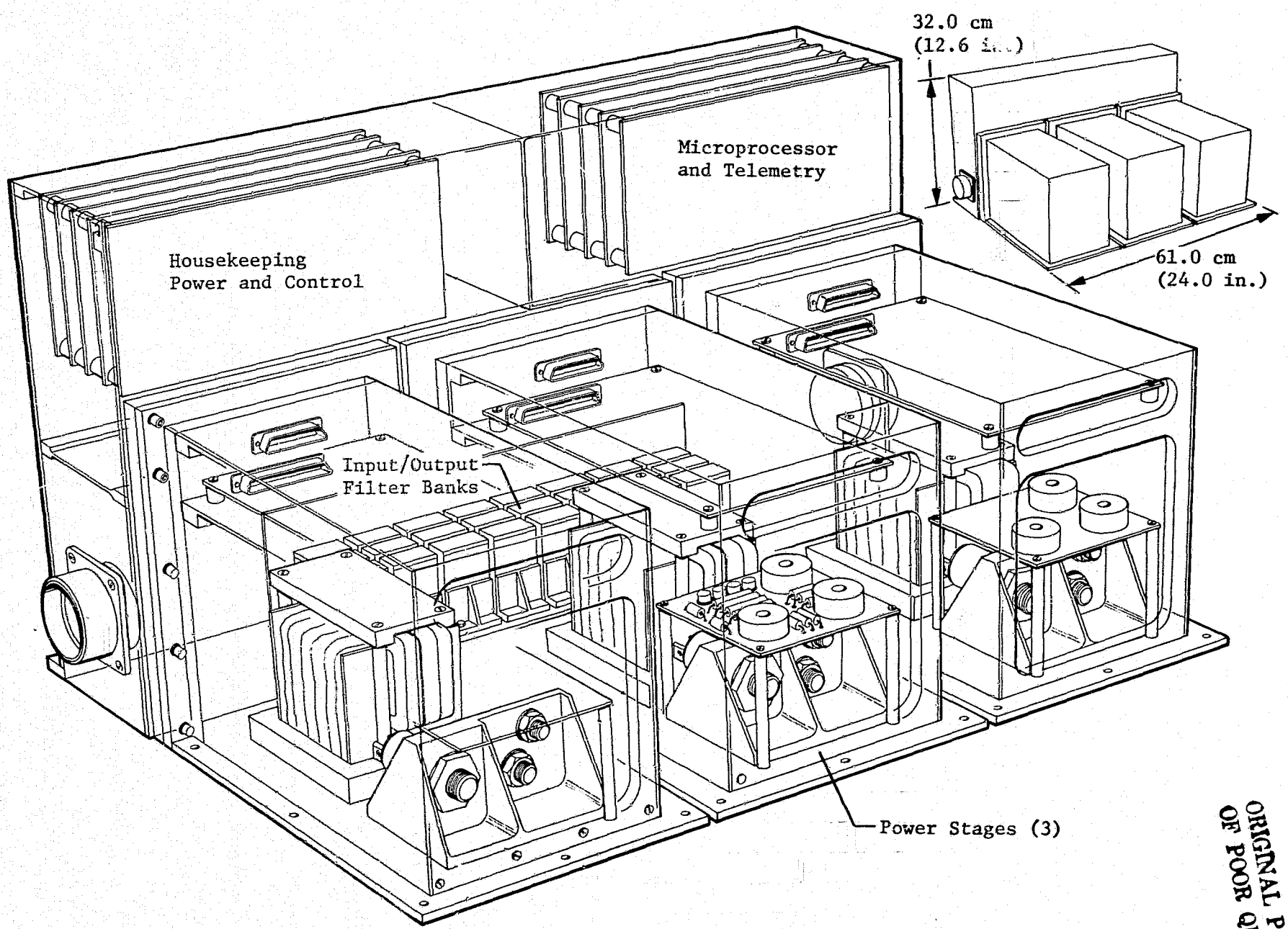


Figure 7 Configuration 5, P^3 Packaging Layout

2. Rating Factors

Table 1 is an attempt at rating conceptual alternatives for such factors as cost potential (producibility), ease of trouble-shooting and repair or replacement of components (maintainability), isolation of sensitive components or major EMI sources (EMI control), plus relative weight, size and overall thermal performance.

Table 1 Packaging Factors

	Configuration				
Factor	1	2	3	4	5
Producibility	Fair	Poor	Good	Excellent	Poor
Maintainability	Fair	Good	Fair	Fair	Excellent
EMI Control	Fair	Good	Fair	Good	Good
Weight	Good	Fair	Fair	Good	Poor
Size	Fair	Fair	Fair	Excellent	Poor
Themal Performance	Good	Fair	Good	Unsatis-factory	Good

Since the design concepts are very preliminary at this stage of P^3 development, the ratings tend to be qualitative judgments rather than based on hard facts. In evaluating producibility factors we considered the number of machined details to fabricate and assemble, plus the relative accessibility of components in final assembly. Maintainability was considered enhanced through the use of connectors and replaceable modules. EMI control considered short and direct routing of high-current conductors as being desirable. Weight, size and thermal performance factors were based on preliminary packaging and thermal analyses results.

3. Weight and Volume Summary

Table 2 summarizes the weight breakdown and integration volume requirements for each of the five packaging concepts. For this estimate the base structures (primary component-mounting surfaces) were assumed to be equivalent in weight to a uniform aluminum plate with a 0.48 centimeter (0.188-in.) thickness, recognizing that in the actual design the dimensions vary considerably based on thermal and structural considerations. Similarly, walls and covers were assumed to average 0.25-centimeter (0.10 in.) thick aluminum except in areas of insert bosses. For configuration 4 the aluminum cover enclosures were taken to be 0.16 centimeters (0.063 in.) in thickness.

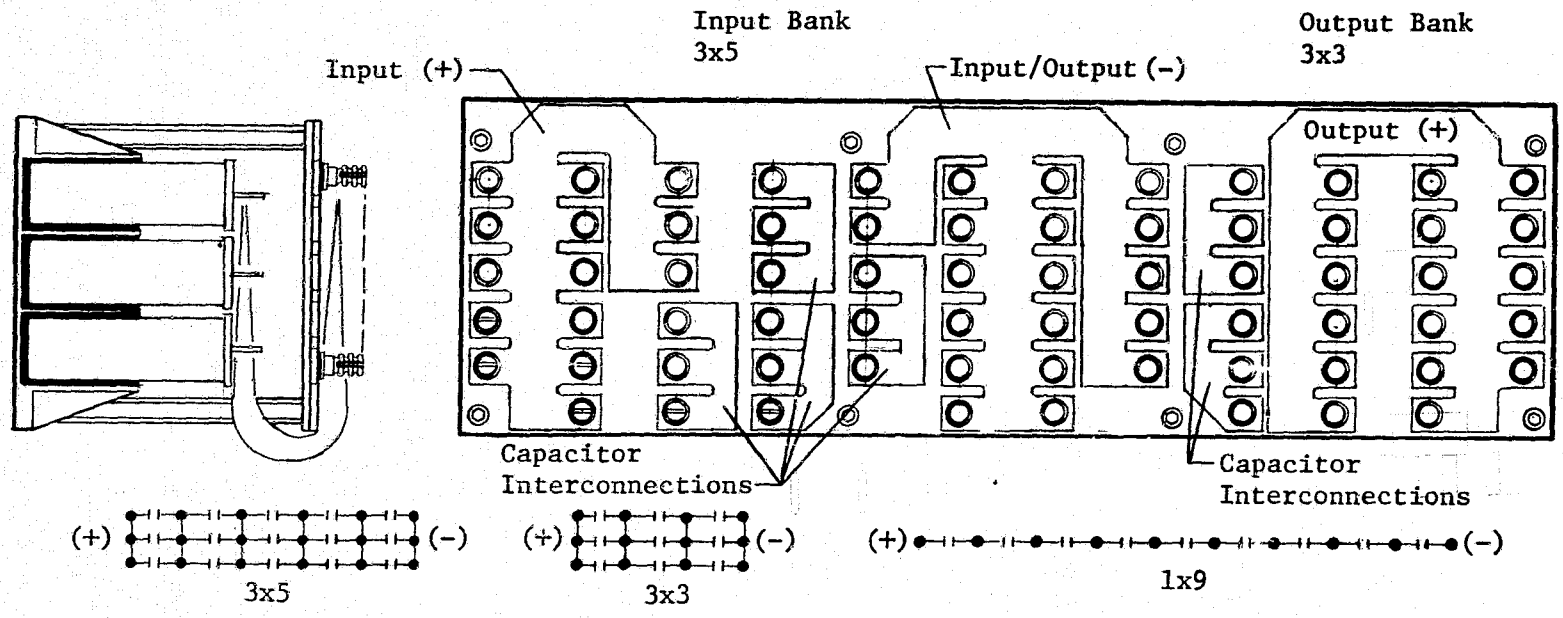
The integration volumes listed in Table 2 were calculated as the product of overall width, length and height using maximum dimensions and ignoring flanges and connectors. The irregular shapes of configurations 1 and 5 suffer somewhat in this comparison but more accurately reflect the usable space requirements for spacecraft integration.

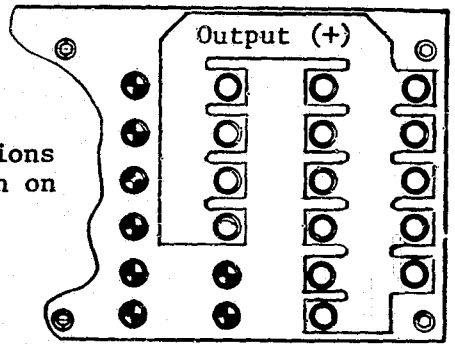
Table 2 P^3 Weight and Volume Summary (Weight in kg)

Component	Configuration 1	2	3	4	5
-Housekeeping Power and Control Circuits (4 Boards + 6 Large Transistors)	0.907				
-Base Drive PWB Assembly	0.581				
-Microprocessor (2 PWB Assemblies)	0.363				
-Pulsewidth Modulator (3 PWB Assemblies)	0.807				
-Capacitor Bank Terminal Board	0.209				
-Power Diode (MR874)	0.051		These Items Are the		
-Power Transistor (D60T455010)	0.680	16.512	Same for All		
-Base Drive Transistor	0.090		Configurations		
-Capacitor Banks	2.722				
-Capacitor Holders	0.331				
-Inductor	9.771				
-Basic Structure	7.046	10.696	9.671	7.239	14.170
-Connectors	0.476	0.748	0.295	0.340	0.408
-Wire, Potting, Miscellaneous Hardware	1.814	1.588	1.814	1.588	1.588;
-Total Weight, kg	25.8	29.5	28.3	25.7	32.7
-Integration Volume, $m^3 x10^{-2}$	2.93	3.57	2.82	2.40	8.08

4. Power Stage Interconnection

As described earlier in this report, the power stage circuits are operated in parallel from the input power bus and sequenced by the control circuits to deliver the appropriate load current. To physically accommodate this paralleling function and provide for a 100-ampere line capacity to each power stage, the P^3 packaging approaches all utilize the terminal board-busbar configuration illustrated in Figure 8. In this approach large bifurcated terminals are used as junctions for multiple 12-gage conductors from the input shunt and the three power stage buses. A conductor pattern stamped or machined from 1-millimeter thick copper sheet is laminated to an epoxy glass substrate to form an interconnection bus pattern. Terminals are installed and soldered to finger-like extensions of the bus that act to facilitate soldering by reducing the heat sinking effect of the copper bus. The terminal board is designed to also accept and interconnect the filter capacitors that comprise the input and output filter banks. The bus geometry shown in the figure is representative of P^3 configurations 2, 4 and 5. Variations of the same approach are used in the other conceptual designs. The unusally large quantity of terminals shown in the figure are required to provide terminations for six 12-gage conductors to each of the three power stage positive buses, which must have the capacity for 100 amperes. Additional terminals are required for multiple conductors from the input and power stage shunts, output connector and capacitor bank. The negative bus, located in the center of the terminal board, functions as a single-point ground for all power circuits.





Capacitor Interconnections for a 1x9 Configuration on Output Bank

Figure 8 Terminal Board Busing Approach

As a design requirement not previously mentioned, the output filter capacitors must be capable of being interconnected as a 3x3 parallel-series combination when the P^3 is configured as a battery charge control unit, and connected as nine capacitors in series when operating as a load bus regulator. The terminal board interconnection approach easily accommodates this requirement as illustrated in Figure 8.

Terminal junctions were selected over other methods using mechanical joints to facilitate insulation of high-voltage conductors and terminations and avoid the air entrapment during conformal coating or encapsulating operations that could lead to corona problems in flight. This problem is discussed in the following Section C. Although not particularly desirable in highvoltage equipment design, soldered terminal configurations suitable for high-voltage applications are well defined and have been successfully used in spaceflight hardware. Care must be taken to avoid sharp edges, protrusions of wire ends, and other conditions that concentrate electrical fields leading to eventual breakdown of the insulation system.

C. HIGH-VOLTAGE CONSIDERATIONS

In spacecraft equipment design, high-voltage packaging is usually associated with particle detector experiment power supplies, CRT circuits, traveling wave tube amplifiers and similar

devices with circuits operating in the kilovolt or 10's of kilovolts range. Great care is invariably taken during the electrical and mechanical design of such hardware to reduce or avoid corona effects and insulation breakdown--often with less than complete success.

Most spacecraft equipment is operated at voltages low enough that corona or insulation breakdown is not even a consideration during design reviews and prototype testing, despite the fact that given appropriate conditions corona can exist at almost any voltage level.* The usual design practices employed for circuit board design, conformal coating, cleanliness and outgassing control are sufficient to prevent electrical breakdown problems in most cases.

1. The P^3 High-Voltage Problem

The P^3 circuits and operating modes involve dc voltages up to 375 volts and ac voltage levels at 10 kHz squarewave and at a 375-volt peak. Based on Paschen's law concerning the behavior of electrical disharges in gases, corona and subsequent arcing will occur at a theoreteical minimum voltage of 275 volts peak for air under certain conditions of temperature, electrode configuration, etc. The inclusion of trace quantities of other gases can considerably reduce the minimum breakdown voltage. The effect of ac frequency is to lower the breakdown peak voltage at critical pressure so that at 10 kHz the lower voltage breakdown limit is 210 volts peak. This is shown in Figure 9 extracted from JPL Design Requirements, DM509306A. In addition to ac frequency and gas composition, the minimum breakdown voltage is influenced by the electrode configuration, temperature, conductor surface properties and the presence of coatings or contaminants on conductors.

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*W. G. Dunbar: High-Voltage Design Criteria, 50M05189, George C. Marshall Space Flight Center, August 1972.

The voltage breakdown and corona onset voltage data based on Paschen's law are presented as a function of gas pressure for fixed spacing of electrodes (Fig. 10) or as a function of pressure times spacing.* Considering the maximum operating voltages for the P^3 circuits of 375 volts and electrode spacing ranging from probable minimum of 0.25 centimeter to a maximum path inside the enclosure of 65.0 centimeters, the critical pressure range for the P^3 works out to approximately 0.2 N/m^2 to 2000 N/m^2 (1.5×10^{-3} to 15.0 torr).

This assumes an air atmosphere. The range may shift up to two orders of magnitude at the high end in helium or argon atmospheres. In this range of critical pressure with maximum operating voltages, the unit could experience electrical breakdown in the form of an avalanche discharge corona or arcing unless special precautions are taken in the design and manufacture to prevent their occurrence. Similarly, inadequate or improper use of solid dielectrics, contamination of insulating surfaces, sharp-edged or pointed conductors or any of several other factors can cause breakdown of solid insulation at these voltages, irrespective of ambient gas pressure.

2. Operational Requirements

Several approaches appear to be available to ensure that the P^3 will function properly in its assigned mission. The specific approach taken must consider such operational requirements as the extent of pressure decay at the initial turn-on of the P^3, the gas composition during operational life, and expected pressure changes in the environment due to spacecraft coolant venting, EVAs, RCS firings, etc.

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*Ibid

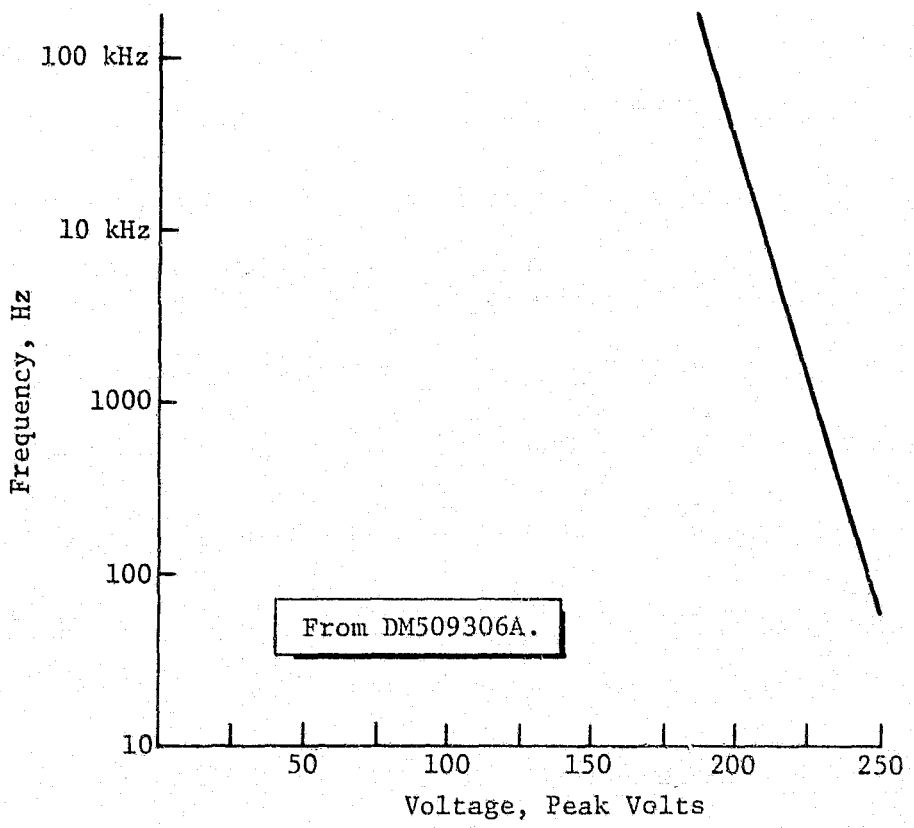

Figure 9 Lower Voltage Breakdown Limit vs Frequency

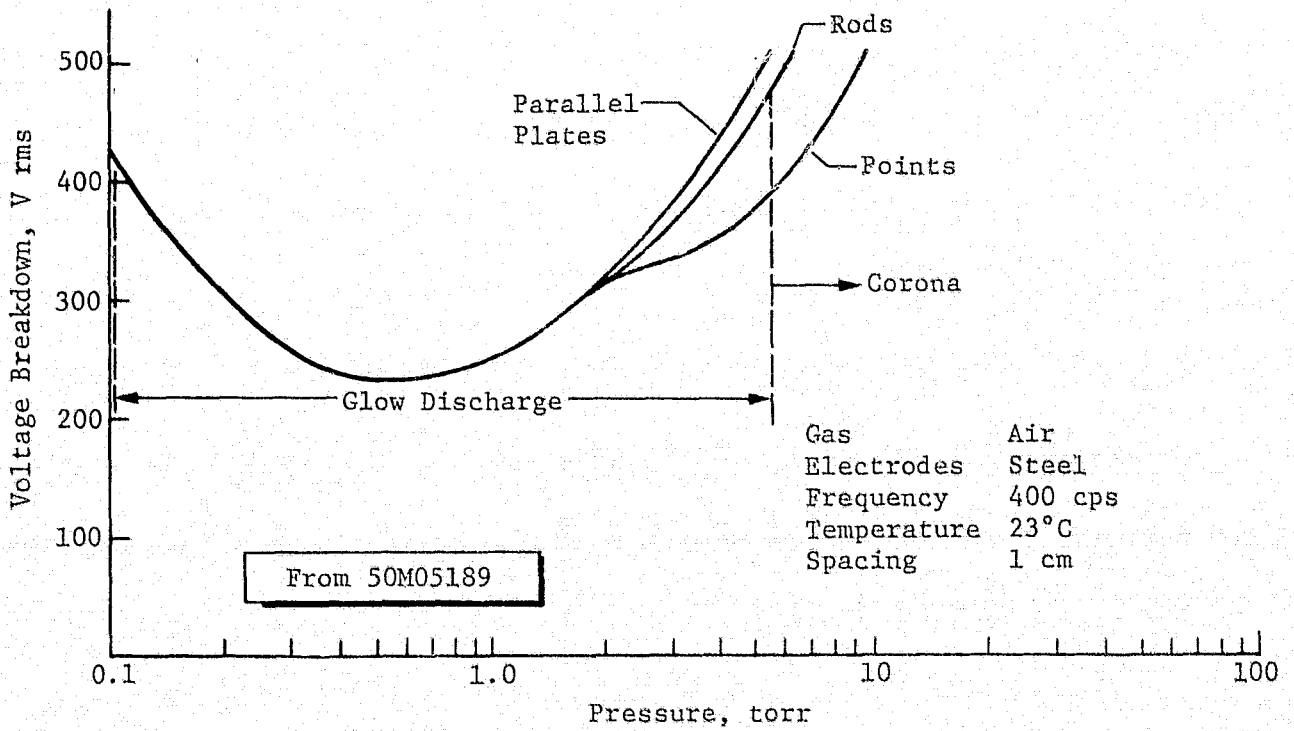

Figure 10
Voltage Breakdown and Corona As a Function of Pressure for Fixed Electrodes

For instance, one might assume that the P^3 assembly will never be required to operate within its critical pressure range. Or as a mission constraint the P^3 operation may be restricted to environmental pressures outside of its critical range.

Alternatively, the P^3 assembly may be considered as having to operate for short periods of time at critical pressures and during such time corona may be allowed to occur provided there is no damage to either internal or external components and the degradation is kept within acceptable limits.

A third approach to high-voltage design for the P^3 might be to consider the unit as having to operate within full specification requirements throughout its design life without arcing or corona at any pressure.

There are significant cost advantages in designing for operation outside of the critical pressure range, not only in development costs but also in fabrication and testing. High-voltage design techniques would still be required in the selection and application of solid dielectrics, printed wiring board layouts and joining techniques, and special attention to venting provisions in the design would be required to prevent entrapment of gases. However, shielding of high-voltage conductors and terminations could be simplified or eliminated in the absence of a corona-susceptible atmosphere, making connector selection and application easier.

The compromise approach that allows for corona and/or arcing to a limited degree has about the same benefits as designing for restricted-pressure operation. The design and manufacturing cost would be lower as compared with a design that must operate totally corona-free in any pressure environment. Allowing a limited degree of corona such as might occur during initial spacecraft venting and outgassing or during propellent venting or heat exchanger water dumping may be acceptable within mission constraints.

The approach that requires a design capable of unlimited pressure operation with no corona or arcing permitted results in maximum flexibility in the use of P^3 equipment, but requires extreme care in the design, fabrication and testing to assure total corona-free operation. Additional shielding of high-voltage cabling and components would be required along with the probable need to develop a suitable power connector to operate in this environment.

3. High-Voltage Design Applications

The circuits in the P^3 assembly that must be given special consideration for high-voltage protection include the entire positive power bus, input and output filter bank, preregulator and base drive circuits, the power stage components and the power connectors. To avoid breakdown, special techniques in printed wiring board design and assembly are required. Conductor patterns, lead spacing, part mounting and soldering of leads and hookup wire should follow the criteria defined in the NASA publications on high-voltage design to avoid high localized fields that could overstress the insulation. Component and conductor spacing must be controlled to limit dielectric stress to about 10% of its actual breakdown voltage to account for aging factors, variations in material properties, temperature and outgassing effects and conductor shapes.

If the equipment is to operate at critical pressures, ground shields must be employed to prevent the buildup of strong electric fields on the surface of insulation leading to eventual breakdown of the surrounding gas volume. This gas discharge occurs in both ac and dc circuits and will eventually lead to breakdown of the insulating materials by tracking or treeing and sustained arcing.

Dunbar* presents an equation for the voltage developed across a gas capacitor in series with a solid dielectric that can be used to illustrate how applied voltage is distributed in a dielectric path between an insulated conductor and a bare conductor or gound return path

$$Vg = \frac{V}{\frac{t_s}{t_g}\frac{}{\varepsilon_s} + 1}$$

where

V = applied voltage,

V_g = voltage across the gas gap,

t_s = solid dielectric thickness,

t_g = gas dielectric thickness,

ε_s = dielectric constant of solid,

and dielectric constant of gas is = 1.

For a typical insulating material with $\varepsilon_s = 3$ and $t_s/t_g = 1$, the potential across the gas dielectric Vg is 75% of the total applied voltage. If the t_s/t_g ratio is 0.1, the voltage across the gas dielectric is about 97% of the applied voltage.

Thus, in the P^3 circuits, to avoid electrical discharge of a gas in the critical pressure range we must carefully insulate and shield all high-voltage conductors and components to prevent gas pockets from occurring in places where high electric fields exist and to minimize possibility of gases occurring at critical pressure during operation.

For the dc circuits operating up to 375 volts, we can design for voltage stress levels up to 250 volts applied across the gas volumes, assuming a reasonable degree of contamination control and proper conductor configurations. At higher voltage stress levels, the minimum breakdown voltage level of the gas would be exceeded, resulting in periodic corona discharges and eventual failures.

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*Ibid.

For dc circuits the discharge rate of solid-gaseous dielectrics in series is a function of dielectric constant and resistivity of the materials involved. This can result in low repetition rates for gaseous discharge on the order of one per hour. Because of the possibility of low-rate corona discharge, it is necessary to test for sufficiently long periods to verify design performance. When considering the high-voltage 10-kHz squarewave circuits found in the preregulator power stage base drive and power stage output devices, the lower voltage breakdown potential for air is reduced to 210 volts. Careful insulating and shielding of conductors and circuit elements is even more important here since corona breakdown will be in the form of sustained discharge with rapid degradation of insulating systems.

Adequate venting is very important in designs intended to operate below the critical pressure range. In addition to providing sufficient vent areas in the main enclosure and to avoid high-pressure differentials in subchassis during ascent pressure decay, special provisions must be made to preclude entrapped gases in the component subassemblies, cabling and connectors. Cabling presents a particulary difficult problem since entrapped gas can cause long-term outgassing at cable ends, exposing wire terminations to gases at critical pressure levels. Flaws in the wire jacketing material or damage to insulated wire due to flexing can result in delamination of the insulation layers with entrapment of gas. The gas pocket eventually reaches critical pressure and becomes a likely source for corona discharge and breakdown of the insulating materials.

Connectors are also noted for gas entrapment and must be modified by adding vent holes or selecting high-voltage connectors designed to eliminate voids where trapped gas could exist.

The use of encapsulants and conformal coatings often results in gas bubbles that diffuse down to critical pressures with resulting corona. Special techniques must be used in cleaning surfaces to be encapsulated or coated and the insulating compounds must be degassed and subjected to vacuum prior to curing to eliminate voids.

The design criteria and guidelines for high-voltage design are covered to some degree in several NASA publications issued by Marshall Space Flight Center (MSFC-STD-531, soon to be released), Goddard Space Flight Center (NASA SP-208 and NASA TND-7948), and Jet Propulsion Laboratories (JPL Design requirements, DM509306A). These documents emphasize the need for a thorough development program, strict controls on part and material selection and application, manufacturing process controls and a comprehensive testing program.

D. THERMAL ANALYSIS

The P^3 design utilizes three semiconductor power stages, input/output capacitors and printed wiring boards (PWBs) as listed in Table 3. The temperature requirements of the semiconductor junctions and the temperature of the PWBs are the thermal design drivers. In our thermal analysis we utilized a conservative upper temperature limit of 125°C for the semiconductor junctions and 85°C for the PWBs and parts. The analyses showed that spacecraft application requires the P^3 package to be coldplated because of the high power dissipation of 608 watts.

The five alternative P^3 packaging concepts, the selected baseline approach and a thermal design summary of the baseline configuration are shown in Figure 11. The packaging concepts illustrated consider one and two-level concepts in conjunction with power stage modularity approaches. Each candidate design is coldplate-mounted except configuration 4, which utilizes coldrails. All cases are aluminum and base/coldplate areas vary from 149 cm^2 for configuration 4 to 1988 cm^2 for configuration 5.

Table 3 Programmable Power Processor Part Description and Power

Part Description	Max Power, W
I_{in} Shunt	20
Input Capacitors	15
Output Capacitors	1
Power Stage 1	
Transistor	100
Diode	30
Inductor	13
Resistor	6
Driver Transistor	6
Power Stage 2	
Transistor	100
Diode	30
Inductor	13
Resistor	6
Driver Transistor	6
Power Stage 3	
Transistor	100
Diode	30
Inductor	13
Resistor	6
Driver Transistor	6
Shunt 1	8
Shunt 2	8
Shunt 3	8
Printed Wiring Boards	
Base Drive 1	3
Base Drive 2	3
Base Drive 3	3
Telemetry	12
Control	2
Pulsewidth Modulator 1	5
Pulsewidth Modulator 2	5
Pulsewidth Modulator 3	5
Preregulator	15
dc-dc Converter	10
Postregulator	5
Microprocessor	5
Wiring	10
Total	608

(3)

(1) MSFC-specified.
(2) (PWB Specified Total Power)-(Chassis-Mounted Parts) = 34 W.
(3) Includes 30 watts for chassis mounted transistors.

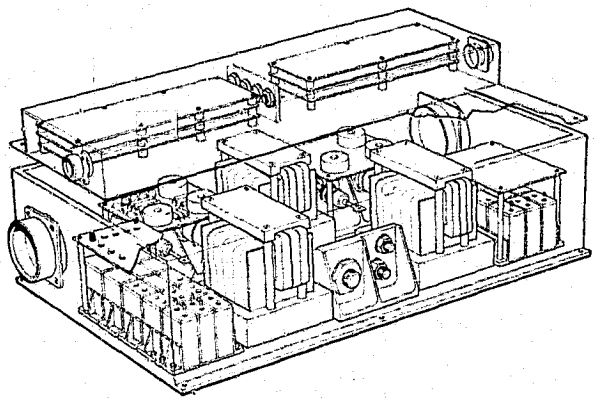
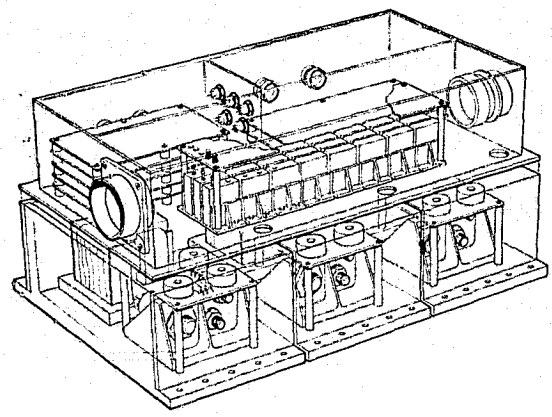
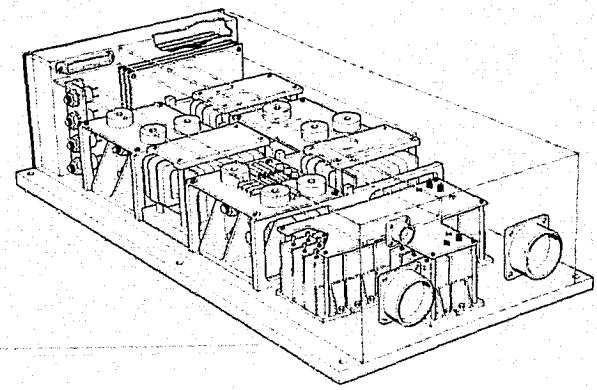
Config	Description	Comments
1		Two-Level-Requires PWB Conductive Cooling
2		Two-Level with Modular Power Stages -Requires PWB Conductive Cooling
3		One-Level - Acceptable Thermal Performance

Figure 11 Alternative Packaging Concepts and Thermal Design Summary

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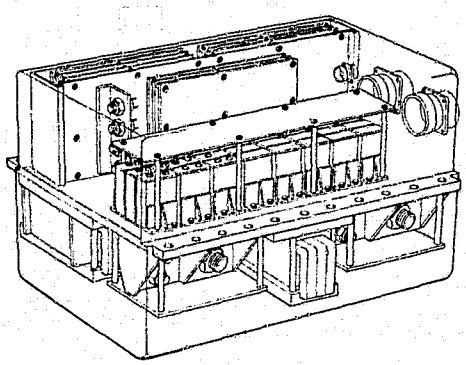
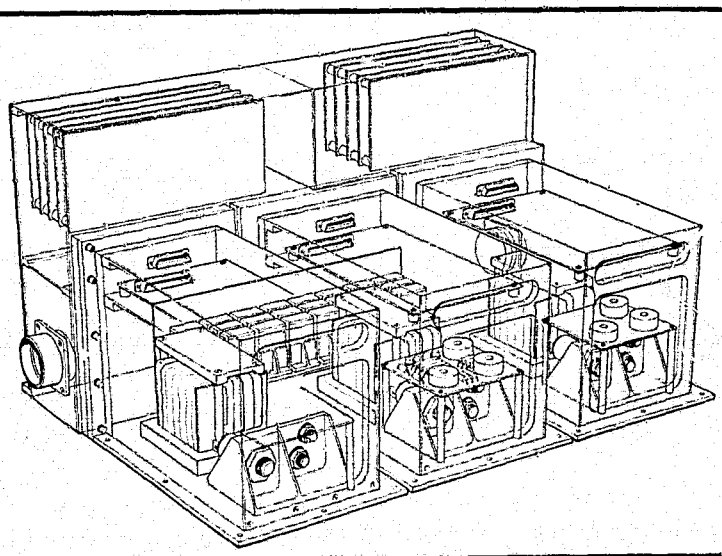
Thermal Design Summary

- MSFC-Specified Parts and Part Powers, 608 W Total
- Semiconductor Electrically Isolated with Cho-Therm Spacers
- PWBs Dissipate Heat by Radiation Only
- Heat Pipes Not Required
- Spacelab-Specified Thermal Filler Between Base and 10°C Coldplate
- No Radiation to External Environment
- Internal Radiation with Surface Emissivity of 0.9
- Average Case Wall Thickness 0.1 in. (0.25 cm), Base 3/16-in. (0.48 cm) Thick

Conf	Description	Comments
4		Coldrails - Not Viable Because of Small Effective Coldplate Area
5		Modular -Plug-In Power Stage Modules; Acceptable Thermal Performance

A computerized thermal math model was constructed for each alternative packaging concept and part temperature predictions were generated. These studies showed that the thermal requirements can be met for all parts for each configuration except configuration 4 (Fig. 1) without the complexity of heat pipes. Configuration 3 has been baselined because of adequate thermal performance and the inherent simplicity of one-level packaging. Configuration 3 also does not require that the PWB's radiation cooling be supplemented by a conduction enhancement approach. The thermal performance of configuration 5 is at least as good as configuration 3 but it was not selected because of the higher fabrication costs and relatively poor weight and volume factors.

Configuration 3 analyses showed that the average temperatures for the case and base are 22.9° and 15.2°C respectively. The peak temperature of 105.7°C occurs for the power stage 2 diode junction and the PWB average temperature is 80°C. Subsequent parametric analyses indicated an adequate thermal design margin.

The thermal analysis task was divided into a preliminary and final phase as shown in Figure 12. The preliminary analysis task considered the five packaging options whereas the final studies concentrated on the thermal performance evaluation of the selected baseline. The preliminary studies utilized a 30-node thermal math model for each option and the final studies a 50-node model. The thermal models are coded for use by the Martin Marietta interactive thermal analysis system (MITAS) computer program.

The thermal conductivities and thermal conductance values used in construction of the thermal models are listed in Table 4. The Transistor D.A.T.A. Book provides the semiconductor junction-to-case thermal conductance, whereas the base-to-coldplate conductances have been obtained from the Spacelab Accommodations Handbook.

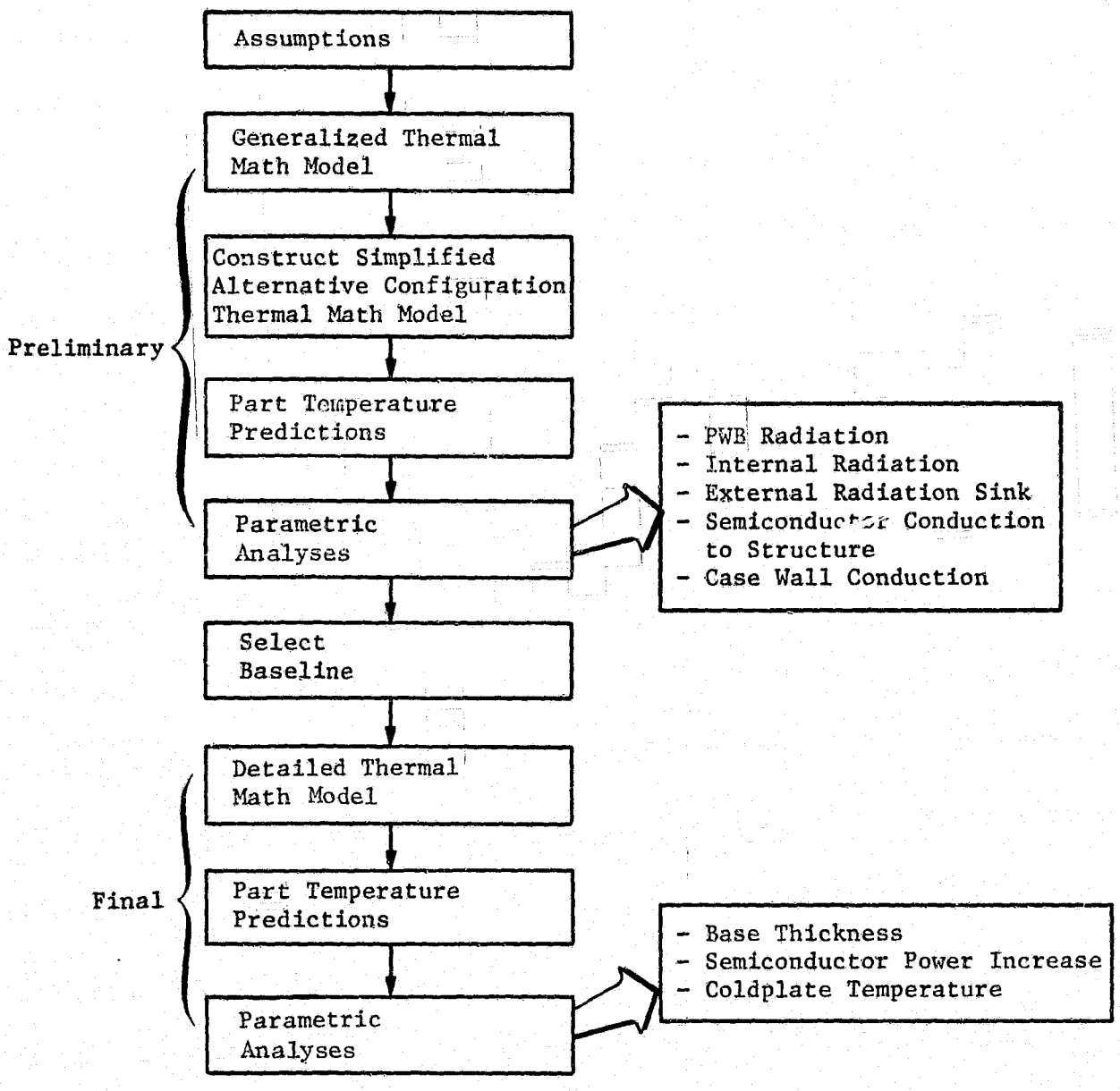


Figure 12 Thermal Analysis Approach

Table 4 Thermal Design Data

Item	Value
Parts/Case	
Aluminum Thermal Conductivity	1.73 W/cm °C
Bolt Thermal Conductance	0.26 W/ °C
Parts/Case Emissivity	0.9
Semiconductors	
Junction-to-Case Thermal Conductance (1)	
Power Transistor (T159)	5.0 W/°C
Driver (T061)	0.5 W/°C
Diode (MR874)	1.25 W/°C
Cho-Therm-R (1671) (2)	
Thermal Conductivity	0.042 W/cm °C
Contact Thermal Conductance	4.55 W/°C
Metal-to-Metal Contact Thermal Conductance at 250 psi	0.45 W/cm^2 °C
Semiconductor Case-to-Structure Calculated Thermal Conductance	
Power Transistor (T159)	2.86 W/°C
Driver & Diode	0.70 W/°C
Coldplate	
Component Surface That Serves as Heat Transfer Area to Coldplate	
Without Filler	6.25 cm^2/Bolt
With Filler (4)	Ail
Thermal Conductance from Component Heat Transfer Area to Coldplate Coolant	
Without Filler	0.15 W/cm^2 °C
With Filler (4)	0.08 W/cm^2 °C

(1) Transistor D.A.T.A. Book, autumn 1975.

(2) Chromerics, Woburn, Mass, 01801.

(3) Spacelab Accommodation Data Book, SLP/2104, June 1977

(4) Cho-Seal 1224 (0.5-mm thick).

1. Part Thermal Models

Part mounting approaches are similar for all options and they have been categorized for the thermal analysis discussions into power stage semiconductors, printed wiring boards and miscellaneous parts.

a. Power Stage Semiconductors - Each power stage consists of three stud-mounted semiconductors as shown in Figure 13. Each semiconductor is electrically hot and insulation is required between the semiconductor case and the mounting structure. A 0.46 mm (18-mil) thick silicone rubber washer (Cho-Therm-R) provides semiconductor case electrical insulation.

The semiconductor mount minimizes the thermal conductance from the semiconductor case to the package base by using a 1.27 cm (0.50 in.) thick aluminum structure. Semiconductor power is dissipated at the semiconductor junction and transferred by conduction to the case. The overall thermal conductance between the case and the mounting structure has been calculated considering the contact thermal conductance and the thermal conductance of the Cho-Therm washer.

b. Printed Wiring Boards - A typical printed wiring board assembly is illustsrated in Figure 14. The PWBs are modeled as a single node that represents the average temperature of outer boards. Inner boards are assumed to have negligible power dissipations. Heat is dissipated from the PWBs by radiation to the local environment and conduction to the case through the mounts. Low PWB power density can result in an adequate design that dissipates heat only by radiation. High PWB power density may require conductive heat loss to maintain an acceptable temperature. The PWBs are typically manufactured of low thermal conductivity material and conductance enhancement schemes are often required. An aluminum plate (0.05 cm thick assumed) bonded to the board can be used to enhance conduction from the boards to the case.

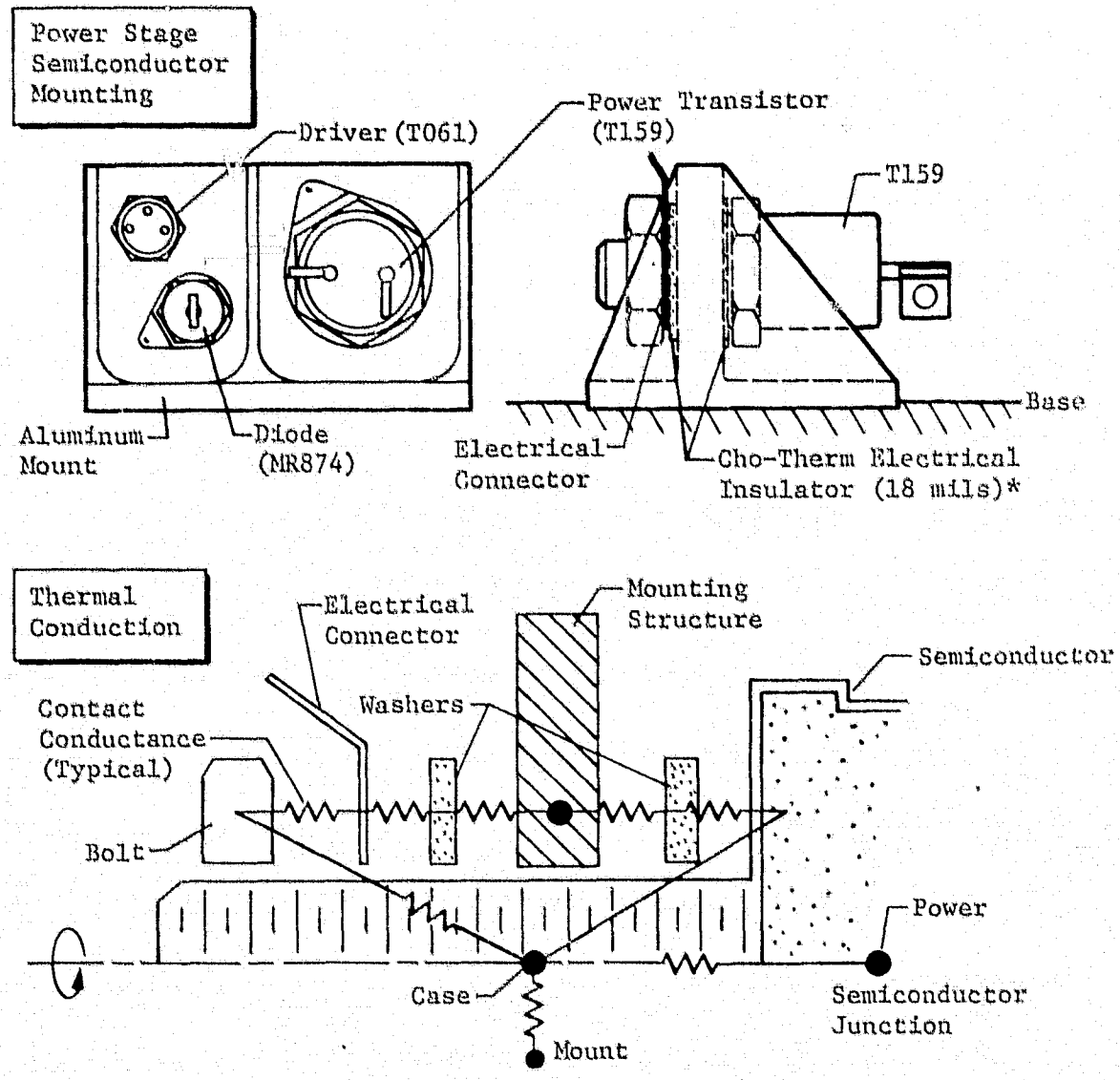


Figure 13 Semiconductor Mounting Configuration

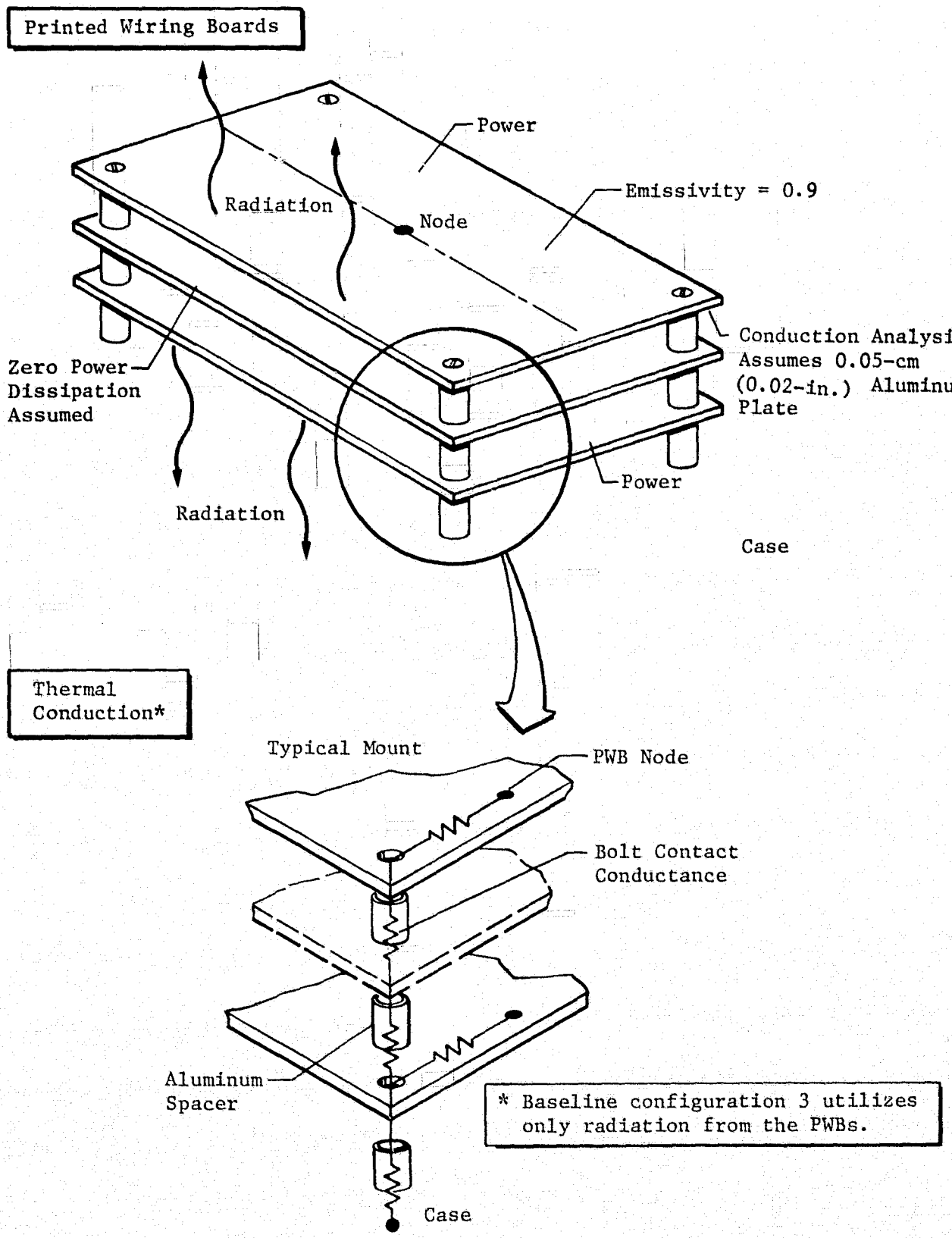


Figure 14 Printed Wiring Board Typical Mounting Configuration

In calculation of the overall thermal conductance from the PWB to the case we considered the bolt and aluminum spacer effects. Both radiation and radiation/conduction PWB heat rejection approaches have been evaluated.

c. Miscellaneous Parts - Other than semiconductors and PWBs, most of the parts are mounted as depicted in Figure 15. The parts are modeled as a single node and radiative and conductive heat losses are considered. Part thermal conduction considered the bolt conductance between the part mounting flange and the base as indicated. Analysis has shown that a thermal filler is not required between any part and the mounting structure.

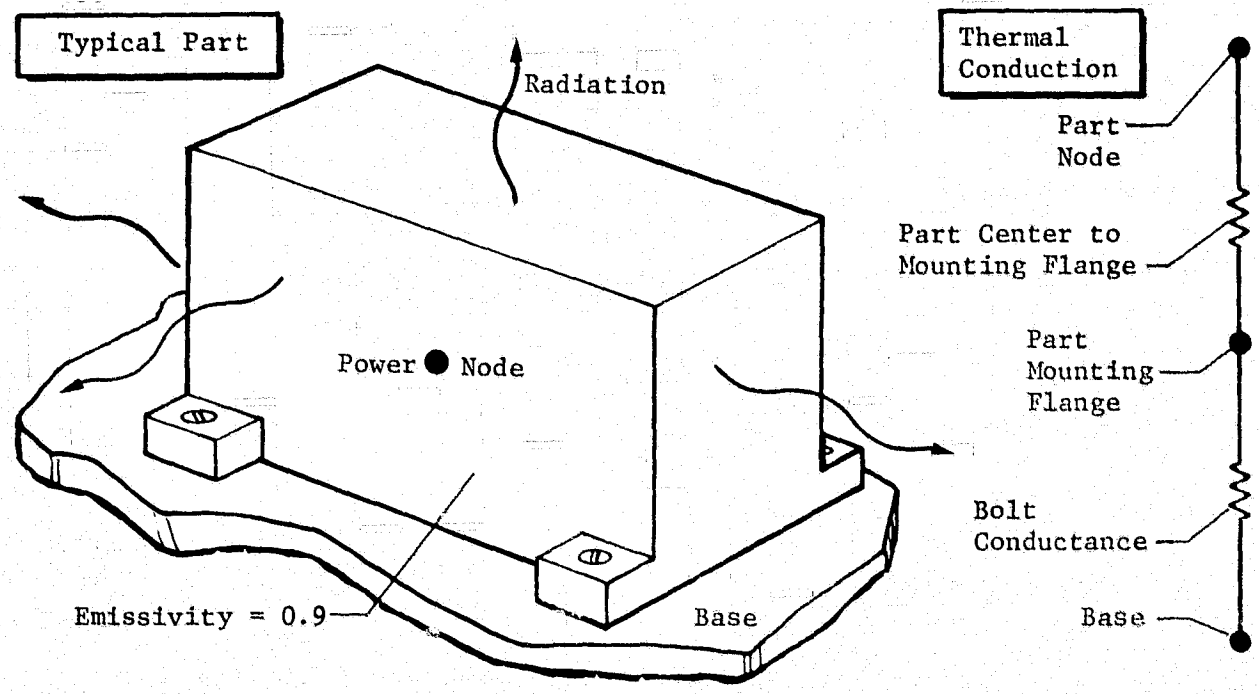


Figure 15 Part Typical Mounting Configuration

2. Configuration Thermal Models

All package options utilize the same parts and to facilitate the analysis a generalized model has been developed to serve as a common starting point. The generalized P^3 model nodal arrangement is illustrated in Figure 16. The P^3 case is represented by three nodes and each part has been represented as a single node. Radiation and conduction couplings calculated for each P^3 configuration have been used to update the generalized model to represent each packaging option.

A simplified radiation analysis approach has been used where individual radiation couplings between nodes are replaced by a single coupling to an effective radiation node (ERN). In the thermal math model, the ERN is an arithmetic node that assumes a temperature representing a coupling-weighted-average of the surface temperatures of the enclosure.

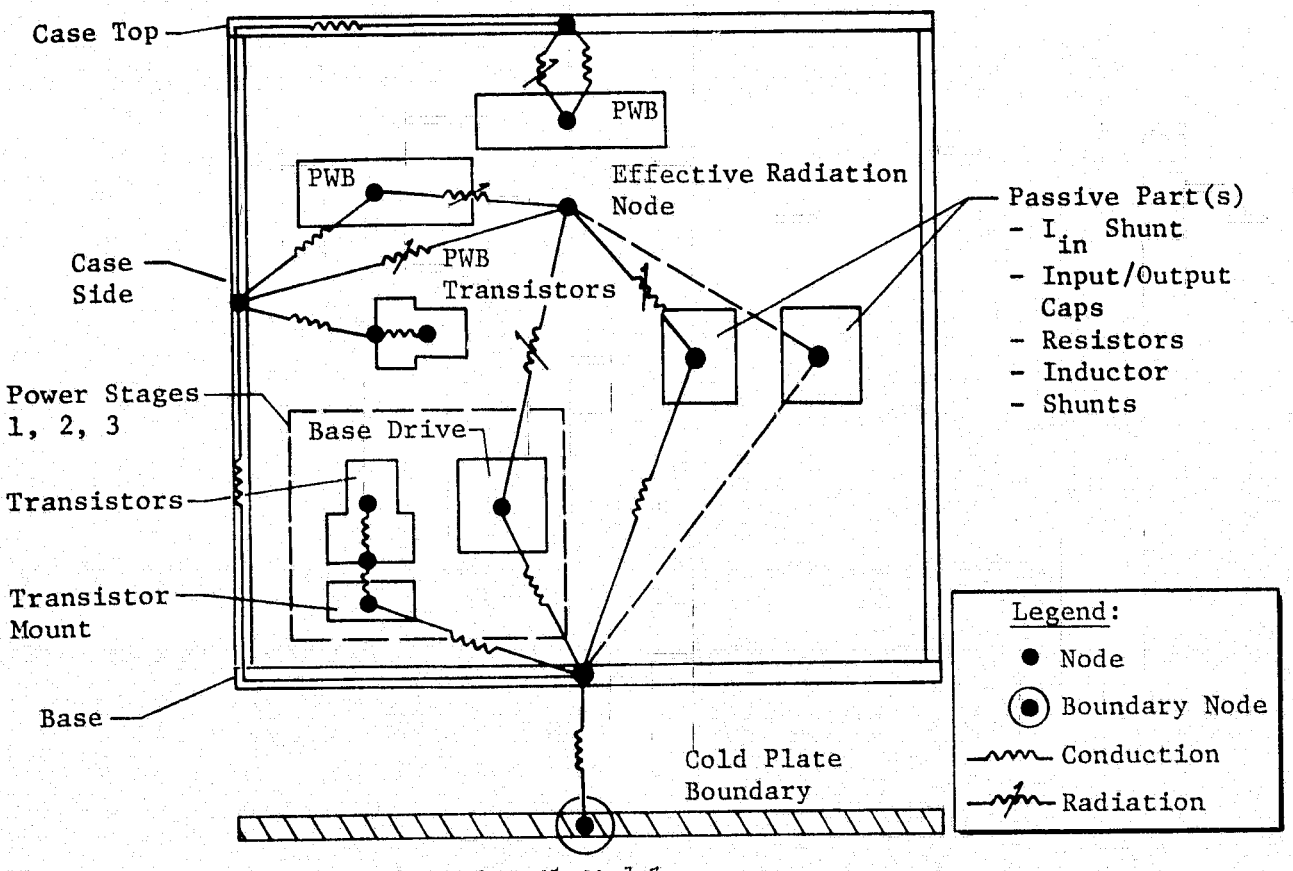


Figure 16 Generalized Thermal Math Model

The results of the preliminary studies presented in subsection 3 were used in the selection of configuration 3 as our baseline packaging concept. The configuration 3 thermal math model was derived from the preliminary model by increasing the number of nodes used to represent the case. The case nodal breakdown was increased from 2 to 10 nodes and the base from 1 to 9 nodes.

3. Analysis Results

Part temperature predictions for normal operations and selected parametric studies are discussed in the following subsections.

a. Thermal Performance of Configurations 1 through 5 - Part temperature predictions are presented in Table 5 for configurations 1 through 5 where temperatures are listed for six

Table 5
Part Temperature Predictions for Configurations 1 Through 5

Part Description	Temperature, °C				
	Configuration (1)				
	1	2	3	4	5
Input Caps	21.7	50.6	21.1	60.0	20.6
Output Caps	16.7	45.0	15.6	55.0	15.6
Diode Junction	100.6	102.2	100.6	166.7 (2)	100.0
Inductor	22.8	25.0	21.7	60.6	21.1
PWB	56.1	61.7	55.0	98.3 (3)	38.3
Base Drive (PWB)	29.4	38.3	22.8	61.7	31.1
Average, Part (4)	24.4	35.0	21.7	61.1	23.3
Average, Case	32.2	36.1	41.4	63.7	18.3

(1) Simplified Thermal Math Models,
608 W Total Power,
PWB Dissipates Heat by Radiation and Conduction,
Spacelab Filler Between Base and 10°C Coldplate,
No External Radiation, Internal Emissivity = 0.9.
(2) Exceeds Selected Upper Limit of 125°C
(3) Exceeds Selected Upper Limit of 85°C
(4) All Parts Except Semiconductors and PWBs.

representative parts. The six selected parts include the thermal design drivers, i.e., the diode junction and the PWB. Conservative upper temperature limits of 125° and 85°C were selected for the semiconductor junction and the PWB respectively; an 85°C upper temperature limit has been used for all other parts. The average part temperature presented was calculated using the area-weighted temperature of all parts other than semiconductors and PWBs. The average case temperature was similarly calculated using the area-weighted temperatures of the case top and sides.

The analysis results presented in Table 5 show that all parts are within temperature limits for all options except configuration 4. Configuration 4 was eliminated from further consideration because the diode and the PWBs exceed their upper temperature limits. Note that the optimal PWB thermal design approach that utilizes both radiation and conduction was considered in the part temperatures presented in Table 5.

The effects of PWB radiation/conduction cooling on PWB temperatures are presented for the four viable P^3 configurations in Table 6. Temperature predictions are presented for the PWB and base drive (also a PWB) for radiation cooling and for radiation plus conduction cooling. The results show that radiation cooling is adequate for all configurations except 1 and 2. The PWBs are located on the case top level, that is removed from the coldplated base. Conduction cooling reduces the PWB temperature from 92.8 to 56.1°C for configuration 1 and from 95.0 to 61.7°C for configuration 2. An alternative design approach would be to reduce the power density by increasing the area.

Configuration 3, a one-level packaging concept, was selected for further thermal analysis because of its inherent simplicity, low cost and acceptable thermal performance. The following parameters that affect thermal performance of the P^3 package have been investigated:

Table 6
Printed Wiring Board Radiation/Conduction Analysis Results

Part Description	Heat Rejection Mode	Temperature, °C			
		Configuration			
		1	2	3	5
PWB	Radiation (3)	92.8 (3)	95.0 (3)	72.2	58.3
	Radiation (1) & Conduction (2)	56.1	61.7	55.0	38.3
Base Drive	Radiation (1)	65.0	70.6	61.1	60.6
	Radiation (1) & Conduction (2)	29.4	38.3	22.8	31.1

(1) Radiation from outer surfaces, emissivity = 0.9

(2) Conduction assumes 0.02-inch aluminum plate bonded to PWB.

(3) Above 85°C upper limit.

1) Internal case radiation;

2) External radiation sink;

3) Semiconductor conduction to structure;

4) Case wall conduction.

Even though these studies are for configuration 3 the results apply to all viable package options because of design similarities.

b. Internal Case Radiation - The analysis results presented in Table 7 show the effect of internal radiation on part temperatures. Part temperatures are changed by 1°C or less by elimination of internal radiation for all listed parts except the PWB and base drives. The analysis results without radiation correspond to a zero thermal emittance part surface. A high-emittance part coating, though not a major thermal design factor for normal operation, provides a margin for contingencies or failed mode operations and is recommended.

Table 7
Part Temperature Predictions As a Function of Internal Case Radiation

Part Description	Temperature, °C	
	Configuration	
	With Internal Radiation	Without Internal Radiation
Input Caps	21.1	20.6
Output Caps	15.6	15.0
Diode Junction	100.6	100.6
Inductor	21.7	21.7
PWB	55.0	86.7
Base Drive	12.8	22.8
Average, Part	21.7	21.7
Average, Case	23.3	22.2

(1) Simplified thermal math model,
608 W total power,
PWB dissipates heat by radiation and conduction,
Spacelab filler between base and 10°C coldplate,
No external radiation, internal emissivity = 0.9.

c. External Radiation Sink - All thermal analyses have assumed that the P^3 package is thermally insulated from the environment. A study was completed to determine the effect of an external radiation environmental thermal sink on P^3 temperatures. Critical part temperatures are presented as a function of the radiation environment temperature in Figure 17 where the radiation sink has been varied from -20 to 80°C. The analysis results show that even though the average case temperature is increased from 13 to 47°C, the average part and diode junction are changed by less than 2°C over the environmental temperatures considered. The PWB temperature is acceptable at 70°C when the radiation environment is 80°C. Even for a high-emittance case, part temperatures are not a strong function of the external radiation environment.

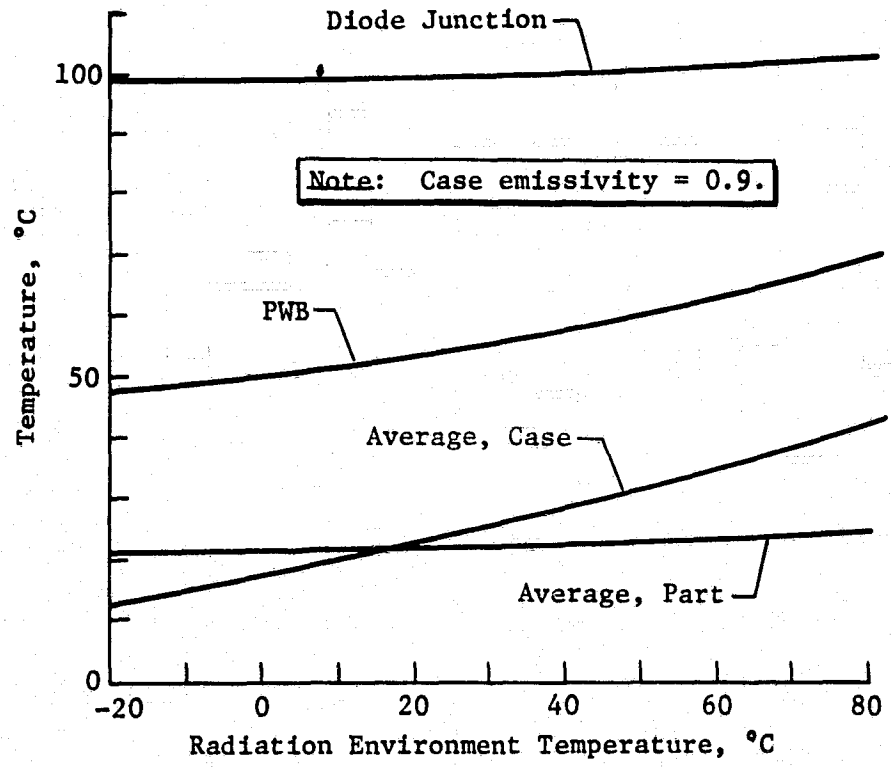


Figure 17
Part Temperature As a Function of External Radiation Sink, Configuration 3

d. Semiconductor Conduction to Structure - All semiconductor cases are electrically isolated from the structure using a Cho-Therm silicon rubber washer. A parametric study was completed to determine the sensitivity of the diode junction and part temperatures to changes in the semiconductor case-to-structure thermal conductance.

Analysis results are presented in Figure 18 where part temperatures are shown as a function of the change in semiconductor case-to-structure thermal conductance. Parts other than the semiconductor junction are unaffected because a semiconductor case-to-structure coupling is changed from -25 to +25% of nominal. The diode junction temperature increases from 100 to 114°C.

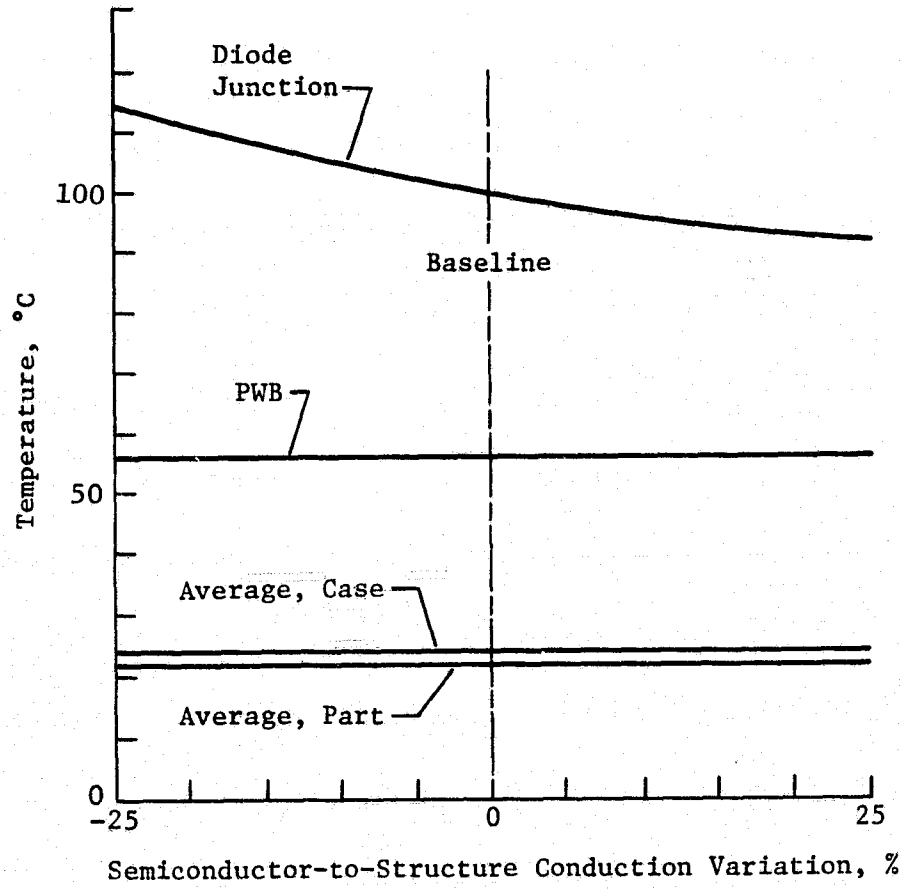


Figure 18
Part Temperature As a Function of Semiconductor Case-Structure Conduction, Configuration 3

Hardware development of a P^3 package would require testing to determine the actual semiconductor case-to-structure thermal conductance.

e. Case Wall Conduction - Case wall thermal conduction is an important design parameter because of the direct effect the case thickness has on P^3 weight. Part temperatures are presented as a function of variation in case wall conduction in Figure 19. Case wall thermal conductors are a function of the conductivity of the wall material and the number of case bolts. A $\pm$50% change in case thermal conductors results in a maximum temperature change of $10^{o}C$ for the PWB. The studies show that a nominal 0.25 cm (0.10 in.) case wall provides an acceptable thermal design with adequate margin.

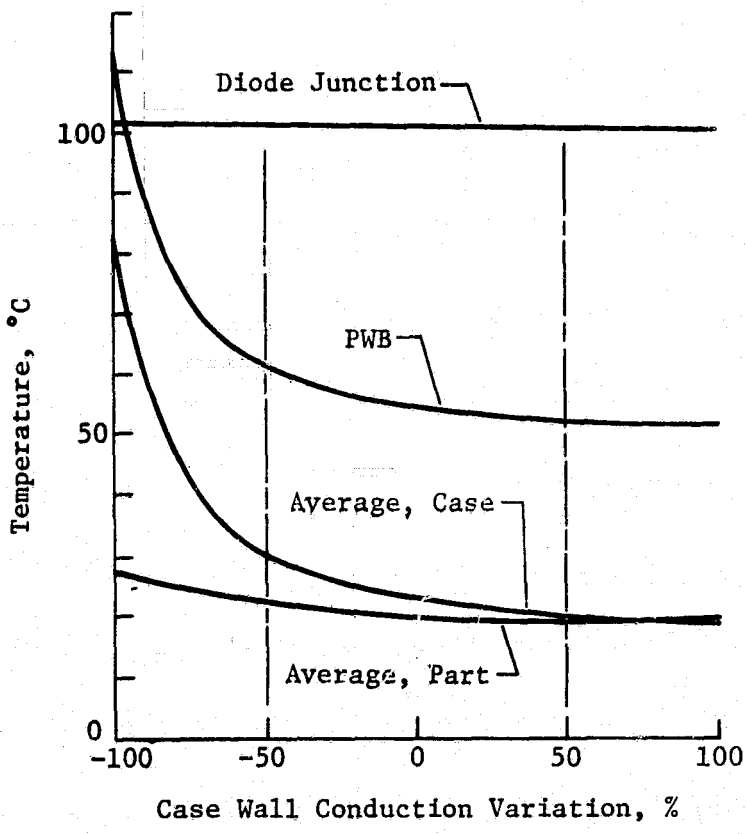


Figure 19
Part Temperature As a Function of Case Wall Conduction, Configuration 3

f. Configuration 3 Thermal Performance - Configuration 3 was selected as our baseline and the final analysis results are presented in Figure 20. The baseline design uses a thermal filler between the base and the coldplate and the nominal base thickness is 0.48 cm (0.19 in.).

The following parametric studies have been completed using the final configuration 3 thermal model:

1) Base thickness;
2) Semiconductor power increase;
3) Coldplate temperatures.

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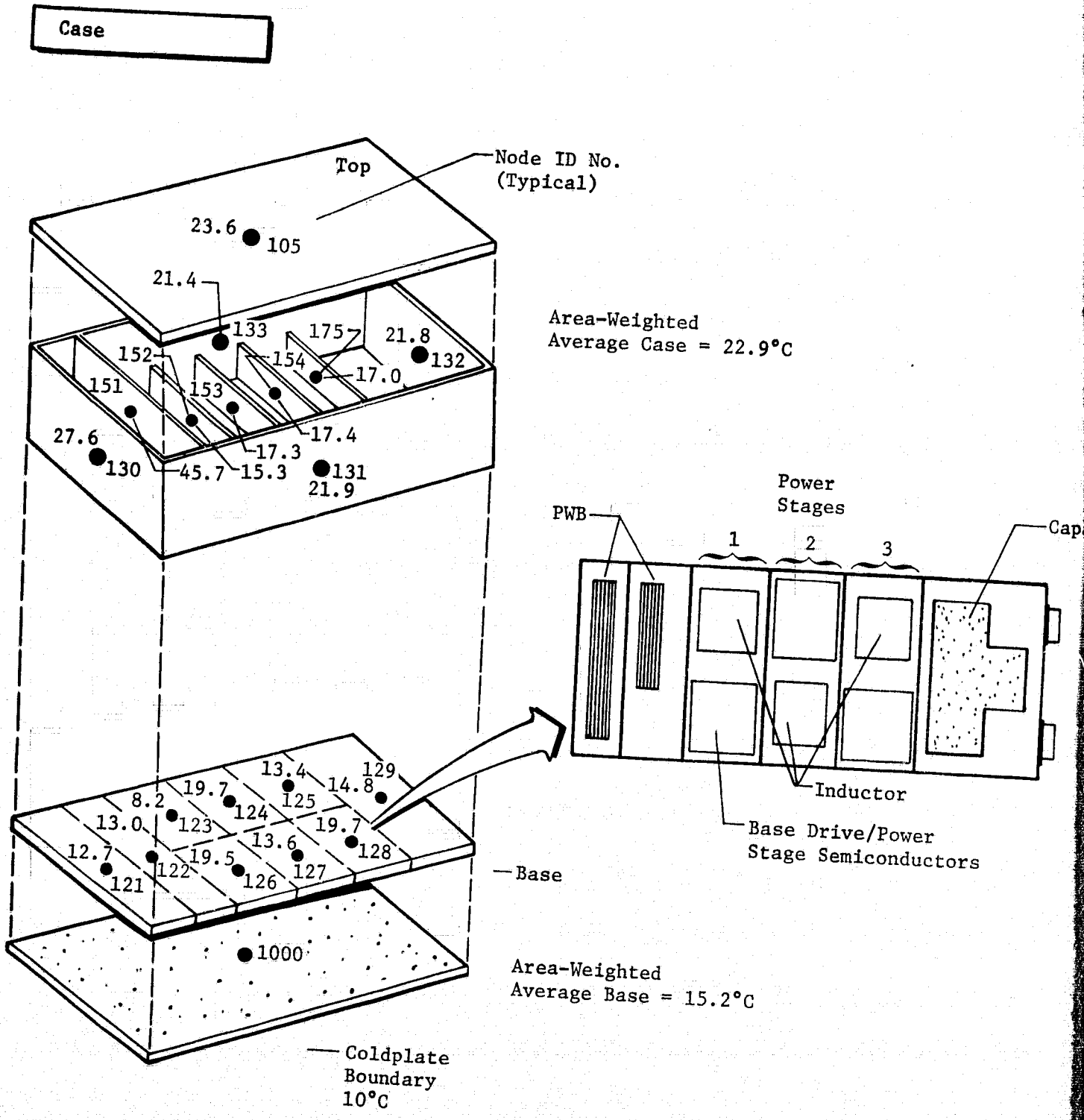

Figure 20 Temperature Predictions for Baseline Configuration 3

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PARTS

Part Description	Max Power, W (1)	Node Identification Number	Temperature, °C (2)
I_{in} Shunt	20	1	52.2
Input Caps	15	2	21.8
Output Caps	1	3	66.7
Power Stage 1			
Transistor	100	10/610 (3)	73.5/93.5 (3)
Diode	30	11/611 (3)	81.5/105.5 (3)
Inductor	13	12	21.3
Resistor	6	13	35.7
Drive Transistor	6	14/04 (3)	47.0/59.0 (3)
Power Stage 2			
Transistor	100	20/620 (3)	73.7/93.7 (3)
Diode	30	21/621 (3)	81.7/105.7 (3)
Inductor	13	22	21.6
Resistor	6	23	36.1
Drive Transistor	6	24/624 (3)	47.3/59.3 (3)
Power Stage 3			
Transistor	100	30/630 (3)	73.7/93.7 (3)
Diode	30	21/631 (3)	81.8/105.8 (3)
Inductor	13	12	21.5
Resistor	6	33	35.7
Drive Transistor	6	34/634 (3)	47.3/59.3 (3)
Shunt 1	8	4	30.0
Shunt 2	8	5	30.0
Shunt 3	8	6	30.0
Printed Wiring Boards			
Base Drive 1	3	15	62.2
Base Drive 2	3	25	62.2
Base Drive 3	3	35	62.2
Telemetry	12	702	80.0 (5)
Control	2		
Pulsewidth Modulator 1	5		
Pulsewidth Modulator 2	5		
Pulsewidth Modulator 3	5		
Preregulator	15		
dc-dc Converter	10		
Postregulator	5		
Microprocessor	5		
PWB Chasis Mounted Transistors (6)	30	55/655 (3)	52.9/62.9 (3)
Wiring	10		
Total	608		

(1) MSFC-specified.

(2) Detailed thermal math model.

(3) Semiconductor case junction.

(4) (PWB specified power)-(chasis-mounted parts) = 34 W.

(5) PWB radiation only.

Base Thickness - Part temperatures as a function of base thickness are presented in Figure 21. The results show that part temperatures are a weak function of base thickness when a thermal filler is used between the base and the coldplate. Bolting the base (0.48 cm thickness) to the coldplate without filler and using 36 bolts results in a diode junction temperature of 170°C. In fact analysis has shown that application of 72 bolts still results in diode temperatures above 125°C. A thermal filler between the base and coldplate has therefore been baselined.

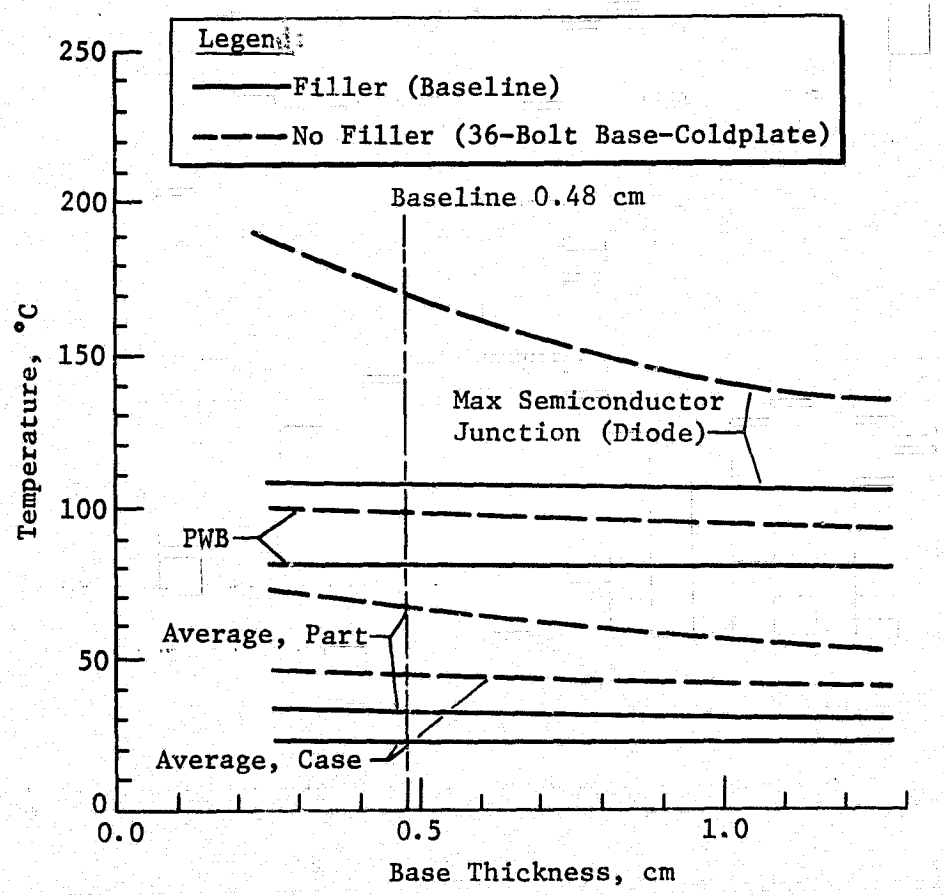


Figure 21
Part Temperature As a Function of Baseplate Thickness

Semiconductor Power Increase - Part temperature as a function of power stage total power is presented in Figure 22. The nominal power stage total power (three power stages) is 408 watts and the analysis showed that a 20% power increase results in a diode junction temperature at the upper temperature limit of 125°C. Average part and case temperatures changed by less than 1°C.

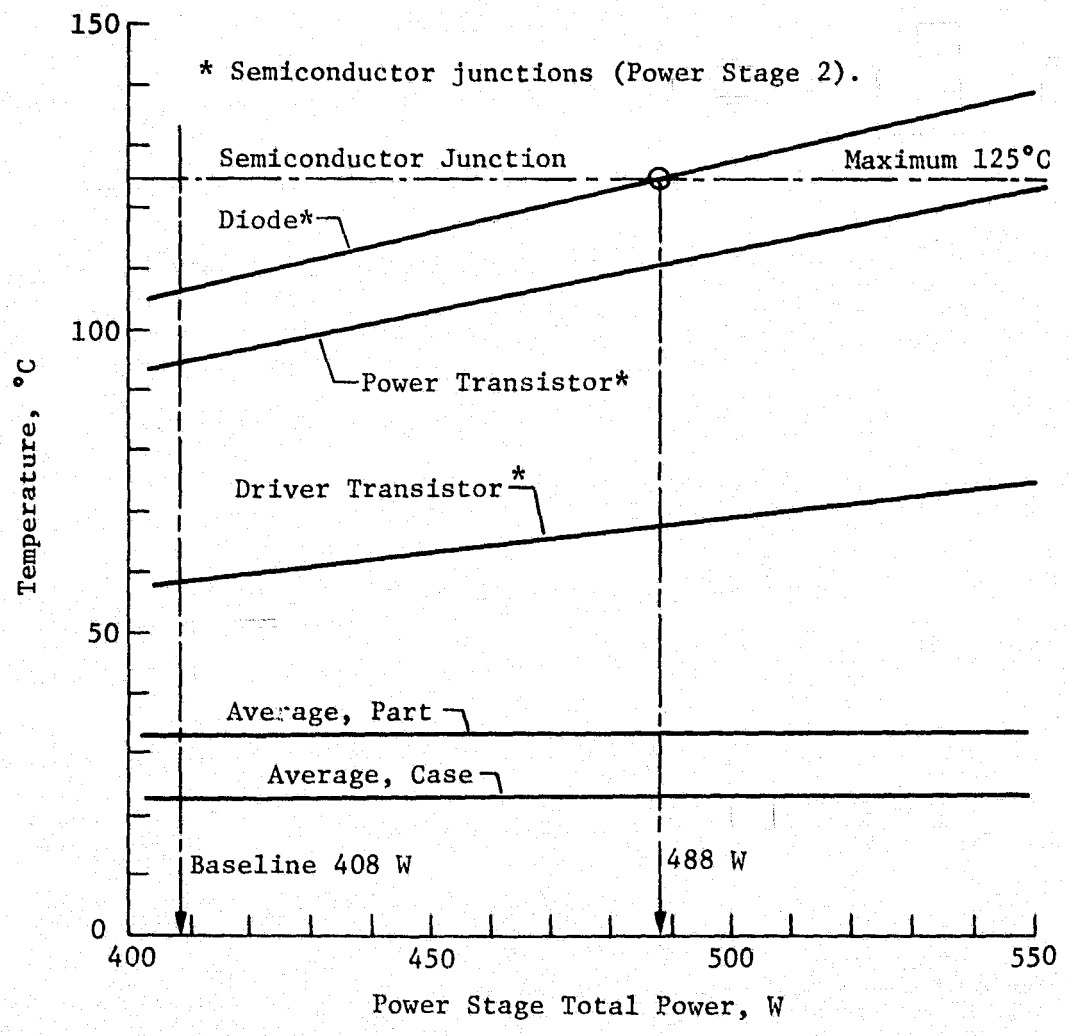


Figure 22
Part Temperature As a Function of Semiconductor Power Increase

Coldplate Temperature - All thermal studies presented in this report have assumed a 10°C coldplate mounted to the P^3 base. Analyses have been completed to determine part temperatures as a function of coldplate temperature and the results are presented in Figure 23. The analysis shows that the coldplate temperature can be increased from 10 to 17.6°C before the radiation-cooled PWB reaches the upper limit of 85°C. The diode junction reaches the upper temperature limit of 125°C at a coldplate temperature of 28.4°C.

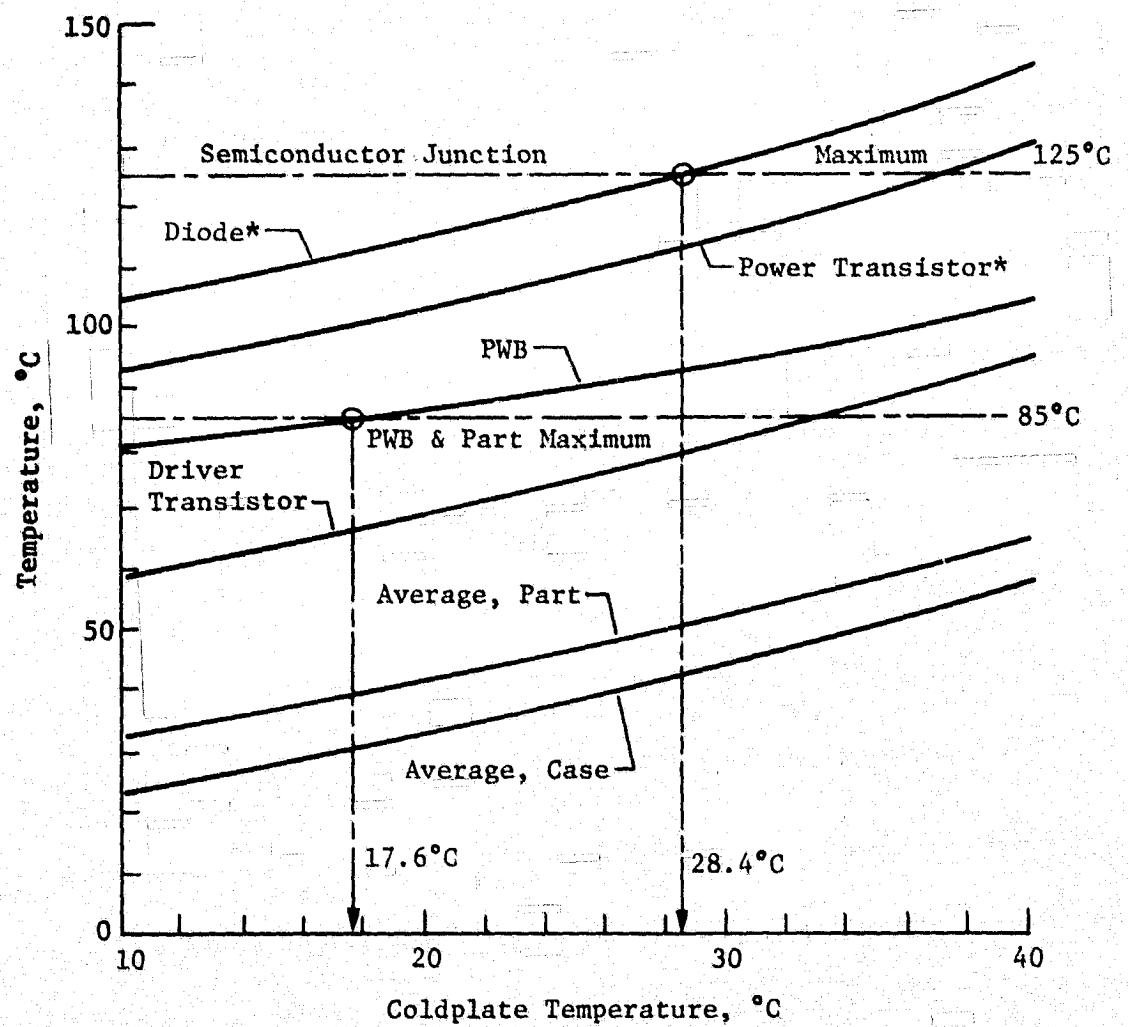


Figure 23
Part Temperature As a Function of Coldplate Temperature, Configuration 3

III. CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

This conceptual study has shown that conventional techniques are acceptable for packaging the programmable power processor if sufficient heat transfer area is provided at the assembly-coldplate interface and adequate thermal conductance is achieved in mounting the major heat-dissipating components. Of the five configurations examined, four are considered acceptable in thermal performance. The coldrail approach was eliminated from consideration because of the high part temperatures resulting from inadequate heat transfer area at the mounting interface.

It became apparent early in the design study that controlling thermal resistance of the part and assembly mounting interfaces was of major importance in achieving acceptable part temperatures. The placement and structural support for the high-heat-dissipating components provide good thermal conduction to the coldplate interface so that heat pipes, useful in some designs for reducing thermal gradients, were not beneficial in the P^3 application. The additional heat pipe interface resistances negate the advantages in improved heat conduction that heat pipes offer. The study also shows that for all viable packaging approaches, a thermal filler is required between the P^3 base and the coldplate to take advantage of conduction over the entire base area interface.

Configuration 3 (Fig. 5) was selected as the best overall packaging approach on the basis of its potential for cost advantage over other design approaches, its acceptable thermal performance and its reasonable size and weight potential. It features an uncomplicated single-enclosure approach with good structural and thermal load paths for the larger components, and has a good potential for adequate EMI control and maintainability.

The parametric thermal studies have shown a design margin of about 20% with regard to maximum P^3 power and, with enhanced thermal conduction from the circuit board assemblies, the design will allow an increase in maximum coldplate temperatures to about 28°C at the specified maximum power levels before the power semiconductor junction temperature limits are reached.

High-voltage considerations examined in this study have indicated a strong relationship between the high-voltage design approach and program costs. Weight and size are not greatly influenced by the approach taken for high-voltage protection. In all cases, special care must be taken to prevent electrical breakdown failures. However, if P^3 operation can be restricted to environmental pressures above or below the critical pressure range of, say, 200 to 10^{-4} torr, the development, fabrication and testing costs will be significantly reduced.

B. RECOMMENDATIONS

The detailed packaging design for the power processor should be generally configured as shown in Figure 5, with emphasis on reducing part mounting thermal interface resistance. The assembly must be mounted to a coldplate using a thermal filler to achieve a conductance of 0.08 watt/cm^2°C or better at the base coldplate interface. Major power dissipating components should be mounted directly to base structure, using electrical insulators for isolation if required. Insulators must have proven heat transfer characteristics and be selected for efficient thermal performance as well as favorable electrical characteristics.

For EMI control the susceptible circuits should be housed in a compartmented subchassis and shielded from the high-level ac circuits. Internal connector interfaces are recommended between the subchassis-mounted circuits and the main assembly components to facilitate production testing, assembly and maintenance.

High-level switching circuits should be shielded for EMI control, with consideration given to shielding component assemblies as wel as cabling. Configuration 3 provides for a removable structure located above the power stages and capacitor banks to support, segregate and shield conductors inside the enclosure. The detailed design must consider methods of providing these functions without obstructing access to the base-mounted components for troubleshooting and repair.

To reduce the development and manufacturing costs, the P^3 operational criteria should include a restriction on operation within the critical pressure range of 200 to 10^{-4} torr. If this restriction is incompatible with mission requirements, an approach that tolerates nondestructive corona discharge for limited periods is recommended. The detailed design must provide adequate venting of all high-voltage assemblies, wiring and component mounting configurations unless void-free encapsulating techniques are employed. If corona-free operation at critical pressures is an operational requirement, a more comprehensive packaging development and testing program will be necessary to assure design adequacy and to verify production methods.

APPENDIX A

P^3 CONFIGURATION LAYOUTS AND PARTS LIST

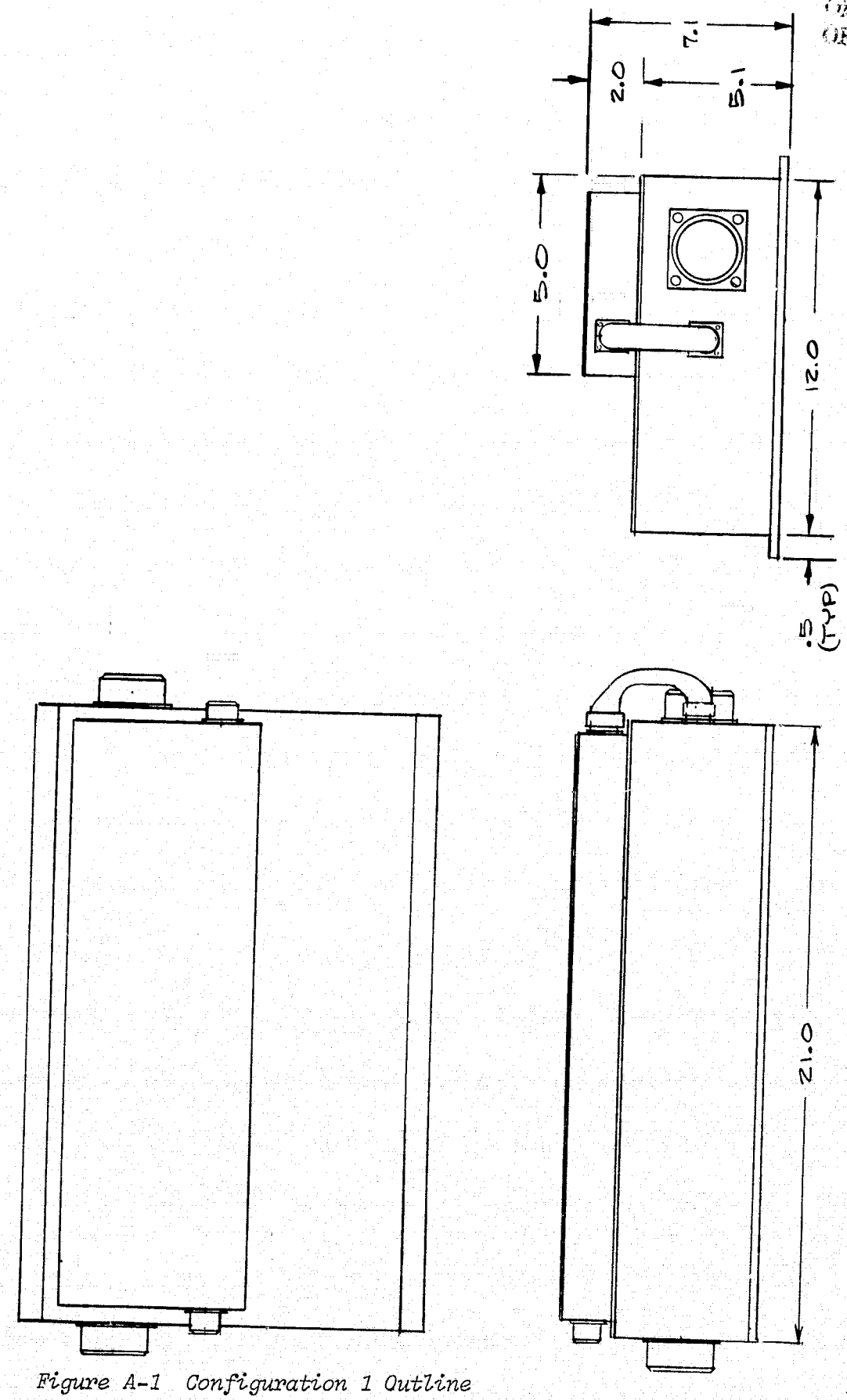


Figure A-1 Configuration 1 Outline

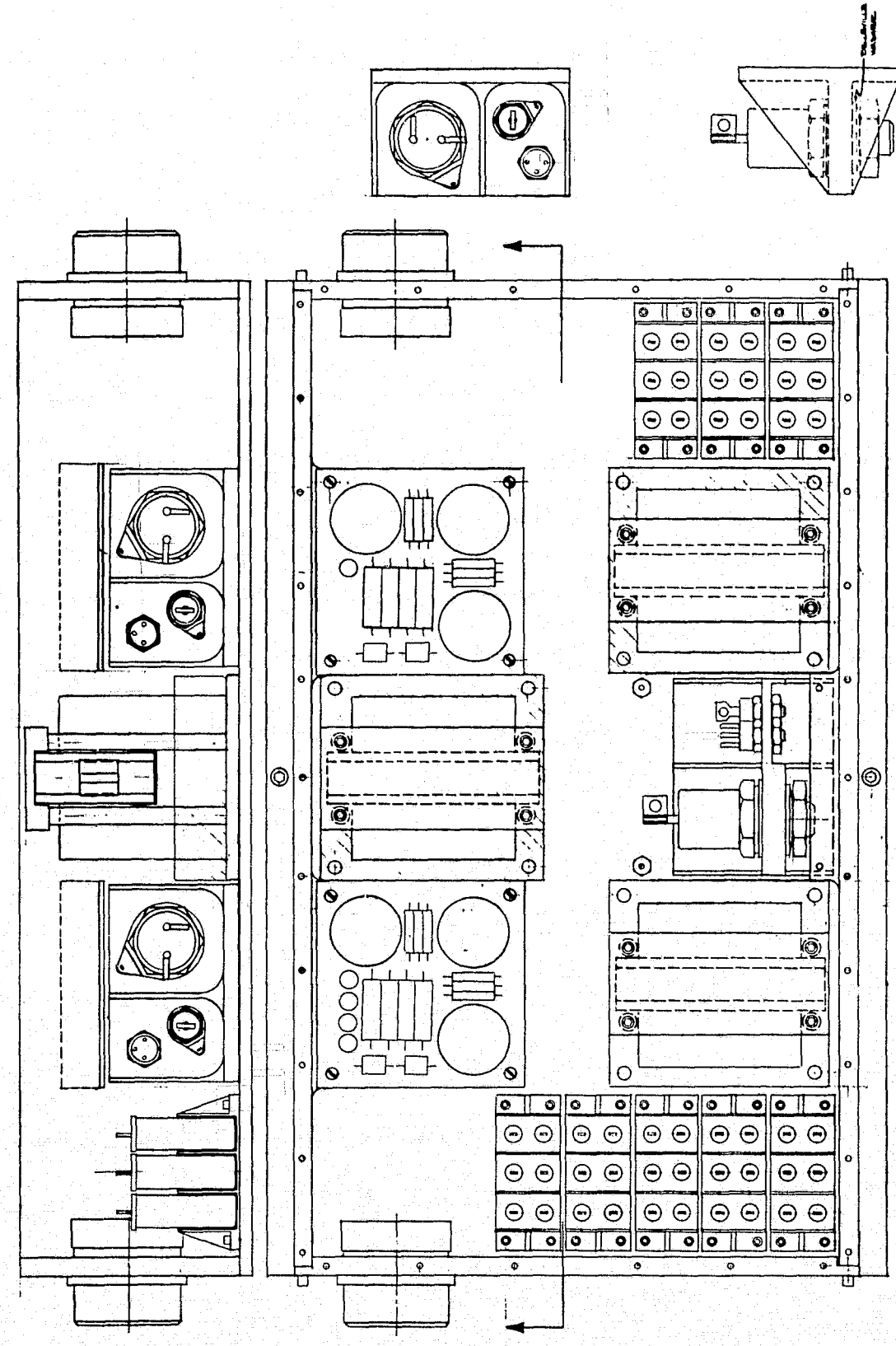


Figure A-2 Configuration 1 Layout

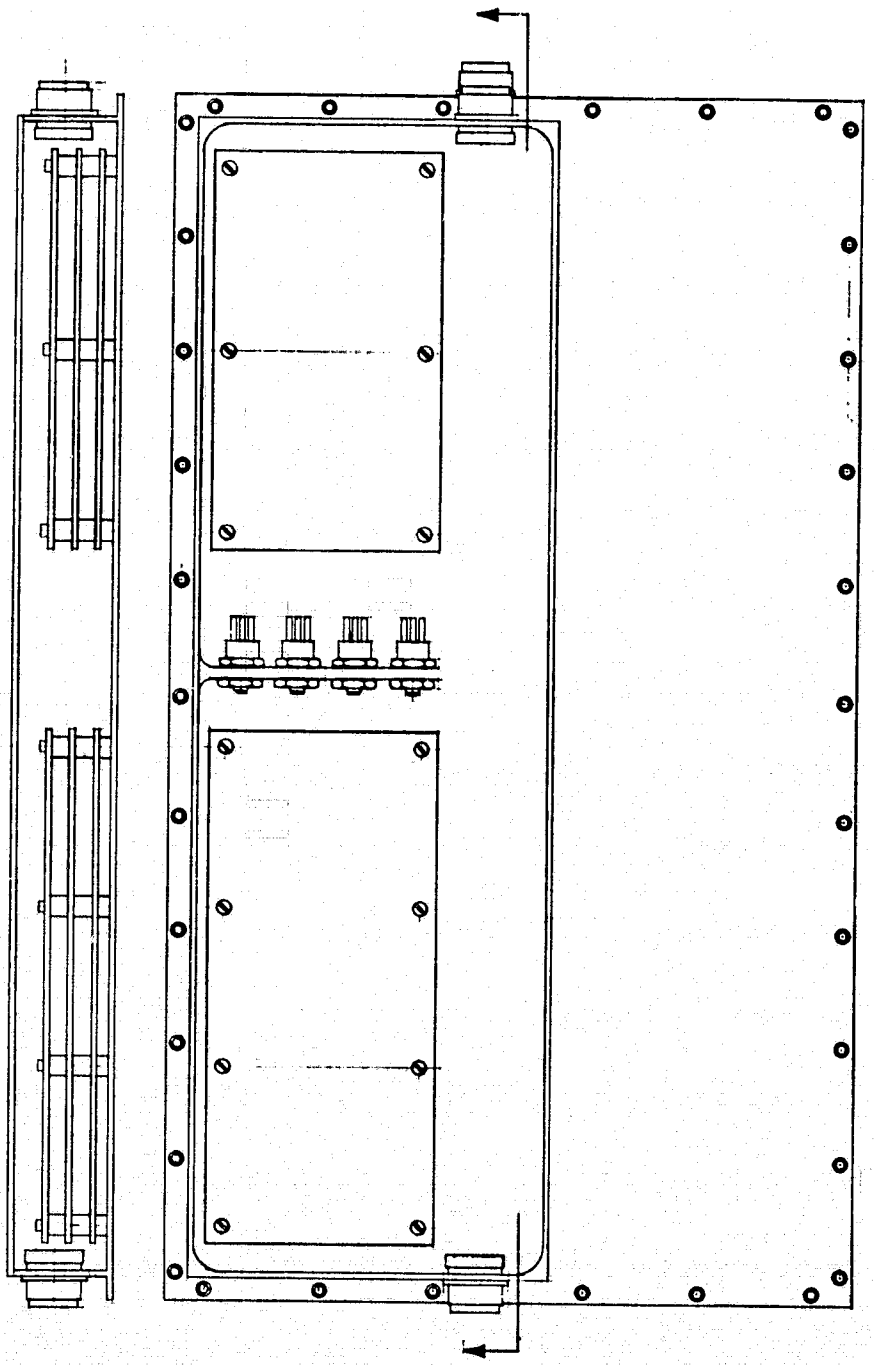
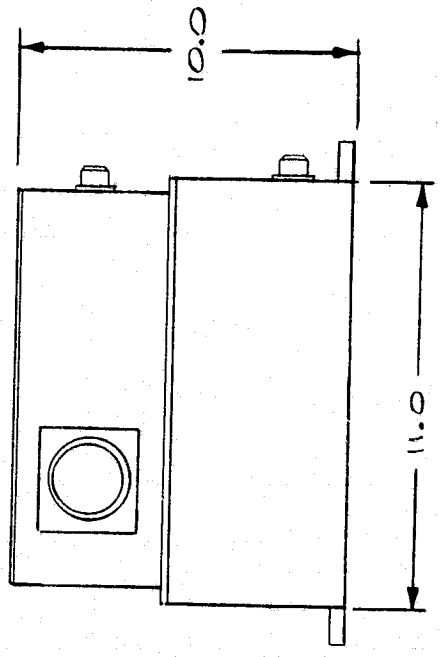


Figure A-3 Configuration 1 Upper-Level Layout



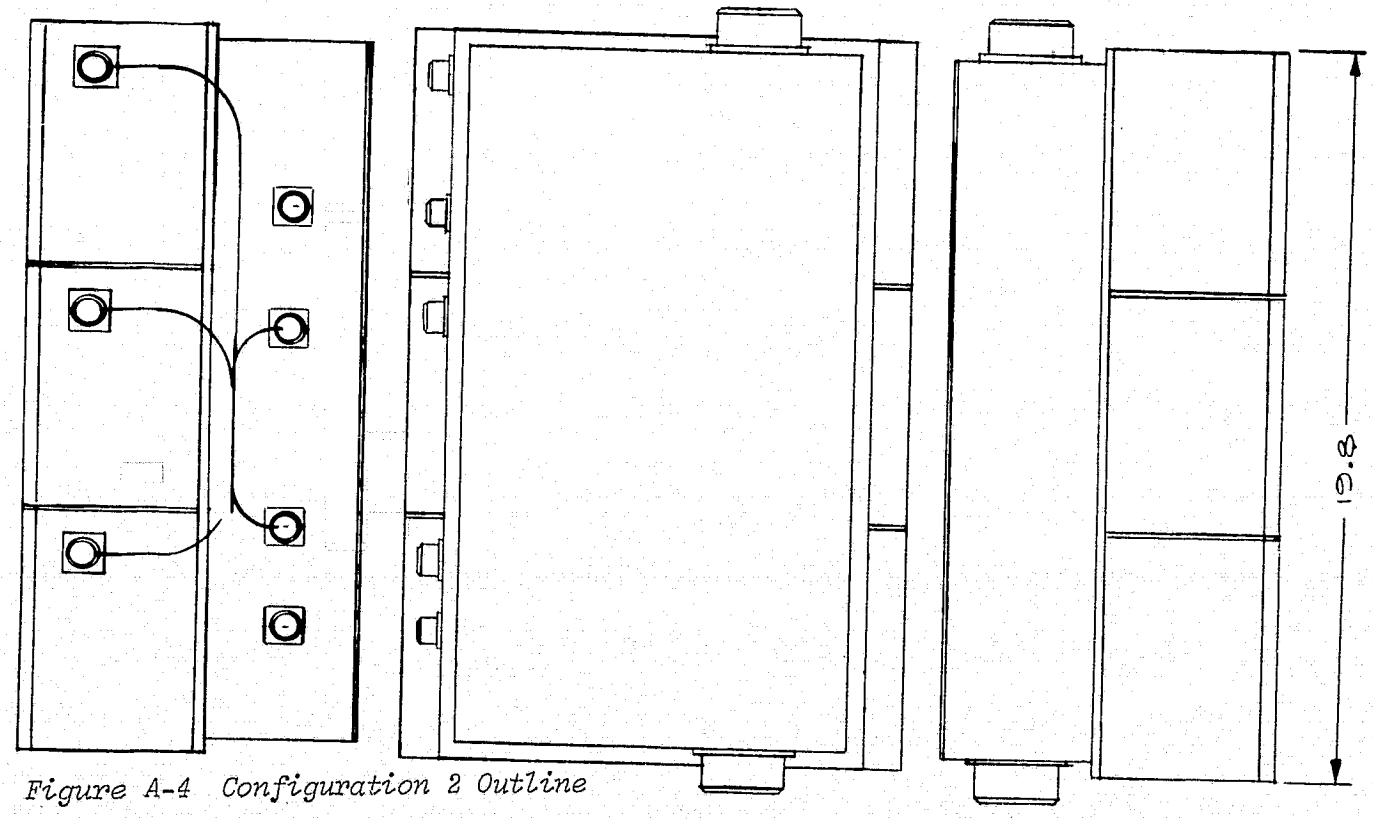


Figure A-4 Configuration 2 Outline

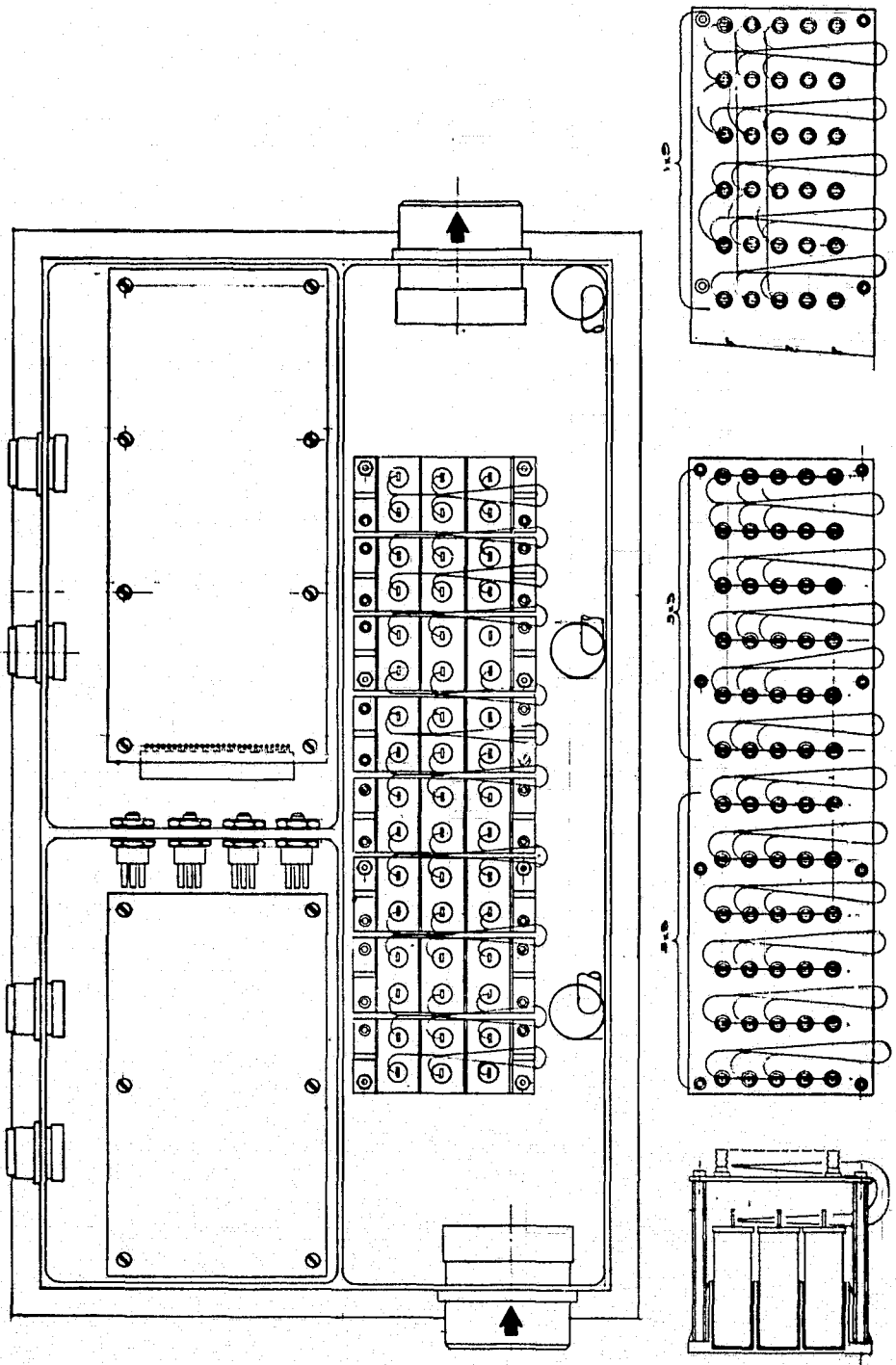


Figure A-5 Configuration 2 Upper-Level Layout

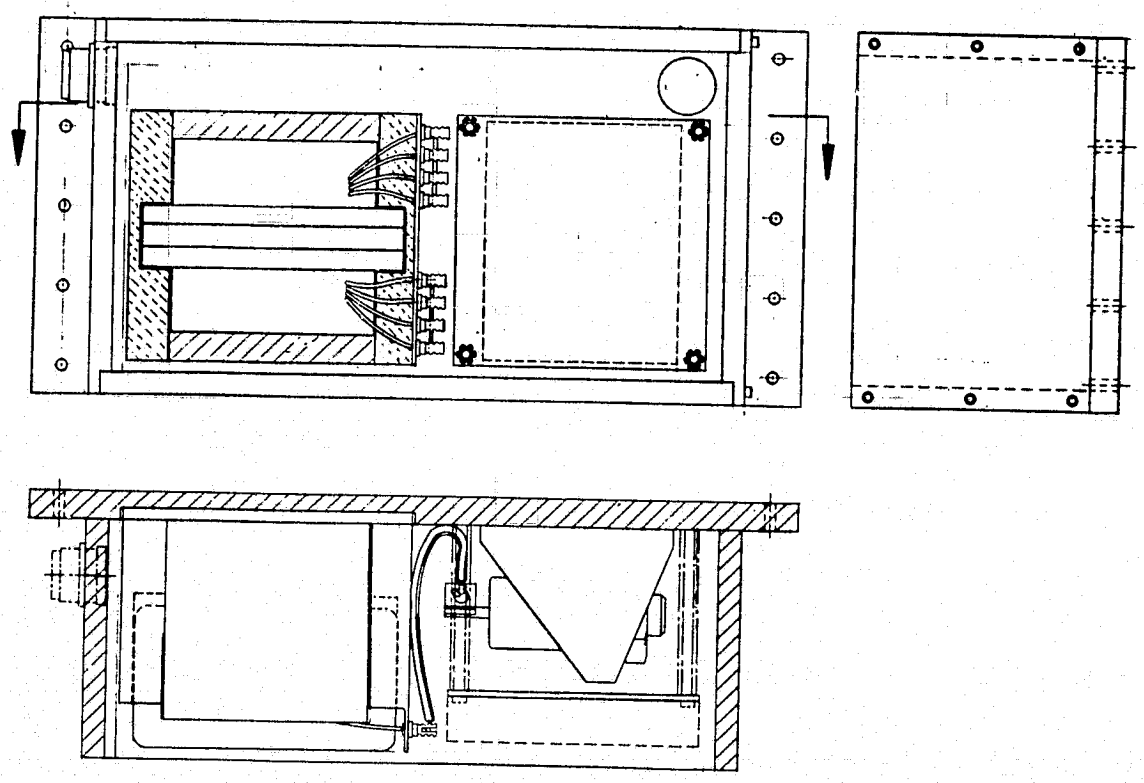


Figure A-6 Configuration 2 Power Stages

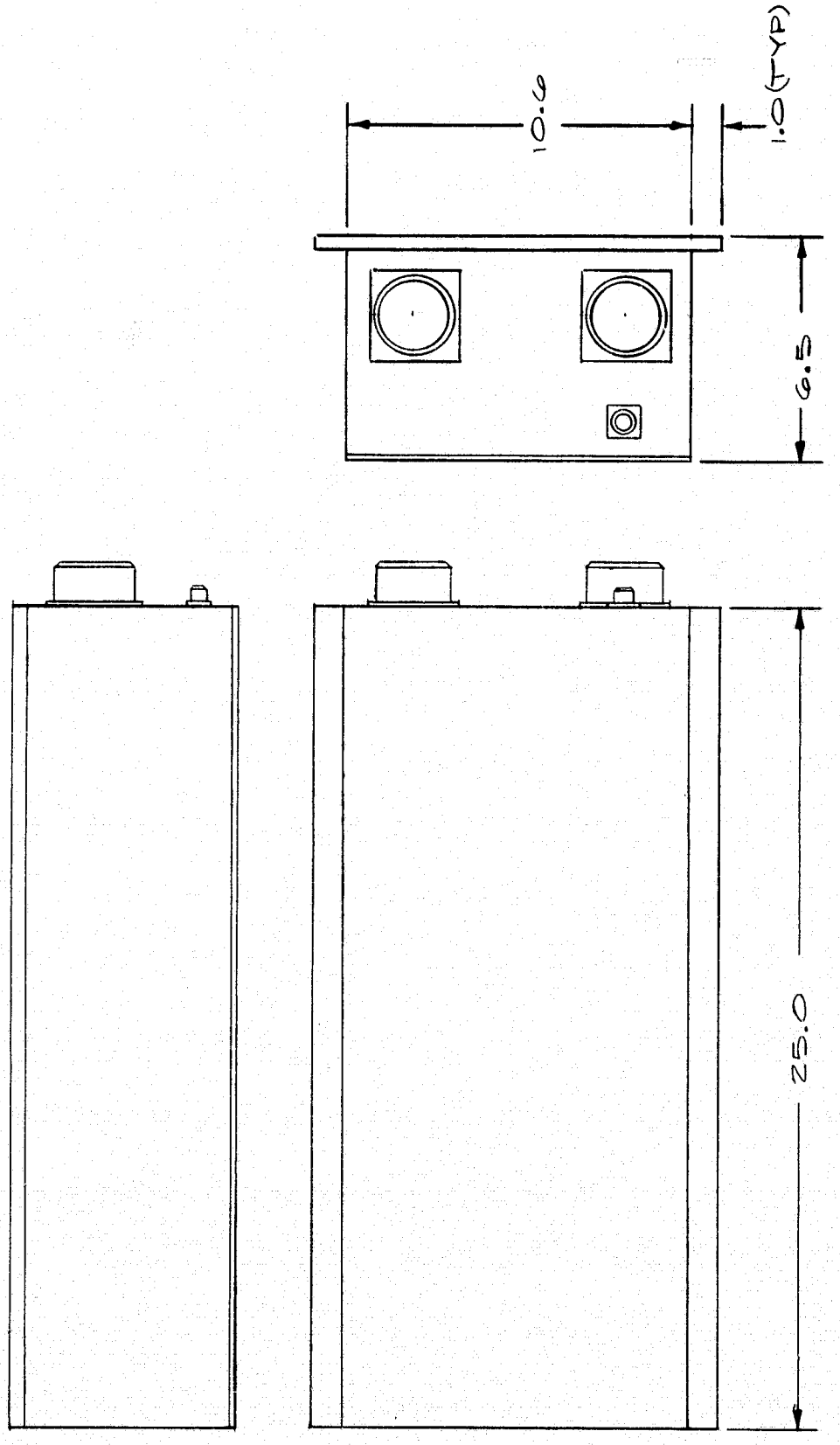


Figure A-7 Configuration 3 Outline

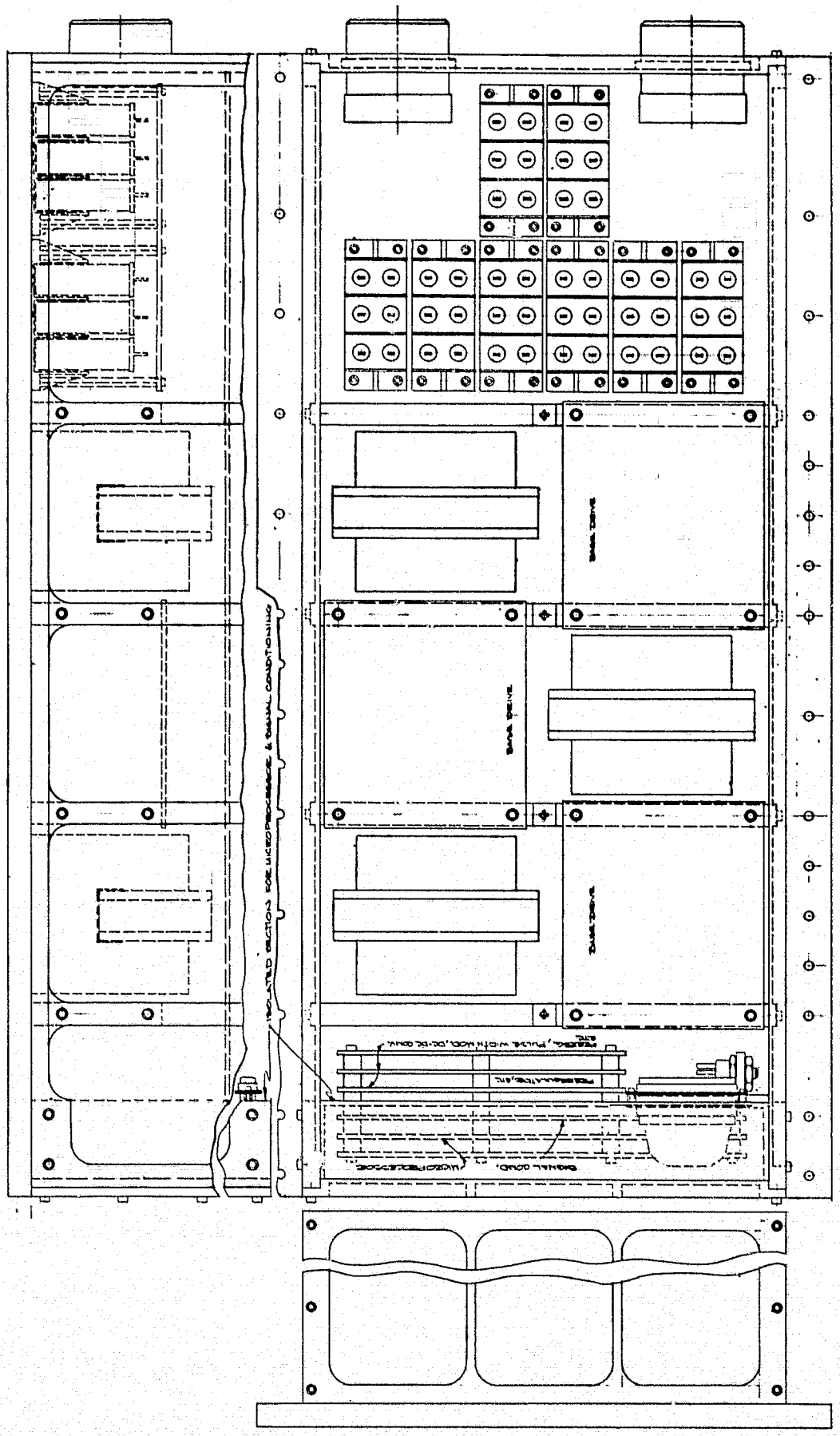


Figure A-8 Configuration 3 Layout

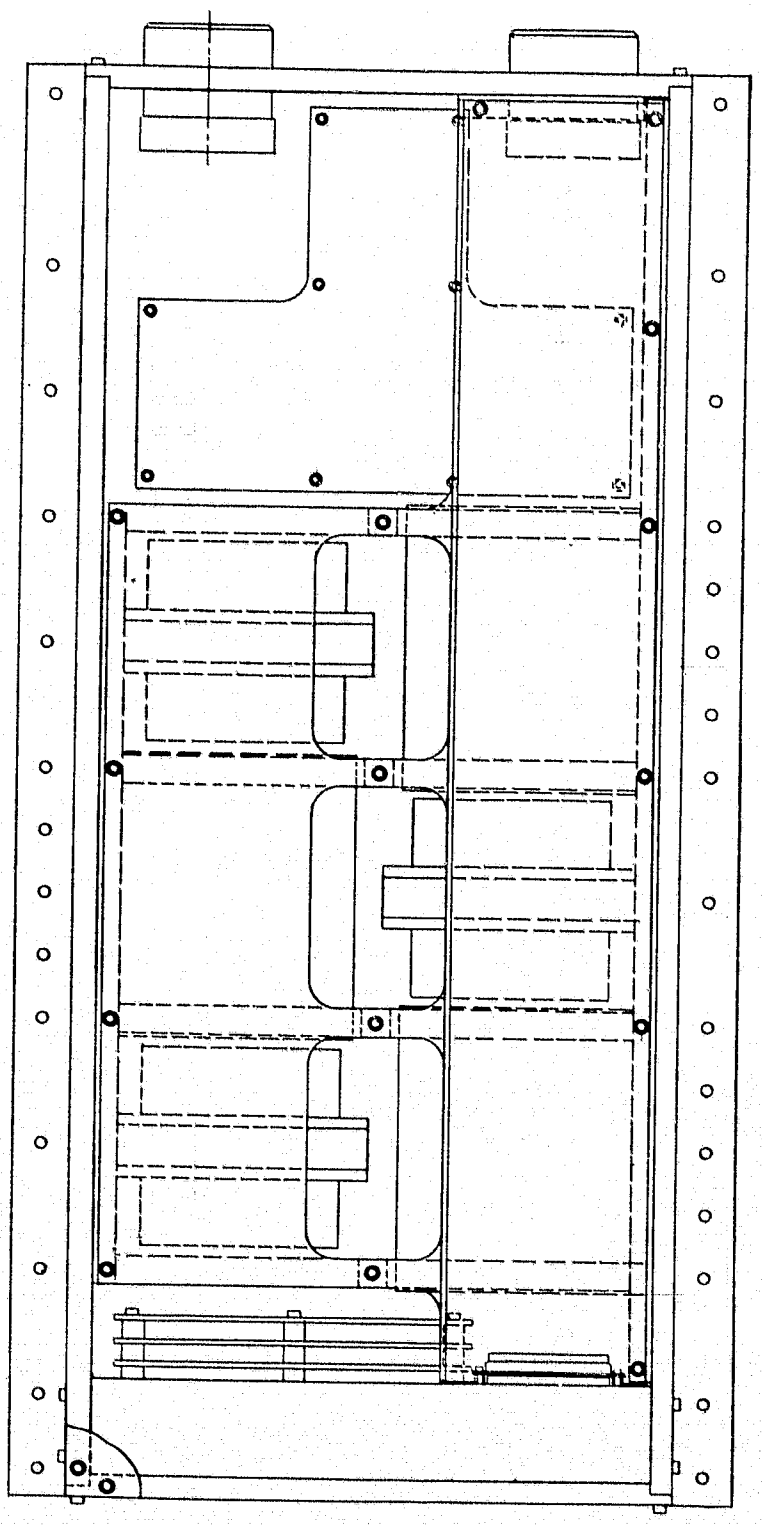


Figure A-9 Configuration 3 Cable Support

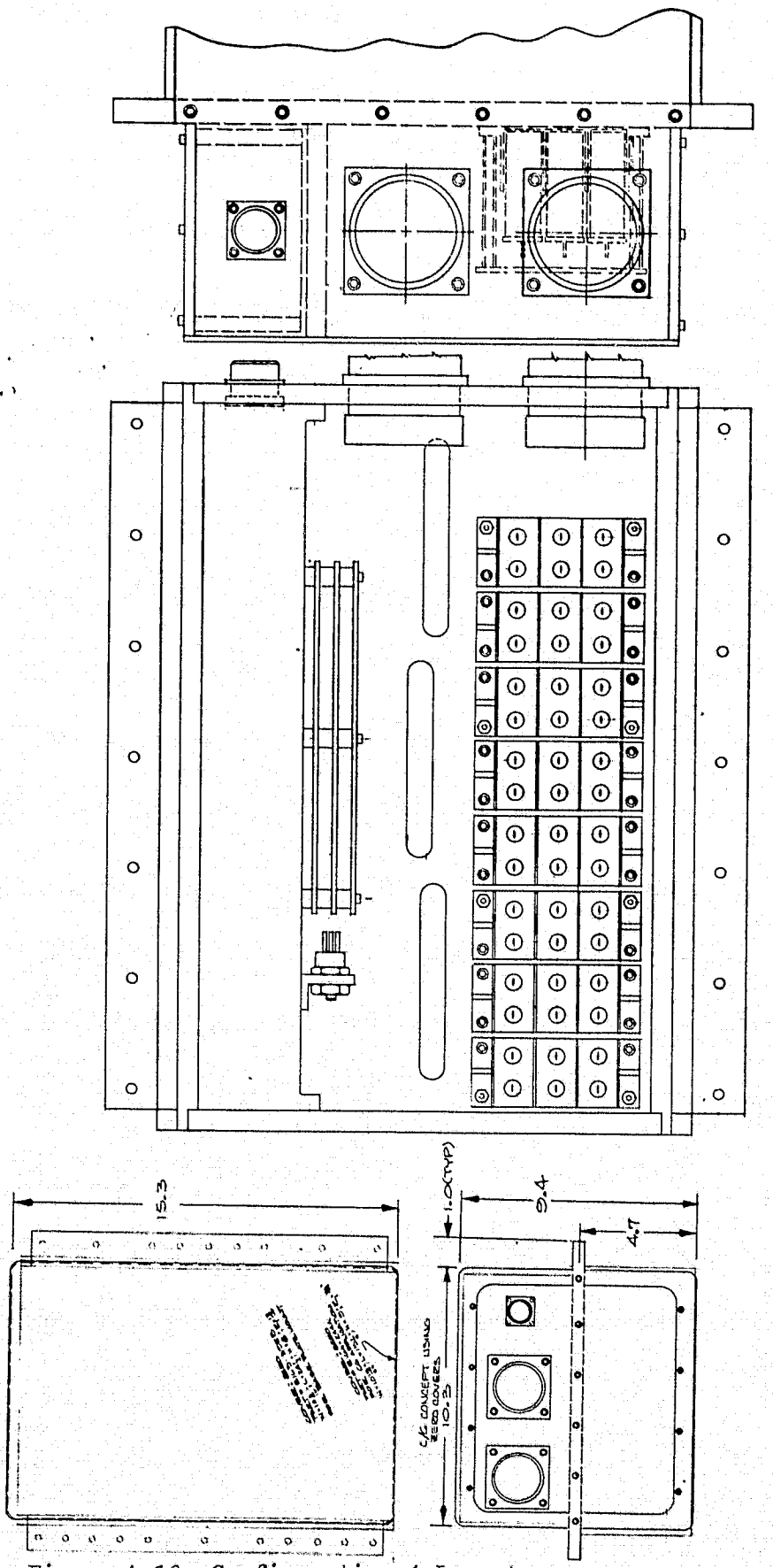


Figure A-10 Configuration 4 Layout

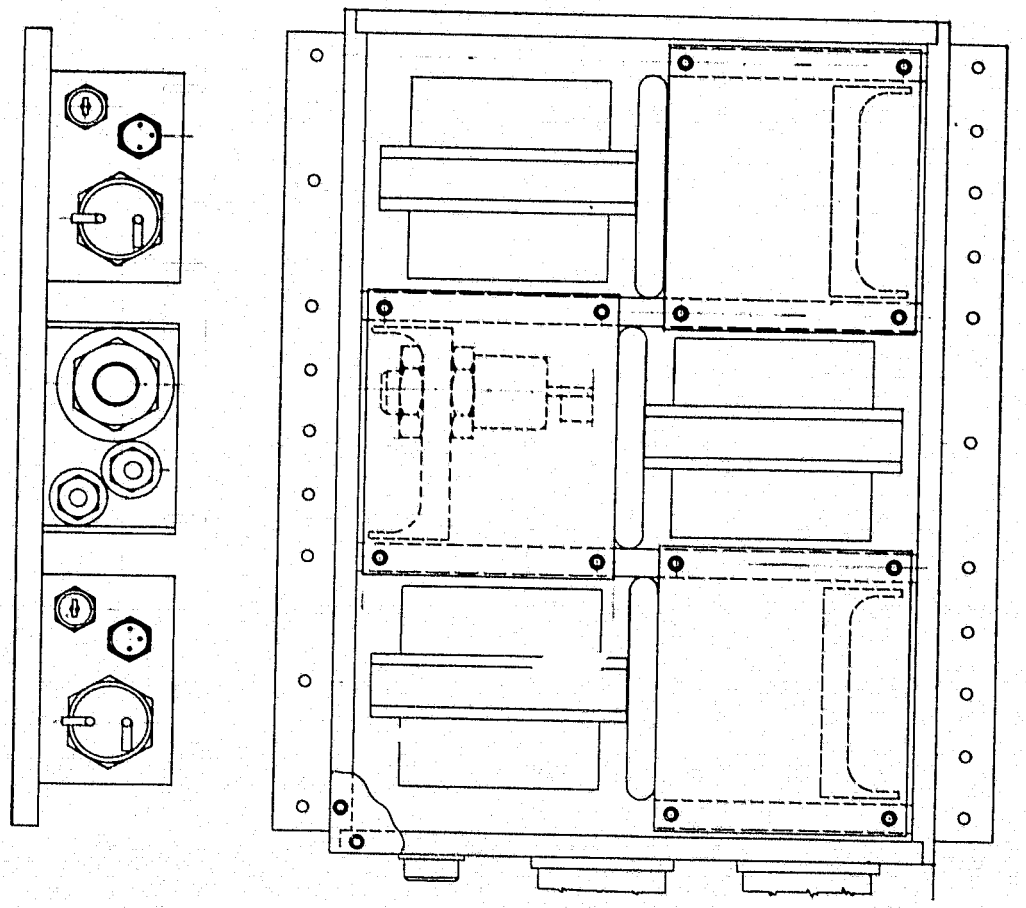
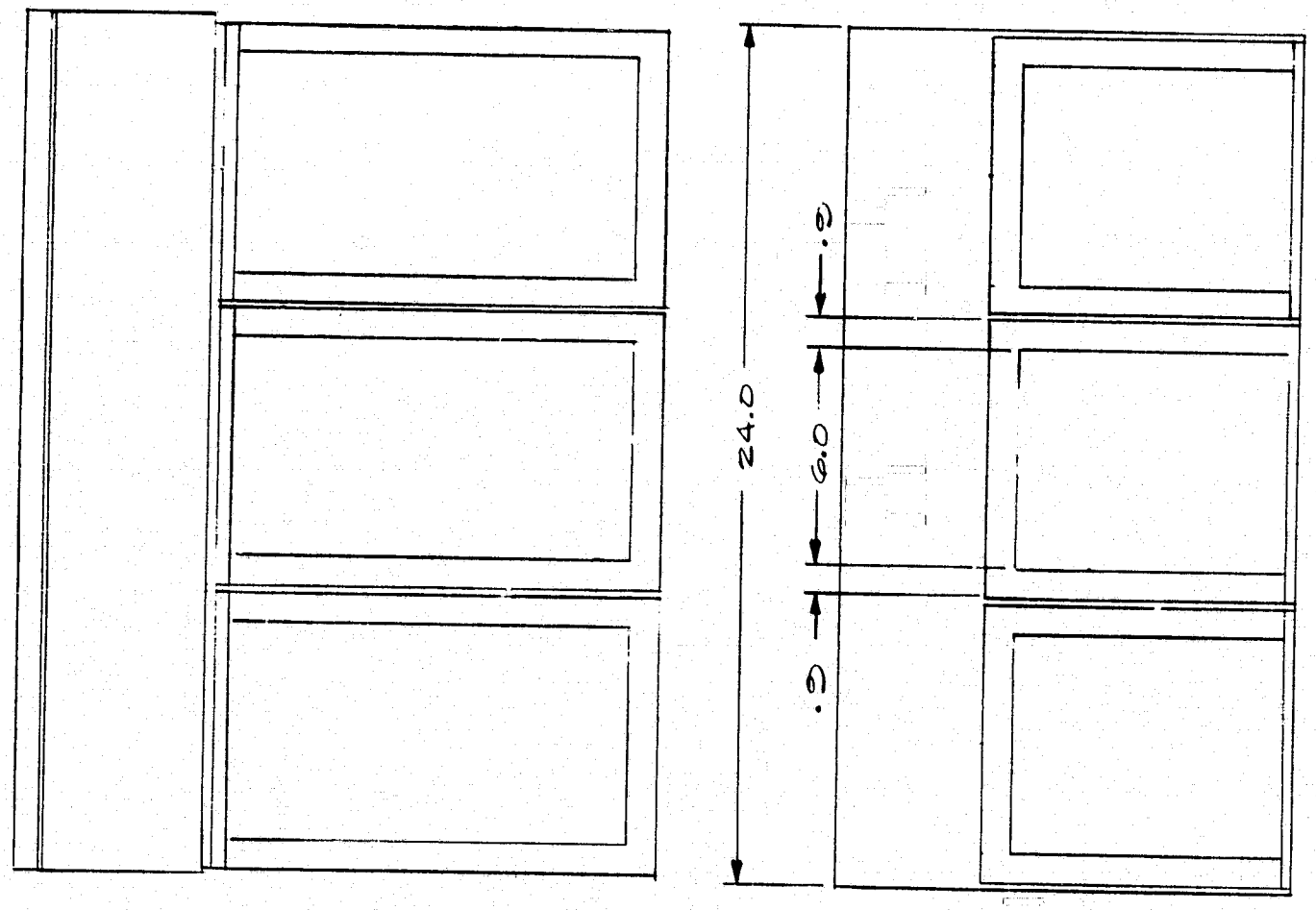


Figure A-11 Configuration 4 Power Stages



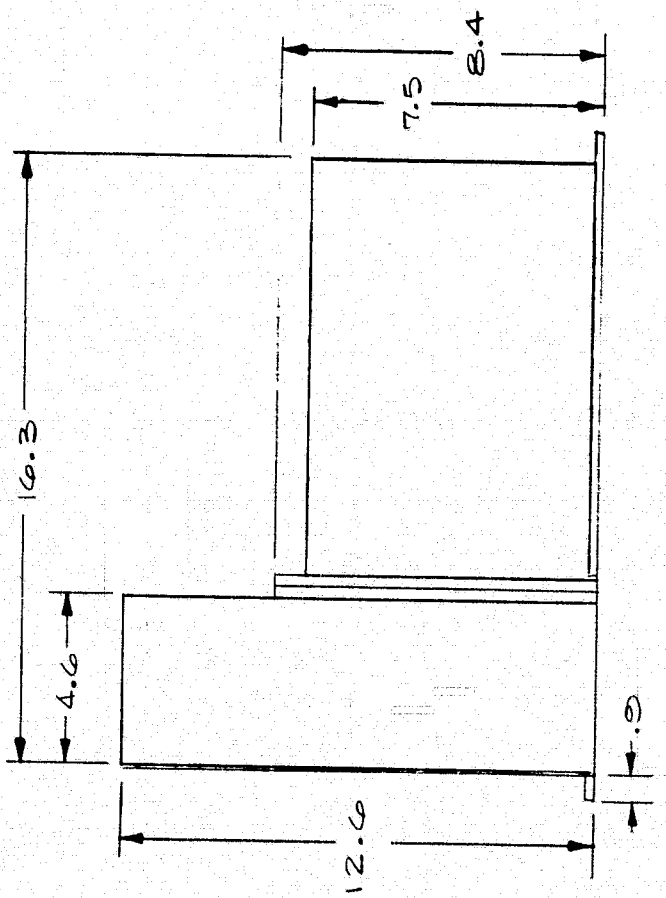


Figure A-12 Configuration 5 Outline

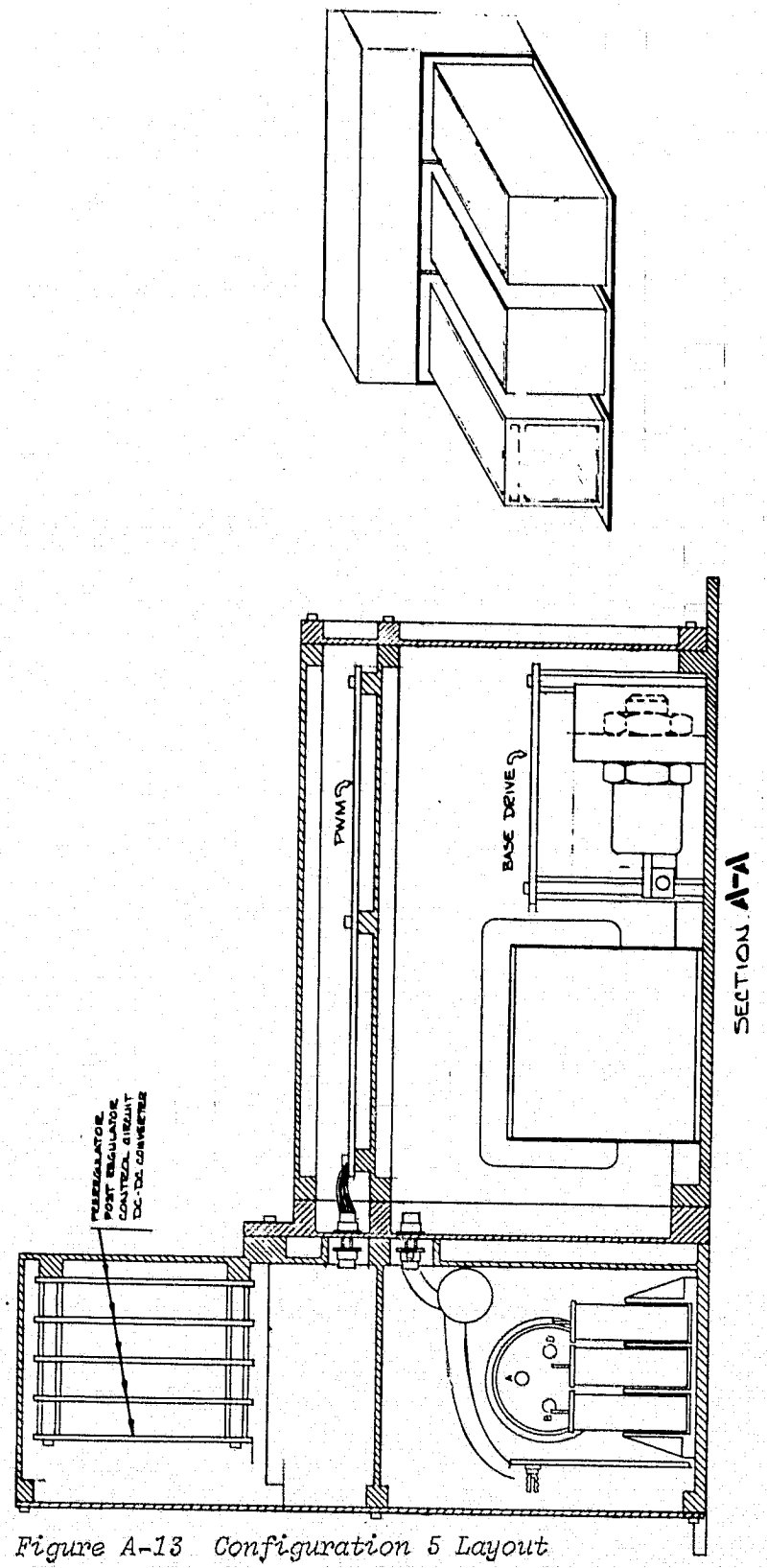


Figure A-13 Configuration 5 Layout

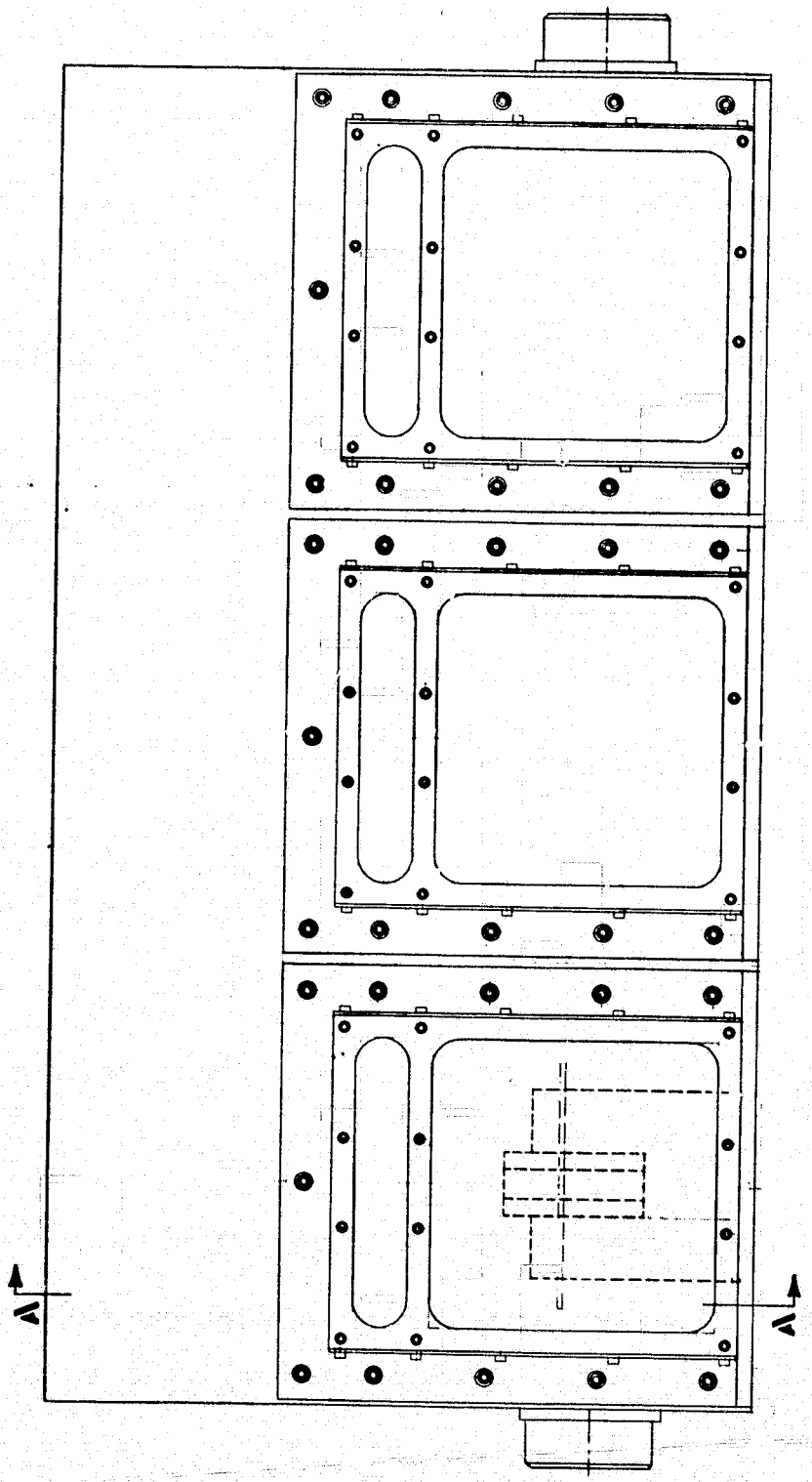


Figure A-14 Configuration 5 Side View

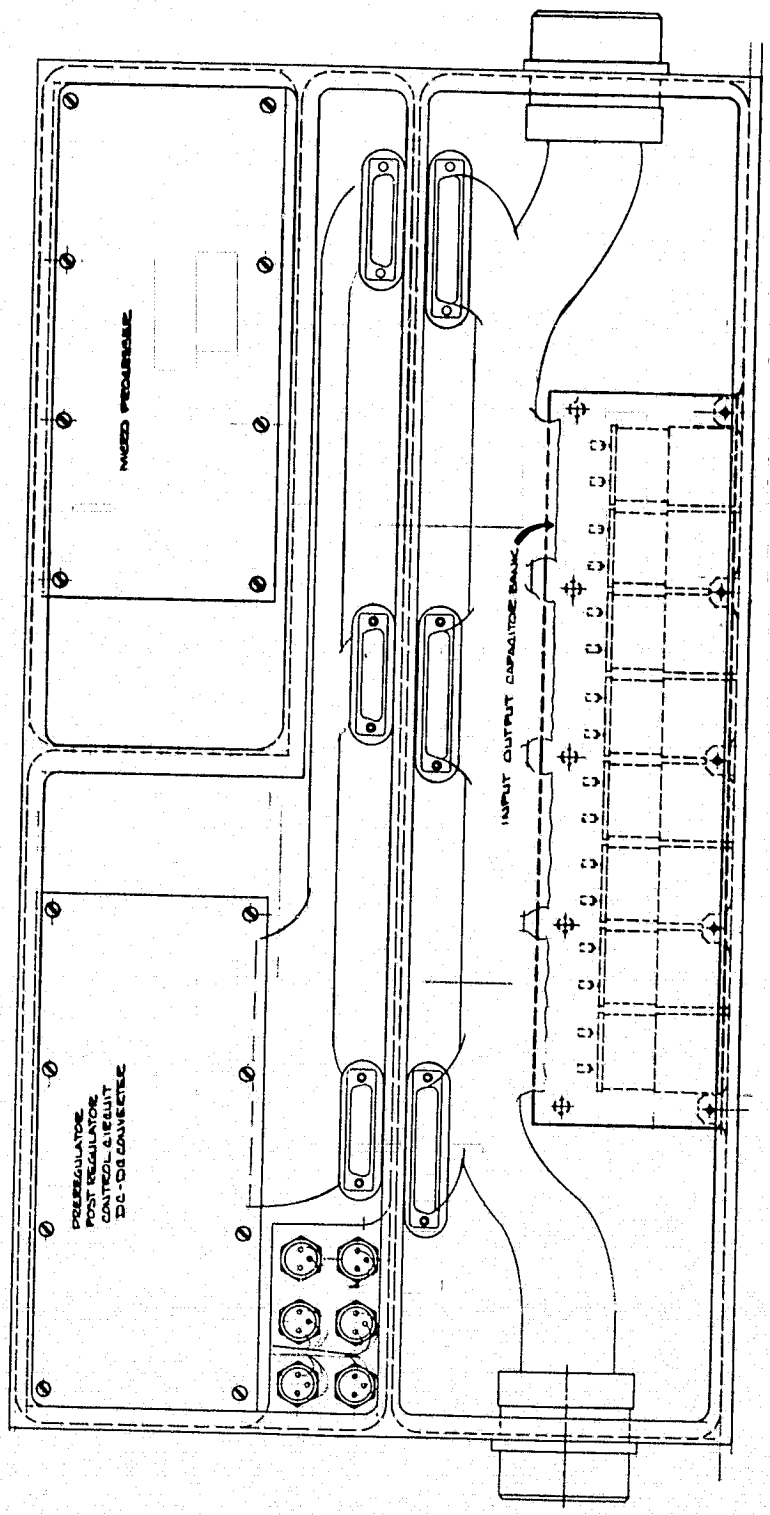


Figure A-15 Configuration 5 Mainframe Layout

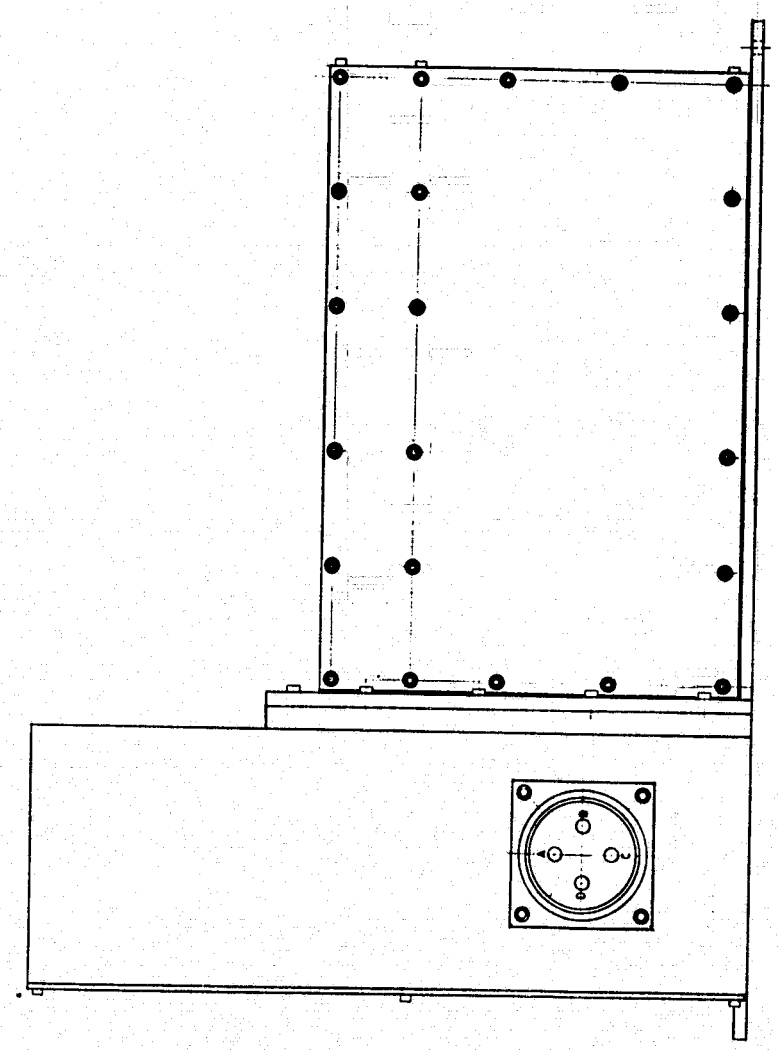


Figure A-16 Configuration 5 End View

Table A-1
Preliminary Parts List

Estimate of Parts for P^3
11/21/78

PWM (Pulsewidth Modulator) (Total of 3)	Quantity	Total Quantity
DIPs: 4023 (14-Lead)	1	3
4027 (16-Lead)	2	6
4011 (14-Lead)	1	3
4052 (16-Lead)	2	6
LM111 (14-Lead)	2	6
HA2-2500	3	9
Transistors: 2N910 (TO18)	2	6
2N2907A (TO18)	3	9
Zener Diodes: IN1509 (D012) Axial Lead	1	3
IN746 (A1) Axial Lead	1	3
Diodes: IN4449 (D035) Axial Lead	6	18
FETs: 2N6659	3	9
Capacitors: 470 pF, 4700 pF, 15 pF, 1 µF	16	48
Resistors: ½ W	2	6
¼ W, 5%	29	87
Telemetry & Current Signal Conditioner (Total of 4)		
DIPs: HA2-2500	1	4
Resistors: ¼ W	9	36
Transistor: 2N2614 (Requires Heat Sink for 2 W)	1	4
TO1 (Consider as a Small Stud-Mounted Rather Than TO1)	1	4
Capacitor: 1 µF, 50 V	1	4
Base Drive (Total of 3)		
Capacitor: 4.7 µF	1	3
Resistor: 0.25 Ω	1	3

Estimate of Parts for P^3
11/21/78

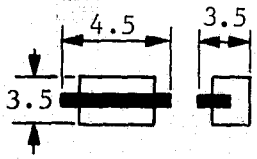
Base Drive Board (Total of 3)	Quantity (per Board)	Total Quantity (3 Boards)
Capacitor: 4.7 μF (Metal Film)	1	3
Resistor: 10 W, 0.25 Ω	1	3
Diode: IN4449 (Axial Lead)	2	6
IN5824 (Axial Lead)	2	6
IN5806 (Axial Lead)	2	6
IN5821 (Axial Lead)	2	6
IN5297 (Axial Lead)	3	9
FET: 2N6659	3	9
Resistor: ¼ W	3	9
½ W	1	3
Transistor: 2N4150 (TO5)	1	3
Transformer:	2	6
Capacitor: 150 μF, 30 V	4	12
1 μF, 50 V	1	3
Power Stage (Chasis-Mounted):		
Transistor: IN2814	1	3
D60T455010	1	3
Diode: MR874 or D2540D	1	3
Inductor: (C651-$1AA, ARNOLD) 	1	3
dc-dc Converter:		
Capacitor: 82 μF, 50 V	1	1
4.7 μF	1	1
Diodes: IN4449 (Assumed) (Axial Lead)	8	8
Resistor: 3.3 Ω, 1W	2	2
Inductors: L1-L5 (55120-M4 Core)	5	5
Transformer: T2 (80531-½D)	1	1
T1 (52176-1F)	1	1
Transistor: 2N2814 (Stud-Mounded)	2	2

Table A-1 (concl)

Estimate of Parts for P^3 11/21/78		
	Quantity	Total Quantity
Input Capacitor Bank:		
Cap: M3965/25,Size A5, 460 µF, 125 V	15	15
Resistors: ¼ W, 100k	5	5
Output Capacitor Bank:		
Capacitor: M3965/25,Size A5, 620 µF, 125 V	9	9
Resistor: ¼ W, 100k	3	3
Preregulator: TBD		
Postregulator: TBD		
Control Circuit: TBD		
Microprocessor Part No.	Quantity	No. of Leads
CD4013 (Flip-Flop)	1	14
CD4020 (Binary Counter/Divider)	2	16
7400 (Hex Inverter)	1	14
7404 (NAND Gate)	1	14
7474 (Flip-Flop)	1	14
8080A (Microprocessor)	1	40
7111 (RAM)	8	18
8205 (Decoder)	3	16
8212 (Input/Output Port)	2	24
8216 (Bus Driver)	2	16
8224 (Clock Generator)	1	16
8228 (System Controller)	1	28
1702 (E-PROM)	16	24
2N2222 (Transistor)(TO18)	1	--
0.1 µF Capacitor (CKR06)	34	--

APPENDIX B

THERMAL MATH MODEL LISTING AND ANALYSIS RESULTS FOR BASELINE CONFIGURATION 3

START OF INPUT DECK PROCESSING

```
INPUT CARD COL. = 12345678 1 2345678 2 2345678 3 2345678 4 2345678 5 2345678 6 2345678 7 2345678 8 EDIT NO.      CARD NO.

      BCD 3TITLE DATA                                                                    A.    1            1
      BCD 9 PROGRAMABLE POWER PROWER PROCESSOR  1/79  CHAPTER                          A.    2            2
      BCD 9 CONFIGURATION  -  CONFIGURATION  #3A FINAL MODEL                           A.    3            3
      BCD 9 PWR STG POWER INCREASE PWR FACT=1.000 BASE=3/16IN                          A.    4            4
C                                                                                      A.    5            5
C   ****************************************                                           A.    6            6
C   *  FILE NAME P3CONFIG3A ID=CHAPTER       *                                       A.    7            7
C   ****************************************                                           A.    8            8
C                                                                                      A.    9            9
C         CONFIGURATION DEPENDENT DATA INDICATED ON RIGHT                              A.   10           10
C                                                                                      A.   11           11
      END                                                                              A.   12           12
```

```
        BCD 3NODE DATA                                                                  A.   13      13
C                                                                                       A.   14      14
C                                                                                       A.   15      15
      1, 150.0 ,  1.0   $ IIN SHUNT                                                     A.   16      16
      2, 150.0 ,  1.0   $ INPUT CAPACTORS                                               A.   17      17
      3, 150.0 ,  1.0   $ OUTPUT CAPACTORS                                              A.   18      18
      4, 150.0 ,  1.0   $ SHUNT-PWR STG 1                                               A.   19      19
      5, 150.0 ,  1.0   $ SHUNT-PWR STG 2                                               A.   20      20
      6, 150.0 ,  1.0   $ SHUNT-PWR STG 3                                               A.   21      21
     10, 150.0 ,  1.0   $ XTR  CASE       -PWR STG 1                                    A.   22      22
     11, 150.0 ,  1.0   $ DIODE CASE      -PWR STG 1                                    A.   23      23
     12, 150.0 ,  1.0   $ L               -PWR STG 1                                    A.   24      24
     13, 150.0 ,  1.0   $ RES             -PWR STG 1                                    A.   25      25
     14, 150.0 ,  1.0   $ DRVER XTR CASE -PWR STG 1                                    A.   26      26
     15, 150.0 ,  1.0   $ BASE DRIVE      -PWR STG 1                                    A.   27      27
C                                                                                       A.   28      28
     20, 150.0 ,  1.0   $ XTR  CASE       -PWR STG 2                                    A.   29      29
     21, 150.0 ,  1.0   $ DIODE CASE      -PWR STG 2                                    A.   30      30
     22, 150.0 ,  1.0   $ L               -PWR STG 2                                    A.   31      31
     23, 150.0 ,  1.0   $ RES             -PWR STG 2                                    A.   32      32
     24, 150.0 ,  1.0   $ DRVER X*R CASE -PWR STG 2                                    A.   33      33
     25, 150.0 ,  1.0   $ BASE DRIVE      -PWR STG 2                                    A.   34      34
C                                                                                       A.   35      35
     30, 150.0 ,  1.0   $ XTR CASE        -PWR STG 3                                    A.   36      36
     31, 150.0 ,  1.0   $ DIODE CASE      -PWR STG 3                                    A.   37      37
     32, 150.0 ,  1.0   $ L               -PWR STG 3                                    A.   38      38
     33, 150.0 ,  1.0   $ RES             -PWR STG 3                                    A.   39      39
     34, 150.0 ,  1.0   $ DRVER XTR CASE -PWR STG 3                                    A.   40      40
     35, 150.0 ,  1.0   $ BASE DRIVE      -PWR STG 3                                    A.   41      41
C                                                                                       A.   42      42
     55, 150.0 ,  1.0   $ T061  XTR (6) CASES (SUPPORT PC COMPONENTS)                   A.   43      43
C                                                                                       A.   44      44
C XTR & DIODE JUNCTIONS                                                                 A.   45      45
     610, 150.0,  1.0                                                                   A.   46      46
     611, 150.0,  1.0                                                                   A.   47      47
     614, 150.0,  1.0                                                                   A.   48      48
     620, 150.0,  1.0                                                                   A.   49      49
     621  150.0,  1.0                                                                   A.   50      50
     624, 150.0,  1.0                                                                   A.   51      51
     630, 150.0,  1.0                                                                   A.   52      52
     631, 150.0,  1.0                                                                   A.   53      53
     634, 150.0,  1.0                                                                   A.   54      54
     655, 150.0,  1.0   $ (6) T061 XTR JUNCTIONS                                        A.   55      55
C COMPONENT STRUCTURE                                                                   A.   56      56
C                                                                                       A.   57      57
C CASE STRUCTURE                                                                        A.   58      58
       105, 150., 1.0       $ TOP                                                       A.   59      59
       121, 150., 1.0       $ BASE                                                      A.   60      60
       122, 150., 1.0       $ BASE                                                      A.   61      61
       123, 150., 1.0       $ BASE                                                      A.   62      62
       124, 150., 1.0       $ BASE                                                      A.   63      63
       125, 150., 1.0       $ BASE                                                      A.   64      64
```

```
      126, 150., 1.0        $ BASE                                          A.   65      65
      127, 150., 1.0        $ BASE                                          A.   66      66
      128, 150., 1.0        $ BASE                                          A.   67      67
      129, 150., 1.0        $ BASE                                          A.   68      68
      130, 150., 1.0        $ SIDES                                         A.   69      69
      131, 150., 1.0        $ SIDES                                         A.   70      70
      132, 150., 1.0        $ SIDES                                         A.   71      71
      133, 150., 1.0        $ SIDES                                         A.   72      72
      151, 150., 1.0        $ INTERNAL WALLS                                A.   73      73
      152, 150., 1.0        $ INTERNAL WALLS                                A.   74      74
      153, 150., 1.0        $ INTERNAL WALLS                                A.   75      75
      154, 150., 1.0        $ INTERNAL WALLS                                A.   76      76
      155, 150., 1.0        $ INTERNAL WALLS                                A.   77      77
      170, 150.,-1.0        $ INTERFACE                                     A.   78      78
      171, 150.,-1.0                                                        A.   79      79
      172, 150.,-1.0                                                        A.   80      80
      173, 150.,-1.0                                                        A.   81      81
      174, 150.,-1.0                                                        A.   82      82
      175, 150.,-1.0                                                        A.   83      83
      176, 150.,-1.0        $ INTERFACE                                     A.   84      84
      177, 150.,-1.0        $ INTERFACE                                     A.   85      85
      178, 150.,-1.0        $ INTERFACE                                     A.   86      86
C                                                                           A.   87      87
C                                                                           A.   88      88
    111, 150.0 ,  1.0   $ PWR STAGE 1 STRUCTURE                           A.   89      89
    112, 150.0 ,  1.0   $ PWR STAGE 2 STRUCTURE                           A.   90      90
    113, 150.0 ,  1.0   $ PWR STAGE 3 STRUCTURE                           A.   91      91
C                                                                           A.   92      92
C                                                                           A.   93      93
C                                                                           A.   94      94
C MAIN PC BOARDS -TM,PRE REG,DC-DC CON,POST-REG,CNTRL,MICRO-P               A.   95      95
C                                                                           A.   96      96
    700, 150.0 ,  1.0                                                       A.   97      97
C                                                                           A.   98      98
C COMPARTMENT EFFECTIVE RADIATION NODES                                     A.   99      99
C                                                                           A.  100     100
      501, 150.0 ,-1.0$ ERN COMPARTMENT 1                                   A.  101     101
C                                                                           A.  102     102
C THERMAL SINK NODES                                                        A.  103     103
C                                                                           A.  104     104
     -1000,  50.,0.   $ COLDPLATE SINK                                      A.  105     105
     -1001, 100.,0.   $ RADIATION ENVIRONMENTAL SINK                        A.  106     106
C                                                                           A.  107     107
C DUMMY NODES                                                               A.  108     108
     -2000, 100.,0.   $ AVERAGE COMPONENT TEMPERATURE                       A.  109     109
     -2001, 100.,0.   $ AVERAGE CASE TEMPERATURE                            A.  110     110
     END                                                                    A.  111     111
```

NODE SUMMARY

THERE ARE 58 DIFFUSION NODES, 10 ARITHMETIC NODES, 0 HEATER NODES, AND 4 BOUNDARY NODES
FOR A TOTAL OF 72 NODES IN THE NETWORK

NODE DIRECTORY
INPUT/INTERNAL

DIFFUSION NODES

1=	1 $	2=	2 $	3=	3 $	4=	4 $	5=	5 $	6=	6 $	10=	7 $	11=	8 $	12=	9
13=	10 $	14=	11 $	15=	12 $	20=	13 $	21=	14 $	22=	15 $	23=	16 $	24=	17 $	25=	18
30=	19 $	31=	20 $	32=	21 $	33=	22 $	34=	23 $	35=	24 $	55=	25 $	610=	26 $	611=	27
614=	28 $	620=	29 $	621=	30 $	624=	31 $	630=	32 $	631=	33 $	634=	34 $	655=	35 $	105=	36
121=	37 $	122=	38 $	123=	39 $	124=	40 $	125=	41 $	126=	42 $	127=	43 $	128=	44 $	129=	45
130=	46 $	131=	47 $	132=	48 $	133=	49 $	151=	50 $	152=	51 $	153=	52 $	154=	53 $	155=	54
111=	55 $	112=	56 $	113=	57 $	700=	58 $										

ARITHMETIC NODES

170=	59 $	171=	60 $	172=	61 $	173=	62 $	174=	63 $	175=	64 $	176=	65 $	177=	66 $	178=	67
501=	68 $																

HEATER NODES
++NONE++

BOUNDARY NODES

1000=	69 $	1001=	70 $	2000=	71 $	2001=	72 $

```
INPUT CARD COL. = 12345678 1 2345678 2 2345678 3 2345678 4 2345678 5 2345678 6 2345678 7 2345678 8 EDIT NO.   CARD NO.
        BCD 3CONDUCTOR DATA                                                                    A.  112        112
C                                                                                              A.  113        113
C                                                                                              A.  114        114
C  CASE COUPLINGS TO ENVIRONMENT-------                                                       A.  115        115
C                                                                                              A.  116        116
C  XTR & DIODE   JUNCTIONS TO CASE-----                                                       A.  117        117
      500,610,   10,  9.48                                                                     A.  118        118
      501,611,   11,  2.372                                                                    A.  119        119
      502,614,   14,  0.948                                                                    A.  120        120
      503,620,   20,  9.48                                                                     A.  121        121
      504,621,   21,  2.372                                                                    A.  122        122
      505,624,   24,  0.948                                                                    A.  123        123
      506,630,   30,  9.48                                                                     A.  124        124
      507,631,   31,  2.372                                                                    A.  125        125
      508,634,   34,  0.948                                                                    A.  126        126
      509,655,   55,  0.948*6.0          $ (6) T061'S                                          A.  127        127
C                                                                                              A.  128        128
C  CASE STRUCTURE MODEL ----------------------------                                          A.  129        129
C                                                                                              A.  130        130
       195,126,111, 13.6                 $ XTR MNT TO BASE                                     A.  131        131
       196,124,112, 13.6                 $ XTR MNT TO BASE                                     A.  132        132
       197,128,113, 13.6                 $ XTR MNT TO BASE                                     A.  133        133
C CASE CONDUCTION                                                                              A.  134        134
        200,105,130,    .5                                                                     A.  135        135
        201,105,131,   1.94                                                                    A.  136        136
        202,105,132,    .5                                                                     A.  137        137
        203,105,133,   1.94                                                                    A.  138        138
        204,130,131,    .27                                                                    A.  139        139
        205,131,132,    .27                                                                    A.  140        140
        206,132,133,    .27                                                                    A.  141        141
        207,133,130,    .27                                                                    A.  142        142
        208,130,170,   1.64                                                                    A.  143        143
        209,131,178,   3.84                                                                    A.  144        144
        210,132,176,   1.64                                                                    A.  145        145
        211,133,177,   3.84                                                                    A.  146        146
        212,151,171,   2.41                                                                    A.  147        147
        213,151,133,    .21                                                                    A.  148        148
        214,151,131,    .21                                                                    A.  149        149
        215,152,172,   2.41                                                                    A.  150        150
        216,152,133,    .21                                                                    A.  151        151
        217,152,131,    .21                                                                    A.  152        152
        218,153,173,   2.41                                                                    A.  153        153
        219,153,133,    .21                                                                    A.  154        154
        220,153,131,    .21                                                                    A.  155        155
        221,154,174,   2.41                                                                    A.  156        156
        222,154,133,    .21                                                                    A.  157        157
        223,154,131,    .21                                                                    A.  158        158
        224,155,175,   2.41                                                                    A.  159        159
        225,155,133,    .21                                                                    A.  160        160
        226,155,131,    .21                                                                    A.  161        161
C                                                                                              A.  162        162
C BASE CONDUCTION                                                                              A.  163        163
```

```
          227,121,170,    7.96*1.88                                  A.  164   164
          228,121,177,     .33*1.88                                  A.  165   165
          229,121,178,     .33*1.88                                  A.  166   166
          230,121,171,    7.96*1.88                                  A.  167   167
          231,122,171,    8.96*1.88                                  A.  168   168
          232,122,177,     .47*1.88                                  A.  169   169
          233,122,172,    8.96*1.88                                  A.  170   170
          234,122,178,     .47*1.88                                  A.  171   171
          235,123,172,    2.11*1.88                                  A.  172   172
          236,123,177,    1.32*1.88                                  A.  173   173
          237,123,173,    2.11*1.88                                  A.  174   174
          238,123,126,     .66*1.88                                  A.  175   175
          239,124,173,    2.11*1.88                                  A.  176   176
          240,124,177,    1.32*1.88                                  A.  177   177
          241,124,174,    2.11*1.88                                  A.  178   178
          242,124,127,     .66*1.88                                  A.  179   179
          243,125,174,    2.11*1.88                                  A.  180   180
          244,125,177,    1.32*1.88                                  A.  181   181
          245,125,175,    2.11*1.88                                  A.  182   182
          246,125,128,     .66*1.88                                  A.  183   183
          247,126,172,    2.11*1.88                                  A.  184   184
          249,126,173,    2.11*1.88                                  A.  185   185
          250,126,178,    1.32*1.88                                  A.  186   186
          251,127,173,    2.11*1.88                                  A.  187   187
          253,127,174,    2.11*1.88                                  A.  188   188
          254,127,178,    1.32*1.88                                  A.  189   189
          255,128,174,    2.11*1.88                                  A.  190   190
          257,128,175,    2.11*1.88                                  A.  191   191
          258,128,178,    1.32*1.88                                  A.  192   192
          259,129,175,    2.18*1.88                                  A.  193   193
          260,129,177,    1.27*1.88                                  A.  194   194
          261,129,176,    2.18*1.88                                  A.  195   195
          262,129,178,    1.27*1.88                                  A.  196   196
C                                                                    A.  197   197
          263,121,1000,   141.*.17                                   A.  198   198
          264,122,1000,   141.*.15                                   A.  199   199
          265,123,1000,   141.*.16                                   A.  200   200
          266,124,1000,   141.*.18                                   A.  201   201
          267,125,1000,   141.*.16                                   A.  202   202
          268,126,1000,   141.*.16                                   A.  203   203
          269,127,1000,   141.*.16                                   A.  204   204
          270,128,1000,   141.*.16                                   A.  205   205
          271,129,1000,   141.*.21                                   A.  206   206
C                                                                    A.  207   207
          272,170,1000,   0.0                                        A.  208   208
          273,176,1000,   0.0                                        A.  209   209
          274,177,1000,   0.0                                        A.  210   210
          275,178,1000,   0.0                                        A.  211   211
C                                                                    A.  212   212
C COMPONENT CONDUCTION TO CASE OR BASE                               A.  213   213
      100,  1,  129,  1.00                                           A.  214   214
      101,  2,  129,  4.46                                           A.  215   215
```

```
      102,  3,  129,  2.63                                                    A.  216   216
      103,  4,  129, 1.00                                                     A.  217   217
      104,  5,  129, 1.00                                                     A.  218   218
      105,  6,  129, 1.00                                                     A.  219   219
      106, 10,  111,  5.41                                                    A.  220   220
      107, 11,  111,  1.32                                                    A.  221   221
      108, 12,  123, 3.330                                                    A.  222   222
      109, 13,  123,  .500                                                    A.  223   223
      110, 14,  111,  1.32                                                    A.  224   224
      112, 20,  112,  5.41                                                    A.  225   225
      113, 21,  112,  1.32                                                    A.  226   226
      114, 22,  127, 3.330                                                    A.  227   227
      115, 23,  127,  .500                                                    A.  228   228
      116, 24,  112,  1.32                                                    A.  229   229
      118, 30,  113,  5.41                                                    A.  230   230
      119, 31,  113,  1.32                                                    A.  231   231
      120, 32,  125, 3.330                                                    A.  232   232
      121, 33,  125,  .500                                                    A.  233   233
      122, 34,  113,  1.32                                                    A.  234   234
      124, 55,  151, 1.32*6.0                                                 A.  235   235
C PWB CONDUCTION                                                              A.  236   236
C     125,700,  151,  1.62                  $ PWB TO CASE                     A.  237   237
C     126, 15,  152,   .667*.5              $ BASE DRIVE PWB TO STRUC         A.  238   238
C     127, 15,  153,   .667*.5              $ BASE DRIVE PWB TO STRUC         A.  239   239
C     128, 25,  153,   .667*.5              $ BASE DRIVE PWB TO STRUC         A.  240   240
C     129, 25,  154,   .667*.5              $ BASE DRIVE PWB TO STRUC         A.  241   241
C     130, 35,  154,   .667*.5              $ BASE DRIVE PWB TO STRUC         A.  242   242
C     131, 35,  155,   .667*.5              $ BASE DRIVE PWB TO STRUC         A.  243   243
C ERN COUPLINGS----------------                                               A.  244   244
   -1100,  1,  501,  1.713E-9*.9*.020                                         A.  245   245
   -1101,  2,  501,  1.713E-9*.9*.466                                         A.  246   246
   -1102,  3,  501,  1.713E-9*.9*.309                                         A.  247   247
   -1103,  4,  501,  1.713E-9*.9*.020                                         A.  248   248
   -1104,  5,  501,  1.713E-9*.9*.020                                         A.  249   249
   -1105,  6,  501,  1.713E-9*.9*.020                                         A.  250   250
   -1108, 12,  501,  1.713E-9*.9*.425                                         A.  251   251
   -1109, 13,  501,  1.713E-9*.9*.014                                         A.  252   252
   -1114, 22,  501,  1.713E-9*.9*.425                                         A.  253   253
   -1115, 23,  501,  1.713E-9*.9*.014                                         A.  254   254
   -1120, 32,  501,  1.713E-9*.9*.425                                         A.  255   255
   -1121, 33,  501,  1.713E-9*.9*.014                                         A.  256   256
   -1150,130,  501,  1.713E-9*.9*.49                                          A.  257   257
   -1151,132,  501,  1.713E-9*.9*.49                                          A.  258   258
   -1152,133,  501,  1.713E-9*.9*1.14                                         A.  259   259
   -1153,131,  501,  1.713E-9*.9*1.14                                         A.  260   260
   -1154,105,  501,  1.713E-9*.9*1.88                                         A.  261   261
C  PC BOARDS TO ERN OR STRUCTURE                                              A.  262   262
   -1200,700,  130,  1.713E-9*.9*.9*.380          $PWB TO CASE                A.  263   263
   -1201,700,  151,  1.713E-9*.9*.9*.630          $PWB TO CASE 2SIDE          A.  264   264
   -1202,700,  501,  1.713E-9*.9*.9*.250          $PWB TO CASE                A.  265   265
   -1111, 15,  501,  1.713E-9*.9*.140 $BASE DRIVE-ERN                         A.  266   266
   -1117, 25,  501,  1.713E-9*.9*.140 $BASE DRIVE-ERN                         A.  267   267
```

PROGRAMABLE POWER PROWER PROCESSOR 1/79 CHAPTER CONFIGURATION - CONFIGURATION #3A FINAL MODEL PWR STG POW

INPUT CARD COL. = 12345678 1 2345678 2 2345678 3 2345678 4 2345678 5 2345678 6 2345678 7 2345678 8 EDIT NO. CARD NO.

```
                -1123, 35,  501,  1.713E-9*.9*.140 $BASE DRIVE-ERN                A.  268      268
                C                                                                 A.  269      269
                      END                                                         A.  270      270
```


CONDUCTOR SUMMARY

THERE ARE 108 LINEAR CONDUCTORS AND 23 NON-LINEAR CONDUCTORS , FOR A TOTAL OF 131 CONDUCTORS IN THIS NETWORK

CONDUCTOR DIRECTORY
INPUT=INTERNAL

500=	1	$	501=	2	$	502=	3	$	503=	4	$	504=	5	$	505=	6	$	506=	7	$	507=	8	$	508=	9
509=	10	$	195=	11	$	196=	12	$	197=	13	$	200=	14	$	201=	15	$	202=	16	$	203=	17	$	204=	18
205=	19	$	206=	20	$	207=	21	$	208=	22	$	209=	23	$	210=	24	$	211=	25	$	212=	26	$	213=	27
214=	28	$	215=	29	$	216=	30	$	217=	31	$	218=	32	$	219=	33	$	220=	34	$	221=	35	$	222=	36
223=	37	$	224=	38	$	225=	39	$	226=	40	$	227=	41	$	228=	42	$	229=	43	$	230=	44	$	231=	45
232=	46	$	233=	47	$	234=	48	$	235=	49	$	236=	50	$	237=	51	$	238=	52	$	239=	53	$	240=	54
241=	55	$	242=	56	$	243=	57	$	244=	58	$	245=	59	$	246=	60	$	247=	61	$	249=	62	$	250=	63
251=	64	$	253=	65	$	254=	66	$	255=	67	$	257=	68	$	258=	69	$	259=	70	$	260=	71	$	261=	72
262=	73	$	263=	74	$	264=	75	$	265=	76	$	266=	77	$	267=	78	$	268=	79	$	269=	80	$	270=	81
271=	82	$	272=	83	$	273=	84	$	274=	85	$	275=	86	$	100=	87	$	101=	88	$	102=	89	$	103=	90
104=	91	$	105=	92	$	106=	93	$	107=	94	$	108=	95	$	109=	96	$	110=	97	$	112=	98	$	113=	99
114=	100	$	115=	101	$	116=	102	$	118=	103	$	119=	104	$	120=	105	$	121=	106	$	122=	107	$	124=	108
1100=	109	$	1101=	110	$	1102=	111	$	1103=	112	$	1104=	113	$	1105=	114	$	1108=	115	$	1109=	116	$	1114=	117
1115=	118	$	1120=	119	$	1121=	120	$	1150=	121	$	1151=	122	$	1152=	123	$	1153=	124	$	1154=	125	$	1200=	126
1201=	127	$	1202=	128	$	1111=	129	$	1117=	130	$	1123=	131	$											

```
      BCD 3CONSTANTS DATA                                                    A.  271      271
C                                                                            A.  272      272
      ARLXCA=.0010                                                           A.  273      273
      DRLXCA=.0010                                                           A.  274      274
      TIMEN = 0.0                                                            A.  275      275
      TSTEPI= 0.0                                                            A.  276      276
      TSTEPO= 0.0                                                            A.  277      277
      TIMEND= 0.0                                                            A.  278      278
      SBCNST=1.00                                                            A.  279      279
      ABSZRO=-460.0                                                          A.  280      280
      NDSTOR=200                                                             A.  281      281
      EBALNA=.001                                                            A.  282      282
      EBALSA=.001                                                            A.  283      283
      ITERMX=  1000                                                          A.  284      284
C                                                                            A.  285      285
      1=   20.*3.413 $ IIN SHUNT                                             A.  286      286
      2=   15.*3.413 $ INPUT CAPACTORS                                       A.  287      287
      3=    1.*3.413 $ OUTPUT CAPACTORS                                      A.  288      288
      4=    8.*3.413 $ SHUNT-PWR STG  1                                      A.  289      289
      5=    8.*3.413 $ SHUNT-PWR STG  2                                      A.  290      290
      6=    8.*3.413 $ SHUNT-PWR STG  3                                      A.  291      291
      610=  100.*3.413 $ XTR   -PWR STG 1                                    A.  292      292
      611=   30.*3.413 $ DIODE -PWR STG 1                                    A.  293      293
      12=   13.*3.413 $ L      -PWR STG 1                                    A.  294      294
      13=    6.*3.413 $ RES    -PWR STG 1                                    A.  295      295
      614=    6.*3.413 $ DRVER XTR -PWR STG 1                                A.  296      296
      15=    3.*3.413 $ BASE DRIVE -PWR STG 1                                A.  297      297
C                                                                            A.  298      298
      620=  100.*3.413 $ XTR  -PWR STG 2                                     A.  299      299
      621=   30.*3.413 $ DIODE-PWR STG 2                                     A.  300      300
      22=   13.*3.413 $ L     -PWR STG 2                                     A.  301      301
      23=    6.*3.413 $ RES   -PWR STG 2                                     A.  302      302
      624=    6.*3.413 $ DRVER XTR -PWR STG 2                                A.  303      303
      25=    3.*3.413 $ BASE DRIVE -PWR STG 2                                A.  304      304
C                                                                            A.  305      305
      630=  100.*3.413 $ XTR   -PWR STG 3                                    A.  306      306
      631=   30.*3.413 $ DIODE -PWR STG 3                                    A.  307      307
      32=   13.*3.413 $ L      -PWR STG 3                                    A.  308      308
      33=    6.*3.413 $ RES    -PWR STG 3                                    A.  309      309
      634=    6.*3.413 $ DRVER XTR -PWR STG 3                                A.  310      310
      35=    3.*3.413 $ BASE DRIVE -PWR STG 3                                A.  311      311
      51=    5.*3.413 $ PWM 1                                                A.  312      312
      52=    5.*3.413 $ PWM 2                                                A.  313      313
      53=    5.*3.413 $ PWM 3                                                A.  314      314
      655=  30.*3.413 $ (6) T061 XTR                                         A.  315      315
C                                                                            A.  316      316
C PC BOARDS ----------------------------------                               A.  317      317
C            12.*3.413 $ TM CURRENT SIG COND                                 A.  318      318
C            15.*3.413 $ PRE REG                                             A.  319      319
C            10.*3.413 $ DC-DC CONVERTER                                     A.  320      320
C             5.*3.413 $ POST REG                                            A.  321      321
C             2.*3.413 $ CNTRL                                               A.  322      322
```

```
INPUT CARD COL. = 12345678 1 2345678 2 2345678 3 2345678 4 2345678 5 2345678 6 2345678 7 2345678 8 EDIT NO.    CARD NO.
C              5.*3.413 $ MICRO PROCESSOR (PER MSFC PHONE CALL)                          A.  323          323
C              -----                                                                     A.  324          324
      700=    19.*3.413 $ PC TOTAL NOT INCLUDING (6) TO61                               A.  325          325
C COMPONENT STRUCTURE                                                                   A.  326          326
      130=     2.5*3.413 $ COMPONENT STRUCTURE WIRING DISSIPATION                       A.  327          327
      131=     2.5*3.413 $ COMPONENT STRUCTURE WIRING DISSIPATION                       A.  328          328
      132=     2.5*3.413 $ COMPONENT STRUCTURE WIRING DISSIPATION                       A.  329          329
      133=     2.5*3.413 $ COMPONENT STRUCTURE WIRING DISSIPATION                       A.  330          330
C                                                                                       A.  331          331
      END                                                                               A.  332          332
```

CONSTANTS DIRECTORY

INPUT=INTERNAL

1=	1 $	2=	2 $	3=	3 $	4=	4 $	5=	5 $	6=	6 $	610=	7 $	611=	8 $	12=	9
13=	10 $	614=	11 $	15=	12 $	620=	13 $	621=	14 $	22=	15 $	23=	16 $	624=	17 $	25=	18
630=	19 $	631=	20 $	32=	21 $	33=	22 $	634=	23 $	35=	24 $	51=	25 $	52=	26 $	53=	27
655=	28 $	700=	29 $	130=	30 $	131=	31 $	132=	32 $	133=	33 $						

```
INPUT CARD COL. = 12345678 1 2345678 2 2345678 3 2345678 4 2345678 5 2345678 6 2345678 7 2345678 8 EDIT NO.    CARD NO.

                  BCD 3ARRAY DATA                                                    A.  333          333
                  END                                                                A.  334          334

++NOTE++ NO ARRAY DATA
```

```
INPUT CARD COL. = 12345678 1 2345678 2 2345678 3 2345678 4 2345678 5 2345678 6 2345678 7 2345678 8 EDIT NO.  CARD NO.
      BCD 3EXECUTION                                                                          A.  335      335
C VARY PWR STG POWER                                                                          A.  336      336
        R610= R610*1.000                                                                      A.  337      337
        R611= R611*1.000                                                                      A.  338      338
        R614= R614*1.000                                                                      A.  339      339
        R620= R620*1.000                                                                      A.  340      340
        R621= R621*1.000                                                                      A.  341      341
        R624= R624*1.000                                                                      A.  342      342
        R630= R630*1.000                                                                      A.  343      343
        R631= R631*1.000                                                                      A.  344      344
        R634= R634*1.000                                                                      A.  345      345
C CONDUCTANCE TO COLD PLATE WITH SPACE LAB FILLER                                             A.  346      346
C                                                                                             A.  347      347
      STDSTL                                                                                  A.  348      348
C                                                                                             A.  349      349
C CONDUCTANCE TO COLDPLATE  WITH AL ADAPTER PLATE                                             A.  350      350
        G263=  G263/2.0                                                                       A.  351      351
        G264=  G264/2.0                                                                       A.  352      352
        G265=  G265/2.0                                                                       A.  353      353
        G266=  G266/2.0                                                                       A.  354      354
        G267=  G267/2.0                                                                       A.  355      355
        G268=  G268/2.0                                                                       A.  356      356
        G269=  G269/2.0                                                                       A.  357      357
        G270=  G270/2.0                                                                       A.  358      358
        G271=  G271/2.0                                                                       A.  359      359
C                                                                                             A.  360      360
      STDSTL                                                                                  A.  361      361
C                                                                                             A.  362      362
C CONDUCTANCE TO COLDPLATE  WITH NO FILLER                                                    A.  363      363
        G263= 0.0                                                                             A.  364      364
        G264= 0.0                                                                             A.  365      365
        G265= 0.0                                                                             A.  366      366
        G266= 0.0                                                                             A.  367      367
        G267= 0.0                                                                             A.  368      368
        G268= 0.0                                                                             A.  369      369
        G269= 0.0                                                                             A.  370      370
        G270= 0.0                                                                             A.  371      371
        G271= 0.0                                                                             A.  372      372
        G272= 1.78*6.                                                                         A.  373      373
        G273= 1.78*6.                                                                         A.  374      374
        G274= 1.78*12.                                                                        A.  375      375
        G275= 1.78*12.                                                                        A.  376      376
C                                                                                             A.  377      377
      STDSTL                                                                                  A.  378      378
C                                                                                             A.  379      379
      END                                                                                     A.  380      380
```

```
INPUT CARD COL. = 12345678 1 2345678 2 2345678 3 2345678 4 2345678 5 2345678 6 2345678 7 2345678 8 EDIT NO.   CARD NO.
 BCD 3VARIABLES 1                                                                          A.  381          381
Q1= R1                                                                                     A.  382          382
Q2= R2                                                                                     A.  383          383
Q3= R3                                                                                     A.  384          384
Q4= R4                                                                                     A.  385          385
Q5= R5                                                                                     A.  386          386
Q6= R6                                                                                     A.  387          387
Q610= R610                                                                                 A.  388          388
Q611= R611                                                                                 A.  389          389
Q12= R12                                                                                   A.  390          390
Q13= R13                                                                                   A.  391          391
Q614= R614                                                                                 A.  392          392
Q15= R15                                                                                   A.  393          393
Q620= R620                                                                                 A.  394          394
Q621= R621                                                                                 A.  395          395
Q22= R22                                                                                   A.  396          396
Q23= R23                                                                                   A.  397          397
Q624= R624                                                                                 A.  398          398
Q25= R25                                                                                   A.  399          399
Q630= R630                                                                                 A.  400          400
Q631= R631                                                                                 A.  401          401
Q32= R32                                                                                   A.  402          402
Q33= R33                                                                                   A.  403          403
Q634= R634                                                                                 A.  404          404
Q35= R35                                                                                   A.  405          405
Q655= R655                                                                                 A.  406          406
Q700= R700+R51+R52+R53                                                                     A.  407          407
Q130= R130                                                                                 A.  408          408
Q131= R131                                                                                 A.  409          409
Q132= R132                                                                                 A.  410          410
Q133= R133                                                                                 A.  411          411
 END                                                                                       A.  412          412
```

```
INPUT CARD COL. = 12345678 1 2345678 2 2345678 3 2345678 4 2345678 5 2345678 6 2345678 7 2345678 8 EDIT NO.    CARD NO.
                  BCD 3VARIABLES 2                                                                A.  413        413
                  END                                                                             A.  414        414
```

```
INPUT CARD COL. = 12345678 1 2345678 2 2345678 3 2345678 4 2345678 5 2345678 6 2345678 7 2345678 8 EDIT NO.  CARD NO.
      BCD 3OUTPUT CALLS                                                                          A.  415      415
C                                                                                                A.  416      416
C AVERAGE COMPONENT TEMPERATURE (DOES NOT INCLUDE XTRS OR DIODES)                                A.  417      417
C  AREA WEIGHTED                                                                                A.  418      418
      X1= (.020*T1+.466*T2+.309*T3+.020*T4+.020*T5)                                              A.  419      419
      X2= (.020*T6+.425*T12+.014*T13+.270*T15+.425*T22 )                                         A.  420      420
      X3= (.014*T23+.270*T25)                                                                    A.  421      421
      X4= (.425*T32+.014*T33+.270*T35 )                                                          A.  422      422
      T2000= (X1+X2+X3+X4 )/(2.978)                                                              A.  423      423
C                                                                                                A.  424      424
C                                        AVERAGE CASE(SIDES&TOP) TEMPERATURE                     A.  425      425
      T2001=(.49*T130+.49*T132+1.14*T133+1.14*T131+1.88*T105)/5.14                               A.  426      426
C                                                                                                A.  427      427
      TPRINT                                                                                     A.  428      428
C                                                                                                A.  429      429
C   TEMPERATURES DEGREES C                                                                       A.  430      430
F     DO 100 I=1,NNT                                                                             A.  431      431
F100  T(I)= (5./9.)*( T(I) - 32.)                                                                A.  432      432
C                                                                                                A.  433      433
      TPRINT                                                                                     A.  434      434
C                                                                                                A.  435      435
F     DO 102 I=1,NNT                                                                             A.  436      436
F102  T(I)= (9./5.)*T(I) +  32.                                                                  A.  437      437
C                                                                                                A.  438      438
      END                                                                                        A.  439      439
```

```
INPUT CARD COL. = 12345678 1 2345678 2 2345678 3 2345678 4 2345678 5 2345678 6 2345678 7 2345678 8 EDIT NO.    CARD NO.
                  BCD 3SUBROUTINE DATA                                                          A.  440          440
                  END                                                                           A.  441           44
                  BCD 3END OF DATA                                                              A.  442          442
```

++NOTE++ -STDSTL- REQUIRES 136 WORDS OF DYNAMIC STORAGE

TIMEN = 0. EBALSC = 0. CSGMIN(0) = 0. DRLXCC(0) = 0.
TSTEPU = 0. EBALNC(0) = 0. CSGMAX(0) = 0. ARLXCC(0) = 0.
ITERCT = 1 DMXTCC(0) = 0. AMXTCC(0) = 0.

DIFFUSION NODES

T	1=	150.000	T	2=	150.000	T	3=	150.000	T	4=	150.000	T	5=	150.000	T	6=	150.000
T	10=	150.000	T	11=	150.000	T	12=	150.000	T	13=	150.000	T	14=	150.000	T	15=	150.000
T	20=	150.000	T	21=	150.000	T	22=	150.000	T	23=	150.000	T	24=	150.000	T	25=	150.000
T	30=	150.000	T	31=	150.000	T	32=	150.000	T	33=	150.000	T	34=	150.000	T	35=	150.000
T	55=	150.000	T	610=	150.000	T	611=	150.000	T	614=	150.000	T	620=	150.000	T	621=	150.000
T	624=	150.000	T	630=	150.000	T	631=	150.000	T	634=	150.000	T	655=	150.000	T	105=	150.000
T	121=	150.000	T	122=	150.000	T	123=	150.000	T	124=	150.000	T	125=	150.000	T	126=	150.000
T	127=	150.000	T	128=	150.000	T	129=	150.000	T	130=	150.000	T	131=	150.000	T	132=	150.000
T	133=	150.000	T	151=	150.000	T	152=	150.000	T	153=	150.000	T	154=	150.000	T	155=	150.000
T	111=	150.000	T	112=	150.000	T	113=	150.000	T	700=	150.000	T					

ARITHMETIC NODES

T	170=	150.000	T	171=	150.000	T	172=	150.000	T	173=	150.000	T	174=	150.000	T	175=	150.000
T	176=	150.000	T	177=	150.000	T	178=	150.000	T	501=	150.000	T					

HEATER NODES

++NONE++

BOUNDARY NODES

T	1000=	50.0000	T	1001=	10.0000E+01	T	2000=	150.201	T	2001=	150.000	T					

TIMEN = 0. EBALSC = 0. CSGMIN(0) = 0. DRLXCC(0) = 0.
TSTEPU = 0. EBALNC(0) = 0. CSGMAX(0) = 0. ARLXCC(0) = 0.
ITERCT = 1 DMXTCC(0) = 0. AMXTCC(0) = 0.

DIFFUSION NODES

T	1=	65.5556	T	2=	65.5556	T	3=	65.5556	T	4=	65.5556	T	5=	65.5556	T	6=	65.5556
T	10=	65.5556	T	11=	65.5556	T	12=	65.5556	T	13=	65.5556	T	14=	65.5556	T	15=	65.5556
T	20=	65.5556	T	21=	65.5556	T	22=	65.5556	T	23=	65.5556	T	24=	65.5556	T	25=	65.5556
T	30=	65.5556	T	31=	65.5556	T	32=	65.5556	T	33=	65.5556	T	34=	65.5556	T	35=	65.5556
T	55=	65.5556	T	610=	65.5556	T	611=	65.5556	T	614=	65.5556	T	620=	65.5556	T	621=	65.5556
T	624=	65.5556	T	630=	65.5556	T	631=	65.5556	T	634=	65.5556	T	655=	65.5556	T	105=	65.5556
T	121=	65.5556	T	122=	65.5556	T	123=	65.5556	T	124=	65.5556	T	125=	65.5556	T	126=	65.5556
T	127=	65.5556	T	128=	65.5556	T	129=	65.5556	T	130=	65.5556	T	131=	65.5556	T	132=	65.5556
T	133=	65.5556	T	151=	65.5556	T	152=	65.5556	T	153=	65.5556	T	154=	65.5556	T	155=	65.5556
T	111=	65.5556	T	112=	65.5556	T	113=	65.5556	T	700=	65.5556	T					

ARITHMETIC NODES

T	170=	65.5556	T	171=	65.5556	T	172=	65.5556	T	173=	65.5556	T	174=	65.5556	T	175=	65.5556
T	176=	65.5556	T	177=	65.5556	T	178=	65.5556	T	501=	65.5556	T					

HEATER NODES

++NONE++

BOUNDARY NODES

T	1000=	1.00000E+01	T	1001=	37.7778	T	2000=	65.6675	T	2001=	65.5556	T					

++NOTE++ BOTH DRLXCA(1.000000E-03) AND ARLXCA(1.000000E-03) HAVE BEEN MET ON ITERATION 50.

TIMEN = 0. EBALSC = 0. CSGMIN(0) = 0. DRLXCC(634) = 9.771277E-04
TSTEPU = 0. EBALNC(0) = 0. CSGMAX(0) = 0. ARLXCC(501) = 2.268736E-05
ITERCT = 50 DMXTCC(0) = 0. AMXTCC(0) = 0.

DIFFUSION NODES

T	1=	125.971	T	2=	71.1578	T	3=	62.0607	T	4=	85.9112	T	5=	85.9112	T	6=	85.9112
T	10=	164.254	T	11=	178.736	T	12=	70.3490	T	13=	98.2599	T	14=	116.681	T	15=	143.990
T	20=	164.654	T	21=	179.135	T	22=	70.9882	T	23=	98.9319	T	24=	117.080	T	25=	143.990
T	30=	164.704	T	31=	179.185	T	32=	70.7531	T	33=	98.6953	T	34=	117.131	T	35=	143.990
T	55=	127.130	T	610=	200.257	T	611=	221.902	T	614=	138.282	T	620=	200.656	T	621=	222.301
T	624=	138.682	T	630=	200.706	T	631=	222.351	T	634=	138.733	T	655=	145.131	T	105=	74.4852
T	121=	54.8545	T	122=	55.4114	T	123=	55.7399	T	124=	67.4367	T	125=	56.1882	T	126=	67.0375
T	127=	56.4320	T	128=	67.4899	T	129=	58.7050	T	130=	81.7026	T	131=	71.4556	T	132=	71.1861
T	133=	70.4785	T	151=	114.202	T	152=	59.5151	T	153=	63.2172	T	154=	63.4048	T	155=	62.5353
T	111=	101.168	T	112=	101.567	T	113=	101.619	T	700=	176.071	T					

ARITHMETIC NODES

T	170=	57.5062	T	171=	59.3084	T	172=	57.5194	T	173=	61.8667	T	174=	62.0869	T	175=	61.0659
T	176=	62.2721	T	177=	61.8662	T	178=	64.0094	T	501=	80.9709	T					

HEATER NODES

++NONE++

BOUNDARY NODES

T	1000=	50.0000	T	1001=	10.0000E+01	T	2000=	90.9434	T	2001=	73.2982	T			

TIMEN = 0. EBALSC = 0. CSGMIN(0) = 0. DRLXCC(634) = 9.771277E-04
TSTEPU = 0. EBALNC(0) = 0. CSGMAX(0) = 0. ARLXCC(501) = 2.268736E-05
ITERCT = 50 DMXTCC(0) = 0. AMXTCC(0) = 0.

DIFFUSION NODES

T	1=	52.2059	T	2=	21.7544	T	3=	16.7004	T	4=	29.9507	T	5=	29.9507	T	6=	29.9507
T	10=	73.4747	T	11=	81.5199	T	12=	21.3050	T	13=	35.6999	T	14=	47.0451	T	15=	62.2168
T	20=	73.6985	T	21=	81.7417	T	22=	21.6490	T	23=	36.0733	T	24=	47.2689	T	25=	62.2168
T	30=	73.7244	T	31=	81.7696	T	32=	21.5279	T	33=	35.9418	T	34=	47.2953	T	35=	62.2168
T	55=	52.2502	T	610=	93.4759	T	611=	105.501	T	614=	59.0458	T	620=	93.6977	T	621=	105.723
T	624=	59.2676	T	630=	93.7256	T	631=	105.751	T	634=	59.2950	T	655=	62.8507	T	105=	23.6029
T	121=	12.6970	T	122=	13.0063	T	123=	13.1888	T	124=	19.6871	T	125=	13.4379	T	126=	19.4653
T	127=	13.5733	T	128=	19.7165	T	129=	14.8361	T	130=	27.6125	T	131=	21.9198	T	132=	21.7701
T	133=	21.3759	T	151=	45.6679	T	152=	15.2862	T	153=	17.3429	T	154=	17.4471	T	155=	16.9641
T	111=	38.4284	T	112=	38.6482	T	113=	38.6772	T	700=	80.0396	T					

ARITHMETIC NODES

T	170=	14.1701	T	171=	15.1713	T	172=	14.1774	T	173=	16.5926	T	174=	16.7149	T	175=	16.1477
T	176=	16.8178	T	177=	16.5923	T	178=	17.7630	T	501=	27.2061	T					

HEATER NODES

++NONE++

BOUNDARY NODES

T	1000=	1.000000E+01	T	1001=	37.7778	T	2000=	32.7463	T	2001=	22.9434	T			

++NOTE++ EBALSA(1.000000E-03) HAS BEEN MET ON ITERATION 53.

TIMEN = 0. EBALSC =-5.550631E-04 CSGMIN(0) = 0. DRLXCC(132) =-3.917880E-04
TSTEPU = 0. EBALNC(128) =-1.063568E-03 CSGMAX(0) = 0. ARLXCC(176) =-1.270963E-04
ITERCT = 53 DMXTCC(0) = 0. AMXTCC(0) = 0.

DIFFUSION NODES

T	1=	125.971	T	2=	71.1579	T	3=	62.0608	T	4=	85.9113	T	5=	85.9113	T	6=	85.9113
T	10=	164.254	T	11=	178.736	T	12=	70.3490	T	13=	96.2599	T	14=	116.681	T	15=	143.990
T	20=	164.654	T	21=	179.135	T	22=	70.9382	T	23=	96.9320	T	24=	117.080	T	25=	143.990
T	30=	164.708	T	31=	179.189	T	32=	70.7501	T	33=	96.6953	T	34=	117.134	T	35=	143.990
T	55=	127.130	T	610=	200.257	T	611=	221.902	T	614=	138.282	T	620=	200.656	T	621=	222.301
T	624=	138.682	T	630=	200.710	T	631=	222.355	T	634=	138.736	T	655=	145.131	T	105=	74.4853
T	121=	54.8545	T	122=	55.4114	T	123=	55.7399	T	124=	67.4367	T	125=	56.1883	T	126=	67.0375
T	127=	56.4320	T	128=	67.4906	T	129=	58.7051	T	130=	81.7026	T	131=	71.4557	T	132=	71.1863
T	133=	70.4785	T	151=	114.202	T	152=	59.5151	T	153=	63.2173	T	154=	63.4049	T	155=	62.5355
T	111=	101.168	T	112=	101.567	T	113=	101.621	T	700=	176.071	T					

ARITHMETIC NODES

T	170=	57.5062	T	171=	59.3084	T	172=	57.5194	T	173=	61.8667	T	174=	62.0871	T	175=	61.0661
T	176=	62.2722	T	177=	61.8663	T	178=	64.0095	T	501=	80.9710	T					

HEATER NODES

++NONE++

BOUNDARY NODES

T	1000=	50.0000	T	1001=	10.0000E+01	T	2000=	90.9435	T	2001=	73.2983	T					

TIMEN = 0. EBALSC =-5.550631E-04 CSGMIN(0) = 0. DRLXCC(132) =-3.917880E-04
TSTEPU = 0. EBALNC(128) =-1.063568E-03 CSGMAX(0) = 0. ARLXCC(176) =-1.270963E-04
ITERCT = 53 DMXTCC(0) = 0. AMXTCC(0) = 0.

DIFFUSION NODES

T	1=	52.2059	T	2=	21.7544	T	3=	16.7005	T	4=	29.9507	T	5=	29.9507	T	6=	29.9507
T	10=	73.4747	T	11=	81.5198	T	12=	21.3050	T	13=	35.6999	T	14=	47.0451	T	15=	62.2168
T	20=	73.6964	T	21=	81.7416	T	22=	21.5490	T	23=	36.0733	T	24=	47.2668	T	25=	62.2168
T	30=	73.7264	T	31=	81.7716	T	32=	21.5279	T	33=	35.9418	T	34=	47.2968	T	35=	62.2168
T	55=	52.8501	T	610=	93.4758	T	611=	105.501	T	614=	59.0458	T	620=	93.6976	T	621=	105.723
T	624=	59.2676	T	630=	93.7276	T	631=	105.753	T	634=	59.2975	T	655=	62.8507	T	105=	23.6030
T	121=	12.6970	T	122=	13.0053	T	123=	13.1666	T	124=	19.6871	T	125=	13.4379	T	126=	19.4653
T	127=	13.5733	T	128=	19.7170	T	129=	14.8382	T	130=	27.6126	T	131=	21.9198	T	132=	21.7702
T	133=	21.3770	T	151=	45.6679	T	152=	15.2862	T	153=	17.3429	T	154=	17.6472	T	155=	16.9642
T	111=	38.4264	T	112=	38.6482	T	113=	38.6781	T	700=	80.0396	T					

ARITHMETIC NODES

T	170=	14.1701	T	171=	15.1713	T	172=	14.1774	T	173=	16.5926	T	174=	16.7150	T	175=	16.1479
T	176=	16.8179	T	177=	16.5924	T	178=	17.7831	T	501=	27.2061	T					

HEATER NODES

++NONE++

BOUNDARY NODES

T	1000=	1.00000E+01	T	1001=	37.7778	T	2000=	32.7464	T	2001=	22.9435	T					

++NOTE++ EBALNA(1.000000E-03) HAS BEEN MET ON ITERATION 54.

TIMEN = 0. EBALSC =-2.783245E-04 CSGMIN(0) = 0. DRLXCC(33) = 6.218462E-05
TSTEPU = 0. EBALNC(128) =-3.152036E-04 CSGMAX(0) = 0. ARLXCC(176) =-2.658832E-05
ITERCT = 54 DMXTCC(0) = 0. AMXTCC(0) = 0.

DIFFUSION NODES

T	1=	125.971	T	2=	71.1579	T	3=	62.0608	T	4=	85.9113	T	5=	85.9113	T	6=	85.9113
T	10=	164.254	T	11=	178.736	T	12=	70.3490	T	13=	96.2599	T	14=	116.681	T	15=	143.990
T	20=	164.654	T	21=	179.135	T	22=	70.9682	T	23=	96.9320	T	24=	117.080	T	25=	143.990
T	30=	164.708	T	31=	179.189	T	32=	70.7502	T	33=	96.6953	T	34=	117.134	T	35=	143.990
T	55=	127.130	T	610=	200.257	T	611=	221.902	T	614=	138.282	T	620=	200.656	T	621=	222.301
T	624=	138.682	T	630=	200.710	T	631=	222.355	T	634=	138.736	T	655=	145.131	T	105=	74.4854
T	121=	54.8545	T	122=	55.4114	T	123=	55.7399	T	124=	67.4367	T	125=	56.1883	T	126=	67.0375
T	127=	56.4320	T	128=	67.4906	T	129=	58.7051	T	130=	81.7026	T	131=	71.4557	T	132=	71.1863
T	133=	70.4785	T	151=	114.202	T	152=	59.5151	T	153=	63.2173	T	154=	63.4050	T	155=	62.5355
T	111=	101.168	T	112=	101.567	T	113=	101.621	T	700=	176.071	T					

ARITHMETIC NODES

T	170=	57.5082	T	171=	59.0084	T	172=	57.5104	T	173=	61.8667	T	174=	62.0871	T	175=	61.0661
T	176=	62.2721	T	177=	61.8663	T	178=	64.0095	T	501=	80.9710	T					

HEATER NODES

++NONE++

BOUNDARY NODES

T	1000=	50.0000	T	1001=	10.0000E+01	T	2000=	90.9435	T	2001=	73.2983	T					

TIMEN = 0. EBALSC =-2.783245E-04 CSGMIN(0) = 0. DRLXCC(33) = 6.218462E-05
TSTEPU = 0. EBALNC(128) =-3.152036E-04 CSGMAX(0) = 0. ARLXCC(176) =-2.658832E-05
ITERCT = 54 DMXTCC(0) = 0. AMXTCC(0) = 0.

DIFFUSION NODES

T	1=	52.2059	T	2=	21.7544	T	3=	16.7005	T	4=	29.9507	T	5=	29.9507	T	6=	29.9507
T	10=	73.4747	T	11=	81.5198	T	12=	21.3050	T	13=	35.6999	T	14=	47.0451	T	15=	62.2168
T	20=	73.6964	T	21=	81.7416	T	22=	21.6490	T	23=	36.0733	T	24=	47.2669	T	25=	62.2168
T	30=	73.7264	T	31=	81.7716	T	32=	21.5279	T	33=	35.9418	T	34=	47.2968	T	35=	62.2168
T	55=	52.8501	T	610=	93.4758	T	611=	105.501	T	614=	59.0458	T	620=	93.6976	T	621=	105.723
T	624=	59.2576	T	630=	93.7276	T	631=	105.753	T	634=	59.2975	T	655=	62.8507	T	105=	23.6030
T	121=	12.6070	T	122=	13.0033	T	123=	13.1933	T	124=	19.6071	T	125=	13.4379	T	126=	19.4653
T	127=	13.5733	T	128=	19.7170	T	129=	14.8382	T	130=	27.6126	T	131=	21.9198	T	132=	21.7701
T	133=	21.3770	T	151=	45.6679	T	152=	15.2382	T	153=	17.3429	T	154=	17.4472	T	155=	16.9642
T	111=	38.4264	T	112=	38.6482	T	113=	38.6781	T	700=	80.0396	T					

ARITHMETIC NODES

T	170=	14.1701	T	171=	15.1713	T	172=	14.1774	T	173=	16.5926	T	174=	16.7150	T	175=	16.1478
T	176=	16.8178	T	177=	16.5924	T	178=	17.7831	T	501=	27.2061	T					

HEATER NODES

++NONE++

BOUNDARY NODES

T	1000=	1.00000E+01	T	1001=	37.7778	T	2000=	32.7464	T	2001=	22.9435	T					

++NOTE++ -STDSTL- REQUIRES 136 WORDS OF DYNAMIC STORAGE

TIMEN = 0.
TSTEPU = 0.

EBALSC =-2.783245E-04
EBALNC(128) =-3.152036E-04
ITERCT = 1

CSGMIN(0) = 0.
CSGMAX(0) = 0.
DMXTCC(0) = 0.

DRLXCC(33) = 6.218462E-05
ARLXCC(176) =-2.658832E-05
AMXTCC(0) = 0.

DIFFUSION NODES

T	1=	125.971	T	2=	71.1579	T	3=	62.0608	T	4=	85.9113	T	5=	85.9113
T	6=	85.9113	T	10=	164.254	T	11=	178.736	T	12=	70.3490	T	13=	96.2599
T	14=	116.681	T	15=	143.990	T	20=	164.654	T	21=	179.135	T	22=	70.9682
T	23=	96.9320	T	24=	117.080	T	25=	143.990	T	30=	164.708	T	31=	179.189
T	32=	70.7502	T	33=	96.6953	T	34=	117.134	T	35=	143.990	T	55=	127.130
T	610=	200.257	T	611=	221.902	T	614=	138.282	T	620=	200.656	T	621=	222.301
T	624=	138.682	T	630=	200.710	T	631=	222.355	T	634=	138.736	T	655=	145.131
T	105=	74.4854	T	121=	54.8545	T	122=	55.4114	T	123=	55.7399	T	124=	67.4367
T	125=	56.1883	T	126=	67.0375	T	127=	56.4320	T	128=	67.4906	T	129=	58.7051
T	130=	81.7026	T	131=	71.4557	T	132=	71.1863	T	133=	70.4785	T	151=	114.202
T	152=	59.5151	T	153=	63.2173	T	154=	63.4050	T	155=	62.5355	T	111=	101.168
T	112=	101.567	T	113=	101.621	T	700=	176.071	T					

ARITHMETIC NODES

T	170=	57.5062	T	171=	59.3084	T	172=	57.5194	T	173=	61.8667	T	174=	62.0871
T	175=	61.0661	T	176=	62.2721	T	177=	61.8663	T	178=	64.0095	T	501=	80.9710
T														

HEATER NODES

++NONE++

BOUNDARY NODES

T	1000=	50.0000	T	1001=	10.0000E+01	T	2000=	90.9435	T	2001=	73.2983	T		

TIMEN = 0.
TSTEPU = 0.

EBALSC =-2.783245E-04
EBALNC(128) =-3.152036E-04
ITERCT = 1

CSGMIN(0) = 0.
CSGMAX(0) = 0.
DMXTCC(0) = 0.

DRLXCC(33) = 6.218462E-05
ARLXCC(176) =-2.658832E-05
AMXTCC(0) = 0.

DIFFUSION NODES

T	1=	52.2059	T	2=	21.7544	T	3=	16.7005	T	4=	29.9507	T	5=	29.9507
T	6=	29.9507	T	10=	73.4747	T	11=	81.5198	T	12=	21.3050	T	13=	35.6999
T	14=	47.0451	T	15=	62.2168	T	20=	73.6964	T	21=	81.7416	T	22=	21.6490
T	23=	36.0733	T	24=	47.2669	T	25=	62.2168	T	30=	73.7234	T	31=	81.7716
T	32=	21.5979	T	33=	35.9418	T	34=	47.2968	T	35=	62.2168	T	55=	52.8501
T	610=	93.4758	T	611=	105.501	T	614=	59.0458	T	620=	93.6976	T	621=	105.723
T	624=	59.2676	T	630=	93.7276	T	631=	105.793	T	634=	59.2975	T	655=	62.8507
T	105=	23.6030	T	121=	12.8977	T	122=	13.0063	T	123=	13.1888	T	124=	19.6871
T	125=	13.4379	T	126=	19.4653	T	127=	13.5733	T	128=	19.7170	T	129=	14.8362
T	130=	27.6126	T	131=	21.9198	T	132=	21.7701	T	133=	21.3770	T	151=	45.6679
T	152=	15.2062	T	153=	17.3429	T	154=	17.4472	T	155=	16.9642	T	111=	38.4264
T	112=	38.6482	T	113=	38.6781	T	700=	80.0396	T					

ARITHMETIC NODES

T	170=	14.1701	T	171=	15.1713	T	172=	14.1774	T	173=	16.5926	T	174=	16.7150
T	175=	16.1478	T	176=	16.8178	T	177=	16.5924	T	178=	17.7831	T	501=	27.2061
T														

HEATER NODES

++NONE++

BOUNDARY NODES

T	1000=	1.00000E+01	T	1001=	37.7778	T	2000=	32.7464	T	2001=	22.9435	T		

++NOTE++ BOTH DRLXCA(1.000000E-03) AND ARLXCA(1.000000E-03) HAVE BEEN MET ON ITERATION 35.

TIMEN = 0. EBALSC =-2.783245E-04 CSGMIN(0) = 0. DRLXCC(634) =-6.783290E-04
TSTEPU = 0. EBALNC(128) =-3.152036E-04 CSGMAX(0) = 0. ARLXCC(501) =-2.626782E-04
ITERCT = 35 DMXTCC(0) = 0. AMXTCC(0) = 0.

DIFFUSION NODES

T 1=	135.204	T 2=	80.4430	T 3=	71.3917	T 4=	95.1882	T 5=	95.1882	T 6=	95.1882
T 10=	177.520	T 11=	192.001	T 12=	78.4016	T 13=	104.170	T 14=	129.947	T 15=	150.315
T 20=	178.592	T 21=	193.073	T 22=	79.9194	T 23=	105.823	T 24=	131.019	T 25=	150.315
T 30=	178.710	T 31=	193.191	T 32=	79.4433	T 33=	105.305	T 34=	131.136	T 35=	150.315
T 55=	134.193	T 610=	213.522	T 611=	235.167	T 614=	151.548	T 620=	214.594	T 621=	236.240
T 624=	152.621	T 630=	214.712	T 631=	236.357	T 634=	152.737	T 655=	152.194	T 105=	83.7638
T 121=	60.9757	T 122=	62.4787	T 123=	63.6455	T 124=	81.3772	T 125=	64.8155	T 126=	80.3022
T 127=	65.3505	T 128=	81.4909	T 129=	67.9982	T 130=	89.4514	T 131=	81.2737	T 132=	80.5191
T 133=	79.8266	T 151=	121.265	T 152=	67.9318	T 153=	73.9865	T 154=	74.4776	T 155=	72.9807
T 111=	114.433	T 112=	115.507	T 113=	115.622	T 700=	181.221	T			

ARITHMETIC NODES

T 170=	63.7881	T 171=	65.9616	T 172=	65.7328	T 173=	72.8426	T 174=	73.4193	T 175=	71.6615
T 176=	71.5766	T 177=	71.3382	T 178=	74.5341	T 501=	89.6992	T			

HEATER NODES

++NONE++

BOUNDARY NODES

T 1000=	50.0000	T 1001=	10.0000E+01	T 2000=	99.1206	T 2001=	82.5712	T

TIMEN = 0. EBALSC =-2.783245E-04 CSGMIN(0) = 0. DRLXCC(634) =-6.783290E-04
TSTEPU = 0. EBALNC(128) =-3.152036E-04 CSGMAX(0) = 0. ARLXCC(501) =-2.626782E-04
ITERCT = 35 DMXTCC(0) = 0. AMXTCC(0) = 0.

DIFFUSION NODES

T 1=	57.3355	T 2=	26.9128	T 3=	21.8843	T 4=	35.1045	T 5=	35.1045	T 6=	35.1045
T 10=	80.8445	T 11=	88.8896	T 12=	25.7787	T 13=	40.0943	T 14=	54.4147	T 15=	65.7306
T 20=	81.4401	T 21=	89.4852	T 22=	26.6219	T 23=	41.0130	T 24=	55.0108	T 25=	65.7306
T 30=	81.5054	T 31=	89.5506	T 32=	26.3574	T 33=	40.7248	T 34=	55.0755	T 35=	65.7306
T 55=	56.7739	T 610=	100.846	T 611=	112.871	T 614=	68.4154	T 620=	101.441	T 621=	113.466
T 624=	67.0115	T 630=	101.567	T 631=	113.592	T 634=	67.0762	T 655=	66.7745	T 105=	28.7577
T 121=	16.0976	T 122=	16.9326	T 123=	17.5808	T 124=	27.4318	T 125=	18.2308	T 126=	26.8345
T 127=	18.5281	T 128=	27.4949	T 129=	19.9000	T 130=	31.9175	T 131=	27.3743	T 132=	26.9550
T 133=	26.5703	T 151=	49.5916	T 152=	19.9321	T 153=	23.3258	T 154=	23.5987	T 155=	22.7671
T 111=	45.7958	T 112=	46.3925	T 113=	46.4504	T 700=	82.9004	T			

ARITHMETIC NODES

T 170=	17.6601	T 171=	18.8675	T 172=	18.7404	T 173=	22.6903	T 174=	23.0107	T 175=	22.0342
T 176=	21.9670	T 177=	21.8545	T 178=	23.6300	T 501=	32.0551	T			

HEATER NODES

++NONE++

BOUNDARY NODES

T 1000=	1.00000E+01	T 1001=	37.7778	T 2000=	37.2892	T 2001=	28.0951	T

++NOTE++ EBALSA(1.000000E-03) HAS BEEN MET ON ITERATION 43.

```
TIMEN  = 0.              EBALSC          =-4.358904E-05  CSGMIN(     0) = 0.          DRLXCC(   132) =-2.140046E-03
TSTEPU = 0.              EBALNC(   105) =-6.609835E-04  CSGMAX(     0) = 0.          ARLXCC(   501) = 6.165467E-05
                         ITERCT          =        43     DMXTCC(     0) = 0.          AMXTCC(     0) = 0.

                                                    DIFFUSION NODES
T    1=  135.203    T    2=  80.4426    T    3=  71.3913    T    4=  95.1878    T    5=  95.1878    T    6=  95.1878
T   10=  177.519    T   11=  192.000    T   12=  78.4014    T   13=  104.170    T   14=  129.945    T   15=  150.315
T   20=  178.595    T   21=  193.076    T   22=  79.9192    T   23=  105.823    T   24=  131.021    T   25=  150.315
T   30=  178.707    T   31=  193.188    T   32=  79.4430    T   33=  105.304    T   34=  131.134    T   35=  150.315
T   55=  134.193    T  610=  213.521    T  611=  235.166    T  614=  151.547    T  620=  214.597    T  621=  236.242
T  624=  152.623    T  630=  214.709    T  631=  236.354    T  634=  152.735    T  655=  152.194    T  105=  83.7632
T  121=  60.9755    T  122=  62.4786    T  123=  63.6454    T  124=  81.3777    T  125=  64.8153    T  126=  80.3018
T  127=  65.3504    T  128=  81.4902    T  129=  67.9980    T  130=  89.4509    T  131=  81.2732    T  132=  80.5185
T  133=  79.8261    T  151=  121.265    T  152=  67.9316    T  153=  73.9864    T  154=  74.4774    T  155=  72.9803
T  111=  114.432    T  112=  115.508    T  113=  115.620    T  700=  181.220    T
                                                  ARITHMETIC NODES
T  170=  63.7879    T  171=  65.9614    T  172=  65.7326    T  173=  72.8425    T  174=  73.4191    T  175=  71.6611
T  176=  71.5752    T  177=  71.3380    T  178=  74.5337    T  501=  89.6987    T
                                                    HEATER NODES
                                                     ++NONE++
                                                  BOUNDARY NODES
T 1000=  50.0000    T 1001=  10.0000E+01 T 2000=  99.1202    T 2001=  82.5706    T

TIMEN  = 0.              EBALSC          =-4.358904E-05  CSGMIN(     0) = 0.          DRLXCC(   132) =-2.140046E-03
TSTEPU = 0.              EBALNC(   105) =-6.609835E-04  CSGMAX(     0) = 0.          ARLXCC(   501) = 6.165467E-05
                         ITERCT          =        43     DMXTCC(     0) = 0.          AMXTCC(     0) = 0.

                                                    DIFFUSION NODES
T    1=  57.3353    T    2=  26.9125    T    3=  21.8840    T    4=  35.1043    T    5=  35.1043    T    6=  35.1043
T   10=  80.9437    T   11=  88.8889    T   12=  25.7785    T   13=  40.0942    T   14=  54.4141    T   15=  65.7303
T   20=  81.4414    T   21=  89.4866    T   22=  26.6218    T   23=  41.0129    T   24=  55.0118    T   25=  65.7303
T   30=  81.5039    T   31=  89.5491    T   32=  26.3572    T   33=  40.7246    T   34=  55.0743    T   35=  65.7303
T   55=  56.7737    T  610=  100.845    T  611=  112.870    T  614=  66.4148    T  620=  101.443    T  621=  113.468
T  624=  67.0125    T  630=  101.505    T  631=  113.530    T  634=  67.0750    T  655=  66.7742    T  105=  28.7573
T  121=  16.0975    T  122=  16.9025    T  123=  17.5008    T  124=  27.4320    T  125=  18.2307    T  126=  26.8343
T  127=  18.5280    T  128=  27.4945    T  129=  19.9989    T  130=  31.9172    T  131=  27.3740    T  132=  26.9547
T  133=  26.5701    T  151=  49.5914    T  152=  19.9620    T  153=  23.3258    T  154=  23.5985    T  155=  22.7668
T  111=  45.7954    T  112=  46.3931    T  113=  46.4556    T  700=  82.9002    T
                                                  ARITHMETIC NODES
T  170=  17.6599    T  171=  18.8674    T  172=  18.7403    T  173=  22.6903    T  174=  23.0106    T  175=  22.0340
T  176=  21.9368    T  177=  21.8545    T  178=  23.6298    T  501=  32.0549    T
                                                    HEATER NODES
                                                     ++NONE++
                                                  BOUNDARY NODES
T 1000=  1.000000E+01 T 1001=  37.7778    T 2000=  37.2890    T 2001=  28.0948    T

++NOTE++  EBALNA( 1.000000E-03) HAS BEEN MET ON ITERATION    44.
```

TIMEN = 0. EBALSC =-2.419979E-04 CSGMIN(0) = 0. DRLXCC(105) =-9.801060E-05
TSTEPU = 0. EBALNC(105) =-1.607585E-04 CSGMAX(0) = 0. ARLXCC(501) =-2.471851E-05
ITERCT = 44 DMXTCC(0) = 0. AMXTCC(0) = 0.

DIFFUSION NODES

T	1=	135.203	T	2=	80.4426	T	3=	71.3913	T	4=	95.1878	T	5=	95.1878	T	6=	95.1878
T	10=	177.519	T	11=	192.000	T	12=	78.4014	T	13=	104.170	T	14=	129.945	T	15=	150.315
T	20=	178.595	T	21=	193.076	T	22=	79.9192	T	23=	105.823	T	24=	131.021	T	25=	150.315
T	30=	178.707	T	31=	193.188	T	32=	79.4430	T	33=	105.304	T	34=	131.134	T	35=	150.315
T	55=	134.193	T	610=	213.521	T	611=	235.166	T	614=	151.547	T	620=	214.597	T	621=	236.242
T	624=	152.623	T	630=	214.709	T	631=	236.354	T	634=	152.735	T	655=	152.194	T	105=	83.7631
T	121=	60.9755	T	122=	62.4786	T	123=	63.6454	T	124=	81.3777	T	125=	64.8153	T	126=	80.3018
T	127=	65.3504	T	128=	81.4901	T	129=	67.9980	T	130=	89.4509	T	131=	81.2732	T	132=	80.5185
T	133=	79.8261	T	151=	121.265	T	152=	67.9316	T	153=	73.9864	T	154=	74.4774	T	155=	72.9803
T	111=	114.432	T	112=	115.508	T	113=	115.620	T	700=	181.220	T					

ARITHMETIC NODES

T	170=	63.7879	T	171=	65.9614	T	172=	55.7226	T	173=	72.8425	T	174=	73.4191	T	175=	71.6611
T	176=	71.5763	T	177=	71.3380	T	178=	74.5337	T	501=	89.6987	T					

HEATER NODES

++NONE++

BOUNDARY NODES

T	1000=	50.0000	T	1001=	10.0000E+01	T	2000=	99.1202	T	2001=	82.5706	T					

TIMEN = 0. EBALSC =-2.419979E-04 CSGMIN(0) = 0. DRLXCC(105) =-9.801060E-05
TSTEPU = 0. EBALNC(105) =-1.607585E-04 CSGMAX(0) = 0. ARLXCC(501) =-2.471851E-05
ITERCT = 44 DMXTCC(0) = 0. AMXTCC(0) = 0.

DIFFUSION NODES

T	1=	57.3353	T	2=	26.9125	T	3=	21.8841	T	4=	35.1043	T	5=	35.1043	T	6=	35.1043
T	10=	80.8437	T	11=	88.8889	T	12=	25.7786	T	13=	40.0943	T	14=	54.4141	T	15=	65.7303
T	20=	81.4414	T	21=	89.4866	T	22=	26.6218	T	23=	41.0129	T	24=	55.0118	T	25=	65.7303
T	30=	81.5039	T	31=	89.5491	T	32=	26.3572	T	33=	40.7246	T	34=	55.0743	T	35=	65.7303
T	55=	56.7737	T	610=	100.845	T	611=	112.870	T	614=	66.4148	T	620=	101.443	T	621=	113.468
T	624=	67.0125	T	630=	101.505	T	631=	113.530	T	634=	67.0750	T	655=	66.7742	T	105=	28.7573
T	121=	16.0975	T	122=	16.9325	T	123=	17.5908	T	124=	27.4320	T	125=	18.2307	T	126=	26.8343
T	127=	18.5280	T	128=	27.4945	T	129=	19.9989	T	130=	31.9172	T	131=	27.3740	T	132=	26.9547
T	133=	26.5701	T	151=	49.5914	T	152=	19.9620	T	153=	23.3258	T	154=	23.5985	T	155=	22.7668
T	111=	45.7954	T	112=	46.3931	T	113=	46.4556	T	700=	82.9002	T					

ARITHMETIC NODES

T	170=	17.6599	T	171=	18.8674	T	172=	18.7403	T	173=	22.6903	T	174=	23.0106	T	175=	22.0340
T	176=	21.9868	T	177=	21.8545	T	178=	23.6298	T	501=	32.0548	T					

HEATER NODES

++NONE++

BOUNDARY NODES

T	1000=	1.00000E+01	T	1001=	37.7778	T	2000=	37.2890	T	2001=	28.0948	T					

++NOTE++ -STDSTL- REQUIRES 136 WORDS OF DYNAMIC STORAGE

TIMEN = 0. EBALSC =-2.419979E-04 CSGMIN(0) = 0. DRLXCC(105) =-9.801060E-05
TSTEPU = 0. EBALNC(105) =-1.607585E-04 CSGMAX(0) = 0. ARLXCC(501) =-2.471851E-05
ITERCT = 1 DMXTCC(0) = 0. AMXTCC(0) = 0.

DIFFUSION NODES

T	1=	135.203	T	2=	80.4426	T	3=	71.3913	T	4=	95.1878	T	5=	95.1878	T	6=	95.1878
T	10=	177.519	T	11=	192.000	T	12=	78.4014	T	13=	104.170	T	14=	129.945	T	15=	150.315
T	20=	178.595	T	21=	193.076	T	22=	79.9192	T	23=	105.823	T	24=	131.021	T	25=	150.315
T	30=	178.707	T	31=	193.188	T	32=	79.4430	T	33=	105.304	T	34=	131.134	T	35=	150.315
T	55=	134.193	T	610=	213.521	T	611=	235.166	T	614=	151.547	T	620=	214.597	T	621=	236.242
T	624=	152.623	T	630=	214.709	T	631=	236.354	T	634=	152.735	T	655=	152.194	T	105=	83.7631
T	121=	60.9755	T	122=	62.4786	T	123=	63.6454	T	124=	81.3777	T	125=	64.8153	T	126=	80.3018
T	127=	65.3504	T	128=	81.4901	T	129=	67.9990	T	130=	89.4509	T	131=	81.2732	T	132=	80.5185
T	133=	79.8261	T	151=	121.265	T	152=	67.9316	T	153=	73.9864	T	154=	74.4774	T	155=	72.9803
T	111=	114.432	T	112=	115.508	T	113=	115.620	T	700=	181.220	T					

ARITHMETIC NODES

T	170=	63.7879	T	171=	65.9614	T	172=	65.7325	T	173=	72.8425	T	174=	73.4191	T	175=	71.6611
T	176=	71.5763	T	177=	71.3380	T	178=	74.5337	T	501=	89.6987	T					

HEATER NODES

++NONE++

BOUNDARY NODES

T	1000=	50.0000	T	1001=	10.0000E+01	T	2000=	99.1202	T	2001=	82.5706	T			

TIMEN = 0. EBALSC =-2.419979E-04 CSGMIN(0) = 0. DRLXCC(105) =-9.801060E-05
TSTEPU = 0. EBALNC(105) =-1.607585E-04 CSGMAX(0) = 0. ARLXCC(501) =-2.471851E-05
ITERCT = 1 DMXTCC(0) = 0. AMXTCC(0) = 0.

DIFFUSION NODES

T	1=	57.3353	T	2=	26.9125	T	3=	21.8841	T	4=	35.1043	T	5=	35.1043	T	6=	35.1043
T	10=	80.8437	T	11=	88.8889	T	12=	25.7786	T	13=	40.0943	T	14=	54.4141	T	15=	65.7303
T	20=	81.4414	T	21=	89.4866	T	22=	26.6218	T	23=	41.0129	T	24=	55.0118	T	25=	65.7303
T	30=	81.5039	T	31=	89.5491	T	32=	26.3572	T	33=	40.7246	T	34=	55.0743	T	35=	65.7303
T	55=	56.7737	T	610=	100.845	T	611=	112.870	T	614=	66.4148	T	620=	101.443	T	621=	113.468
T	624=	67.0125	T	630=	101.505	T	631=	113.530	T	634=	67.0750	T	655=	66.7742	T	105=	28.7573
T	121=	16.0975	T	122=	16.9325	T	123=	17.5808	T	124=	27.4320	T	125=	18.2307	T	126=	26.8343
T	127=	18.5280	T	128=	27.4945	T	129=	19.9989	T	130=	31.9172	T	131=	27.3740	T	132=	26.9547
T	133=	26.5701	T	151=	49.5914	T	152=	19.9820	T	153=	23.3258	T	154=	23.5985	T	155=	22.7668
T	111=	45.7954	T	112=	46.3931	T	113=	46.4556	T	700=	82.9002	T					

ARITHMETIC NODES

T	170=	17.6599	T	171=	18.8674	T	172=	18.7403	T	173=	22.6903	T	174=	23.0106	T	175=	22.0340
T	176=	21.9868	T	177=	21.8545	T	178=	23.6298	T	501=	32.0548	T					

HEATER NODES

++NONE++

BOUNDARY NODES

T	1000=	1.00000E+01	T	1001=	37.7778	T	2000=	37.2890	T	2001=	28.0948	T			

++NOTE++ BOTH DRLXCA(1.000000E-03) AND ARLXCA(1.000000E-03) HAVE BEEN MET ON ITERATION 65.

TIMEN = 0. EBALSC =-2.419979E-04 CSGMIN(0) = 0. DRLXCC(630) = 7.913566E-04
TSTEPU = 0. EBALNC(105) =-1.607585E-04 CSGMAX(0) = 0. ARLXCC(173) = 2.456809E-04
ITERCT = 65 DMXTCC(0) = 0. AMXTCC(0) = 0.

DIFFUSION NODES

T	1=	183.062	T	2=	127.879	T	3=	118.980	T	4=	143.294	T	5=	143.294	T	6=	143.294
T	10=	270.671	T	11=	285.153	T	12=	150.483	T	13=	179.852	T	14=	223.098	T	15=	179.214
T	20=	283.111	T	21=	297.593	T	22=	161.305	T	23=	192.095	T	24=	235.538	T	25=	179.214
T	30=	277.638	T	31=	292.119	T	32=	156.147	T	33=	186.251	T	34=	230.066	T	35=	179.214
T	55=	175.480	T	610=	306.674	T	611=	328.319	T	614=	244.699	T	620=	319.113	T	621=	340.759
T	624=	257.139	T	630=	313.640	T	631=	335.286	T	634=	251.667	T	655=	193.481	T	105=	114.382
T	121=	94.9513	T	122=	120.077	T	123=	140.973	T	124=	185.895	T	125=	147.666	T	126=	173.455
T	127=	153.785	T	128=	180.424	T	129=	116.390	T	130=	114.877	T	131=	109.161	T	132=	96.6295
T	133=	108.114	T	151=	162.552	T	152=	128.222	T	153=	154.350	T	154=	157.195	T	155=	141.035
T	111=	207.585	T	112=	220.025	T	113=	214.553	T	700=	207.173	T					

ARITHMETIC NODES

T	170=	78.5539	T	171=	112.081	T	172=	131.636	T	173=	162.317	T	174=	165.657	T	175=	146.681
T	176=	71.2300	T	177=	84.9471	T	178=	87.3073	T	501=	127.966	T					

HEATER NODES

++NONE++

BOUNDARY NODES

T	1000=	50.0000	T	1001=	10.0000E+01	T	2000=	154.622	T	2001=	110.189	T					

TIMEN = 0. EBALSC =-2.419979E-04 CSGMIN(0) = 0. DRLXCC(630) = 7.913566E-04
TSTEPU = 0. EBALNC(105) =-1.607585E-04 CSGMAX(0) = 0. ARLXCC(173) = 2.456809E-04
ITERCT = 65 DMXTCC(0) = 0. AMXTCC(0) = 0.

DIFFUSION NODES

T	1=	83.9231	T	2=	53.2663	T	3=	48.3224	T	4=	61.8299	T	5=	61.8299	T	6=	61.8299
T	10=	132.595	T	11=	140.640	T	12=	65.8236	T	13=	82.1402	T	14=	106.165	T	15=	81.7855
T	20=	139.506	T	21=	147.551	T	22=	71.8358	T	23=	88.9414	T	24=	113.077	T	25=	81.7855
T	30=	136.466	T	31=	144.511	T	32=	68.9703	T	33=	85.6950	T	34=	110.037	T	35=	81.7855
T	55=	79.7113	T	610=	152.596	T	611=	164.622	T	614=	118.166	T	620=	159.507	T	621=	171.533
T	624=	125.077	T	630=	156.467	T	631=	168.492	T	634=	122.037	T	655=	89.7119	T	105=	45.7678
T	121=	34.9730	T	122=	48.9318	T	123=	60.5406	T	124=	85.4972	T	125=	64.2587	T	126=	78.5862
T	127=	67.6584	T	128=	82.4577	T	129=	46.8831	T	130=	46.0428	T	131=	42.8671	T	132=	35.9053
T	133=	42.2858	T	151=	72.5290	T	152=	53.4589	T	153=	67.9724	T	154=	69.5526	T	155=	60.5751
T	111=	97.5471	T	112=	104.458	T	113=	101.418	T	700=	97.3185	T					

ARITHMETIC NODES

T	170=	25.8633	T	171=	44.4893	T	172=	55.3532	T	173=	72.3984	T	174=	74.2539	T	175=	63.7118
T	176=	21.7945	T	177=	29.4151	T	178=	30.7203	T	501=	53.3144	T					

HEATER NODES

++NONE++

BOUNDARY NODES

T	1000=	1.00000E+01	T	1001=	37.7778	T	2000=	68.1235	T	2001=	43.4382	T					

++NOTE++ EBALSA(1.000000E-03) HAS BEEN MET ON ITERATION 112.

TIMEN = 0. EBALSC =-7.762631E-04 CSGMIN(0) = 0. DRLXCC(35) =-1.010889E-04
TSTEPU = 0. EBALNC(124) =-1.977904E-04 CSGMAX(0) = 0. ARLXCC(501) = 9.211003E-05
ITERCT = 112 DMXTCC(0) = 0. AMXTCC(0) = 0.

DIFFUSION NODES

T	1=	183.063	T	2=	127.881	T	3=	118.982	T	4=	143.296	T	5=	143.296	T	6=	143.296
T	10=	270.675	T	11=	285.156	T	12=	150.485	T	13=	179.855	T	14=	223.102	T	15=	179.215
T	20=	283.115	T	21=	297.596	T	22=	161.307	T	23=	192.097	T	24=	235.542	T	25=	179.215
T	30=	277.645	T	31=	292.126	T	32=	156.149	T	33=	186.254	T	34=	230.071	T	35=	179.215
T	55=	175.482	T	610=	306.677	T	611=	328.323	T	614=	244.703	T	620=	319.117	T	621=	340.762
T	624=	257.143	T	630=	313.647	T	631=	335.292	T	634=	251.673	T	655=	193.483	T	105=	114.384
T	121=	94.9528	T	122=	120.079	T	123=	140.976	T	124=	185.898	T	125=	147.668	T	126=	173.458
T	127=	153.788	T	128=	180.428	T	129=	116.391	T	130=	114.879	T	131=	109.162	T	132=	96.6308
T	133=	108.116	T	151=	162.554	T	152=	128.225	T	153=	154.353	T	154=	157.198	T	155=	141.038
T	111=	207.588	T	112=	220.028	T	113=	214.558	T	700=	207.175	T					

ARITHMETIC NODES

T	170=	78.5547	T	171=	112.082	T	172=	131.058	T	173=	162.320	T	174=	165.660	T	175=	146.684
T	176=	71.2306	T	177=	84.9481	T	178=	87.3084	T	501=	127.968	T					

HEATER NODES

++NONE++

BOUNDARY NODES

T	1000=	50.0000	T	1001=	10.0000E+01	T	2000=	154.625	T	2001=	110.190	T					

TIMEN = 0. EBALSC =-7.762631E-04 CSGMIN(0) = 0. DRLXCC(35) =-1.010889E-04
TSTEPU = 0. EBALNC(124) =-1.977904E-04 CSGMAX(0) = 0. ARLXCC(501) = 9.211003E-05
ITERCT = 112 DMXTCC(0) = 0. AMXTCC(0) = 0.

DIFFUSION NODES

T	1=	93.9241	T	2=	53.2673	T	3=	48.3235	T	4=	61.8309	T	5=	61.8309	T	6=	61.8309
T	10=	132.597	T	11=	140.642	T	12=	65.8251	T	13=	82.1417	T	14=	106.168	T	15=	81.7864
T	20=	139.508	T	21=	147.553	T	22=	71.8374	T	23=	88.9430	T	24=	113.079	T	25=	81.7864
T	30=	136.469	T	31=	144.514	T	32=	68.9719	T	33=	85.6967	T	34=	110.040	T	35=	81.7864
T	55=	79.7121	T	610=	152.593	T	611=	164.624	T	614=	118.168	T	620=	159.509	T	621=	171.535
T	624=	125.079	T	630=	156.470	T	631=	168.496	T	634=	122.040	T	655=	89.7127	T	105=	45.7689
T	121=	34.9738	T	122=	48.9830	T	123=	68.5421	T	124=	85.4989	T	125=	64.2603	T	126=	78.5879
T	127=	67.6600	T	128=	82.4599	T	129=	46.8840	T	130=	46.0437	T	131=	42.8680	T	132=	35.9060
T	133=	42.2867	T	151=	72.5298	T	152=	53.4583	T	153=	67.9740	T	154=	69.5543	T	155=	60.5766
T	111=	97.5490	T	112=	104.460	T	113=	101.421	T	700=	97.3192	T					

ARITHMETIC NODES

T	170=	25.8637	T	171=	44.4903	T	172=	55.3546	T	173=	72.4000	T	174=	74.2557	T	175=	63.7134
T	176=	21.7948	T	177=	29.4156	T	178=	30.7269	T	501=	53.3155	T					

HEATER NODES

++NONE++

BOUNDARY NODES

T	1000=	1.00000E+01	T	1001=	37.7773	T	2000=	68.1247	T	2001=	43.4391	T					

++NOTE++ EBALNA(1.000000E-03) HAS BEEN MET ON ITERATION 113.

TIMEN = 0. EBALSC =-7.595126E-04 CSGMIN(0) = 0. DRLXCC(35) = 7.168456E-05
TSTEPU = 0. EBALNC(10) =-1.241170E-04 CSGMAX(0) = 0. ARLXCC(501) = 9.860152E-06
ITERCT = 113 DMXTCC(0) = 0. AMXTCC(0) = 0.

DIFFUSION NODES

T 1=	183.063	T 2=	127.681	T 3=	118.982	T 4=	143.296	T 5=	143.296	T 6=	143.296
T 10=	270.675	T 11=	285.156	T 12=	150.485	T 13=	179.855	T 14=	223.102	T 15=	179.216
T 20=	283.115	T 21=	297.596	T 22=	161.307	T 23=	192.097	T 24=	235.542	T 25=	179.216
T 30=	277.645	T 31=	292.126	T 32=	156.149	T 33=	186.254	T 34=	230.071	T 35=	179.216
T 55=	175.482	T 610=	306.677	T 611=	328.323	T 614=	244.703	T 620=	319.117	T 621=	340.762
T 624=	257.143	T 630=	313.647	T 631=	335.292	T 634=	251.673	T 655=	193.483	T 105=	114.384
T 121=	94.9528	T 122=	120.079	T 123=	140.976	T 124=	165.898	T 125=	147.668	T 126=	173.458
T 127=	153.768	T 128=	180.428	T 129=	116.391	T 130=	114.879	T 131=	109.162	T 132=	96.6308
T 133=	108.116	T 151=	162.554	T 152=	128.225	T 153=	154.353	T 154=	157.198	T 155=	141.038
T 111=	207.588	T 112=	220.028	T 113=	214.558	T 700=	207.175	T			

ARITHMETIC NODES

T 170=	78.5547	T 171=	112.082	T 172=	131.638	T 173=	162.320	T 174=	165.660	T 175=	146.684
T 176=	71.2306	T 177=	84.9481	T 178=	87.3084	T 501=	127.968	T			

HEATER NODES

++NONE++

BOUNDARY NODES

T 1000=	50.0000	T 1001=	10.0000E+01	T 2000=	154.625	T 2001=	110.190	T			

TIMEN = 0. EBALSC =-7.595126E-04 CSGMIN(0) = 0. DRLXCC(35) = 7.168456E-05
TSTEPU = 0. EBALNC(10) =-1.241170E-04 CSGMAX(0) = 0. ARLXCC(501) = 9.860152E-06
ITERCT = 113 DMXTCC(0) = 0. AMXTCC(0) = 0.

DIFFUSION NODES

T 1=	83.9241	T 2=	53.2673	T 3=	48.3235	T 4=	61.8309	T 5=	61.8309	T 6=	61.8309
T 10=	132.597	T 11=	140.642	T 12=	65.8251	T 13=	82.1417	T 14=	106.168	T 15=	81.7864
T 20=	139.508	T 21=	147.553	T 22=	71.8374	T 23=	88.9430	T 24=	113.079	T 25=	81.7864
T 30=	136.469	T 31=	144.514	T 32=	68.9719	T 33=	85.6967	T 34=	110.040	T 35=	81.7864
T 55=	79.7121	T 610=	152.598	T 611=	164.624	T 614=	118.168	T 620=	159.509	T 621=	171.535
T 624=	125.079	T 630=	156.470	T 631=	168.496	T 634=	122.040	T 655=	89.7126	T 105=	45.7689
T 121=	34.9738	T 122=	48.9330	T 123=	60.5421	T 124=	85.4989	T 125=	64.2603	T 126=	78.5879
T 127=	67.6600	T 128=	82.4599	T 129=	46.8840	T 130=	46.0437	T 131=	42.8686	T 132=	35.9060
T 133=	42.2867	T 151=	72.5298	T 152=	53.4583	T 153=	67.9740	T 154=	69.5543	T 155=	60.5766
T 111=	97.5490	T 112=	104.460	T 113=	101.421	T 700=	97.3192	T			

ARITHMETIC NODES

T 170=	25.8637	T 171=	44.4903	T 172=	55.3546	T 173=	72.4000	T 174=	74.2557	T 175=	63.7134
T 176=	21.7948	T 177=	29.4156	T 178=	30.7209	T 501=	53.3155	T			

HEATER NODES

++NONE++

BOUNDARY NODES

T 1000=	1.00000E+01	T 1001=	37.7778	T 2000=	68.1248	T 2001=	43.4391	T			

++NOTE++ END OF EXECUTIONER PHASE.