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DEVELOPMENT OF LOW COST CONTACTS TO SILICON SOLAR CELLS

FIRST QUARTERLY REPORT

FOR PERIOD COVERING

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BY

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"The JPL Low-Cost Silicon Solar Array Project is sponsored by the U. S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effect toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE."

ABSTRACT

This reporting period has involved an empirical scan through several possible schemes for applying copper contacts to solar cells by plating methods.

Commercial electroless Cu solutions have been used. Satisfactory adhesion (and fairly good cell performance) has resulted from use of thin layers of barrier metals such as Au, Cr or Pd. In these tests, photoresist masks were used to contact silicon P-type slices with diffused N+ and alloyed P+ surfaces; an electrolytic Cu solution was used to build up the contact thickness to provide good cell behavior.

In addition some cells with evaporated Cr-Cu contacts were also made (along with evaporated Ti-Pd-Ag contacts as controls), with the intention of subjecting cells to gradually increasing heat-treatments, to determine whether Cu causes the cells to be inherently unstable.

The work to date has provided several possible plating contacting sequences with fair I-V curves, and adhesion. With this technology in hand, present effort is aimed at detailed measurement of contact resistance, adhesion, solderability and other factors considered essential for good cell usage.

In addition, tests will settle the issue of whether the rapid migration of Cu in the silicon can lead to appreciable cell degradation. Work will continue to reduce overall costs as far as possible.

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INTRODUCTION

The contract involves evaluation of the technical feasibility and effective cost of a copper plating system for the manufacture of solar cells for high volume production of low cost solar array (LSA) modules. The LSA goal is to provide low cost silicon solar cells formed into operational arrays. At present, the cost breakdown shows that about 1/3 of the array cost is in materials (silicon and metals), slightly more than 1/3 for processing into cells, and the remainder for array formation. Much of the LSA effort (Tasks 1, 2) is aimed at reduced silicon cost; other effort in Task 4 is aimed at process cost reduction and at automated processing. Other efforts are directed towards cell interconnection and encapsulation. Already the projected silicon costs show promise of reaching the near-term LSA goals, although as the minimum array efficiency goals are increased, more attention is being paid to the adequacy of lower cost silicon for use in high efficiency arrays. In most cases, it appears that the silicon cost goals may be achieved. Also many of the individual cell process steps appear to be capable of cost reduction to fit the goals.

The major process costs are those involved with the metallization required to contact and interconnect the cells. The costs of metals is rising, and with present understanding it appears that at least 1.6×10^{-4} cm^3 of good conductivity metal will be needed for each cm^2 of cell area; this is an irreducible cost factor. It is, however, important to provide this minimum amount of metal with as little waste (or even reclaimable) metal as possible. It is for this reason that

careful analysis is proceeding on vacuum evaporation systems (where over 90% waste metal is used in depositing fine metal pattern), or of silk screened systems, where equivalent excesses are involved, although with greater ease of re-use.

Of all present methods, plating is most attractive in reduced metal usage; with resist patterns applied to the cell surface to leave the required areas available for metallization, it is possible by plating to deposit metal only where required. Thus metal usage can be kept to the minimum, and in addition the fact that a high vacuum is not required makes plated contacts most promising for reduced costs.

There are other aspects of contacts which must be considered. To date, most of the field failures have been attributed to the cell contacts, either because of reduced cell efficiency showing thermal cycling, or after corrosion caused by exposure to the atmosphere. The latter problem can be reduced by improved encapsulation methods.

With the above background, it is clear why plated systems merit study in the present program, and also the required precautionary and proving-out tests can be defined.

BACKGROUND

Historically, silicon solar cells were made first with plated contacts. The system used was deposition of nickel by electroless methods, followed by solder build up to provide adequate conductance, and to provide an interconnectable contact area. Later, space-use cells modified this system (in improving adhesion, and also in providing an improved ohmic contact) by adding a thin ($\sim$500 Å) layer of gold, also deposited by electroless methods.

As the space-cell requirements were made more demanding (minimum pull-strength increased above 450 gm per 0.02 cm^2 areas, need to contact highly polished surfaces, and very shallow junctions, and adaptability to welding), the contact structure was changed to an evaporated stack of titanium-silver. Later to increase moisture resistance, a thin layer of palladium was added between the Ti and Ag. This contact system has proved to be a satisfactory space-use contact for most missions, and has been adapted to masking methods capable of providing the closely spaced, narrow grid pattern now being used for space or concentrator-use cells. In some cases some of the silver has been deposited by evaporation, and the required thickness is obtained by electroplating. Many of the current terrestrial cells use this space contact system, mainly because of the already existing technology. Several other contact systems (all-Al, all-Ag, Ce-Ag, Cr-Au-Ag, Cr-Pd-Ag, Ta-Pd-Ag) have been tested but have not been used for reasonably large numbers of cells.

In addition, work has proceeded on various forms of metal pastes or inks, deposited mainly through silk screen masks. In a few cases, the paste

has been dispersed in photoresistive matrices and can be patterned by photoexposure methods. These methods are still under intensive study.

The modified Au-Ni-solder system has also been used again for terrestrial panels.

Developmental work (at Motorola[1]) has also led to a Pd-Ni-solder system.

This was the context into which the present program fitted. A method was needed, which could retain the advantages of a plated system (effective metal usage, relatively inexpensive equipment) while including other favorable aspects, such as easy control and repeatability, compatibility with inexpensive masking systems. The contacts had to have required properties to form an efficient cell, including low contact resistance, good conductance, good adhesion, good corrosion resistance and good thermal cycling properties.

We will examine these requirements in more detail.

(a) Metal Choice

There are relatively few metals of sufficient conductance (for reasonable thicknesses); these are silver, copper, aluminum, gold. If greater thicknesses are tolerable, other elements like Mg, Ni, Rh, Mo, W, or Cr, Pd, Nb, Ta have fair conductance, but are mostly ruled out because of difficulty of application or other properties. Also some combinations (such as Sn-Pb solders) can be used in relatively large thicknesses.

Of the four major conductors for the cost goals required, gold and silver were ruled-out because of cost, and aluminum also, because of the difficulty in plating methods (mostly only non-aqueous solutions have been successful) and also because of present reluctance to develop simple interconnect methods.

This left copper as a candidate metal, and for this reason, this program was initiated to explore the promise and problems resulting from choice of copper as the major metal constituent in cell contacts. Certainly the conductance of copper is most competitive. Copper can be of reasonably low cost, and an extensive technology exists for plating copper both by electroless and by electroplating methods.

(b) Contact Resistance

The contact resistance between silicon and metal (such as copper) is determined by two factors: the doping level of the silicon surface, and the detailed band properties of the metal, determining the Fermi level position, and the resultant contact potential. For silicon, however, the surface states can make the latter metal properties less predictable in determining the contact resistance, and in practice it is usual to resort to empirical determination of the actual contact potential resulting from a given silicon surface condition, and method of deposition of the metal.

It is customary to assume that the silicon slices requiring contacts will probably have N+ and P+ surfaces both fairly highly doped, and already formed before contact application. We have used such slices in our program.

If empirical tests show that for given silicon surface conditions, a metal does have too high a contact resistance, often a satisfactory reduction in this resistance can be provided by use of a thin interfacial layer of another metal, deposited directly on the silicon before applying the main contact metal. The Au used in the electroless Ni system served such a purpose.

Below we will discuss tests of several different metals as underlayers for copper; included in these thin metal layers are Au, Pd, Cr and Ni.

(c) Contact Adhesion

No matter how attractive the conducting properties of any metal contact system, it is essential that the contacts have good adhesion to the silicon. This is necessary, to ensure ease of handling into an array, and stability in operation.

The contact adhesion is determined by two factors, the surface finish, and the metal bonding mechanism at the surface. In general, rougher surfaces promote better adhesion for plated systems; thus use of a textured silicon surface (a competitive low cost method for processing silicon slices) has been assumed, although early tests have used fairly well polished surfaces. The bonding strength between silicon and metals is enhanced by use of a very clean silicon surface (and metals) and in some cases by relatively mild heat treatments (sintering) to consolidate the bonded interface. In some cases, the bonding is improved by use of a thin interfacial layer of the same type required to reduce contact resistance, and this approach has been used here in early studies of plating onto polished surfaces.

(d) Stability in Operation

There are three main possible causes of cell deterioration in practice. These are the chances of failure under thermal cycling, a mechanism minimized by choice of metals matched to the silicon, by providing high contact adhesion, or by restriction to thin metal layers. There is also the chance of corrosion, and this must be checked experimentally for the particular combination of cell contacts and interconnect metals.

Finally there is the chance of cell degradation because some of the metal contact components can migrate to regions in the cell where they can reduce cell efficiency. It is this latter possibility which has often been invoked for copper, because of its well known high diffusivity (diffusion rate), so that even at relatively low temperatures, copper atoms can move fairly long distances in the silicon. On the other hand, large quantities of copper have been introduced into bulk silicon without much loss of cell output.[2] Thus again, empirical experimentation is needed to choose between these possibilities. In practice a set of carefully performed tests, using gradually increased temperature-time schedules, can identify the probability of such degradation by monitoring the cell efficiency resulting from this series of heat treatments.

There is an additional factor which can alter this possible mode of degradation. This factor involves the use of another thin interfacial layer of another metal, and above we have seen that such a layer may be needed to reduce contact resistance and to improve contact adhesion. The use of such a "barrier" metal could retard or prevent the motion of copper into silicon.

With this background, the approach to be used in the program can be better understood.

MAIN APPROACH

Use of Commercial Solutions

The program is based on the commercial availability of electroless solutions for depositing copper. The electroless methods involve the use of various pretreatments (sensitizing) which involve the deposition of very thin metal layers, possibly palladium and/or tin. A commercial sequence of solutions was tested first. The resultant adhesion of copper layers was poor. No success resulted from omission of the pretreatments by attempting direct plating of copper onto the silicon.

Use of Alternate Pre-treatments

In attempts to improve the sequence, alternate pre-treatments were used. The first alternate system, a gold electroless deposition, gave fair adhesion of copper, and although the costs of even this modestly thin gold layer ($\sim$500 Å) were estimated to be high ($\sim 8^{c}$/Watt). Some cells were made to demonstrate the feasibility of gold as an interface layer.

Because of the success of chromium as an evaporated barrier layer, the existence of a few electroless baths for chromium deposition, and the promising compatibility of Cr-Cu combined, some samples were also made using Cr as the barrier layer.

Because of the success of Pd as a barrier metal in the Motorola work, some tests were performed with the Pd-Cu system. In addition a few tests introduced very thin layers of electroless Ni, mainly used as a sensitizing solution.

Although the system was more complex (because of the greater number of steps) some tests used a blend of pre-treatments, such as a very thin (50 Å) layer of Pd (the Motorola immersion bath), with later use of Cr-Cu electroless baths.

Contact Buildup

In most cases, the electroless systems have relatively slow deposition rates (∿.1 μ/min.), and attempts to increase this rate often weakened the adhesion. Thus it may be cost-effective to build up the contact (and thereby the conductivity and contactibility) by other means. The major effort here has been by electroplating of copper, and this has proved to be fairly successful. A possible problem will be the chance of corrosion of this copper layer on exposure to the ambient atmosphere, but this corrosion can be identified if present, and possibly retarded by a thin over-plate.

Another possible method of build up is the use of solder layers, and this approach will be included in tests later in this program.

Masking During Plating

To provide grid contact patterns, masking resists are required during plating. These resists must allow adequate resolution, and must not decompose in the plating baths (and any necessary sensitizing treatments). Initially, photoresist masks have proved to be effective, and long term, there is the chance that such methods can be scaled-up, and mechanized to reduce costs. Also planned is the use of screened-on resists, which have low cost promise.

Simultaneous Plating on P+ and N+ Surfaces

If possible, it is preferable to apply contacts to both sides of the cell at the same time. Early tests have achieved this without much trouble.

Philosophy of Program

The program was set-up as a "probe-type" test of several desirable features:

(a) The existence of satisfactory electroless Cu systems.

(b) Need for minimal existing pre-treatments, which give good cell performance.

(c) Use of available resists, with tests of low cost methods.

(d) Build up using existing Cu electroplating, or perhaps soldering.

(e) Availability of typical solar cell slices.

(f) Rapid test of probable achievable values of contact resistance, contact adhesion and corrosion resistance.

(g) Determination of possibility of degradation for migration of copper.

There was little attempt to understand the chemistry involved. The availability of commercial solutions suggested a pragmatic attempt to use these solutions, either as purchased, or with some variations, again adopted after sufficient tests to show their promise.

Description of Tests to Date

The substrates used were 7-14 ohm-cm, p-type CZ <100> silicon. They were diffused by a $POCl_3$ source to a depth of approximately .3-.4 microns yielding a sheet resistance of approximately 25 ohm/square. The cells also have a back surface field obtained by alloying aluminum paste.

Photoresist masks have been used most to obtain the selective plating on the front side. Later a photomask was used to etch a pattern in the 5000 Å silicon monoxide layer on the front. This SiO_2 layer was used as the main surface protection for the cells. Since the backs of the cells have alloyed Al, the back surface is quite rough. Presently the fronts are chemically polished, but we plan to test textured surfaces next.

Copper Only System

First experiments used the commercial Sn-Pd sensitizer-solution and electroless copper (Appendix B), but because poor contact adhesion was obtained, further experiments were not made.

Gold-Copper System

Next a gold plating solution was used to make the copper adhere (see Appendix A). After about 500 Å of Au was electrolessly plated, about 1000 Å of Cu was then also plated electrolessly and the sample was heat treated at 300°C in nitrogen for 5 minutes. Next the copper thickness was increased by an electrolytic copper bath (see Appendix D) to about 4-6 microns thick. All cells made were seriously shunted. The diffused layers used here were shallower than those quoted above, being $\sim$0.2 μm. A deeper diffusion was considered to be a solution to the problem.

A quick cost analysis showed that the 500 Å Au layer required would cost at least 8¢/watt alone, so further work on this system was delayed, although if time permits the system will be carried forward to show practical feasibility despite the adverse costs.

Chromium-Copper System

Chromium was considered next as a possible candidate for the first layer metal. It was promising because (A) There are existing electroless baths, (B) The metal resembles titanium in evaporated contacts, and (C) Evaporated chromium is quite dense and it was hoped that the plated chromium would be dense enough to shield the silicon from the copper if necessary. To test the Cr-Cu contact system on the standard material, tests were conducted on all-evaporated contacts with 1000 Å of Cr and then 5000 Å of Cu. The cells were then heat treated to 400°C for 5 minutes in hydrogen and were electrolytically plated with copper to about 4-6 microns thick. These cells had the 5000 Å SiO_2 on the surface so they directly compared to the cells used in the plating process. From the data on Table 1 and the I-V plot in Figures 1a and 1b it is shown that the cells have reasonably good contact resistance denoted by the high fill factor. Also on contact pull tests over approximately .02 cm^2 areas, the front contact withstood ∿300 gm and the backs ∿600 gm. Since these cells only have 4 microns of copper, it is thought a solder coat would increase the pull strengths even more. All the test samples removed a layer of silicon on the solder tabs.

Later the same cells were made with Ti-Pd-Ag contacts (see Table 2 and Figure 2).

TABLE 1

SOLAR CELL ELECTRICAL DATA

CELL DESCRIPTION: Evaporated Cr-Cu Plated Cu

TEST CONDITION: AMO

TEMPERATURE: 25°C DATE:

NO.	V_{OC}	I_{SC}	I_{SCB}	I_{SCR}	I_{Max}	V_{Max}	P_{Max}	CFF	η*	AREA
	mV	mA	mA	mA	mA	mV	mW	%	%	cm^2
1	600	138	52	86	125.5	.5	62.8	.76	11.6	3.99
2	605	134	49	84	120	.5	60	.74	11.1	3.99
3	602	132.4	--	--	119	.485	57.7	.72	10.8	3.97
4	602	132.1	--	--	118	.495	58.4	.73	10.9	3.97

*AM1 efficiencies will be ~13% higher.

Cells were evaporated Cr (1000 Å) - Cu (5000 Å) heat treated 500°C in hydrogen for 5 minutes and then plated in the copper solution.

FIGURE 1a

CHROMIUM-COPPER EVAPORATED CONTACTS

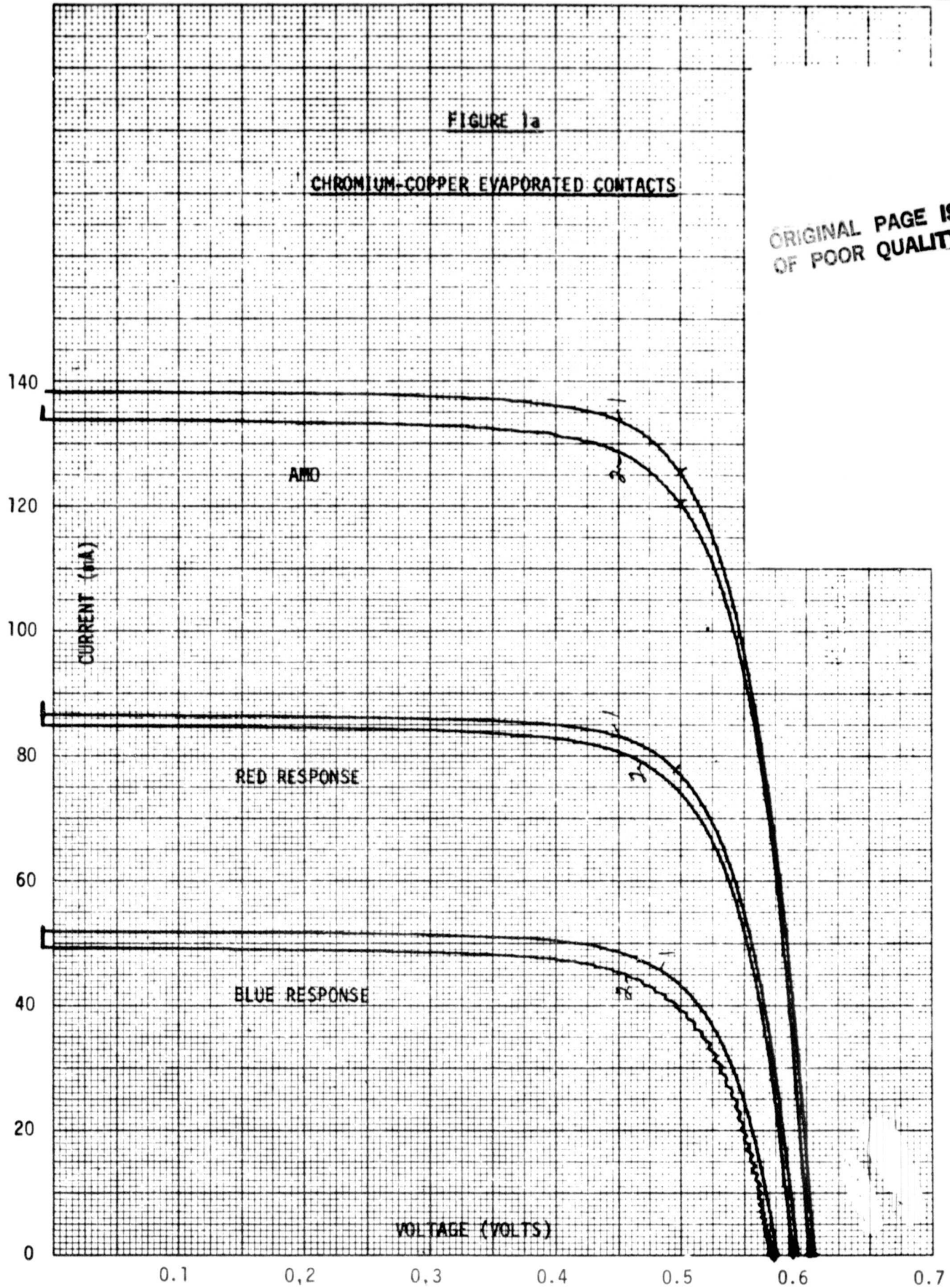


FIGURE 1b

CHROMIUM-COPPER EVAPORATED CONTACTS

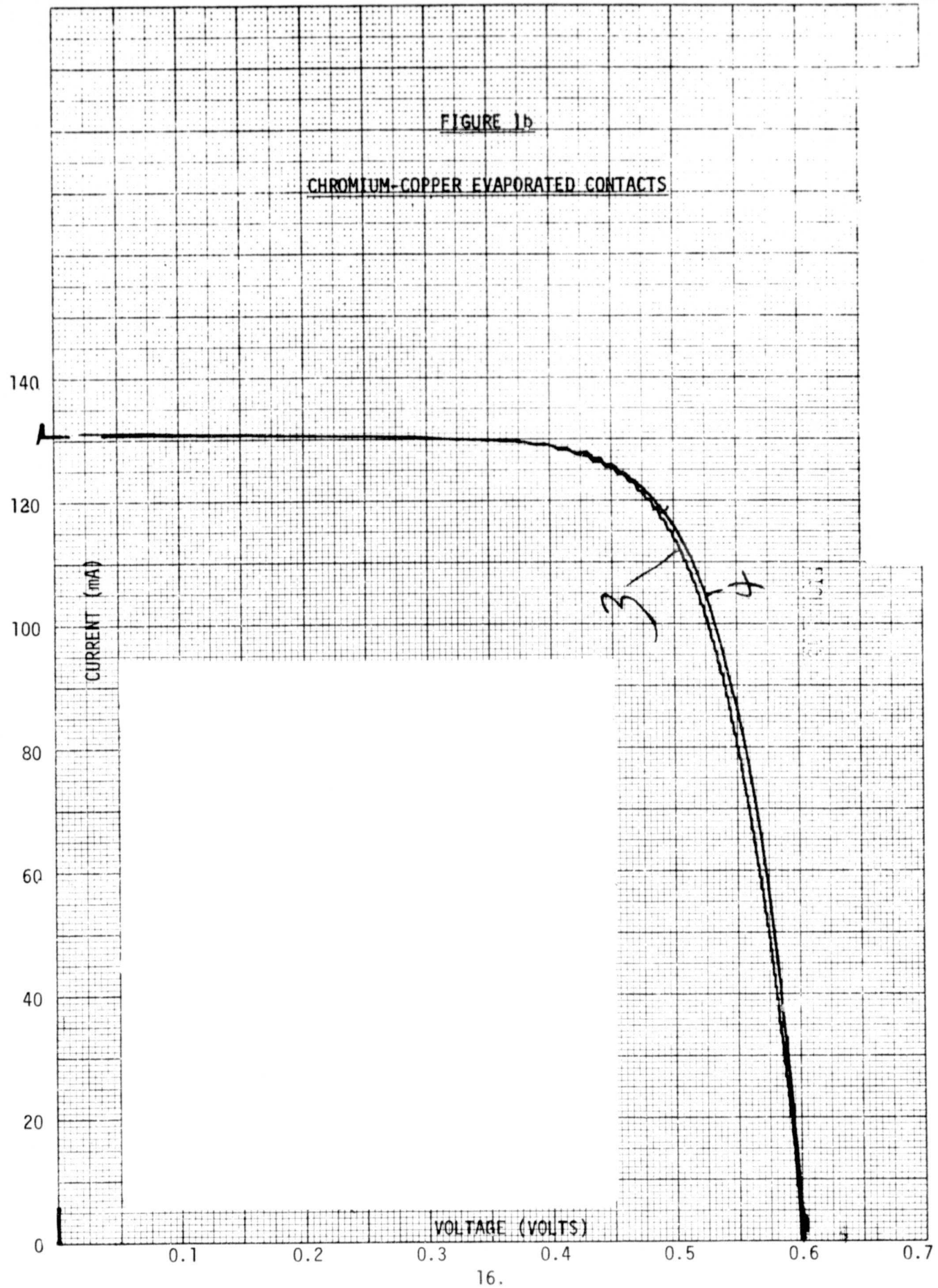


TABLE 2

SOLAR CELL ELECTRICAL DATA

CELL DESCRIPTION: Controls for Cu Plating Experiments

TEST CONDITION: AMO
TEMPERATURE: 25°C DATE:

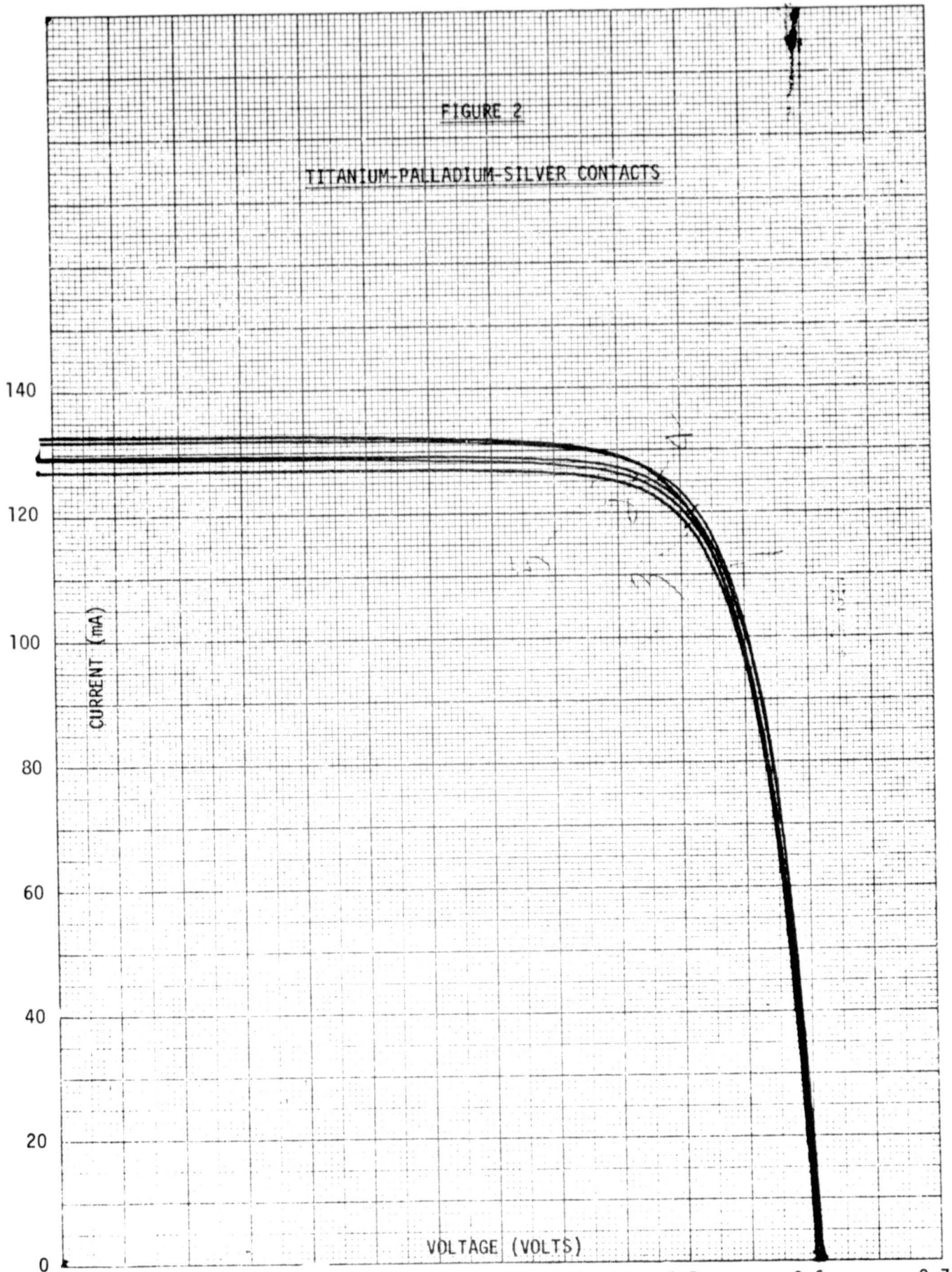
NO.	V_{OC}	I_{SC}	I_{SCB}	I_{SCR}	I_{Max}	V_{Max}	P_{Max}	CFF	η *	AREA
	mV	mA	mA	mA	mA	mV	mW	%	%	cm^2
1	607	134	51	84	121	512	61.95	.76	11.5	4
2	604	130	48	83	120	510	61.2	.78	11.3	4
3	601	129	48	81	118	505	59.59	.77	11.0	4
4	605	135	51	84	120	510	61.2	.75	11.3	4
5	601	131	48	83	119	505	60.1	.76	11.1	4

*AM1 efficiencies will be ∿13% higher.

Titanium-Palladium-Silver Contacts.

FIGURE 2

TITANIUM-PALLADIUM-SILVER CONTACTS



For the plated Cr-Cu system, early experiments with Cr fluoride based bath (Bath A) (Appendix C)[3] gave negative results. Next a chromium acetate based bath (Bath B)[4] was tried and gave only partial plating on the bare silicon surface. It was found that when the silicon surface was sensitized with the Pd-Sn commercial solution, Bath B deposited chromium uniformly at a rate of about 1000 Å in 3 minutes at 100°C. However, the layer did not always adhere. Some work was done on finding an immersion chromium bath to sensitize the silicon with chrome, but this work resulted in little success. The immersion Pd solution, (Appendix E)[5] developed by Motorola was then used with reasonably good results. The chromium plated at a slower rate but the Cr film was uniform and adherent.

The present Cr-Cu process is described in Appendix E. This process has worked in four successive tests although with a yield of only 50%, showing there is still much process development work required. Cell values are shown in Table 3 with I-V plots in Figure 3a and 3b. Cells made with this procedure have typically withstood ∿900 gms over a .02 cm^2 on the backs. The fronts appear to withstand only about 100 gm, failing with the plated chromium peeling. This problem may be solved by heat treating the samples at higher temperatures or by using nitrogen instead of hydrogen (tests in progress).

Palladium-Copper System

The process used for this system is given in Appendix G. The resulting data are on Table 4 and Figure 4. Methods used were generally those developed in the Motorola process.[5] In order, we used the immersion Pd bath, the electroless bath, and the commercial Cu bath.

TABLE 3

SOLAR CELL ELECTRICAL DATA

CELL DESCRIPTION: Cr-Cu Cells Plated

TEST CONDITION: AMO

TEMPERATURE: 25°C DATE:

NO.	V_{OC}	I_{SC}	I_{SCB}	I_{SCR}	I_{Max}	V_{Max}	P_{Max}	CFF	η†	AREA
	mV	mA	mA	mA	mA	mV	mW	%	%	cm^2
4	597	127.6	47	81	113	.5	56.5	.74	10.8	3.86
5*	575	111.3	--	--	96	.485	46.6	.73	8.9	3.9

*Cell made without CVD on surface.

†AM1 efficiencies ∿13% higher.

Immersion Pd - plated Cr - plated Cu heated 400°C plated Cu (electrolytic).

FIGURE 3a

CHROMIUM-COPPER PLATED CONTACTS

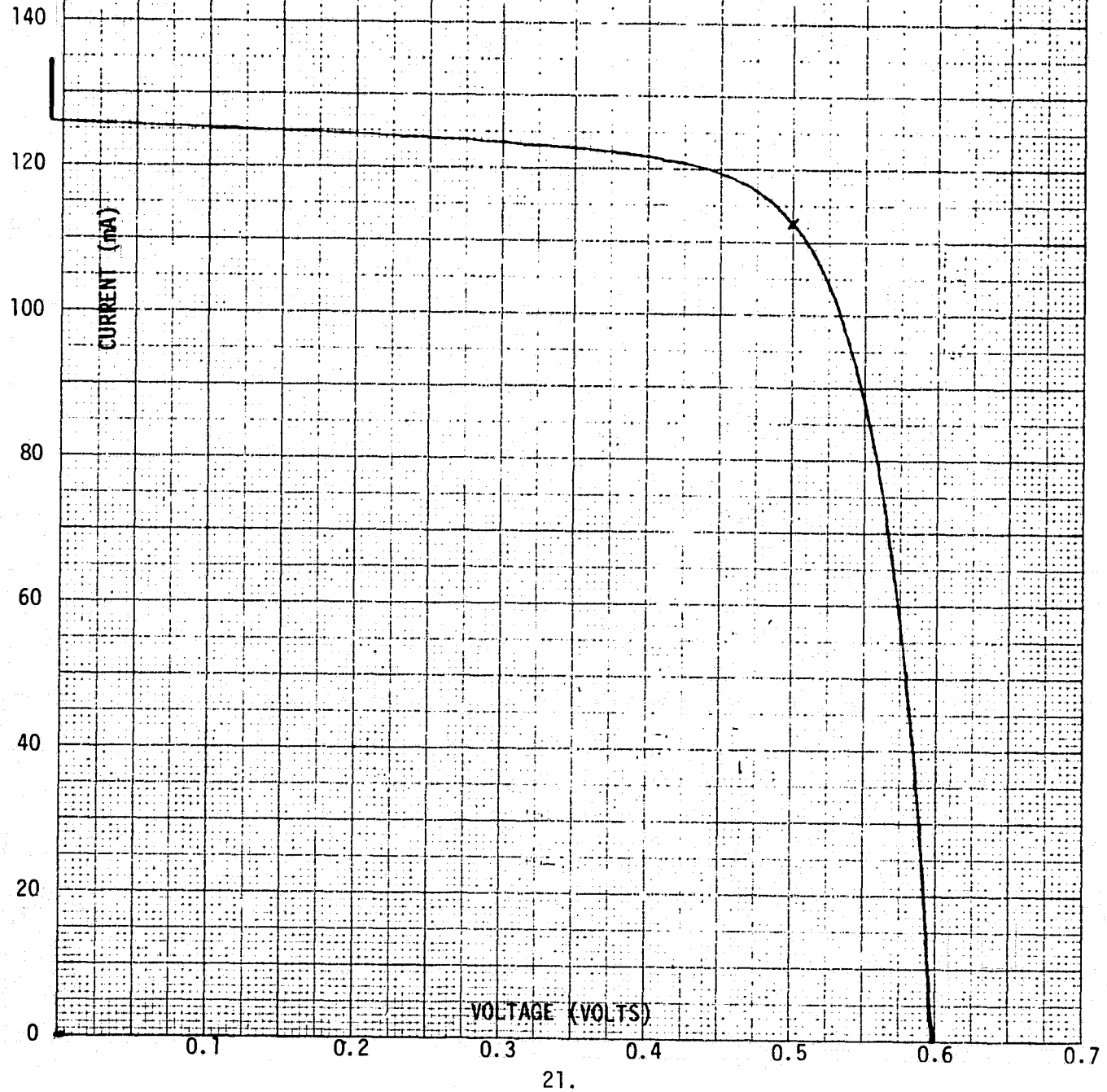


FIGURE 3b

CHROMIUM-COPPER PLATED CONTACTS

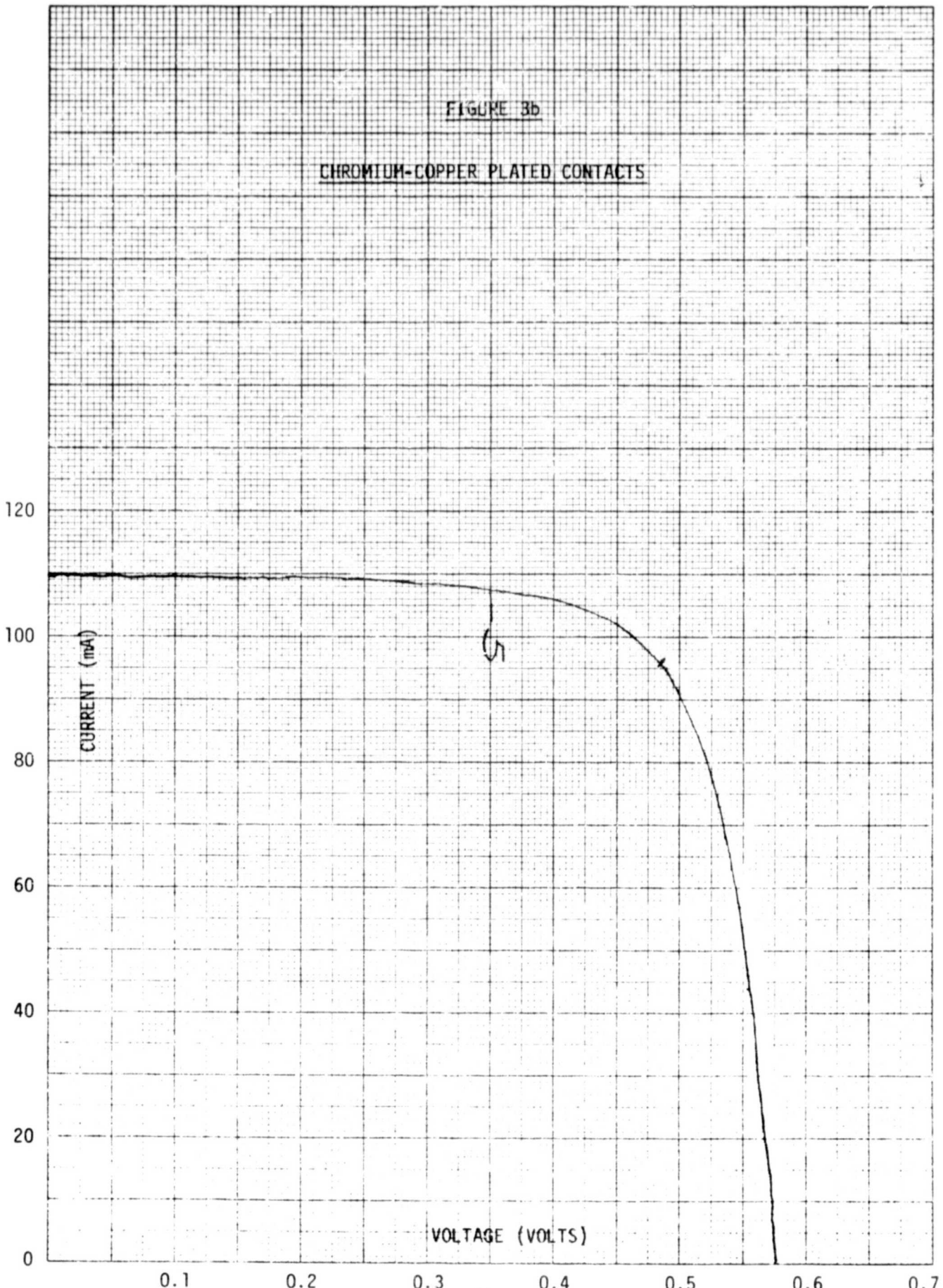


TABLE 4

SOLAR CELL ELECTRICAL DATA

CELL DESCRIPTION: Plated Pd and Plated Cu

TEST CONDITION: AMO

TEMPERATURE: 25°C DATE:

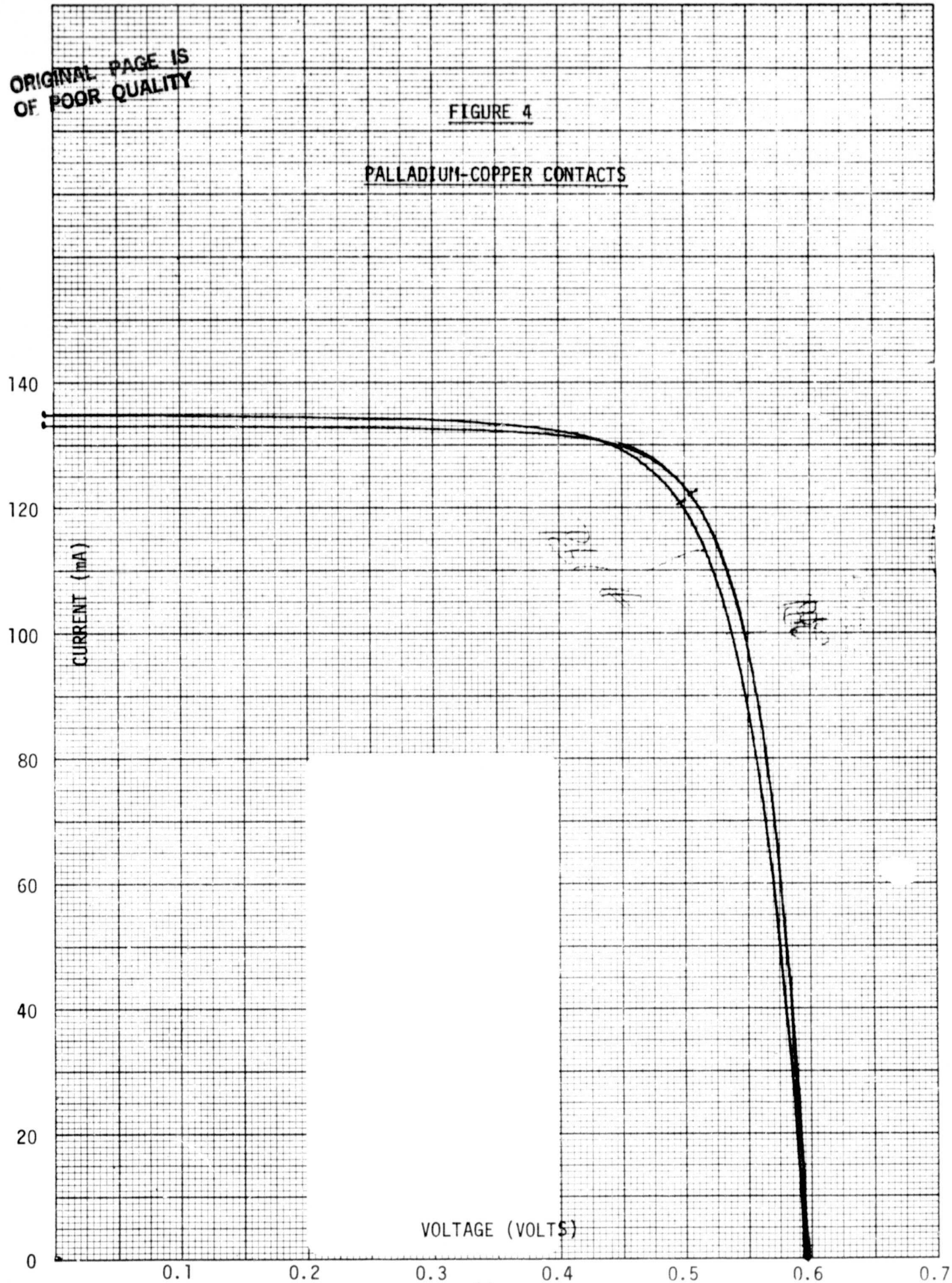
NO.	V_{OC} mV	I_{SC} mA	I_{SCB} mA	I_{SCR} mA	I_{Max} mA	V_{Max} mV	P_{Max} mW	CFF %	η* %	AREA cm^2
1	596	135	--	--	121	.495	60	.74	11.4	3.9
2	595	136	--	--	122	.505	61.6	.77	11.7	3.9

*AM1 efficiencies ~13% higher.

Immersion Pd - electroless Pd - heat treated 5 mm H_2 - electroless Cu - electrolytic Cu.

FIGURE 4

PALLADIUM-COPPER CONTACTS



Only a limited number of cells have been made, buth they appear to have good output; contact adhesion seems to be very good also. More cells will be made to test the feasibility of this contact system.

CONCLUSIONS

The empirical scanning period has resulted in several promising plating sequences. Already these contacts show promise in giving good cell behavior.

The work has progressed to the stage where quantitative results can be obtained on the parameters considered important for solar cell operation. In addition, tests are planned to evaluate the stability of contacts based on Cu plating.

WORK PLANNED

In the next period, we will obtain numerical results of adhesion, contact resistance and cell behavior and will begin to check stability factors. In addition, some tests of less expensive masking methods will be made, along with trials of different heat treatments, to obtain best balance between cell electrical and mechanical behavior, and to evaluate the long term stability of the cells.

NEW TECHNOLOGY

New processes have not been sufficiently developed to be reported as new technology. All new developments will be specified at completion of the contract.

REFERENCES

[1] "Metallization of Large Silicon Wafers", First Quarterly Report, JPL Contract No. 954689 (Motorola).

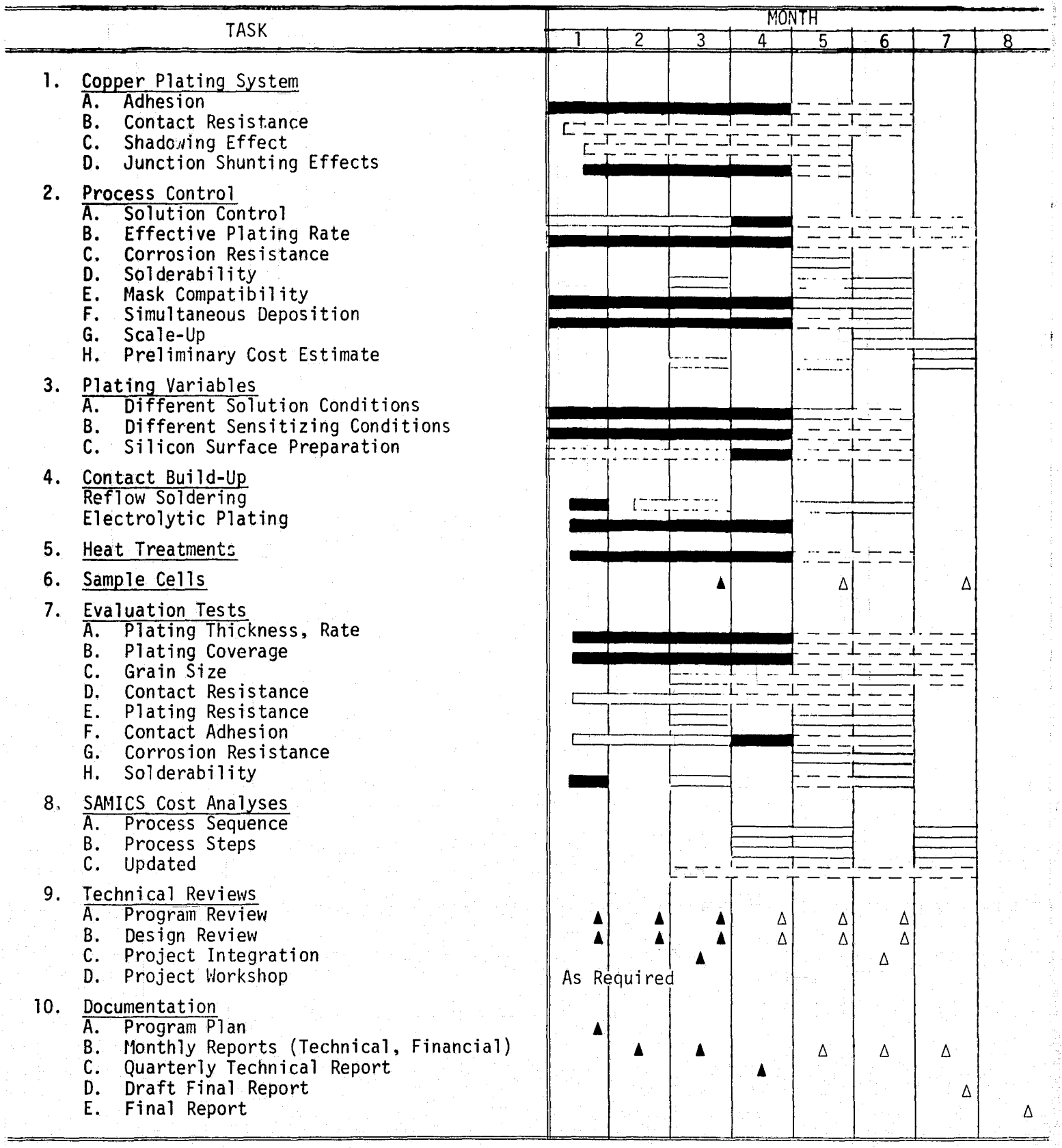
[2] "Effects of Impurities and Processing on Silicon Solar Cells", Tenth Quarterly Report, JPL Contract No. 954331 (Westinghouse).

[3] H. J. West, Metal Finishing, 53, No. 7, 62 (1955).

[4] H. J. West, Prod. Fin., 26, 58 (April, 1962).

[5] "Metallization of Large Silicon Wafers", Third Quarterly Report, JPL Contract No. 954689 (Motorola).

MILESTONE CHART



LEGEND ▭ Scheduled ▭ Continuing ▬ Completed

APPENDIX A

GOLD CYANIDE SOLUTION

200 ml	DI H_2O
2 gm	Gold Cyanide
10 ml	48% HF

Use at room temperature under a bright light for 2 minutes.

APPENDIX B

COMMERCIAL PLATING SYSTEM

A) Dynaplate Activator 120

B) Dynaplate Conditioner 101

C) Dynaplate 240 Electroless Copper

All solutions made by Thiokol/Dynachem Corporation.

APPENDIX C

ELECTROLESS CHROMIUM BATHS

Bath A

Chromium Fluoride	15	gm/l
Chromium Chloride	1	gm/l
Sodium Citrate	7.5	gm/l
Sodium Hypophosphite	7.5	gm/l

The operating temperature was 85°C to 95°C.

Bath B

DI H_2O	200	ml
Chromium Acetate	6	gm
Nickel Acetate	.4	gm
Sodium Citrate	8	gm
Sodium Glycolate	8	gm
Sodium Acetate	4	gm
Sodium Hypophosphite	4	gm

The operating temperature was 100°C.

Formulations taken from "Electroless Plating Today" by Dr. Edward B. Saubestre.

APPENDIX D

ELECTROLYTIC COPPER SOLUTION

1000 ml	DI H_2O
30 ml	H_2SO_4
200 gm	$CuSO_4$

Solution used at room temperature.

APPENDIX E

MOTOROLA'S PLATING SOLUTIONS

Immersion Pd Bath

300 ml	H_2O
.01 gm	PdCL
1 ml	HCL
20 ml	NH_4F

Mixed in a sonic bath and used at room temperature in the dark.

Electroless Pd Plating Bath

830 ml	DI H_2O
4 ml	HCL
2 gm	$PdCL_2$
27 gm	NH_4CL
6 gm	NAH_2PO_d $2H_2O$
160 ml	NH_4OH

APPENDIX F

CHROMIUM-COPPER PLATED CONTACT PROCEDURE

1) Standard 2x2cm substrates.

2) Photoresist and etch.

3) Immersion Pd bath (Appendix E)

   A) Five (5) seconds 10% HF

   B) Immersion Pd bath for 3 minutes in the dark

   C) Scrub cell with Q-tip, DI H_2O rinse

   D) Remove Photoresist with acetone

   E) Heat treat 15 minutes at 400°C in N_2

4) Electroless chromium bath (Appendix C)

   A) Five (5) seconds 10% HF

   B) DI H_2O rinse 5 seconds

   C) Immerse cells for 10 minutes, rinse DI H_2O

   D) Heat treat 5 minutes at 400°C in H_2

5) Immerse in Dynachem electroless copper solution for 5 minutes at 35°C.

6) Plate in electrolytic copper solution for 30 minutes at 30 ma for plating front and back simultaneously. Procedure plates 4-6 microns of dense copper.

APPENDIX G

PLATED PALLADIUM - PLATED COPPER PROCEDURES

1) Standard 2x2 cm substrates

2) Photoresist and etch

3) Immersion Pd bath (Appendix E)
   - A) Five (5) seconds 10% HF
   - B) Immersion Pd bath - 3 minutes
   - C) Scrub with Q-tip, DI H_2O rinse
   - D) Heat treat 400°C in N_2 - 15 minutes

4) Electroless Pd bath (Appendix E)
   - A) Five (5) seconds in 10% HF
   - B) Immerse in bath for 2 minutes at 40°C
   - C) Heat treat 400°C in N_2 - 5 minutes

5) Electroless Cu bath (Appendix B), for 2 minutes

6) Electrolytic Cu bath (Appendix D)
   - A) Thirty (30) minutes at 30 ma for 4-6 μm layer.