NASA CR-159,524

NASA-CR-159524

NASA-CR-159524

1979 0013102

DEVELOPMENT AND FABRICATION OF IMPROVED POWER TRANSISTOR SWITCHES

P. L. Hower
Westinghouse R&D Center
Pittsburgh, PA 15235

C. K. Chu
Westinghouse Semiconductor Division
Youngwood, PA 15697

LIBRARY COPY
MAY 5 1979
LANGLEY RESEARCH CENTER
LIBRARY, NASA
HAMPTON, VIRGINIA

Prepared for
National Aeronautics and Space Administration
NASA Lewis Research Center
Contract NAS3-18916

NASA CR-159524

DEVELOPMENT AND FABRICATION OF IMPROVED POWER TRANSISTOR SWITCHES

P. L. Hower
Westinghouse R&D Center
Pittsburgh, PA 15235

C. K. Chu
Westinghouse Semiconductor Division
Youngwood, PA 15697

N79-21273#

Prepared for
National Aeronautics and Space Administration
NASA Lewis Research Center
Contract NAS3-18916

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
CR-159524		

4. Title and Subtitle	5. Report Date
Development and Fabrication of Improved Power Transistor Switches	January 1979
	6. Performing Organization Code
7. Author(s)	8. Performing Organization Report No.
P. L. Hower; C. K. Chu	
	10. Work Unit No.
9. Performing Organization Name and Address	11. Contract or Grant No.
Westinghouse R&D Center 1310 Beulah Road Pittsburgh, PA 15235	NAS 3-18916
	13. Type of Report and Period Covered
12. Sponsoring Agency Name and Address	Contractor Report Final
National Aeronautics & Space Administration Lewis Research Center Cleveland, OH 44135	14. Sponsoring Agency Code

15. Supplementary Notes

Project Manager, Gale Sundberg, Space Propulsion and Power Division

NASA Lewis Research Center, Cleveland, Ohio

16. Abstract

A new class of high-voltage power transistors has been achieved by adapting present interdigitated thyristor processing techniques to the fabrication of npn Si transistors. Present devices are 2.3 cm in diameter and have V_{CEO} (sus) in the range of 400 to 600V. V_{CEO} (sus) = 450V devices have been made with an h_{FE} I_C product of 900A at V_{CE} = 2.5V. The electrical performance obtained is consistent with the predictions of an optimum design theory specifically developed for power switching transistors. The report describes the device design, wafer processing, and assembly techniques. Experimental measurements of the DC characteristics, forward SOA, and switching times are included. A new method of characterizing the switching performance of power transistors is proposed.

17. Key Words (Suggested by Author(s))	18. Distribution Statement
Power Transistors Switching Transistors Second Breakdown Transistor Modeling	Unclassified-Unlimited

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price*
Unclassified	Unclassified		

* For sale by the National Technical Information Service, Springfield, Virginia 22151

TABLE OF CONTENTS

Page

List of Figures ii

List of Tables v

1. Summary 1

2. Introduction 2

3. Device Design 5

   3.1 Background 5
   3.2 Design Examples 5
   3.3 Sensitivity to Changes in Device Variables 11
   3.4 Emitter-Base Geometry 11
   3.5 Forward Safe Operating Area 12
   3.6 Dynamic Considerations 18

      3.6.1 Turn-on 18
      3.6.2 Storage Time 20

   3.7 Other Considerations 24

4. Processing Investigation 25

   4.1 Packaging Considerations 25
   4.2 Impurity Profile 27
   4.3 Wafer and Fusion Processing 32

5. Electrical Performance 34

   5.1 Collector Characteristic 34
   5.2 Forward SOA 37
   5.3 Switching Performance- Resistive Load 40
   5.4 Switching Performance - Inductive Load 40

      5.4.1 Waveform Measurements 45
      5.4.2 Energy Loss Measurements 45

   5.5 Reverse SOA 52

6. Scale-Up Study 56

   6.1 33 mm Design 56
   6.2 Effect of Base Metallization 56

7. Conclusions 62

8. Acknowledgements 62

9. References 63

10. Appendices 64

LIST OF FIGURES

		Page
Fig. 1	Optimum design results for (a) V_{CEO} (sus) = 400V and (b) 600V. Collector current density is plotted perpendicular to the plane formed by peak current gain (h_{FEO}) and reach-through parameter m.	7,8
Fig. 2	General shape of the triple-diffused impurity profile.	9
Fig. 3	Sensitivity of V_{CEO} (sus) and h_{FE} (I_C = 50A, V_{CE} = 2.5V) to (a) collector doping, (b) collector width and (c) peak current gain.	13
Fig. 4	Effective area vs. collector current for the 659 mask design (A_{EM} = 1.6 cm^2, Z = 33 cm, I_{CR} = 142A).	16
Fig. 5	Collector current vs. collector emitter voltage corresponding to the onset of thermal instability with emitter ballast resistance as the parameter.	17
Fig. 6	Collector current rise time vs. collector current for different turn-on base currents.	19
Fig. 7	Collector-emitter voltage waveforms for different turn-on base currents.	21
Fig. 8	Storage time vs. collector current with base current as the parameter.	22
Fig. 9	Storage time vs. collector current with collector recombination lifetime as the parameter (I_{BF} = I_{BR}).	23
Fig. 10	Influence of lifetime on the current gain and storage time for the V_{CEO} (sus) = 450V design.	24
Fig. 11	Cross-sections showing conventional and CBE assembly techniques. The external package (not shown) provides the compressive force indicated by the arrows.	26
Fig. 12	Transistor fusion with emitter preform attached.	28
Fig. 13	Stud package used for encapsulating fusion of Fig. 12.	29

Fig. 14 Metallization pattern for 659 mask. The outer diameter is 1.67 cm. 30

Fig. 15 Impurity profile showing typical concentrations and dimensions. 31

Fig. 16 Processing flow sheet with device cross-sections, 33

Fig. 17 Measured collector characteristics for two devices with different sustaining voltage. 35

Fig. 18 Measured gain-current product vs. sustaining voltage for devices from three different runs. 38

Fig. 19 Second breakdown current vs. emitter ballast resistance. The measured currents are the largest values that pass the test for 0.5A increments. 39

Fig. 20 Forward SOA diagram for different pulse times. 41

Fig. 21(a) $i_C(t)$ and $v_{CE}(t)$ waveforms for transistor 18B53. Scales: i_C = 5A/d, v_{CE} = 20 V/d, t = 0.2 μs/d. I_{BF} = 6A, V_{CC} = 200V. 42

Fig. 21(b) Turn-off waveforms for transistor 18B53. Scales: i_C = 5A/d, i_B = 1 A/d, t = 1 μs/d. $I_{BF} = I_{BR}$ = 3A.

Fig. 22 Test circuit used for switching performance evaluation. 43

Fig. 23 Turn-off waveforms for transistor 22B-92. Scales: (a) i_C = 10 A/d, v_{CE} = 50 V/d, t = 0.1 μs/d. (b) i_C = 10 A/d, p = 2 KW/d, t = 0.1 μs/d. T_c = 23.5°C. 44

Fig. 24 Block diagram of switching-loss measurement. 46

Fig. 25 Example of waveforms for the turn-off interval, showing collector-current, collector-emitter voltage, instantaneous power, base current and integrator gating signal. 47

Fig. 26 Turn-on waveforms for device 25A-49. Scales: 48
(a) i_C = 20A/d, v_{CE} = 100 V/d, t = 0.1 μs/d,
(b) i_C = 20A/d, p = 2 KW/d, t = 0.1 μs/d.
L = 530 μH, $L_s \simeq 0$, V_{CC} = 300V, T_C = 30°C.

Fig. 27 Measured turn-on and turn-off losses. 49

Fig. 28 Total power lost in the transistor (P_L) and dissipated power (P_D) due to the thermal path through the device and heat sink vs. junction temperature. P_L is shown for two frequencies. 51

Fig. 29 Safe operating frequency vs. heat sink thermal resistance for different collector currents. 53

Fig. 30 Reverse SOA and test circuit. 54

Fig. 31 Base-emitter voltage (normalized to kT/q = 25.6 mV) and current density for the typical sector shown in Fig. 32. 58

Fig. 32 Metallization pattern showing base fingers and radial distance from base trunk centerline. 59

Fig. 33 Fractional reduction in emitter area vs. collector current due to base metallization sheet resistance for the pattern of Fig. 32. 60

LIST OF TABLES

Table		Page
1	Optimum Designs for h_{FE} = 10 at V_{CE} = 2.5V	10
2	Characteristics of Transistors of Fig. 17	36
3	Predicted Performance of a 33 MM Dia. Fusion	57
4	DC Characteristics	66
5	Switching Times	67
6	Test Data on Sample Devices	68
7	Test Data	73

1. SUMMARY

The overall objective of this program is the development of device design and processing techniques which permit the fabrication of npn transistors suitable for high-efficiency switching applications where the required BV_{CEO} voltage is in the range of 400 to 600V. An important aspect of the program has been the increase of the emitter area over that available in present commercial devices.

The transistors described in this final report are 23 mm in diameter and have an emitter area that is approximately eight times larger than that practical with a TO-3 package. This "scale-up" has been achieved without serious side-effects such as voids at the Si/header interface and non-uniformities in the emitter current distribution.

The electrical performance achieved is consistent with the predictions of the optimum design theory used for the transistor design. Specific sections of the report describe the device design, wafer processing techniques, and also various measurements which include DC characteristics, the forward safe operating area, and switching times. A new method is proposed for characterizing the switching performance of power transistors for operation in switching regulator circuits. The report ends with projected performance for a 33 mm diameter transistor.

2. INTRODUCTION

During the first half of the 1960's, the bipolar transistor was generally viewed as a device capable of switching only relatively low power levels. For most applications that needed a voltage blocking capability greater than about 200V and currents in excess of about 30A, the only semiconductor device available was a thyristor. These devices usually had a much larger conducting area than did the transistors of that era.

In the late 60's and early 70's, higher voltage transistors became available at a cost that made them attractive for off-line switching regulator applications. It is interesting to note that the market need which spurred the cost reduction of these devices was that of the automobile electronic ignition. The ignition application requires an open-base sustaining voltage V_{CEO} (sus) in the range of 300 to 500V, which turns out to be convenient for applications using rectified 110 and 220V AC line voltage. The packaging and assembly technology used for these transistors (TO-3) limited emitter areas to about 0.2 cm^2, with the result that output power levels were limited to a few hundred watts.

About that time, it became clear to a number of workers that some of the techniques used for making large-area thyristors (e.g. 2 to 3 cm in diameter) might also be used to increase the conducting area of bipolar transistors. A notable effort along these lines was the Westinghouse 1401.

This transistor had a metallurgical emitter area of 2.2 cm^2 and used a "single-diffused" impurity profile. That is, the base region is lightly-doped with respect to the collector. An inherent feature of this profile is that the current density that can be controlled for a given V_{CEO} (sus) is considerably less than that of a "triple-diffused"

or epitaxial collector profile, where the collector is lightly doped with respect to the base. Other disadvantages are the low value of V_{CEO} (sus) that is practical ($\stackrel{\sim}{<}$ 250V) and the long rise and fall times during switching, e.g., 1 to 2 μs.

In the meantime, circuit designers working with higher voltage TO-3's overcame one of the drawbacks of triple-diffused transistors, i.e. device failure during turn-off of inductive loads, by adding protective networks that by-pass the inductive energy around the transistor during turn-off. This improvement, coupled with the ability to control higher current densities and the ability to operate at higher switching frequencies, favors the triple-diffused type of profile over the single-diffused for most power electronic applications. There are some noteworthy exceptions to this rule, namely, applications where the transistor must dissipate a significant amount of power, e.g., low-frequency amplifiers and current limiting circuits.

As experience with high-voltage TO-3 size transistors increased, it became clear that there were applications e.g. motor control, induction heating, and inverters in the 5 to 20 KW range, where a larger area transistor would be useful. In these applications, the alternative approach of paralleling many smaller devices presents problems due to non-uniform current distribution during turn-off. Thus, a single large transistor was needed.

The obvious question is: can larger transistors be made and still be cost-competitive? We believe the answer to this question is "yes". For example, the techniques described in this report are routinely used to produce interdigitated thyristors up to 5 cm in diameter. While the steps necessary to adapt thyristor and rectifier processing techniques to transistors are not trivial, they pose no major technological hurdles. We are confident that many of the processing and design procedures worked out for the present 23 mm transistors will be applicable to even larger devices.

This final report describes our approach to the adaptation of these techniques. The first section of the report describes the basic device design, with subsequent sections dealing with processing, measurement of switching performance, and projections of performance for a larger 33 mm diameter transistor.

3. DEVICE DESIGN

3.1 Background

As is true in many situations, the design of a transistor requires a compromise. The desire to achieve a large blocking voltage conflicts with the need to control a large collector current at a given current gain h_{FE}. By using appropriate models for transistor behavior, it is possible to state this conflict quantitatively and at the same time develop an "optimized" design [1]. For example, if V_{CEO} (sus) and h_{FE} (at some V_{CE}) are given, then it is possible to determine an impurity profile that will maximize the collector current density, thereby giving a minimum area design (for a given I_C), or a maximum current (for a given emitter area A_E).

The physical reasons for this result can be traced to basic electrical properties of silicon, e.g., carrier mobilities, impact ionization coefficients, and heavy doping effects. Therefore, once V_{CEO} (sus) and h_{FE} (V_{CE}) are chosen, there will be a corresponding current density that cannot be exceeded and the only way to obtain the desired I_C is to make A_E large enough.

There are also other criteria which influence the transistor design. For example, switching times, forward and reverse safe-operating-areas, and junction leakage currents should be given consideration when designing a transistor; however, in most designs, the dominant terms are V_{CEO} (sus) together with some specification describing the on state, such as h_{FE} at some I_C and V_{CE}.

3.2 Design Examples

To demonstrate the design approach used during this contract, two examples are given here for V_{CEO} (sus) = 400V and 600V. During the

contract period, the method of [1] was modified to include the difference in electron diffusion coefficient D_n between base and collector regions. Also, the optimization sequence of [1] has been included as part of a computer program and the optimum impurity profile is now obtained directly without any intermediate steps.

The fact that current density goes through a maximum is demonstrated in Fig. 1. In this Figure, the peak current gain h_{FEO} is related to the impurity profile of Fig. 2 by

$$h_{FEO} = \frac{G_e}{Q_B/D_B} \quad (1)$$

where $G_e \simeq 5 \times 10^{13}$ cm^{-4} -s and is the emitter "Gummel number". Q_B is the total number of base impurity atoms per unit area, shown as the shaded area of Fig. 2. For an npn transistor

$$Q_B = \int_0^{W_{BO}} N_A(x)dx \quad (2)$$

where N_A is the base acceptor concentration and W_{BO} is the metallurgical base width. D_B is the electron diffusion coefficient in the base and is approximately equal to 20 cm^2/s for the type of designs used in this program.

Thus, as h_{FEO} is increased the "device variable" Q_B decreases according to (1). The remaining axis of Fig. 1 is called the reach-through parameter m and is defined by

$$m = N_C/N_{BB} \quad (3)$$

where N_C is the collector doping and N_{BB} is doping that corresponds to bulk breakdown with the emitter open (BV_{CBO}). Once m and h_{FEO} are chosen, it is possible to determine the three device variables Q_B, N_C and W_C, as is shown in [1]. Of these three, the collector width W_C is the most critical in terms of meeting a given V_{CEO} (sus), h_{FE} specification. The optimum design results are summarized in Table 1.

Curve 714553-A

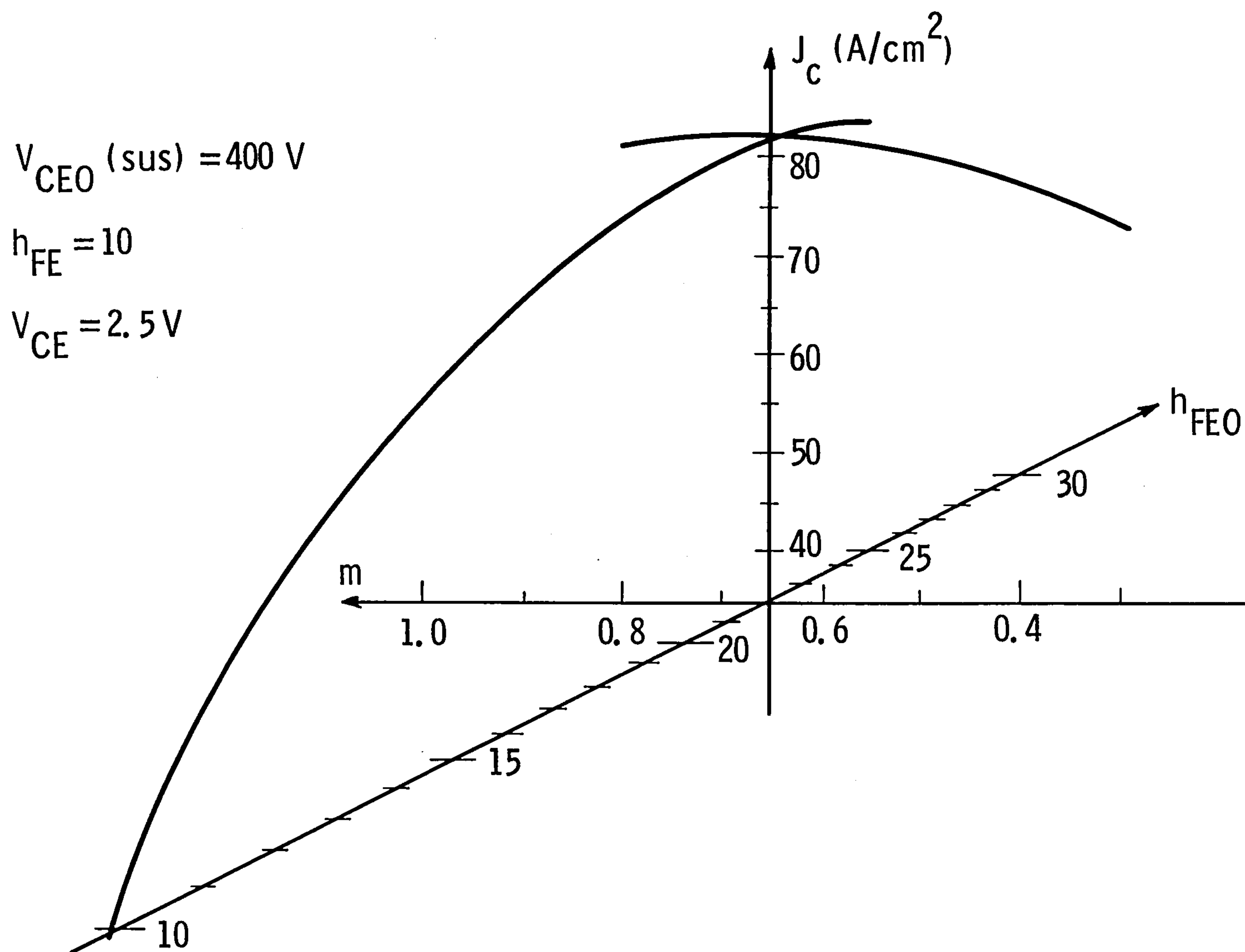


Fig. 1(a) Optimum design results for V_{CEO} (sus) = 400V. Collector current density is plotted perpendicular to the plane formed by peak current gain (h_{FEO}) and reach-through parameter m.

Curve 714552-A

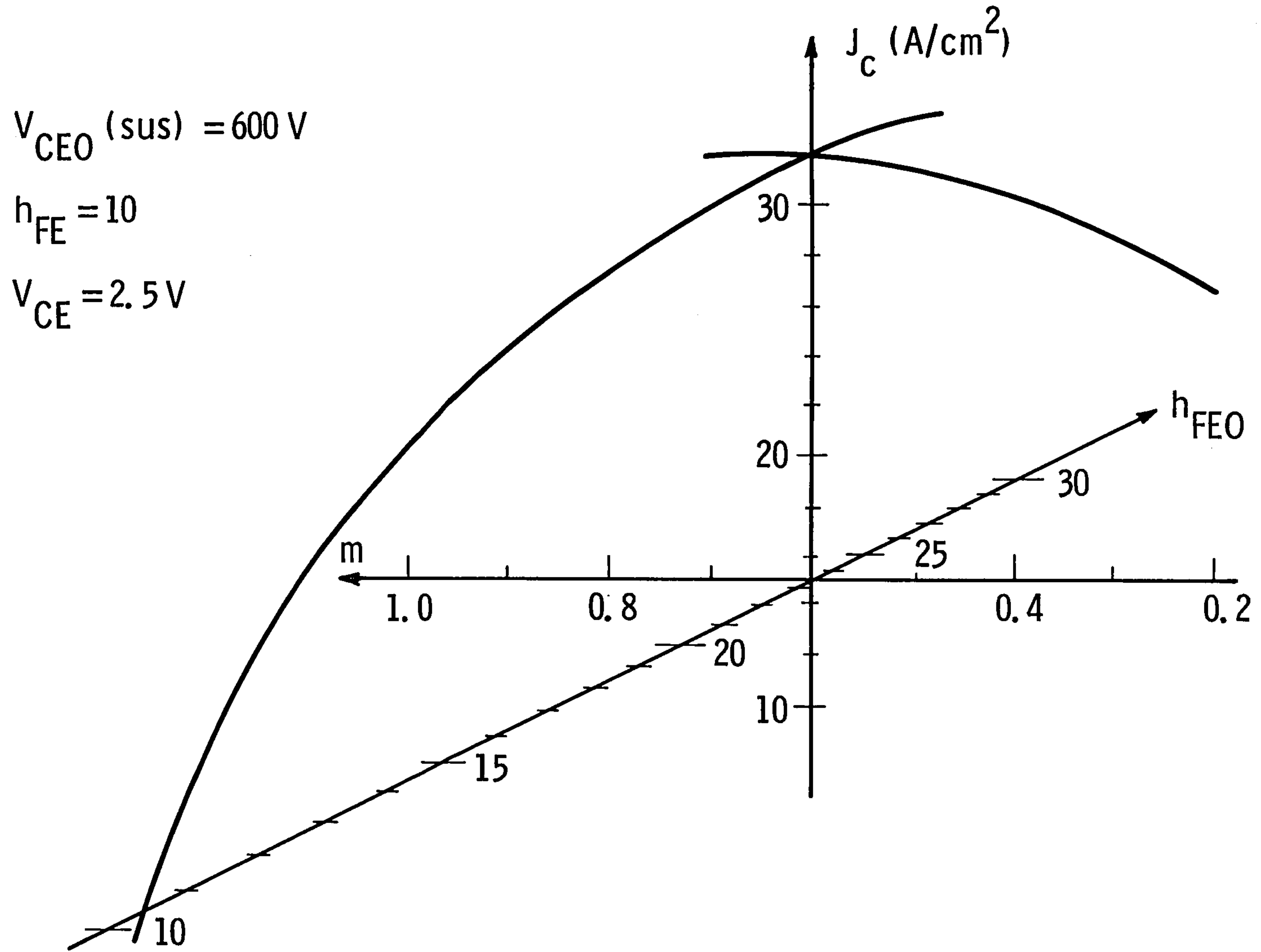


Fig. 1(b) Optimum design results for 600V. Collector current density is plotted perpendicular to the plane formed by peak current gain (h_{FEO}) and reach-through parameter m.

Dwg. 7684A90

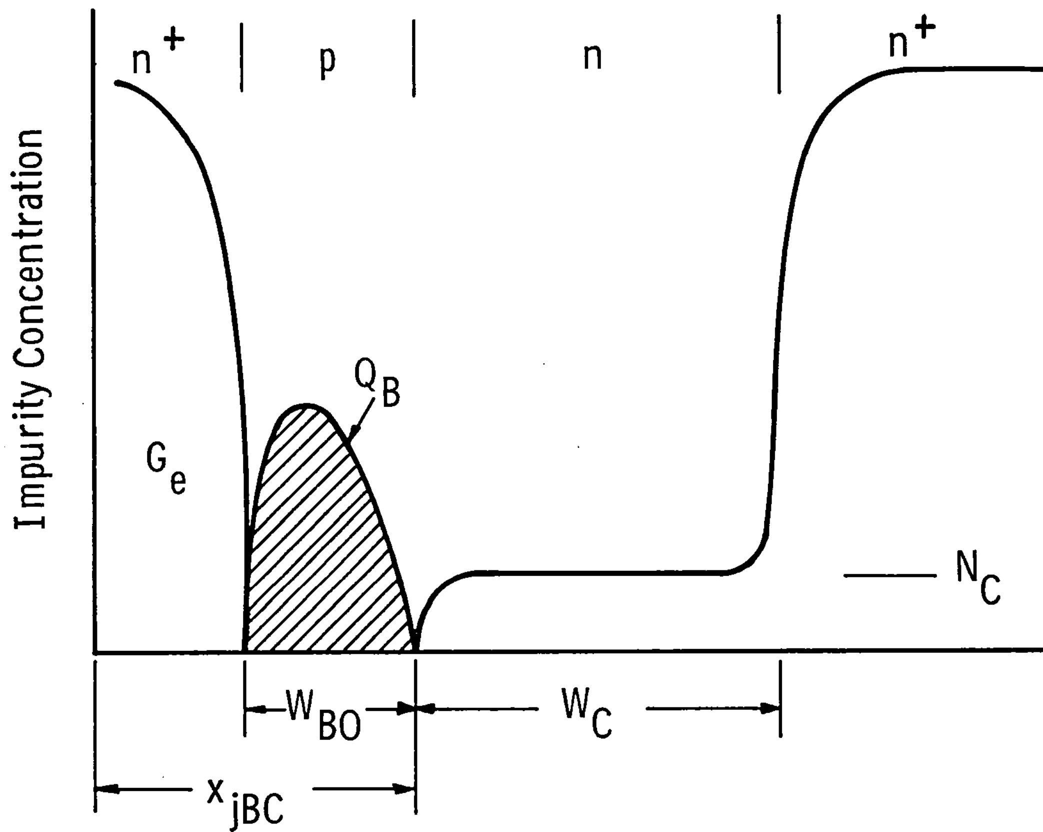


Fig. 2 General shape of the triple-diffused impurity profile.

TABLE 1

Optimum designs for h_{FE}=10 at V_{CE}=2.5V

V_{CEO}(sus)	J_C,max	N_C	W_C	h_{FEO}	Q_B
(V)	(A/cm^2)	(cm^{-3})	(μm)	-	cm^{-2}
400	81.4	1.72×10^{14}	44.1	23.6	4.24×10^{13}
600	32.1	1.01×10^{14}	69.1	23.6	4.24×10^{13}

physical constants: D_C = 22 cm^2/s, G_e = 5×10^{13} cm^{-4}-s, μ_{co} = 1.3×10^3 cm^2/(V-s)

D_B = 20 cm^2/s, ionization coefficient data from (1).

3.3 Sensitivity to Changes in Device Variables

It is important to consider variations in the three device variables, particularly if the device is to be manufactured in large numbers. The design theory has been extended to include the case where two of the variables are fixed and the third is varied over a range and the resulting h_{FE} and V_{CEO} (sus) is calculated. In this way, estimates of an acceptable limit on each device variable can be determined.

For example, Fig. 3 shows the effects of changing N_C, W_C and h_{FEO}. For this example V_{CEO} (sus) was chosen to be 450V and an $A_E = 1.0\ cm^2$ was assumed. As an example of specification limits, it was assumed that V_{CEO} (sus) $\geq$ 400V and $h_{FE} \geq 10$ at $I_C = 50A$, $V_{CE} = 2.5V$. The curves of Fig. 3 then show the maximum acceptable range of W_C (43 to 60 microns), N_C (0.58 to 2.2 x 10^{14}) and h_{FEO} (16 to 43). In reality, operation within smaller ranges would be desirable since all three quantities will have some distribution about the optimum value.

3.4 Emitter-Base Geometry

The design of the previous section assumes that the current density is uniformly distributed over the emitter. In reality, this never occurs since the lateral flow (under the emitter) of the base current I_B results in a "crowding" of the emitter current to the edge of the emitter stripe.

During the contract a new analysis of this problem has been worked out [2]. The two important parameters which characterize an interdigitated emitter-base geometry are the metallurgical emitter area A_{EM} and the perimeter along the base-emitter boundary Z. For most designs it is possible to relate the emitter finger width to A_{EM} and Z by

$$A_{EM} = Z\ L_E \qquad (4)$$

where L_E is approximately equal to one-half of the average emitter stripe width.

Most base-emitter geometries can be characterized by a "cross-over current" I_{CR} defined by

$$I_{CR} = 36\, q\, \frac{Z}{L_E} \frac{1 + b}{b}\, G_e\, D_C^2 \qquad (5)$$

where b is the electron-hole mobility ratio at high injection levels ($b \simeq 2$), and $D_C \simeq 22\ cm^2/s$ is the high-level electron diffusion coefficient in the collector. As I_C becomes comparable to I_{CR}, current crowding effects decrease the "effective" emitter area A_E from the metallurgical area A_{EM}. In this context, A_E is the area of a one-dimensional transistor with equal h_{FE}.

Figure 4 shows an example of the A_E reduction that occurs with increasing I_C for a mask design (659) that is described in Section 4 of this report. This graph was calculated using the mask dimensions and the analysis of [2]. Taken together with Fig. 1, this graph demonstrates the fact that the amount of interdigitation required will decrease for higher voltage transistors. For example, the maximum current density decreases from 81 to 32 A/cm^2 as V_{CEO} (sus) increases from 400 to 600V. Operating with A_E at the same percentage of A_{EM} would then allow almost a factor of 3 increase in L_E. This means that photolithography and emitter patterning techniques become less stringent as V_{CEO} (sus) is increased.

3.5 Forward Safe Operating Area

In the initial part of the program, a fair amount of effort was placed on predicting and measuring the forward SOA. Recently, switching performance has received more attention and for these applications, forward SOA is of secondary importance.

For applications where the transistor must dissipate significant power, as in a linear amplifier, the forward SOA is important and can be increased by "building-in" emitter ballast resistance R_E by selective emitter metallization schemes. For these applications, a realistic operating boundary is the onset of thermal instability which is shown in Fig. 5. It can be seen that the forward SOA can be improved substantially by making small increases in R_E.

Curve 714554-A

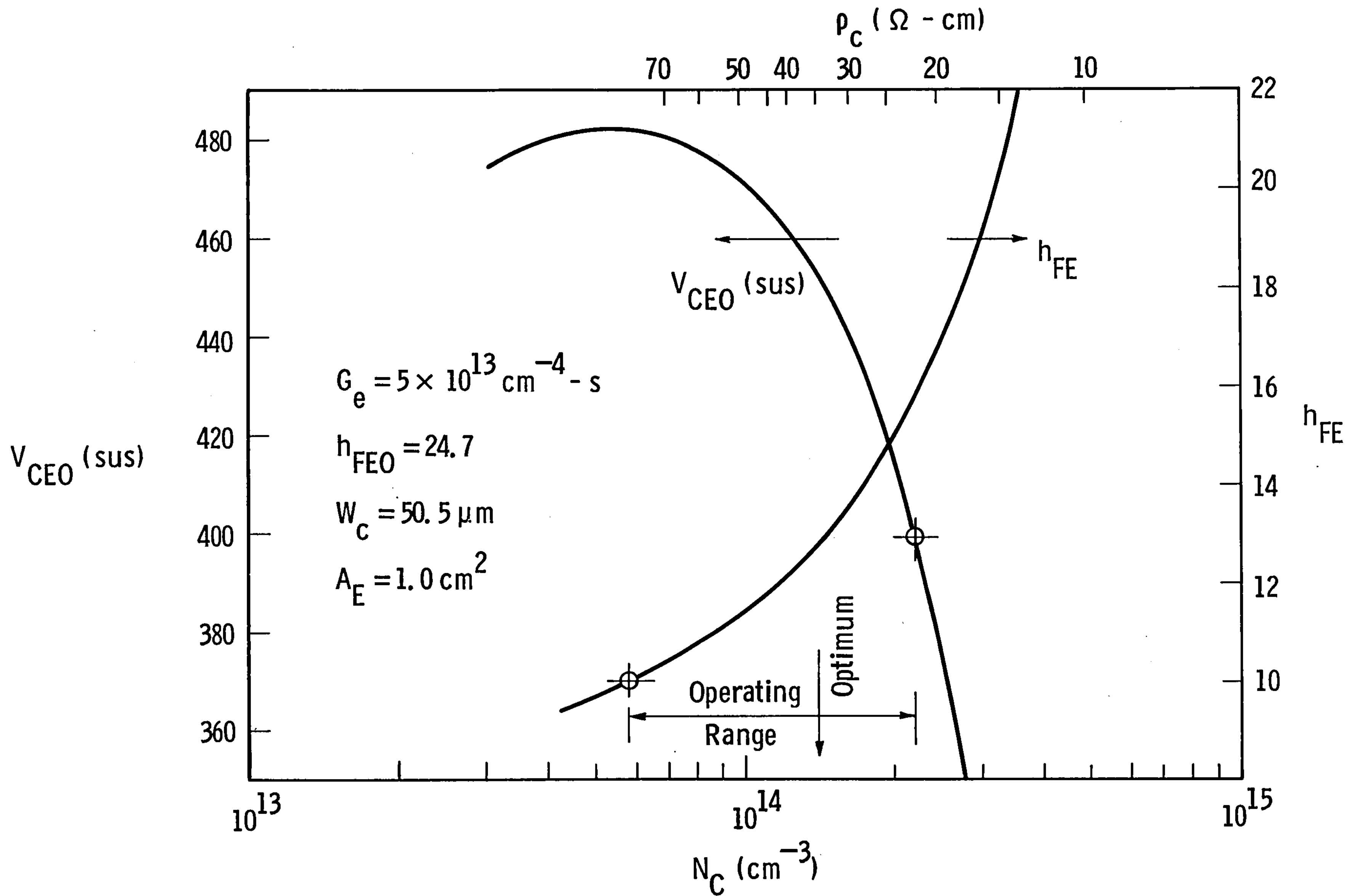


Fig. 3(a) Sensitivity of V_{CEO} (sus) and h_{FE} (I_C = 50A, V_{CE} = 2.5V) to collector doping.

Curve 714556-A

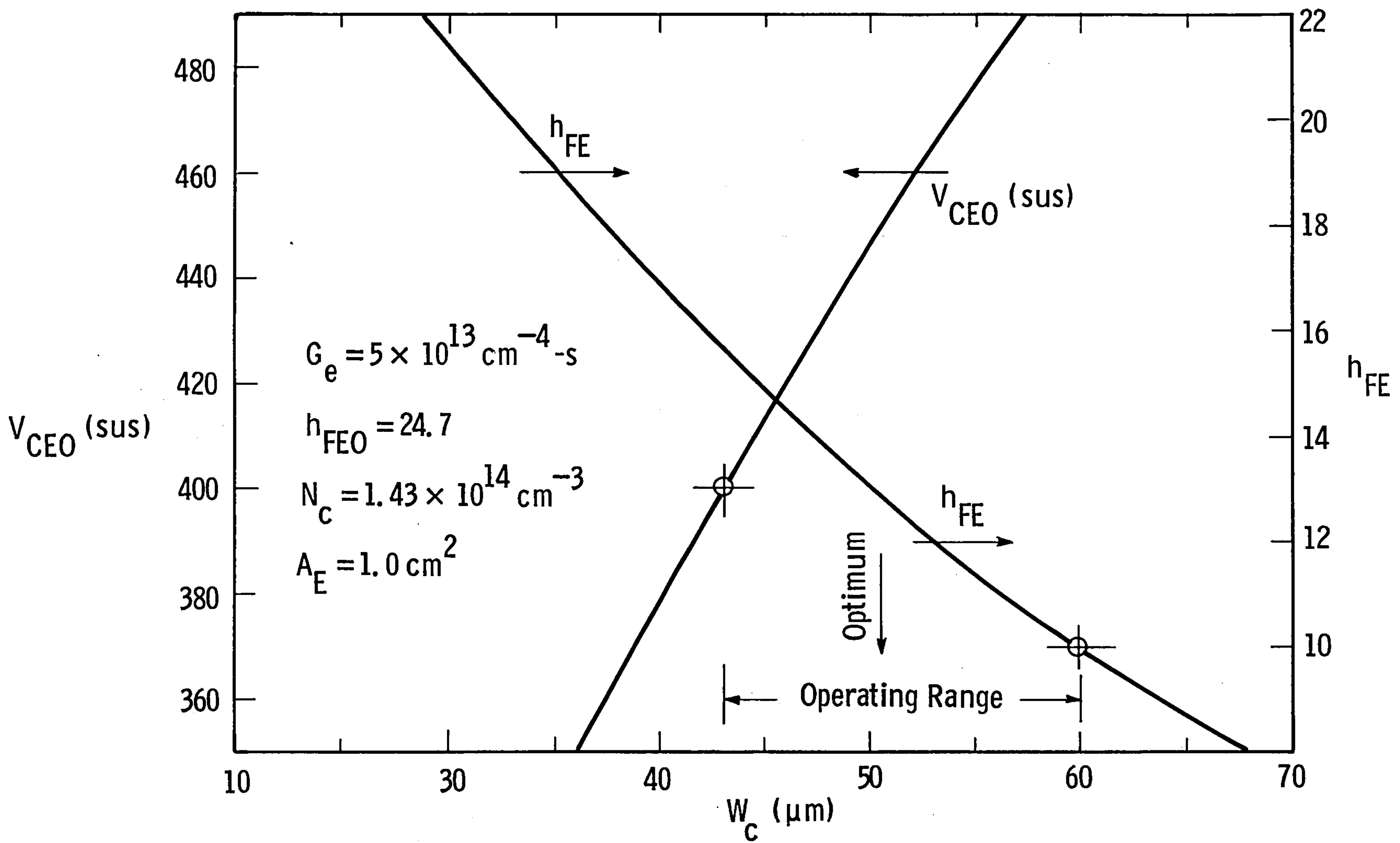


Fig. 3(b) Sensitivity of V_{CEO} (sus) and h_{FE} (I_C = 50A, V_{CE} = 2.5V) to collector width.

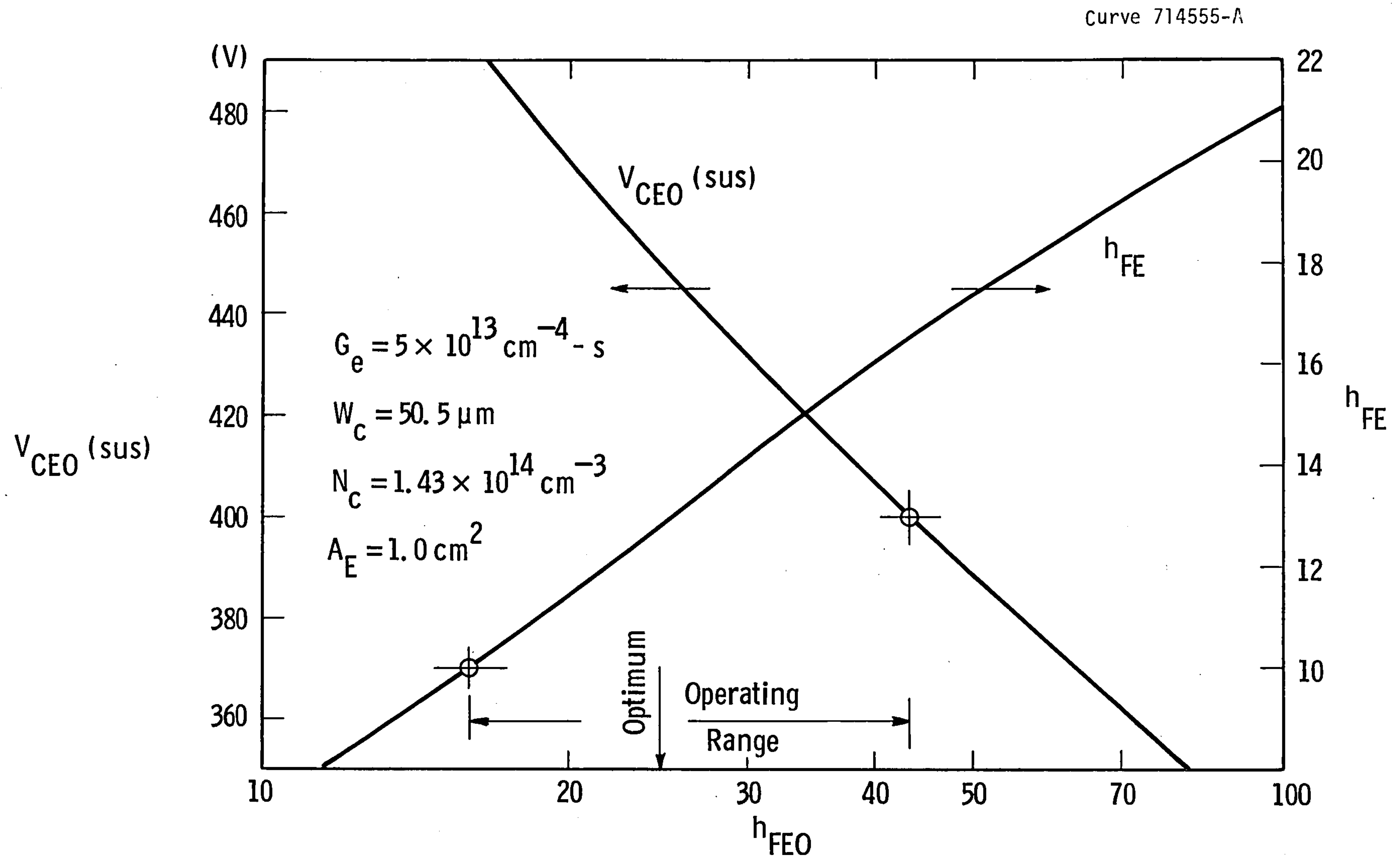


Fig. 3(c) Sensitivity of V_{CEO} (sus) and h_{FE} (I_C = 50A, V_{CE} = 2.5V) to peak current gain.

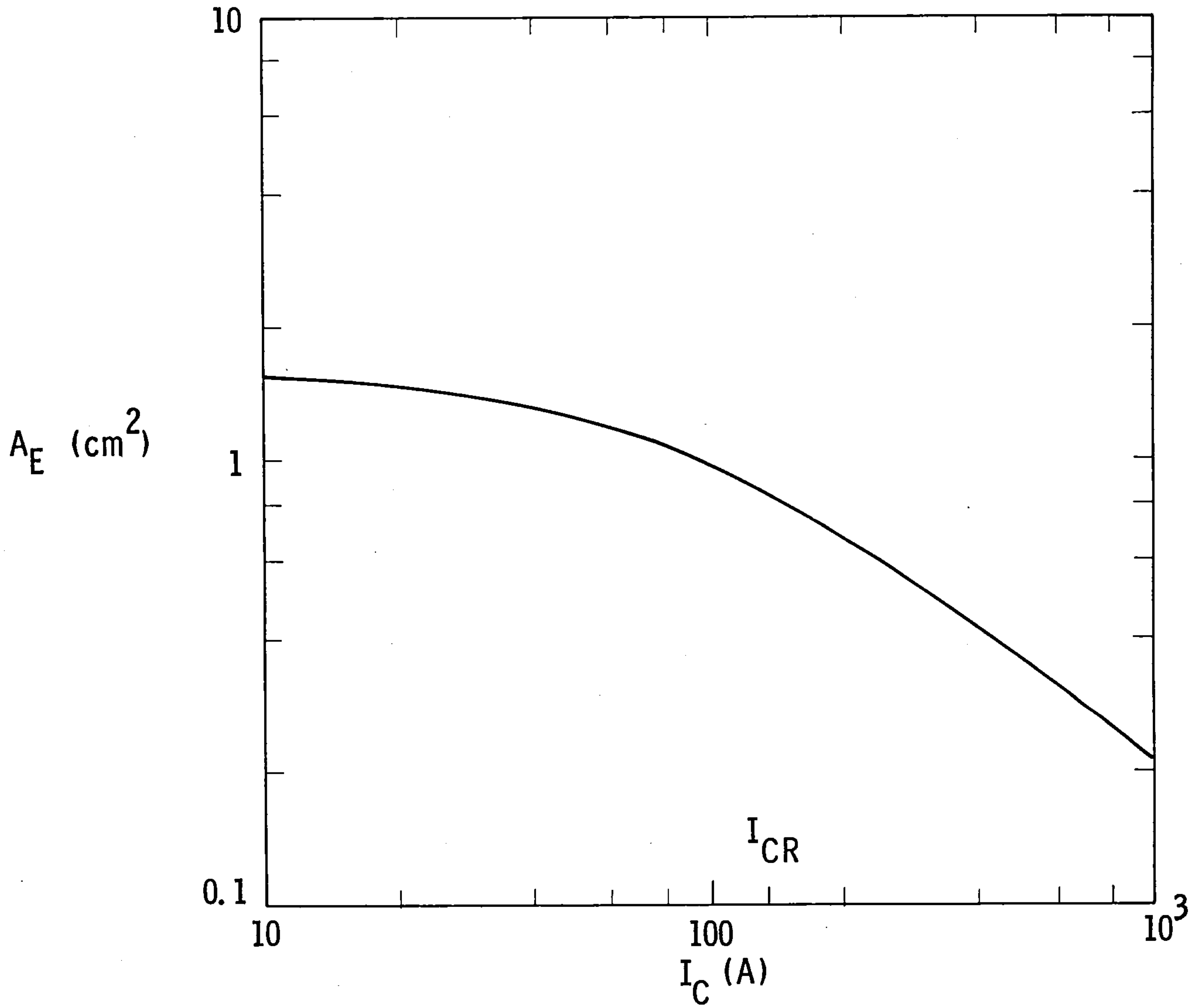


Fig. 4 Effective area vs. collector current for the 659 mask design (A_{EM} = 1.6 cm^2, Z = 33 cm, I_{CR} = 142A).

Curve 714625-A

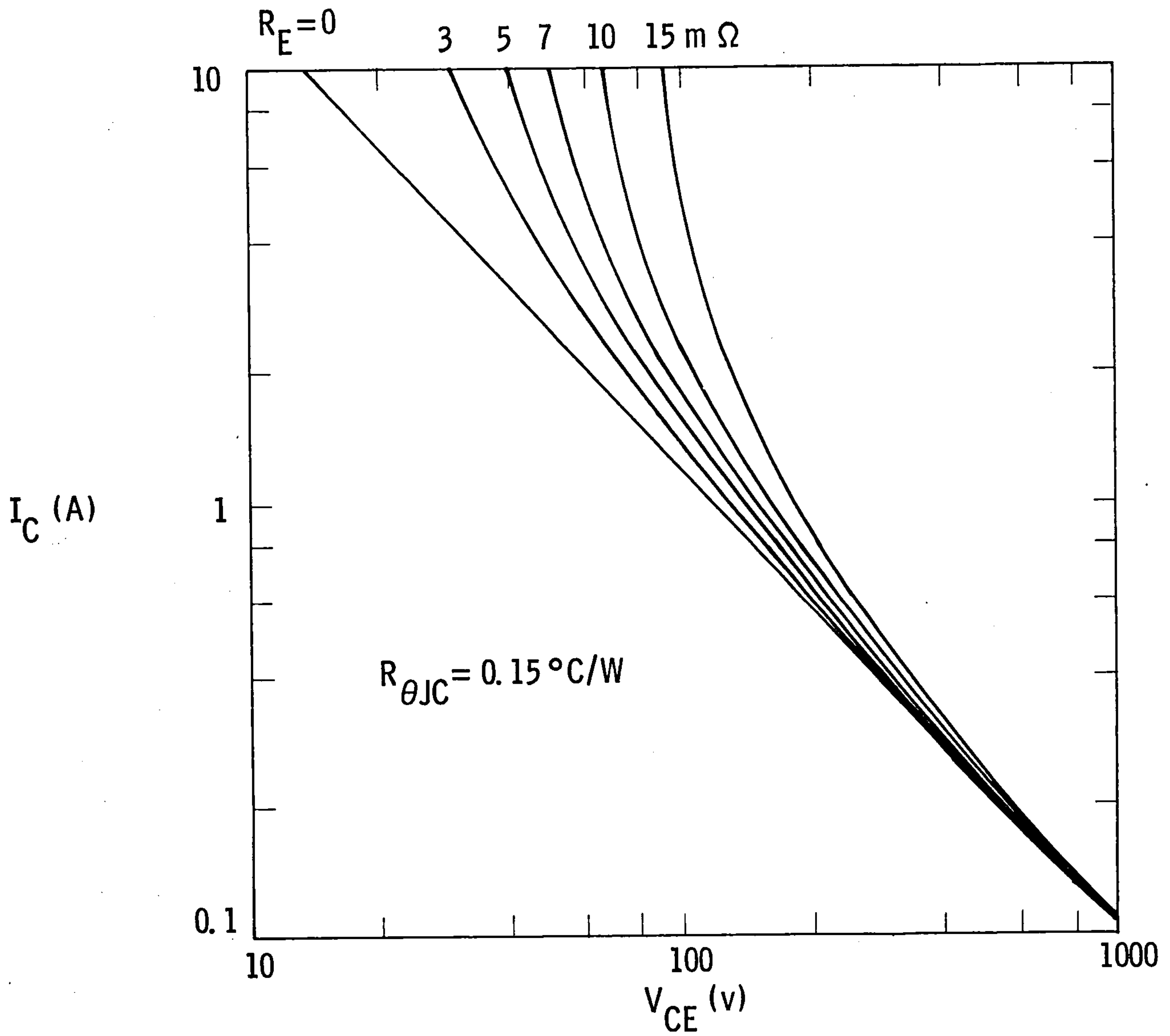


Fig. 5 Collector current vs. collector emitter voltage corresponding to the onset of thermal instability with emitter ballast resistance as the parameter.

3.6 Dynamic Considerations

At the present time, there is no comprehensive design theory for predicting the switching performance of bipolar transistors. This difficulty can be traced to the dearth of practical device models that account for device/circuit interaction in a typical regulator application. The inadequacy is particularly evident in trying to predict the turn-on and turn-off waveforms or the point of onset of second breakdown (Reverse SOA) for switching regulator type circuits.

Some progress has been made in predicting turn-on waveforms with a resistive load and also storage time, which is relatively insensitive to load inductance.

3.6.1 Turn-on

When the transistor is turned-on, a charge due to excess carriers is initially supplied to the metallurgical base and emitter regions of the transistor. As the turn-on process continues, the excess carrier concentrations reach a point where the base-collector junction changes from a blocking to an injecting junction and the effective base region "widens" into the metallurgical collector. Beyond this point, the turn-on process tends to slow down because of the relatively long time it takes to build-up the steady-state carrier profiles in the collector.

This process has been analyzed using a charge-control model [4] for the case of a resistive load. For this project, the predicted waveforms have been calculated for the 450V optimum design indicated in Fig. 3.

The collector current rise time corresponding to a 10 to 90 percent increase in $i_C(t)$ is shown in Fig. 6, where a step-like base drive current I_{BF} is assumed. As one might expect, increasing I_{BF} decreases the rise time. The abrupt increase in the slope of the curves corresponds to the onset of the base-widening process. On this portion of the curve, t_r is a strong function of I_C and I_{BF}. It can be seen that t_r values in the range of 0.2 to 0.5 μs should be obtainable for I_C in the range of 40 to 60A.

Curve 714626-A

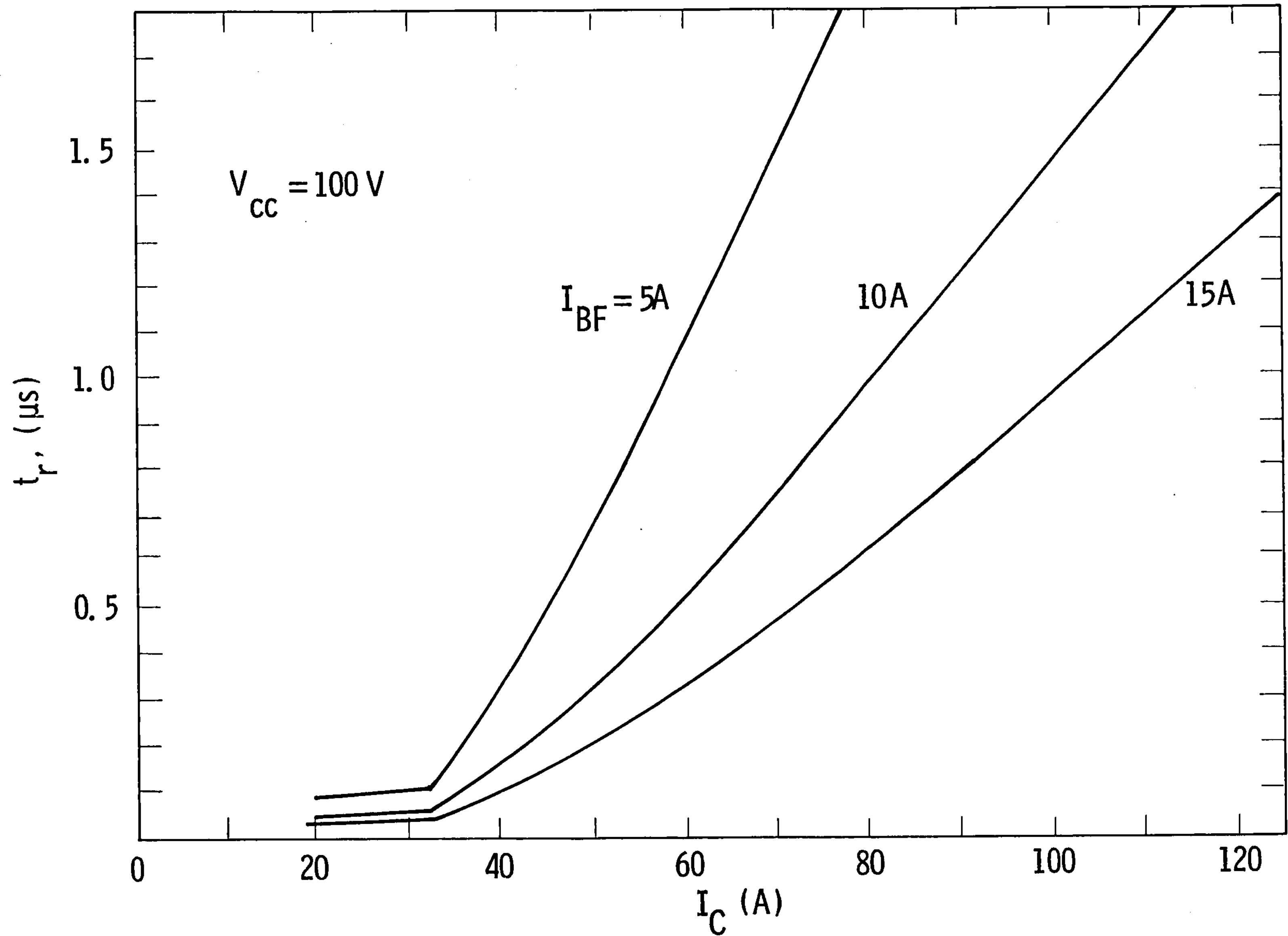


Fig. 6 Collector current rise time vs. collector current for different turn-on base currents.

The behavior of $v_{CE}(t)$ during turn-on is usually of more interest, since the voltage waveform exhibits a "tail" that can contribute a significant component to the overall switching loss. Figure 7 shows the predicted waveforms for the same conditions as in Fig. 6. Again, the abrupt change in slope at V_{CE} = 14.7V is due to the onset of the base-widening. Beyond this point v_{CE} is directly proportional to the thickness of the neutral or unmodulated portion of the collector.

3.6.2 Storage Time

Under this program a model for storage time has also been developed. This model accounts for the behavior in the "active" and "remote" base regions during the time it takes to reduce the excess hole concentration to zero at the n-n^+ (collector) junction by applying a reverse base current I_{BR}.

It is intended that the details of the analysis will be published at a later date. For present purposes it is only necessary to consider the results of the analysis. The curves of Fig. 8 are plotted for different values of base drive which is assumed to be symmetrical, i.e., $I_{BF} = I_{BR}$. If lifetime is varied, it has a monotonic effect on storage time with the greatest influence being at low values of I_C as can be seen from Fig. 9.

The reason the curves show t_s going to zero as I_C increases is that the "internal" base current required to achieve I_C is increasing and a smaller portion of the terminal current I_B is then available to forward bias the "remote" base-collector diode. Eventually, all of I_B is required to turn-on the transistor and it is no longer possible to forward bias the remote base-collector diode. At this point t_s = 0 and the operating point moves from the classical to the quasi-saturation region of the collector characteristic. For an approximate operating range of 10 to 60A of collector current these calculations show that a t_s in the range of 1 to 3 μs can be expected for typical base drive conditions.

Curve 714623-A

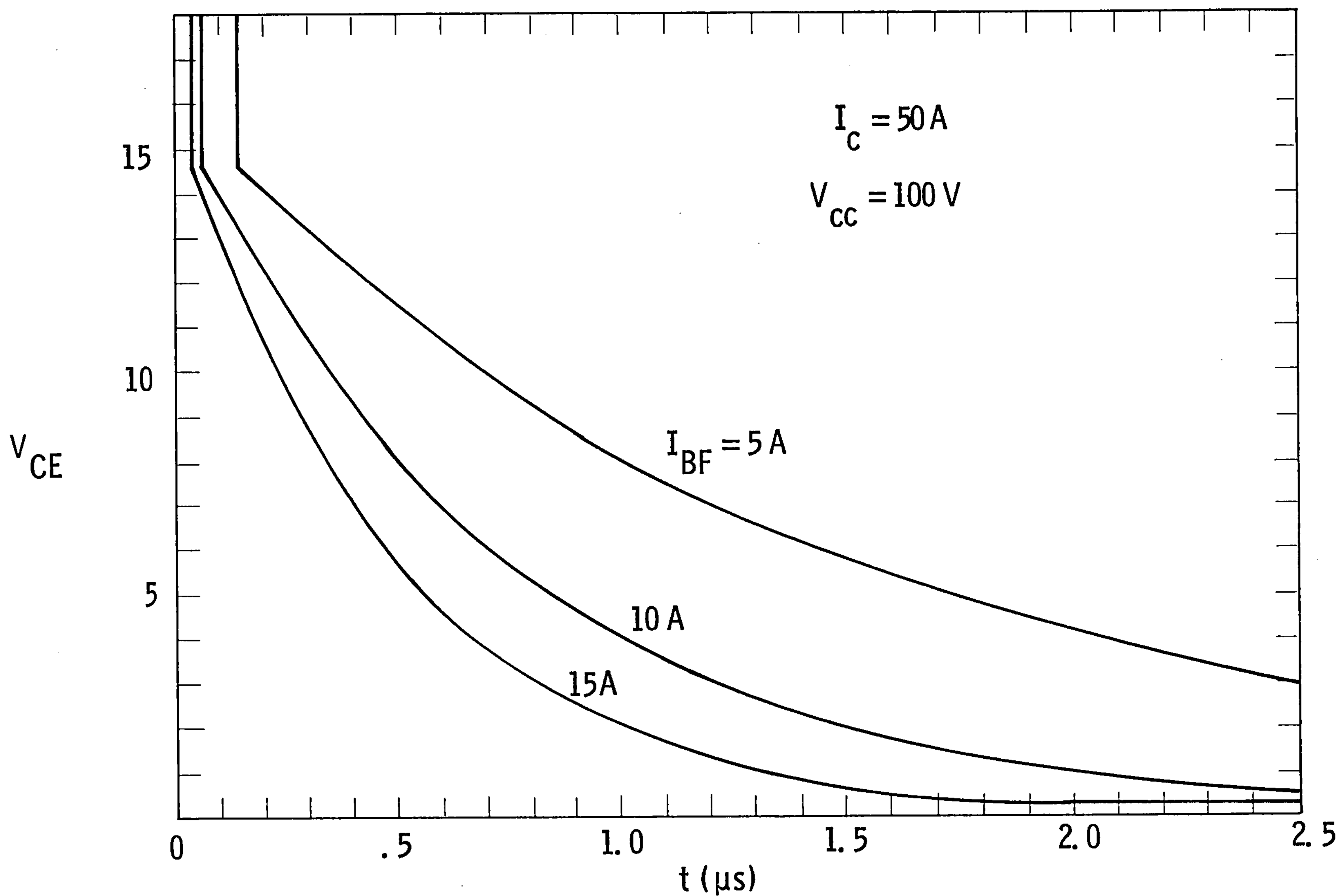


Fig. 7 Collector-emitter voltage waveforms for different turn-on base currents.

Curve 714650-A

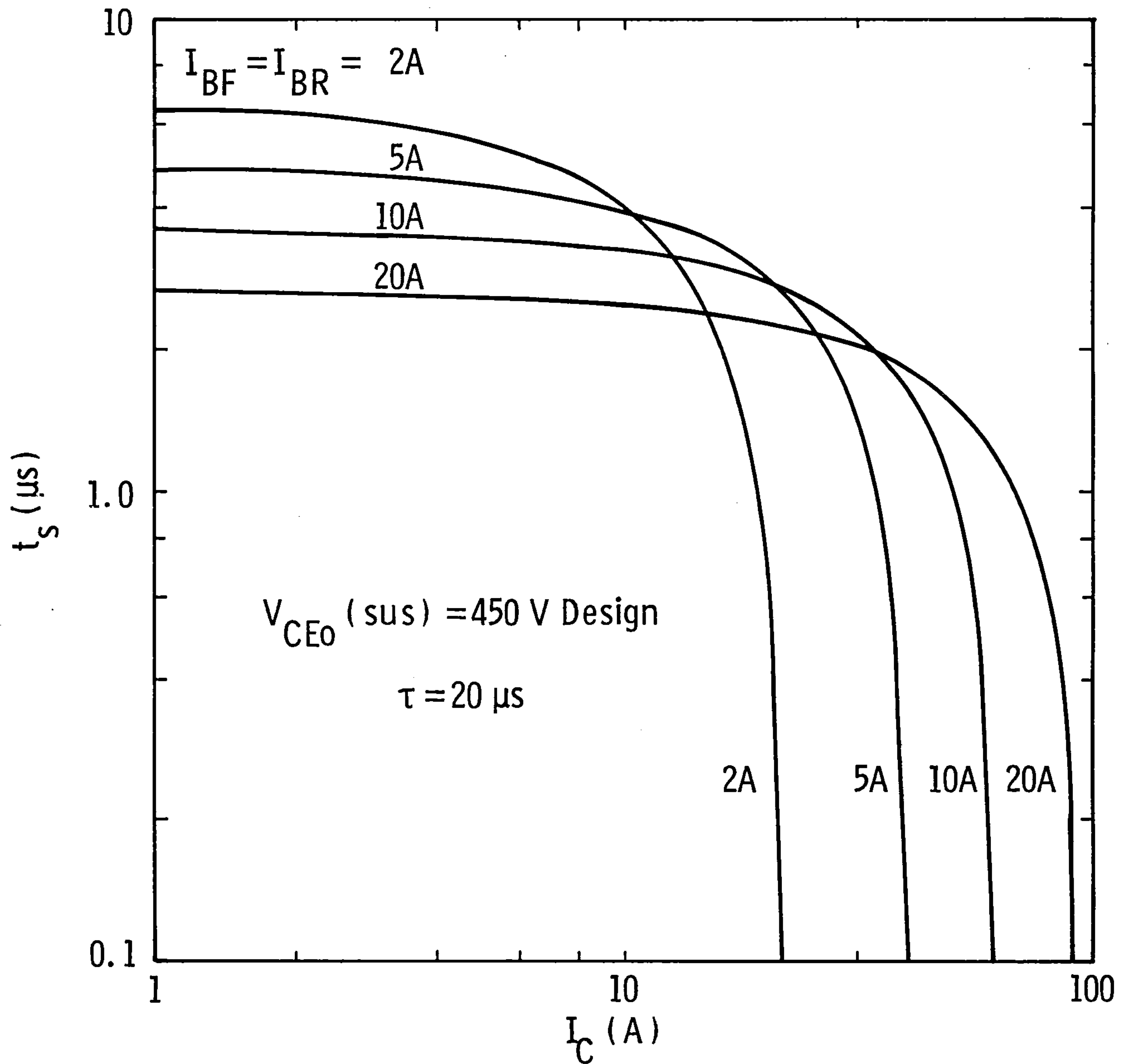


Fig. 8 Storage time vs. collector current with base current as the parameter.

Curve 714655-A

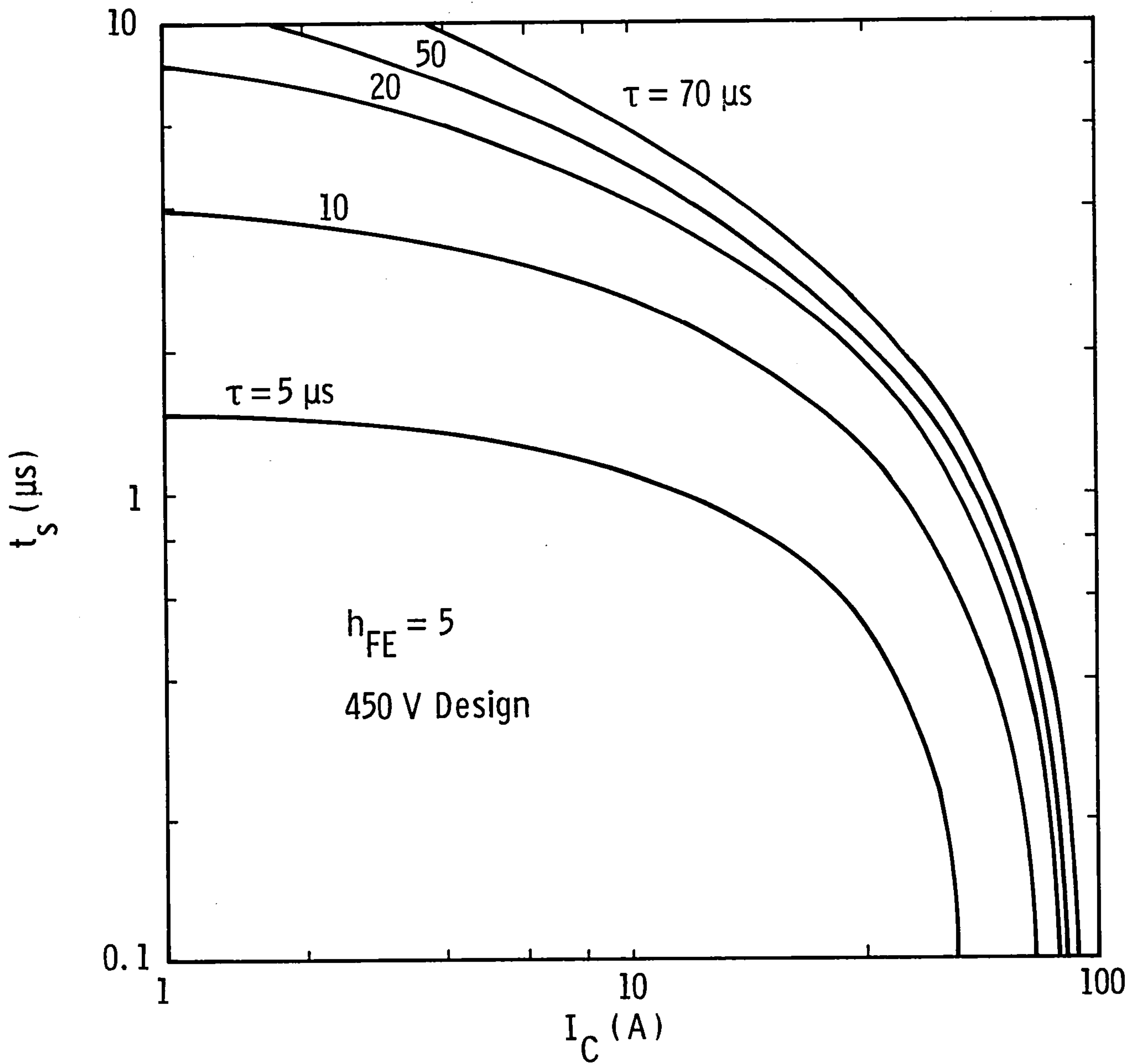


Fig. 9 Storage time vs. collector current with collector recombination lifetime as the parameter ($I_{BF} = I_{BR}$).

3.7 Other Considerations

For the calculations of Sections 3.2 and 3.3, the effect of collector recombination is ignored; however, a decreasing value of τ can seriously degrade h_{FE}, since additional base current is now required to accommodate the recombination process occurring in the base-widened portion of the collector.

The influence of τ on h_{FE} at I_C = 50A and t_s at I_C = 20A is shown in Fig. 10. The value of h_{FE} for an infinite τ is 12.9. It is possible to stay within 10 percent of this value provided $\tau \geq 35$ µs. Thus this type of calculation can be used to provide a guide for lifetime requirements of the wafer processing.

The topics of turn-off behavior and reverse SOA are discussed in Section 5. Also included in that section are comparisons between measurements and the models used for the device designs of the present section.

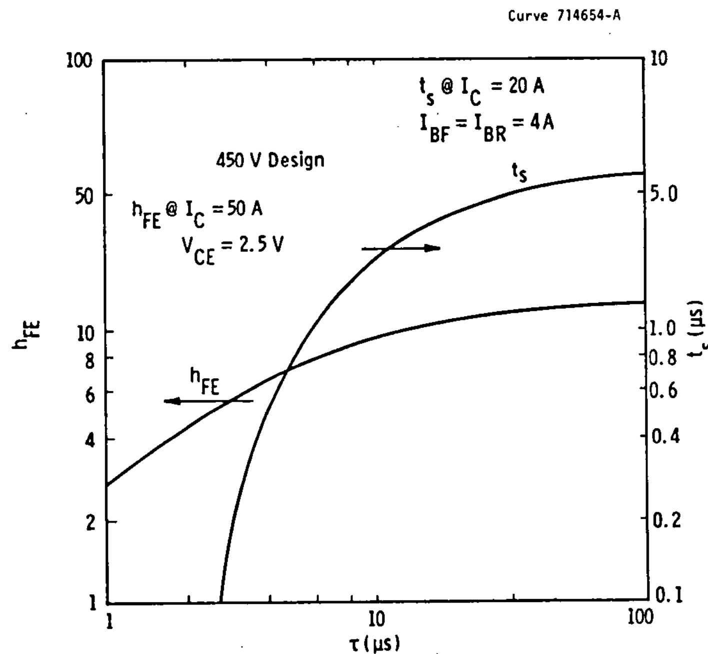


Fig. 10 Influence of lifetime on the current gain and storage time for the V_{CEO}(sus) = 450V design

4. PROCESSING INVESTIGATION

4.1 Packaging Considerations

One of the major strengths of the approach used in this program is that maximum use is made of existing Westinghouse high-power silicon device technology. The problems of fabricating p-n junctions over a large area, say $\gtrsim 2\ cm^2$, have been solved to a large extent with these techniques.

In addition, problems with "hot spots" due to voids in the silicon-metal interface are generally avoided with present techniques. These include alloying the silicon wafer to a molybdenum substrate and then packaging the resulting element or "fusion" under pressure to ensure good electrical and thermal contact. This process has been termed Compression-Bonded Encapsulation ®, or CBE, and has many advantages which are appealing for large-area transistor fabrication.

The CBE technique differs significantly from methods used to make the large majority of power transistors which typically have a chip area $< 1\ cm^2$. For these devices, the silicon chip or die is solder-bonded to a header, and base and emitter contact is made via soldered tabs or ultrasonically-bonded wires as shown in Fig. 11.

It might appear that the conventional methods could be "scaled-up" to larger areas, but there are difficulties with this approach. Contacting the emitter area with many wire bonds would be needed to ensure uniform current distribution. This becomes topologically awkward and also expensive. In addition, solder-bonding a large area chip runs the risk of forming a void which can seriously degrade the forward SOA.

The CBE technique overcomes these problems and, in addition, provides an opportunity for topside heat removal if a disc-type package is used. Figure 11 shows the cross-section of the stud package which was used for most of the devices fabricated under this program. This

Dwg. 1702B79

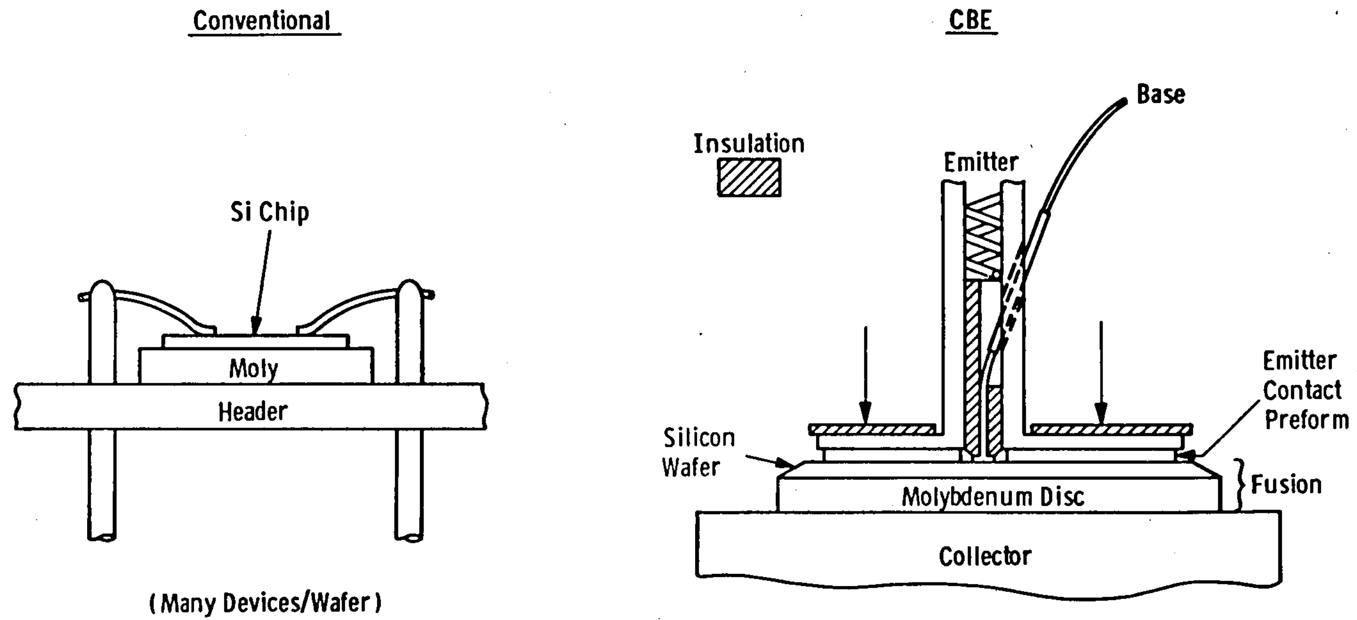


Fig. 11 Cross-sections showing conventional and CBE assembly techniques. The external package (not shown) provides the compressive force indicated by the arrows.

package is generally more convenient to use and the resulting thermal resistance (0.13 to 0.18 °C/W) is adequate for most applications. Figures 12 and 13 show the transistor fusion and stud package. Figure 14 is reproduction of the metallization pattern of the 659 mask used for the fusion of Fig. 12.

4.2 Impurity Profile

While the techniques used under this program have many things in common with high-power rectifier and thyristor technology, there are also some significant differences. Foremost among these is the impurity profile, which is shown in Fig. 15 for a typical design. It can be seen that the junction depths are considerably shallower than for a typical high-power rectifier or thyristor.

It is worth noting that deeper junctions could also be used here, but this would require some sacrifice in switching times t_r and t_f. However, the advantage of this approach is that there would be some improvement in the base-collector breakdown voltage (BV_{CBO}) due to the improved contouring that can be obtained with a deeper base-collector junction [5]. In addition, some improvement beyond the "optimum design" results can be obtained if the base contains a region that has a concentration comparable to the collector. This problem has been investigated by Kotowski [6], who concludes that for metallurgical base-widths less than approximately $W_C/5$, the improvement will be negligible. Thus a $W_{BO} \gtrsim 20$ μm would probably be necessary.

The improvements that might be obtained with a deeper base-collector junction become of secondary importance if the transistor is to have low losses during turn-off. As shown in Section 5, these losses are usually dominant and therefore limit the maximum switching frequency. For this reason, emphasis was placed on a profile having a metallurgical base-width of 10 to 12 μm.

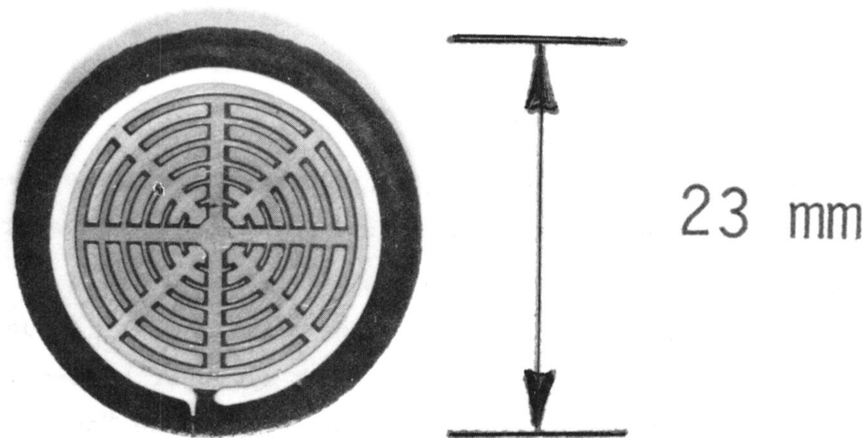


Fig. 12 Transistor fusion with emitter preform attached.

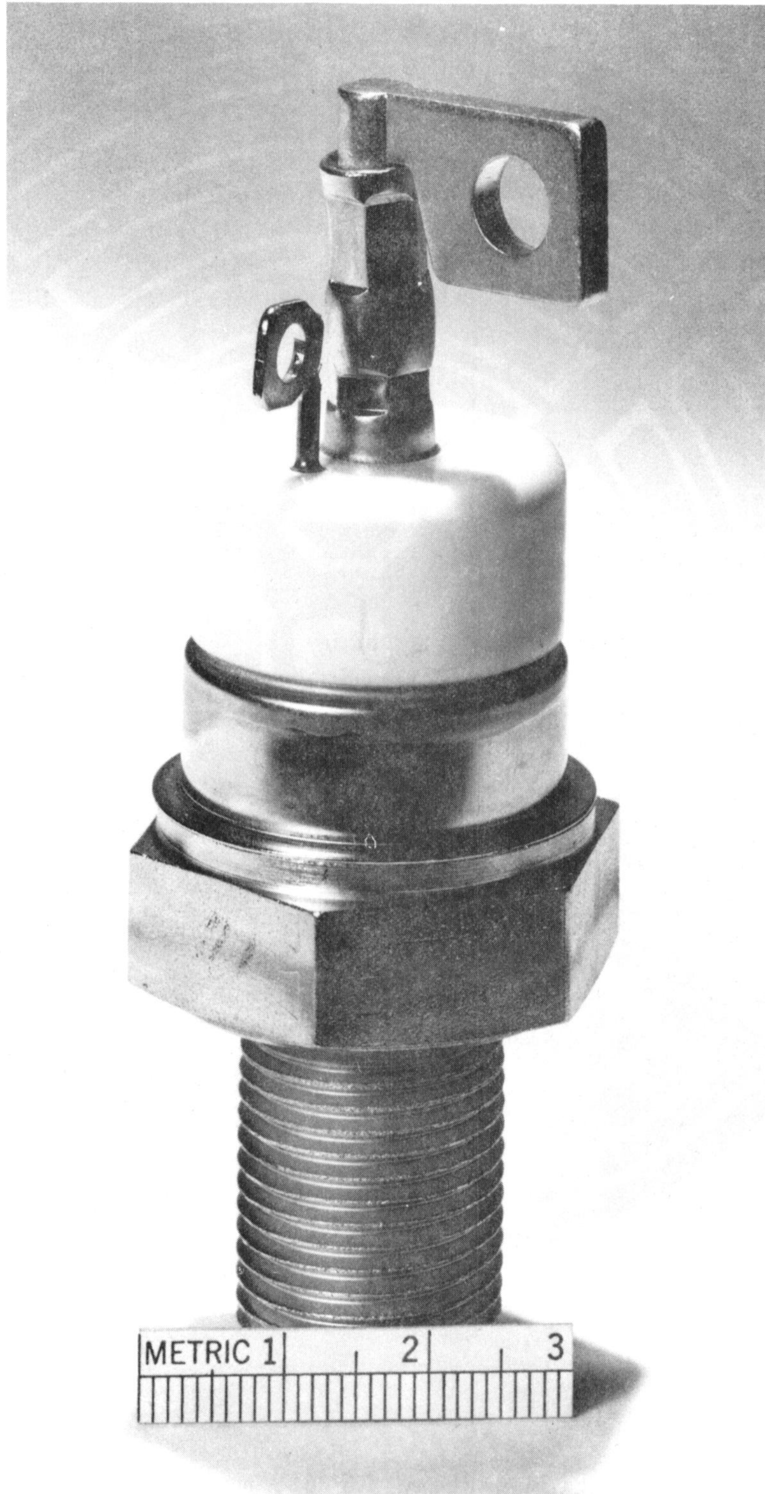


Fig. 13 Stud Package used for encapsulating fusion of Fig. 12.

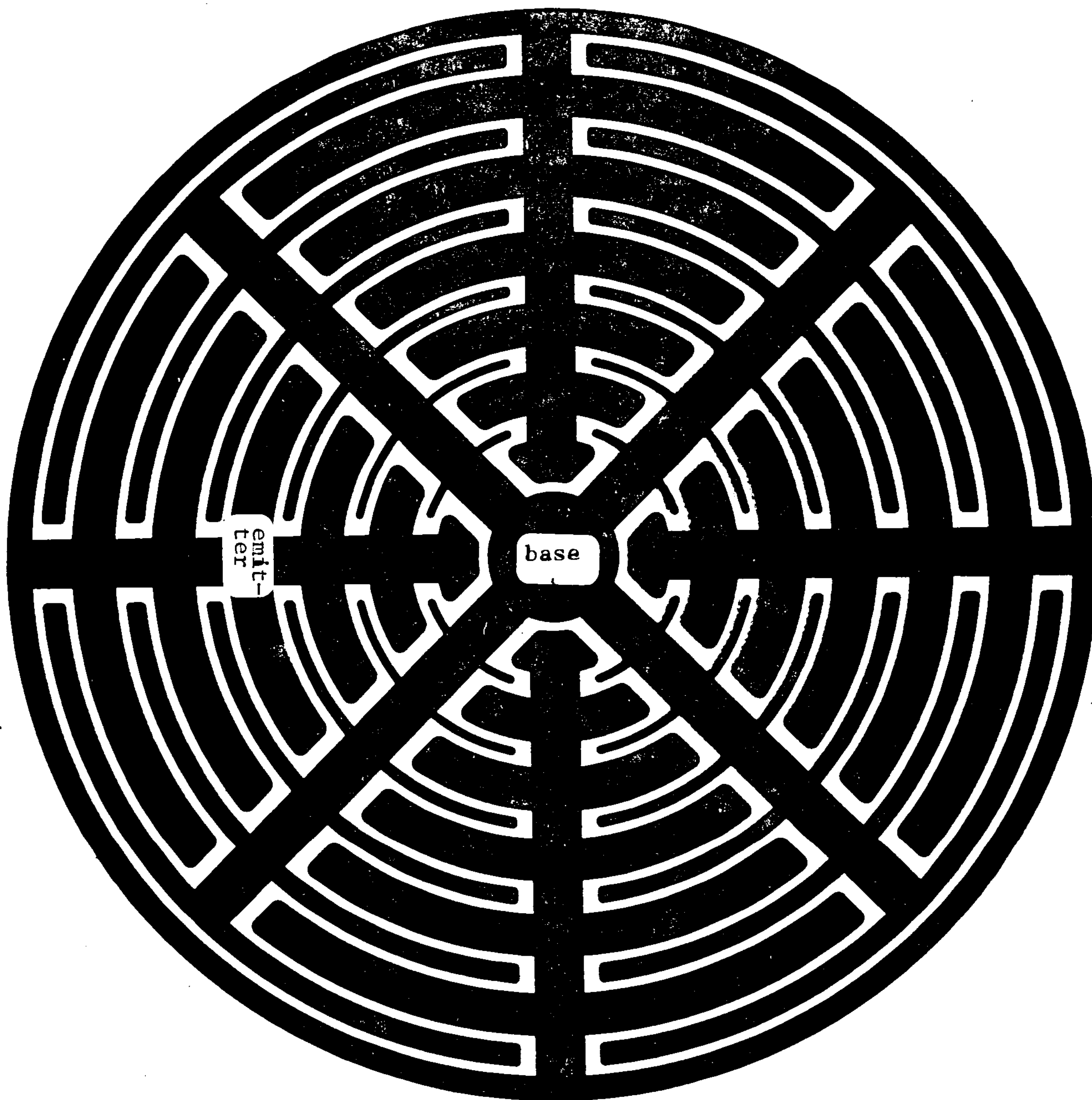


Fig. 14 Metallization pattern for 659 mask.
The outer diameter is 1.67 cm.

Curve 714656-A

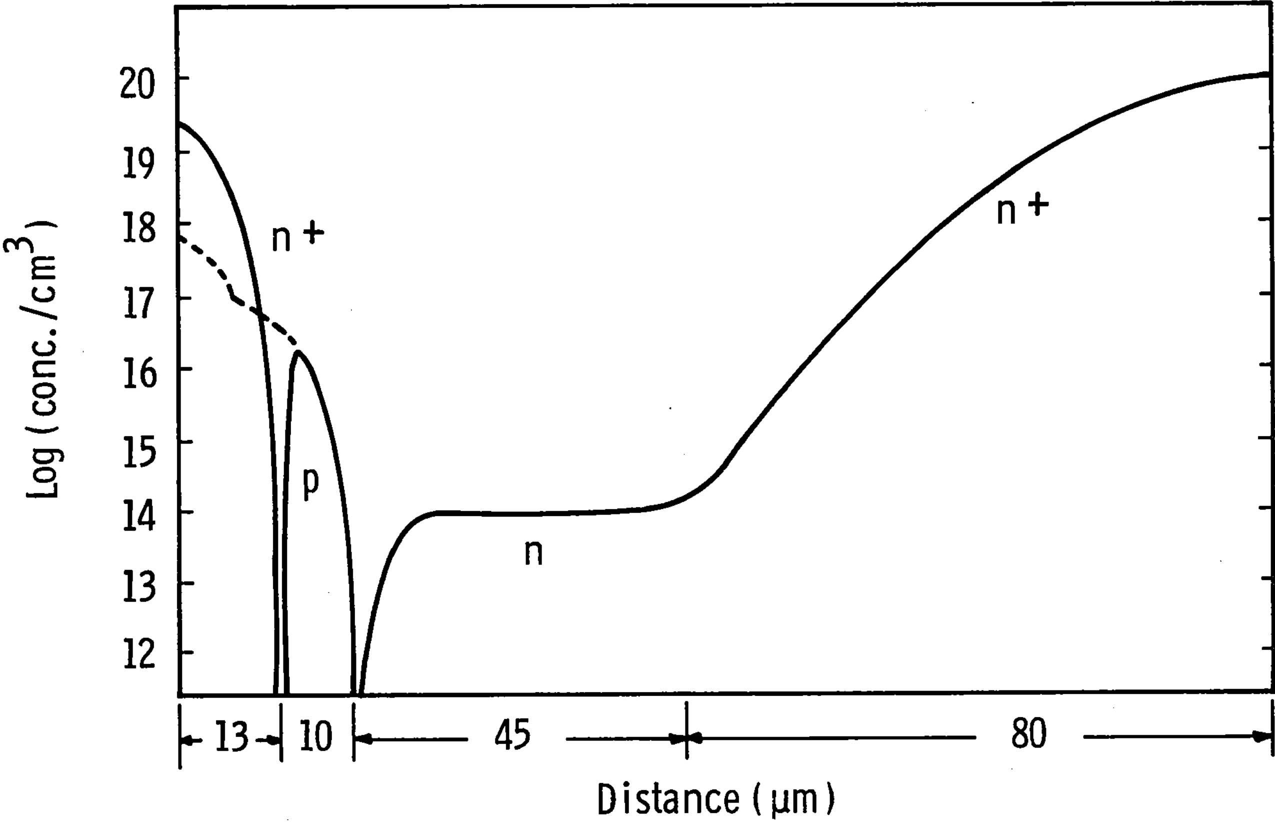


Fig. 15 Impurity profile showing typical concentrations and dimensions.

4.3 Wafer and Fusion Processing

Standard silicon wafer processing techniques were used to fabricate the transistor wafers. Numerous processing options were investigated and the particular sequence outlined in Fig. 16 was found to give the most favorable results. This Figure also shows a schematic cross-section of the wafer at each step.

The "emitter preform" is a replica of the metallized emitter region that is etched from a thin sheet (6 mil) of molybdenum. As shown in Fig. 11, the preform allows metallurgical contact to the emitter but avoids shorting out the base, which is contacted separately at the center of the fusion.

Beveling the base-collector junction is accomplished using a 5 deg. (negative) bevel. As described in the Interim Report [7], high-voltage planar junctions were also investigated with some success; however it was felt that this process requires additional work before it can compete satisfactorily with the standard bevel-etch technique.

For the diffusion steps, the phosphorous and boron diffusions are conventional open tube processes ($POCl_3$ and BBr_3) while the Ga-Al diffusion is a sealed-tube process. The experimental results obtained under this contract indicate that the process of Fig. 16 is a good candidate for a production process of large-area transistors.

Dwg. 2621C51

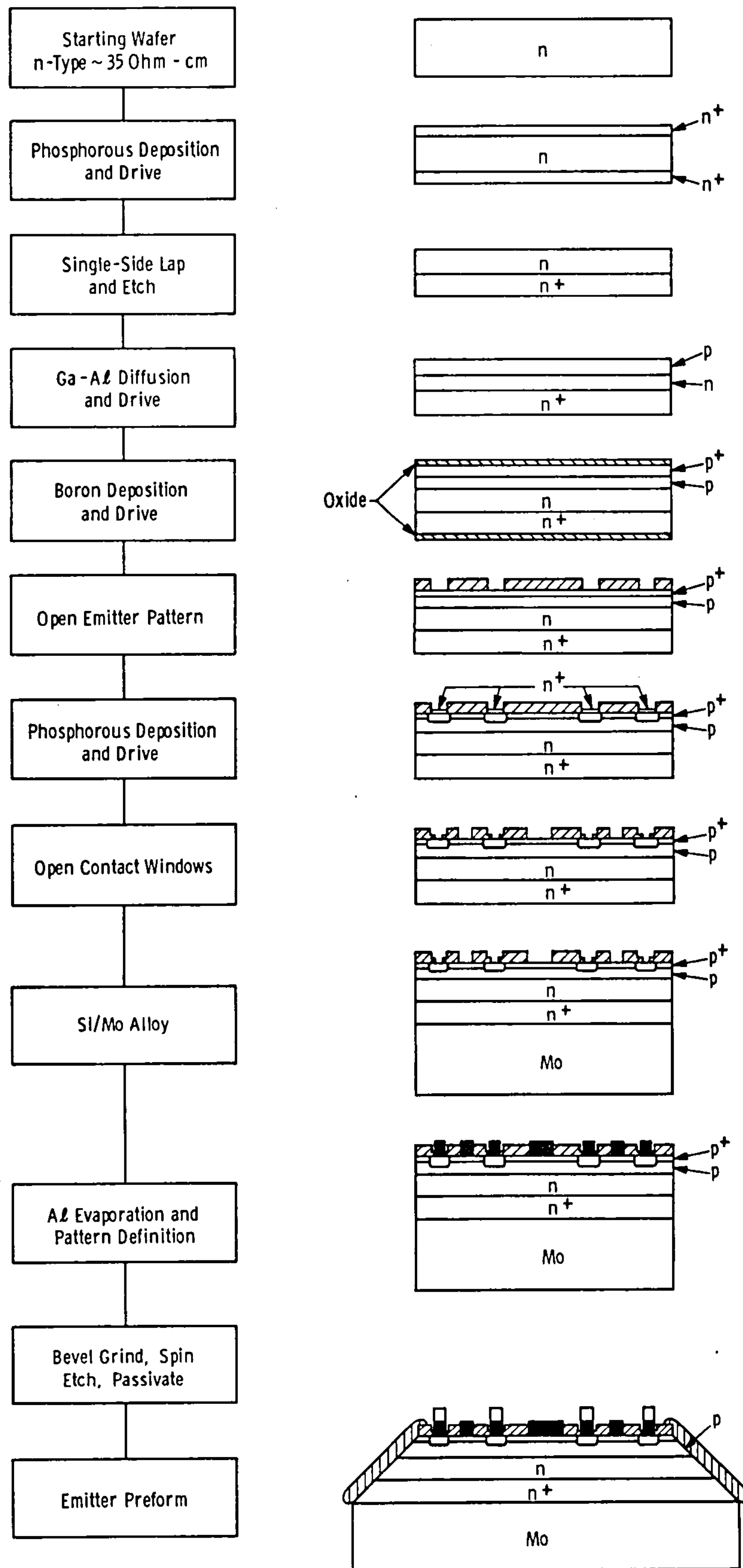


Fig. 16 Processing flow sheet with device cross-sections.

5. ELECTRICAL PERFORMANCE

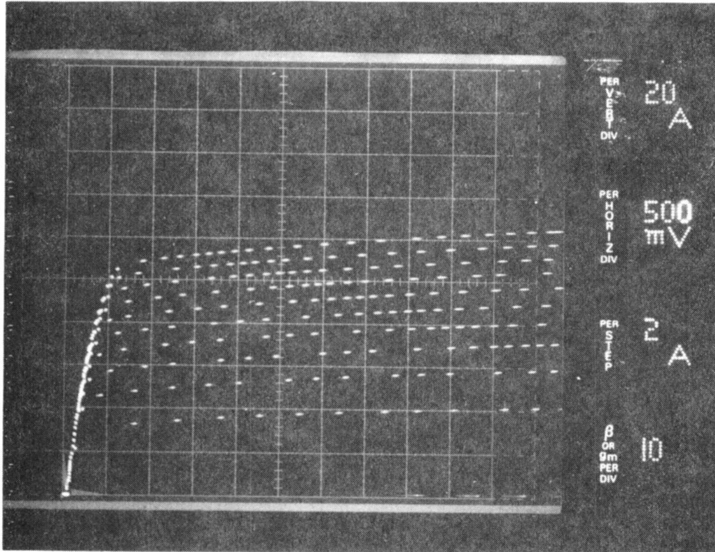
Several electrical characteristics were measured for each experimental run of transistors. Typically, these measurements included the characteristics discussed in Section 2 (h_{FE}, V_{CEO} (sus), forward SOA, t_t, and t_s). In addition, a new method of rating the switching performance [8] was developed during this program. These new results are summarized in this section. Detailed device data is given in Appendices 1 and 2. Appendix 1 summarizes the results obtained during the period covered by the Interim Report [7], while Appendix 2 gives data on devices fabricated during the final portion of the contract.

5.1 Collector Characteristic

The collector characteristics were measured using a Tektronix 576 curve tracer with a 176 power pulse unit. This combination has a maximum I_B of 20A and a maximum I_C of 200A. V_{CEO} (sus) was measured using a conventional inductive load circuit with a load inductance of 25 mH. Two examples of the collector characteristics are shown in Fig. 17 for devices having different V_{CEO} (sus) voltages.

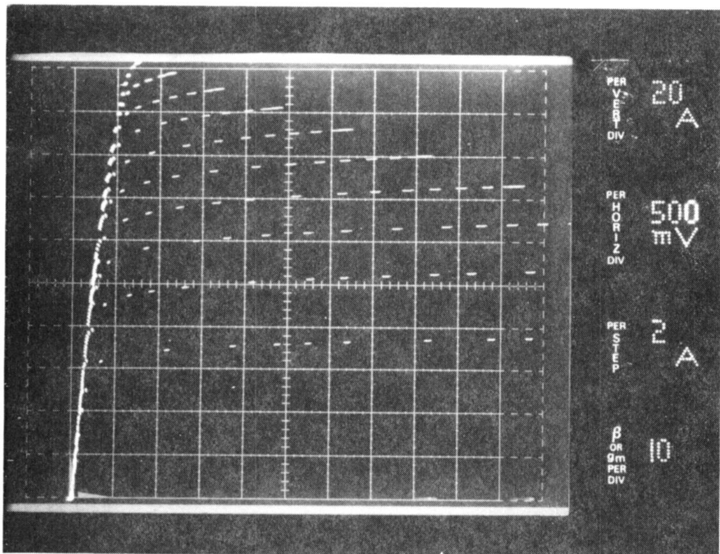
At large currents, h_{FE} becomes approximately inversely proportional to I_C. That is, the product h_{FE} I_C approaches a constant. As noted in Table 2 transistor 25A21 has h_{FE} I_C = 700A and for 21A7, h_{FE} I_C = 2500A. These values are about 70 percent of the maximum h_{FE} I_C products one could expect with infinite lifetime and all other device parameters at their optimum values.

Figure 18 shows the distribution of h_{FE} I_C vs. V_{CEO} (sus) for approximately 50 devices taken from different experimental runs. It can be seen that h_{FE} I_C for some devices exceeds the maximum theoretical value. This is most likely due to G_e exceeding the value of 5×10^{13} cm^{-4} -s which was used for the calculation. Values of $G_e = 8 \times 10^{13}$ cm^{-4} -s have been obtained in some cases, e.g., see Table 2. These G_e values are also in agreement with the results reported in [9].



Device 25 A 21

$V_{CEO}(sus) = 485V$



Device 21 A 7

$V_{CEO}(sus) = 190V$

Fig. 17. Measured collector characteristics for two devices with different sustaining voltage.

TABLE 2

Characteristics of Transistors of Fig. 17

$V_{CEO}(sus)^{(3)}$ (V)	G_e (cm^{-4}-s)	Measured h_{FE} $I_C^{(1)}$ (A)	Maximum h_{FE} $I_C^{(2)}$ (A)
485	8.02×10^{13}	700	988
190	6.0×10^{13}	2500	3410

Notes:

(1) $V_{CE} = 2.5V$, $h_{FE} = 10$

(2) For $\tau = \infty$ using measured G_e, the current-crowding analysis of [2], and $N_C = 1.43 \times 10^{14}$ cm^{-3}.

(3) At $I_C = 200$ mA.

The devices of Fig. 18 showed collector lifetimes in the range of 10 to 40 μs. This variation accounts for some of the scatter in the data points. Other quantities also vary about their target values, e.g., h_{FEO}, N_C and W_C, and contribute to the dispersion of the data points.

The amount of scatter indicated in Fig. 18 is considered to be acceptable as a starting point for an initial attempt at quantity production. Refinements in production methods can be expected to reduce the scatter.

5.2 Forward SOA

Some experiments were carried out using a metallization pattern which increases the effective value of series emitter resistance R_E. In this way it was possible to increase the forward SOA as mentioned in Section 2 in connection with Fig. 5.

The normal 659 mask pattern typically gives an R_E of 3 milliohms, as measured on the 576 curve tracer by the floating collector method [10]. For a one second test at V_{CE} = 100, the predicted I_C for thermal instability is 1.35A for this R_E.

As R_E is increased, the thermal instability collector current will increase as shown by the curve of Fig. 19. R_E was measured for a number of devices which were subjected to successive single pulses (t_p = one second). I_C was increased in 0.5A steps until second breakdown (SB) was detected. The data points of Fig. 19 show the largest value of I_C for which SB was not observed during the one second pulse.

It can be seen that the points follow the theory reasonably well for $R_E \lesssim$ 15 milliohms. For larger R_E there is a marked deviation from the theory and increasing R_E results in no improvement in $I_{C,SB}$. It is likely that the simple one-dimensional model used for the calculations is no longer applicable for large R_E and it becomes necessary to consider two-dimensional effects [11].

Curve 716022-A

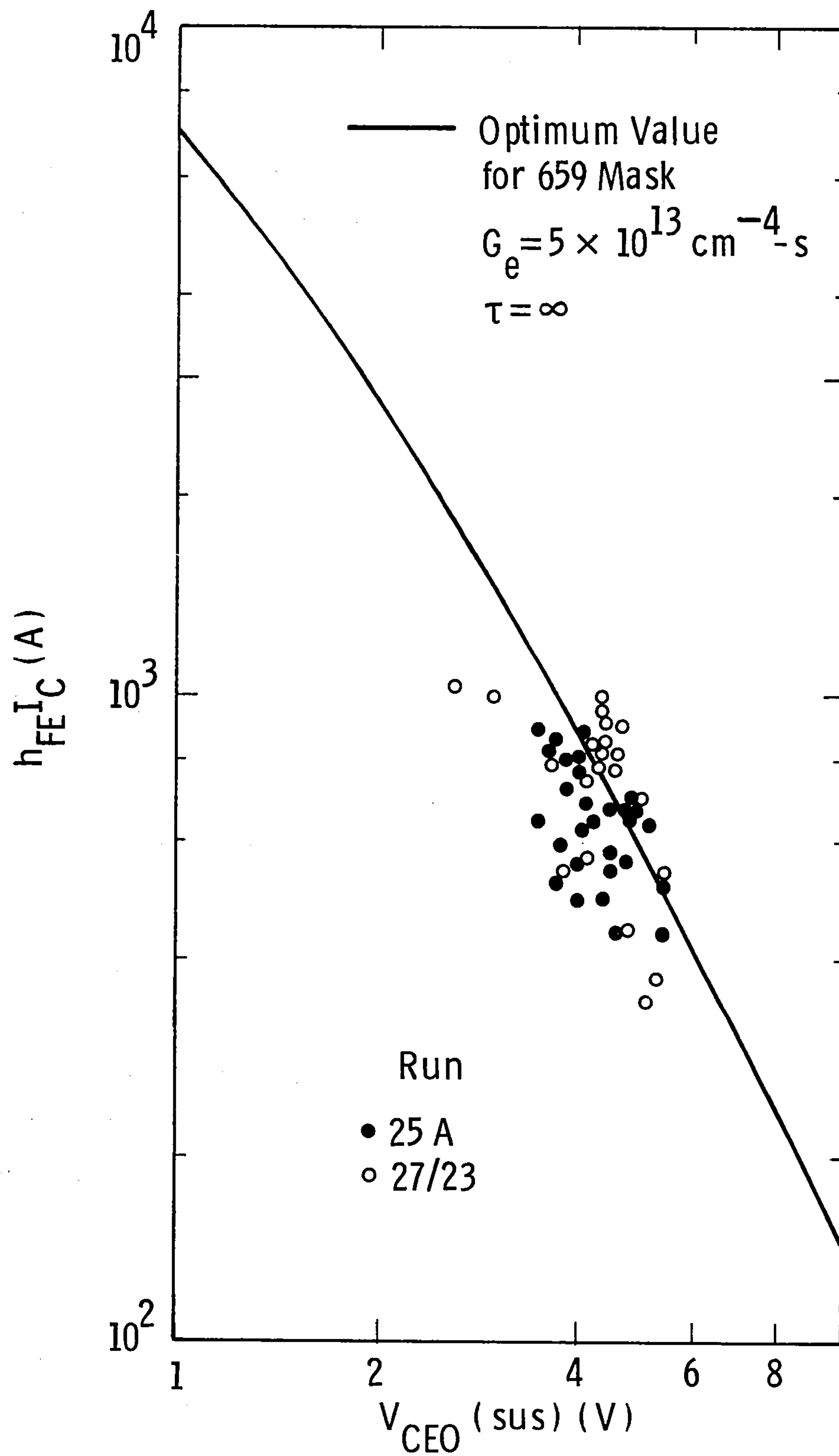


Fig. 18 Measured gain-current product vs. sustaining voltage for devices from three different runs.

Curve 714627-A

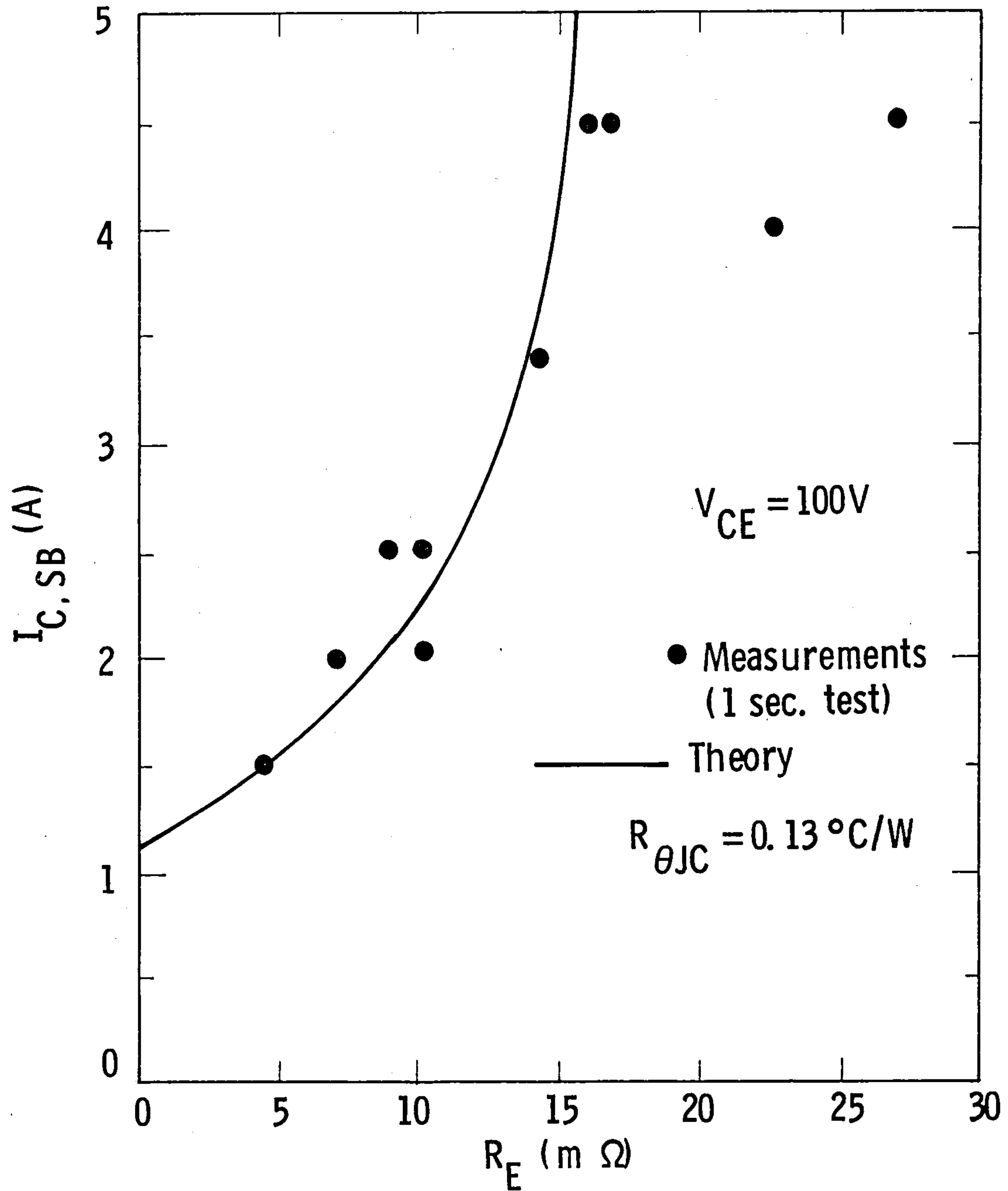


Fig. 19 Second breakdown current vs. emitter ballast resistance. The measured currents are the largest values that pass the test for 0.5A increments.

Figure 20 shows the predicted forward SOA for different pulse times assuming a single pulse of duration t_p. These curves were calculated by using measured transient thermal impedance data together with the criterion that the transistor becomes thermally unstable at a particular junction-to-case temperature. This temperature will be a function of I_C and R_E. Since the transistor must be in the thermally unstable mode for some time before it reaches second breakdown, these predictions will be conservative for short pulse times, e.g., $t_p \lesssim 1$ ms.

5.3 Switching Performance - Resistive Load

Only a limited number of measurements were made under resistive load conditions because this circuit does not adequately reflect operation in most inverter applications. Figure 21 shows turn-on and turn-off waveforms for transistor 18B53. It can be seen that the turn-on waveforms are in qualitative agreement with the predictions of Figs. 6 and 7.

The turn-off waveforms show $t_s \simeq 4.5$ μs (at 0.9 I_C) which is larger than one might expect from Fig. 8. This is probably due to a higher lifetime and h_{FEO} for transistor 18B53 than was used for the calculations of Fig. 8. For example, with the measured h_{FEO} (= 45) and a τ of 35 μs, a storage time of 3.9 μs is predicted. This is reasonably close to the measured value.

5.4 Switching Performance - Inductive Load

A large number of measurements were made using the test circuit of Fig. 22 which simulates the waveforms seen in a typical switching regulator circuit. For these tests a v_{CE} snubber circuit was not used, so that $v_{CE}(t)$ rose very rapidly to the clamp voltage during turn-off, See Fig. 23(a). For this test I_{BF} = 15A, I_{BR} = 8A, V_{CC} = 300V and L = 280 μH. It can be seen that a peak power of 14 KW is reached during turn-off as shown in Fig. 23(b). This represents a "worst-case" situation for the transistor. Peak-powers in excess of 27 KW (90A @ 300V) have been

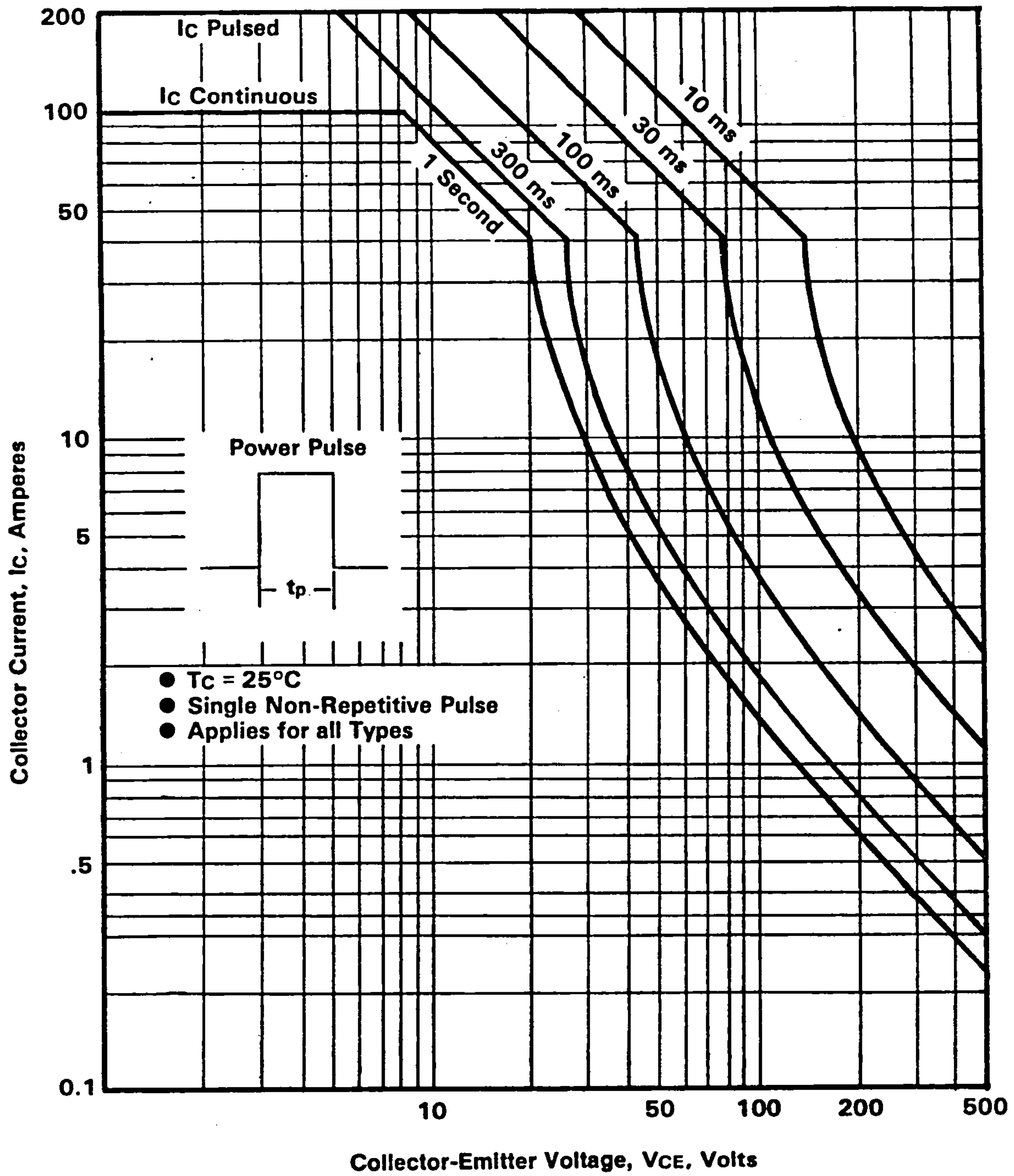


Fig. 20 Forward SOA diagram for different pulse times.

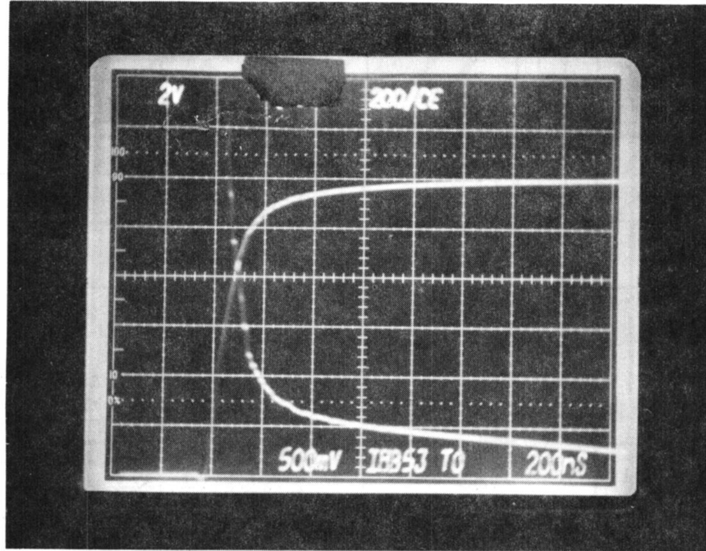


Fig. 21(a). $i_C(t)$ and $v_{CE}(t)$ waveforms for transistor 18B53.
Scales: i_C = 5 A/d, v_{CE} = 20 V/d, t = 0.2 μs/d.
I_{BF} = 6A, V_{CC} = 200V.

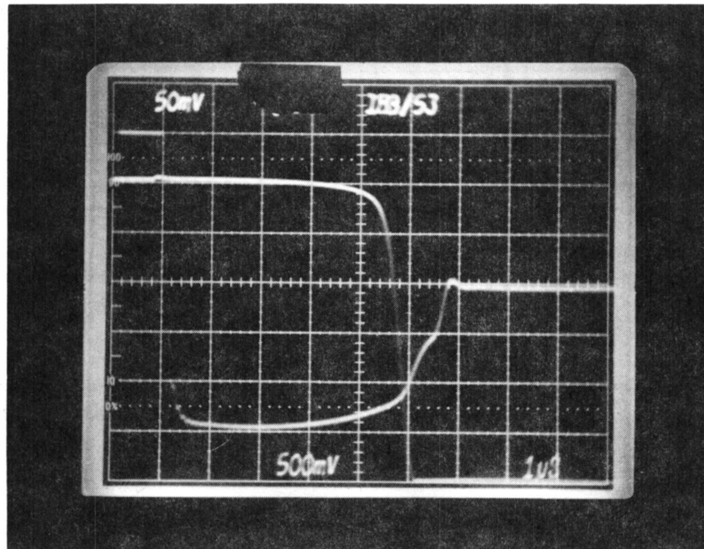


Fig. 21(b). Turn-off waveforms for transistor 18B53.
Scales: i_C = 5 A/d, i_B = 1 A/d,
t = 1 μs/d. I_{BF} = I_{BR} = 3A.

Dwg. 6439A26

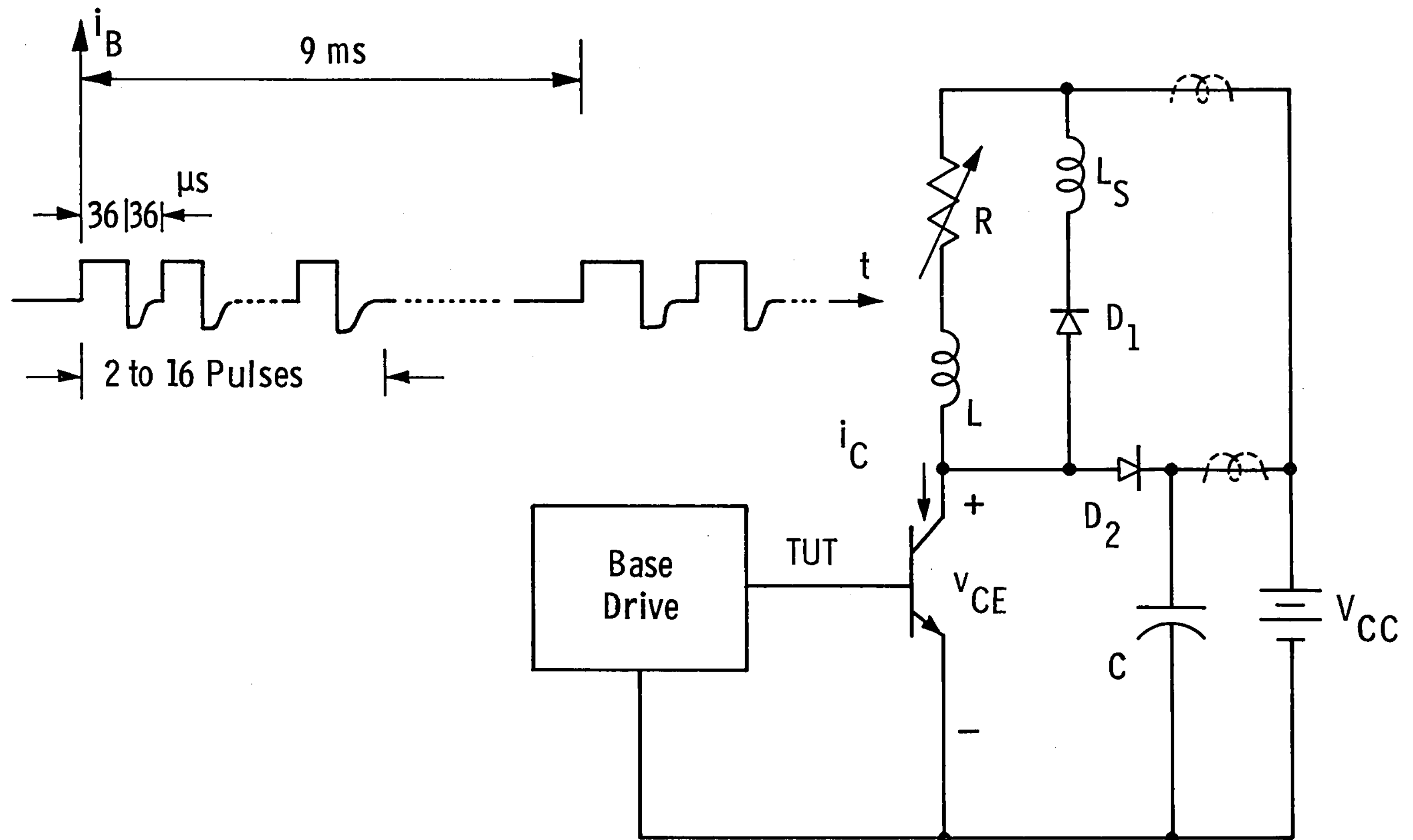
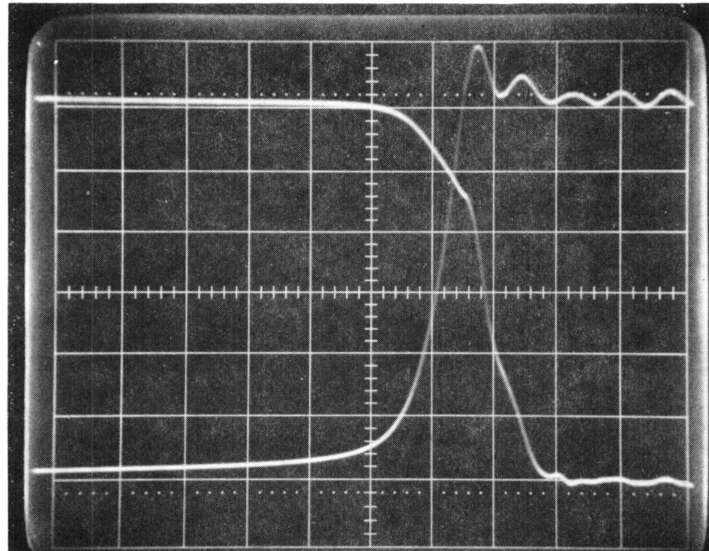
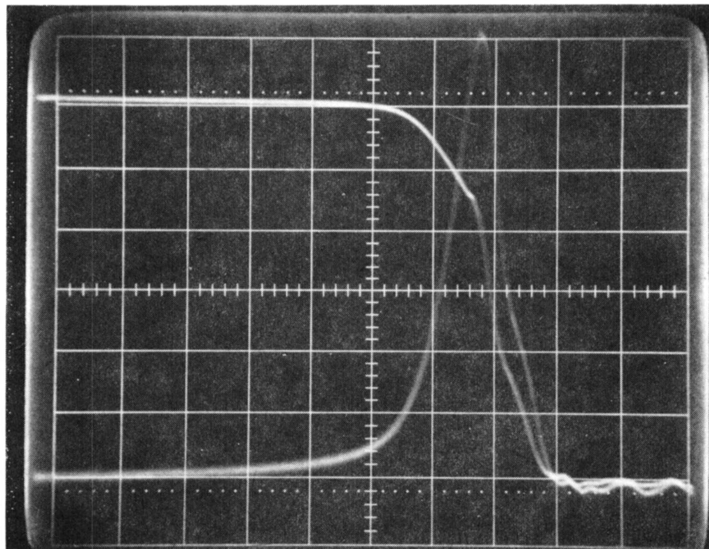


Fig. 22 Test circuit used for switching performance evaluation.



(a)



(b)

Fig. 23. Turn-off waveforms for transistor 22B-92. Scales:
(a) i_C = 10 A/d, v_{CE} = 50 V/d, t = 0.1 μs/d.
(b) i_C = 10 A/d, p = 2 KW/d, t = 0.1 μs/d.
T_c = 23.5°C.

applied during turn-off with no destructive effects; however this topic (which is related to the reverse SOA) requires additional investigation.

5.4.1 Waveform Measurements

Figure 24 shows a block diagram of the measurement set-up used to evaluate the switching performance [8]. The gated integrator integrates the multiplier output of a Philips PM 3252 oscilloscope during the interval of interest, e.g. for the time interval where $p(t) \geq \hat{p}/10$ and $\hat{p}$ is the peak power. (It has been found that no serious error results if an even larger interval of tg = 1 μs is used.)

The integrator output is proportional to a switching energy, E_{ON} or E_{OFF}, corresponding to the turn-on or turn-off intervals. A typical set of data is shown in the waveforms of Fig. 25. For this test, the integrator gave E_{OFF} = 4.03 mJ. Assuming a triangular p(t) waveform during turn-off, the triangle would have a base equal to $2 \times 4.03 \times 10^{-3}/20.8 \times 10^{3} = 0.39$ μs, which agrees well with the p(t) waveform shown. Similar measurements have been made during turn-on [8].

The idea of using E_{ON} and E_{OFF} to describe the switching performance is appealing because it is not necessary to take into account the detailed shape of the $v_{CE}(t)$ and $i_C(t)$ waveforms during the switching interval. This is particularly true for the p(t) waveform during turn-on, which can be rather complex, e.g., see Fig. 26. For this example E_{ON} = 2.65 mJ.

5.4.2 Energy Loss Measurements

E_{ON} and E_{OFF} have been measured for a wide range of conditions on a single transistor that is typical of the recent experimental runs. Perhaps the most important type of data obtained using this method is shown in Fig. 27, which shows E_{OFF} and E_{ON} as a function of case temperature and peak collector current. Because the average power is kept to a small value during the measurement, the junction temperature is approximately equal to the case temperature. With this data and

Dwg. 6439A27

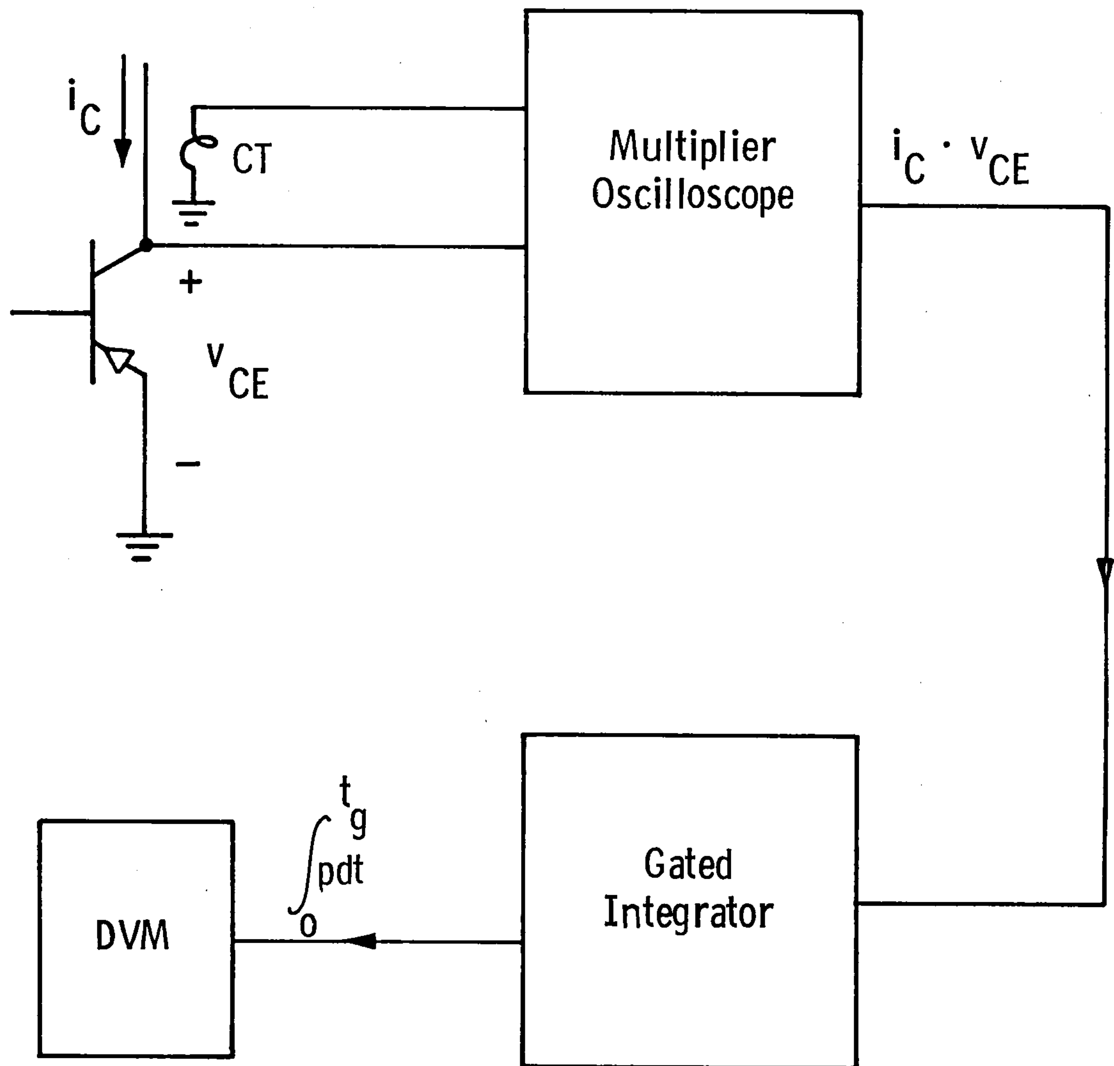
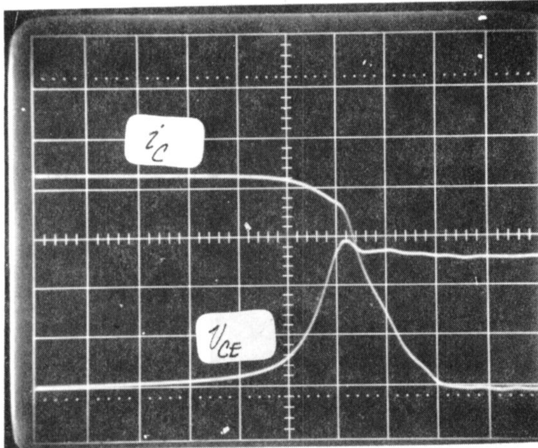


Fig. 24 Block diagram of switching-loss measurement.

Ⓦ Transistor - Test Data - Inductive Switching

Date 12-12-76

Device 22B #106



v_{CE} 100 V/d

i_C 20 A/d

p - W/d

t 0.1 μs/d

T_C = 25 °C

V_{CC} = 250 V

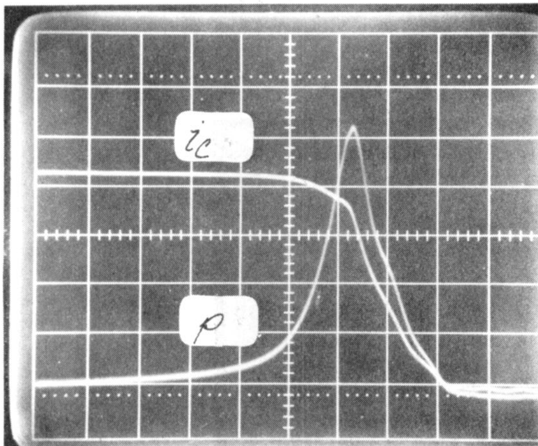
$\hat{i}_C$ = 85 A

I_{B1} = 15 A

I_{B2} = 7 A

L = 280 μH

L_s = 1.5 μH



v_{CE} 200 V/d

i_C 20 A/d

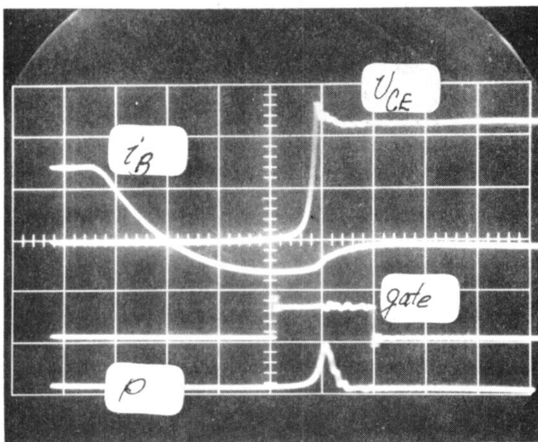
p 4 k W/d

t 0.1 μs/d

V_{int} = 10.08V

SF = 0.5 mJ/V

E_{OFF} = 4.03 mJ



v_{CE} 100 V/d

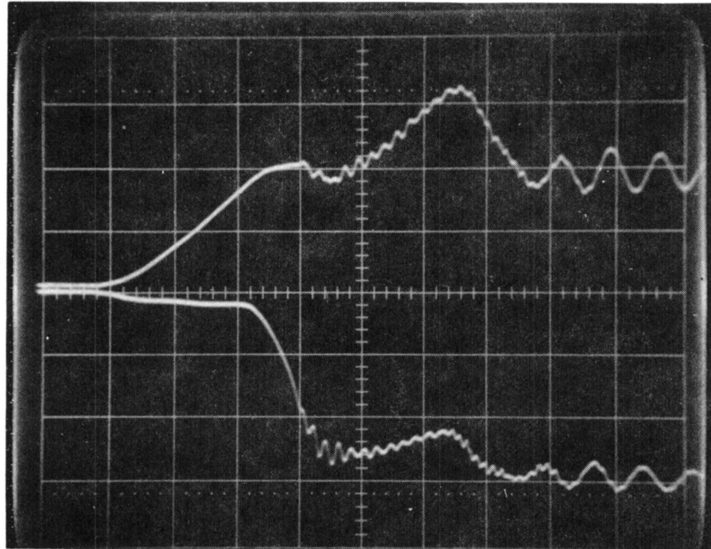
i_B 10 A/d

p 20 k W/d

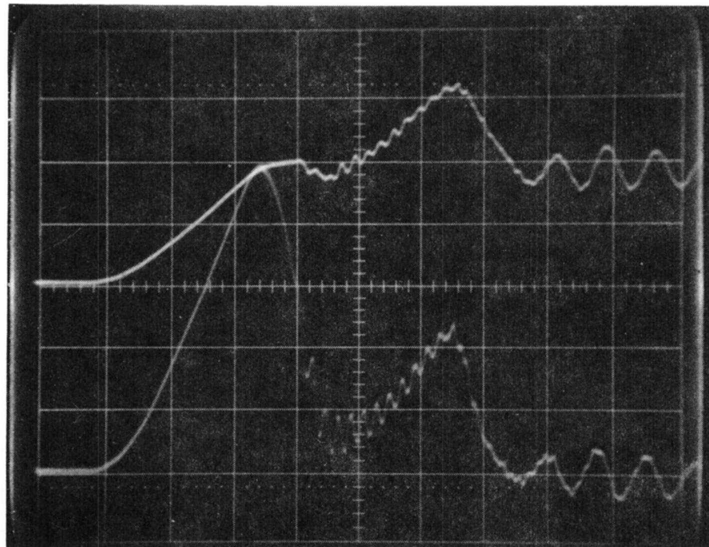
t 0.5 μs/d

t_{sv} = 1.3 μs

Fig. 25. Example of waveforms for the turn-off interval, showing collector-current, collector-emitter voltage, instantaneous power, base current and integrator gating signal.



(a)



(b)

Fig. 26. Turn-on waveforms for device 25A-49. Scales:
(a) i_C = 20A/d, v_{CE} = 100 V/d, t = 0.1 μs/d,
(b) i_C = 20A/d, p = 2 KW/d, t = 0.1 μs/d.
L = 530 μH, $L_s \simeq 0$, V_{CC} = 300V, T_C = 30°C.

Curve 696002-A

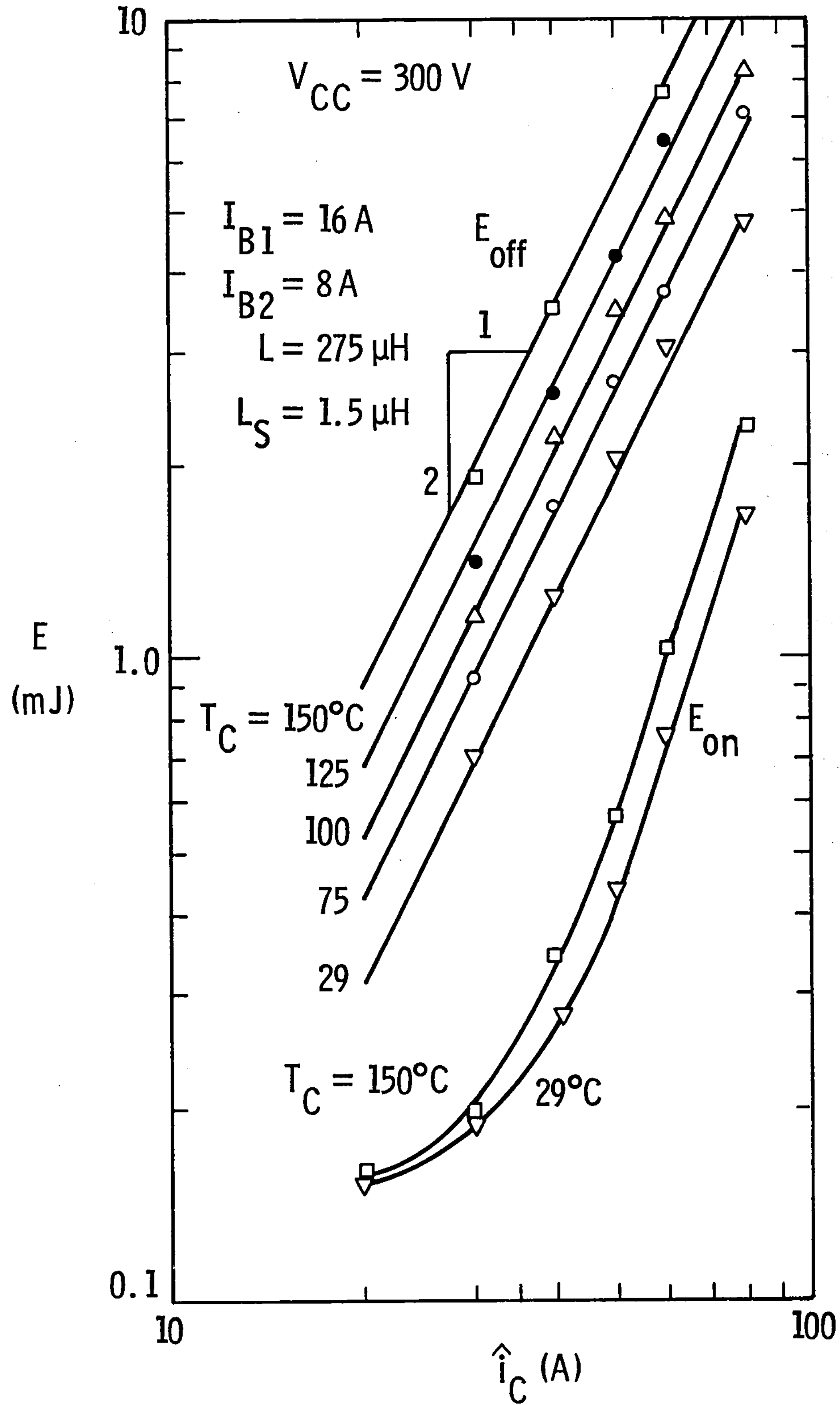


Fig. 27 Measured turn-on and turn-off losses.

knowledge of the intended pulse repetition rate, it is possible to estimate the total switching losses.

For example, for a single periodic pulse of repetition frequency $f(= 1/T)$, with a conduction time t_{cond}, the total power lost in the transistor is

$$P_L = (E_{ON} + E_{OFF})f + P_{ON} \cdot \delta \qquad (6)$$

where $\delta = t_{cond}/T$ and P_{ON} is the steady-state conduction power. P_{ON} can be obtained from the collector characteristic using the I_{BF} of interest. E_{ON}, E_{OFF} and P_{ON} will all be functions of junction temperature T_J. Of these three terms, the most sensitive is E_{OFF}, which increases by approximately 2.5 times as T_J increases from room temperature to 150°C.

Using the data of Fig. 27, together with P_{ON}, which can be obtained from the 576 curve tracer, it is possible to determine whether a particular operating frequency will permit thermally stable operation or not. This determination can be made without subjecting the device to thermal runaway conditions as is demonstrated in Fig. 28.

For this example, P_L is calculated from (6) for two frequencies. Also shown in Fig. 28 is a plot that is determined by the heat flow path from junction to ambient. In some systems the determination of this curve can be rather involved; however, it is usually possible to estimate $T_J - T_A$ as a function of the power dissipated P_D at the junction. As an example, for a junction to case thermal resistance $R_{\theta JC}$ and "heat sink" thermal resistance $R_{\theta CA}$, P_D is given by

$$P_D = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}} \qquad (7)$$

For simple systems where heat flow is due to conduction, $R_{\theta CA}$ will be constant and a straight line plot as shown in Fig. 28 will apply. For convection, forced-air, or liquid cooled systems a more complicated plot may be required.

Curve 715514-A

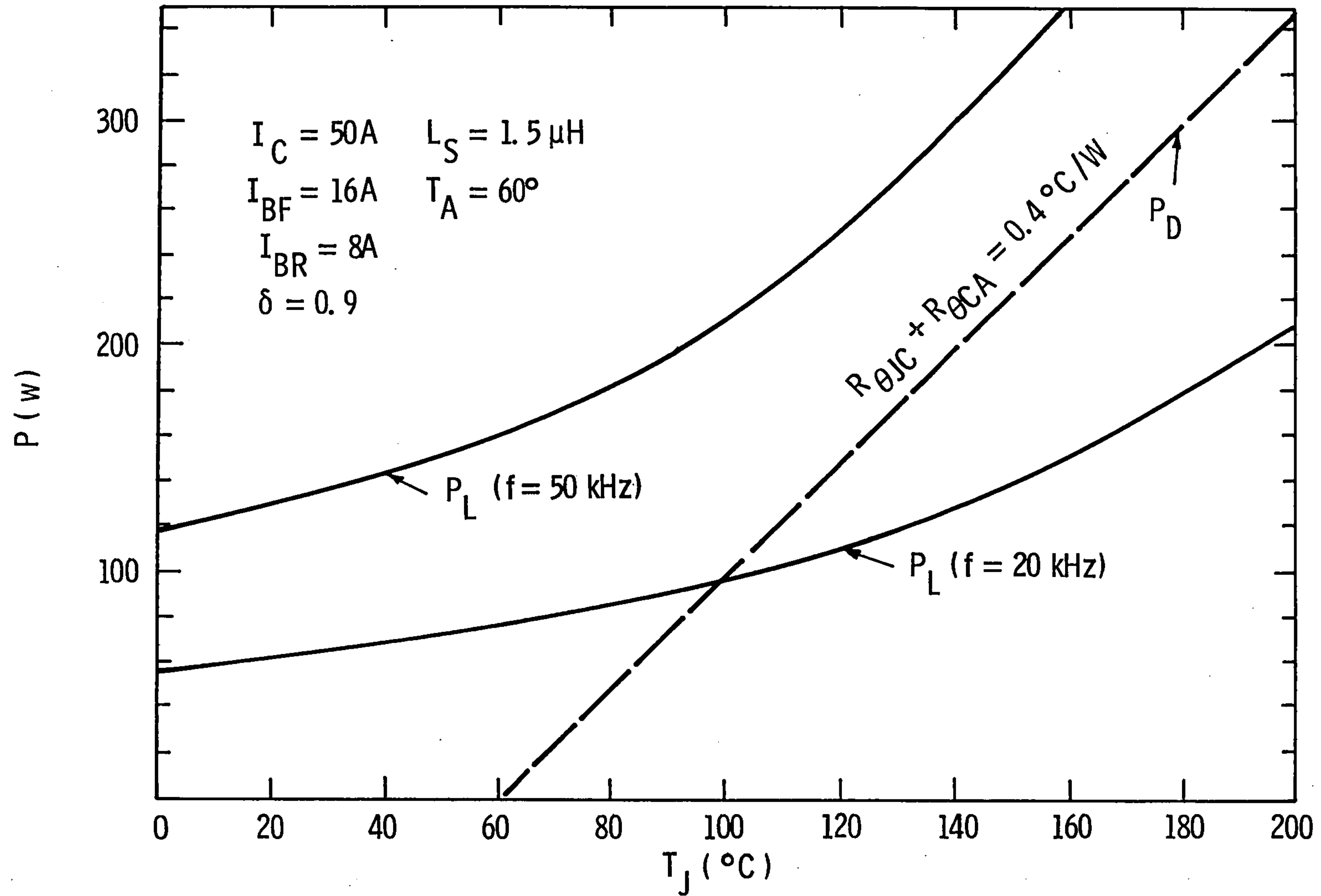


Fig. 28 Total power lost in the transistor (P_L) and dissipated power (P_D) due to the thermal path through the device and heat sink vs. junction temperature. P_L is shown for two frequencies.

By breaking the problem into two parts, one of determining P_L vs. T_J and one of determining P_D vs. T_J, it is possible to predict the steady-state operating conditions. In addition, one can determine what device and circuit conditions will lead to thermal runaway. For example, if $R_{\theta JC} + R_{\theta CA} = 0.4$ °C/W and f = 20 KHz, Fig. 28 shows stable operation at $P_L = P_D = 95W$ and $T_J = 100°C$, for a collector current of 50A. If f is increased to 50 KHz, there is no $P_L = P_D$ solution and an actual system would be thermally unstable. To obtain a steady-state solution at this frequency, T_A must be decreased or $R_{\theta CA}$ decreased.

This idea can be extended further by defining a "maximum safe-operating frequency" SOF, which corresponds to some maximum safe junction temperature, T_{JMAX}. In practice, T_{JMAX} will be somewhat less than the temperature for which increasing junction leakage current leads to transistor thermal runaway.

From (6) the SOF is given by

$$SOF = \left[\frac{T_{JMAX} - T_A}{R_{\theta JC} + R_{\theta CA}} - P_{ON}\,\delta\right] / (E_{ON} + E_{OFF}) \qquad (8)$$

The SOF is plotted vs. the effective heat sink thermal resistance $R_{\theta CA}$ in Fig. 29 for a particular example.

It can be seen that operation in excess of 100 KHz is possible provided $R_{\theta CA}$ and i_C are kept within the appropriate limits. In addition, switching VI products in excess of 24 KVA can be obtained at lower frequencies.

5.5 Reverse SOA

Most "high-voltage" transistors are subject to a failure mechanism (second breakdown) that can occur during turn-off of an inductive load. The region of the I_C, V_{CE} plane within which the failure mechanism can be triggered is termed the Reverse Safe-Operating Area (SOA), a name suggested by the more familiar forward SOA.

Curve 696004-A

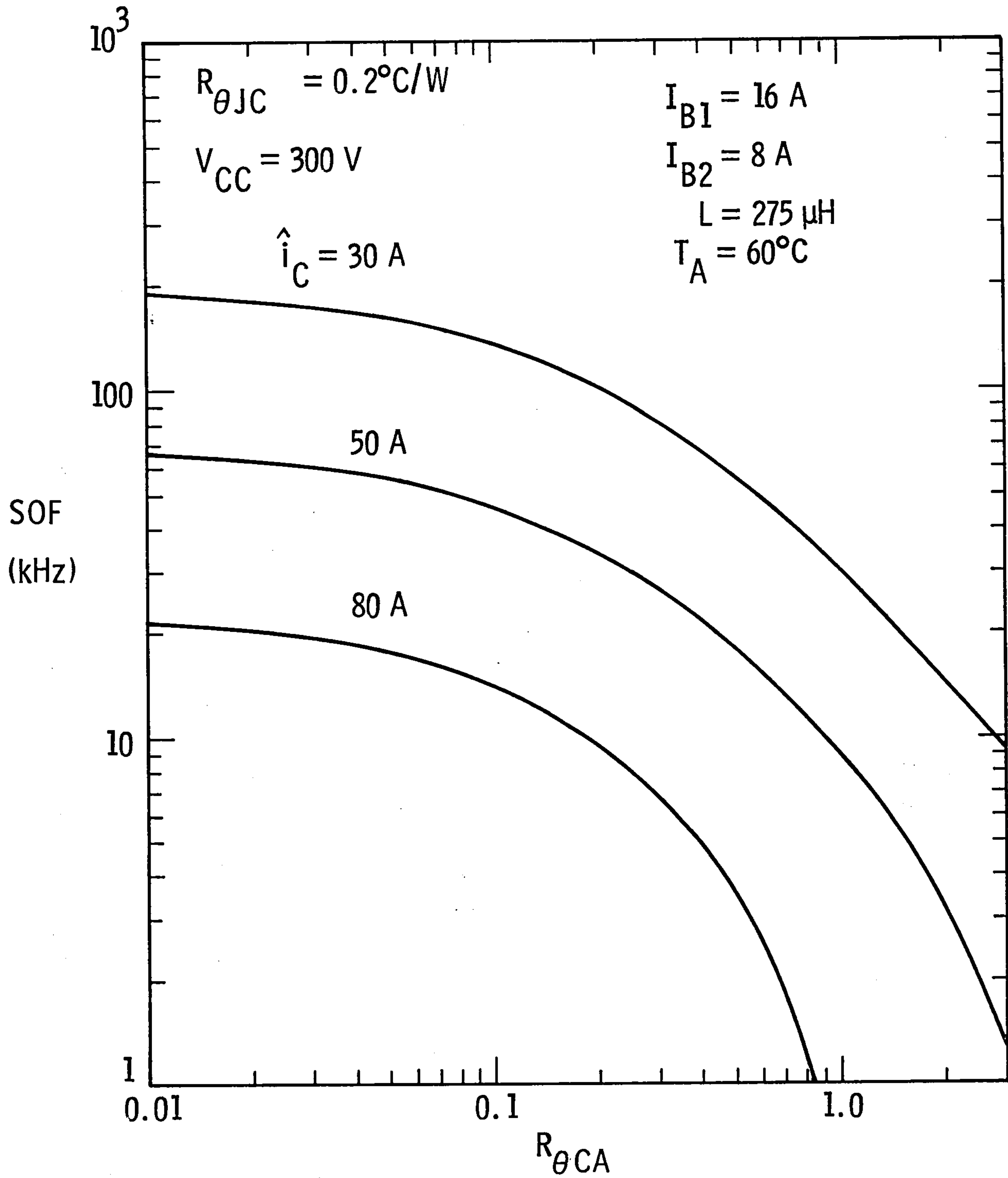


Fig. 29 Safe operating frequency vs. heat sink thermal resistance for different collector currents.

Dwg. 7689A64

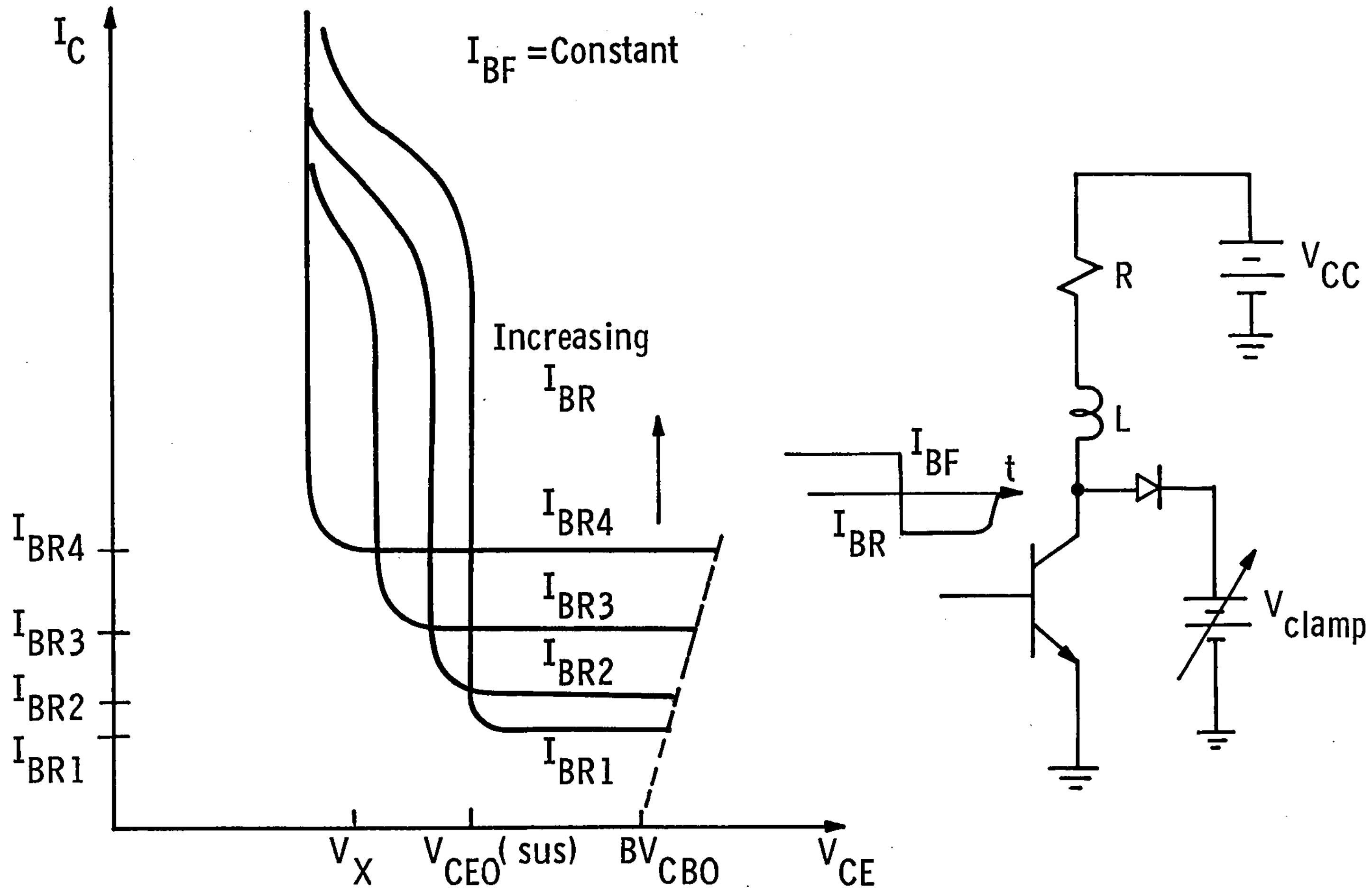


Fig. 30 Reverse Operating Area and Test Circuit.

At present, we have only a limited knowledge of the Reverse SOA for the D60T. An interpretation of some recent work at the National Bureau of Standards [12] suggests that the Reverse SOA will have the general shape shown in Fig. 30, where the curves are drawn for constant I_{BR}, or with V_{BE} clamped to a voltage source (which prevents breakdown of the emitter-base junction).

The details of these curves for the present transistors are still being determined. Experience to date shows that the curves for $I_{BR} \lesssim 10A$ lie to the right of the point $I_C = 80A$, V_x, where $V_x \simeq V_{CEO}$ (sus) - 50V.

6. SCALE-UP STUDY

As noted in the interim report, the methods developed during the present contract period can be extended to even larger devices. As part of the present program, a preliminary design has been worked out for a 33 mm dia. fusion, which is the next larger diameter in production at the Westinghouse Semiconductor Division.

6.1 33 mm Design

For this design a metallurgical emitter area of 3 cm^2 was assumed with an L_E = 15 mils (381 μm), which is the same width used on the present 659 mask. Table 3 gives the predicted electrical performance for this size. The overall current handling capability is expected to increase by more than a factor of two over the present 23 mm design.

It can be seen that a considerably larger base current will also be required. The present base lead is rated at 20A of DC current. The base lead wire can be increased in diameter without much difficulty; however, there is an additional problem related to the voltage distribution along the base metallization pattern. Although transverse current flow through a distributed base resistance is less deleterious than that for an emitter resistance, a non-uniform current distribution will eventually occur as I_C is increased.

6.2 Effect of Base Metallization

The problem has been analyzed in a fashion similar to that of Ref. [2] with the exception that in the present case the resulting differential equations are solved numerically. Figure 31 shows the calculated results for the present 659 mask at a relatively large value

TABLE 3

Predicted Performance for a 33 MM Dia. Fusion

V_{CEO}(sus) (V)	h_{FE} I_C[1] (A)	I_B @ $h_{FE} = 5$ (A)
400	1700	68
600	1200	48

Notes:

(1) $V_{CE} = 2.5V$

Curve 714648-A

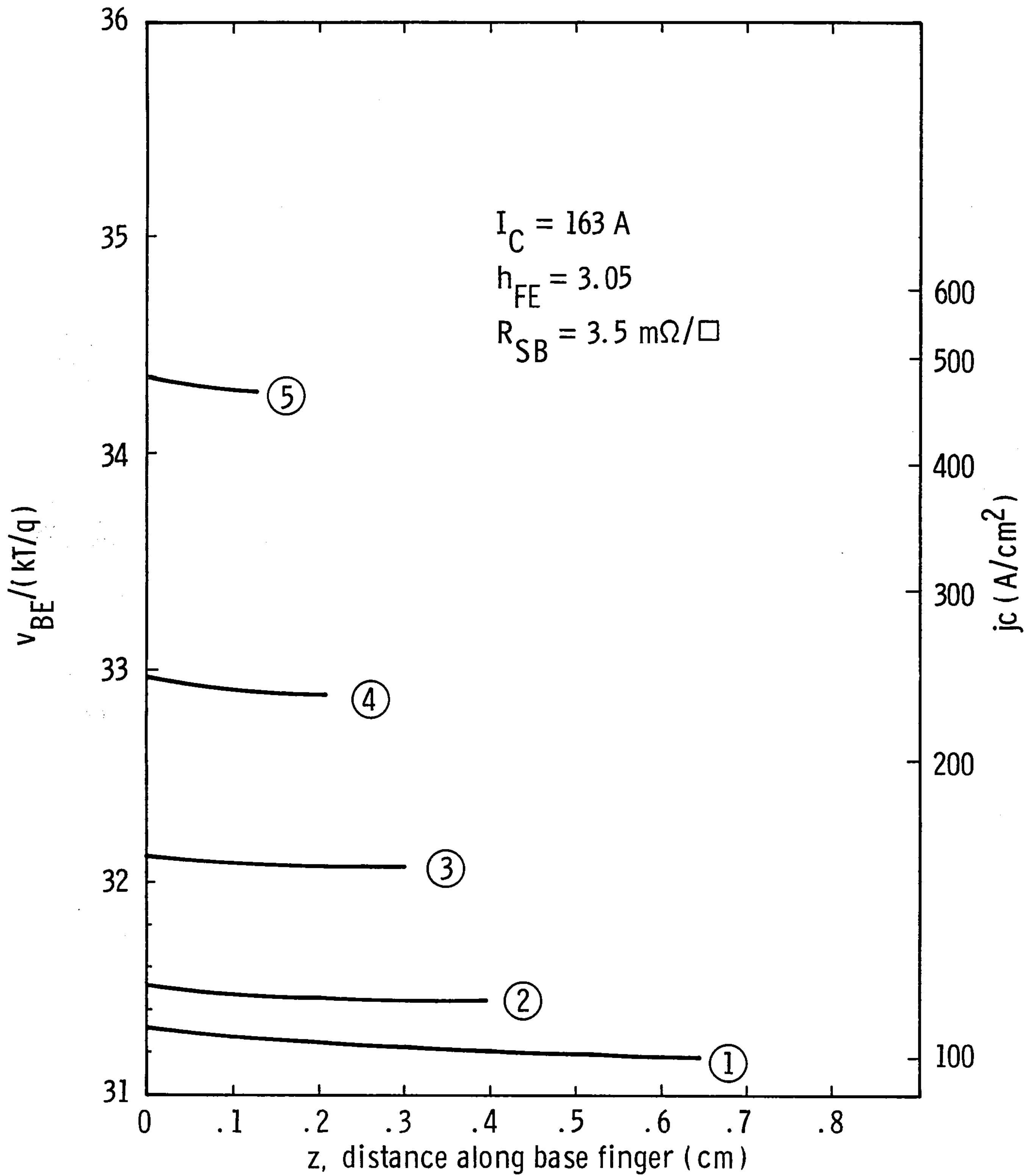


Fig. 31 Base-emitter voltage (normalized to kT/q = 25.6 mV) and current density for the typical sector shown in Fig. 32.

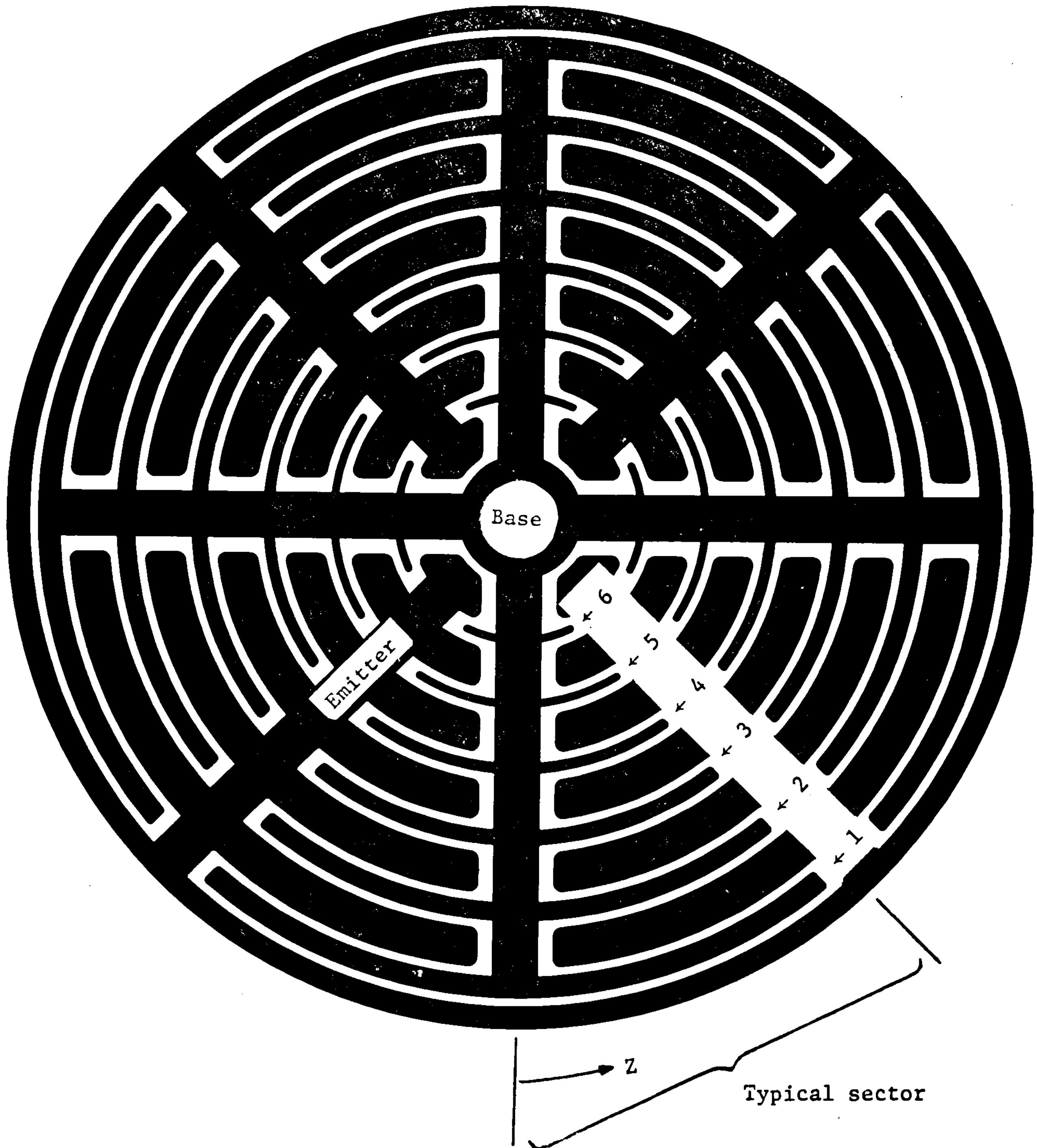


Figure 32. Metallization pattern showing base fingers and radial distance from base trunk centerline.

Curve 714649-A

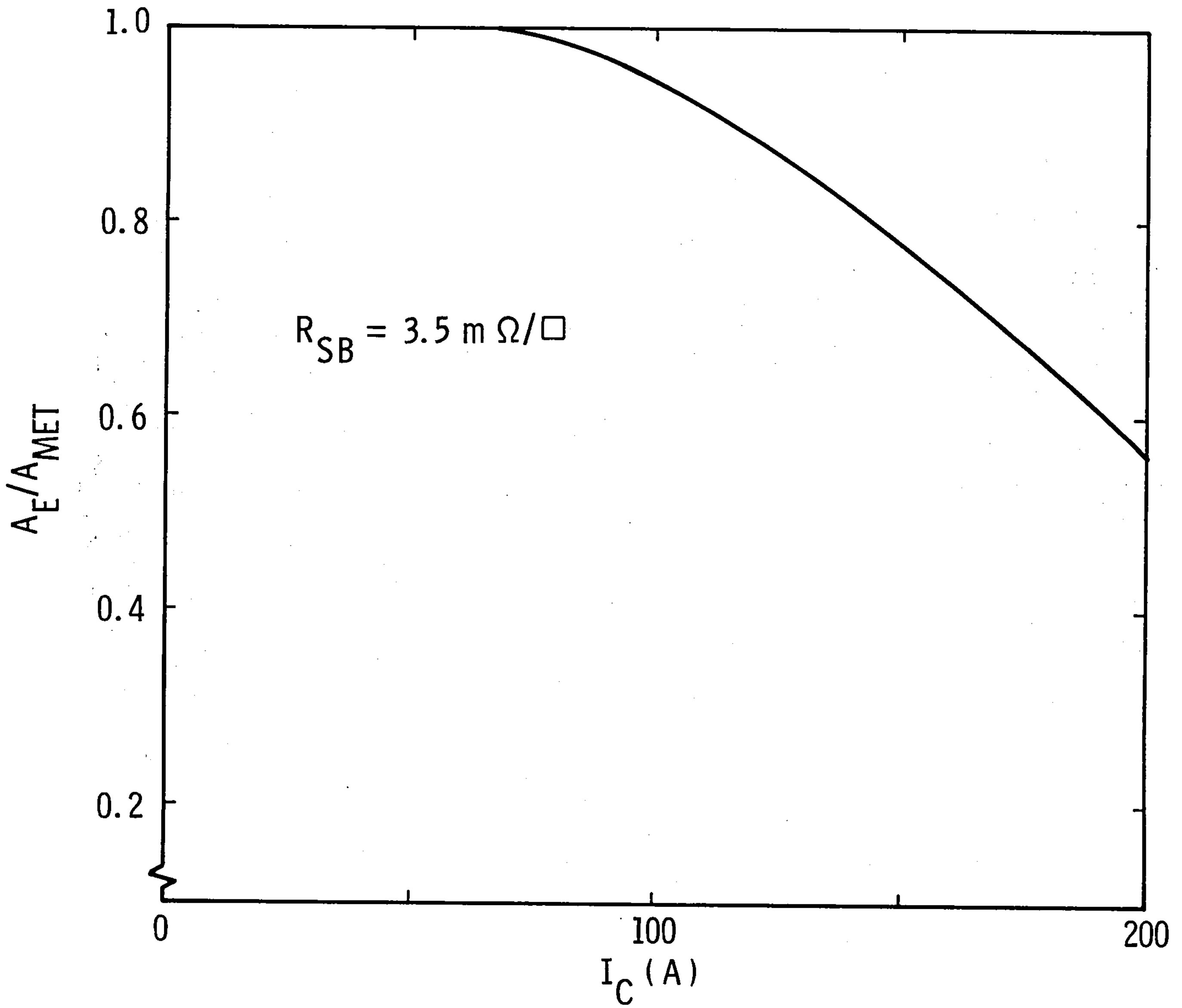


Fig. 33 Fractional reduction in emitter area vs. collector current due to base metallization sheet resistance for the pattern of Fig. 32.

of I_C. Figure 31 is a plot of normalized v_{BE} along each base finger, with the left-hand axis corresponding to the center of the base "bus" or trunk that contacts all fingers. The metallization pattern is labelled in Fig. 32.

It is not too surprising that most of the voltage drop occurs along the trunk and only small voltage differences occur along each finger.

With the present analysis, it is possible to predict the reduction in effective area that will occur with a given pattern and base metallization sheet resistance R_{SB}. An example of this calculation is shown in Fig. 33. This curve does not take into account the problem of emitter current crowding which will cause a further reduction in effective area A_E.

It can be seen that the effects of base metallization begin to be important for $I_C \gtrsim 100A$ for the present design. As the device size is increased, these effects become more serious and it will be desirable to develop methods of improving the base contact to minimize the voltage differences that occur along the base trunk.

7. CONCLUSIONS

The major effort of this program has been the adaptation of present large-area device technology to the fabrication of high-voltage switching transistors. In carrying out this work a number of problems have been solved which deal with the design and fabrication of these transistors.

The work has been successful in the sense that a new transistor (Westinghouse D60T) has been announced which has attracted a great deal of interest from workers in the field of power electronics. The basic design and processing for this device follow closely the results described in this report. (The data sheet for this device is included in Appendix 3.) It is anticipated that the techniques described here will provide a background for future device designs which are larger in area and improved in performance.

8. ACKNOWLEDGEMENTS

The authors acknowledge the technical assistance of D. F. Carnahan, M. N. Sterrett, and G. W. Vomish. The switching evaluation circuit was designed by J. B. Brewster. Assistance with electrical evaluation was given by J. E. Marinchak and R. J. Fiedor. Helpful comments and suggestions were provided by G. R. Sundberg, D. J. Page, and L. R. Lowry.

9. REFERENCES

[1] P. L. Hower, "Optimum design of power transistor switches," IEEE Trans. on Electron Dev., ED-20, pp. 426-435, April 1973.

[2] P. L. Hower and W. G. Einthoven,"Emitter current crowding in high-voltage transistors," IEEE Trans. on Electron Dev., ED-25, pp. 465-471, April 1978.

[3] P. L. Hower and P. K. Govil, "Comparison of one-and two-dimensional models of transistor thermal instability," IEEE Trans. on Electron Dev., ED-21, pp. 617-623, Oct. 1974.

[4] P. L. Hower, "Application of a charge-control model to high-voltage power transistors," IEEE Trans. on Electron Dev., ED-23, pp. 863-870, Aug. 1976.

[5] V.A.K. Temple and M. S. Adler, "The theory and application of a simple etch contour for near ideal breakdown voltage in plane and planar p-n junctions," IEEE Trans. on Electron Dev., ED-23, pp. 950-955, Aug. 1976.

[6] T. W. Kotowski, "High injection region analysis and optimization of power transistors," IEEE Power Elec. Specialists Conf. Record-1977, pp. 27-34.

[7] P. L. Hower and C. K. Chu, "Development fabrication of improved power transistor switches," Contract NAS 3-18916 Interim Report, Report No. NASA CR-135013, National Technical Information Service, Springfield, VA 22151.

[8] P. L. Hower, J. B. Brewster, and M. Morozowich, "A new method of characterizing the switching performance of power transistors," IEEE Ind. App. Soc. Conf. Record-1978 pp. 1044-1049.

[9] R. P. Mertens, H. J. DeMan, and R. J. Van Overstraetan, "Calculation of the emitter efficiency of bipolar transistors," IEEE Trans. on Electron Dev., ED-20, pp. 772-778, Sept. 1973.

[10] B. Kukle and S. L. Miller, "Accurate measurement of emitter and collector series resistances in transistors," Proc. IRE, 45, p. 90, Jan. 1957.

L. J. Giacoletto, "Comments on measurement of emitter and collector series resistances," IEEE Trans. on Electron Dev., ED-19, pp. 692-693, July 1972; ibid., p. 1224, Nov. 1972.

[11] G. Bosch, "Anomalous current distributions in power transistors," Solid-State Elec., 20 pp. 635-640, July 1977.

[12] D. L. Blackburn and D. W. Berning, "Some effects of base current on transistor switching and reverse-bias second breakdown," IEEE Int. Electron Dev. Mtg. Technical Digest-1978, pp. 671-675.

10. APPENDICES

Appendix 1	Data
Appendix 2	Data
Appendix 3	Papers
Appendix 4	Westinghouse D60T Data Sheet

APPENDIX 1

TEST DATA ON TRANSISTORS FABRICATED DURING FIRST PERIOD OF THE CONTRACT

The initial design goals are given in Tables 4 and 5. It was determined early in the contract period that an emitter area of at least 0.5 cm^2 was required to simultaneously meet specifications (1) and (5). A fairly coarse geometry mask was designed (mask 565) and 50 devices were tested and delivered to NASA. These devices were originally intended for an ion-engine space craft application which required V_{CEO} (sus) $\geq$ 600V.

Table 6 lists measured data on these devices. The averaged results are:

Specification Number	V_{CE}(sat) (5)	V_{CE}(sat) (6)	V_{CE}(sus) (1)
Average of 50 devices	0.66V	0.55V	680V
Desired	$\leq$0.4	$\leq$0.8	$\geq$600

As a confirmation of the design theory, a number of the devices did simultaneously meet all three requirements; however, on the average V_{CE}(sat) at 5A was about 50 percent larger than the goal. The main reason for this increase is that the collector width on most of the devices is thicker than the optimum value.

Table 4 — Dc Characteristics*

Symbol	Specification Number	Description	Value
$BV_{CEO}(sus)$	(1)	Minimum collector-emitter sustaining voltage, base open	600 V at 100 mA
$BV_{CER}(sus)$	(2)	Minimum collector-emitter sustaining voltage, R_{BE} = 47 ohm	800 V at 100 mA
BV_{EBO}	(3)	Minimum emitter-base breakdown voltage, collector open	8 V at 1 mA
I_{CER}	(4)	Maximum collector-emitter leakage current, R_{BE} = 47 ohm	0.1 mA at 600 V
$V_{CE}(sat)$	(5)	Maximum collector-emitter saturation voltage at I_C = 5 A, I_B = 0.25 A	0.4 V
$V_{CE}(sat)$	(6)	Maximum collector-emitter saturation voltage at I_C = 10 A, I_B = 1 A	0.8 V
$V_{BE}(sat)$	(7)	Maximum emitter-base saturation voltage at I_C = 5 A, I_B = 0.25 A	1.0 V
h_{FE}	(8)	Minimum dc forward current transfer ratio at I_C = 10 A, V_{CE} = 5 V	10
$I_{C, max}$	(9)	Dc collector current absolute maximum rating	15 A

*Proposed at beginning of contract.

Table 5 — Switching Times

Symbol	Specification Number	Description	RFP Value	Proposed Value	Units
t_r	(10)	Maximum collector current rise time*	0.1	0.15	μs
t_f	(11)	Maximum collector current fall time*	0.1	0.12	μs
t_s	(12)	Maximum collector storage time*	0.5	0.7	μs

*Resistive load with $I_C = 5$ A, $I_{B1} = I_{B2} = 1$ A.

Table 6 Test Data on Sample Devices

Characteristic			$V_{CE}(sat)$		$V_{CE}(sat)$	V_{CEO} at	I_{CEO}	h_{FE}	V_{EBO} at	I_{EBO}	$V_{CEO}(sus)$	$V_{CER}(sus)$ R_{BE} = 47 ohm	L
		Units	(V)	pack-age	(V)	(V)	(mA)	(--)	(V)	(mA)			(mH)
see note			1		2	3	3	4	5	5	6	6	6
Dev.#	Run#	Mask											
63	12A	SF	0.40	D	0.30	400	0.1	65	<1	1	700/40	--	1000
65	12A	SF	0.49	D	0.42	600	0.01	46	<1	1	850	870	1000
79	12B	SF	0.52	D	0.31	600	<0.5µA	50	<1	1	970/60	--	1000
81	12B	SF	0.70	D	0.45	600	0.002	50	<1	1	1000/20	1050/20	1000
83	12A	SF	0.53	D	0.36	600	0.002	54	<1	1	840/60	--	1000
89	12A	SF	0.45	D	0.33	525	0.1	50	<1	1	1000/50	--	1000
90	12A	SF	0.90	D	0.31	22	0.1	39	<1	1	1050/60	--	1000
95	12A	SF	0.74	D	0.41	1.2	0.1	41	<1	1	1000/60	--	1000
99	12B	SF	0.34	D	0.29	20	0.1	80	<1	1	800/20	--	1000
105	12A	565	0.69	S	0.50	480	0.1	46	8	0.5	540	680	1000
109	12A	SF	0.39	S	0.19	600	0.003	63	<1	1	1100/40	1100/40	1000
110	12B	SF	0.27	S	0.15	520	0.1	56	<1	1	870/80	870/80	1000
111	12B	SF	0.97	S	0.90	580	0.1	51	<1	1	920/40	950/40	1000
114	12A	565	>2.0	S	>2.0	425	0.1	17	8	0.01	620	750	1000
116	12B	SF	0.22	S	0.53	220	0.1	47	<1	1	700	750	20
117	12A	SF	0.72	S	0.50	600	0.002	47	<1	1	600	600	20
118	12B	SF	1.01	S	1.01	475	0.1	27	<1	1	570	580	20
119	12B	SF	0.78	S	0.85	600	1.5µA	31	<1	1	560	520 ?	20
121	12A	SF	0.53	S	0.25	550	0.1	49	<1	1	650	680	20
126	12B	565	0.59	S	0.46	420	0.1	50	8	0.2	530	640	20
128	12A	565	0.45	S	0.29	600	<0.5µA	50	8	0.5	550	675	20
129	12B	565	1.14	S	1.20	600	1 µA	32	7.5	1	580	760	20
130	12A	565	0.66	S	0.50	600	1.3µA	54	8	0.01	525	600	20
132	12A	565	0.25	S	0.23	560	0.1	56	8	2µA	525	625	20
133	12A	565	0.65	S	0.36	530	0.1	34	8	0.1	650	775	20

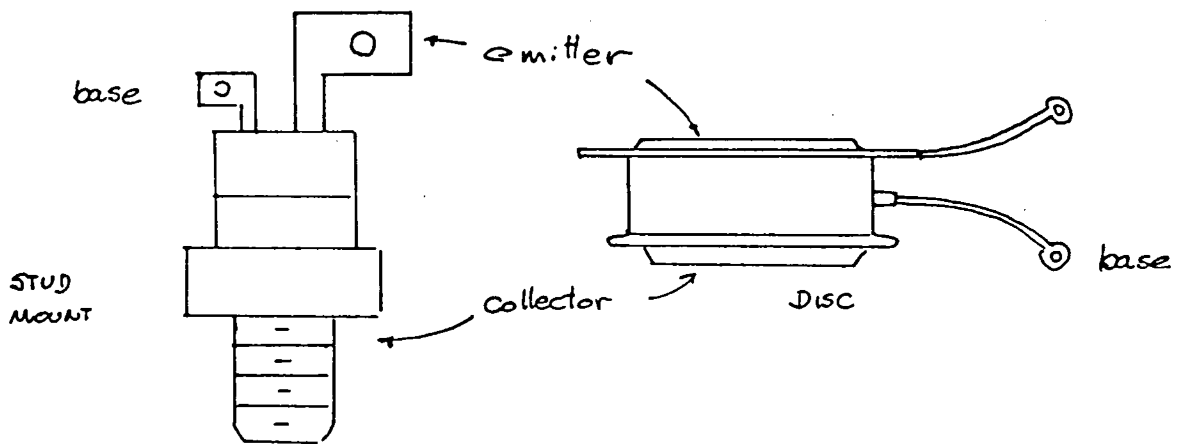
Table 6 (cont.)

Characteristic / Units	$V_{CE}(sat)$ (V)	package	$V_{CE}(sat)$ (V)		V_{CEO} at (V)	I_{CEO} (mA)		h_{FE} (--)		V_{EBO} at (V)	I_{EBO} (mA)	$V_{CEO}(sus)$	$V_{CER}(sus)$ R_{BE} = 47 ohm	L (mH)
see note	1		2		3	3		4		5	5	6	6	6
Dev.# Run# Mask														
134 12B 565	0.47	S	0.37		425	0.1		54		4	1	530	600	20
137 12A 565	0.66	S	0.46		600	< 1μA		48		8	0.1	500	625	20
138 12B 565	1.60	S	1.90		575	0.1		23		6.7	1	560	725	20
139 12B 565	0.92	S	0.88		335	0.1		40		3.5	1	515	650	20
140 12A1 565	0.30	S	0.44		500	0.1		50		<1	1	560	590	20
142 12A 565	0.90	S	0.80		260	0.1		27		7.5	1	500	650	20
144 12A 565	0.55	S	0.35		400	0.1		44		[illegible]	0.1	540	610	20
145 12B 565	0.91	S	0.74		350	0.1		43		<1	1	600	660	20
147 12A1 565	0.34	S	0.39		600	<0.5μA		51		8	8μA	520	660	20
150 12B SF	0.53	S	0.23		600	0.5μA		54		<1	1	600	610	20
152 12A SF	0.67	S	0.41		330	0.1		51		< 1	1	600	600	1000
155 12B SF	0.42	S	0.19		450	0.1		48		< 1	1	700	725	20
156 10 565	0.21	S	0.27		600	0.02		32		8	0.2	800	1000	1000
164 12A SF	0.42	S	0.19		8.5	0.1		59		< 1	1	640	650	20
165 12B 565	1.75	S	>2.0		600	3μA		24		1.5	1	580	725	20
172 12A 565	0.61	S	0.36		50	0.1		36		1.5	1	580	780	20
182 12B 565	0.72	S	0.52		400	0.1		44		7.5	1	500	620	20
188 12A 565	0.65	S	0.35		140	0.1		35		5.5	1	500	610	20
194 12A 565	0.33	S	0.26		250	0.1		44		8	0.02	600	850	20
195 12A1 565	0.45	S	0.58		600	0.02		38		< 1	1	525	540	20
200 11B SF	0.72	S	0.24		22	0.1		32		< 1	1	610	630	20
202 12B 565	0.26	S	0.23		600	1 μA		57		2.5	1	525	650	20
203 12A 565	0.32	S	0.25		600	1 μA		45		8	0.2	625	750	20
208 12A SF	0.24	S	0.15		400	0.1		71		< 1	1	525	550	20
210 12A SF	1.04	S	0.87		60	0.1		39		< 1	1	550	625	20

Table 6 (cont.)

Characteristic			$V_{CE}(sat)$		$V_{CE}(sat)$		V_{CEO} at	I_{CEO}		h_{FE}		V_{EBO} at	I_{EBO}	$V_{CEO}(sus)$	$V_{CER}(sus)$ R_{BE} = 47 ohm	L
Units			(V)	package	(V)		(V)	(mA)		(--)		(V)	(mA)			(mH)
see note			1		2		3	3		4		5	5	6	6	6
Dev.#	Run#	Mask														
214	12A	SF	1.62	S	1.70		2.5	0.1		29		1	1	675	700	20
84	12B	SF	1.03	D	0.85		600	0.014		38		1	1	1175/40	--	1000
85	12A	SF	0.31	D	0.26		520	0.1		62		1	1	925/40	--	1000
86	12A	SF	0.45	D	0.31		600	0.003		60		1	1	1050/40	--	1000

Table 6 (cont.)



Notes

	Test	Conditions	Equipment Used
(1)	V_{CE}(sat)	I_C = 5A, I_B = 0.25A	Tektronix 576, 300μsec pulsed
(2)	V_{CE}(sat)	I_C = 10A, I_B = 1.0A	" " "
(3)	V_{CEO}, I_{CEO}	*	Tektronix 576, full-wave rectified, 60Hz

*I_{CEO} @ V_{CEO} = 600V or V_{CEO} @ I_{CEO} = 0.1mA, whichever occurs first as voltage is increased.

	Test	Conditions	Equipment Used
(4)	h_{FE}	I_C = 10A, V_{CE} = 5V	Tektronix 576, 300μsec pulsed
(5)	V_{EBO}, I_{EBO}	**	Tektronix 576, full-wave rectified, 60Hz

**I_{EBO} @ V_{EBO} = 8V or V_{EBO} @ I_{EBO} = 1mA, whichever occurs first as voltage is increased.

	Test	Conditions	Equipment Used
(6)	*** V_{CEO}(sus), V_{CER}(sus)	I_C = 100mA, except where noted by use of a slash, e.g., 950/40 means the voltage was measured at 40mA	(W) Semiconductor Division inductive test set. L = 20mH or 1000mH as noted.

***This test was initiated using L = 1000mH; however, destructive oscillations were sometimes observed with this inductance and L was reduced to 20mH for the remainder of the test.

APPENDIX 2

TEST DATA ON TRANSISTORS FABRICATED DURING THE FINAL PERIOD ON THE CONTRACT

Data is given in Table 7 for 25 devices which were delivered to NASA at the completion of the contract. The design used for these transistors is given in the text. Switching measurements were made using the circuit of Fig. 22.

TABLE 7 - TEST DATA

	Parameter	$V_{CEO}(su)$	$h_{FE}(I_C) \mid V_{CE} = 2.5V$			$G = h_{FE} I_C$ @60A	E_{OFF}	t_{sv}	h_{FEO}	$I_{EBO} \mid V_{BE} = 7V$	R_{BE}	E_{ON}
	Units	(V)	I_C = 40A	50A	60A	(A)	(mJ)	(μs)	(-)	(mA)	(Ω)	(mJ)
Device No.	See Note:	(1)					(2)	(2)	(3)	(4)	(4)	(2)
27/23 - 1		529	7.5	6.8	6.25	375	2.6	2.6	12	--	278	
2		444	20.0	17.2	14.3	857	3.36	3.7	31	.003		
4		406	12.5	10.8	9.4	563	3.12	3.1	20	.002		
6		464	21.0	17.9	15	900	3.68	4.0	40	--	71	0.75
15		487	14.8	11.9	9.8	590	4.32	3.5	30	.759		
20		435	25.0	20.0	16.2	973	3.08	4.0	43	--	283	
23		437	23.5	19.2	15.8	947	3.39	3.7	29	.002		
24		458	19.0	15.6	13.0	783	3.57	3.4	36	6.95		
29		433	21.0	16.7	13.6	818	3.4	3.5	39	16.4		
45		416	17.0	14.3	12.5	750	2.59	3.7	28	--	177	
48		459	20.0	16.1	13.6	818			36	.001		
49		442	22.0	18.5	15.0	900			39	1.30		
56		426	21.0	16.7	13.6	818			36	1.61		
72		384	11.0	10.0	9.1	545			16	--	59	
79		471	12.5	10.2	8.9	537			22	66		
22B - 90		377	19	14.3	11.5	692	2.34	1.5	39	--	324	
92		382	17.4	13.2	10.7	643	1.71	1.6	38	--	300	
93		384	20.0	14.7	12.2	735	2.88	2.2	41	1.05		
96		392	14.3	10.9	9.2	554			38		93	
98		388	20.0	15.2	12.0	720			52	16.3		
102		370	21.1	16.1	13.3	800	2.67	2.0	46	2.27		
103		411	19.0	13.9	11.3	679			42		125	
107		446	22.0	16.1	13.0	800	3.20	2.5	49		70	0.75
108		393	20.0	15.6	13.0	783			39	1.68		
25B - 2		460	11.8	10.0	8.55	513			24	1.0		

Notes: (1) V_{CEO}(sus) measured using inductive turn-off (L = 25 mH) with base open at I_C = 200 mA.

(2) E_{OFF} is energy in turn-off pulse for collector current of 60A, clamp-voltage of 300V. I_{BF} = 15A, I_{BR} = 8A, load inductance = 280 μH.

(3) h_{FEO} is peak current gain, V_{CE} = 5V.

(4) For I_{EBO} > 20 mA @ 7V, emitter leakage current was usually proportional to V_{EB}, in this case R_{BE} gives effective resistance, emitter-to-base.

APPENDIX 3

PAPERS PUBLISHED UNDER THIS CONTRACT

P. L. Hower, "Power Transistor Performance Tradeoffs," 1975 IEEE Power Electronics Specialists Conference Record, pp. 217-223, Los Angeles, June, 1975.

P. L. Hower and C. K. Chu, "Design and Performance of Large-Area Power Transistors," 1975 IEEE Industry Applications Society Conference Record, pp. 459-463, Atlanta, October 1975.

P. L. Hower, "Application of a Charge-Control Model to High-Voltage Power Transistors," IEEE Trans. on Electron Dev., ED-23, pp. 863-870, August 1966.

P. L. Hower, J. B. Brewster, and M. Morozowich, "A New Method of Characterizing the Switching Performance of Power Transistors," IEEE Ind. App. Soc. Conf. Record-1978 pp. 1044-1049.

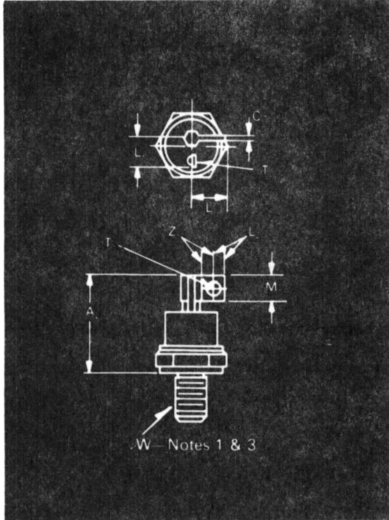
P. L. Hower and W. G. Einthoven, "Emitter Current Crowding in High-Voltage Transistors," IEEE Trans. on Electron Dev., ED-25, pp. 465-471, April 1978.

WESTINGHOUSE D60T DATA SHEET

NPN Power Switching TRANSISTORS D60T/D62T

200 Amperes
400—500 Volts

October 1978

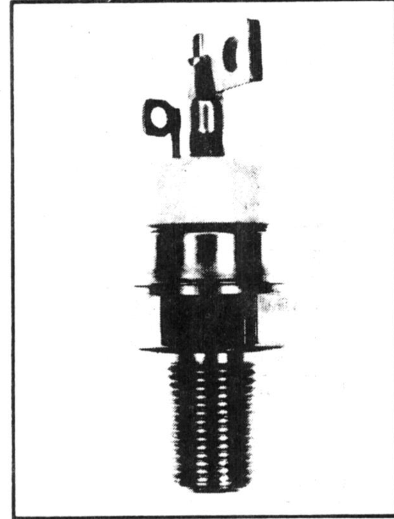


D60 Outline

Symbol	Inches Min.	Inches Max.	Millimeters Min.	Millimeters Max.
A_2		2.500		63.50
C	.110	.140	2.79	3.55
L		.812		20.62
L_1	.500	.600	12.70	15.24
L_2	.250		6.35	
M_1	.350	.450	8.88	11.42
ϕT_1	.200	.240	5.08	6.09
ϕT_2	.145	.160	3.68	4.06
Z_1	.350		8.88	
ϕW	¾-16 UNF-2A			

Creep & Strike Distance.
D60T - .690 in. min. (17.60 mm).
(In accordance with NEMA standards.)
Finish—Nickel Plate.
Approx. Weight—8 oz. (227 g).

1. Complete threads to extend to within 2½ threads of seating plane.
2. Angular orientation of terminals is undefined.
3. Pitch diameter of 3/4-16 UNF-2A (COATED) threads (ASA B1.1-1960)



Maximum Ratings
Collector Current (peak): 200 Amperes
Collector Current (continuous): 100 Amperes
Base Current (continuous): 20 Amperes
Power Dissipation: 625 Watts at Tc = 75°C
Operating and Storage Temperature: -50°C to +200°C

Applications
- High Frequency Inverters
- Motor Controls
- Switching Regulators
- VLF Transmitters

Features
- Triple Diffused Design
- CBE Construction
- 625 Watt Power Capability

Ordering Information

Type	Voltage Rating (Volts)	Current Rating — Amperes 40	50	60	Gain
D60T (Stud) D62T* (Disc)	400	4040	4050	4060	10
	450	4540	4550		10
	500	5040			10

Example: Select the complete ten digit device part number you desire from the shaded area in the table above — i.e. a D60T454010 describes a stud mount transistor rated at 4.50 volts, 40 amperes, and a gain of 10 at rated current (40 amperes).

***Note: Disc package (D62T), consult factory.**

DEVELOPMENTAL PRODUCT

These devices are developmental types intended for engineering evaluation Specifications and data are subject to change without prior notice. Westinghouse assumes no obligation for notice of change or future manufacture of these products.

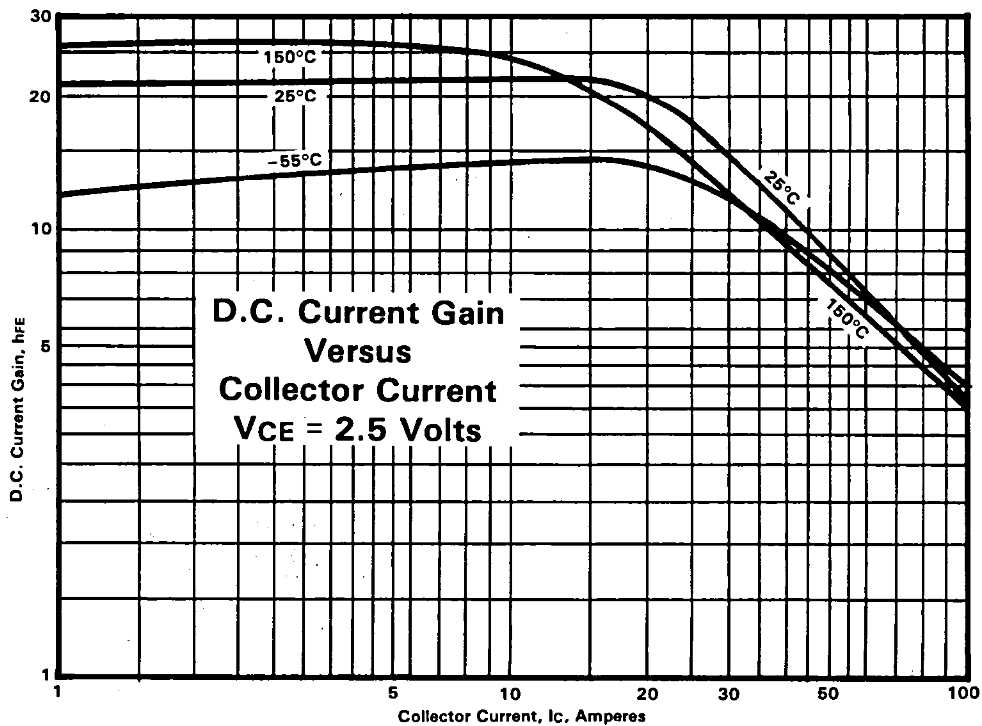
TRANSISTOR

200 Amperes
400—500 Volts

NPN Power Switching TRANSISTORS D60T/D62T

Electrical Characteristics (TCASE = 25°C unless otherwise specified)

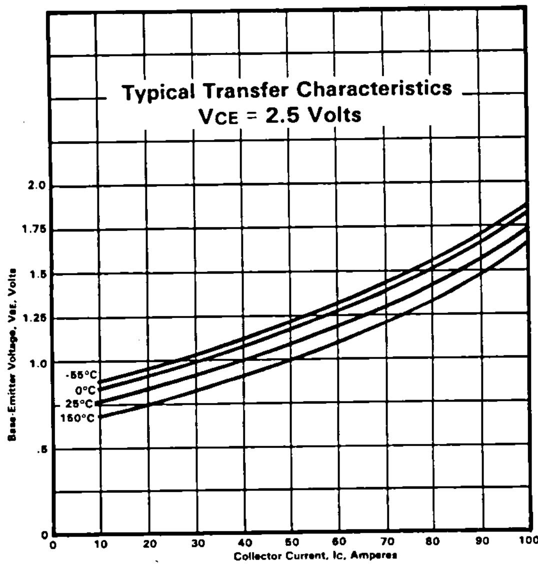
Symbol	Characteristic		Test Conditions	Min.	Typ.	Max.	Units
VCEO (SUS)	Collector-Emitter Sustaining Voltage		IC = 200mA IB = 0 300μs Pulse	See Page T33			
ICEV	Collector Cutoff Current (Base Emitter Reverse Biased)		At Rated VCE VBE (OFF) = -1.5V,		10	100	μA
ICEV	Collector Cutoff Current (Base Emitter Reverse Biased)		At Rated VCE VBE (OFF) = -1.5V, TC = 150°C		.8	3	mA
IEBO	Emitter Cutoff Current		VEB = 7V			5	mA
hFE	DC Current Gain		RC = Rated, VCE = 2.5V	10	15		
hFE	DC Current Gain		IC = 90A, VCE = 2.5V		5		
VCE (SAT)	Collector-Emitter Saturation Voltage		IC = Rated IC/IB = 8.33		.75	1.25	Volts
VBE (SAT)	Base-Emitter Saturation Voltage		IC/IB = 8.33 IC = 40A IC = 50A IC = 60A		1.0 1.25 1.50	1.25 1.50 1.75	Volts
COB	Output Capacitance		fTEST = 1 MHz, VCB = 10V		2500		μμf
f_T	Gain-Bandwidth Product		fTEST = 1 MHz, IC = 5A, VCE = 10V	7	10		MHz
RθJC	Thermal Resistance Junction to Case		VCE = 20V			0.2	°C/W
td	Turn-On Delay	Resistive Load Switch Times	VCC = 250V, IC = 40A			100	ns
t_r	Rise Time		IB1 = IB2 = 4.8A		0.9	1.0	μs
t_s	Storage Time		tp = 50 us		1.25	2.5	μs
t_f	Fall Time		Duty Cycle < 2%		0.3	0.5	μs

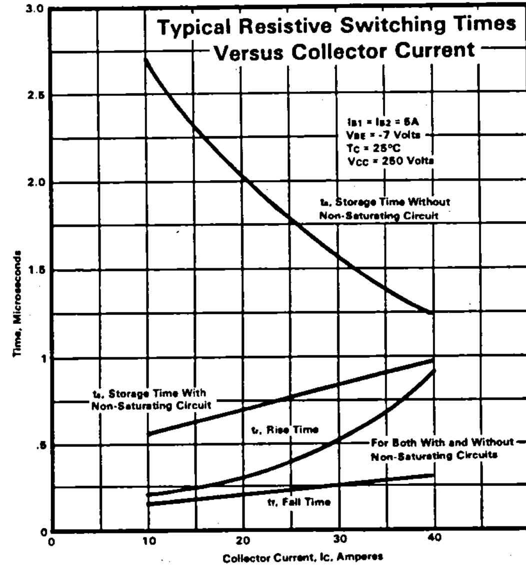


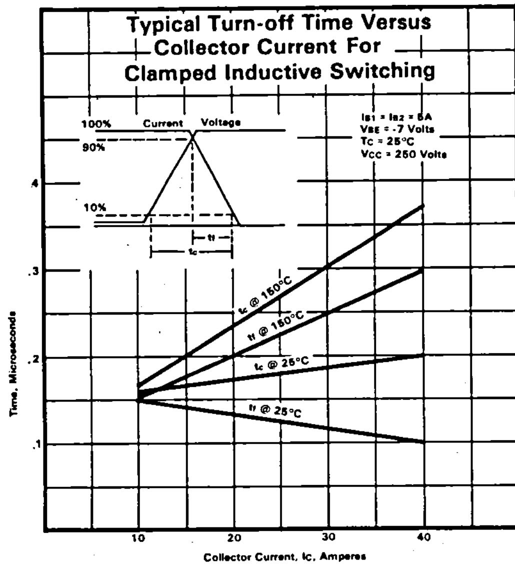
TRANSISTOR

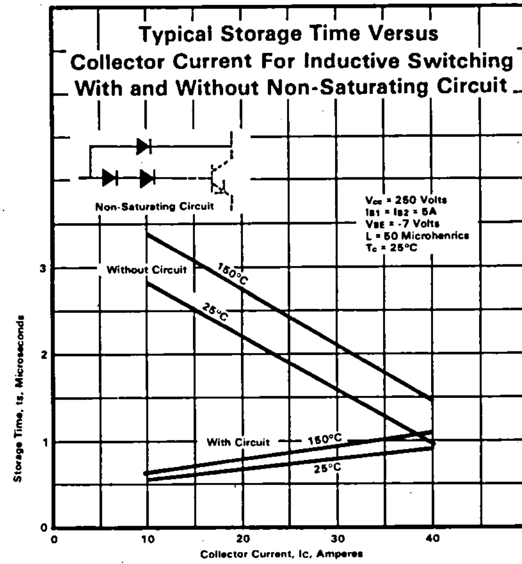
NPN Power Switching TRANSISTORS D60T/D62T

200 Amperes 400—500 Volts









TRANSISTOR

NPN Power Switching TRANSISTORS D60T/D62T

Calculated Maximum Forward Bias Safe Operating Area — S.O.A.

Ic Pulsed
Ic Continuous
10 ms
30 ms
100 ms
300 ms
1 Second
Power Pulse
tp
● Tc = 25°C
● Single Non-Repetitive Pulse
● Applies for all Types
Collector Current, Ic, Amperes
200
100
50
10
5
1
.5
0.1
10
50
100
200
500
Collector-Emitter Voltage, VCE, Volts

REPORT DISTRIBUTION LIST

CONTRACT NAS3-18916

NASA CR-159524

	No. Copies
NASA Lewis Research Center 21000 Brookpark Road Cleveland, OH 44135	
Attn: D. J. Shramo, MS 3-3	1
H. W. Douglass, MS 501-5	1
H. W. Plohr, MS 501-5	1
R. C. Finke, MS 501-8	1
I. T. Myers, MS 501-8	1
G. R. Sundberg, MS 501-8	20
B. L. Sater, MS 501-8	1
J. F. Been, MS 501-7	1
A. G. Birchenough, MS 49-6	1
L. E. Light, MS 500-213	1
P. E. Foster, MS 7-3	1
Librarian, MS 60-3	2
Report Control, MS 5-5	1
R & QA Office, MS 500-211	1
R. L. Pickrell, MS 49-5	1
NASA Headquarters Washington, DC 20546	
Attn: RP/J. Lazar	1
RPP/J. P. Mullin	1
RE/P. R. Kurzhals	1
RES/E. C. Pontius	1
KSA/Librarian	1
NASA Goddard Space Flight Center Greenbelt, MD 20771	
Attn: Librarian, 252.0	1
NASA George C. Marshall Space Flight Center Marshall Space Flight Center, AL 35812	
Attn: R. Lanier, EC 12	1
R. Kapustka, EC 12	1
A. M. Holladay, EC 41	1
F. Villella, EC 43	1
Librarian	1

	No. Copies
NASA Lyndon B. Johnson Space Center	
Houston, TX 77058	
Attn: J. T. Edge, EG 5	1
M. E. Wood, EG 2	1
W. Stagg, EH 5	1
Librarian	1
NASA Ames Research Center	
Moffett Field, CA 94035	
Attn: Librarian, MS 202-3	1
NASA Langley Research Center	
Hampton, VA 23365	
Attn: Librarian	1
NASA Flight Research Center	
P.O. Box 273	
Edwards, CA 93523	
Attn: Librarian	1
NASA John F. Kennedy Space Center	
Kenneday Space Center, FL 32899	
Attn: IS-DOC-IL/Librarian	1
NASA Jet Propulsion Laboratory	
4800 Oak Grove Drive	
Pasadena, CA 91103	
Attn: D. K. Decker, MS 198-220	1
Librarian	1
NASA Scientific and Technical Information Facility	
P.O. Box 8757	
Balt./Wash. International Airport, MD 21240	
Attn: Accessioning Department	25
Department of the Air Force	
Wright-Patterson Air Force Base, OH 45433	
Attn: AFAPL/POP-2, D. G. Fox	1
AFAPL/POD, P. Herron	1
AFAPL/FDL, D. K. Bird	1

	No. Copies
Advisory Group on Electron Devices 201 Varick Street New York, NY 10014 Attn: Working Group on Power Devices	1
Commander U.S. Army Electronics Command Fort Monmouth, NJ 07703 Attn: R. A. Gerhold, DRSEL-TL-1	1
Commanding -icer U.S. Army Research Office P.O. Box 12211 Research Triangle Park, NC 27709 Attn: C. Boghosian	1
Naval Research Laboratory 4555 Overlook Avenue, SW Washington, DC 20375 Attn: D. F. Barbe, Code 5260	1
Commander NAVSEC Code 420 CTRBG 801 Center Building Hyattsville, MD 20782 Attn: A. D. Hitt, Jr.	1
Commander Harry Diamond Labs. 2800 Powder Mill Rd. Adelphi, MD 20783 Attn: A. J. Baba, DRXDO-RCC	1
Naval Electronics Systems Command Washington, DC 20360 Attn: Ron Wade, ELEX-0151431	1
Commander RADC Griffiess AFB, NY 13441 Attn: J. B. Brauer, RBRM	1
Naval Air Systems Command Department of the Navy Washington, DC 20360 Attn: AIR 5368/W. T. Beatson AIR 5368/L. Klein	1 1

	No. Copies
Naval Electronics Laboratory Center San Diego, CA 92152 Attn: J. Foutz, Code 9234	1
U.S. Army Electronics Command Fort Monmouth, NJ 07703 Attn: E. Kittl	1
William R. Peltz DRSEL-PP-I-PI	1
United State Army Mobility Equipment Research & Development Command Fort Belvoir, VA 22060 Attn: E. Reimers	1
D. L. Fetterman, DRX FB-EM	1
National Bureau of Standards Building 225, Room D310 Washington, DC 20234 Attn: D. L. Blackburn, DLB/721	1
Department of Energy Division of Electrical Engineering Systems 20 Massachusetts Aven. Washington, DC 20545 Attn: R. Eaton, MS 2221-C	1
Naval Air Development Center Department of the Navy Johnville, PA 18974 Attn: R. H. Ireland (3043)	1
Jodeph Segrest (3043)	1
Naval Ship Research & Development Center Annapolis, MD 21404 Attn: Carl Kelkenbenz, Code 2771	1
Aerospace Research Application Center 1201 E. 38th Street Indianapolis, IN 46205 Attn: E. Guy Buck	1
Naval Avionics Facility 6000 East 21st Street Indianapolis, IN 46218 Attn: J. H. Jentz	1
Naval Civil Engineering Laboratory Port Hueneme, CA 93043 Attn: H. H. Kajihara	1

No. Copies

	No. Copies
Abacus Controls, Inc. P.O. Box 893 Somerville, NJ 08876 Attn: G. A. Sullivan	1
Aybin Corp, Energy Div. 3180 Hanover Street Palo Alto, CA 94303 Attn: S. Geiger	1
AiResearch Manufacturing Company 2525 W. 190th Street Torrance, CA 90509 Attn: J. Ashmore	1
The Boeing Aerospace Company P.O. Box 3999 Seattle, WA 98124 Attn: I. S. Mehdi, MS 4[illegible]03	1
J. M. Voss, MS 8C-[illegible]2	1
Delco Electronics General Motors Coproration 6767 Hollister Ave. Goleta, CA 93017 Attn: A. Barrett	1
Delta Electronic Control Corporation 2801 S. E. Main Street Irvine, CA 92714 Attn: C. W. Jobbins	1
Electrical Engineering Department Duke University Durham, NC 27706 Attn: T. G. Wilson	1
Hughes Aircraft Company Space Systems Group El Segundo, CA 90245 Attn: R. Martinelli	1
General Dynamics Corporation Convair Aerospace Division P.O. Box 748 Fort Worth, TX 76101 Attn: A. J. I. Carline	1

No. Copies

General Electric Company
Corporate Research & Development
Schenectady, NY 12301
Attn: S. Krishna — 1
D. Schaeffer — 1

ESB Research
19 W. College Ave.
Yardley, PA 19067
Attn: G. Oughton — 1

Electrical Engineering Department
Texas Tech University
Lubback, TX 79409
Attn: W. Portnoy — 1

Gruman Aerospace Corporation
WEDE, Plant 35
Bethpage, L.I., NY 11714
Attn: E. Miller — 1

Instrument Systems Corp.
Telephonics Division
770 Park Avenue
Huntington, L.I., NY 11743
Attn: S. Oken — 1

International Rectifier Corporation
Semi-Conductor Division
233 Kansas Street
El Segundo, CA 90245
Attn: W. Collins — 1

LTV Aerospace Corporation
Vought Missiles & Space Company
P.O. BOx 5907
Dallas, TX 75222
Attn: A. Marek — 1

Lockheed Electronics Co.
1830 NASA Road One
Houston, TX 77058
Attn: C. Wright — 1

Lockheed Missiles & Space Company
P.O. Box 504
Sunnyvale, CA 94088
Attn: R. E. Corbett — 1

	No. Copies
Martin-Marietta Corporation Denver Division P.O. Box 179 Denver, CO 80201 Attn: E. Buchanen	1
National Semi-Conductor Corp. Danbury, CT 06810 Attn: R. R. Bregar	1
Neomed 5595 Arapaho Boulder, CO 80303 Attn: J. Esty	1
McDonnell Douglas Aircraft Co. 3855 Lakewood Blvd. Long Beach, CA 90808 Attn: W. E. Murray, MS 36-43	1
McDonnel Douglas P.O. Box 516, Dept. B454 St. Louis, MO 63166 Attn: J. Gilbert, Bldg. 106/2, MS 074	1
Motorola Semiconductor Products Div. 5005 E. McDowell Road Phoenix, AR 85008 Attn: R. White	1
Power Electronics Associates, Inc. Round Hill Road Lincoln, MA 01773 Attn: F. C. Schwarz	1
Power Tech, Inc. 9 Baker Court Clifton, NJ 07011 Attn: A. M. Plner	1
RCA Solid State Div. New Holland Ave. Lancaster, PA 17604 Attn: S. W. Kessler	1
Rockwell International Corp. Columbus Aircraft Div. 4300 E. Fifth Ave., P.O. Box 1259 Columbus, OH 43216 Attn: J. L. Frencho	1

	No. Copies
Simmonds Precision, Engine Systems Div. Norwich-Oxford Road Norwich, NY 13815 Attn: R. Close	1
Silicon Transistor Corp. Katrina Road Chelmsford, MA 01824 Attn: P. Fitzgerald	1
Solitron Devices, Inc. 1177 Blue Heron Blvd. Riviera Beach, Fl 33404 Attn: S. Holander	1
Texas Instruments, Inc. P.O. Box 5474, MS 72 Dallas, TX 75222 Attn: H. D. Toombs	1
Transitron Electronic Corp. 168 Albrion STreet Wakefield, MA 01880 Attn: S. Bakalar	1
Trans Therm Corp. Ann Arbor, MI 48106 Attn: J. Souder	1
TRW Systems Group One Space Park Redondo Beach, CA 90278 Attn: J. Biess, MC M2/2367	1
D. Zerbel, MC M2/2145	1
University of Cincinnati Dept. of Electrical Engineering 898 Rhodes Hall Cincinnati, OH 45221 Attn: H. T. Henderson, ML 30	1
Westinghouse Aerospace Electrical Div. P.O. Box 989 Lima, OH 45802 Attn: R. Skampfer	1
K. Shuey	1
Westinghouse Research Laboratories 1310 Beulah Road Pittsburgh, PA 15235 Attn: P. L. Hower, 501-2D22	1