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PHASE 2

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SECTION I
INTRODUCTION

The Automated Array Assembly Task, Phase 2 of the Low Cost Silicon Solar Array (LSSA) Project is a process development task. This contract includes solar cell module process development activities in the areas of Surface Preparation. Plasma Processing, Diffusion, Cell Processing and Module Fabrication. In addition, a High Efficiency Cell Development Activity is included. The overall goal is to advance solar cell module process technology to meet the 1986 goal of a production capacity of 500 megawatts per year at a cost of less than $500 per kilowatt. This contract will focus on the process element developments stated above and will propose an overall module process.

During 1978, process step development was carried out on texture etching including the evolution of a conceptual process model for the texturing process; plasma etching; and diffusion studies that focused on doped polymer diffusion sources. Cell processing was carried out to test process steps and a simplified diode solar cell process was developed. Cell processing was also run to fabricate square cells to populate sample minimodules. Module fabrication featured the demonstration of a porcelainized steel-glass structure that should exceed the 20 year life goal of the LSA program.

In a related set of studies, high efficiency cell development was carried out on the Texas Instruments developed Tandem Junction Cell (TJC) and a modification of the TJC called the Front Surface Field cell. These cells feature planar backside contacts with no metallization of the frontside. Cell efficiencies in excess of 16% at AM1 have been attained with only modest fill factors. Photo generated current densities as high as 44 mA/cm^2 at AM0 have been attained. A transistor-like model has been proposed that fits the cell performance and provides a guideline for future improvements in cell performance.

SECTION II
TECHNICAL DISCUSSION

All major task areas are complete. A brief description of the activities in each area follows.

A. SURFACE PREPARATION

Surface texturing experiments have provided a point where some definite conclusions can be drawn and the direction of future work is more obvious. This report summarizes the most significant observations and postulates a mechanism that is consistent with the available data.

All texturing work was done with sodium hydroxide (NaOH) solutions. Hydrazine hydrate also is reported to be useful, but due to cost and safety factors, it has not been included in this study. All texturing work has been done on <100> silicon wafers. The surface texture is the result of preferential etching to form pyramids, whose faces are <111>, on the prior <100> surface.

The following factors have been observed in aqueous NaOH systems. (many of these have been reported by others in earlier studies.)

1. Alcohol Additions

Addition of 1 to 35% isopropyl alcohol (IPA) to dilute NaOH solutions enhances the formation of pyramids. Typically aqueous NaOH with added IPA gives a high density of small pyramids. Optimum conditions have been reported [1, 2] to be a 35% IPA-water solvent, 2% NaOH, at 80°C for 50 minutes.

2. Proximity Effect

It has been observed earlier at Texas Instruments that the presence of another surface, essentially parallel to and in close proximity (0.4-1.0 mm) to the etching surface promotes surface texturing even at NaOH concentrations that normally do not favor pyramid formation, ($\geq$4%). The controlling factor appears to be the entrapment of hydrogen (H_2) bubbles between the two surfaces. This effect allows

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one to texture one surface selectively. Since the effect is dependent on H_2 bubble entrapment; viscosity, flow and position of the parallel surfaces are all factors.

3. Water-Glass ($Na_2SiO_3 \cdot X\ H_2O$) Additions

It has been observed that "used" NaOH solutions were more effective in surface texturing than "fresh" NaOH solutions. Therefore, it is reasonable to assume that small amounts of the reaction product, Na_2SiO_3, would promote the desired selective etching to produce the textured surface. The expected enhancement of selective etching was observed for NaOH solutions containing 0.5-2.0% (vol) $Na_2SiO_3 \cdot X\ H_2O$.

4. Surface Roughness and Damage

Sawed surfaces subjected to concentrated (40%) aqueous NaOH etching to remove damage can exhibit deep pits at damage locations. The walls of these pits initiate pyramid formation more readily than the rest of the surface. To eliminate this effect, chem-mechanically polished surfaces may be used.

5. Greases and Organic Contaminants

Long chain carboxylic acids have been reported to promote texturing.[2] We have observed that greases, even finger prints, have the same effect. Some organic materials, such as polyvinyl chloride cement, seriously inhibit pyramid formation. In our studies, plastic containers were avoided and each wafer was etched for 3 minutes in 30 to 40% aqueous NaOH at 100°C prior to texture etching.

From the foregoing data, the following conclusions were drawn. First, on a <100> surface, all surface atoms are equivalent in their bonding to the crystal lattice. Each atom has an equal chance to become the tip of a pyramid. Therefore, some external influence selects the preferred sites for pyramid formation. Second, since pyramid formation is enhanced in dilute (<4%) aqueos NaOH solutions and not in concentrated (40%) aqueos NaOH solutions, the external factor is related to either solubility in the etchant or dissolution rate. Third, the presence of certain insoluble or slightly soluble materials, greases or fingerprints, enhances pyramid formation, therefore a reaction product is probably a key factor in clean experiments. Fourth, the addition of small amounts of $Na_2SiO_3 \cdot X\ H_2O$ enhances pyramid formation. Na_2SiO_3 is the main reaction product, along with H_2, of the NaOH-Si reaction. Na_2SiO_3 has limited solubility in aqueos NaOH solutions and even lower solubility in water-IPA mixtures. Fifth,

bringing another surface close to the etching one forces the H_2 bubbles to flatten against both surfaces and effectively screens the boundary layer from the remainder of the solution. (This action is intermittent because the bubbles grow, escape, and reform.) Thus, silicate concentration can build up near the surface and promote silicate nucleus formation.

It has been proposed[3] that pyramid formation in the KOH/IPA/H_2O system is caused by silicate precipitation on the surface. These random precipitates protect the top of the pyramid during formation. A similar scheme is envisioned here, except that the protection may be by silicate nuclei growing on the silicon surface rather than by random precipitation in the solution. Figure 1 shows the stages from the formation of protective nuclei to the completion of texturing. The effectiveness or uniformity of the pyramid formation is related to the formation and density of these protected sites.

6. Experimental

In order to quantify the various effects, pyramid formation was measured for the various additives and conditions. This was done by using texturing times that gave only a small fraction of coverage on the surface by pyramids, which allowed them to be counted separately. Texturing was done at 90°C. Data were taken at two NaOH concentrations: 4% and 1%. Chem-mechanically polished surfaces were used to eliminate the roughness effect.

Figure 2 compares the results of:

1) 4% aqueos NaOH for 10 minutes.

2) 4% aqueos NaOH for 10 minutes, with 1% IPA (by volume) added.

3) 4% aqueos NaOH for 10 minutes, with 1% Na_2SiO_3 solution added.

4) 4% aqueos NaOH for 10 minutes, with 0.51 mm proximate surface.

Pyramids were counted from 1/2 to full size. Figure 2 shows that each additive or promoting condition causes a 2-10X increase in pyramid density for this set of conditions.

Figure 3 compares the results of

1) 1% NaOH for 5 minutes.

2) 1% NaOH for 5 minutes, with 1% IPA added.

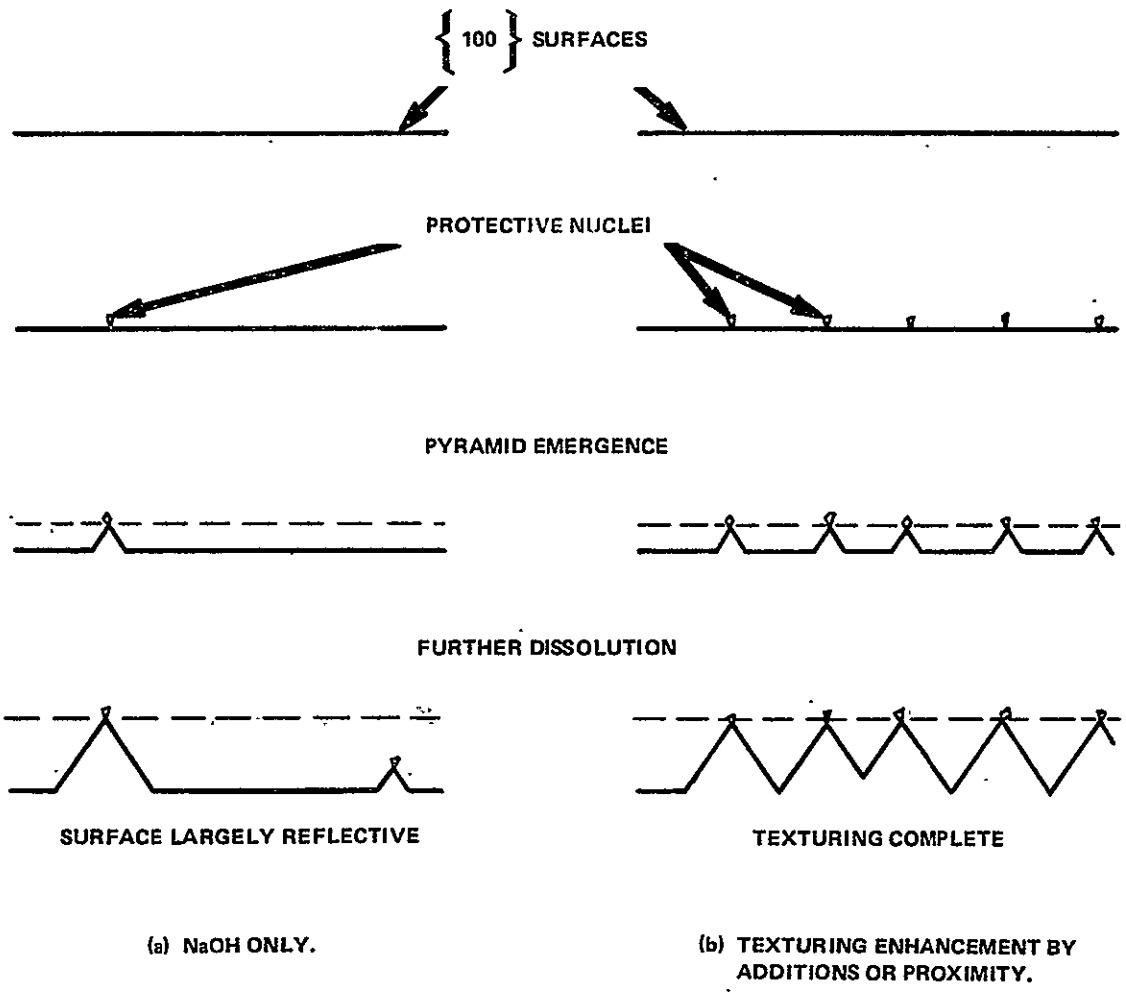


Figure 1. Pictorial Representation of Texturing Process and Enhancement Effects

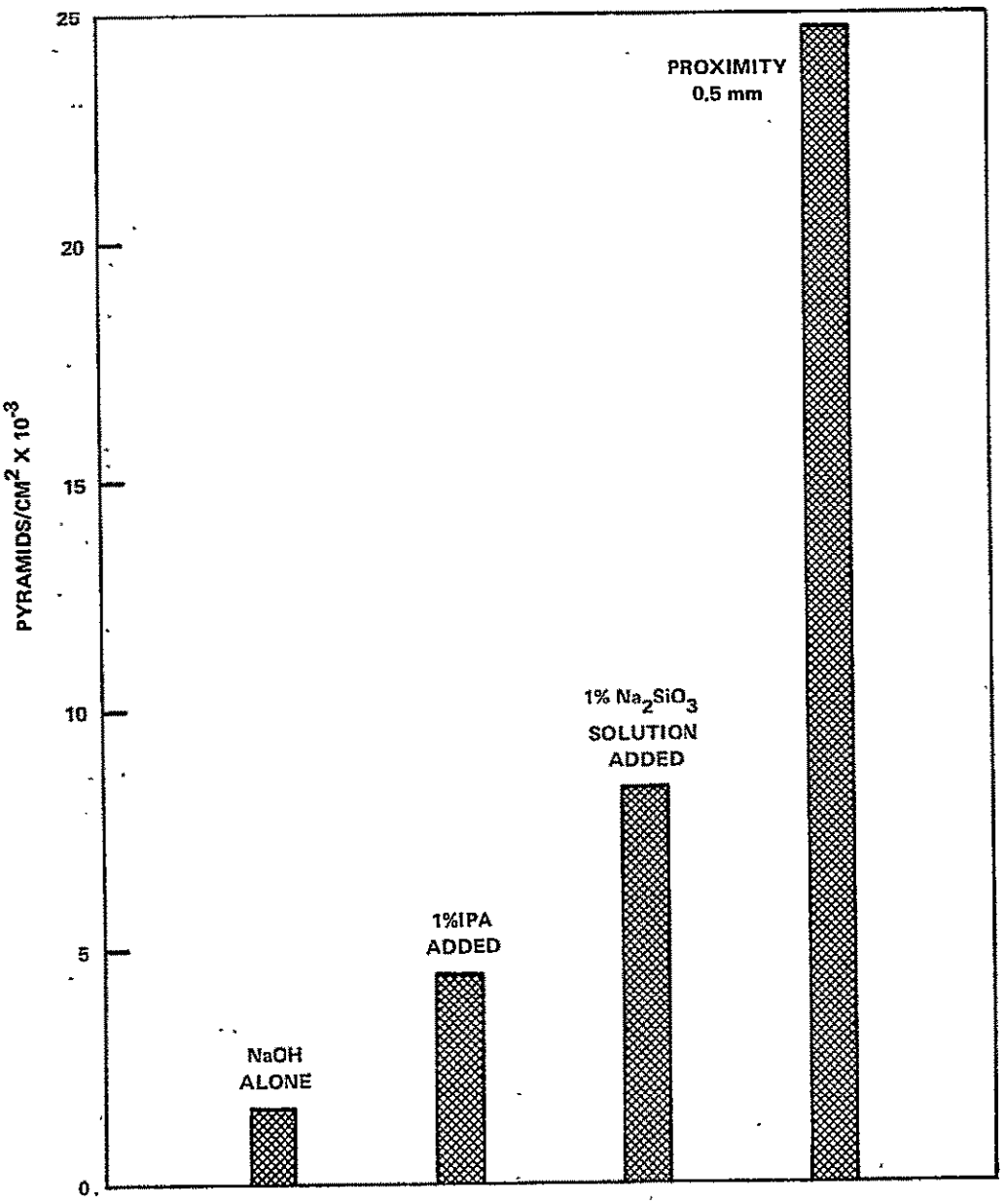


Figure 2. Effects of Various Enhancement Conditions of Pyramid Density in 4% NaOH for 10 Minutes at 90°C

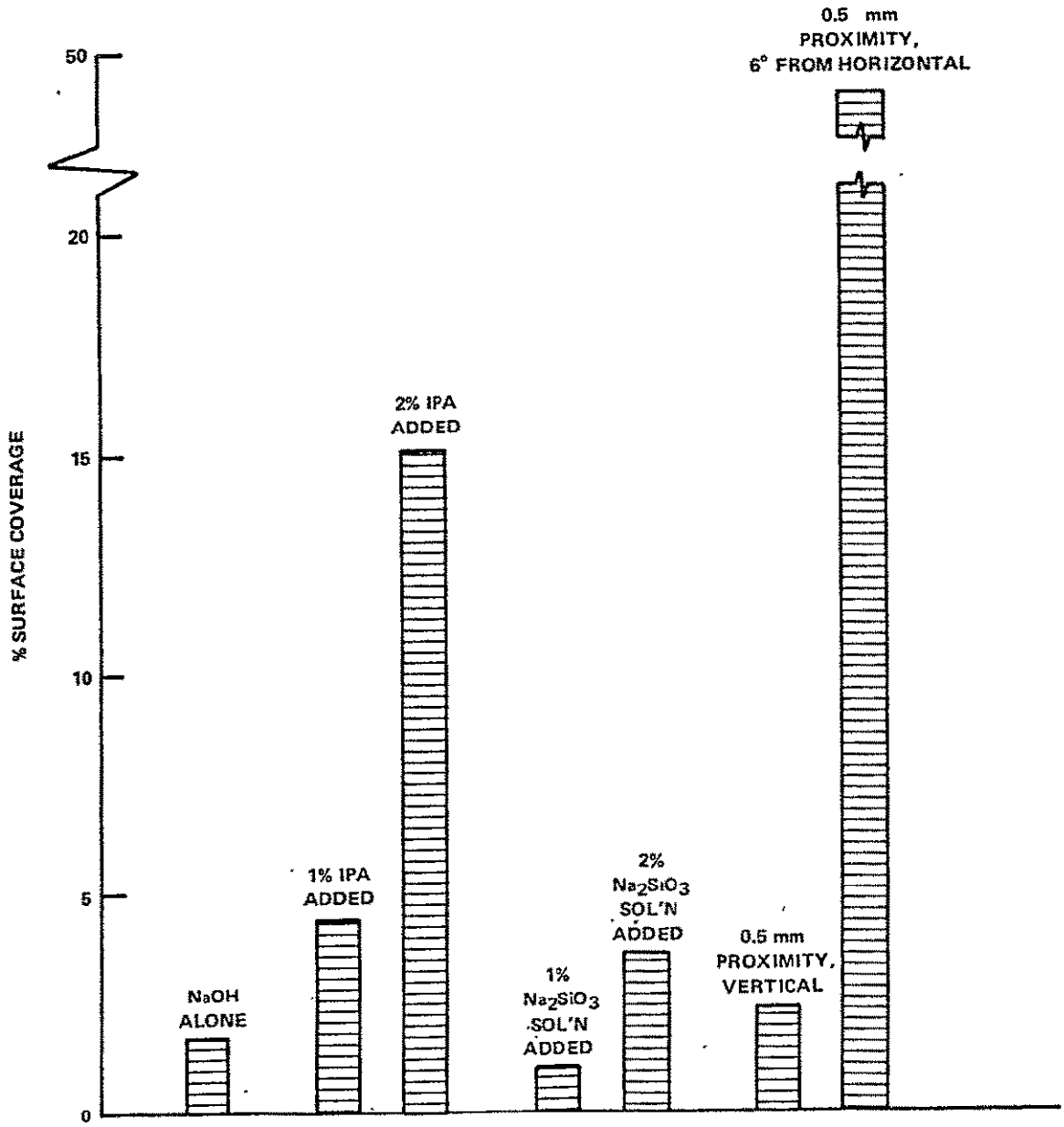


Figure 3. Effects of Various Enhancement Conditions of Pyramid Density in 1% NaOH for 5 Minutes at 90°C

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3) 1% NaOH for 5 minutes, with 2% IPA added.

4) 1% NaOH for 5 minutes, with 1% Na_2SiO_3 solution added.

5) 1% NaOH for 5 minutes, with 2% Na_2SiO_3 solution added.

6) 1% NaOH for 5 minutes, with 0.51 mm proximate surface, vertical.

7) 1% NaOH for 5 minutes, with 0.51 mm proximate surface, 6° off horizontal.

In this case, total areas covered by the pyramids were measured and plotted. This study shows similar results to the foregoing one and that a threshold concentration exists for some additives.

Microscopic examination of the pyramidized surfaces showed a definite connection between silicate growth nuclei and pyramid formation. Such nuclei were present after any pre-etching in concentrated sodium hydroxide and probably accounted for a fraction of the pyramids seen from the unenhanced texturing solution. Often the growth nuclei could still be seen connected to the pyramids even after water rinsing and drying. Figure 4 shows an example as seen by the scanning electron microscope.

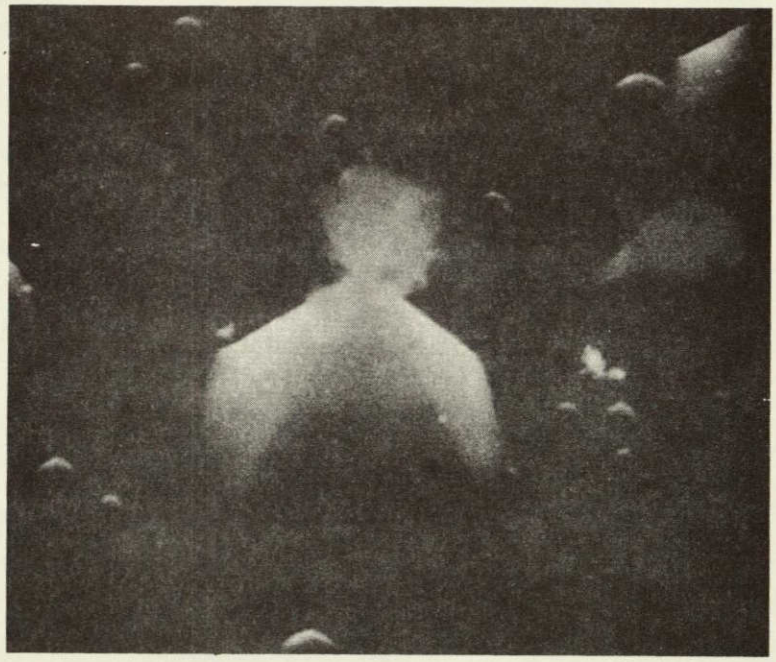


Figure 4. Silicate Growth Nucleus at Top of Texturing Pyramid

Combined use of additives or proximity greatly enhances pyramid formation -- complete texturing can be achieved at reasonable etch times using any two of the additives or conditions noted in the foregoing.

At this stage, texturing appears to be controlled by the formation of Na_2SiO_3 growths on the <100> surface and texturing efficiency can be enhanced by any of the several techniques or combinations of the techniques discussed above. Effective texture etching can be achieved using a variety of conditions. No one best set of conditions is apparent.

The following is a successful texturing process.

A TEXTURING PROCESS

STARTING MATERIALS

(1) Sodium Hydroxide, Pellet or Concentrate (40%)

(2) {100} Oriented Silicon Slices

(3) Teflon Slice Boat

(4) DI Rinse Water

(5) Dilute Acetic Acid

(6) Spin Dryer

(7) Corrosive Etch Hood with Exhaust for H_2 and NaOH-Carrying Vapors

PROCESS PREPARATION

(1) Mix 2% sodium hydroxide and 1% sodium silicate solution by weight, observing usual safety precautions with caustics.

(2) Heat solution to 90°C $\pm$ 2°C, in etch hood.

(3) Load silicon slices into boat with close spacings - 0.5 mm between slices.

Surface Texturing

(4) Place etching boat in solution for 25 minutes.

(5) Dip boat in tank fed with running DI water $\geq$ 5-10 seconds.

(6) Dip boat in dilute acetic 10-20 seconds.

(7) Dip boat in 2nd tank with running DI water 1 minute.

(8) Spin dry.

POST PROCESS STEPS

Maintain texturing solution by adding DI water.

OUTPUT

Wafers texture etched on both sides.

The capacity of the process is limited only by the size of the etch tank. The process can be changed to yield wafers texture etched on one side only by raising the NaOH concentration to 4% (weight) and maintaining the close spacing on one side only.

B. PLASMA ETCHING

Plasma etching represents a potential low cost process element for the removal of unwanted material. Plasma processes have been commercially demonstrated for the etching of SiO_2, Si_3N_4 and Si using flourinated hydrocarbons as the reactive gas. Patterned etching can be achieved by the use of non-reactive etch masks, thick reactive masks and mask stencils. Pattern dimensions are restricted, in the case of solar cells, only by the ability to dimension the masking medium. In this context, only mask stencils impose a possible limiting factor in the ability to produce fine dimension, less than 75 μm. This is not a serious problem for large area solar cell fabrication.

Plasma etching is an attractive low cost process element in that the reactant species is a gas and all reaction products are gases. In this case, the resultant etched surface should be clean at the end of the etching process and no further cleaning operations should be necessary. This is only true,

however, for non-patterned etching and etching through mask stencils. For non-reactive etch masks and thick reactive etch masks, the problem of removing the masking material remains as a cost escalating step.

For plasma etching to be useful in a manufacturing environment, it is felt that a positive etch stop is a requirement. In this context, a positive etch stop means that the etch rate for the removal of a film should be at least 10 X the etch rate of the substrate. This allows the operation to be run to completion with little or no removal of the substrate. In order to operate within an acceptable process window, film thickness variation, etch rate variation, etc., an etch time in excess of the minimum necessary to remove the film must be employed. This excess time should be in the range of 30-50% of the minimum etch time, e.g. if a 3000 Å SiO_2 film can be etched in 10 minutes, the process etch time should be 13 to 15 minutes. In this case, the SiO_2 etch rate is 300 Å per minute, therefore the substrate etch rate should be less than 30 Å per minute. Then the excess etch time would remove less than 90-150 Å of substrate. The ideal, of course, would be no removal of substrate material.

With these constraints in mind, a series of etch rate experiments were run on silicon dioxide, SiO_2, silicon nitride, Si_3N_4, and silicon using carbon tetrafluoride, CF_4, as the reactive plasma etchant. For a standard set of conditions the etch rates are given below.

Material	Etch rate (Å/minute)
SiO_2	300-400
Si_3N_4	300-400
Si	80-100

The etch stop properties of silicon and the substrate are not deemed acceptable for this etchant gas. For a solar cell process using a SiO_2 or Si_3N_4 film on a Si substrate, CF_4 plasma etching is not a good candidate for a low cost process sequence.

Discussions with vendors and persons active in the field of plasma etching as a semiconductor process step indicate that plasma etching is a very useful process tool in less cost conscious operations. Other reactant gases, such as C_3F_8, permit slightly better differential etch rates at a significant increase in reactant gas cost.

At this time, we feel that reactant gas plasma etching is not a prime candidate for a low cost solar cell process sequence.

C. DIFFUSION

A key element in the fabrication of a diode type solar cell is the formation of the collecting junction. In this study the collecting junction is an N^+/P junction formed by the diffusion of an N-Type impurity into a P-type Si substrate. The junction must be shallow to insure high current collection, possess good diode characteristics, provide low sheet resistivity and form low resistance ohmic contact to the current collection metal grid. For comparison purposes, a standard phosphorous diffusion procedure was employed. The standard phosphorous diffusion conditions are listed below:

Source	$POCl_3$
Carrier Gas	N_2, O_2
Temperature	850°C
Time	3 minute heat-up in N_2 12 minute deposition 3 minute flush
Insertion-Withdraw	4 inch per minute
Sheet Resistivity	50 Ω/□ I 10
Diffusion depth	0.3 μm

The usefulness of a collecting junction formation technique was assessed by fabricating solar cells using various diffusion schemes and comparing the resultant photoresponse.

1. Process Temperature and Junction Depth

A diffusion sensitivity experiment containing a matrix of temperatures from 800°C-950°C at times ranging from 7 minutes to 140 minutes was run during the Phase I contract. Further analysis of the minority carrier lifetime, measured by the Surface Photovoltage (SPV) technique, before and after processing as a function of processing temperature and time show the following trends:

1) Diffusion temperature >950°C causes substantial degradation in lifetime (9 μs→5μs).

2) Long diffusion time with phosphorus is beneficial to lifetime ($9\ \mu s \rightarrow 11 \mu s$).

3) Long diffusion time without phosphorus degrades lifetime ($9\mu s \rightarrow 7\mu s$).

These trends are being evaluated in this study.

Based on the above observations on the effect of high temperature, $\geqslant 950°C$, processing steps on base minority carrier lifetime, it appears desireable to minimize time at high temperatures and eliminate temperatures greater than 900°C. On the further observation that dark current density for test diodes fabricated on the wafer with hexagon cells was significantly higher for the diodes than it was for the solar cells, a further hypothesis was made. Test diode dark current density is lower for diodes with deeper junctions. Base resistivity of these test devices was 0.6Ω-cm, therefore dark current is dominated by current injected into the diffused region. The diodes have a high percentage of the surface area (51%) covered by metal and the solar cells have a low percentage of the surface area <10%) covered by metal, therefore:

1) Dark current for the solar cell may be controlled by current injection in the diffused layer area covered by the contact metallization

2) Deeper diffusion under the contact metal area should reduce dark current (and raise V_{oc}) in the solar cell.

A series of test runs have been made to test these hypotheses, using several base resistivities, lower temperature oxide formation steps and a deep N^+ diffusion under the metal contact regions. In all cases the collecting junction diffusion is $\approx 0.3\ \mu m$ deep and formed by an 850°C, $POCl_3$ diffusion. The steam oxidation step was run at 950°C and 900°C and in some cases a low-temperature chemical vapor deposition from silane was used to form the first oxidation. The deep N^+ diffusion, $\approx 1.0 \mu m$, was formed by a masked two-step 850°C, $POCl_3$ diffusion. This data is summarized in Table 1.

Table 1. Process Lot Data – $POCl_3$ Diffusion

Lot No. AAAP-II-	Base Resistivity Ω-cm	Oxide Type (°C)	Deep N^+	Avg* V_{OC} (V)	Avg* I_{SC} (A)
4	1.5	950	No	0.589	1 207
10	1.5	950	No	0.589	1.190
11	1.5	950	Yes	0 598	1.163
24	1.5	900	No	0.535†	0.710†
18	1.5	Silane	No	0.594	1.257
26**	1.5	Silane	No	0.588	1.247
24	0.9	900	No	0 595	1.243
26**	0.9	Silane	No	0.595	1.283
4	0.6	950	No	0.591	1.160
16	0.6	950	Yes	0.608	1 203
25	0.6	Silane	Yes	0.605	1.247
25	0.2	Silane	Yes	0.606	1.083

*Averages based on best 3 of 4 solar cells.

**Square cell design – cell area = 37.2 cm^2, all other data is for hexagonal cell area = 37.7 cm^2.

†This lot may have been contaminated, see Cell Processing.

Lots AAAP-II-4 and -10 are representative of haxagonal cells produced by the standard baseline process using 1.5 Ω-cm material. Lots AAAP-24, -18 and -26 represent the baseline process using a 900°C oxidation step or CVD silane oxide. (The data from lot AAAP-II-24 is questionable due to a probable Cu contamination during February, see Cell Processing.) Note that lots AAAP-II-18 and -26 using silane oxide give $I_{sc} \approx 4\%$ higher than the baseline. Lot AAAP-II-11 uses the baseline process with the deep N^+ diffusion under the contact metallization. V_{oc} is ≈ 9-10 mV higher for this configuration. The increase in V_{oc} is limited by the base resistivity in this case. The increase in I_{sc} for the silane oxide lots implies an improvement in base minority carrier lifetime as predicted.

Lots AAAP-II-24 and -26 were run on 0.9 Ω-cm material using a 900°C steam oxidation and a silane oxide, respectively. Both lots give very good V_{oc} and I_{sc} values with the silane oxide lot ≈3% higher than the 900°C oxidation lot. V_{oc} for the 0.9 Ω-cm materials is≈6mV higher than for the 1.5 Ω-cm material, as expected.

Lots AAAP-II-4, -16 and -25 were run on 0.6 Ω-cm material, using the 950°C oxidation (baseline) and silane oxide. The deep N^+ diffusion was used on lots AAAP-II-16 and -25. Lot AAAP-II-16 using the deep N^+ shows an improvement in both V_{OC} and I_{SC} over the baseline process (AAAP-II-4). The V_{OC}=0.608 V is the best we have seen for large area cells, the increase in I_{SC}, ≈2%, is unexpected and may not be significant. The silane oxide lot with a deep N^+, AAAP-II-25, gave excellent V_{OC} and I_{SC} values, as expected.

Lot AAAP-II-25 run on 0.2 Ω-cm material using silane oxide and deep N^+ diffusion gives high V_{OC}, 0.606 V, but lower I_{SC} is due to the reduced minority carrier lifetime in the low resistivity base material.

In summary, the hypotheses that lower processing temperatures (<900°C) would improve current collection, I_{SC}, and that a deeper N^+ diffusion under the contact metallization would improve V_{OC}, appear to be valid. Under optimum conditions, an improvement of 5% to 10% in V_{OC} might be realizable.

2. Arsenic Ion Implant and Arsenic Polymer Dopant

Results on As ion implant (II) and As polymer dopant are summarized in Tables 2 and 3. Lots AAAP-II-5, -9 and -19, all use the baseline process with the As II operation in place of the $POCl_3$ diffusion. Solar cells were fabricated with and without a 1000°C, 10-minute anneal after implant and with and without

Table 2. Results of Arsenic Ion Implanted Lots

Lot No. AAAP-II-	Cell No.	Base Resistivity Ω-cm	Oxide Type (°C)	Anneal Temp (°C)	Getter Temp (°C)	V_{OC} (V)	I_{SC} (A)
5	13	1 5	950	–	850	0.534	0 84
	14	1 5	950	–	850	0 539	0.89
	15	1.5	950	--	–	0 490	1.1
	16	1.5	950	–	–	0 495	1.1
9	A-9	1.5	950	1000	850	0.552	0.80
	A-10	1.5	950	1000	850	0.563	0 89
	A-11	1.5	950	1000	850	0.556	0.84
	A-12	1.5	950	1000	–	0.567	0.89
19	C-6	1.5	950	1000	–	0.575	1.0
	C-7	1 5	950	1000	850	0 579	1.1
	C-8	1.5	950	1000	850	0 526	0.72

a 850°C $POCl_3$, 5-minute gettering step. Both V_{oc} and I_{sc} are lower than with the baseline process (compare to lots AAAP-II-4 and -10, Table 1). Lot AAAP-II-19 appears to have a cell number identity problem (C-6 and C-8 are reversed?). As ion implant has not yielded results equivalent to the baseline process in this work.

As spin-on polymer dopant diffusions were run at 900°C and 1000°C. At 900°C a diffusion time of 7.6 hours is required to achieve an N^+ sheet resistivity of $\approx 60\Omega/\square$. At 1000°C, the diffusion time is 2 hours. The data is summarized in Table 3. Both V_{oc} and I_{sc} are better for the 900°C diffusion but not equivalent to the results from the baseline process. The low diffusion coefficient of As at acceptable process temperatures effectively rules out As as an N^+ dopant for high throughput processes requiring junction depths on the order of 0.3 μm.

TABLE 3. AM0 PHOTORESPONSE FOR As POLYMER DOPANT

Diffusion Temperature (°C)	Time (Hr)	V_{OC} (V)	I_{SC} (A)
900	7.6	0.58	0.97
1000	2.0	0.53	0.75

Arsenic ion implanted solar cells were fabricated using a 50 keV, $2 \times 10^{15}/cm^2$ dose implant for the N^+ layer. The implant was activated at 1000°C or using a two-temperature annealing cycle. The data for these two groups are shown in Table 4. The higher V_{oc} for lot AAAP-II-30 indicates better activation of the implanted As at 1000°C, but the lower I_{sc} indicates more residual damage. Neither process is quite as good as the baseline $POCl_3$ process.

TABLE 4. PHOTORESPONSE DATA ON II SOLAR CELLS

Lot No.	Anneal	V_{OC} (V)	I_{SC} (A)
AAAP-II-30	1000°C/20 min	0.584	1.09
AAAP-II-48	500-850-500°C	0.560	1.16

3. Phosphorous and Boron Polymer Dopant

Samples of phosphorous (P) and boron (B) doped polymer sources were obtained from Allied Chemical and Emulsitone. Initial evaluation of Accuspin PX-10 (Allied Chemical) at 850°C diffusion temperature indicated this is a suitable N^+ diffusion source. The Accuspin B-120 (Allied Chemical) source was run at 850°C, 900°C, and 925°C. Data for both diffusion sources are shown in Table 5. A second boron source, B-122, with a higher boron content gave results similar to the B-120 polymer dopant. The PX-10, phosphorous source, gives acceptable N^+ diffused layers at 850°C with a 30-90 minute diffusion. The slower diffusing boron may form an acceptable base contact during a simultaneous diffusion. The faster diffusing phosphorous should be an acceptable alternate to the arsenic-doped polymer sources.

Table 5. Polymer Dopant Diffusion Results (N_2 ambient)

Temperature (°C)	Source	Sheet Resistivity (Ω/□) @ Time (minutes)		
		30	60	90
850	PX-10	67	43	32
850	B-120	≈500	≈500	225
900	B-120	–	160	110
925	B-120	–	88	95

Phosphorous doped polymer sources make an attractive diffusion source for solar cells. The doped polymer can be applied by a number of high throughput processes such as spin-on, spray or print. In this study spin-on application was used. Application and diffusion processes provided by the vendor are very acceptable. The polymer dopant sources are very attractive process elements due to the inherent ability to apply the diffusion source to only one side as opposed to the gas phase diffusion schemes that diffuse all exposed surfaces. An evaluation of solar cells fabricated with doped polymer sources is included in the Cell Processing Task.

D. CELL PROCESSING

Two types of solar cells were fabricated during this program, diode cells and tandem junction cells (TJC s). TJC experiments and fabrication are reported in Section II. F, High Efficiency Cell Development. Diode cell process experiments were carried out using a hexagonal cell developed in Phase I of this program until the square cell masks were available. The square cells used for all module assembly were fabricated as part of this task.

A baseline cell fabrication process featuring a gas phase $POCl_3$ diffusion was used as a standard for comparison. Since no metallization development was included as part of this study, evaporated Ti-Pd-Ag contact metallization was used in all process variations.

1. Cell Design

A revised large-area cell was designed for use on this contract as a vehicle for process development and to provide cells for assembly of modules. This cell is a truncated square scribed from 7.62 cm (3 inch) circular slices. Based on module optimization studies, the cell is 6.2 centimeters on a side. The cell contains some of the test patterns developed on the previous contract for evaluation of processes.

A layout of the cell is shown in Figure 5. Number of metal stripes and spacing were determined by design techniques developed on the previous contract. Test patterns included on the cell are indicated by letters. The test patterns are variations of designs from the previous contract and include:

A) Concentric Ring Pattern - (4 variations)

B) 4-point metal pattern - on stripe

C) 4-point metal pattern - on oxide

D) Diodes (2 each)

E) Spreading resistance contact to base region on backside (3 each)

F) Test cell with AR coating

G) Test cell without AR coating

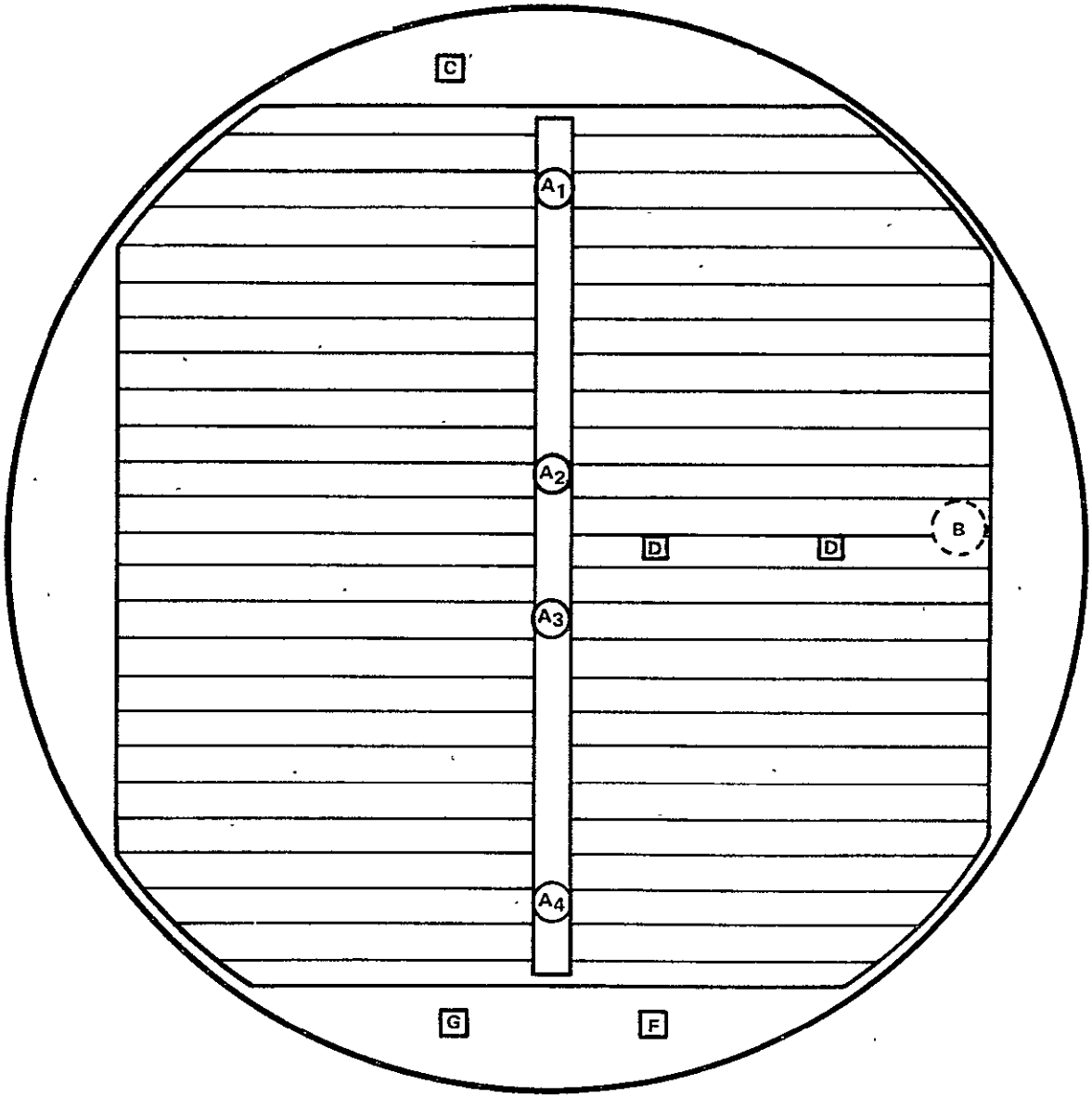


FIGURE 5. LAYOUT OF CELL AND TEST PATTERNS

2. Processing Baseline

A standard process was defined. Process steps are shown in Figure 6.

Starting Material
P-type
<100>
0.3-2.0 Ω-cm
$\tau > 50\mu s$
Cleanup
Oxidize - 2 KÅ
Pattern Oxide - Front side
Diffuse N^+ - $POCl_3$, 850°C, 15 minute
Deposit Silane (1200Å) - front side
Remove Oxide - back side
Evaporate Aluminum - back side
Sinter
Open Contacts - front side
Evaporate Metal - front side
Pattern Metal - front side
Test

FIGURE 6. STANDARD BASELINE PROCESS

A set of process step variations was run to optimize each process step in this baseline process sequence. The results are shown in Table 1 in the previous section. From these results, the oxidation was run at 900°C or a chemically vapor deposited (CVD or silane oxide) oxide was used. Although improved V_{oc} was attained by using a deep N^+ diffusion directly under the contact metallization, this extra step was not included in the baseline cell process. The back side aluminum sinter provided a back surface field and a back contact.

3. Ion Implant

Arsenic (As) ion implant was briefly investigated as an alternate to the $POCl_3$ diffusion. The results are summarized in Table 2 and Table 4. These solar cell lots were processed to compare As ion implant with As polymer dopant. Ion implant evaluation and optimization were not primary tasks in this study.

Ion implantation is an attractive process element in a solar cell process sequence for a number of reasons. Impurity atoms can be implanted on one side of the wafer under controllable depth and dosage conditions. However, the implant technique creates significant crystal damage in the impurity layer that must be removed by annealling techniques and machine throughput is limited with presently available technology.

In this limited test, ion implanted As is equivalent to arsenic polymer dopant as a diffusion source, but neither technique is equivalent to a $POCl_3$ diffusion for solar cell fabrication. Therefore, As ion implantation was not further pursued as a process element in a low cost solar cell process sequence.

4. Polymer Dopants

a. Arsenic

Arsenic polymer dopants have been used at Texas Instruments in integrated circuit production for a number of years. A proprietary As polymer dopant is available within Texas Instruments. Evaluation of this As polymer dopant for solar cell fabrication is summarized in Table 3. The high diffusion temperatures and long times are not compatible with good solar cell response or with high throughput, low cost processing. Therefore, As polymer dopant was rejected as an acceptable process element in a low cost solar cell process sequence.

b. Phosphorous and Boron

Diffusion experiments with phosphorous and boron polymer dopants (see earlier section) indicated that acceptable diffusion conditions existed for these materials.

Using the results from the spin-on polymer dopant evaluation, a set of low-cost process alternatives can be derived. Based on the diffusion of phosphorous from PX-10, the process alternatives shown in Table 6 were chosen for evaluation. All three process alternatives have steps 2 through 6 in common. Process step 1 represents different approaches to the introduction of a P^+ layer on the back of the cell. Process step 3 is a 850°C diffusion that is also used to drive in the boron or aluminum on the back side, thus eliminating the separate high-temperature operatio

Process step 4, involves evaporation of the contact metallization through a mask stencil. These low-cost process alternatives completely eliminate the use of photoresist or critical alignment operations. Versions of these low-cost process alternates were experimentally evaluated.

Table 6. Low Cost Process Alternatives

Process Step	I	II	III
1	Spin-on B-120	Evaporate Al	Print Ag-Al
2	Spin-on PX-10	Spin-on PX-10	Spin-on PX-10
3	Diffuse-Deglaze	Diffuse-Deglaze	Diffuse-Deglaze
4	Evaporate TiPdAg	Evaporate TiPdAg	Evaporate TiPdAg
5	Plate Ag	Plate Ag	Plate Ag
6	AR Coat	AR Coat	AR Coat

Since front metal contact pattern mask stencils were not available at the time, the Ti-Pd-Ag was patterned by conventional photoresist - etch techniques. Low cost process alternate (LCPA) III was evaluated using an Aluminum - Silver ink supplied by Cermalloy Corporation. The ink contained no glassy frit. Only two Al/Ag ratios were evaluated, 5% and 10% Al. The purpose of the experiment was to evaluate a fritless ink containing a p-type dopant. The p-type dopant in the ink would provide a back surface field and improved ohmic contact during the firing cycle. The Al/Ag ink was fired and the phosphorous polymer dopant (PX-10, Allied Chemical Corporation) was diffused in one 850°C chain furnace operation, dwell time at temperature was 30 minutes. Solar cell photoresponse under AM0 conditions is shown in figure 7. The short circuit current is comparable to cells fabricated using the baseline $POCl_3$ process and the open circuit voltage is only slightly lower. The fill factor for the 10% Al ink, 0.65, is significantly better than for the 5% Al ink. The concept of using a doped metal ink was not pursued beyond this point on this program. However, this feasibility demonstration is very encouraging as a significant process simplification in that three process steps, N^+ diffusion, back surface field and back side metallization, are all combined in a single simultaneous high temperature operation.

LCPA II was evaluated by evaporating 2 - 4000 Å of Al on the back of a wafer, spinning PX-10 on the front and simultaneously alloying and diffusing at 850°C for 30 minutes under N_2 in a tube furnace. Ti-Pd-Ag contact metallization was evaporated onto both sides. Several experimental solar cell lots were processed using this process alternate. Lot to lot repeatibility and uniformity was excellent.

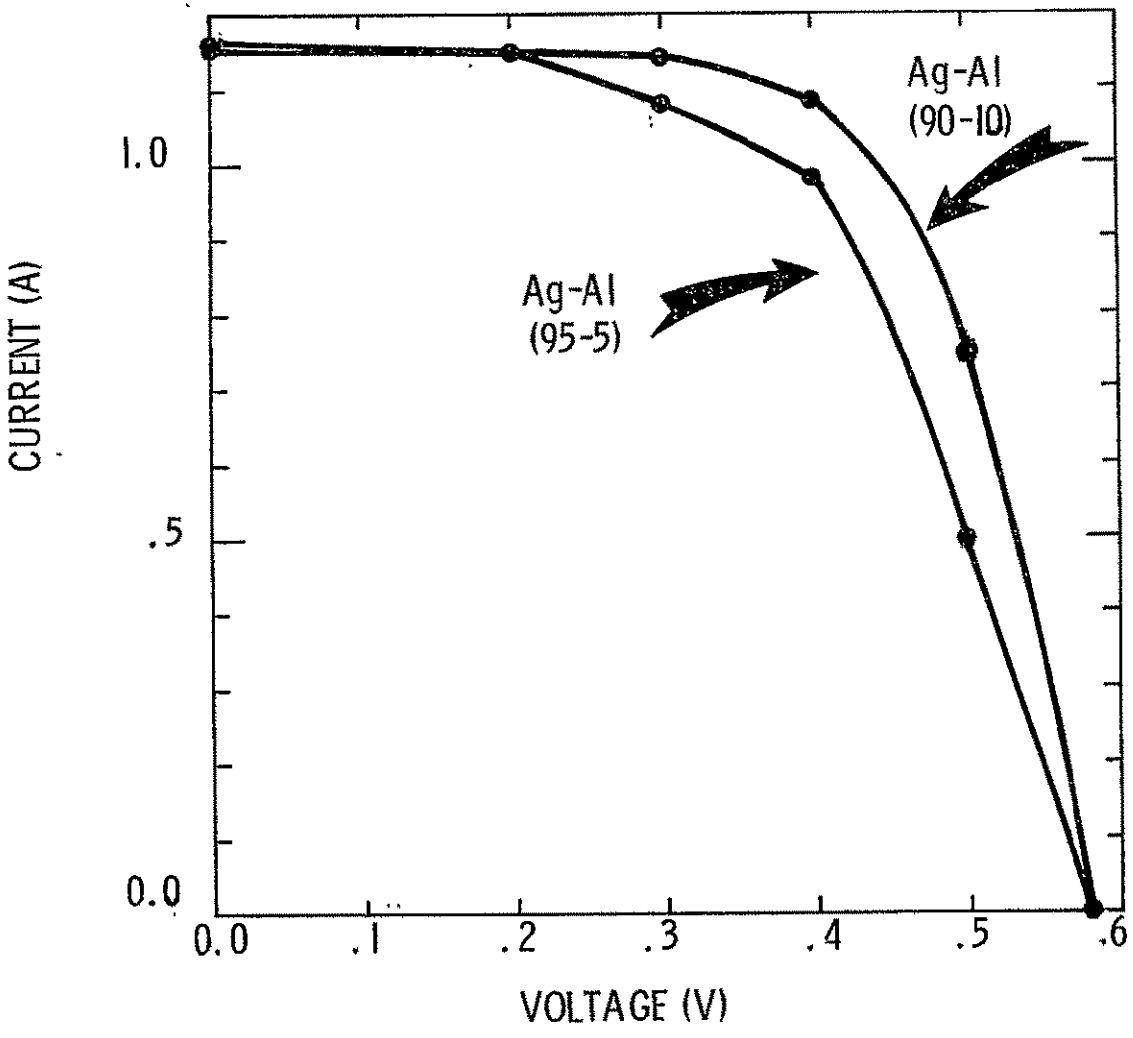


FIGURE 7. PHOTORESPONSE OF PRINT P+ CELL

Photoresponse was as good on the baseline $POCl_3$ process. Photoresponse under AM0 illumination from a 36 cell typical lot is shown in Table 7. Process yield was excellent. No electrical rejects were generated and the only losses

TABLE 7. PHOTORESPONSE FOR LOW COST PROCESS ALTERNATE II.

V_{oc}	0.6084 ± .0045 V
I_{sc}	1.146 ± .036 A
$I_{.500v}$	1.068 ± .037 A
F.F.	.77
AM0	10.6%

were a few broken wafers. Several minimodules were fabricated from solar cells processed using LCPA II.

During the course of process experiments using phosphorous polymer dopants one precautionary thing was observed. A process lot was run using a phosphorous polymer dopant sample, Emulsitone N-250, that had significantly passed its recommended shelf life. After diffusion, significant surface staining was observed under the polymer dopant film. The stain remained after deglaze. The process lot was completed, metallization and antireflection coating, and evaluated. The photoresponse under AM0 illumination showed a much wider spread than normally encountered. The thirty wafer lot was separated into six groups of five cells each. Photoresponse for each of the six groups and for the whole lot is given in Table 8. These cells were used to assemble minimodule 6.

TABLE 8. PHOTORESPONSE OF STAINED SOLAR CELLS AT AM0

Group	V_{oc} (V)	I_{sc} (A)	$I_{.500v}$ (A)
1	.610 ± .002	1.144 ± .041	1.05 ± .033
2	.606 ± .002	1.078 ± .018	1.00 ± .012
3	.605 ± .005	1.064 ± .030	.972 ± .008
4	.608 ± .002	1.044 ± .034	.950 ± .012
5	.607 ± .002	1.032 ± .008	.928 ± .004
6	.604 ± .004	0.960 ± .029	.842 ± .050
Lot Average	.6067 ± .0034	1.054 ± .062	.957 ± .070

The effect of the surface staining can be seen by comparing the data from Table 7 and Table 8. The change in V_{OC} is within the expected lot to lot variation, i.e., there is no measureable effect on V_{OC} due to the staining. The change in I_{SC} is more dramatic. The surface staining causes a drop in I_{SC} of 92 mA, .8% and a significant increase in the standard deviation from $\pm$ 36 mA to $\pm$ 62 mA. The drop in $I_{.500V}$ is similar, 111mA. Apparently the effect of the silicon surface staining is a shadowing effect not a surface recombination effect. The solar cells were useable but selection was required before module assembly to optimize module performance. The cosmetic appearance of the stained cells before or after the deposition of the antireflection coating was very poor. The decrease in photoresponse was ~10%, on average.

This experience reinforces the manufacturers' cautions about shelf life and proper storage of doped polymer films. When proper storage is used and shelf life limitations are observed, no deleterious effects were observed and the materials perform very satisfactorily.

LCPA-I using phosphorous doped polymer and boron doped polymer diffusion sources was also run. Diffusion time in this instance was increased from thirty minutes to sixty minutes at 850°C to accomodate the slower diffusing boron. Experiments were run on 1 and 6 Ω-cm wafers and a control was run using evaporated Al as the P^+ source on the back side (LCPA II). Results are summarized in Table 9. While the boron polymer dopant gives a diffused layer that is adequate to insure ohmic contact, it does not generate an effective BSF in high resistivily material. Higher diffusion temperatures or longer times would generate a BSF but would not be compatible with the simultaneous front-back side diffusion philosophy of these process sequences due to the deeper N^+ junctions that would be generated on the front side of the wafers.

TABLE 9. LCPA - I RESULTS. (AM0)

Substrate Resistivity (Ω-cm)	Dopants (Front/Back)	Time/Temperature (Minutes/°C)	V_{oc} (V)	I_{sc} (A)
1	P/Al	30/850	.607	1.15
1	P/B	60/850	.600	1.06
6	P/B	60/850	.565	1.13

From the above results on LCPA I, II and III, it was concluded that LCPA-I is the least attractive of the three choices. Both LCPA-II and III give very encouraging results. LCPA - II was chosen as the process sequence to use in fabricating solar cells for several of the minimodules. LCPA-III is also very attractive but obviously more development is needed before the doped silver ink approach is ready for implementation even in a laboratory.

5. Polycrystalline Wafer Processing

At the request of the contract monitor, a set of experiments was run on polycrystalline wafers to compare poly versus single crystal results. A crystal was grown that is single crystal at the top and becomes progressively more polycrystalline down the boule. Wafers taken from four sections of this crystal were processed through the baseline process to establish the effect of the polycrystalline grain boundaries. The four sections were labeled A through D, with section A being single crystal and sections B, C and D being successively more polycrystalline. AM0 photoresponse results on large-area square cells are given in Table 10. The N^+/P junction was 0.3 μm deep, formed by a $POCl_3$ diffusion. All polycrystalline samples, B, C and D, were substantially poorer than the single crystal portion. The differences between the polycrystalline groups are not considered to be significant. The effects of increasing numbers of grain boundaries from group B to group D are apparantly not controlling factors in these cells. It was speculated that a deeper N^+ diffusion would improve the properties of the polycrystalline devices, therefore this experiment was rerun using a deeper diffusion.

TABLE 10. PHOTORESPONSE ON POLYCRYSTALLINE SOLAR CELLS

Lot Number	V_{OC} (V)	I_{SC} (A)
AAAP-II-51A	0.586	1.09
AAAP-II-51B	0.540	0.93
AAAP-II-51C	0.556	0.98
AAAP-II-51D	0.550	0.99

The rerun of this experiment using a 0.5 μm N^+/P junction depth gave virtually identical results. The conclusion from these experiments is that polycrystalline wafers produce substantially poorer solar cells than single crystal wafers.

6. Test Module Cell Fabrication

Solar cells were fabricated to populate the minimodules using two cell process sequence. Cells for modules 1, 2, 3 and 5 were fabricated using the baseline process, figure 6, with either SiO_2 or Si_xNy, silicon nitride, as the AR coat. Cells for modules 4 and 6 were fabricated using LCPA II, Table 6. Both processes gave excellent repeatable results. The uniformity within a lot is shown in Tables 11 and 12 for the baseline process and LCPA-II, respectively. All solar cells used on the minimodule assembly were truncated squares, 6.2 cm on a side,

Table 11. Photoresponse at AM0, Si_xNy AR coating, Baseline Process, 28°C

Cell Number	V_{oc} (mV)	I_{sc} (A)	I_{500mV} (A)
1	608	1.15	1.03
2	608	1.17	1.04
3	608	1.15	1.06
4	608	1.14	1.06
5	610	1.17	1.06
6	610	1.16	1.04
7	610	1.17	1.05
8	608	1.14	1.03
9	610	1.15	1.04
10	609	1.16	1.04
11	610	1.15	1.06
12	608	1.14	1.03
13	608	1.16	1.05
14	Broken		
15	609	1.14	1.04
16	609	1.15	1.03
17	608	1.13	1.04
18	608	1.16	1.06
19	609	1.15	1.06
20	610	1.16	1.04
21	610	1.15	1.04
22	606	1.21	1.08
23	608	1.20	1.08
24	Broken		
25	609	1.18	1.02
26	611	1.14	1.03
27	610	1.15	1.02
28	610	1.17	1.07
29	610	1.18	1.07
30	611	1.17	1.07

Table 12. Photoresponse at AM0, Si_xNy Ar coating, LCPA II, 28°C

Cell Number	V_{oc} (mV)	I_{sc} (A)	I_{500mV} (A)
1	613	1.21	1.14
2	613	1.21	1.15
3	611	1.16	1.09
4	600	1.11	1.01
5	611	1.19	1.09
6	609	1.17	1.11
7	614	1.18	1.13
8	614	1.19	1.06
9	614	1.19	1.10
10	607	1.16	1.09
11	613	1.20	1.11
12	612	1.18	1.10
13	609	1.17	1.10
14	615	1.18	1.10
15	601	1.14	1.03
16	605	1.10	1.05
17	610	1.13	1.05
18	607	1.18	1.05
19	605	1.12	1.03
20	613	1.13	1.07
21	605	1.12	1.03
22	608	1.12	1.05
23	601	1.10	1.01
24	611	1.12	1.07
25	610	1.16	1.10
26	605	1.10	1.04
27	605	1.10	1.04
28	607	1.10	1.04
29	610	1.10	1.05
30	602	1.12	1.04
31	597	1.09	1.00
32	608	1.13	1.06
33	605	1.15	1.06
34	609	1.15	1.05
35	613	1.17	1.10
36	609	1.12	1.06

cut from 7.62 cm round wafers (see figure 5). The process lots shown in Tables 11 and 12 show excellent mechanical yield and excellent electrical yield. This performance is typical of both processes. The broken cells shown in Table 11 are the result of handling mistakes. A well engineered, mechanized process should have a near zero mechanical loss. The LCPA-II process obviously gives photoresponse equivalent to the more complex baseline process. For the diode cell structure, the LCPA-II process is the process of choice at this time.

7. Tandem Junction Cell Processing

TJC processing is covered in section II. F. High Efficiency Cell Development.

E. MODULE FABRICATION

A model has been developed [4] which analyzes the effect of the various efficiency components on the overall module efficiency and is a valuable tool to assess the impact of the design factors. The overall module efficiency of the model is the product of the encapsulation efficiency η_{EC} and packing efficiency η_p. Encapsulation efficiency considers all the variables influencing the electrical performance of each individual cell in the cell array, and the packing efficiency contains all the variables determining the active cell area in relation to the total module area.

Overall module efficiency is expressed by the following equations:

$$\text{Module Efficiency} = \frac{\text{module power}}{\text{module area X 1000 watt/M}^2}$$

$$\eta_M = \overbrace{[\eta_C\ \eta_{MIS}\ \eta_\tau\ \eta_{NOCT}]}^{\eta_{EC}} \times \overbrace{[\eta_{BR}\ \eta_{BS}\ \eta_{IC}\ \eta_N]}^{\eta_p}$$

where

η_{EC} = Encapsulated cell efficiency

η_C = Cell efficiency at 28°C, 100 mW/cm^2

η_{MIS} = Cell mismatch efficiency

η_τ = Optical transmission efficiency

η_{NOCT} = Cell operating temperature efficiency

η_p = Packing efficiency

η_{BR} = Border area efficiency

η_{BS} = Bus area efficiency

η_{IC} = Interconnect area efficiency

η_N = Cell nesting efficiency

Theoretical packing efficiencies were calculated using the following constraints:

6.16 cm and 6.20 cm square silicon cells

0.10 cm spacing between cells

1.00 cm allowance for bus and interconnect

1.00 cm border

Module width = 0.750 (N) -- 0.12 inch

Where "N" is an integer value from 13 to 64 (obtained from JPL Drawing J10082854 Rev. A, Note 7) Refer to Table 13.

In the encapsulation efficiency a high cell efficiency at standard condition η_C, is achieved using the thin Tandem Junction cell structure. The cell mismatch efficiency η_{MIS} is generally not controlled at the module design stage but is maximized through close process control at cell manufacturing. In a parallel-series module configuration, selection of cells for each parallel connected row can be used so that the short circuit current for each row is equal. In the model I^2R loss efficiency is considered to be part of the cell mismatch efficiency, however, it can be influenced in significant degree by the module design and the related interconnect arrangement and the selected materials to be used in the interconnections and bus bars and could, therefore, be considered as an individual item in the module efficiency equation.

TABLE 13. ALLOWABLE MODULE WIDTHS

Module Width = 0.750 (N) – 0.12 inch
Where N = 13 to 64 (integer value)

N	Inches	cm	N	Inches	cm
13	9 63	24.46	39	29.13	73.99
14	10.38	26.37	40	29 88	75.90
15	11.13	28.27	41	30.63	77.80
16	11.88	30.18	42	31.38	79 71
17	12 63	32.08	43	32.13	81.61
18	13.38	33.99	44	32.88	83.52
19	14.13	35.89	45	33.63	85.42
20	14 88	37.80	46	34.38	87.33
21	15 63	39.70	47	35.13	89 23
22	16.38	41.61	48	35.88	91 14
23	17.13	43.51	49	36.63	93.04
24	17.88	45.42	50	37.38	94.95
25	18.63	47.32	51	38.13	96.85
26	19.38	49.23	52	38.88	98 76
27	20.13	51.15	53	39.63	100.66
28	20 88	53.04	54	40 38	102.57
29	21.63	54 94	55	41.13	104.47
30	22 38	56.85	56	41 88	106 38
31	23 13	58.75	57	42.63	108.28
32	23.88	60.66	58	43.38	110.19
33	24.63	62.56	59	44.13	112.09
34	25 38	64 47	60	44.88	114.00
35	26.13	66.37	61	45.63	115.90
36	26 88	68.28	62	46.38	117.81
37	27.63	70 18	63	47.13	119.71
38	28 38	72 09	64	47 88	121.62

The optical transmission efficiency η_T is determined by the characteristics of the encapsulant. To meet the requirements of high optical transmission and durability against environmental deterioration and mechanical damage during the twenty year expected life time, glass has shown to be the best choice at this time. By using low iron glass and proper antireflection treatments optical transmission efficiency $\eta_T = 0.95$ can be achieved. The last component of the encapsulation efficiency, the nominal operating cell temperature efficiency η_{NOCT}, is influenced in significant degree by the module design. Due to the antireflection treatments used on the photovoltaic cells, up to 95% of the incident radiation transmitted through the encapsulant is absorbed in the cell and has to be either converted to electrical energy or dissipated as heat. Of the commercially available materials within a competitive price range porcelain-enameled steel has shown to be an excellent choice. It has a demonstrated 20 year life, good thermal transmission characteristics and allows broad latitude in the design of the module components. By using porcelain-enameled steel, a major portion of the thermal energy can be conducted through the substrate and dissipated from the back side of the module.

The packing efficiency is more receptive to optimization at the module design phase. Four components, η_{BR}= border efficiency, η_{BS}= bus bar efficiency, η_{IC} = interconnect efficiency and η_N = nesting efficiency, constitute the components of η_P = packing efficiency. A high border efficiency is obtained by the narrow picture frame structure and when porcelain-enameled steel is the structural materia the down turned flanges provide the necessary mechanical strength and stiffness for the substrate. The bus efficiency can be high by judicial design of large area modules and a parallel-series interconnection arrangement. The flexibility of the porcelain-enameled steel as a substrate material permits contouring of the substrate so that bus bars for the parallel interconnections can be recessed behind the silicon solar cells and exposed bus area is required only for the series interconnections. The parallel interconnection, with bus bars running across the solar cells, reduces the problem of open circuits due to cell cracking thereby improving reliability. The series interconnects between the parallel rows, at both ends of the rows, reduces the I^2R losses and at the same time establishes redundancy. A higher value of η_{IC} would be obtained with Tandem Junction cells in back-contact configuration, which eliminates the shadowing losses of front metallization. Clearance is not required between the cells for front-to-back connection. The spacing between the cells has to be only sufficient to provide electrical isolation and to prevent shorting during cell row soldering, therefore, reducing the interconnect area.

The nesting efficiency η_N is the component of packing efficiency which is most influenced by the cell array design and by the type, shape, and dimensions of the cell in relation to the module size, which has been determined by the design objectives. To evaluate the effect of the module and cell dimensions on packing efficiency we have selected a module size with an overall length of 121.6 cm, while overall width must be (N X 1.9 cm) - 0.3 cm where N is an integer from 13 to 64. These constraints were established for the LSA Project. As was pointed out earlier this module size has been selected only for illustration purposes, and the principles are applicable to any module size. Design border is subtracted from the 121.6 cm overall length; in our example, one cm at each end. This brings the adjusted length of the area available for cells and interconnect spacing to 119.6 cm. To obtain high nesting efficiency it is obviously very difficult to pack round or hexagonal cells into the allocated rectangular area without wasted space. Therefore, rectangular or square cells must be used to optimize packing density. In selecting the cell size for the module, practical aspects of the cell manufacturing have to be considered. Although, ribbon or sheet growth processes are under development most of today's solar cells are manufactured from Czochralski grown single crystals of silicon. Therefore, 6.2 cm square cells, which could be cut from 8.8 cm (3.5 in.) diameter wafers, were selected for basic packing efficiency calculations. If 0.1 cm is allocated for spacing between the cells for electrical isolation, 19 cells will fill the 119.6 cm length. The width of the module is determined by the number of cells per row and can be changed and optimized. Tables 14 through 17 and Figures 8 through 10 show the effect of the numbers of cells per row on the packing efficiency. For square cells the nesting efficiency is 100 and the interconnect efficiency remains constant. Bus efficiency increases with the number of cells per row because the bus area is constant. Border efficiency, which includes the picture frame and the excess area generated by the mismatch between the cumulative width of the cells and the permitted module widths, increases in a discontinuous manner with increasing number of cells per row. Because of weight limitations the best efficiency for a practical size (2' X 4') module is achieved at eleven cells per row. For our work 10 cells per row was selected because at this point, the packing efficiency exceeded 90%. Obviously, the more restrictive the dimensions of the cell and module are, the more difficult it is to achieve a high overall packing efficiency η_p.

When the relative cost of the silicon sheet, made out of Czochralski crystal, and the add-on cost of the module, per unit area, are considered, it might not be advantageous to cut a full square out of the round wafer, but a modified square with rounded corners could give the highest overall material utilization efficiency and the lowest cost per peak watt. At today's silicon wafer prices a round cell would be optimum to minimize the module cost per peak watt. However, when the

TABLE 14. MODULE DESIGN EFFICIENCY CALCULATIONS - 6.16-cm CELL

Module Length 47.88 inches = 121.62 cm
Cell Length (19 @ 6.16 cm) = 117.04 cm
Cell Spacing (18 @ 0.1 cm) = 1.80 cm
Border (2 @ 1.0 cm) = 2.00 cm
Excess Length = 0.78 cm
19 Cells/Column (fixed) 6.16 cm x 6.16 cm each

		Numbers of Cells Per Row															
		3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Total Cell Width (cm)		18.48	24.64	30.80	36.96	43.12	49.28	55.44	61.6	67.76	73.92	80.08	86.24	92.40	98.56	104.72	110.88
Cell Space Width																	
Total (cm)		0.20	0.30	0.40	0.50	0.60	0.70	0.80	0.90	1.0	1.10	1.20	1.30	1.40	1.50	1.60	1.70
Border Width (cm)		2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2.00
Bus Allowance																	
Width (cm)		1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20
Total Module																	
Width (cm)		21.88	28.14	34.40	40.66	46.92	53.18	59.44	65.70	71.96	78.22	84.48	90.74	97.00	103.26	109.52	115.78
Recommended JPL																	
Width (cm)		24.46	28.27	35.89	41.61	47.32	54.94	60.66	66.37	72.09	79.71	85.42	91.14	98.76	104.47	110.19	115.90
Excess Area (cm)		323.70	37.30	203.90	144.60	84.10	250.70	191.40	130.80	71.50	238.10	177.60	118.30	284.90	224.30	165.00	104.60
Module Area (cm^2)	A	2974.8	3438.2	4364.9	5060.6	5755.1	6681.8	7377.5	8071.9	8767.6	9694.3	10388.8	11084.4	12011.2	12705.6	13401.3	14095.8
Planned Border Plus																	
Excess Area (cm^2)	B	611.9	333.1	514.9	467.1	418.0	599.8	552.0	502.8	454.9	636.8	587.7	539.8	721.7	672.5	624.6	575.6
Bus Area (cm^2)	C	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143.5
Interconnect Area																	
(cm^2)	D	70.2	93.6	117.0	140.4	163.9	187.3	210.7	234.1	257.5	280.9	304.3	327.7	351.1	374.5	397.9	421.3
Cell Area (cm^2)	E	2162.9	2883.9	3604.8	4325.8	5046.8	5767.7	6488.7	7209.7	7930.6	8651.6	9372.6	10093.5	10814.5	11535.5	12256.4	12977.4
Efficiency (%)																	
Border	η_{BR}	79.4	90.3	88.2	90.8	92.7	91.0	92.5	93.8	94.8	93.4	94.3	95.1	94.0	94.7	95.3	95.9
Bus	η_{BS}	93.9	95.4	96.3	96.9	97.3	97.6	97.9	98.1	98.3	98.4	98.5	98.6	98.7	98.8	98.9	98.9
Interconnect	η_{IC}	96.8	96.8	96.8	96.8	96.8	96.8	96.8	96.8	96.8	96.8	96.8	96.8	96.8	96.9	96.9	96.9
Nesting	η_N	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
Packing	η_P	7.27	83.9	82.6	85.5	87.7	86.3	88.0	89.3	90.5	89.2	90.2	91.1	90.0	90.8	91.5	92.1

TABLE 15. MODULE DESIGN EFFICIENCY CALCULATIONS - 6.16-cm CELL

		Number of Cells Per Row															
Efficiency (%)		**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**
Border Area		79.4	90.3	88 2	90.8	92.7	91.0	92 5	93.8	94 8	93 4	94.3	95.1	94.0	94.7	95.3	95.9
Bus Area		93 9	95.4	96.3	96.9	97.3	97.6	97 9	98.1	98.3	98 4	98.5	98.6	98 7	98.8	98.9	98.9
Interconnect Area		96 8	96 8	96.8	96.8	96.8	96.8	96.8	96 8	96.8	96.8	96 8	96.8	96.8	96.9	96.9	96.9
Cell Nesting		100 0	100.0	100.0	100.0	100.0	100.0	100 0	100.0	100.0	100.0	100.0	100 0	100.0	100.0	100.0	100 0
Packing		72.7	83.9	82.6	85.5	87.7	86.3	88.0	89.3	90.5	89.2	90.2	91.1	90.0	90.8	91.5	92.0
Cell @ 28°C, 100 mW/cm^2	AM1	20 0	20.0	20.0	20.0	20.0	20 0	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0
Cell Mismatch																	
Optical Transmission	P 91.0 R 95 0 O 98 0	95 0	95 0	95 0	95.0	95.0	95 0	95.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0	95.0
NOCT																	
Encapsulated	**R (95.0)**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**
	Pessimistic	13 2	15.3	15.0	15.6	16.0	15.7	16.0	16.3	16.5	16.2	16.4	16 6	16.4	16.5	16.7	16.7
Module	Realistic	13.8	15.9	15.7	16.2	16.7	16 4	16.7	17.0	17.2	16 9	17.1	17.3	17.1	17.3	17.4	17.5
	Optimistic	14.2	16.4	16.2	16.8	17.2	16.9	17.2	17.5	17.7	17.5	17.7	17.9	17.6	17.8	17.9	18.0

TABLE 16. MODULE DESIGN EFFICIENCY CALCULATIONS - 6.2-cm CELL

Module Length 47.88 inches = 121.62 cm
Cell Length (19 @ 6.20 cm) = 117.80 cm
Cell Spacing (18 @ 0.1 cm) = 1.80 cm
Border (2 @ 1.0 cm) = 2.00 cm
19 Cells/Column (fixed) 6.2 cm x 6.2 cm each

	Number of Cells Per Row															
	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Total Cell Width (cm)	18.60	24.80	31.00	37.20	43.40	49.60	55.80	62.00	68.20	74.40	80.60	86.80	93.00	99.20	105.40	111.60
Total Cell Space Width (cm)	0.20	0.30	0.40	0.50	0.60	0.70	0.80	0.90	1.00	1.10	1.20	1.30	1.40	1.50	1.60	1.70
Border Width (cm)	2.00	2.00	2.00	2.00	2.00	2.00	2.00	2 00	2 00	2 00	2.00	2.00	2.00	2.00	2 00	2.00
Bus Allowance Width (cm)	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20
Total Module Width (cm)	22.00	28.30	34.60	40.90	47.20	53.50	59.80	66.10	72.40	78.70	85.00	91.30	97.60	103.90	110.20	116.50
Recommended JPL Width (cm)	24.46	28.27	35.89	41.61	47.32	54.94	60.66	66.37	73.99	79 71	85.42	93.04	98.76	104.47	110.19	117.81
Excess Area (cm^2)	294.27	– 0 –	154.31	84.93	14.35	172 25	102.87	32.30	190.20	120.82	50.24	208.14	138.76	68.18	– 0 –	156.70
Module Area (cm^2)	2974.8	3438.2	4364.9	5060.6	5755.1	6681.8	7377.5	8071.9	8998.7	9694.3	10388.8	11315.5	12011.2	12705.6	13401.3	14328.1
Planned Border Plus Excess Area (cm^2)	582.47	295.8	465.31	407.43	348.25	521.35	463.47	404.30	573.60	519.52	460.34	629.64	575.56	516.38	459.6	627.70
Bus Area (cm^2)	143.5	143.5	143.5	143.5	143.5	143.5	143.5	143 5	143 5	143.5	143.5	143.5	143 5	143.5	143.5	143.5
Interconnect Area (cm^2)	70.6	94.2	117.8	141.3	164.9	188.4	212.0	235.6	259.1	282.7	306.2	329.8	353.4	376.9	400.5	424.0
Cell Area (cm^2)	2191.1	2921.4	3651.8	4382.2	5112.5	5842.9	6573.2	7303.6	8034 0	8764 3	9494 7	10225.0	10955.4	11685.8	12416.1	13146.5
Efficiency (%)																
Border	80.4	91.4	89.3	91.9	93.9	92 2	93.7	95.0	93.6	94.6	95.6	94.4	95.2	95.9	96.6	95.6
Bus	94.0	95.4	96 3	96.9	97.3	97.7	97.9	98.1	98.3	98.4	98.6	98.7	98.7	98.8	98.9	99.0
Interconnect	96.9	96.9	96 9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9
Nesting	100.0	100.0	100.0	100.0	100.0	100 0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
Packing	73.7	85.0	83.7	86.6	88 8	87 4	89 1	90.5	89.3	90.4	91.4	90 4	91.2	92.0	92.6	91.8

TABLE 17. MODULE DESIGN EFFICIENCY CALCULATIONS - 6.2-cm CELL

		Number of Cells Per Row															
Efficiency (%)		**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**
Border Area		80.4	91.4	89.3	91.9	93.9	92 2	93.7	95.0	93.5	94.6	95.6	94.4	95.2	95.9	96.6	95.6
Bus Area		94.0	95.4	96 3	96 9	97.3	97 7	97.9	98 1	98.3	98.4	98.6	98.7	98.7	98.8	98.9	99.0
Interconnect Area		96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96.9	96 9	96 9	96.9	96.9	96.9
Cell Nesting		100 0	100.0	100.0	100.0	100.0	100 0	100 0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0	100.0
Packing		**73.7**	**85.0**	**83.7**	**86.6**	**88.8**	**87.4**	**89.1**	**90.5**	**89.3**	**90.4**	**91.4**	**90.4**	**91.2**	**92.0**	**92.6**	**91.8**
Cell @ 28°C, 100 mW/cm^2	AM1	20.0	20.0	20.0	20 0	20 0	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20 0	20.0	20.0	20.0
Cell Mismatch																	
Optical Transmission	P 91.0 R 95.0 O 98.0	95 0	95.0	95.0	95 0	95.0	95 0	95.0	95.0	95.0	95 0	95.0	95.0	95.0	95.0	95.0	95.0
NOCT																	
Encapsulated	**R (95.0)**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**	**19.0**
Module	Pessimistic	13.4	15.5	15.2	15.8	16.2	15.9	16.2	16.5	16.3	16.5	16.6	16.5	16.6	16.7	16.9	16.7
	Realistic	14 0	16.2	15.9	16.5	16 9	16.6	16.9	17.2	17.0	17.2	17.4	17.2	17.3	17.5	17.6	17.4
	Optimistic	14 4	16.7	16.4	17.0	17.4	17.1	17.5	17.7	17.5	17.7	17.9	17.7	17.9	18.0	18.1	18.0

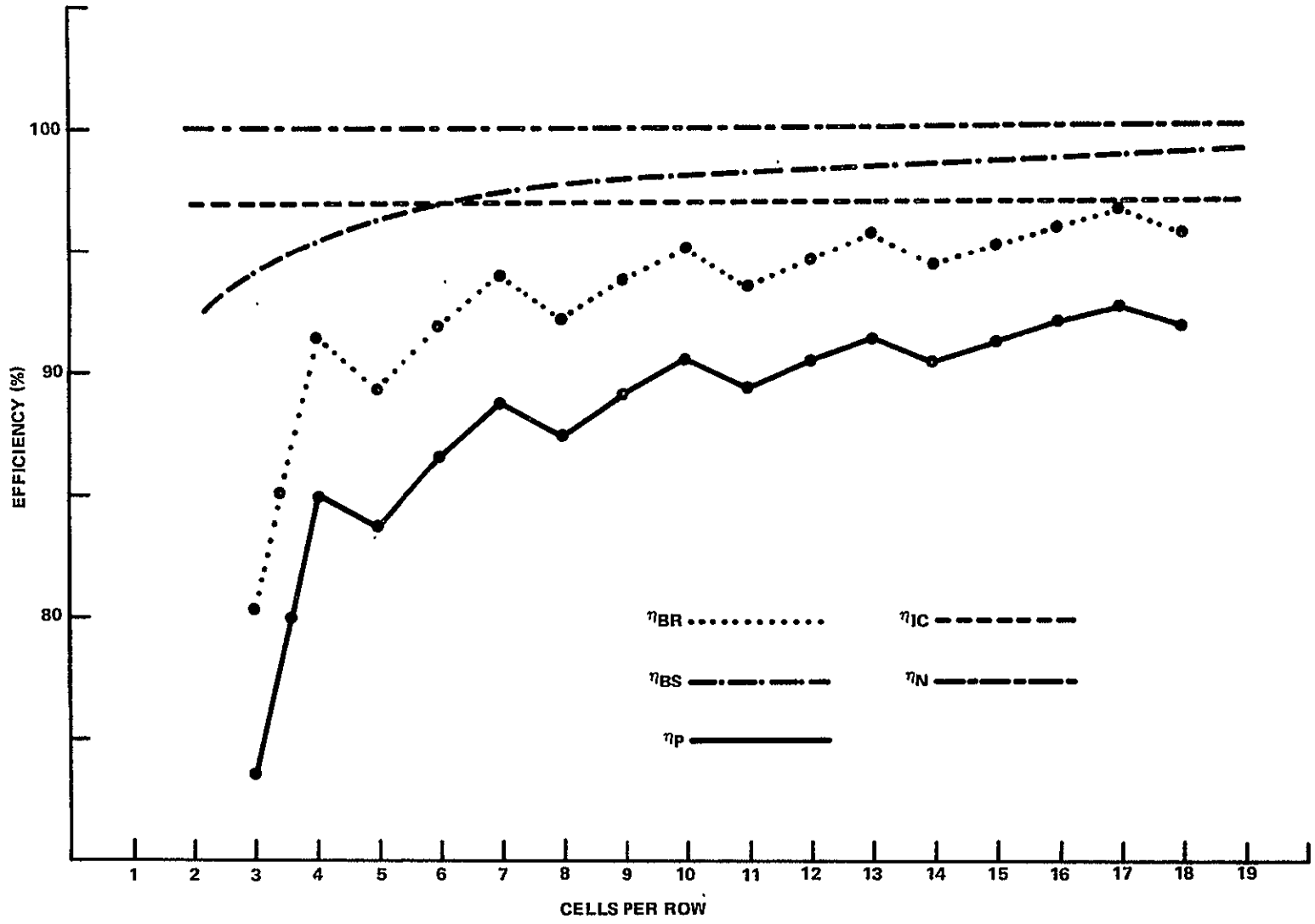


FIGURE 8. PACKING EFFICIENCY - 6.16-cm CELL

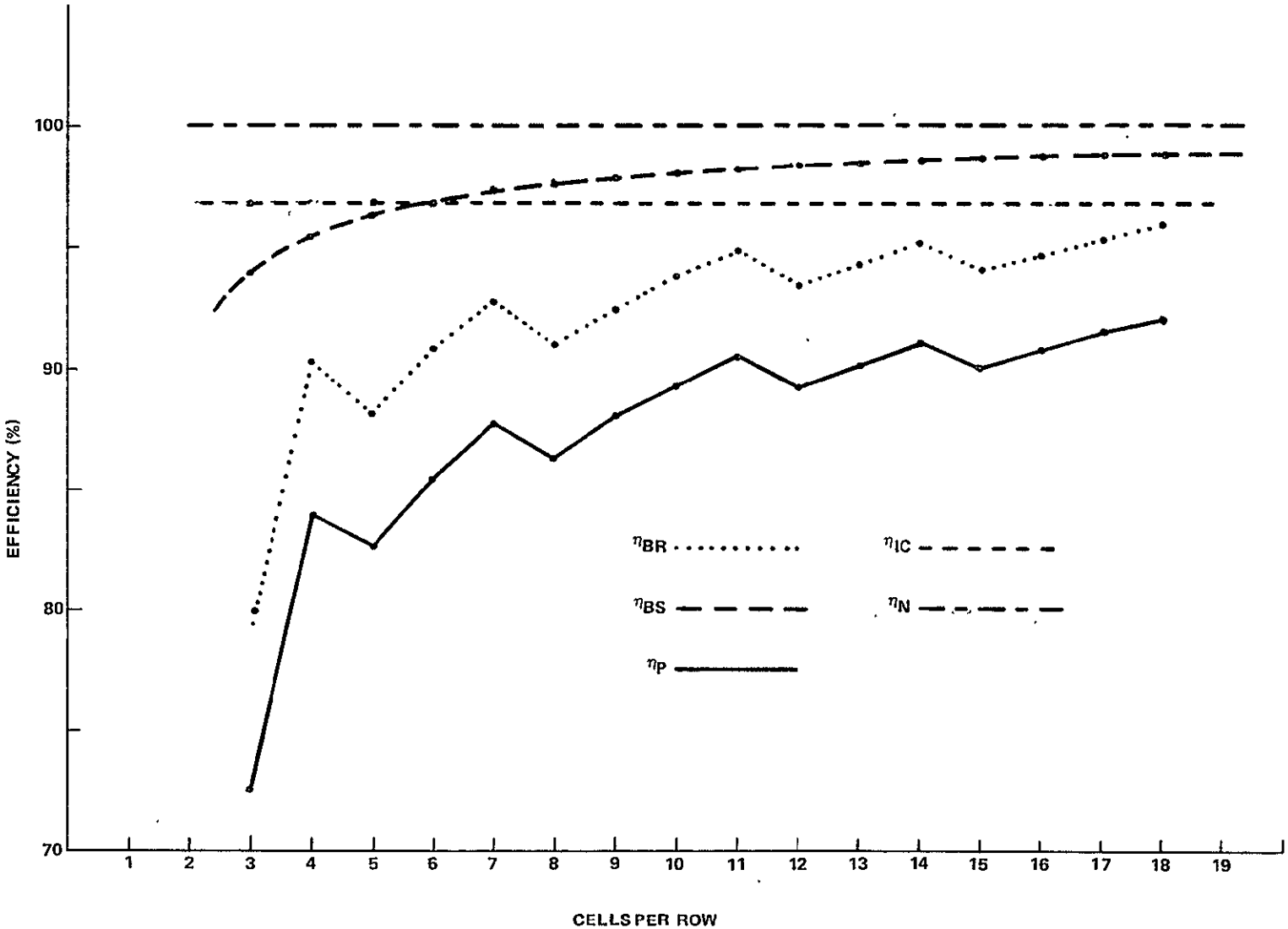


FIGURE 9. PACKING EFFICIENCY - 6.2-cm CELL

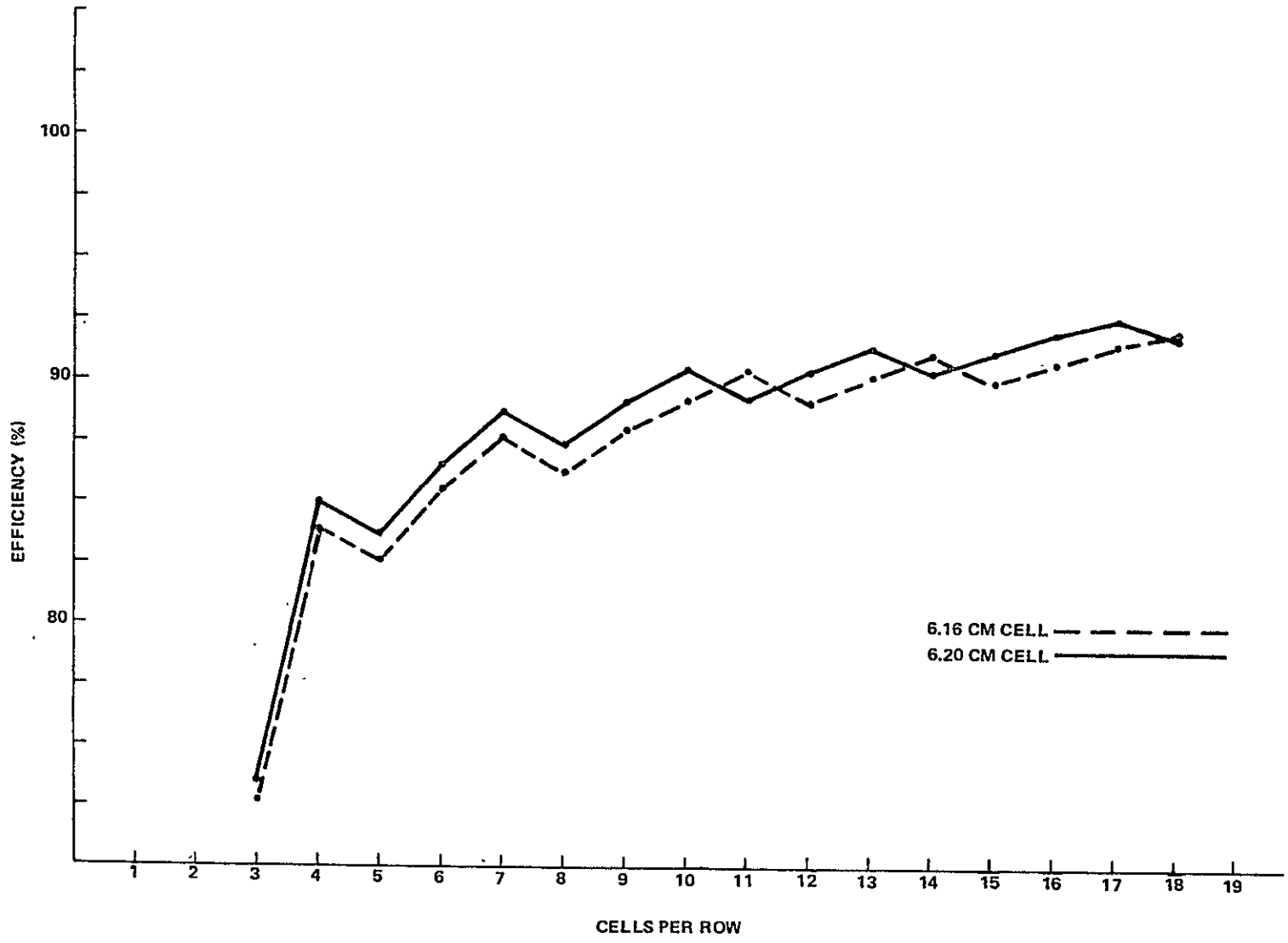


FIGURE 10. PACKING EFFICIENCY COMPARISON - 6.16 and 6.2-cm CELLS

cost of the silicon is brought down to the level of module add-on costs per peak watt, the size of modified square cut from the wafer can be optimized. Figure 11 shows the results of optimization of the cell size cut from a 7.62 cm diameter wafer and used in the 66.4 cm X 121.6 cm module. The horizontal axis shows the edge of the modified square in centimeters. The vertical axis shows the silicon usage efficiency η_{SI}, the packing efficiency η_p and their product. The silicon usage efficiency decreases with the decreasing size of the square while the packing efficiency increases discontinuously due to the mismatch between the size of the cell array and the module. The unweighted product of the silicon usage and packing efficiency as a function of the dimension of the square cell represents the optimization value for the case where the silicon solar cell and the module add-on cost per peak watt are equal.

At the point where the product η_{SI} X η_p is at maximum, minimum overall cost is achieved - at 6.9 cm for a 66.37 cm X 121.62 cm module. If the add-on cost of the module increases in relation to the cell the optimum point will move toward the full square cell. With increasing cost of silicon solar cells in relation to the add-on cost of the module, the optimum cell dimension will move toward the full round cell. Obviously, the optimization is applicable only to the point where a full square has been achieved (5.4 cm).

Tables 14 and 15 display packing efficiency calculations based on various module widths with a constant module length. Excess width generated by cumulative mismatch between overall cell width and JPL module width was included in the "border efficiency" calculation.

As expected with rectangular or square cells, the nesting efficiency is 100%. At this time square cells with rounded corners were not taken into account. The interconnect area efficiency calculated for TJC's remained constant at 96.8% because it is assumed that there will be all back side connections and the spacing between the cells remains constant. As the module area increases so does the bus area efficiency, because the bus area is independent of module size. In Table 15 cell efficiency is assumed to be 20%. Optical transmission is based on water-white crystal glass with a transmittance value of 91%. Transmittance of 95% and 98% are also used to demonstrate the effect of antireflecting coatings. PRO (Pessimistic, Realistic, Optimistic) calculations were made for module efficiencies based on existing information. These calculations do not include cell mismatch or NOCT efficiencies since these values are not yet defined for the tandem junction cell.

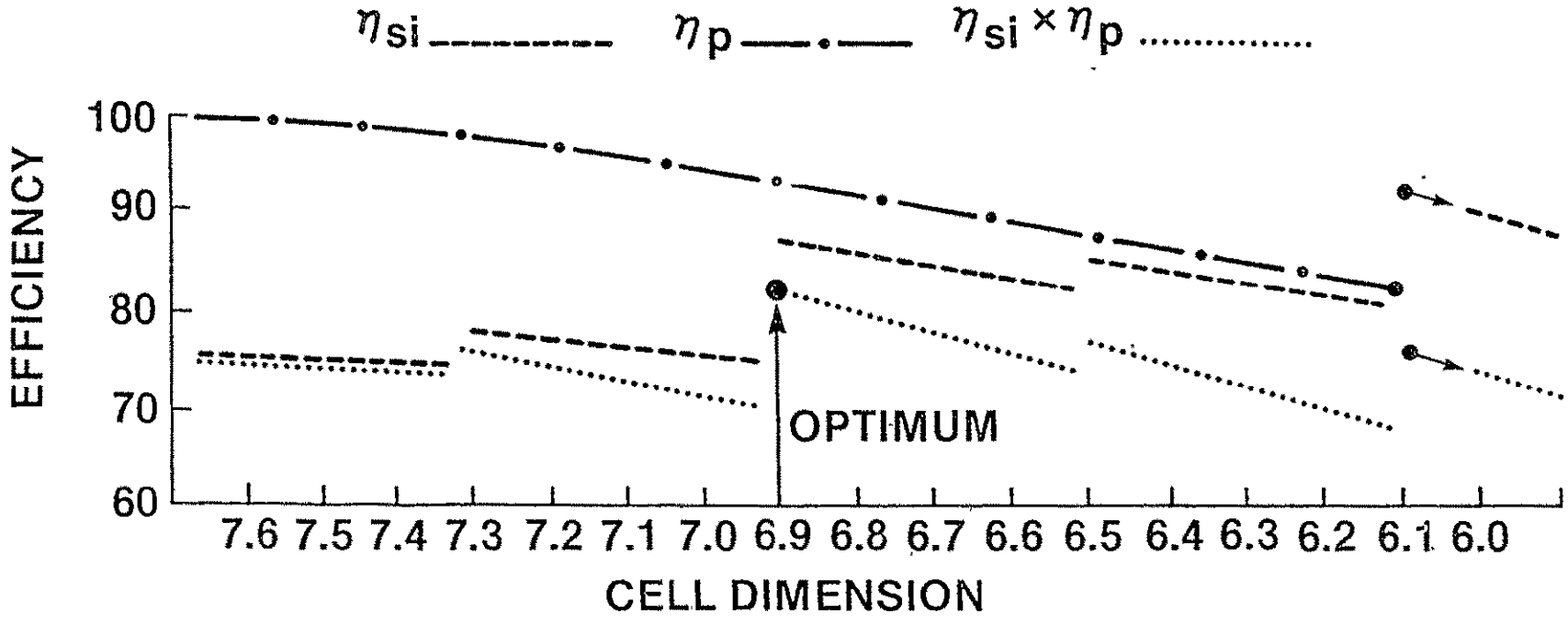


FIGURE 11. PACKING EFFICIENCY AND SILICON USEAGE EFFICIENCY OF VARIOUS SQUARE CELL DIMENSIONS AS CUT FROM A 7.62 cm ROUND WAFER AND PLACED ON A FIXED MODULE 66.37 cm × 121.62 cm.

The module length constraints listed in Table 14 show an excess of 0.78 cm on the overall length of the module. This excess length was proportionately added to each cell to arrive at a 6.2 cm by 6.2 cm cell. Efficiencies were recalculated using a 6.2 X 6.2 cm cell and the new values are shown in Tables 16 and 17.

It should be clarified at this point that the recommended JPL dimensions were used in all calculations to maintain continuity with JPL. In other than JPL test stations, modules would be designed using an optimized cell manufacturing process, and then, the encapsulation would be optimized to fit the cells. Similarly, an optimum cell size can be calculated for a given module. Silicon sheet material could be specified as a function of module dimensions.

Figure 8, 9 and 10 are a graphical presentation of packing efficiencies using 6.16 cm cells, 6.20 cm cells, and a comparison of the two respectively.

A 1.3% increase in unit cell area results in a 1.3% decrease in the number of modules required for a given power output. For example, a 0.807 m^2 module with 17% efficiency will supply 124.16 watts with a 6.2 cm cell against 122.56 watts with a 6.16 cm cell and result in an annual requirement of 80,542 modules versus 81,593 modules for a 10 MW facility; a reduction of 1051 modules annually. Some annual savings would be as follows:

	POUNDS	DOLLARS
Steel	24,990	5372.25
Glass	17,182	4030.44

Plus related manufacturing costs.

The smaller the module, the higher the ratio of bus and border to total module area. This shows up dramatically in the plots where bus and border efficiencies drop significantly as the number of columns is decreased. Consequently, desired packing efficiencies can only be achieved with 2' X 4' modules or larger.

Submodule sizes of 34.60 cm X 40.34 were manufactured to incorporate a 6X5 matrix of 6.20 square cells. Three submodules could be mounted on a rack to form a 121.62 cm long module. The rack will increase the overall module width to the JPL dimension of 35.89 cm.

1. SUBSTRATE

Porcelainized steel was chosen as the best candidate for the module substrate. Steel is inexpensive, readily available, non-strategic, a good thermal conductor, strong, and easily formed to accommodate solar cells with back-side contact configurations or front and back contact configurations. Porcelainizing the steel makes it an extremely good electrical insulator and gives the steel twenty year life in an uncontrolled environment.

It is intended that the steel sheet be drawn into the desired shape. Soft tooling was manufactured and used in conjunction with a 75 ton press to form substrates for mini modules. See Figures 12 and 13. Dimensions of the module were set at 35.56 cm X 41.28 cm (14" X 16.25"). A one-half inch (1.27 cm) raised border around the substrate allows sufficient recess for the cells and front bus bar clearance under the glass cover. The six depressions on the substrate accommodate the backside bus bars for each of the six parallel rows. The sides of the substrate were turned down to provide strength and receivers for the snap tabs on the lock frame.

The covers were welded since we did not have the precision dies and press capacity to deep draw the substrate.

2. LOCK FRAME

Porcelainized steel was also chosen for the lock frame. See Figures 14 and 15. The object of the lock frame was to maintain the integrity of the seal between the glass cover and procelainized substrate. The steel was sheared to 5.08 cm X 153.68 cm and then box braked into an angle along its length. Ninety degree (90°) "V" cuts were made at the appropriate corners and the steel was then bent into a "picture frame" configuration. Resulting seams were welded and ground. A tool was designed to form the snap tabs which are located on the sides of the lock frame. These snap tabs match the receivers located on the substrate. Twenty (20) gage (0.0359") steel was used for both the lock frame and the substrate.

The substrates and lock frames were then sent to Ervite Corporation of Erie, Pennsylvania for porcelainizing.

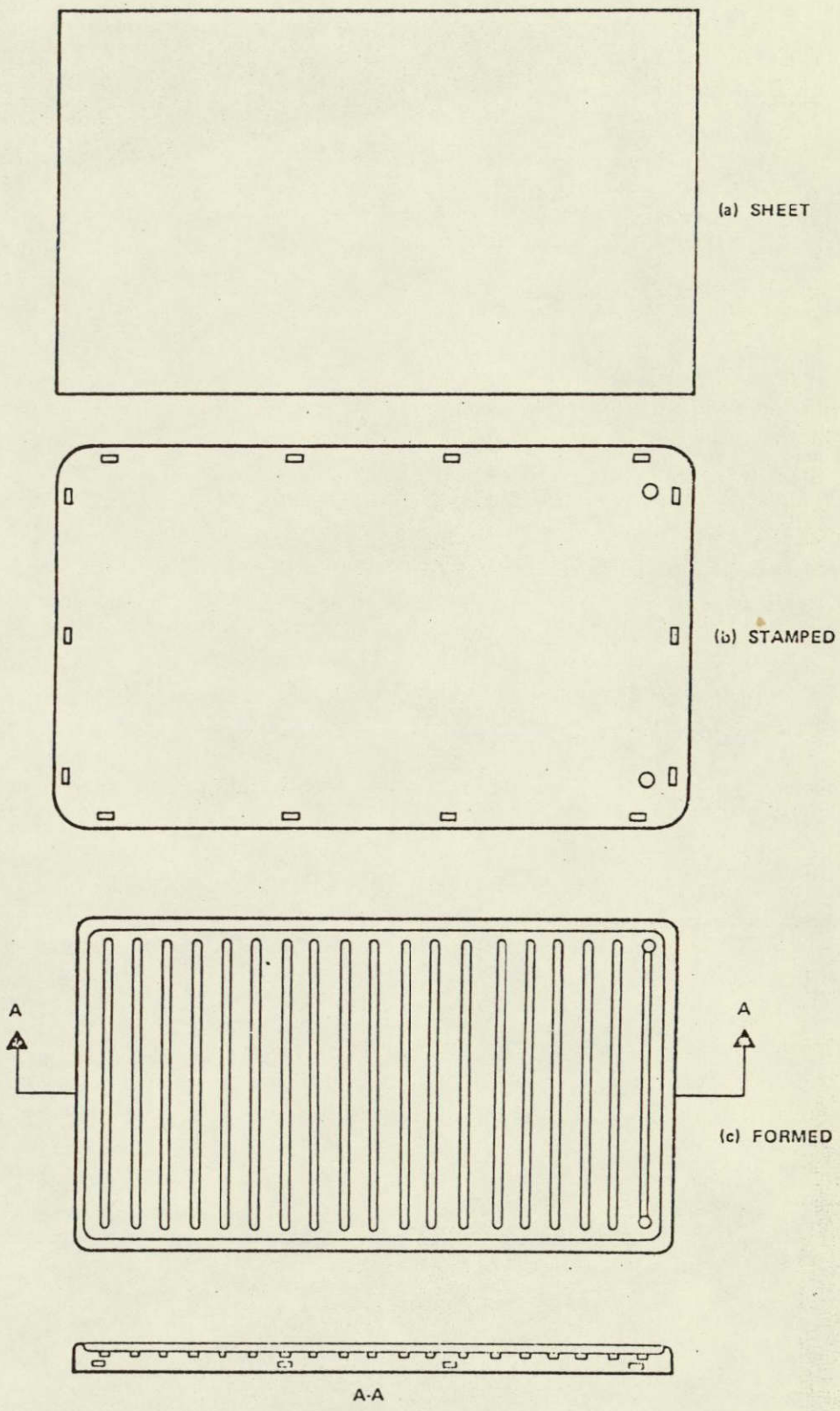


FIGURE 12. SUBSTRATE

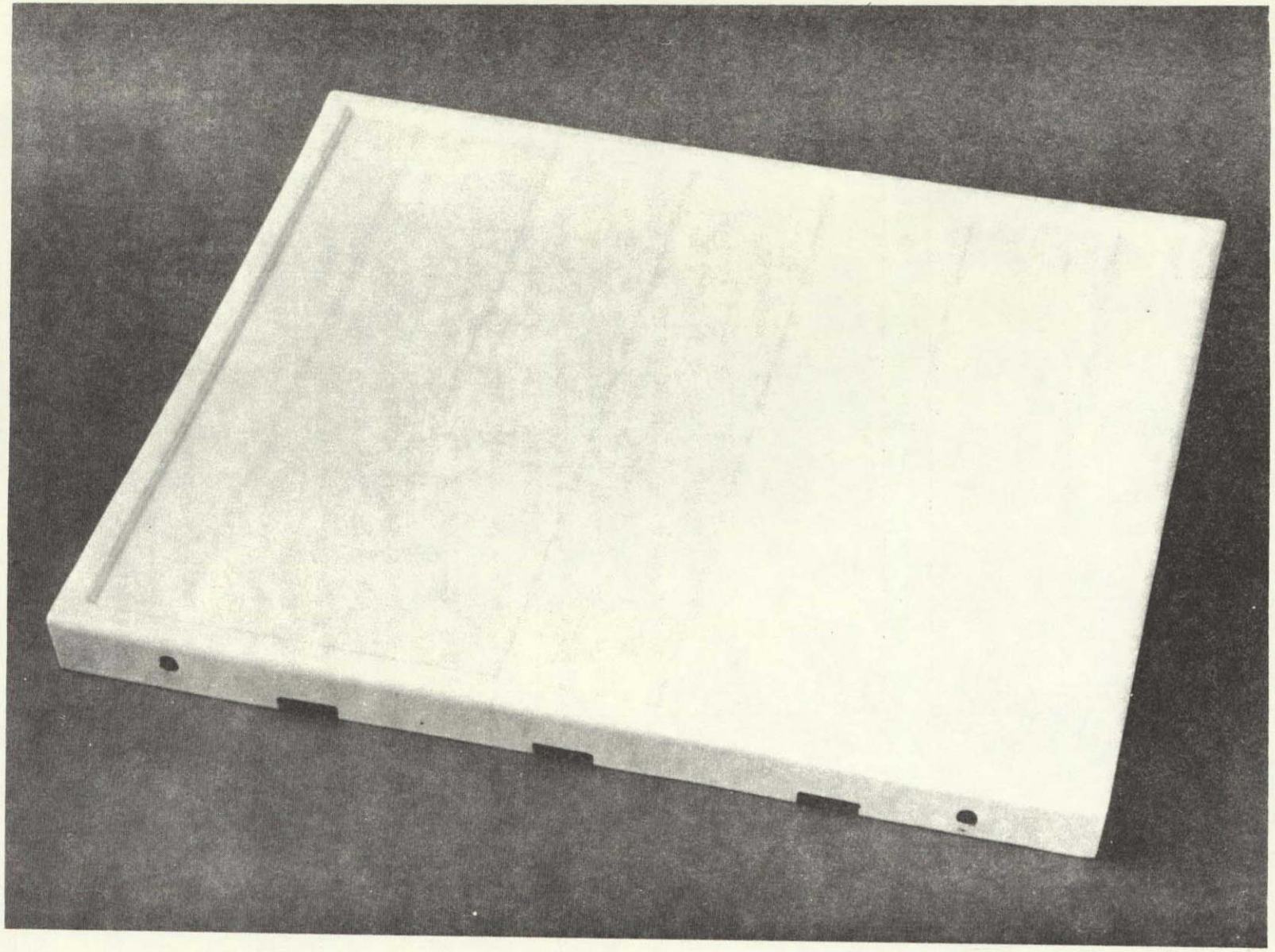
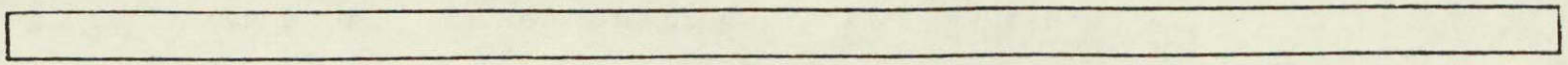
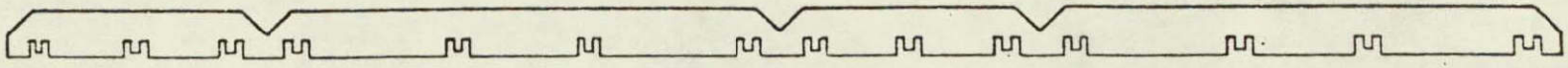


FIGURE 13. PORCELAINIZED STEEL SUBSTRATE

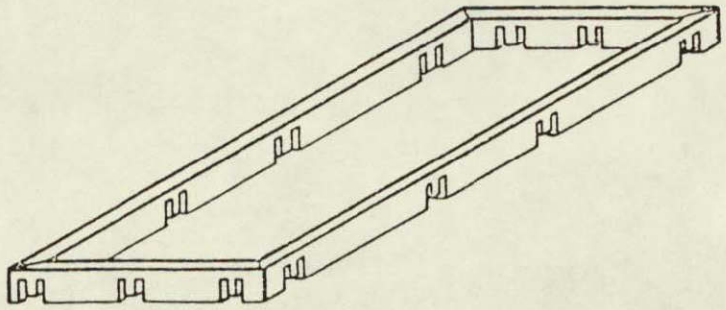
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(a) AS SLIT



(b) NOTCHED AND CUT TO LENGTH



(c) FORMED AND WELDED

FIGURE 14. LOCK FRAME

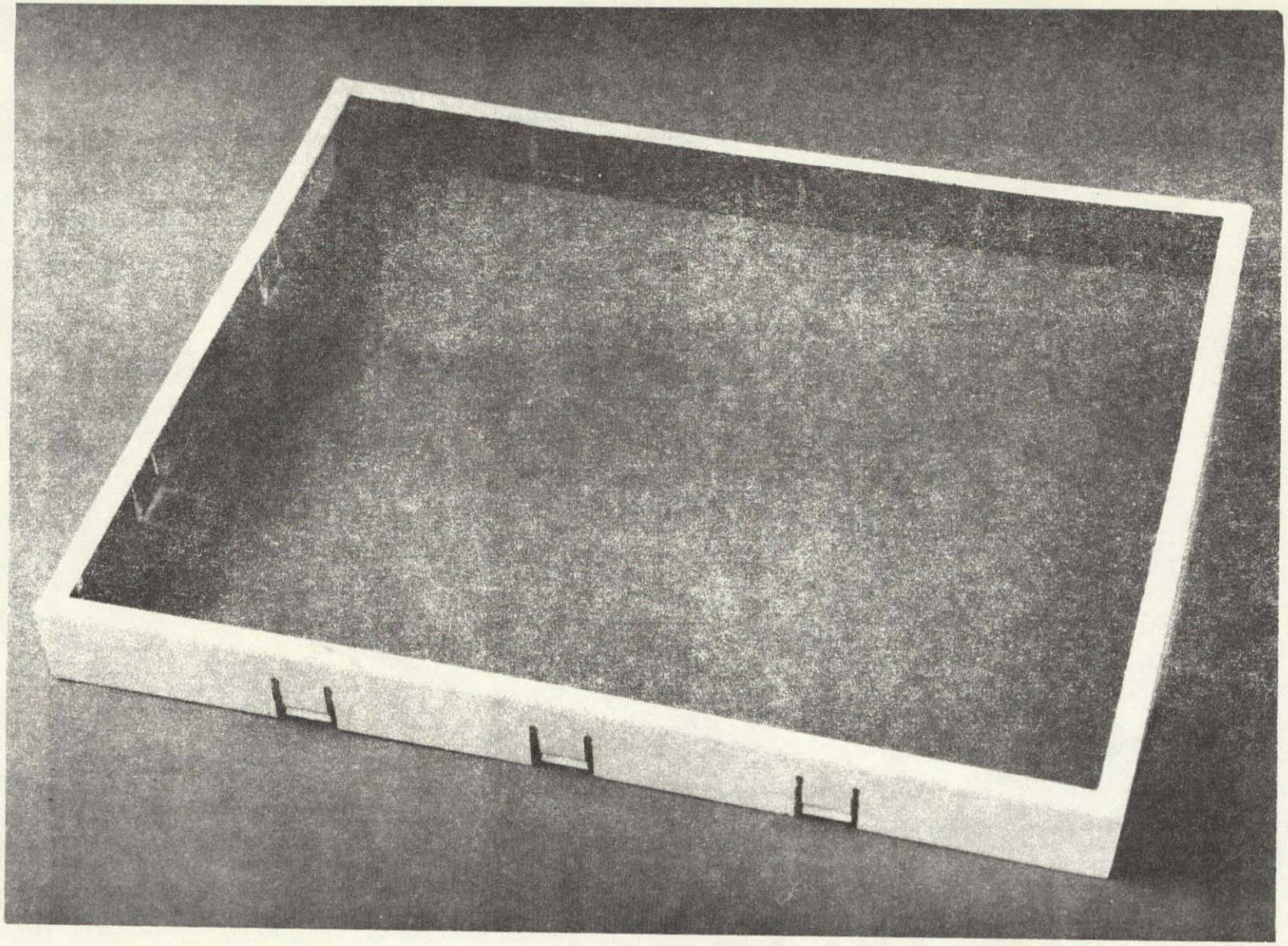


FIGURE 15. PORCELAINIZED STEEL LOCK FRAME

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3. PORCELAIN-ENAMEL

Porcelain enamel is an inorganic finish which is fused to the steel at temperatures ranging from 900°F to 1800°F. This process created a number of problems which were identified and addressed.

Six substrates and lock frames were fabricated to evaluate design, handling, and potential problems associated with processing. Previous substrates had been formed with 18-gauge (0.0478-inch, 1.21 mm) steel using the soft die. The surface of the substrate designed to accept the cells row mounting was convexed (bowed) by 0.040 inch to 0.050 inch (1.02-1.27 mm). After porcelainizing, convexity increased to 0.0938 inch (2.38 mm), making the substrates useless for cell mounting. With properly designed hardened dies, the substrates could have been made at this gauge. Design reviews, however, concluded that 18-gauge material was heavier than required for a substrate. Six substrates were formed from 20 gauge (0.0359 inch, 0.91 mm) using the soft die. Coarse measurements indicate that there is an increase in the depth of the substrate recess area from 0.150 inch (3.81 mm) at the peripheral boss area to 0.200 inch (5.08 mm) approximately one to 1.5 inches into the recess area. The remainder of the recess area is flat at 0.200 inch (5.08 mm).

The embossing set up unequal stresses in the substrate which caused some "oil can" effect during the firing process. The substrates will subsequently have to be stress relieved prior to procelainizing. The spring tabs on the lock frames also lost their temper during firing but the rigidity of the porcelain enamel was an off-setting factor. A satisfactory mating of the lock frame and substrate was achieved.

4. GLASS COVER

Regular window glass was used for module development. Glass was chosen as the module cover because of its strength, good transmission characteristics, wear and impact resistance, resistance to ultraviolet breakdown, and ease of cleaning.

5. CELLS

Cell design and sizing are explained in detail in earlier sections of this report.

6. CELL INTERCONNECT

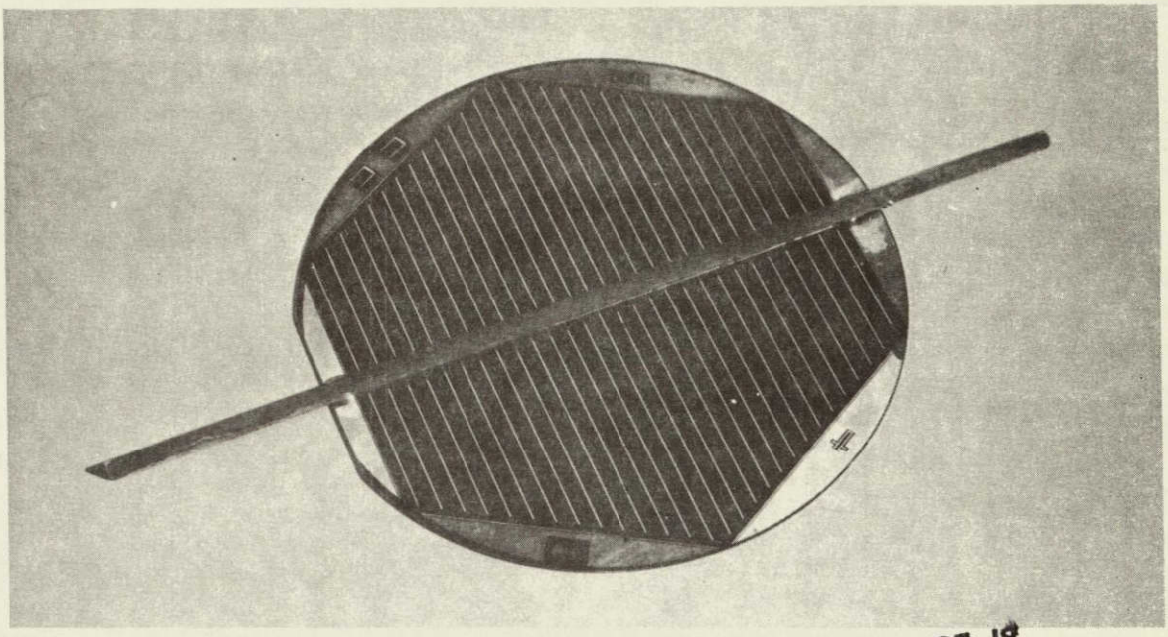
Condensation/Vapor Phase Reflow Soldering was selected as the best method for soldering interconnections to the cells. Condensation/vapor-phase reflow soldering is a process which uses the latent heat of a hot condensing saturated vapor on an assembly to provide precise temperature control and high heat transfer rates for soldering assemblies[5]. The vapor is produced by boiling a suitable inert fluid at atmospheric pressure.

Front bus bars of triangular cross section were soldered to 12 cells using various soldering conditions. These conditions included pretinned bus bars, solder preforms with untinned bus bars and combinations of both. Visual appearances are very good. Figure 16a shows a section of a triangular bus bar soldered to the front of a hexagonal solar cell (the cell is not scribed from the round wafer). Figure 16b shows a close-up, from the top, of the bus bar attachment. These bus bars used Cu/Alloy 42 (Invar was not available at that time) which does not match the thermal expansion coefficient of silicon as well as Cu/Invar. No thermal shock was observed during soldering. One assembly was cycled (725 cycles) from -40°C to +90°C with no apparent ill effect. Metallurgical cross-sectioning of the solder joint shows a very uniform solder joint with no voids. A multicell condensation soldering fixture was completed and evaluated.

The multicell soldering fixture was designed to solder a cell string consisting of five cells in parallel. Cycle time for soldering a five-cell string was ultimately cut to ten minutes. Since actual soldering takes only 25 seconds it is evident that fixturing of the cells, solder, and bus bars is a fairly tedious manual operation.

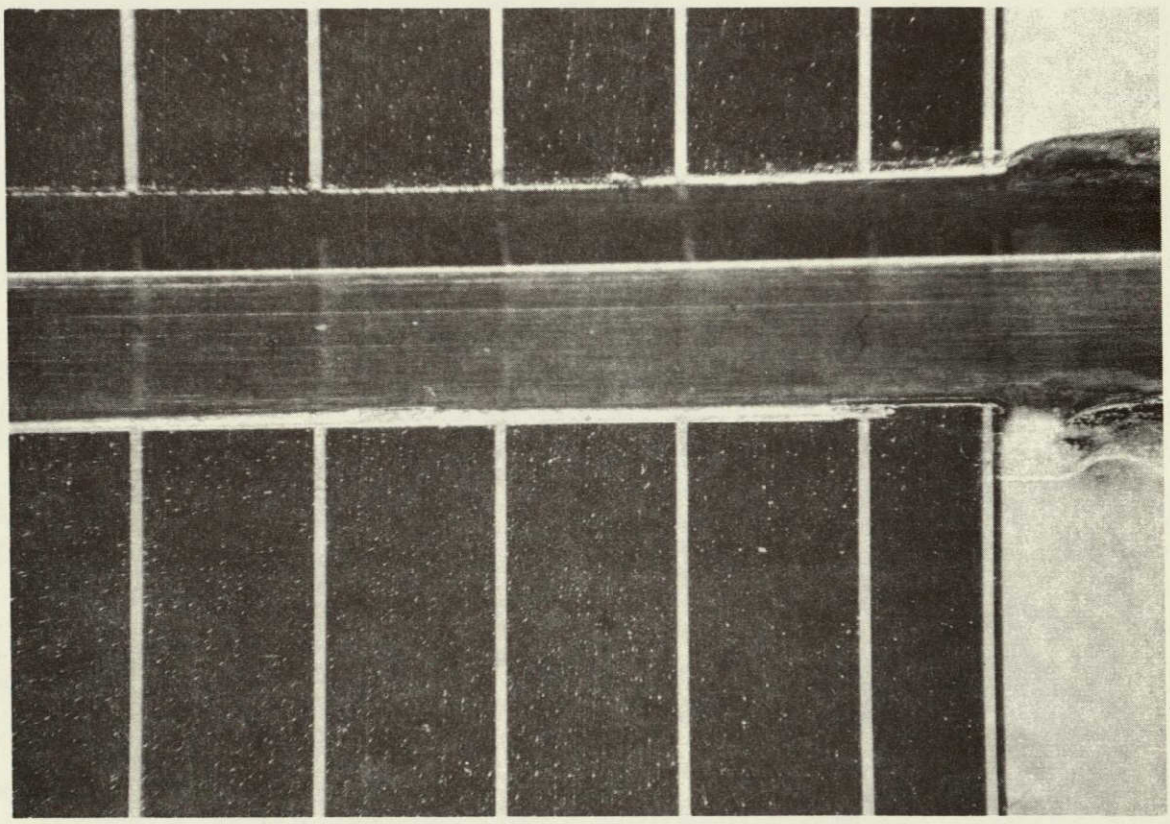
The vapor temperature remains constant at 419°F (215°C) so a eutectic solder was used. All condensation soldering was done at Hybrid Technology Corporation in Concord, Massachusetts.

After the cell strings were completed six of each were then hand soldered in series to form a 6X5 cell matrix. The top bus bar at each end of the string was soldered to each end of the bottom bus bar on the adjacent string for redundancy and to minimize the I^2R loss. The matrix was then ready for mounting to the substrate.



(a) TOTAL ASSEMBLY

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(b) TOP VIEW, CLOSE-UP OF TRIANGULAR BUS BAR ON THE SOLAR CELL

FIGURE 16. TRIANGULAR BUS BAR SOLDERED TO SOLAR CELL

7. FRONT AND BACK CONDUCTORS

The conductors are soldered directly across the front and the back of the silicon solar cells. In both cases a good electrical conductivity is required to minimize the I^2R losses and the coefficient of thermal expansion of the conductor cannot differ too significantly from that of silicon, $\alpha_{Si}=2.33 \times 10^{-6}$ cm/cm/°C. Conductor material should be easy to solder. None of the monolithic metals or alloy meet these requirements. However, composite metal technology can be used to manufacture material systems to meet the requirements. For this application the best choice, from the standpoint of manufacturability and cost, is copper-clad Invar.

The coefficient of the thermal expansion of two layer composite metal, parallel to the layers can be calculated from the approximate equation

$$\alpha_c = \alpha_1 + \frac{A_2E_2}{A_1E_1} \times \alpha_2 \qquad (1)$$

in which

α_1 = coefficient of thermal expansion of the material with lower alpha
α_2 = coefficient of thermal expansion of the material with higher alpha
A_1 and A_2 are cross sectional areas of the component layers
E_1 and E_2 are moduli of elasticity of component metals.

Similarly the resistance per unit of length of the composite metal conductors can be calculated parallel to the layers from the parallel circuit equation.

$$\frac{1}{R_c} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \cdots\cdots\cdots\cdots \qquad (2)$$

Where R_1, R_2 and R_3 are the respective resistance of the composite metal layers per unit length.

The conductors were dimensioned by permitting a certain I^2R loss per row. For the calculations it was assumed that current pickup was constant per unit length of the conductor, Figure 17.

FRONT AND BACK CONDUCTORS (cont'd)

The apparent coefficient of thermal expansion of the composite metal conductor is calculated from equation (1).

$$\alpha_c = \alpha_1 + K\alpha_2$$

in which $K = A_2E_2/A_1E_1$ and

$\alpha_1 = \alpha_{Invar} = 1.5 \times 10^{-6}$ cm/cm/°C

$\alpha_2 = \alpha_{Cu} = 16.5 \times 10^{-6}$ cm/cm/°C

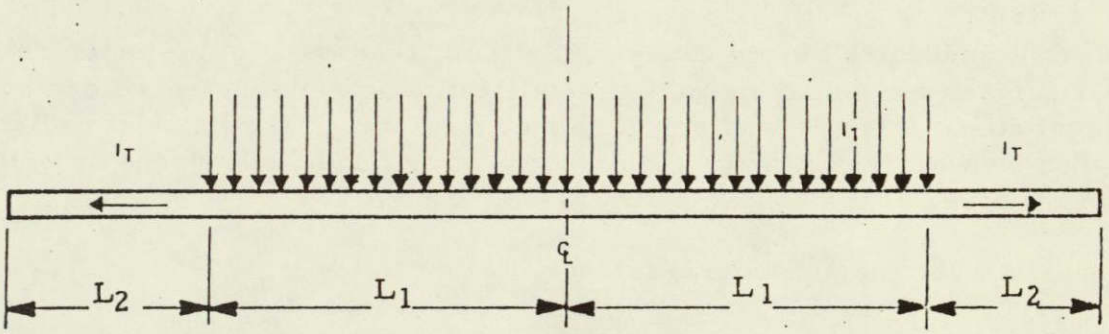
$E_1 = E_{Invar} = 21.4 \times 10^6$ lb/in^2

$E_2 = E_{Cu} = 16.0 \times 10^6$ lb/in^2

$A_1 = 0.75\ A$

$A_2 = 0.25\ A$

$\alpha_c = 5.7 \times 10^{-6}$ cm/cm°C



L_1 = LENGTH TO WHICH SILICON SOLAR CELLS ARE SOLDERED

L_2 = AVERAGE TERMINATION LENGTH OUTSIDE OF THE CELLS

I_1 = CURRENT PICKUP A/CM

I_T = TOTAL CURRENT FOR HALF LENGTH OF CONDUCTION = $L_1 \times I_1$

FIGURE 17. SCHEMATIC OF MODULE INTERCONNECTS

FRONT AND BACK CONDUCTORS (cont'd)

For the length L_1 the I^2R losses can be can be calculated from equation (3).

$$\Delta P = \int_0^{L} (I_1 x)^2 R_c \, dx$$

$$\Delta P = \frac{1}{3} I_L^2 R_c L_1^3$$

The total I^2R losses are then

$$\Delta P_T = \frac{1}{3} I_L^2 R_c L_1^3 + I_T^2 R_c L_2 \qquad (3)$$

Assigning a specific value e.g. 2%, for the loss component ΔP, the necessary cross sections of the conductors can be calculated.

The required cross section of the composite metal conduction for the mini module with five cells in parallel is given as follows:

Cell Output In Amps	Area for Each Bus Bar (cm^2)
.75	0.015
1.00	0.030
1.25	0.046

The front conductor should cause a minimum shadowing of the solar cell and offer a flat surface for soldering to the metallization pattern on the silicon solar cell. An equilateral triangle was selected because some of the incident radiation, blocked by the base of the triangular conductor can be recovered by reflection from the sides of the conductor to the cell surface.

Dimensions for the equilateral triangle are as follows:

Cell Output In Amps	Area for Each Bus Bar (cm^2)	Equilateral Height (cm)	Triangle Base (cm)
.75	0.015	0.106	0.119
1.00	0.030	0.145	0.168
1.25	0.046	0.175	0.203

A. FRONT CONDUCTOR

Assuming transmittance for the front cover, 13.5% cell efficiency and permitting 2% I^2R loss at peak output, we obtain $R_c = 0.0001757\ \Omega/cm$ from equation (3). Twenty-five percent of the cross section of the conductor is assumed to be copper and 75% Invar. From equation (2) we obtain

$$\frac{1}{R_c} = \frac{A_1}{\rho_1} + \frac{A_2}{\rho_2} + \ldots\ldots\ldots \qquad (4)$$

in which

$A_1 = 0.25$. A for copper
$A_2 = 0.75$. A for Invar
$\rho_1 = 1.7 \times 10^{-6}\ \Omega$-cm for copper
$\rho_2 = 50 \times 10^{-6}\ \Omega$-cm for Invar

B. BACK CONDUCTOR

The width of the back conductor was selected to be 0.6 cm. The conductivity of the 60% Sn-40% Pb solder, which is used to solder the conductor to the back metallization of the silicon colar cell is taken into consideration, however, the contribution of the back metallization of the silicon solar cell is disregarded as in the previous calculations

$$\frac{1}{R} = \frac{w.t_1}{\rho_1} + \frac{w.t_2}{\rho_2} + \frac{w.t_3}{\rho_3.} \qquad (5)$$

$t_1 = 0.25\ t$ = total thickness of copper layers
$t_2 = 0.75\ t$ = thickness of Invar layer
$t_3 = 0.0125$ cm = thickness of tin-lead solder
$\rho_3 = 14.5 \times 10^{-6}\ \Omega$-cm for tin-lead solder
$R_c = 0.000189\ \Omega/cm$ for 1.5% I^2R loss

The back conductor thickness from the above equation becomes:

$$t = 0.06 \text{ cm}$$

The coefficient of the thermal expansion is the same $\alpha_c = 5.7 \times 10^{-6}$ cm/cm/°C as for the triangular front conductor, because the area ratio between the copper and Invar are the same.

8. CONDUCTOR MANUFACTURING

A. FRONT CONDUCTOR

Invar was purchased and received in 0.500" diameter wire form. It was broken down to bonding gage and then subsequently bonded with OFHC copper in our wire department.

Special rolls were designed for our Turks Head Unit which would allow us to draw round wire into a triangular cross-section.

Previous work indicated that for a full size (2' X 4') module with ten cells per string, a cross-sectional area of 0.0409 cm^2 was required, approximately an equilateral triangle with h=0.254 cm and b = 0.290 cm. These dimensions were used for determination of the optimum starting wire size to result in the desired equilateral triangle.

Starting Wire Size (cm)	No. of Passes Thru Turks Head	Triangle b (cm)	Triangle h (cm)
0.340	6	0.290	0.254
0.318	2	0.290	0.254
0.292	1	0.254	0.229
0.267	1	0.241	0.216

The 0.340 cm starting wire size required six passes through the Turks Head to achieve the required triangular cross section. Finning was also generated at each apex although it was easily removed with steel wool.

The 0.318 only required two passes through the head with only slight finning observed.

The 0.292 and 0.267 wire sizes were not large enough to fill the triangular dimensions.

B. BACK CONDUCTOR

Copper at 0.127 cm thick was rolled to 0.032 cm andannealed. Invar at 0.318 cm was rolled to 0.191 cm and annealed. This was necessary to get the materials to the proper ratio prior to bonding. The copper and Invar were then slit to 8.255 cm wide and abraded.

The combination was bonded, annealed, and rolled to 0.06 cm and sheared to 0.6 cm and 0.3 cm widths by 31.75 cm in length.

9. ASSEMBLY

A small drop of RTV was placed on the back side of each cell in the 6X5 cell matrix. The cell matrix was then positioned on the porcelainized steel substrate and connected electrically with the feed-throughs.

A small RTV bead was laid around the periphery of the glass 3/8" of an inch in from the edge. After curing, the glass was placed on the substrate with the RTV gasket in contact with the matching raised area on the substrate. The purpose of this gasket was to act as a dam for the polysulfide seal. EC801 was the polysulfide used for final sealing. It was applied using an automatic dispensing unit and it filled the cavity from the RTV gasket out to the edge of the module. A twenty-four hour curing cycle at 120°F was followed by liquid filling.

Liquid filling was chosen instead of a gel pottant for a number of reasons. Gels inherently are associated with delamination at cell interfaces, interconnect areas, or along module borders. Gels are not as easy to work with. The major disadvantage of a liquid results when the seal integrity is violated or the glass cover breaks.

The liquid chosen was a Union Carbide Silicone Fluid (L-45). L-45 has excellent mechanical properties, resist breakdown by shear, is compressible, and highly efficient at dampening vibrations. It is available in high purity, for electrical use, which has high resistance to breakdown by voltage, exceptional insulation quality and resistivity, and very low electrical losses. Union Carbide L-45 silicone dielectrics are used in AC and DC circuitry.

Liquid filling was accomplished using the automatic dispensing unit. The seal on the module was punctured with a needle from the dispensing unit and then filled. Another approach was also to leave a section of seal uncompleted, fill the module cavity using an ordinary oil can, and then finish the seal.

After liquid-filling and curing of the gating seal,the lock frame was snapped into position. Figure 18 shows a photograph of a mock up of the module with cells in position but without copper-Invar bus bars.

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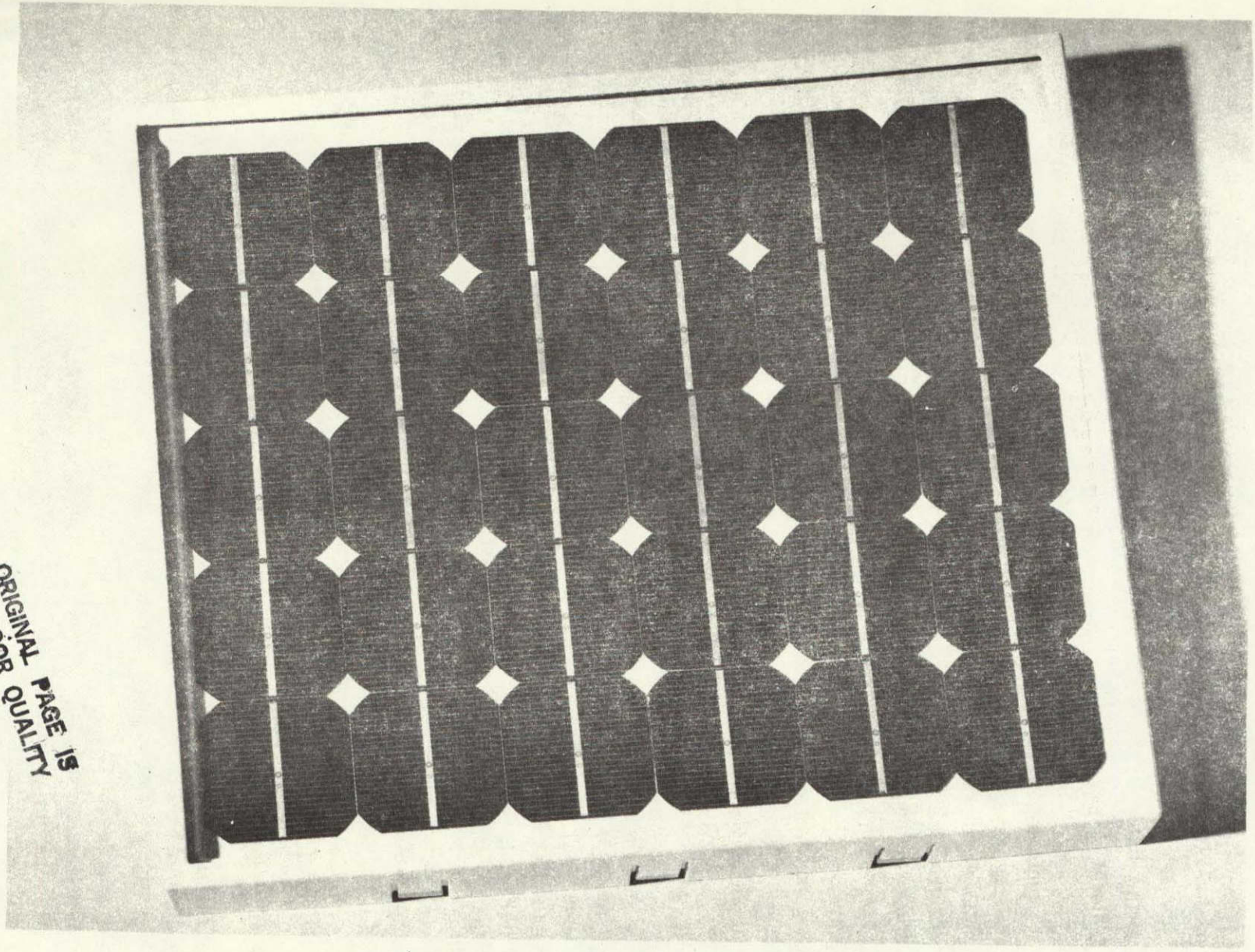


FIGURE 18. MOCK-UP OF TEST MODULE

10. TESTING

Metallographic

Metallagraphic cross-sections were prepared for samples from condensation soldering. One hundred percent bond integrity was achieved.

Thermal Cycling

Two Tenny Jr. chambers are presently being used to cycle small components and subassemblies from -40°C to +90°C every six hours. One bus bar and cell assembly has cycled over 750 times with no visible degradation of bond integrity.

Environmental

Two mini-modules were placed on the roof to cycle naturally. Both modules incorporated thermal collectors for heat generation instead of solar cells. One module consisted of a porcelainized steel substrate with a glass cover and no potting medium. The second module was the same as the first with the only difference being that the second was liquid filled. Both modules incorporated an EC801 polysulfide gasket material from 3M. The temperature of the liquid filled module at peak intensity was approximately 25°F less than the module with the air void.

Optical Characteristics

Optical transmission characteristics were evaluated on polyethylene glycol, demiethyl silicones, and polyalkylene glycols as identified below:

Polyethylene glycol	----	Carbowax 200
Polyalkylene glycol	----	LB65
		LB70X
		LB385
		LB400X
Demiethyl silicone	----	L45 (four viscosities)
		50 Cstk 2000 Cstk
		500 Cstk 10000 Cstk

Results are shown in Figure 19.

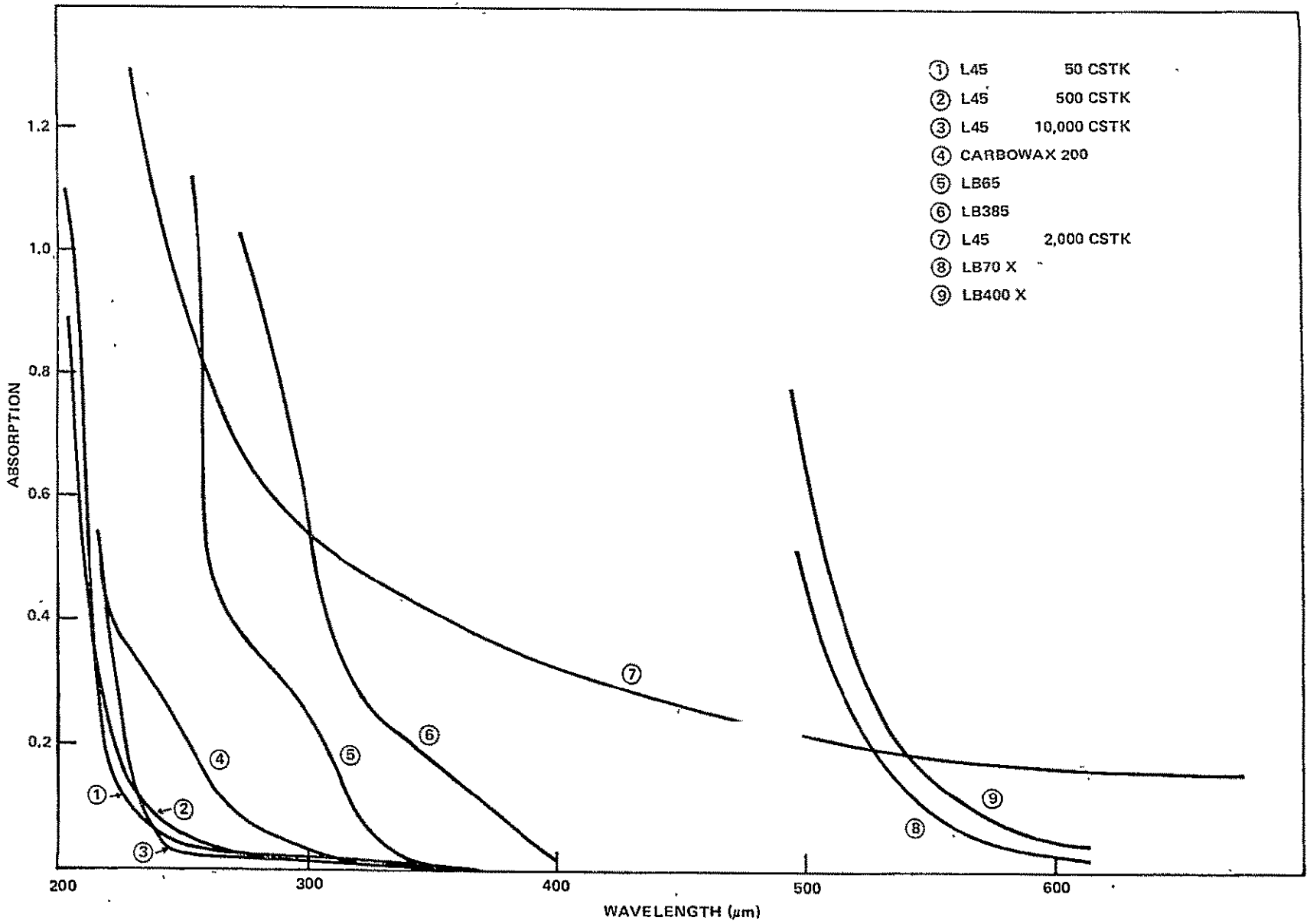


FIGURE 19. OPTICAL TRANSMISSION CHARACTERISTICS OF VARIOUS LIQUIDS

11. COST DATA

Material costs in 1978 dollars for a 0.664m X 1.216m module having a total area of 0.807m^2 and a module efficiency of 13% (105 watts) are given in Table 18.

TABLE 18. MODULE MATERIAL COSTS

	WEIGHT (lbs)	COST ($)	$/W 105W (13%)
Substrate	15.94	3.28	0.031
Lock Frame	2.53	.49	0.005
Porcelain-Enamel	2.17	1.52	0.014
Glass	20.94	3.84	0.037
Front Bus	1.07	3.82	0.036
Back Bus	1.07	3.05	0.029
RTV Adhesive/ Sealant	.10	.62	0.006
EC801	.10	1.60	0.015
Connectors	.10	.70	0.007
Liquid Pottant	.25	1.47	0.014
TOTAL	44.27	20.39	0.194

Detailed module design versus cost reviews continued to identify areas of cost reduction in the module fabrication area. Prior analysis points to a packing efficiency in excess of 90% for module sizes 0.664m by 1.21m or greater. Using this module size, Table 19 was generated for a 10MW facility. The data is plotted in Figure 20 to show the cumulative effect of material, labor (including OH), depreciation and factory OH. At all module efficiencies, material is the dominant cost factor in the present design. No material substitutions are available at this time that can provide the 20-year lifetime goal. Unique design characteristics are being continuously evaluated to identify areas for material cost reductions.

TABLE 19. $/W AS A FUNCTION OF VARIOUS EFFICIENCIES

Module Efficiency	Watts Per Module	Modules Per 10 MW	Material	Labor	Depreciation	Factory OH	Total
10	80.7	126,445	0.253	0.111	0.028	0.022	0.413
13	105	96,689	0.194	0.090	0.028	0.018	0.330
16	129	78,579	0.158	0.073	0.028	0.015	0.274
19	153	66,607	0.133	0.059	0.028	0.013	0.233
22	177	57,651	0.115	0.048	0.028	0.011	0.202

Module Size = 0.664m X 1.216m

Module Area = 0.807m^2

Total Module Cost - $20.39 (excluding cells)

1978 Dollars

Immediate cost reductions can be seen in the lock frame and the bus bar. The lock frame can be eliminated altogether while the cost of the bus bar can be cut in half through redesign and elimination of the Invar.

The effects of these cost reductions are as follows:

	Weight	Cost	$/Watt 13% (105W)
From Table 18	44.27	20.39	0.194
No Lock Frame	(2.53)	(.49)	(0.005)
No Invar	(1.07)	(3.43)	(0.033)
Total	40.67	16.47	0.156

Table 19 was recalculated using these cost reductions. The data is given in Table 20.

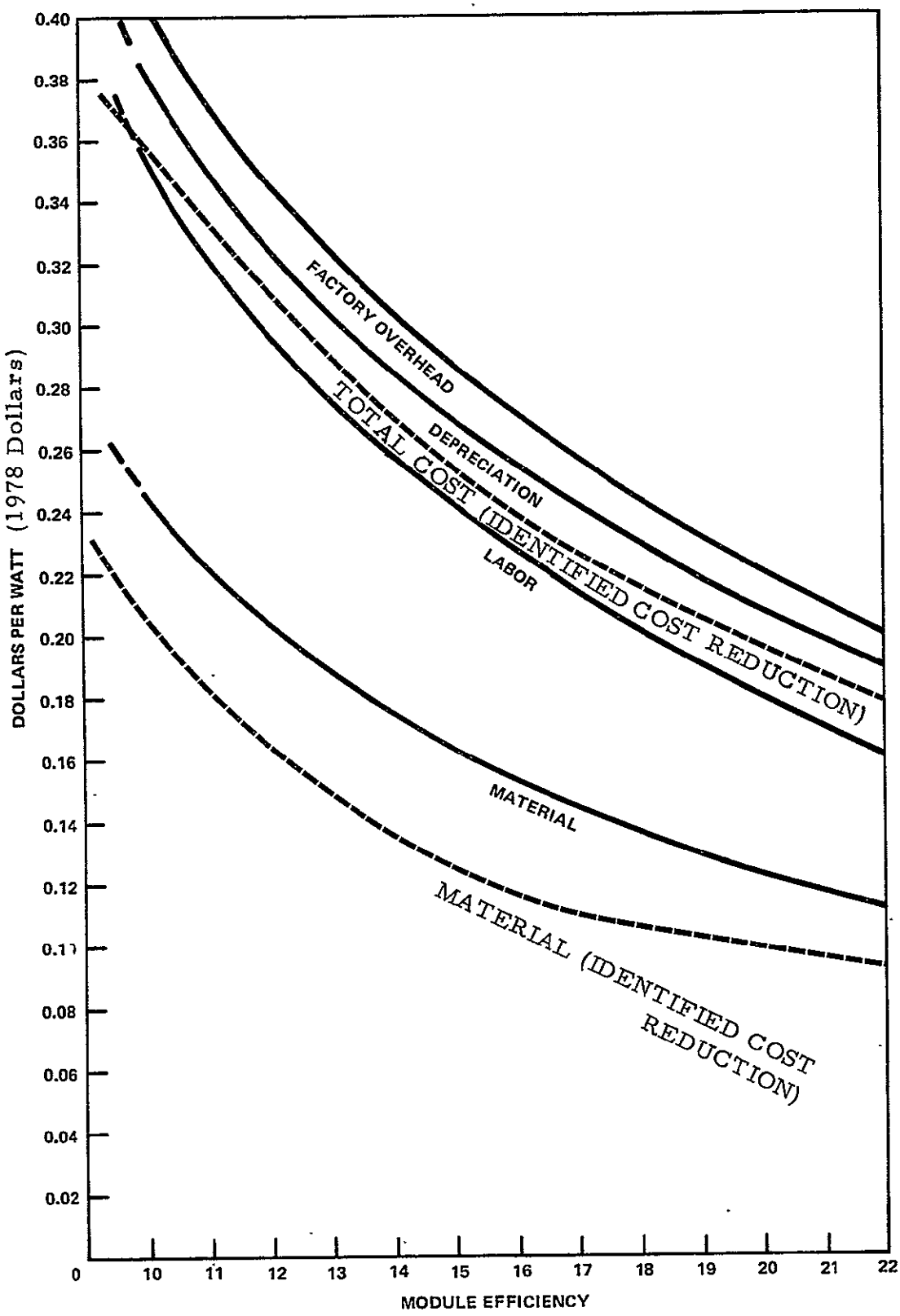


FIGURE 20. MODULE COSTS AS A FUNCTION OF MODULE EFFICIENCY

TABLE 20 $/W AS A FUNCTION OF VARIOUS EFFICIENCIES

Module Efficiency	Watts per Module	Module per 10MW	Material	Labor	Depreciation	Factory OH	Total
10	80.7	126,445	0.204	0.111	0.028	0.022	0.365
13	105	96,689	0.157	0.090	0.028	0.018	0.293
16	129	78,579	0.128	0.073	0.028	0.015	0.244
19	153	66,607	0.108	0.059	0.028	0.013	0.208
22	177	57,651	0.093	0.048	0.028	0.011	0.180

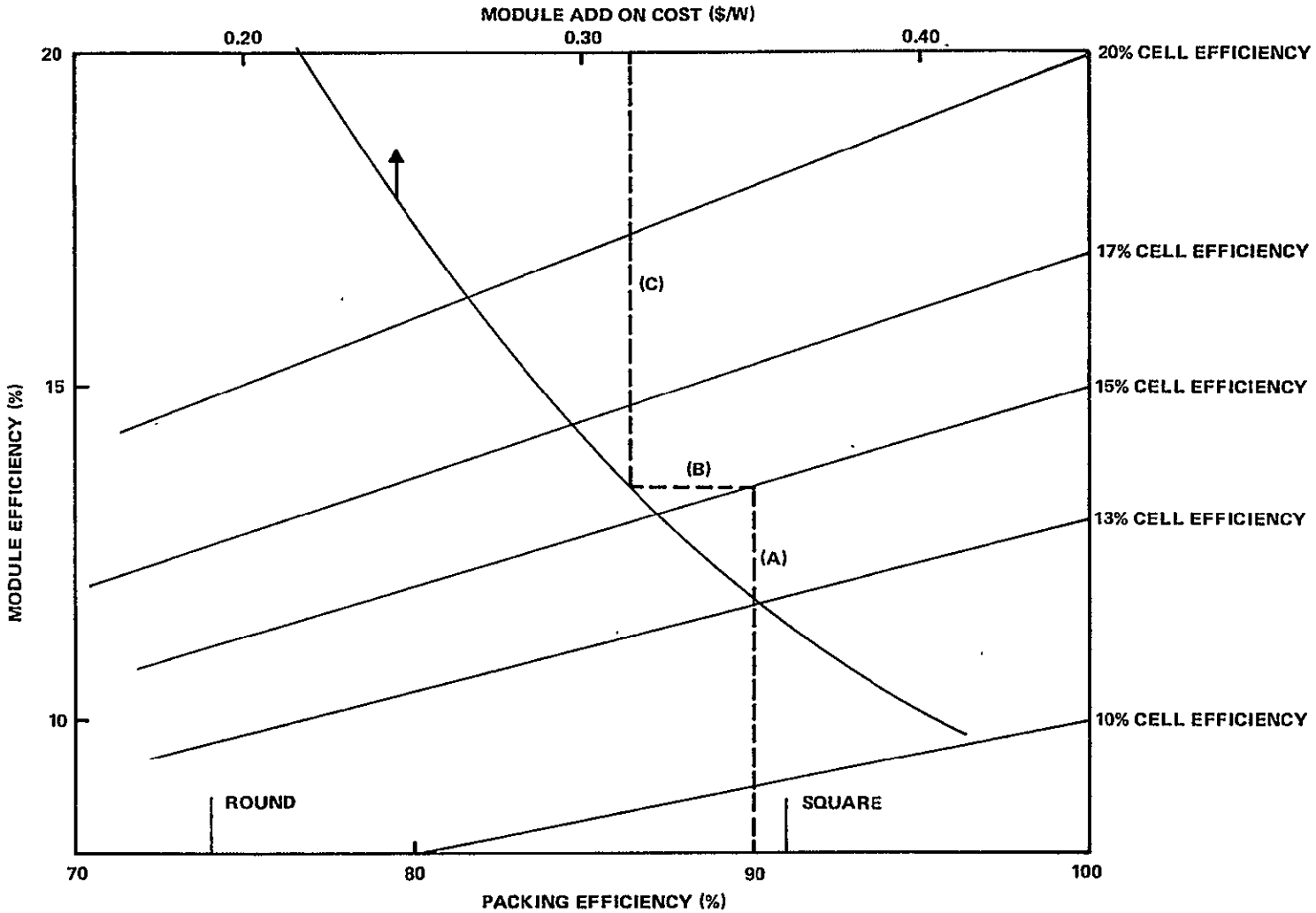
Module Size = 0.664m X 1.216m

Module Area= 0.807m^2

Total Module Cost = $16.47 (excluding cells)

1978 Dollars

From the data in Table 19 relating module add-on cost ($/W) as a function of various module efficiencies, a correlation can be drawn between cell efficiency, packing efficiency and module add-on cost. Figure 21 is a plot of module efficiency versus packing efficiency for various cell efficiencies and versus module add-on cost ($/W). This particular figure is drawn for a module add-on cost of approximately $20.00 for a 0.664m X 1.216m module. The figure demonstrates the need for high efficiency in both cells and module to achieve low module add-on cost. The figure can be used as a nomograph. From the packing efficiency of the module, proceed vertically to the line for a given cell efficiency, dotted line A for 90% packing efficiency and 15% cell efficiency, to determine module efficiency, 13.5% in this case. Then proceed horizontally to the module add-on cost curve, dotted line B. From this intersection, proceed vertically to determine the module add-on cost, dotted line C, $0.314/W in this case. For this module configuration, maximum packing efficiencies for round and square cells are shown on the bottom ordinate in the Figure. As the module cost changes, the module add-on cost curve will move but the general shape of the curve is the same. This approach can be used to analyze the impact of cell efficiency on module add-on costs and for given module designs and costs, establish lower limits for acceptable cell efficiency. In this particular case, module cost is too high to meet the 1986 goal but the magnitude of the needed cost reduction can be readily established, and the need for maximum achieveable cell efficiency and module packing efficiency is obvious.



MODULE AREA = 0.807 m^2
MODULE COST = $20.00 (excluding cells)

FIGURE 21. MODULE ADD-ON COST NOMOGRAPH

12. MINI-MODULE TESTING

Seven (7) mini-modules composed of a 5 (parallel) X 6 (series) array were fabricated. All modules used the same basic construction but several experimental variations were incorporated to evaluate or verify various design parameters. All cells were fabricated using either the baseline process, Figure 6, or LCPA II, Table 6. AR coating was either $Si0_2$ or Si_xN_y. Two modules were fabricated without the lock frame, instead using only the polysulfide seal. One module used undersized bus bars to asses the impact of material saving on this item.

All modules were tested in sunlight (29 and 30 November in Dallas, Texas) at a calculated isolation of 95 - 98 mW/cm^2. Module 1 used the undersized bus bars, and $Si0_2$ as the AR coating. The impact on F. F. is due to I^2R losses in the bus bars. Module 2 had 2 cracked cells on rows 1 and 2 (due to impact on the assembled module); half of the cells had $Si0_2$ and half had Si_xN_y AR coating. The cracked cells caused the reduction in I_{sc} but did not hurt F. F. Module 3 had half $Si0_2$ and half Si_xN_y AR coating. Module 4 had Si_xN_y AR coating and the

TABLE 21. MODULE ASSEMBLY PHOTORESPONSE

Module Number	V_{oc} (V)	I_{sc} (A)	P_m (W)	F.F.
1	3.47	3.8	8.35	.63
2	3.49	3.48	9.25	.765
3	3.45	4.20	10.77	.745
4	3.49	4.47	11.33	.72
5	3.42	3.7	10.09	.79
6	3.41	4.15	10.15	.72
7	3.49	4.64	12.09	.75

cells were fabricated using LCPA II. Module 5 cells were fabricated in a diode manufacturing area and had Si_xN_y AR coating; the cause of the high F. F. and low I_{sc} are not apparent. Module 6 cells were fabricated using LCPA II and had Si_xN_y AR coating. The cell surfaces were severely stained due to using a spin-on dopant that had exceeded its shelf life (see diffusion). These cells had the widest spread in I_{sc} and the cells were sorted and each row current output was matched. The lowered I_{sc} was due to the spread of I_{sc} values among the cells. The staining did not appear to affect the dark characteristics of the cells but did act as a light filter or shadow. Module 7 cells were fabricated using LCPA II and had Si_xN_y AR coating.

Modules 1 through 6 were shipped to JPL for further testing. No further electrical or environmental testing was performed on these modules at Texas Instruments.

F. HIGH EFFICIENCY CELL DEVELOPMENT

This activity focused on the development of a novel cell structure, the Tandem Junction Cell (TJC), developed at Texas Instruments. The TJC features an all back contact cell having a textured front surface that contains an electrically floating N^+/P junction. A cross section view of the TJC, not to scale, is shown in Figure 22. The illuminated side (front) of the TJC is textured to reduce reflection and to increase the path length of the absorbed light. A shallow N^+ junction is diffused into the front surface. The thin base region, ~100 μm, is P type. The N^+ collecting junction and P^+ contact regions are formed on the back side. The N^+ and P^+ regions are in the form of an interposed finger pattern.

This solar cell structure has several very attractive built-in features. With no contact metallization on the front side, shadowing is eliminated. The back contact system is particularly useful in module assembly. All interconnects and bus bars can be located behind the solar cells and virtually no module space is wasted. The TJC appears to offer the opportunity to achieve very high efficiency for silicon solar cells.

Development work under this activity was primarily focused on improvements in the contact metallization pattern, shallow front N^+ diffusion and methods to improve V_{OC}. Included in this effort, is the effect of minority carrier lifetime and cell thickness. At the beginning of this program, 2 x 2 cm TJC's with AM 1 efficiency in the 10-12% range had been fabricated.

1. BACKGROUND

At the start of this program an experimental TJC mask set was available that had two cell sizes, 1 x 1 cm and 2 x 2 cm, each with eight (8) N^+ contact fingers per cell. TJC's were fabricated on 3 Ω-cm material. These cells had N^+ diffused layers on both sides, ~0.3 μm, and a $Si0_2$ AR coating on the front. The cells were 110 μm thick. Sample TJC's were submitted to JPL and to NASA-Lewis for photoresponse measurements. Photoresponse data is shown in Table 22. Several features are nonoptimum, the AR coating has a low refractive index and the finger spacing is too wide for the 3 Ω-cm material.

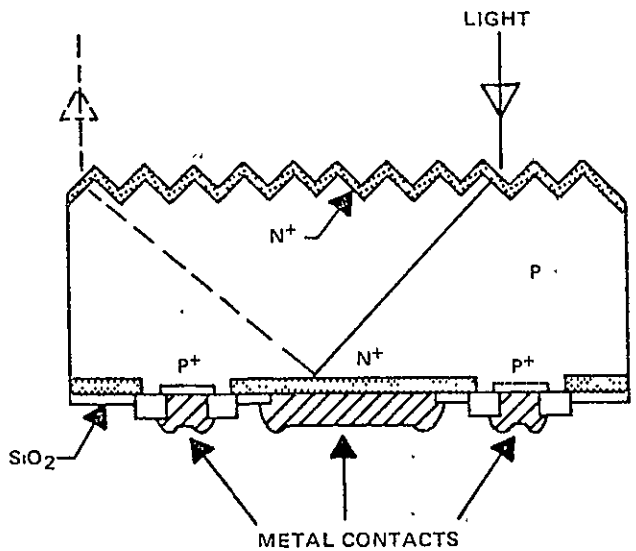


FIGURE 22. SKETCH OF TANDEM JUNCTION CELL

TABLE 22. PHOTORESPONSE FOR TJC WITH BACK CONTACT ONLY

Cell No.	Area (cm^2)	Measured by	Isolation	I_{SC} (mA)	V_{OC} (V)	F.F.	η (%)
20-6	0.975	NASA-Lewis	AM0	36.4	0.593	0.758	12.4
			AM1	33.3	0.586	0.753	15.1
20-2	0.975	NASA-Lewis	AM0	34.0	0.590	0.762	11.6
			AM1	31.0	0.584	0.756	14.1
20-1	3.90	JPL	AM1	115.2	0 595	0 65	11.8
20-8	0.975	JPL	AM1	30.0	0.595	0.766	14.1

The effect of finger spacing is most evident in the low fill factor on cell 20-1, the 2 x 2 cm cell. Current collection, measured over the total cell area, is good and V_{oc} is good. This early success was very encouraging.

2. CELL THICKNESS - LIFETIME

A number of lots of thin TJC's were processed. The first comparison was by base material resistivity and minority carrier lifetime. Lot AAAP-II-7 was run on crystal 370, 0.2-0.3 Ω-cm, $_{SPV}$ <1 μs; lot AAAP II-12 was run on crystal 278, 0.8-1.0 Ω-cm, $_{SPV}$ = 8-10 μs. Both lots were run using the standard process ($POCl_3$, 850°C diffusion). The data is summarized in Table 23.

TABLE 23. TJC RESISTIVITY DATA

Lot Number	Thickness (μm)	τ_{SPV} (μs)	τ^1 (μs)	J_{SC} (mA/cm^2)
AAAP-II-7	110	<1	1.2[2]	12
AAAP-II-7	90	<1	1.2[2]	16
AAAP-II-12	75	8-10	11[3]	31

1. Lifetime after processing.
2. Measured by diode recovery (3 to 4 X greater than SPV).
3. Measured by short circuit current method.

Two conclusions can be drawn from this data. First, J_{sc} for back side only collection is strongly dependent on minority carrier lifetime at thickness near 100 μm. Lot AAAP-II-12 gives J_{sc} approximately twice that of AAAP-II-7. Second, for low lifetime, J_{sc} is strongly dependent on thickness. This J_{sc} - thickness relationship is even more strongly supported by the following experiments.

Four lots of thin TJC's were completed on crystal 278 material (including lot AAAP-II-12 above). Lots AAAP-II-12 and -23 represent a baseline process, lots AAAP-13 and -14 use As polymer dopant and As ion implant, respectively, to achieve a very shallow, 500 A, front N^+ layer on the TJC. Lot AAAP-II-23 was subjected to Cu contamination and lots AAAP-II-13 and -14 may have been contaminated. All lots featured a textured front surface and back contacts only. Cell thickness ranges from 67 to 110 μm.

Table 24 lists the lifetime after processing, measured by the short circuit current method, J_{sc} range for all thickness and V_{oc} for each of these lots run on crystal 278. The only difference between lots AAAP-II-12 and -23 is the back side contact pattern and the apparent Cu contamination on lot AAAP-II-23. Note the very severe impact on cell performance and lifetime due to Cu contaminatio

TABLE 24. TJC EVALUATION

Lot No.	τ (μs)	J_{SC} (mA/cm^2)	V_{OC} (V)
AAAP-II-12	11	24-31	0 58-0.59
AAAP-II-13	2	13-23	0.55-0.57
AAAP-II-14	≈0.03	1-11	0.39-0.53
AAAP-II-23	≈0.03	1-8	0.4 -0.5

Log current density versus thickness is plotted in Figure 23 for lots AAAP-II-12, -13 and -14. The trend to higher J_{sc} for thinner cells is evident for all samples, even with the low lifetime observed on lots AAAP-II-13 and -14. Only the data on lot AAAP-II-12 can be taken as representative due to the very low lifetime on AAAP-II-13 and -14. The expected higher J_{sc} for thinner N^+ front layers was not observed due to the severe lifetime degradation problem.

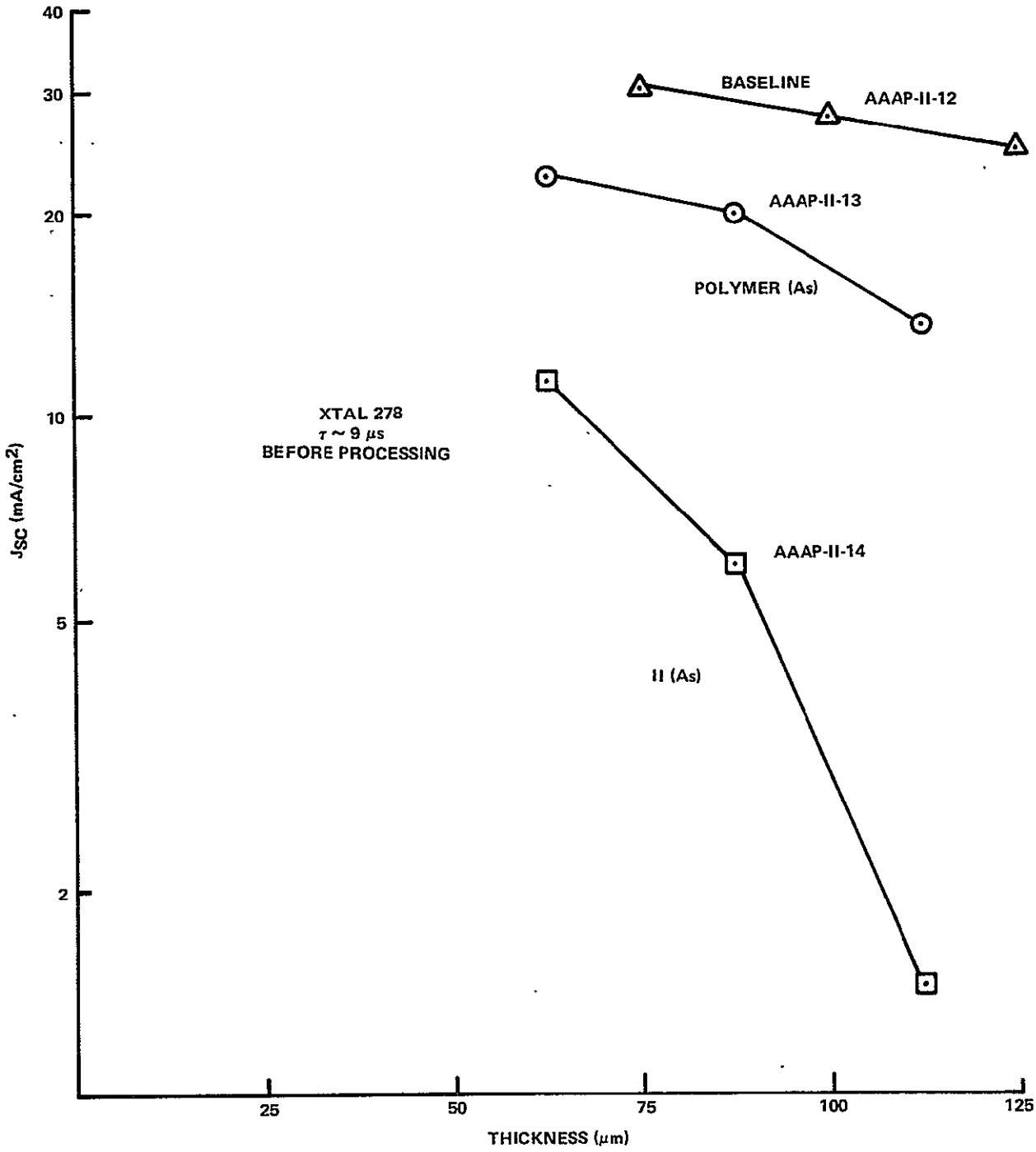


FIGURE 23. CURRENT DENSITY VERSUS THICKNESS FOR TJC STRUCTURES

3. CELL DESIGN

At the beginning of this program a cell design existed that featured 9 N^+ fingers and 8 P^+ fingers in an interposed finger design on a 2 x 2 cm pattern. A 1 x 1 cm version also existed that was a photographic shrink of the 2 x 2 cm pattern. Early results, see Table 22, showed that the 8 finger design was not adequate to achieve a satisfactory fill factor on a 2 x 2 cm TJC. The back contact area of the 2 x 2 cm was redesigned, taking into account the lateral resistance of the thin base region. The new cell layout featured one 12 and one 16 (P^+) finger (6 or 8 fingers/cm) pattern per 5.0 cm wafer. Three small, .83 X .83 cm, cells were included on the 5.0 cm wafer with very dense finger patterns, 30, 36 and 48 fingers/cm, to test the impact of a very dense pattern. A front contact metallization pattern was also generated. A schematic of the back contact pattern is shown in figure 24.

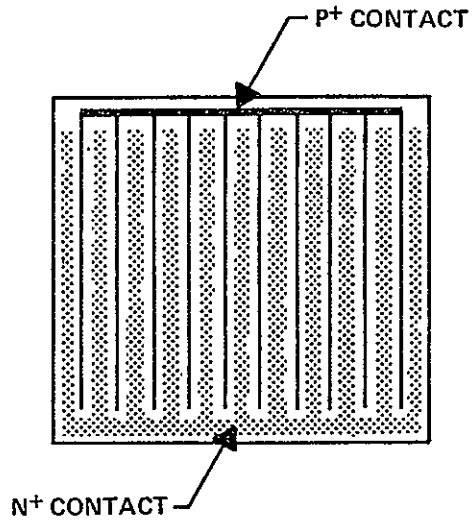


FIGURE 24. SCHEMATIC OF METALLIZATION PATTERN FOR BACK OF 2 cm X 2 cm TANDEM JUNCTION CELL

Using this design the N+ area, P area and P+ area on the back of the $4cm^2$ cell can be readily calculated as in Table 25. The center to center spacing of the P^+ contact fingers is the cell width divided by the number of fingers. If one assumes that the photogenerated carriers generated above the P regions must migrate laterally to be collected, then the collection efficiency above the P regions

will be somewhat lower (longer diffusion path). Therefore the P regions should be narrow. In this design the P regions are .0127 cm wide and the P^+ contact regions are .00762 cm wide.

TABLE 25. AREA ALLOCATIONS ON THE TJC

Region	12 Finger Area (cm^2)	12 Finger %	16 Finger Area (cm^2)	16 Finger %
P	.429	10.7	.524	13.1
P^+	.239	6.0	.296	7.4
N^+	3.571	89.3	3.476	86.9

4. BASELINE PROCESS

The TJC process is somewhat different from the standard diode solar cell process in that one is controlling both a front side and a back side N^+ region and the back N^+ region must be patterned. A basic process flow was developed that allows for separate control of the front and back N^+ regions. The contact resistivity to the P^+ region is also more critical since the area devoted to the P^+ contact is less than 10% of the cell area (see Table 25). The outline of the process is given in Figure 25. Although the process looks complicated a number of process simplifications are possible. At this point in the development of the TJC structure, process flexibility has been retained.

The front and back N^+ diffusions can be combined if the same dopant, depth and profile are used. The two N^+ diffusions can be partially combined using polymer dopants or ion implant to achieve different diffusion depths by using different diffusing species. Other process simplifications can be made in a similar fashion as the final structure is defined.

All high temperature operations, oxidation, diffusion, etc., are at 850°C or lower, as appropriate, to maintain minority carrier lifetime. The standard N^+ diffusion operation uses a $POCl_3$ liquid source, nitrogen carrier gas, a nitrogen-oxygen ambient and is run at 850°C. Diffusion depth is controlled by time at temperature. A slow-push, slow-pull technique is employed.

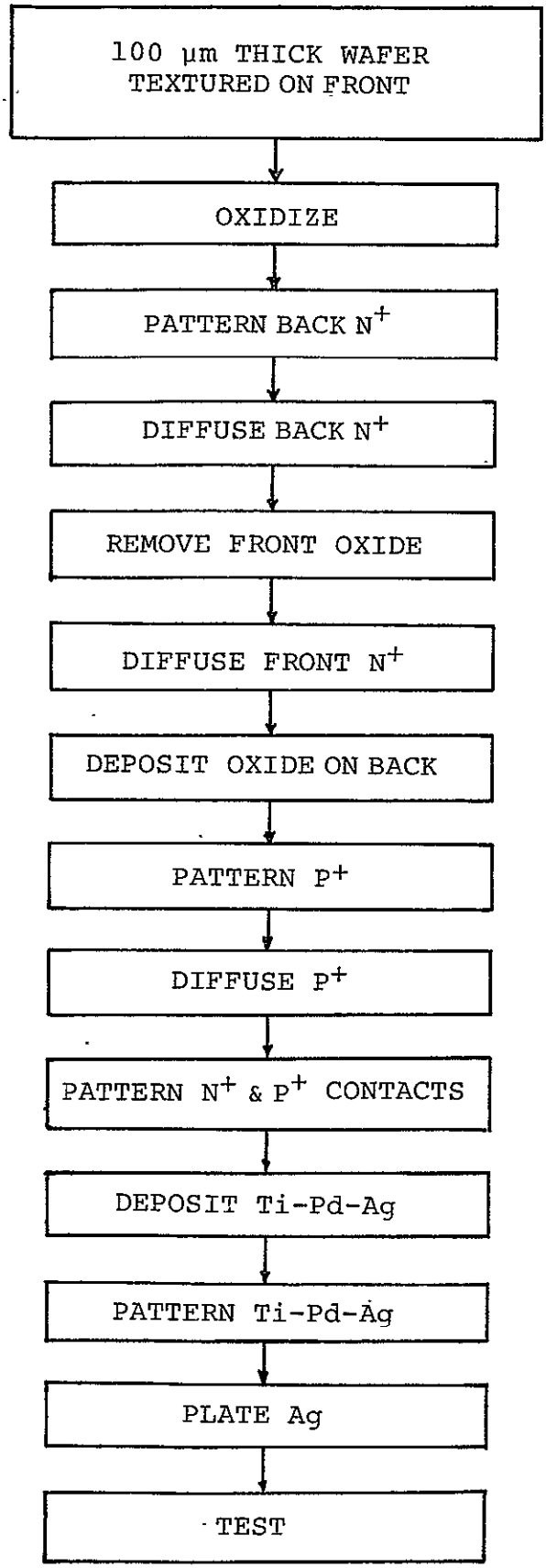


FIGURE 25. TJC PROCESS FLOW

All patterning was done using photolithography. All contact metal evaporations were done in an electron beam, multiple source evaporator.

5. CELL FABRICATION

TJC fabrication was carried out using variations on the baseline process to achieve particular cell features. Various experiments are described below.

A typical TJC run using the baseline process, $POCl_3$ diffusion, N^+ junction depths (front and back) of 0.3 μm is shown in Table 26. Photoresponse measurements were run at JPL and at NASA-Lewis. The current collection is excellent. The V_{OC} and F.F. were lower than desired. The starting material was 6 Ω-cm, <100> material. The last digit in the cell number identifies the number of P fingers in the contact pattern. The high resistivity of the base material accounts for the lowered F.F., note the difference between 16 finger and 12 finger cells.

TABLE 26. TJC PHOTORESPONSE OF LOT AAAP-II-38

Cell No.	Insolation	V_{oc} (V)	I_{sc} (mA)	J_{sc} (mA/cm^2)	F.F.
AAAP-II-38-1-16	AM0	0.572	172.0	43.0	0.741
AAAP-II-38-1-16	AM1	0.591	149.2	37.3	0.74
AAAP-II-38-5-12	AM0	0.579	168.4	42.1	0.685
AAAP-II-38-6-12	AM0	0.591	159.1	39.8	0.717

A process variation was run, on the same 6 Ω-cm base material, to improve V_{OC}. The P region between the N^+ and P^+ contacts was ion implanted with boron, 1×10^{14} atoms/cm^2, 35 KeV, to form a thin doped region between the contacts. The purpose of this intercontact "P^+" region is to act as a back surface field and retard recombination in the intercontact regions. Photoresponse at AM0 is shown in Table 27. The improvement in V_{OC} is evident in the table. F.F. is still limited by the P^+ contact finger pattern. The current collection on these 110 μm thick cells is excellent.

TABLE 27. AM0 PHOTORESPONSE FOR IMPROVED TJC

Cell No.	Structure	J_{sc} (mA/cm^2)	V_{oc} (V)	F.F.	η (%)
AAAP-II-47-2-12	TJC	44.2	0.61	0.685	13.7
AAAP-II-47-3-16	TJC	42.0	0.612	0.741	14.1
AAAP-II-47-4-12	TJC	43.5	0.620	0.714	14.3
AAAP-II-47-5-16	TJC	41.5	0.615	0.748	14.1

The effect of contact finger design on fill factor was investigated using the small TJC's, 0.83 x 0.83 cm, that have 30, 36 or 48 contact fingers per cm. The increased P^+ contact area reduced the current collection but the fill factor is raised to 0.80 for all contact finger configurations. Table 28 shows AMO photoresponse for these small, dense finger pattern cells. From the data, one can see that 30 fingers/cm is more than is needed to achieve a good fill factor. It is also obvious, that as more of the backside area is committed to P^+ contacts, the J_{SC} and V_{OC} begin to decrease. An optimum finger contact pattern for 6Ω-cm base material can be designed.

TABLE 28. AMO PHOTORESPONSE OF DENSE FINGER TJC

Cell Number	Contact Pattern (Finger/cm)	J_{SC} (mA/cm^2)	V_{OC} (V)	F.F.
AAAP-II-47-11	30	38.5	0.605	0.80
AAAP-II-47-12	36	36.3	0.60	0.80
AAAP-II-47-13	48	34.8	0.595	0.80

Further experiments using higher dose boron implants, 2×10^{14} atom/cm^2 and 5×10^{14} atom/cm^2, to assess the effect on V_{OC}, proved to be process variation in the wrong direction. As the intercontact doping increased, the reverse diode breakdown decreased to unacceptable levels, causing significant cell leakage with resultant degradation in photoresponse. At a boron dose of 5×10^{14} atom/cm^2, the shunt resistance has decreased to a few ohms. Further experiments are necessary using lower boron implant doses to optimize the intercontact doping. These experiments were not run on this program due to a lack of time.

Another process variation used ion implanted As, 1×10^{15} atom/cm^2, 35 KeV for the front N^+ region. The implanted As layer was activated and diffused using a 550° - 1000° - 550°C temperature treatment. The resultant front N^+ layer was calculated to be 0.2 μm deep. The photoresponse was essentially identical to a diffused phosphorous front junction. The As ion implanted front junction can be used interchangeably with a phosphorous diffused front junction as a process step.

6. SPECTRAL RESPONSE

Spectral response was measured* on two 110-μm thick TJC's. Measurement using low-intensity chopped monochromatic light gives a response significantly lower than anticipated for a conversion efficiency of 12% (AMO). When the cell was flooded with a white light (intensity ~0.5 sun) and the low intensity chopped monochromatic light was superimposed, a significantly higher spectral response was observed at all wavelengths. The data for one cell is shown in Figure 26. Several features are worthy of note: the peak spectral response for the TJC occurs at a longer wavelength, 1.0 μm, than is typical of conventional solar cells, the thin TJC exhibits significant response at 1.1μm, the upper limit of the measurement, and significant enhancement of the blue response occurs when the cell is flooded with white light. The longer wavelength peak response is expected for a thin TJC using back contacts. The high spectral response at 1.1 μm is probably related to the long wavelength peak response. Both the response at short wavelengths (0.4 μm) and the enhancement in this region were not expected since these cells have no contacts on the front (illuminated) junction.

The high spectral response at short wavelengths is particularly interesting. The original concept of the back contact TJC assumed that the sensitivity to short wavelength light would be sacrificed since the high energy photons would be almost totally absorbed in the N^+ region near the illuminated surface. With no direct electrical contact to this N^+ layer, "floating front junction", it was assumed that collection efficiency from this region would be poor. In fact, collection efficiency is very good indicating a significant electrical interaction in the illuminated TJC.

The enhancement of spectral response as a function of a bias light is another interesting feature. Typical diode solar cells show very little, if any, enhancement of spectral response as a function of light bias. The strong enhancement of spectral response with light bias is apparently related to the longer path length that photogenerated carriers must traverse to reach the back side collecting junction. A trap filling mechanism is postulated. At the low photogenerated current level used in spectral response measurements, trapping sites in the base region could exert a significant modulating effect. The effect of the bias light would then be to generate a background photogenerated current that would fill the available traps.

*Measurements were performed by B. Anspaugh, JPL.

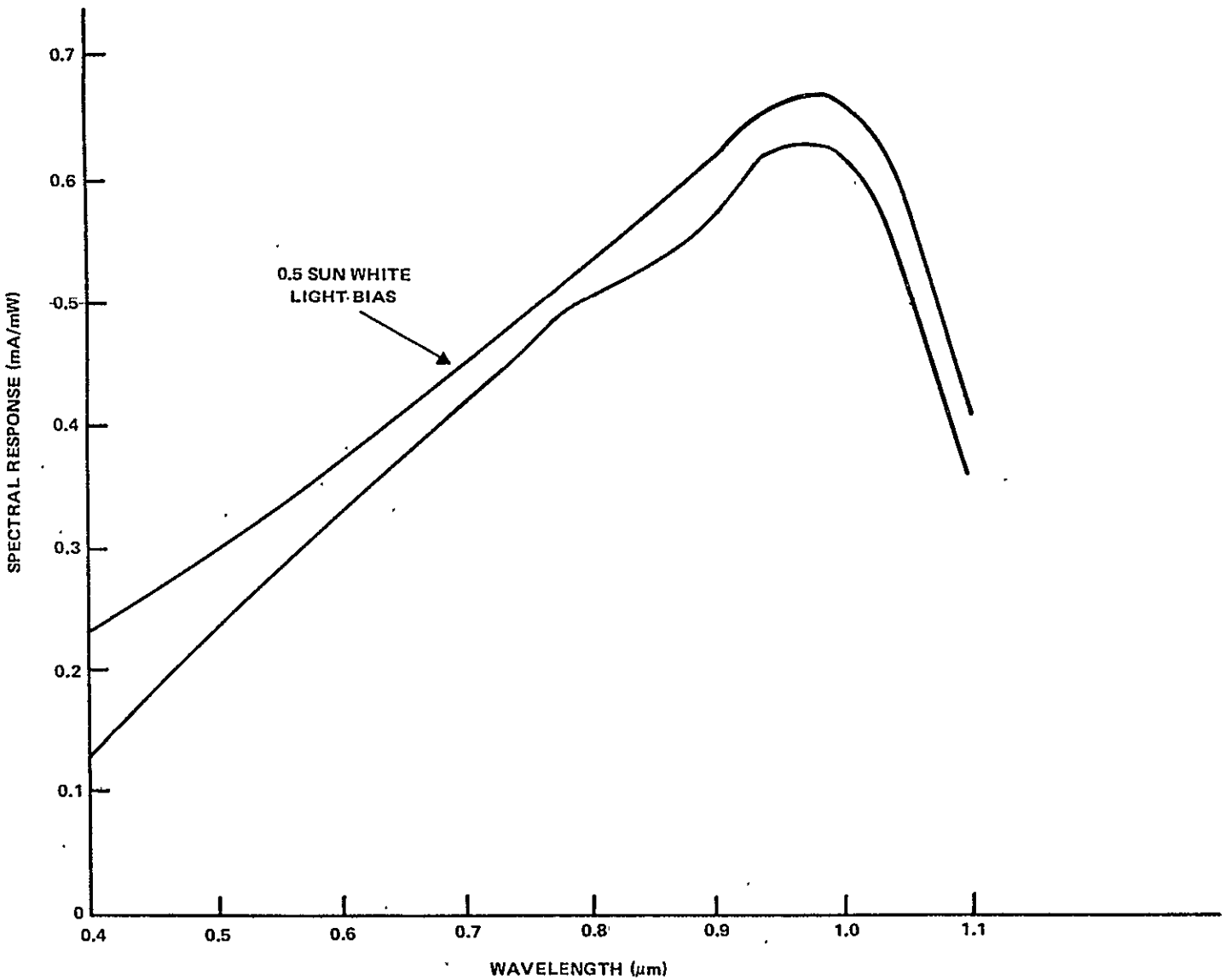


FIGURE 26. SPECTRAL RESPONSE OF TJC

Now the photogenerated current due to the spectral scan would be virtually 100% collected leading to an apparent increase in spectral response. Detailed examination of this phenomena was not possible under the scope of this program.

7. FRONT CONTACT TJC

TJC's were fabricated with metal contacts on both the front and back N^+ junctions. The metal contact regions were separate from one another so that independent front and back photoresponse could be measured. These cells, lot AAAP-II-32, were fabricated on <111> material. The illuminated surface was not textured to eliminate possible problems with metal contacts on textured surfaces. Both front and back side N^+ regions were formed using a $POCl_3$ diffusion at 850°C. Photoresponse measurements were run under a tungsten lamp at an intensity near AMO. V_{OC} and I_{SC} were measured for front, back and front plus back collection, Table 29. In each case, the unused N^+ region was left floating. The current collection was slightly lower than expected for the front and front plus back configurations. The back collection configuration was much lower than anticipated. The presence of metal contacts on the floating front surface appears to exert a striking affect on the back collection. The explanation of this effect is not obvious at this time. A repeat of this experiment gave similar results.

TABLE 29. FRONT AND BACK TJC PHOTORESPONSE

Configuration	V_{OC} (V)	J_{SC} (mA/cm^2)
Front - P^+	0.585	25
Back - P^+	0.565	10
Front + Back - P^+	0.580	30

8. TJC MODEL

The Tandem Junction Cell (TJC) is a high performance silicon solar cell for application in terrestial power systems. A distinctive feature of the TJC is the use of only back contacts to eliminate metal shadowing and facilitate interconnection.

Design relationships for conventional solar cells do not apply to the TJC structure; however, excellent performance has been obtained by empirical optimization. Structures fabricated for use in flat plate systems have demonstrated efficiency potential as high as the best conventional cell designs in one-sun insolation [6] (e.g., 16.4% at AM1). Concentrator cells have measured efficiency of 16.9% at 20 suns (AM1 spectrum) [7].

A conceptual model [8] is described here which provides insight into device operation and gives general design considerations. This model should also provide a foundation for a more rigorous computer analysis.

A. TJC STRUCTURE AND OPERATION

The characteristic structure of the Tandem Junction Cell [6] is shown in Figure 27. The front, illuminated side is a texturized surface with a thin uncontacted junction. The active junction consists of interposed N^+ and P^+ fingers at the back surface.

For a texturized surface of <100> silicon, refraction of light within the silicon increases the optical path length and causes light to strike the back surface at greater than the critical angle ($\approx 15°$) for total reflection. Hence a high percentage of light is absorbed in very thin cells. High collection efficiency is achieved with back contacts because of the thin, high lifetime base region.

B. EXPLANATION OF MODEL

The TJC in cross-section can be compared to a transistor as shown in Figure 28 (a). The front N^+ region corresponds to the emitter, the P-region to the base, and the back N^+ region to the collector. The equivalent circuit model is shown in Figure 28 (b). The current source $I_{\lambda E}$ is due to hole-electron pairs generated in the emitter or in the base near the emitter; the current source $I_{\lambda C}$ results from generation in the collector or in the adjacent base region. The model will be used first to describe current collections for

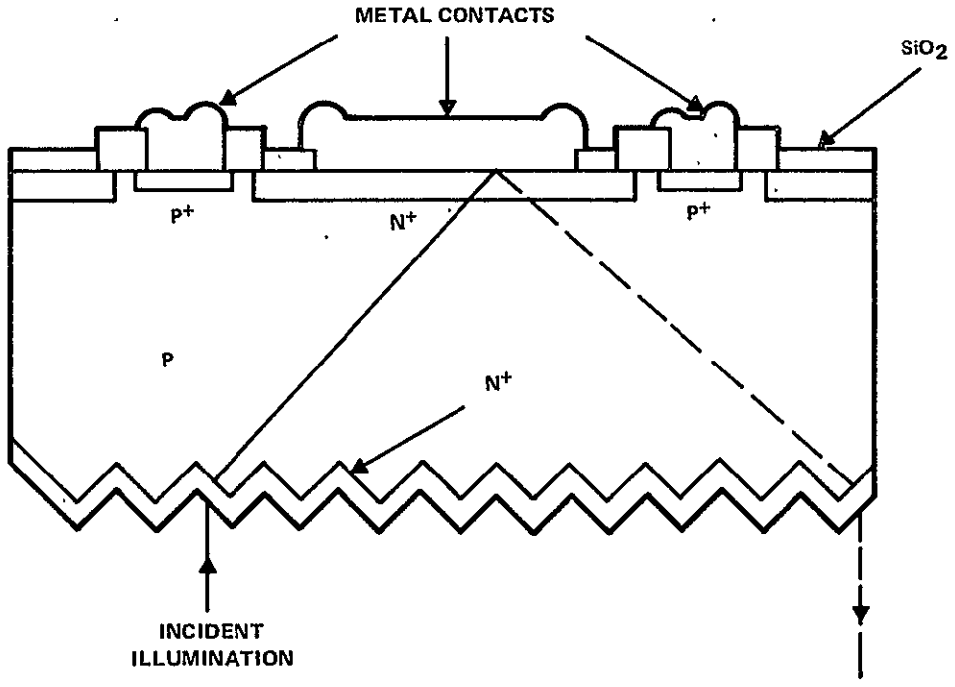
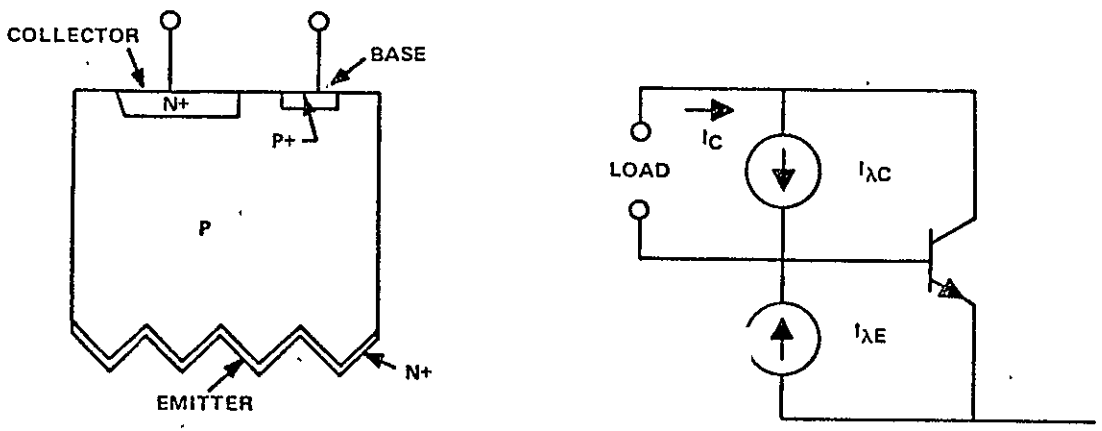


FIGURE 27. SKETCH OF TANDEM JUNCTION SOLAR CELL



(a) TJC CROSS SECTION

(b) EQUIVALENT CIRCUIT

FIGURE 28. REPRESENTATION OF TJC AS TRANSISTOR STRUCTURE

the short-circuit condition and then the open-circuit voltage.

As shown in Figure 29 (a) minority carriers (holes) generated in the front N^+ (emitter) region diffuse to the emitter-base junction and are swept by fields into the base. A forward-bias potential is built up across the junction such that electrons are injected into the base in approximately equal quantities (assuming injection efficiency is high, as discussed later in this section). Figure 29 (b) illustrates the case of generation in the base near the emitter. Electrons diffuse to the emitter-base junction and are swept into the emitter. To maintain charge balance, a voltage is built-up such that electrons are injected back into the base.

Current for either of the above cases is collected by transistor action. The output is between collector and base terminals. Injected electrons diffuse across the base and the collector-base junction. Holes move by fields through the base to the P^+ base contact.

The transistor in the equivalent circuit of Figure 28 (b) is represented by an Ebers-Moll model, which can be characterized by the parameters[9]

α_N	current transfer ratio for normal (forward) bias
α_I	current transfer ratio for inverse bias (i.e., collector biased as an emitter)
I_{cs}	saturation current for collector-base junction

From the equivalent circuit, the short circuit current, I_{sc}, is

$$I_{cs} = \alpha_N I_{\lambda E} + I_{\lambda c} \tag{6}$$

The open circuit voltage, V_{oc}, follows from the Ebers-Moll model. The relationship is

$$V_{oc} = \frac{KT}{q} \ln \frac{I_{sc}}{I_{cbo}} \tag{7}$$

where the dark current, I_{cbo}, is the collector-base saturation current, with emitter open, for the structure as a transistor. In terms of the model parameters defined above

$$I_{cbo} = I_{cs} (1 - \alpha_N \alpha_I) \tag{8}$$

In principle, high V_{oc} can be obtained by making α_N and α_I approach unity.

C. CELL DESIGN CONSIDERATIONS

Collection efficiency and open circuit voltage depend upon the current transfer ratios, α_N and α_I. Structural optimization of these parameters follows well-established design procedures for dc characteristics of transistors.

The current transfer ratio may be expressed as [10]

$$\alpha = \gamma \cdot \beta \tag{9}$$

where the injection efficiency γ, and transport factor β, can be related to structure.

For an emitter junction like that of Figure 29, injection efficiency is defined as the ratio of injected electron current to total emitter current. Injection efficiency depends upon impurity profile and processing of the emitter region. Similarly, injection efficiency for inverse operation depends upon the properties of the collector region.

First order theory indicates that injection efficiency is increased by use of heavily-doped emitter regions. This is generally observed in practice; however actual values of injection efficiency for heavily-doped emitters are lower than predicted. This discrepancy is attributed to effective shrinkage of the band gap. [11]

It has been demonstrated that injection efficiency of NPN power transistors can be substantially increased by use of deeper lighter-doped emitter regions. [12] Other experiments indicate that injection efficiency of N on P solar cells is higher when the N^+ metal contact area is decreased or junction depth increased. [13]

Injection efficiency for the front junction of the TJC should be high since metal contacts are omitted. Deep junctions can be used at the back junction for high injection efficiency since generation rate at the back surface is low.

Transport factor is the fraction of the injected electron current which reaches the collector-base junction. Decrease of the injected current in the base transit process is due to bulk and surface recombination. Bulk recombination is reduced for low ratios of base width to diffusion length. The diffusion length is

$$L = \sqrt{D \tau}$$

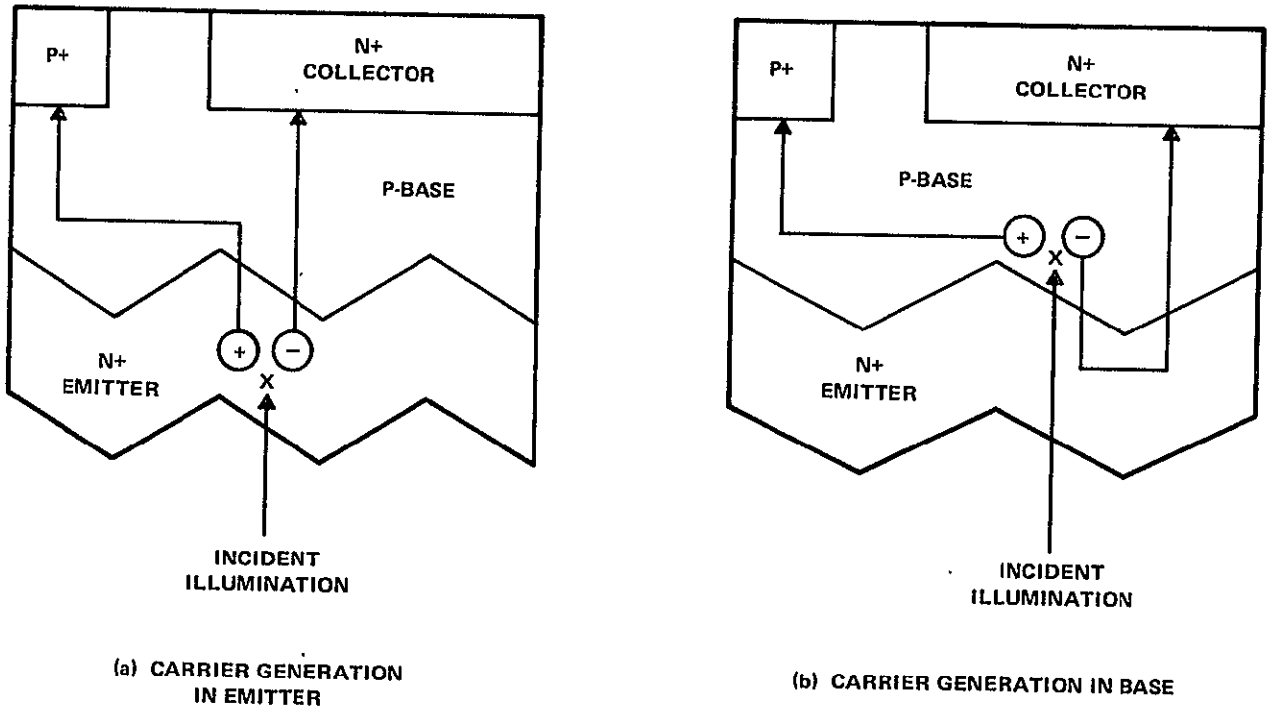


FIGURE 29. SCHEMATIC REPRESENTATION OF CARRIER FLOW IN TANDEM JUNCTION CELL

where D is diffusion coefficient and τ is lifetime for minority carriers in the base region. Bulk recombinations can be minimized with high resistivity base material where high values of D and τ are obtained. Surface recombination is due to the P and P^+ areas of Figure 27 and is decreased by using smaller contact areas.

Design considerations for optimizing TJC performance are summarized in the structure of Figure 30.

D. INTERPRETATION OF MEASURED RESULTS

An essential feature of the model is collection of carriers from the uncontacted front N^+ region. Experimental evidence that this does occur is presented here.

Spectral response for the TJC is plotted in Figure 31 (a) along with quantum efficiency. Also shown for comparison is the OCLI MLAR (multi-layer anti-reflection) cell; efficiency of 16.5% (AM1) for this cell is one of the highest reported to date. Response for the TJC was measured by JPL using the pulsed xenon arc simulator with steady-state light bias.

Short wavelength, spectral response of the TJC exceeds that of the MLAR cell. Quantum efficiency is greater than 70% for illumination at 0.4 μm for which carrier generation is very close to the front surface. This can occur only if carriers generated within the front N^+ region are collected at the back contact.

Comparative spectral response for a Tandem Junction Cell, measured with and without light bias, is shown in Figure 31 (b). Response, particularly at short wavelength, is substantially improved by light bias. The equivalent circuit of Figure 28 (b) provides an explanation. The current transfer ratio, α_N, falls off at low currents due to recombination in the space charge region. Light bias increases current level and α_N so that collection efficiency is improved.

Measured short circuit current for the TJC (42.0 ma/cm^2 at AM0) is consistent with the model. This value could not be obtained without collection from the front N^+ region.

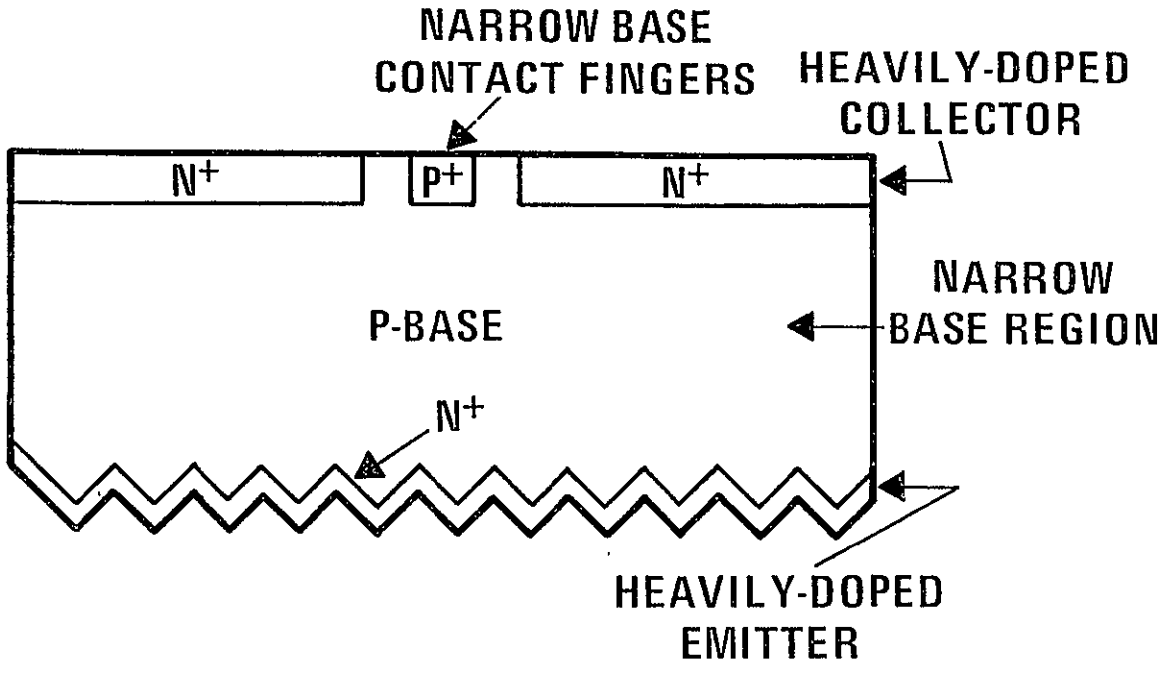
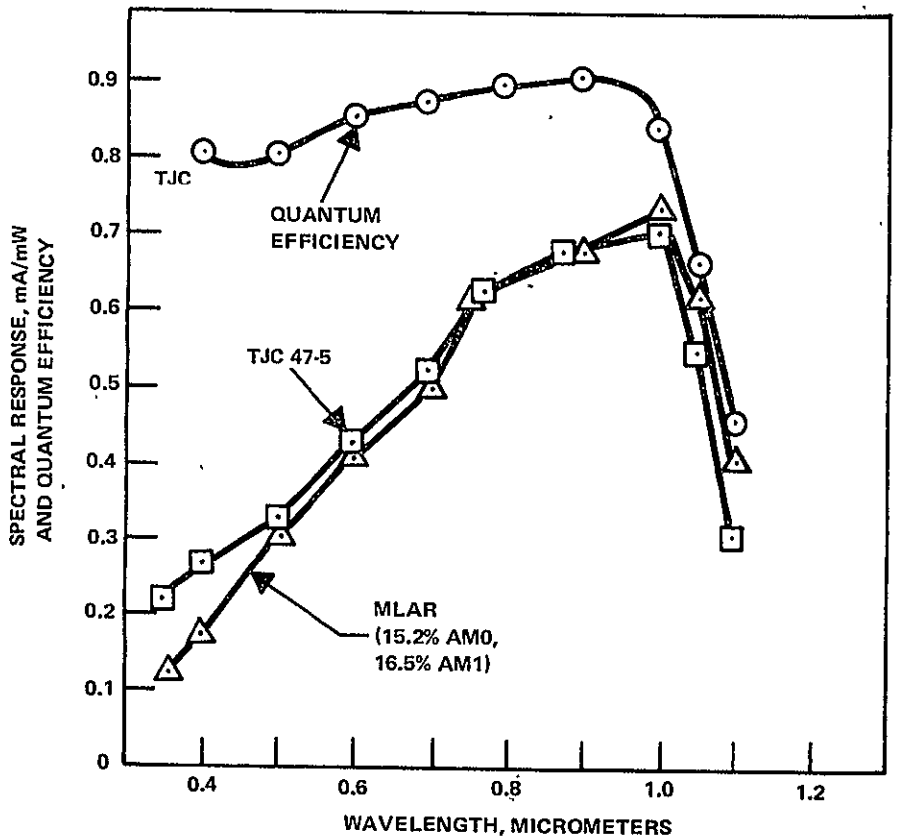
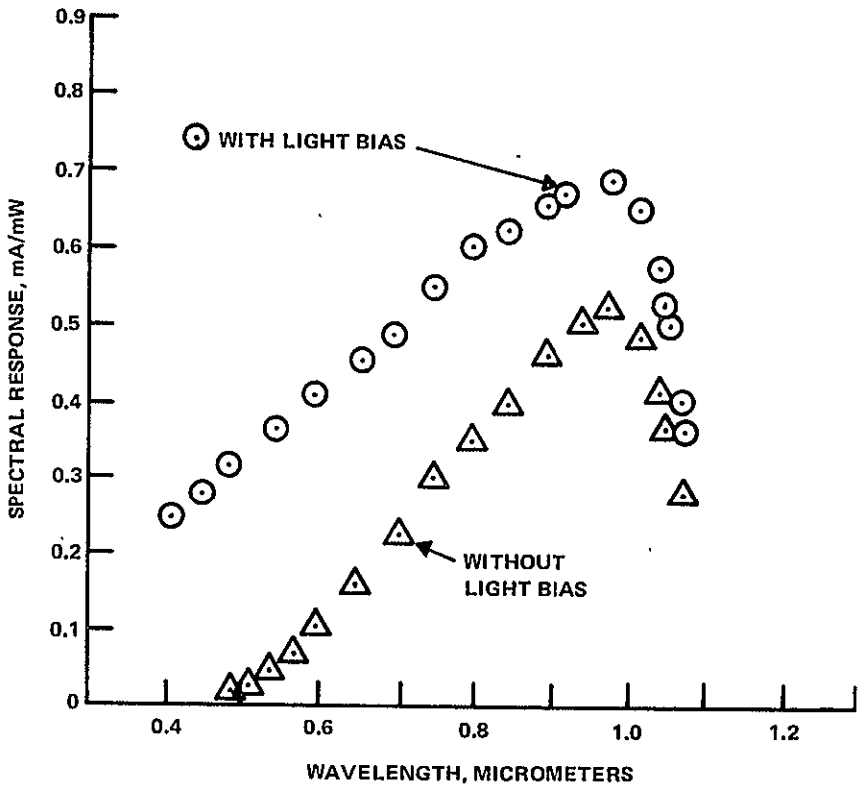


FIGURE 30. OPTIMIZATION THROUGH TRANSISTOR DESIGN PRINCIPLES

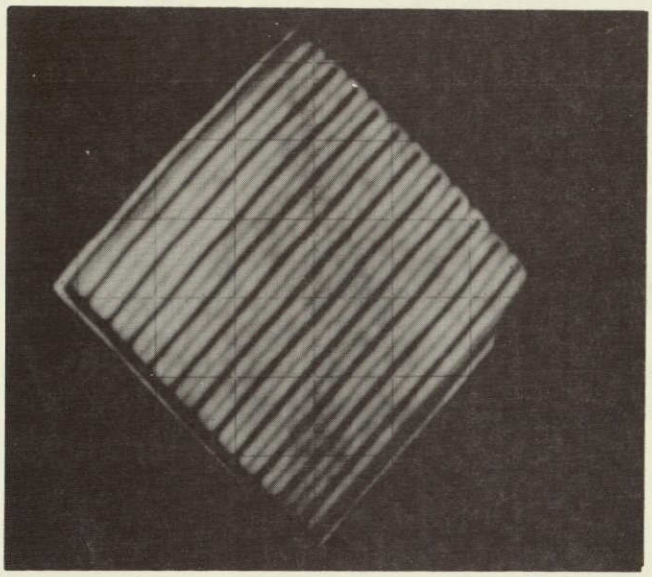


(a) Comparison to MLAR Cell

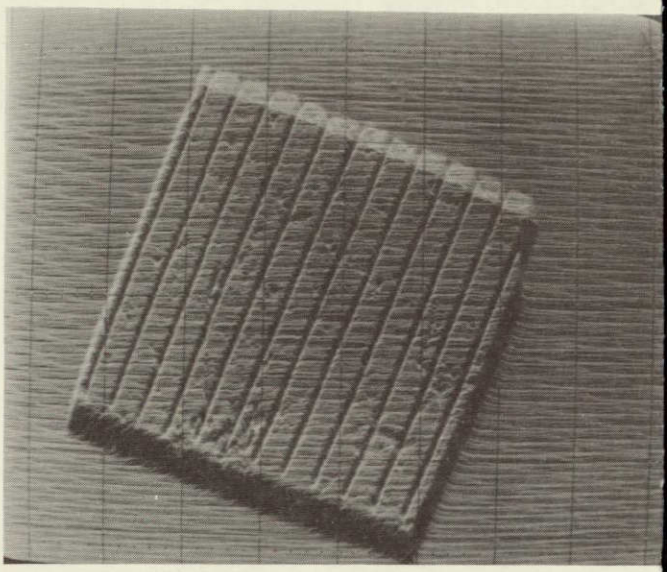


(b) Effect of Light Bias

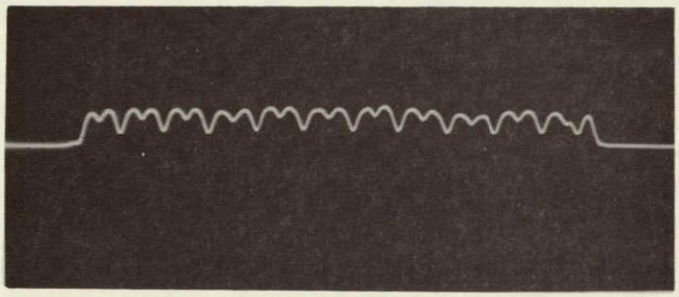
FIGURE 31. SPECTRAL RESPONSE OF TANDEM JUNCTION CELL



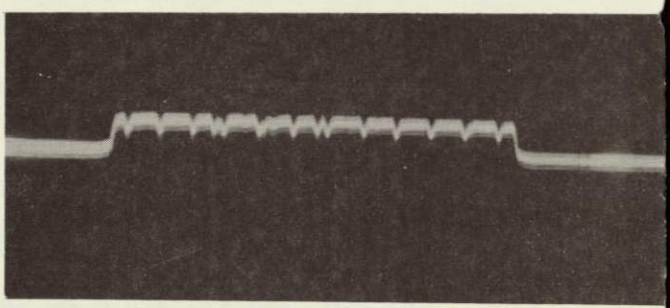
(a)



(c)



(b)



(d)

FIGURE 32. SCANNING PHOTORESPONSE MEASUREMENT OF TJC. (a) and (b) are for 1.15μ illumination and show loss of current collection over both N^+ and P^+ fingers; (c) and (d) are for .65μ illumination and shows current loss over P^+ fingers.

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Open circuit voltage as high as 0.615 volts has been measured for AM0 (25°C). By comparison the highest V_{OC} reported for a back surface field cell is 0.622 volts (AM1, 27°C). [14] High open circuit voltage for the TJC has been explained intuitively by low recombination in the base region and at surfaces. An alternative interpretation is reduction of dark current by transistor action as shown by Equation 7.

9. LASER SCANNING

Some very interesting, but still preliminary, observations were made through laser scanning measurements conducted by D. Sawyer at the National Bureau of Standards. Laser scans were run at two wavelengths, 0.65 μm and 1.15 μm. The scanning photoresponse results are shown in Figure 32 for a 12 finger TJC with back contacts. Figure 32 a and b show the composite and single line scan results at 1.15μm. This low energy wavelength is at or very near the band edge for silicon. The laser beam penetrates the full 100 μm thickness of the cell and shows reduced current collection over both the N^+ and P^+ metallized regions, the darker, wider regions are N^+ metallization. Figure 32 c and d show the results using a 0.65 μm beam. In this case, the laser beam is more strongly absorbed near the illuminated surface and only the effect of the P^+ metallization is seen.

The interpretation of these measurements is not straight forward at this time. Some speculative observation can be made. The reduced current collection over the P^+ metallization observed at 0.65 μm scans is probably related to high recombination at the metal-silicon interface. Better control of this interface might recover part of this lost current component. The absence of any loss of current in the N^+ metallization or back N^+ region indicates that junction depth is not a controlling factor and deeper back side junctions could be employed to improve the emitter-base junction characteristics. The significant current loss over the N^+ metallization shown in the 1.15 μm scans may be an optical effect (lower reflection). A narrower N^+ contact region may improve long wavelength response. The pock marked effect in Figure 32 c is apparently due to defects in the silicon. The defects may be intrinsic in the wafer or they may be damage induced by handling.

This very preliminary work indicates the potential power of laser scanning as a diagnostic tool. Further development of the technique and of the data interpretation could be very beneficial in the development of high efficiency solar cells.

10. FRONT SURFACE FIELD (FSF) CELL

As a variant on the TJC cell, cells were fabricated with the front (illuminated) diffused area being P-type rather than N-type, see Figure 22. The concept of the FSF cell is to create a front surface field in place of the N^+/P junction in the TJC. The function of the front surface field is similar to the back surface field (BSF) in conventional diode solar cells, that is, to create a drift field or concentration gradient near the front surface that would cause photogenerated carriers to be more efficiently collected at the back N^+/P junction.

Two groups of thin textured cells were fabricated using the baseline TJC process, Figure 25. One group, lot AAAP-II-34 were standard TJC's and the other, lot AAAP-II-35 were FSF cells (the process was modified to form a front P^+ layer, BN diffusion source, for the FSF cells). All common process steps were run at the same time. Both groups were fabricated on 6 Ω-cm wafers from the same crystal. Photoresponse at AM1 was measured in sunlight in a back contact only configuration. Photoresponse for the 2 x 2 cm cell is shown in Table 30.

TABLE 30. PHOTORESPONSE OF TJC AND FSF CELLS - AM1

Lot No.	Structure	Thickness (μm)	V_{OC} (V)	J_{SC} (mA/cm^2)	η
AAAP-II-34	TJC	100	0.55	33.6	13.8
AAAP-II-35	FSF	90	0.544	32.0	13.0

The TJC structure shows slightly better performance than the FSF structure but the difference is too small to be significant. The low V_{OC} on both structures is attributed to the high substrate resistivity and the effect of the intercontact regions on the back side.

A second comparison was run, this time the process included the boron implant in the intercontact regions on the back side, see section II. F. 5. Again a group of TJC's and a group of FSF cells were run. Photoresponse at AM0 is shown in Table 31. The improvement in V_{OC} is striking and even accounting for the spectral difference, the improvement in J_{SC} is significant. Both cells have the 12 finger (6 finger/cm) pattern accounting for the low F. F.

TABLE 31. AM0 PHOTORESPONSE FOR IMPROVED TJC AND FSF CELLS

Cell Number	Structure	J_{sc} (mA/cm^2)	V_{oc} (V)	F. F.	(%)
AAAP-II-47-2-12	TJC	44.2	.61	.685	13.7
AAAP-II-52-2-12	FSF	42.0	.59	.685	12.5

The current collection of the FSF cell is excellent but slightly lower than the TJC. Similarly, the V_{OC} is slightly lower for the FSF cell.

In summary, the FSF cell is a promising structure, that can be used to fabricate a diode solar cell with planar back contacts. The module assembly advantages of back contacts are obvious to those familiar with solar cell module assembly. The FSF cell, however, does not appear to be quite as efficient as the TJC in limited comparisions. Since this program has limited resources, the main thrust of this investigation has been focused on understanding and improving the TJC structure.

11. ASSEMBLY CONCEPTS

As part of the module fabrication study, assembly of TJC's was considered. The planar contact system, both N and P contacts on the same surface, of the TJC allows us to achieve virtually 100% nesting efficiency and 100% interconnect efficiency in module assembly. Four small, 0.83 x 0.83 cm, TJC's were series connected on a metallized alumina substrate. The cells were attached using a conductive paste in this test. The photoresponse (AM0) was exactly as expected (Table 32). The assembly is shown in Figure 33.

The particular assembly technique, conductive paste, used in this demonstration is far from ideal. The technique was used only to facilitate the demonstration. Standard integrated circuit welding techniques were tried using thin, .0025 cm, gold ribbon interconnects. The welding conditions used caused damage to the N^+/P junction under the bus bar and no further work was

TABLE 32. PHOTORESPONSE OF TJC ASSEMBLY

	V_{OC} (V)	J_{SC} (mA/cm^2)
One Cell	0.56	33
Four Cell	2.24	33

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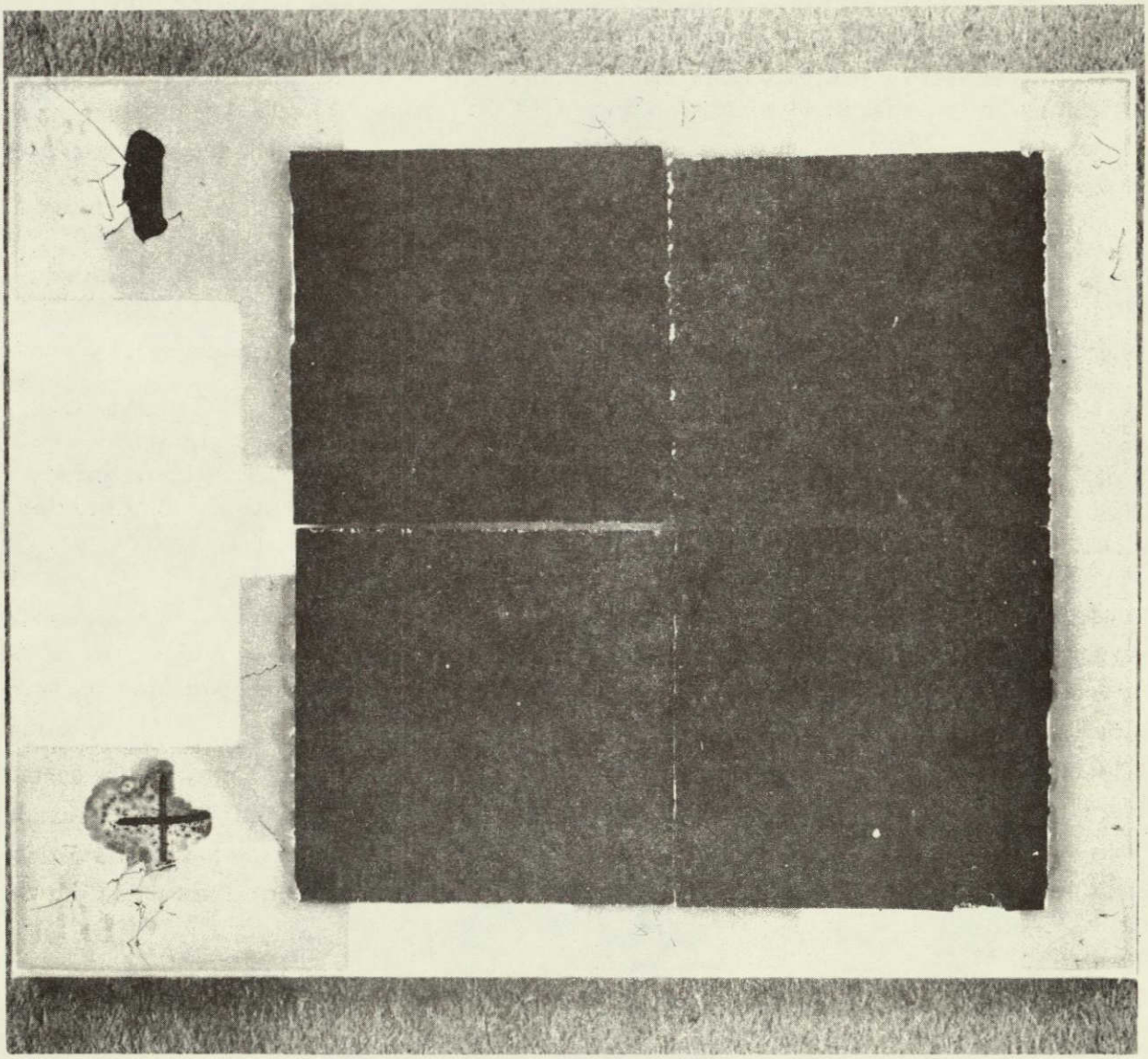


FIGURE 33. TJC FOUR CELL ASSEMBLY

done to optimize welding conditions. Soldering would work, but appropriate soldering fixtures were not available. This demonstration used an all series arrangement but other configurations, e.g. parallel-series, could obviously be used.

12. SAMPLE CELLS

At the end of the development phase of this program, sample TJC and FSF cells were fabricated and shipped to JPL. The TJC's were fabricated using the baseline process shown in Figure 25 with the addition of a boron implant, 1×10^{14} atom/cm^2, 35 KeV, across the back surface before diffusion. All diffusions were done at 850°C. The front N^+ diffusion was either a $POCl_3$ diffusion, lot AAAP-II-90 or an As ion implant, 1×10^{15} atom/cm^2, 80 KeV, lot AAAP-II-98; the back N^+ diffusion was a $POCl_3$ diffusion, 0.6 μm deep.

The FSF cells were fabricated using a similar process with ion implanted B, 1×10^{15} atom/cm^2, 50 KeV, in place of the front N^+ diffusion. The boron implant was run before the back N^+ diffusion and the implant was activated during the 850°C diffusion cycle. The FSF cells also featured a boron implant, 1×10^{14} atom/cm^2, 35 KeV, across the back. Process specifics are given in Table 33.

All cells used an evaporated Ti-Pd-Ag contact matallization. The Ag was plated to a final thickness of 5-7 μm. After plating and sawing to separate individual cells, gold ribbon was thermal compression bonded to the bus bars and thermal compression bonded to metallized ceramic substrates. The bonded assemblies were then tested for photoresponse and shipped to JPL.

TABLE 33. TJC AND FSF PROCESS DESCRIPTION

Lot Number	Resistivity (Ω-cm)	Front Source	Junction Dose or Time	Back Side Boron	Back Side Phosphorous
AAAP-II-90	6	$POCl_3$	5-12-3	$1x10^{14}$/35	10-45-45
AAAP-II-98	6	As	$1x10^{15}$/80	$1x10^{14}$/35	10-45-45
AAAP-II-96	6	B	$1x10^{15}$/50	$1x10^{14}$/35	10-45-45
AAAP-II-97	6	B	$1x10^{15}$/50	$1x10^{14}$/35	10-45-45

All of these cells exhibited good V_{OC}, > .58V, but none of these cells exhibited the high I_{SC} usually observed on these structures, typical AM1 values were 31-34 mA/cm^2. Fill factor was a function of the finger pattern, 12 finger cells 0.68 - 0.71 and 16 finger 0.74 - 0.75. A laser scan on smaples from lots AAAP-II-90 and -98 was run at the National Bureau of Standards after these cells were shipped to JPL. The laser scan at 0.63 μm showed the presence of high density of defects that act as recombination centers. This high defect density probably accounts for the lower than expected values for I_{SC}. The source of the defects is unknown at this time. The defects could arise from inherent crystal problems associated with the crystal growth or from process induced defects.

13. SUMMARY

The Tandem Junction Cell structure developed by Texas Instruments represents a new class of solar cells. The device is actually a transistor with a photo emitter. The planar back contact system is an asset in two ways, there is no shadowing of the front surface by contact metallization and module assembly is facilitated. Using existing understanding of the TJC structure, AM1 efficiencies in excess of 17% are expected with a redesign of the contact pattern to achieve fill factors of 0.78 - 0.80. As understanding of the structure improves, we expect to achieve AM1 efficiencies of 20% or better.

The Front Surface Field cell developed by Texas Instruments enjoys the benefits of the planar back contact system in an inverted diode solar cell. While performance has not quite equalled the TJC, the FSF cell has shown excellent conversion efficiencies. There is every reason to believe that further improvements will also be made in this device. These devices deserve much more development effort as high efficiency solar cells.

Present TJC's are fabricated from Czochralski grown Si. This represents an inefficient use of the Si crystal since a large fraction of the Si crystal is wasted in the preparation of thin, 50-100 μm, substrates or conventional, 200-300 μm, substrates. However, if one ignores the present day Si sheet fabrication and looks at photovoltaic power as a function of Si volume (or mass) used, the TJC with 15% efficiency at 100 μm thickness is at least a factor of 2-3 better than a conventional

solar cell with 15% efficiency at 200-300 μm thickness. Considering the high cost content of Si sheet, this represents a significant area for cost improvement in module fabrication. Direct conversion of polycrystalline Si to Si sheet of 100 μm thickness would eliminate the present-day inefficiencies of converting Cz crystal to thin wafers. It must be remembered that the TJC uses a textured surface and suitable Si sheet (or ribbon) must be amenable to a texturing process. This type of step function cost improvement can contribute significantly to the 1986 LSA Project goals.

SECTION III
CONCLUSIONS AND RECOMMENDATIONS

- Aqueous NaOH etchant is useful for surface damage removal and for surface texturing.

- A conceptual model has been proposed that explains the pyramid formation in texture etching. Control of several different aqueous NaOH etchant parameters can be used to control the texture etch process.

- Plasma etching as a process element to remove silicon dioxide or silicon nitride over a shallow, $\sim 0.3\ \mu m$, junction was judged not to be a viable manufacturing process. The differential etch rate between silicon dioxide or silicon nitride and the underlieing silicon is too low, i.e., the silicon does not provide an etch stop.

- Arsenic doped polymer diffusion sources are not suitable for low-cost high-efficiency solar cell manufacture due to the high process temperatures and/or long diffusion times.

- Phosphorous doped polymer diffusion sources are excellent candidates for a low-cost high-efficiency solar cell manufacturing process.

- Boron doped polymer diffusion sources may be acceptable candidates for a low-cost high-efficiency solar cell manufacturing process.

- Three low cost process alternates, all based on phosphorous doped polymer diffusion sources have been identified. One of these has been demonstrated.

- A long life module construction based on a porcelainized steel substrate - glass cover has been designed and fabricated. The module should withstand outdoor environments for more than 20 years.

- A copper clad Invar interconnect was designed that matches the thermal expansion of silicon.

- Condensation/vapor phase reflow soldering was demonstrated as an excellent method for soldering interconnection to silver plated solar cell contacts. The method provides precise control of temperature and time during the solder operation.

- The Tandem Junction Cell is an excellent candidate for high efficiency silicon solar cells. AM1 cell efficiencies greater than 16% have been fabricated The cell features a planar back contact system with no metallization of the front side. This back contact system is a particularly attractive feature for module fabrication since all interconnects can be behind the cells.

- A model has been developed for the TJC. The model treats the TJC as a transistor with a floating emitter. Using this model further design improvement are anticipated that could increase AM1 efficiency to the 20% region.

- A variation of the TJC, the Front Surface Field cell was also developed. This structure has a P^+ layer on the front of a P base. The FSF cell also features a planar back contact system with no front side metallization. AM1 efficiencies are slightly less than the TJC.

- The very promising results on the TJC structure should be vigorous pursued. Even at comparable efficiencies, the TJC represents a significant savings in silicon if a sheet or ribbon technology can be implemented that produces high quality thin sheets directly from polycrystalline silicon.

SECTION IV
NEW TECHNOLOGY

The following areas of new technology were identified this year.

1. Thin Tandem Junction Cell. The tandem junction cell developed by Texas Instruments exhibits the property of increasing current density with decreasing cell thickness. Cells have been fabricated with thicknesses down to 65 μm. For base material with minority carrier diffusion length less than the cell thickness, in the back contact mode, photogenerated current density exhibits a strong inverse relationship to cell thickness. For long minority carrier diffusion length, the inverse relationship decreases then disappears.

2. The Front Surface Field (FSF) Cell. A modification of the TJC that uses a P^+ diffused layer on the front, illuminated, side was fabricated. This structure uses the front P^+ region as a field to reduce recombination of minority carriers at the front surface of this back contact structure. This structure may also improve the base layer series resistance in these very thin structures.

3. A process variation of TJC and FSF cells was demonstrated. The P-region between the N^+ and P^+ back contacts was ion implanted with boron to create a P^+ back surface field. This process variation improved V_{oc} on TJC cells from $\approx$0.58 V to $\approx$0.61-0.62 V with no reduction in J_{sc}. The resultant TJC cells have AM0 efficiency as high as 14.3%. The anticipated AM1 efficiency should be $\approx$17%.

4. The TJC Device Model. A device model for the TJC in which device operation is modeled as a transistor. The floating front N^+ layer is a photoemitter, the P-region is the base and the back N^+ layer is the collector. The model explains the excellent response observed for this structure.

5. Optimized Packing Efficiency for Photovoltaic Modules. A relationship between cell size and module size including frame area can be developed to calculate optimum cell and module sizes for highest packing efficiency.

SECTION V
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SECTION VI
PROGRAM SUMMARY

Figure 34 shows the work plan status. All scheduled activities for 1978 are complete.

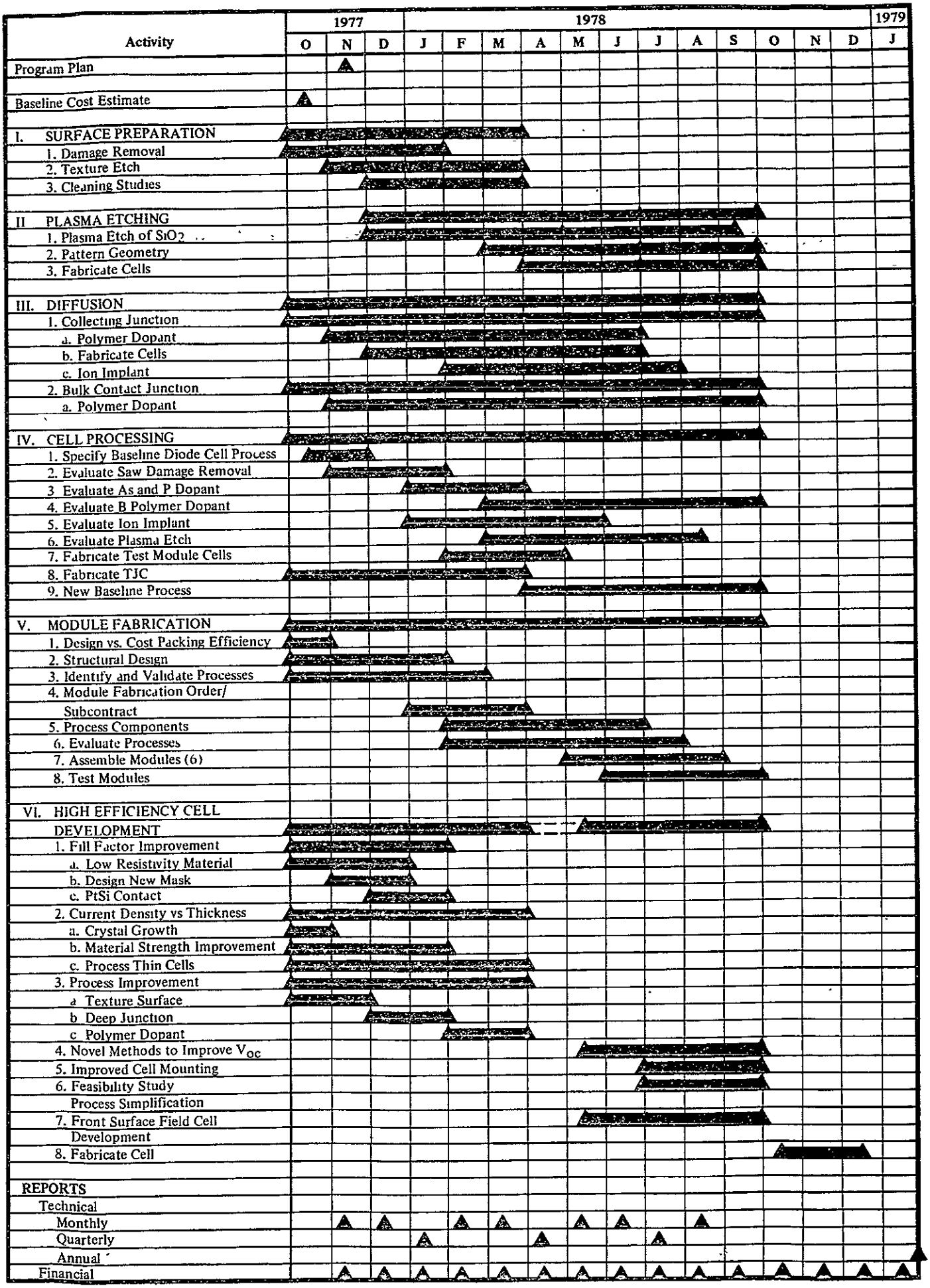


FIGURE 34. WORK PLAN STATUS