9950-52

ERDA/JPL - 954605 - 78/5
Distribution Category UC-63

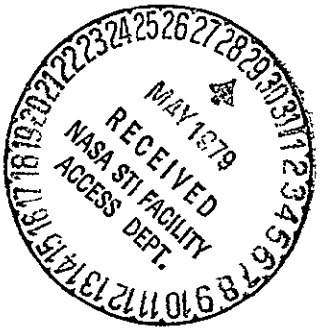
# DEVELOPMENT OF LOW-COST, HIGH ENERGY-PER-UNIT-AREA SOLAR CELL MODULES

FINAL REPORT

Gregory T. Jones, Sanjeev Chitre

Sang S. Rhee

April 1978




JPL CONTRACT NO. 954605

Sensor Technology, Incorporated
21012 Lassen Street
Chatsworth, California 91311



This work was performed for the Jet Propulsion Laboratory California Institute of Technology, under NASA Contract NAS7-100 for the U.S. Department of Energy (DOE).

The JPL Low-Cost Silicon Solar Array Project is funded by DOE and forms part of the DOE Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays.

This report contains information prepared by Sensor Technology, Incorporated under a JPL subcontract. Its content is not necessarily endorsed by the Jet Propulsion Laboratory, California Institute of Technology, the National Aeronautics and Space Administration or the U.S. Department of Energy.

## PREFACE

The information presented in this final report represents the work performed from January 12, 1977 through April 30th, 1978 by Sensor Technology, Inc., in Chatsworth, California. The technical program manager is Gregory T. Jones. The principle investigator is Sanjeev Chitre. Contributors include Sang S. Rhee, Paul A. Dennis, Charles Snyder and Priscilla Marlowe.

The JPL Technical Program Manager is Brian Gallagher.

## ABSTRACT

Development of low-cost, high energy-per-unit-area solar cell modules was conducted in this program. This final report covers the development of two hexagonal solar cell process sequences, a laser-scribing process technique for scribing hexagonal and modified hexagonal solar cells, a large throughput diffusion process, and two surface macrostructure processes suitable for large scale production. Experimental analysis was made on automated spin-on anti-reflective coating equipment and high pressure wafer cleaning equipment. Six hexagonal solar cell modules were fabricated; they demonstrated that module efficiency can be significantly improved by the utilization of hexagonal or modified hexagonal solar cells replacing round solar cells due to increased solar cell packing ratio and increased solar cell photovoltaic energy conversion efficiency.

Also covered in this report is a detailed theoretical analysis on the optimum silicon utilization by modified hexagonal solar cells for low-cost, high energy-per-unit-area solar cell modules. It was shown that an optimum modified hexagonal solar cell module will produce a cost savings compared to a round cell module.

A cost analysis was performed using SAMICS on all process steps in this program. Two model companies were studied: CELLCO, a company that produces solar cells from silicon wafers, and MODULCO, a company that assembles solar cell modules from solar cells and encapsulant materials. The SAMICS method was applied to the hexagonal solar cell module using Sensor Technology's current proprietary process steps and three new process procedures: surface macrostructure, diffusion, and laserscribe. The conclusions show that the 1978 LSSA cost goal of $7/Wpk for solar cell modules is achievable. It is recommended, however, that significant development efforts be directed toward low-cost silicon wafer materials, low-cost encapsulant materials, and process automation.

TABLE OF CONTENTS

## LIST OF FIGURES

## LIST OF TABLES

# INTRODUCTION

Solar cell module costs are high at the present time and photovoltaic energy conversion efficiencies are low. Major contributing factors to high costs are solar cell materials, module encapsulation materials, and production processing techniques. Contributing factors to low module efficiencies are low solar cell efficiencies and low solar cell packing ratios.

Development of low-cost, high energy-per-unit-area solar cell modules is the overall goal of this program. This goal was approached in two phases. The primary objective of Phase I was improvement in solar cell module efficiency by increasing the solar cell packing ratio which is the ratio of solar cell surface area to module surface area. Hexagonal solar cells scribed by laser from 90 millimeter Czochralski silicon wafers were utilized in the fabrication of three densely packed hexagonal solar cell modules. The primary objective of Phase II was the improvement in solar cell module efficiency through utilization of low-cost production process techniques. Investigations

were performed on a high throughput diffusion process, two low-cost surface macrostructure processes, low cost spin-on anti-reflective coatings, high pressure wafer cleaning and hexagonal solar cell grid patterns. Three densely packed modified hexagonal solar cell modules were fabricated. A modified hexagonal solar cell is the figure resulting when a hexagon is cut from a round silicon wafer with a smaller diameter than the point to point diameter of the hexagon. It allows one to optimize the utilization of silicon wafer material which will lead to minimum module costs. A detailed theoretical analysis and discussion of optimum silicon utilization by modified hexagonal solar cells for low-cost, high energy-per-unit-area solar cell modules is presented in this report. A technical and economic cost analysis of the solar cell module production process sequence is included.

## HEXAGONAL SOLAR CELL PROCESS SEQUENCE

## FOR PHASE I

The hexagonal solar cell process sequence for Phase I is outlined in Figure 1. The process begins with a single crystal silicon 90 millimeter round wafer of 0.5 - 2.0 ohm - centimeter resistivity. The wafer is then surface etched and cleaned to remove any undesirable surface damage and impurities. The wafer is diffused in $POCl_3$. The wafer is silk screen printed on the front. It is then back etched in a hydrofluoric and nitric acid solution and then the front surface resist material is stripped off the wafer. Aluminum is evaporated onto the back surface and then fired-in. A pattern is silk screen printed on the front surface. The wafer is then plated in an electroless nickel plating solution and then cleaned. The solar cell is cut into a hexagon by laserscribe. The solar cell is solder dipped and cleaned. It has the silicon glass, $SiO_2$, removed in hydrofluoric acid solution and then an anti-reflective coating of SiO is evaporated onto the solar cell or an anti-reflective coating is spun on the solar cell. Final electrical performance testing of the hexagonal solar cell is made under a tungsten solar simulator at $28^{o}C$ and at 100 $mW/cm^2$.

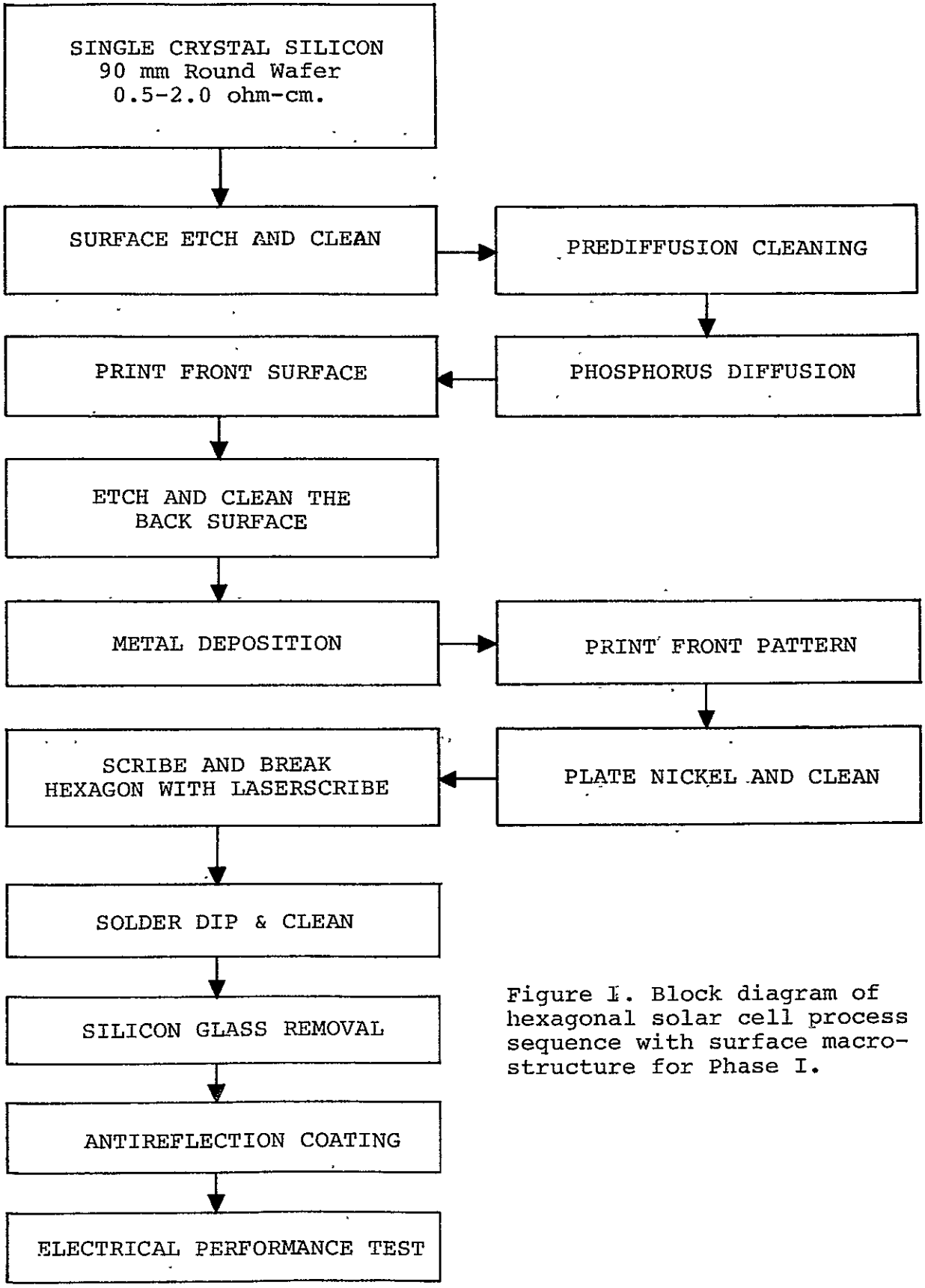



Figure 1. Block diagram of hexagonal solar cell process sequence with surface macro-structure for Phase I.

## HEXAGONAL SOLAR CELL PROCESS SEQUENCE WITH SURFACE MACROSTRUCTURE FOR PHASE II

The hexagonal solar cell process sequence with surface macrostructure for Phase II is outlined in Figure 2. The process begins with a single crystal silicon 90 millimeter round Czochralski wafer. It has a thickness of 15 mil and a resistivity of 0.5 - 2.0 ohm-centimeter. The wafers received from the manufacturer are cleaned in hot trichlorethylene, xylene and alcohol. Wax and organic contaminants are removed. The silicon wafers are next etched in a solution of NaOH and water to produce a surface macrostructure. A prediffusion cleaning process is added to remove any acid and undesirable material. The wafer is diffused in $POCl_3$. The wafer is silk screen printed on the front. It is then back etched in a hydrofluoric and nitric acid solution and then the front surface resist material is stripped off the wafer. Aluminum is evaporated onto the back surface and then fired-in. A pattern is silk screen printed on the front surface. The wafer is then plated in an electroless nickel plating solution and then cleaned. The solar cell

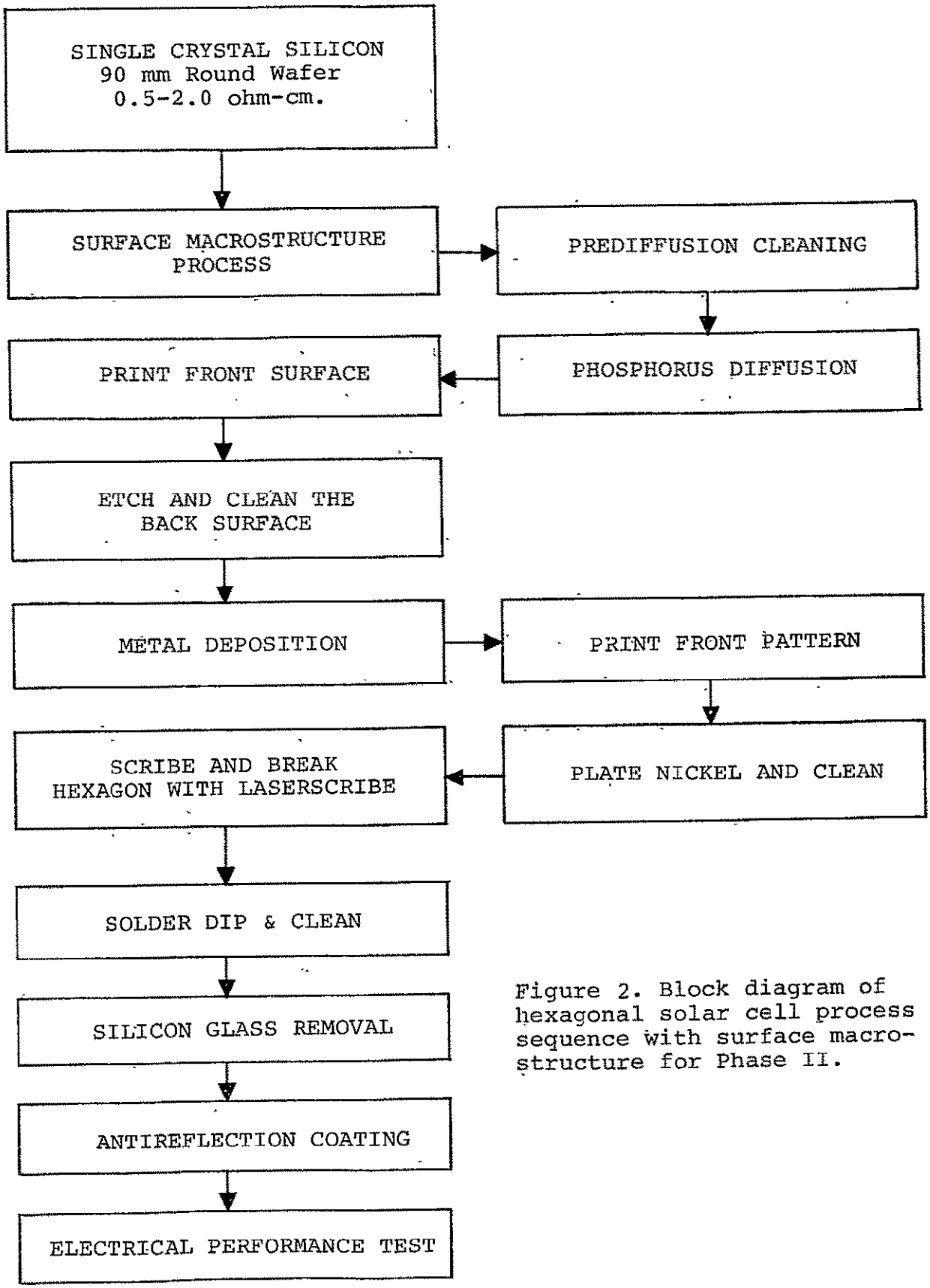



Figure 2. Block diagram of hexagonal solar cell process sequence with surface macrostructure for Phase II.

is cut into a hexagon by laserscribe. The solar cell is solder dipped and cleaned. It has the silicon glass, $SiO_2$ removed in hydrofluoric acid solution and then an anti-reflective coating of SiO is evaporated onto the solar cell or an anti-reflective coating is spun on the solar cell Final electrical performance testing of the hexagonal solar cell is made under tungsten solar simulator at $28^{o}C$ and at 100 $mW/cm^2$.

## LASERSCRIBE HEXAGONAL SOLAR CELL PROCESS

### A. Laserscribe Hexagon Computer Program

Modified hexagonally shaped wafers can be scribed from 90 millimeter or 3.54 inch diameter round silicon wafers using Quantronix Corporation's Laserscribe 603-2. The laserscribe shown in Figure 3, is controlled by a computer program which allows for optional subroutines specified by an option switch. Four options can be utilized and are listed as follows:

OPTION 1. Standard X-Y laserscribe program as specified by Quantronix Corporation. (Ref. 1)

OPTION 2. Scribe modified hexagon, as illustrated in Figure 4, with the following inputs.

a) Wafer diameter specified by two digits, i.e. X.X inches

b) Radius of circumscribed circle from one inch to two inches specified by three digits, i.e. 1.XX inches.

c) Corner cut specified by three digits, i.e. .XXX where 0, if given, means no cut.

OPTION 3. Scribe modified hexagon in half from point to point.

OPTION 4. Scribe modified hexagon in half perpendicular to Option 3 or from the center of one side of the hexagon to the center of the opposite side.

GENERAL Cuts made by the laserscribe should be within plus or minus two mils.

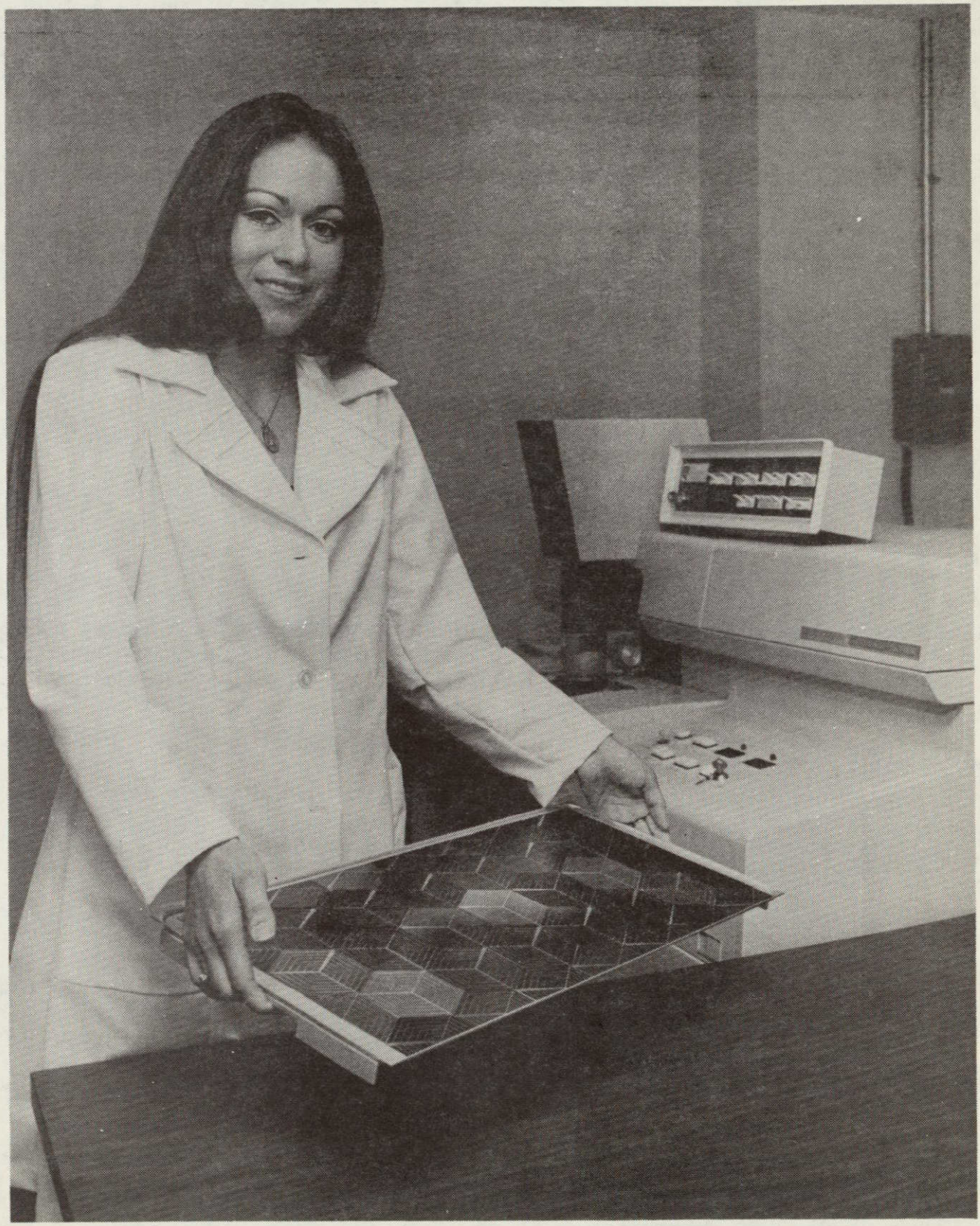




Figure 3. Quantronix Corporation's Laserscribe 603-2 and Sensor Technology's hexagonal solar cell module.

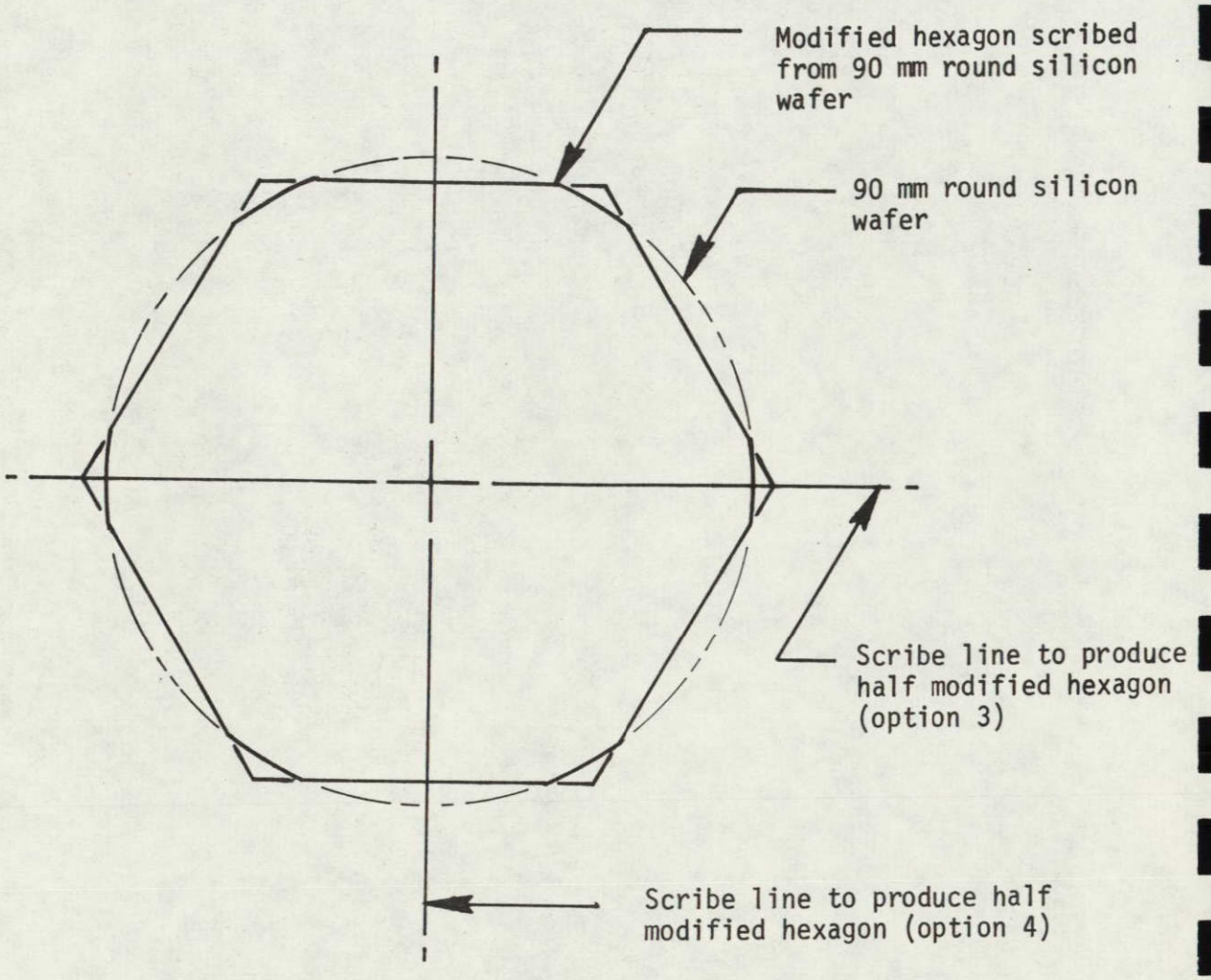



Figure 4. Modified hexagon scribed from 90 mm round silicon wafer.

B. Solar Cell Junction Current Leakage Prior to and After Laserscribing

The junction current leakage for silicon solar cells prior to and after laserscribing was compared. A 2.15 inch diameter circular solar cell with etch ring and the same cell cut into a hexagon by laserscribe is shown in Figure 5.

The p-n junction current leakage or dark reverse current ($I_{DR}$) for ten circular solar cells with etch rings and for the same solar cells cut from the front surface into hexagons by laserscribe are shown for comparison in Table 1. The ten circular solar cells with etch rings were specifically chosen to show a large variation in current leakage. The current leakage is significantly reduced when the solar cells are cut into hexagons with the laserscribe; the current leakage is reduced for some cells by more than an order of magnitude. The junction current leakage for the ten scribed hexagons is uniform and consistent, i.e. at 0.5 volts the current leakage averages .925 ma and at 4.0 volts the current leakage averages 6.4 ma for the ten solar cells.

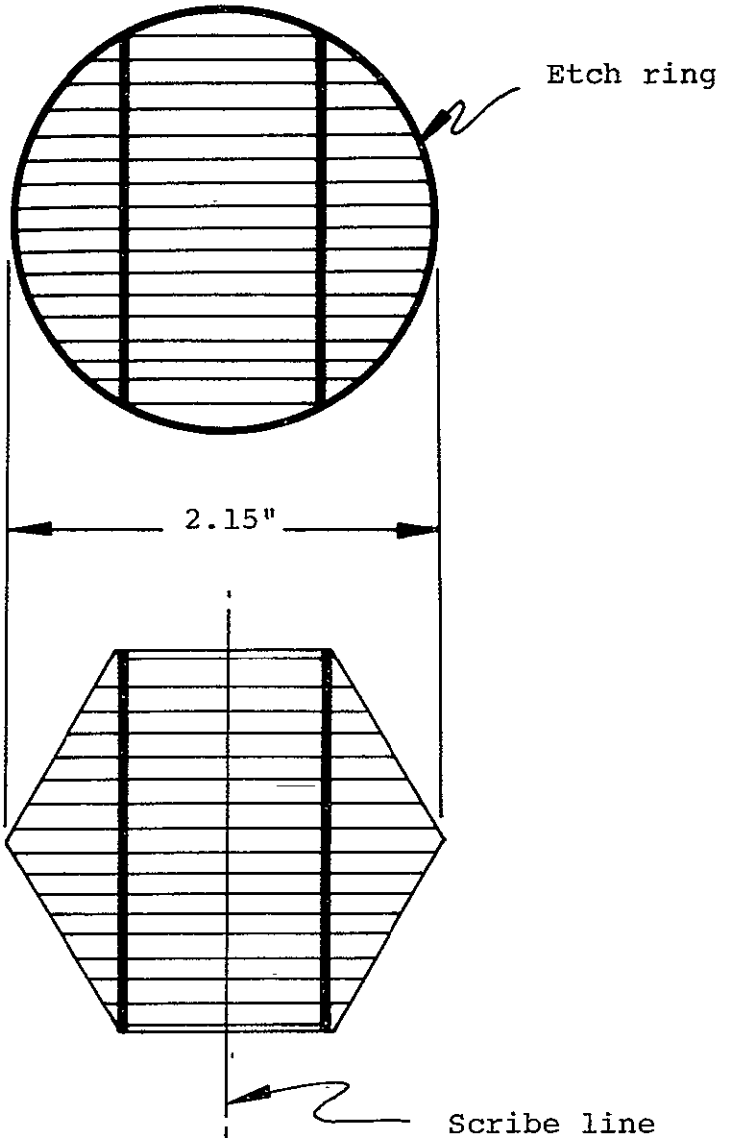



Figure 5. A 2.15 inch diameter circular solar cell with etch ring and the same cell cut into a hexagon by laserscribe. Also shown is the scribe line for cutting the hexagon into two paired halves.

| 2.15" DIAMETER CIRCULAR SILICON SOLAR CELL WITH ETCH RING | | | HEXAGON CUT BY LASERSCRIBE FROM FRONT SURFACE OF CELL | |
|---|---|---|---|---|
| Cell Number | $I_{DR}$ (ma) @ 0.5V | $I_{DR}$ (ma) @ 4.0V | $I_{DR}$ (ma) @ 0.5 V | $I_{DR}$ (ma) @ 4.0 V |
| 1 | 1.0 | 9.0 | 0.6 | 7.0 |
| 2 | 1.5 | 10.0 | 1.1 | 8.0 |
| 3 | 2.0 | 11.0 | 0.8 | 5.0 |
| 4 | 2.5 | 18.0 | 1.3 | 5.8 |
| 5 | 4.0 | 17.5 | 0.7 | ~~22.0~~ |
| 6 | 6.0 | 60.0 | 0.6 | 4.0 |
| 7 | 8.0 | 60.0 | 1.0 | 7.2 |
| 8 | 10.6 | 80.0 | 1.2 | 7.0 |
| 9 | 13.0 | 120 | 0.6 | 12.0 |
| 10 | 14.0 | 125 | 1.4 | 8.0 |
| AVE. | -- | -- | .925 | 6.4 |

Table 1. Junction current leakage ($I_{DR}$) for ten circular solar cells with etch rings and the same solar cells cut from the front surface into hexagons by laserscribe.

The p-n junction current leakage for ten circular solar cells with etch rings and for the same solar cells cut from the back surface into hexagons by laserscribe are shown in Table 2. The ten circular solar cells with etch rings were specifically chosen to show a large variation in current leakage. The current leakage is significantly reduced when the solar cells are cut into hexagons with the laser-scribe; the current leakage is reduced for some cells by more than an order of magnitude. The junction current leakage for the ten scribed hexagons is uniform and consistent, i.e. at 0.5 volts the current leakage averages 0.80 ma and at 4.0 volts the current leakage averages 4.8 ma for the ten solar cells.

The junction current leakage is small and very nearly the same for the hexagonal solar cells whether they were cut by laserscribe from the front of the cell, thus cut through the p-n junction, or whether they were cut by laserscribe from the back of the cell thus the cell is broken or cleaved through the p-n junction. Therefore, it can be concluded that the laserscribe can cut through the p-n junction without damaging the junction.

| 2.15" DIAMETER CIRCULAR SILICON SOLAR CELL WITH ETCH RING | | | HEXAGON CUT BY LASERSCRIBE FROM BACK SURFACE OF CELL | |
|---|---|---|---|---|
| Cell Number | $I_{DR}$ (ma) @ 0.5 V | $I_{DR}$ (ma) @ 4.0 V | $I_{DR}$ (ma) @ 0.5 V | $I_{DR}$ (ma) @ 4.0 V |
| 11 | 0.6 | 3.8 | 0.5 | 3.2 |
| 12 | 0.8 | 5.0 | 0.75 | 2.4 |
| 13 | 1.2 | 8.0 | 0.3 | 2.8 |
| 14 | 1.4 | 11.0 | 1.0 | 6.2 |
| 15 | 1.6 | 11.0 | 1.25 | 4.0 |
| 16 | 1.8 | 10.0 | 0.8 | 6.0 |
| 17 | 2.2 | 17.5 | 1.0 | 9.0 |
| 18 | 3.5 | 40.0 | 0.6 | 3.5 |
| 19 | 5.0 | 32.0 | ~~1.75~~ | ~~14.0~~ |
| 20 | 6.5 | 65.0 | 1.0 | 6.0 |
| AVE. | -- | -- | 0.8 | 4.8 |

Table 2. Junction current leakage ($I_{DR}$) for ten circular solar cells with etch rings and for the same solar cells cut from the back surface into hexagons by laserscribe.

The p-n junction current leakage for six circular solar cells with etch rings and for the same solar cells cut from the front surface into two "half" hexagons by laserscribe are shown in Table 3. It is observed that the sum of the current leakage of the two paired half hexagons is considerably less than the current leakage of the circular solar cells with etch rings.

The p-n junction current leakage for six circular solar cells with etch rings and for the same solar cells cut from the back surface into two "half" hexagons are shown in Table 4. It is observed that the sum of the current leakage of the two paired half hexagons is considerably less than the current leakage of the circular solar cells with etch rings.

Whether the paired half hexagons are cut by laserscribe from the front surface or back surface, the current leakage are not always paired identically, but are averaged nearly the same for the twelve solar cells. This would suggest that the differences in junction current leakage is due to non-uniform current leakage within the solar cell.

| 2.15" DIAMETER CIRCULAR SILICON SOLAR CELL WITH ETCH RING | | | HALF HEXAGONS CUT FROM FRONT SURFACE OF CELL | |
|---|---|---|---|---|
| Cell Number | $I_{DR}$ (ma) @ 0.5 V | $I_{DR}$ (ma) @ 4.0 V | $I_{DR}$ (ma) @ 0.5 V | $I_{DR}$ 9ma) @ 4.0 V |
| 21 | 0.6 | 3.8 | 0.2/0.2 | 1.0/1.0 |
| 22 | 0.75 | 10.0 | 0.7/0.1 | 5.0/0.6 |
| 23 | 0.8 | 8.0 | 0.3/0.3 | 3.5/1.8 |
| 24 | 1.2 | 9.0 | 0.4/0.5 | 3.0/1.8 |
| 25 | 1.5 | 17.0 | 0.7/0.2 | 4.0/1.5 |
| 26 | 2.0 | 16.0 | 0.8/1.2 | 5.5/8.8 |
| AVE | -- | -- | 0.5/0.4 | 3.7/2.6 |

Table 3. Junction current leakage ($I_{DR}$) for six circular solar cells with etch rings and for the same solar cells cut from the front surface into paired half hexagons by laserscribe.

| 2.15" DIAMETER CIRCULAR SILICON SOLAR CELL WITH ETCH RING | | | HALF HEXAGONS CUT FROM BACK SURFACE OF CELL | |
|---|---|---|---|---|
| Cell Number | $I_{DR}$ (ma) @ 0.5 V | $I_{DR}$ (ma) @ 4.0 V | $I_{DR}$ (ma) @ 0.5 V | $I_{DR}$ (ma) @ 4.0 V |
| 27 | 2.2 | 85.0 | 0.5/0.2 | 3.8/1.8 |
| 28 | 3.0 | 100.0 | 0.5/0.8 | 3.0/4.2 |
| 29 | 5.0 | 40.0 | 0.4/0.4 | 2.2/2.2 |
| 30 | 6.0 | 60.0 | 0.8/1.8 | 5.6/8.8 |
| 31 | 8.0 | 110.0 | 0.3/0.5 | 1.8/3.0 |
| 32 | 12.0 | 100.0 | 0.4/0.2 | 2.8/1.8 |
| AVE. | -- | -- | 0.5/0.6 | 3.2/3.6 |

Table 4. Junction current leakage ($I_{DR}$) for six circular solar cells with etch rings and for the same solar cells cut from the back surface into paired half hexagons by laser-scribe.

The average sum of the junction current leakage of the half solar cells cut by laserscribe from the front surface or from the back surface is approximately equal to the junction current leakage for the full hexagons cut by laserscribe from the front surface and from the back surface.

C. Silicon Wafer Laserscribing Technique

Laserscribing is accomplished by moving the silicon wafer through the appropriate pattern, which in this program is a hexagon, under a focused beam of laser light. The high intensity pulses are absorbed by the material, rapidly heating it to the boiling point, generating a kerf by evaporation of material. SEM photographs in Figure 6A and 6B show the effect of laserscribing silicon material. The duration of the pulses is sufficiently short (less than 0.5 nanoseconds) that negligible heat flows from the irradiated region via conduction; as a result, the temperature rise at a distance about one mil from the irradiated spot is only a few degrees and no performance degredation occurs.

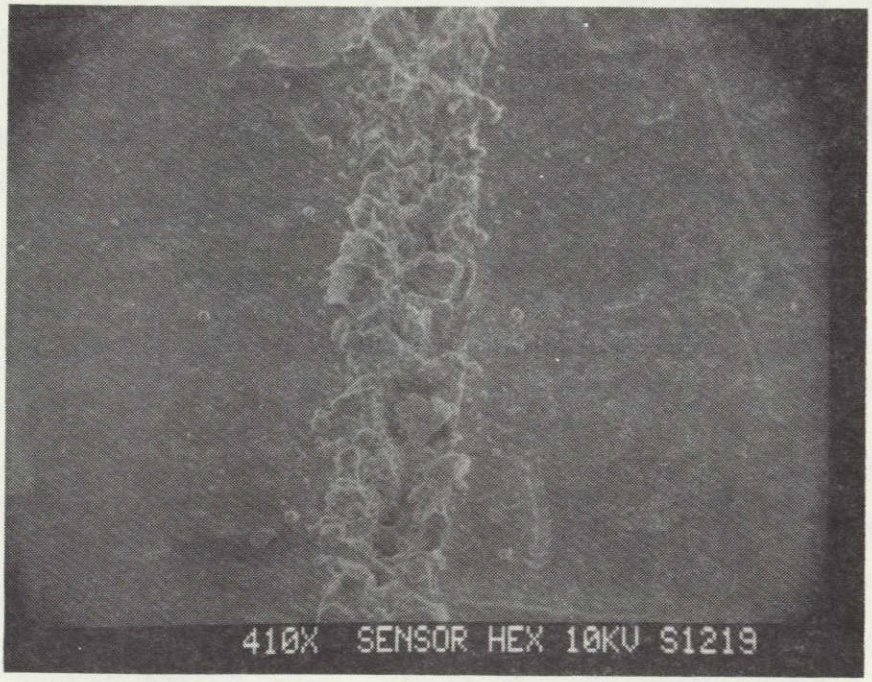



Figure 6a. SEM photograph of laserscribed silicon material at 410 X magnification.

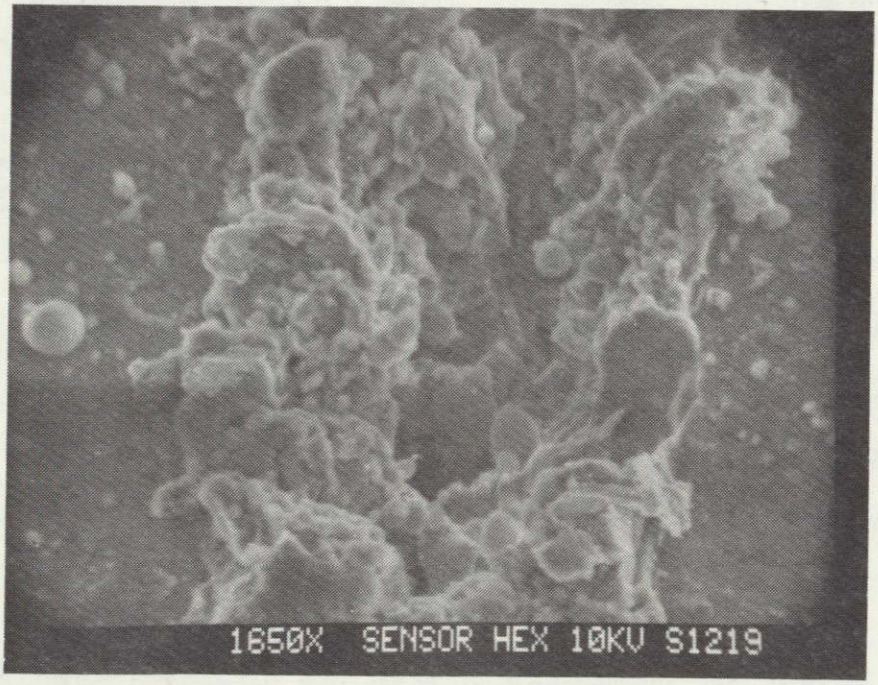



Figure 6 b. SEM photograph of laserscribed silicon material at 1650 X magnification.

The depth of the kerf need only be a few mils on typical silicon wafers so that the stress enhancement when bent assures breaking along the scribe line.

It was shown in the previous section that the laserscribe can cut through the p-n junction without damaging the junction. The technique, however, for scribing a silicon wafer is very important.

First the silicon wafer should be aligned properly. Alignment is done manually in the laserscribe used in this program. The wafers are usually scanned prior to laserscribing to check the alignment for initial experiments. A block or stop can be made which is used to assist the operator in wafer alignment and thus eliminate the necessity of scanning each wafer prior to laser scribing.

Second, the silicon wafer can be cut by laser from the front of the cell, thus cut through the p-n junction or it can be cut by laser from the back of the cell, thus the cell is broken or cleaved through the p-n junction. There is a slightly smaller current leakage produced when the cell is cut from the back and therefore this is the preferred method. It should be noted that there is no etch ring, edge grinding, or edge etching required when the solar cells are cut by the laserscribe.

Third, silicon wafers should be scribed prior to solder coating. Experience has shown that scribing solder coated solar cells by laser produces severly shorted p-n junctions. This technique is not recommended. Scribing solder coated solar cells by laser through the back surface and then breaking or cleaving the p-n junction can be performed without major current leaking problems but the operator must be very careful when breaking the cell so that no solder pieces are left which might cross the p-n junction and short out the cell. This technique is not preferred for large scale production.

Fourth, the wafer breaking technique is performed manually. After a hexagon is scribed the six sides are broken by hand. This is done in the following manner. The solar cell is placed between the thumb and fingers of one hand; the scribe line is face up. The thumb and index finger of the second hand closes on the edge of the wafer just outside the midpoint of the scribed line and exerts a downward force on the segments and snaps the wafer.

## HIGH THROUGHPUT DIFFUSION PROCESS

Experiments were performed to determine the feasibility of diffusing 400 ninety millimeter (3.54 inches) diameter silicon wafers in one hour. The sequence of events included the use of a commercial diffusion furnace with an extended temperature flat zone, the design and fabrication of quartz boats to hold 200 wafers per cycle and the introduction of a buffer.

Experiments were set up around the commercial limitations of the length of the flat zone of the commercial furnace "Brute Ranger XL" type 373 manufactured by Thermco. The commercial flat zone available for a $5^{3}/_{4}$ inch diameter quartz tube was 30 inches for temperatures above 700°C $\pm$ ½°C. An extended flat zone of 38 inches was required. A temperature profile was measured and silicon wafers were diffused with time and flow rate held constant. The variation in wafer sheet resistivity for the initial experiments in the extended flat zone was found to be within $\pm$ 24%. A variation in solar cell efficiency was found to be within $\pm$ 1%. It was concluded that

the flatness of the extended diffusion zone if maintained to within $\pm$ 5°C could be tolerated in solar cell processing.

Quartz boats were designed and fabricated to hold one hundred 90 millimeter silicon wafers. Mechanical considerations were given to the weight of silicon, thermal stresses and ease in loading and unloading.

Two hundred 90 millimeter silicon wafers were diffused with $POCl_3$ in a 38 inch flat zone furnace with a center set temperature of 900°C $\pm$ ½°C. The gas flow was adjusted for uniformity. The sheet resistivity was measured on a left, right and center wafer in each of ten rows. Each silicon wafer was measured at five surface points. A plot of the average sheet resistivity over the silicon wafer surface was made for the left, right and center wafers in each row which is shown in Figure 7. Spots of $POCl_3$ were visible on the silicon wafers due to the spitting effect.

The spitting effect was considerably reduced by the design and fabrication of a buffer. This buffer is positioned between the diffuser and the automatic gas flow meter panel. This buffer helps to thoroughly mix the gases prior to

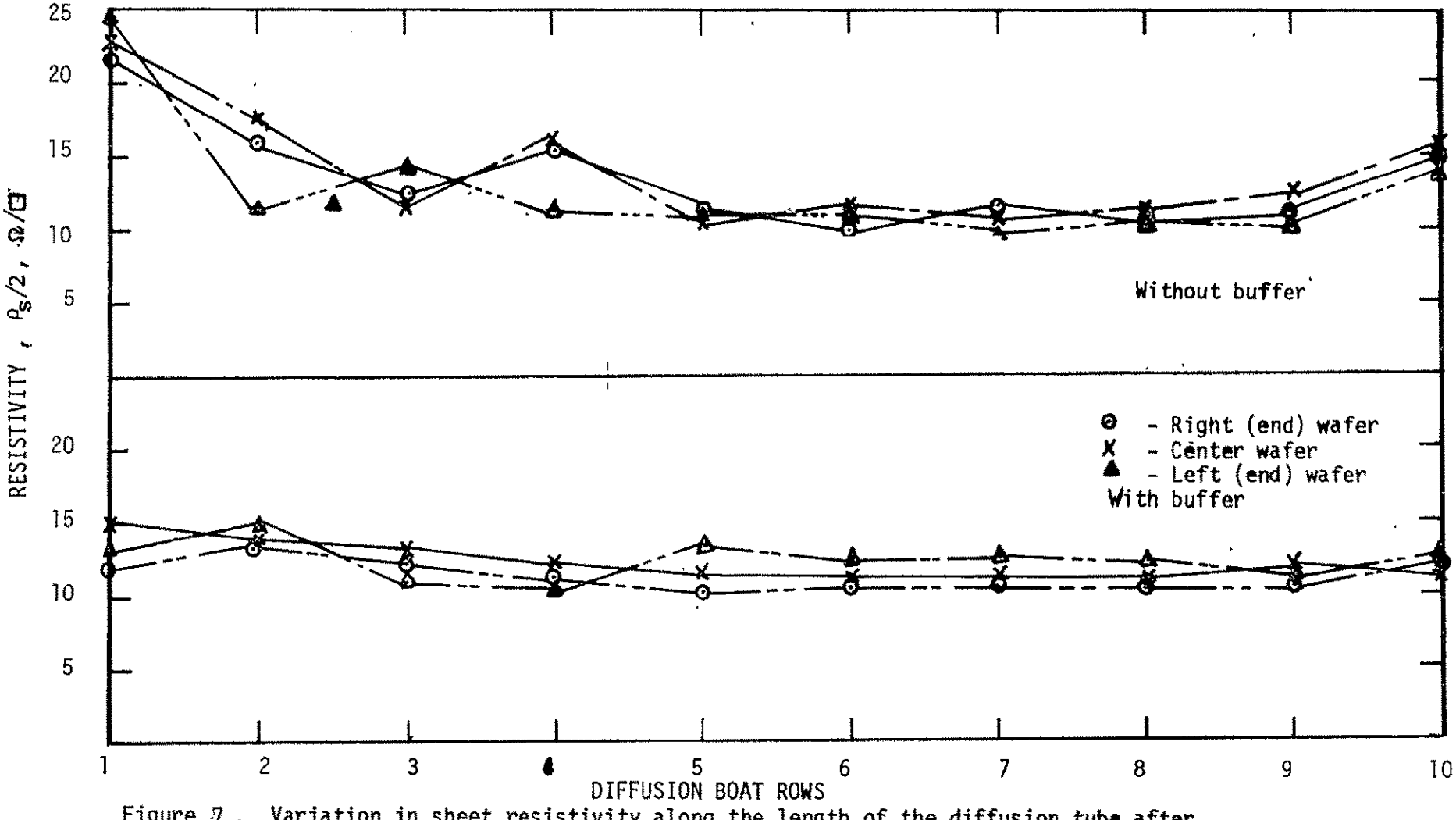



Figure 7 . Variation in sheet resistivity along the length of the diffusion tube after 200 ninety millimeter diameter silicon wafers per half hour run diffusion.

entering the diffuser and to remove traces of $POCl_3$ liquid drops which are carried by the gases. The variations in resistivity obtained with such a buffer with an extended usable temperature zone of $900^{o}C \pm 5^{o}C$ is shown in Figure 7.

It can be concluded that 400 ninety millimeter silicon wafers per hour can be diffused in a 38 inch flat zone furnace at $900^{o}C \pm 5^{o}C$ with the use of a buffer to obtain a uniform sheet resistivity within 20%. This diffusion process allows one to process solar cells in large quantities with less than 1% variation in photovoltaic energy conversion efficiency.

## SURFACE MACROSTRUCTURE PROCESS

Two surface macrostructure processes suitable for large scale production of silicon solar cells have been developed. Silicon wafer surface preparation and etching time, temperature and concentration was optimized relative to surface macrostructures that trap light efficiently. The process procedure was defined for manual large scale production. The process equipment is capable of texturizing 200 ninety millimeter diameter silicon wafers in five minutes. The silicon wafers have black antireflective surfaces which are uniformly etched and are batch to batch reproducible.

### A. Preliminary Studies

#### 1. Surface Preparation

Surface preparation prior to surface macrostructuring plays an important role on the solar cell power output. The electrical performance curves in Figure 8 shows the effect on surface preparation time on solar cell power output. The surface preparation etchant used was a mixture of hydrofluoric acid, nitric acid, and acetic acid.* The solar cells have

---

* The surface preparation etchant was replaced by a 10% NaOH by weight to water solution in the two step surface macrostructure process number two which is discussed in section C.

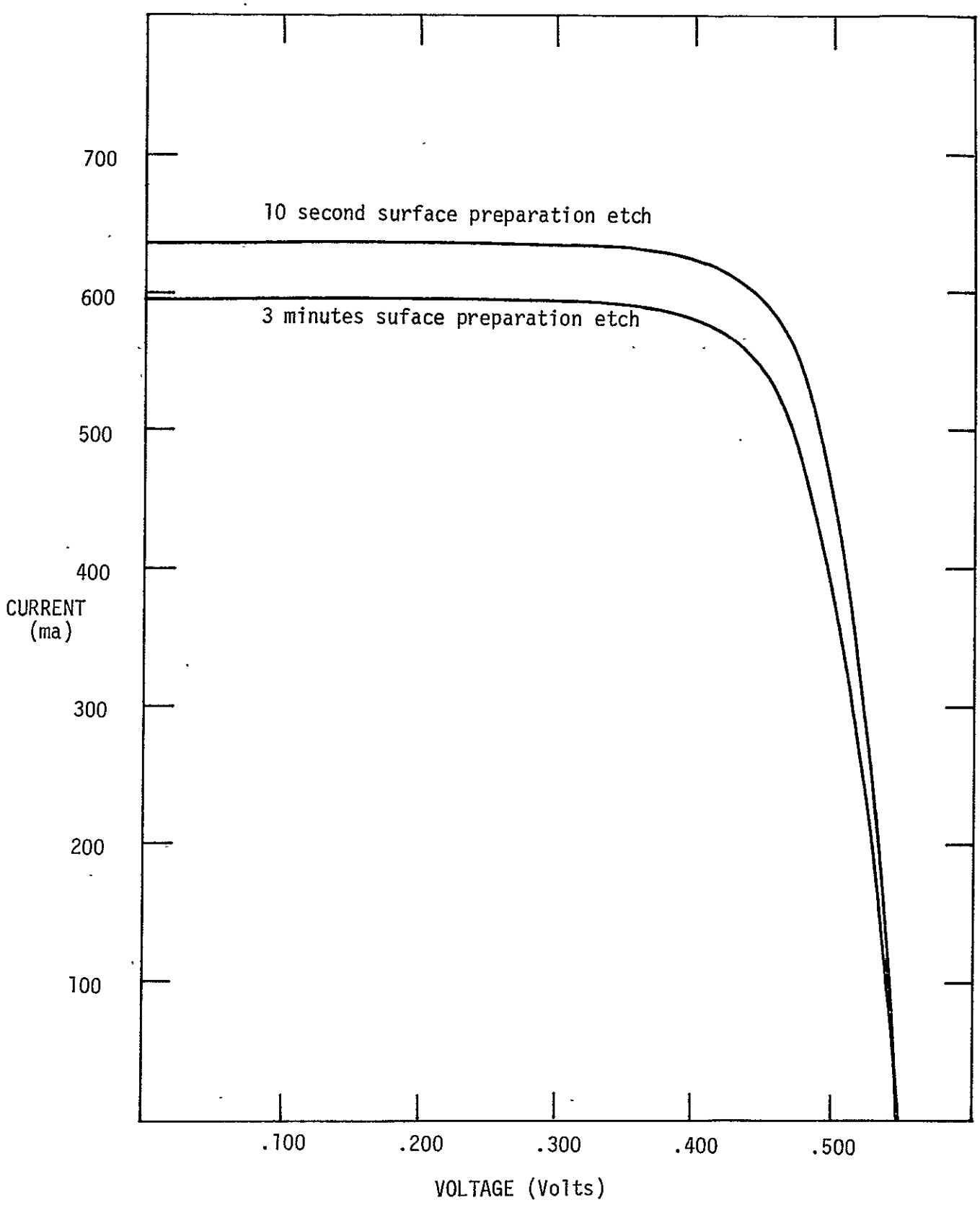



Figure 8. Electrical performance curves showing the effect of surface preparation etching time on solar cell power output.. Surface preparation etchant used is a mixture of hydrofluoric acid, nitric acid and acetic acid. The solar cells have a surface macrostructure etched 30 minutes with NaOH and have a SiO antireflection coating. The cells are measured at 28°C and at 100 mW/cm$^2$.

a surface macrostructure etched thirty minutes with NaOH and water solution and has a $SiO_2$ antireflective coating. A very short 10 second surface preparation etch significantly improves the solar cell power output above a longer 3 minute surface preparation etch. The surface preparation etch removes saw damage and roughs up the silicon wafer surface which reduces the surface macrostructure etching time and makes surface macrostructure more effective in collecting light.

2. Surface Macrostructure Studies and Experiments

A significant innovation to silicon solar cell technology has been the use of orientation dependent etches to reduce reflection from the front surface of the solar cell. Various compounds like sodium hydroxide, hydrazine, ethylene diamine, and potassium hydroxide have been successfully used for anisotropic etches (Ref. 3-9). Some experiments were performed by Sensor Technology using the surface macrostructure etching apparatus in Figure 9 for three types of solutions which are as follows: (1) KOH, isopropyl alcohol and water; (2) ethylene diamine, pyrocatehol and water; and (3) NaOH and water. Observations indicated that surface macrostructures produced by the three mixtures significantly improved the photovoltaic energy conversion

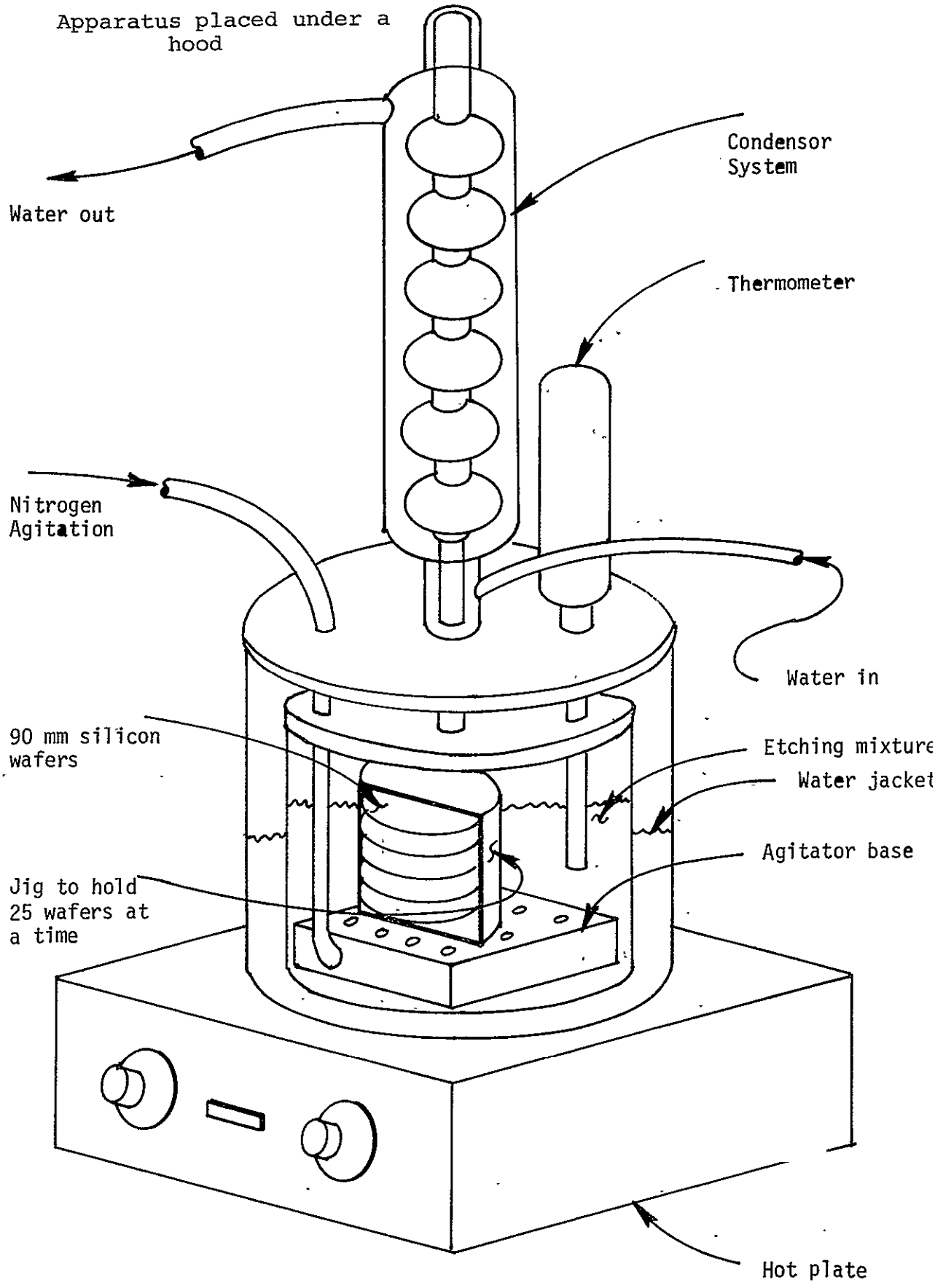



Figure 9. Surface Macrostructure Etching Apparatus

efficiency in silicon solar cells. The NaOH and water mixture was chosen for an indepth study in this program based on cost, safety, and ability to be used in large scale production.

Experimentation was performed on 2.15 inch diameter and 90 mm diameter silicon wafers utilizing the surface macrostructure process. A 30% NaOH/water solution at 80°C was used to etch the surface of the silicon wafers. A nitrogen bubbler was used to agitate the solution. The texturized surface was black after two minutes in the solution. However, uniformity across the silicon wafer surface was difficult to achieve and reproducibility from batch to batch was hard to obtain.

Similar experiments produced the same results with 10% NaOH/water solution at 80°C. The surface macrostructure obtained was compared to our commercial solar cell process which has a phosphor glass surface. The studies were done before and after the application of General Electric RTV-615 encapsulant. Figures 10 and 11 show the spectral response of a 1 cm. x 1 cm. surface macrostructure solar cell with RTV-615 encapsulant and our commercial process solar cell with RTV-615 encapsulant.

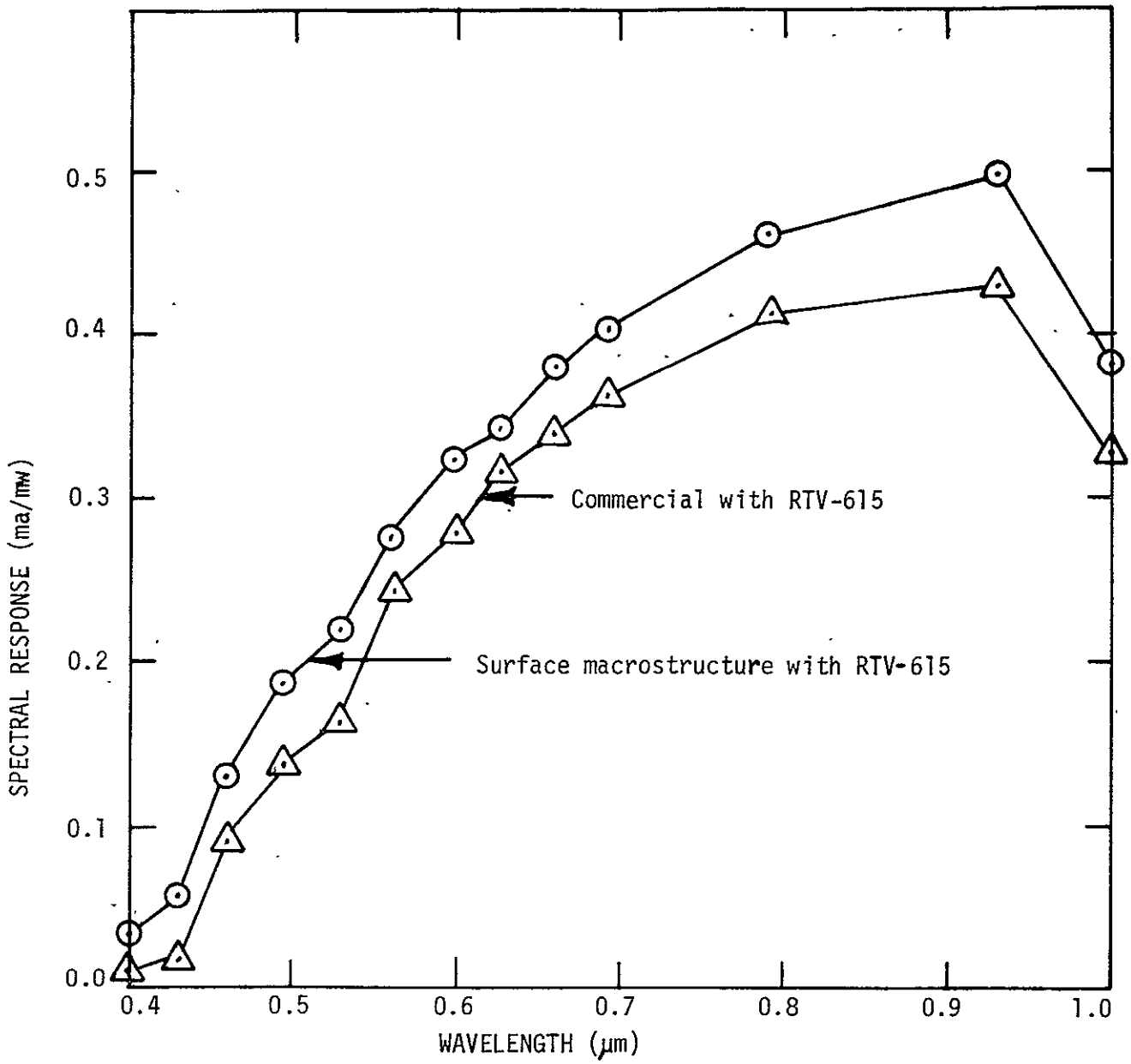



Figure 10. Spectral response curves comparing Sensor Technology's commercial solar cell with RTV-615 encapsulant and surface macrostructure solar cellwith RTV-615 encapsulant. The curves show that solar cells with surface macrostructure absorb more light than commercial process solar cells.

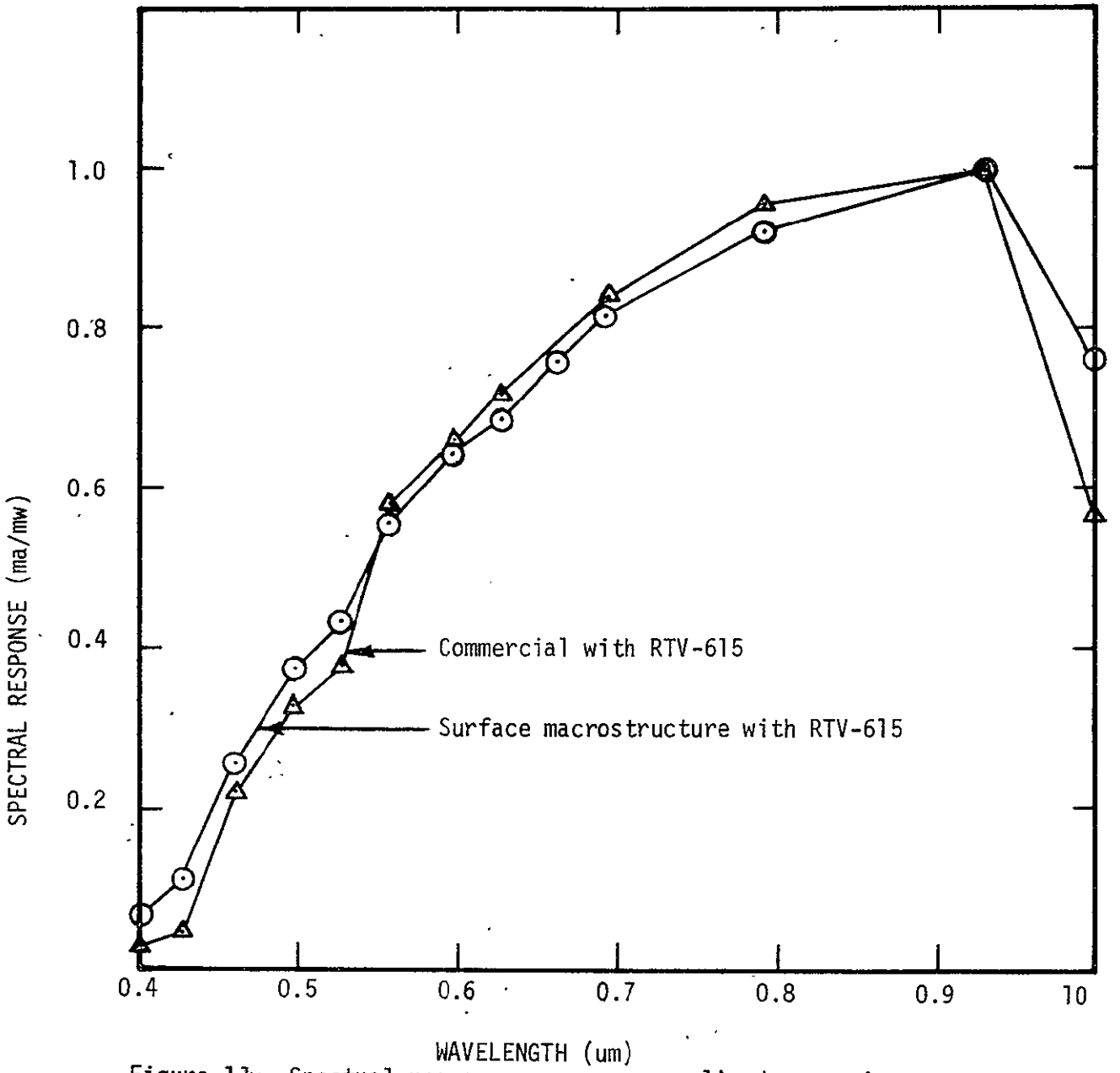



Figure 11. Spectral response curves, normalized comparing Sensor Technology's commercial solar cell with RTV 615, encapsulant and surface macrostructure solar cell with RTV 615 encapsulant. The curves show that the junction depth is the same for both solar cells.

The following observations were made:

(a) The absolute power output is higher for a solar cell with surface macrostructure than for our commercial solar cell because the former absorbs more incident radiation as shown in Figure 10.

(b) The spectral response is similar with and without RTV-615 encapsulant for solar cells with a surface macrostructure and for our commercial process solar cells. This is shown by the normalized spectral response curves in Figure 11.

(c) For solar cells with the same p-n junction depth, the solar cells with surface macrostructure absorb more light in the shorter wavelength and match the solar spectrum better than the commercial process solar cell as shown in Figure 10.

Experiments were performed utilizing an etching solution with 1% NaOH/water/isopropyl alcohol at 80$^{o}$C for 25 minutes. The nitrogen bubbler was used to agitate the solution. While uniformity across the silicon wafer surface was improved, reproducibility from batch to batch was still hard to obtain.

Further experimentation was performed with a 1% NaOH boiling water solution at 100$^{o}$C for 25 minutes. The nitrogen bubbler was not utilized. Results were very good for these experiments. The solution produced black uniform wafer surfaces, and batch to batch reproducibility was good. Experimental analysis led to the following observations:

(a) Clean silicon wafers, which are free of all organic contaminants, are required to etch uniform surface macrostructures.

(b) The wafer jig configuration was important, it affects the flow rate and thus affects the surface uniformity and batch to batch reproducibility.

(c) High concentration of NaOH/water solution etches very fast. However, batch to batch reproducibility is hard to obtain.

(d) Nitrogen agitation at a high flow rate greatly affects surface uniformity and batch to batch reproducibility.

The results of the preliminary experimentation led to two basic surface macrostructure etching solutions to be used as sample volume testing for production. The first solution consisted of 10% NaOH by weight to water. The second solution consisted of 1% NaOH by weight to water.

Two surface macrostructure process procedures were developed. Both process procedures consisted of five steps. They are (1) wafer surface cleaning, (2) surface macrostructure etching, (3) four stage cascade rinse, (4) surface macrostructure final cleaning, and (5) final rinse/spin dry. Surface macrostructure process number one utilized in step (2) 10% NaOH by weight to water.

Surface macrostructure process number two utilized, in step (2), a sequential operation with three separate solutions; 10% NaOH by weight to water followed by a hot D.I. water rinse and then 1% NaOH by weight to water. The two surface macrostructure process procedures are discussed in sections B and C.

3. Surface Macrostructure Production Process Equipment

Surface macrostructure production process equipment was designed and constructed in this program. It has large scale production capability for texturizing 200 ninety millimeter wafers in five minutes. The equipment shown in Figure 12 consists of a surface macrostructure etching tank equipped for ultrasonic agitation and nitrogen agitation. It also has a cascaded rinse system which consists of a hot ultrasonic deionized water cleaning tank with three cascaded deionized water rinse stages, a sulphuric acid hydrogen peroxide cleaning station and a final rinse/spin dry system.

## B. Surface Macrostructure Process Number One

Ninety millimeter diameter, Czochralski (100), as cut, flash etched, 20 mil thick, round silicon wafers were procured and sample inspected for experimentation. They were manually placed

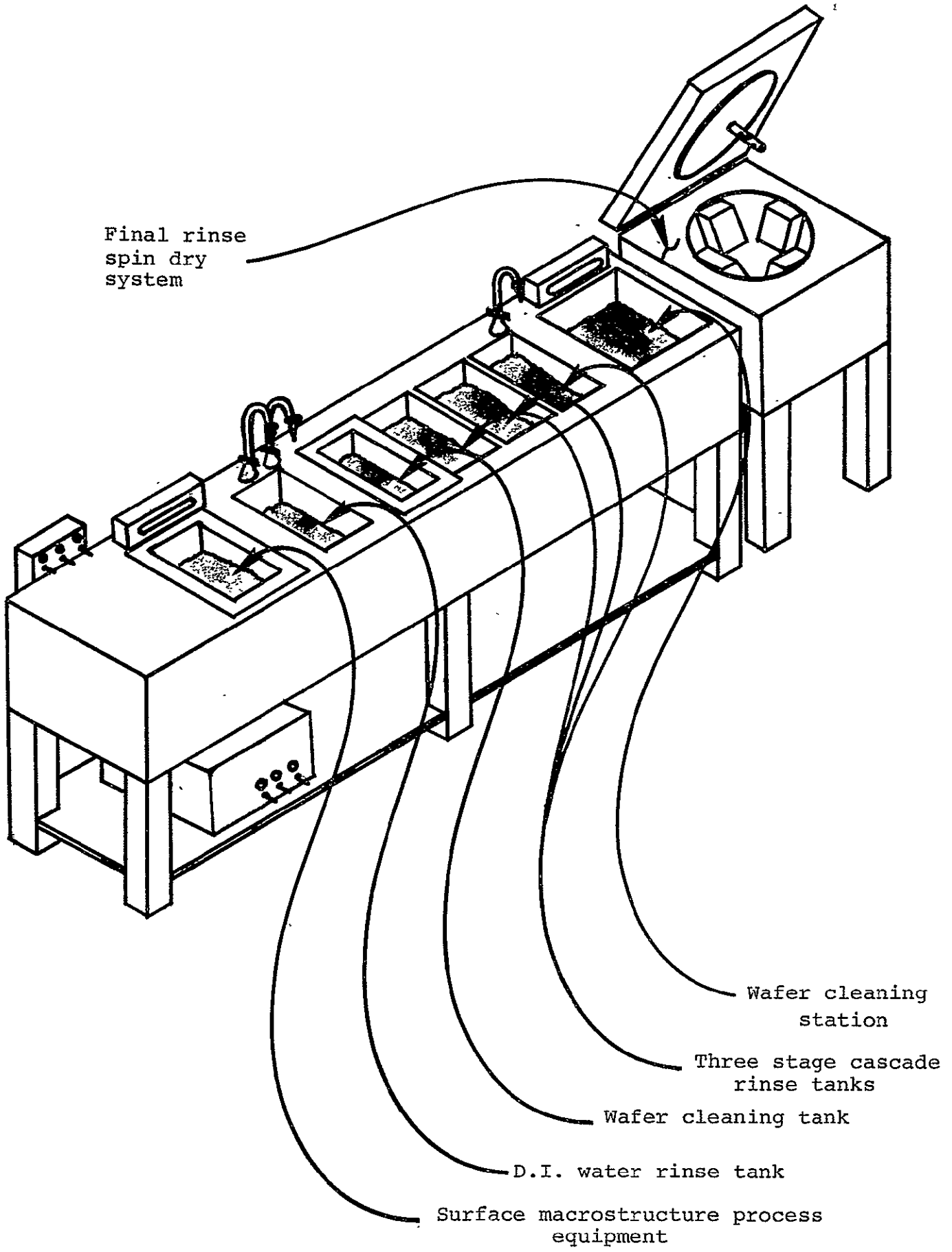



Figure 12. Sketch of surface macrostructure process equipment

into jigs which hold twenty-five wafers. Four jigs or one hundred silicon wafers were processed together.

The first step in the wafer surface macro-structure process consists of a two stage wafer surface cleaning procedure. The silicon wafers are placed into a hot trichlorethylene for five minutes (preferably in an ultrasonic tank) followed by a 5 minute methanol dip. This process step cleans any organic contaminants off the wafer surfaces which might otherwise impede surface macro-structure etching steps.

The second step in the surface macro-structure process is surface macrostructure etching. The four jigs containing the silicon wafers are introduced into an ultrasonic stainless steel tank which has been filled with a 10% solution by weight of NaOH to deionized water at $85^{o}C \pm 2^{o}C$. Suspended in the tank is a nitrogen bubbler system which is designed to agitate the solution in addition to the ultrasonics. 10 liters per minute of nitrogen gas is required for the bubbler designed by Sensor Technology, Inc. It is to be noted that the design and the placement of the bubbler with respect to the silicon wafers determines the consistency of the surface macrostructure etching process. A large amount of nitrogen bubbles which

are small in diameter contribute to uniform surface macrostructures. The process time for this step is five minutes.

The jigs are manually removed from the surface macrostructure etching tank and placed into the first ultrasonic stage of a four stage cascade rinse system which make up the third step in the process. The jigs remain for five minutes in each of the four stages. Hot deionized water flows at a rate of 3.8 liters per minute from the fourth stage where the D.I. water input temperature is $80^{o}C \pm 5^{o}C$ to the first ultrasonic stage where the D.I. water output temperature is $72^{o}C \pm 5^{o}C$. The silicon wafers get progressively cleaner as they move from the first stage to the fourth stage of the cascade rinse system.

The fourth step in the surface macrostructure process is final cleaning. The wafer jigs are manually removed from the cascade rinse and introduced into a sulphuric acid/hydrogen peroxide mixture at $70^{o}C \pm 5^{o}C$ for five minutes. This solution removes any remaining deposits of sodium hydroxide that may be trapped in the wafer surface macrostructure. The wafers are rinsed off in running D.I. water for five minutes and

are now ready for the final step in this process sequence.

The fifth step in the surface macrostructure process is the final rinse/spin dry. The last remaining wafer surface contaminants in this five minute cycle are removed. The wafers are now ready for the junction formation process.

The surface macrostructure process demonstration equipment was used to process 100 ninety millimeter diameter silicon wafers for each carrier basket or four cassettes carrying 25 wafers each. The system capability is 200 wafers per process step assuming two layers of 100 wafers each. The surface macrostructure process therefore, can produce, after the initial startup time, 2400 wafers per hour.

C. Surface Macrostructure Process Number Two

Ninety millimeter diameter, Czochralski (100) as cut, flash etched, 20 mil thick round silicon wafers were procurred and sample inspected for experimentation. They were manually placed into jigs which hold twenty-five wafers. Four jigs or one hundred silicon wafers were processed together.

The first, third, fourth, and fifth steps in the process are identical to the surface macrostructure process number one. Process step (2), surface macrostructure etching has been modified as follows: Four jigs carrying the silicon wafers are introduced into an ultrasonic stainless steel tank which has been filled with a 10% solution by weight of NaOH to deionized water at $80^{o}C \pm 2^{o}C$. Suspended in the tank is a nitrogen bubbler system which is designed to agitate the solution in addition to the ultrasonics. Approximately 10 liters per minute of nitrogen gas is required for the bubbler designed for this step by Sensor Technology, Inc. The process time is approximately five minutes which will vary according to the amount of silicon particles and contaminants in the NaOH solution. The jigs are manually removed from the tank and placed into a hot D.I. water rinse tank. The jigs are then removed and placed into a second ultrasonic stainless steel tank which has been filled with a 1% solution by weight of NaOH to deionized water at $100^{o}C \pm 2^{o}C$. Suspended in the tank is a nitrogen bubbler. Approximately 10 liters per

minute of nitrogen gas is required. The process time is approximately five minutes which will vary according to the amount of silicon particles and contaminants in the NaOH solution.

D. Technical Discussion and Results

A comparison was made between the two surface macrostructure processes. Figure 13 and 14 shows two SEM photographs of the surface macrostructures produced by the 10% NaOH by weight to water solution and also the same solution followed by a D.I. water rinse and then 1% NaOH by weight to water solution. Figure 13 is under 4000X and Figure 14 is under 2000X magnification. A comparison of the two photographs clearly shows that the surface macrostructure process number two consisting of the sequential etching solutions produces pyramidal structures that are more sharply defined than the first process. There is far less rounding of the pyramidal peaks utilizing a sequential 10% NaOH to water etch followed by a water rinse and 1% NaOH the water etching solution than through a one step process that utilizes only a 10% NaOH water solution. The surface

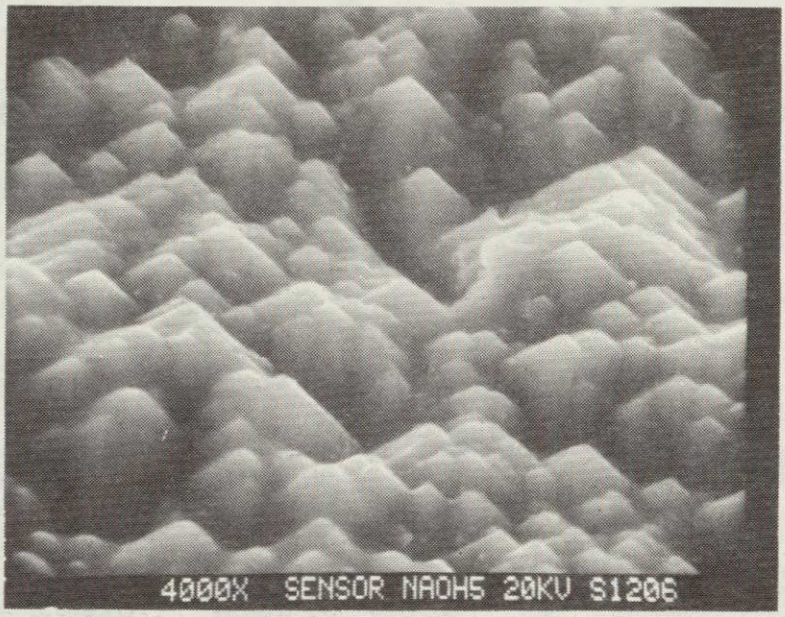



Figure 13. Surface macrostructure SEM photograph at 4000 X magnification for a silicon wafer processed in a 10% NaOH by weight to deionized water etching solution.

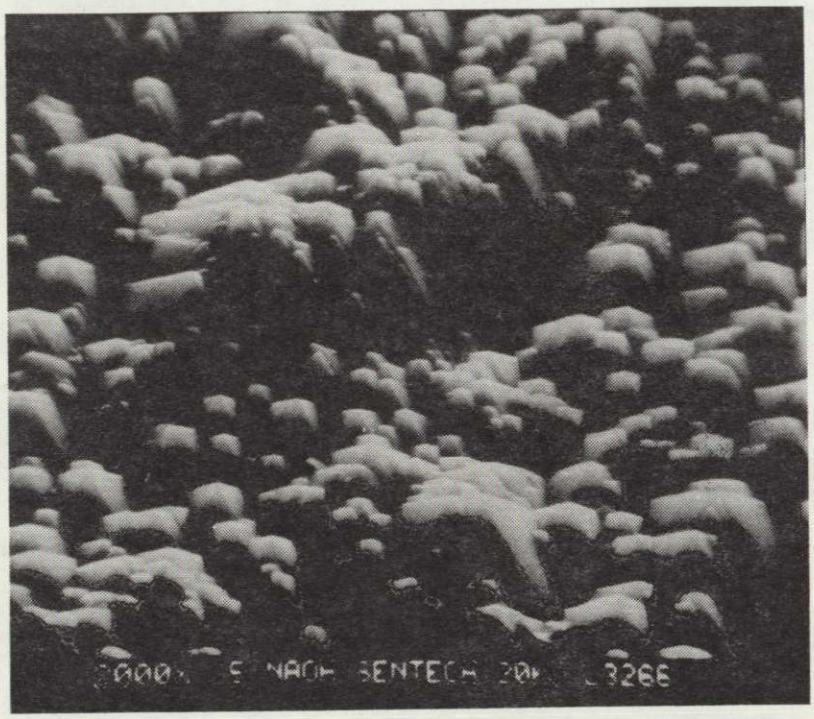


Figure 14. Surface macrostructure SEM photograph at 2000 X magnification for a silicon wafer processed in a 10% NaOH by weight to deionized water followed by a water rinse and then a 1% NaOH by weight to water solution.

macrostructure process number two produces consistent and uniform texturized surfaces and the process is batch to batch reproducible.

A more indepth study was made on the surface macrostructure process number two procedure. Various parameters like temperature of the 10% NaOH by weight to water solution, nitrogen agitation, and ultrasonic agitation were varied. The wafers thus processed were measured for short circuit current, $I_{SC}$, open circuit voltage, $V_{OC}$, and efficiency, $\eta$ . A summary of the experiments performed and their results is shown in Table 5.

Comparing batch Sentex-011 and 012 one can conclude that ultrasonics is needed for silicon wafer definition and uniformity. This result is probably due to an increased etching rate since the ultrasonic agitation helps to remove the hydrogen bubbles which would otherwise cling to the surface and inhibit further etching.

The addition of nitrogen agitation was incorporated into the process to help remove the hydrogen bubbles. The agitation flow pattern was found to be very important for silicon wafer etching uniformity. Sentex-012 in Table 5 shows the results without the use of nitrogen agitation. Sentx 013 shows the results with the use of

Table 5. Summary of surface macrostructure experiments and results for the sequential etching process consisting of 10% NaOH by weight to water followed by a deionized water rinse and then a 1% NaOH by weight to water solution.

| Batch No. | No. of Wafers | Starting Material Thickness | 10% NaOH Bath Conditions Temp. (°C) | Nitrogen (l/min) | Ultrasonic | Thickness Removed (mil) | 1% NaOH Bath Conditions Temp. (°C) | Nitrogen (l/min) | Ultrasonic | Thickness Removed (mil) |
|---|---|---|---|---|---|---|---|---|---|---|
| Sentex 011 | 15 | 20.0 mil | 80 | 0 | Off / 40KHZ | 1.2 | 100 | -- | Off | 0.3 |
| Sentex-012 | 25 | 20.0 mil | 80 | 0 | On / 40KHZ | 1.5 | 100 | -- | Off | 0.3 |
| Sentex-013 | 25 | 20.0 mil | 80 | 7 | On / 40KHZ | 1.4 | 100 | -- | Off | 0.5 |
| Sentex 014 | 25 | 20.0 mil | 80 | 7 | On / 40KHZ | 1.5 | 100 | -- | On | 0.55 |
| Sentex-015 | 25 | 20.0 mil | 80 | 10 | On / 40KHZ | 1.4 | 100 | -- | On | 0.55 |
| Sentex-016 | 25 | 20.0 mil | 80 | 10 | On / 40KHZ | 1.4 | 100 | 7 | On | 0.4 |
| Sentex-017 | 25 | 20.0 mil | 70 | 10 | On / 40KHZ | 1.1 | 100 | -- | On | 0.55 |
| Sentex-018 | 25 | 20.0 mil | 60 | 10 | On / 40KHZ | 0.8 | 100 | -- | On | 0.55 |
| Sentex-019 | 25 | 20.0 mil | 80 | 10 | On / 40KHZ | 1.4 | 100 | -- | On | 0.55 |
| Sentex-027 | 25 | 20.0 mil | 80 | 10 | On / 40KHZ | 1.4 | 100 | -- | On | 0.55 |
| Sentex-029 | 25 | 20.0 mil | 80 | 10 | On / 40KHZ | 1.4 | 100 | -- | On | 0.55 |
| Sentex-032 | 25 | 17.4 mil | 80 | 10 | On / 40KHZ | 1.25 | 100 | -- | On | 0.55 |

Table 5. continued

| No. | Batch No. | No. of Wafers | Starting Material Thickness | Total Etched Thickness | $\overline{Isc}$ (Amp) | $\overline{Voc}$ (Volts) | $\overline{\eta}$ (%) | $\eta$ Peak (%) |
|---|---|---|---|---|---|---|---|---|
| 1. | Sentex-011 | 15 | 20.0 mil | 1.5 mil | 1.455 | 0.580 | 11.12 | 12.21 |
| 2. | Sentex-012 | 25 | 20.0 mil | 1.8 mil | 1.501 | 0.580 | 11.5 | 12.45 |
| 3. | Sentex-013 | 25 | 20.0 mil | 1.7 mil | 1.457 | 0.577 | 11.41 | 12.52 |
| 4. | Sentex-014 | 25 | 20.0 mil | 2.05 mil | 1.432 | 0.585 | 11.20 | 12.3 |
| 5. | Sentex-015 | 25 | 20.0 mil | 1.95 mil | 1.630 | 0.575 | 12.75 | 13.75 |
| 6. | Sentex 016 | 25 | 20.0 mil | 1.8 mil | 1.51 | 0.580 | 11.65 | 12.90 |
| 7. | Sentex-017 | 25 | 20.0 mil | 1.65 mil | 1.414 | 0.580 | 11.06 | 12.40 |
| 8. | Sentex-018 | 25 | 20.0 mil | 1.35 mil | 1.381 | 0.580 | 10.8 | 12.0 |
| 9. | Sentex-019 | 25 | 20.0 mil | 1.95 mil | 1.104 | 0.580 | 12.55 | 13.3 |
| 10. | Sentex-027 | 25 | 20.0 mil | 1.95 mil | 1.560 | 0.580 | 12.2 | 13.4 |
| 11. | Sentex-029 | 25 | 20.0 mil | 1.95 mil | 1.687 | 0.580 | 13.2 | 13.55 |
| 12. | Sentex-032 | 25 | 17.4 mil | 1.8 mil | 1.612 | 0.580 | 12.61 | 13.31 |

nitrogen agitation. Increasing the nitrogen flow rate from 7 to 10 liters per minute increases the unformity as shown by Sentex-015.

Sentex-016 indicates that the introduction of nitrogen agitation into the 1% NaOH to water solution allows one to remove the steric hindrance of sodium silicate, thus improving the pyramid definition on the silicon surface. Also the ultrasonic agitation was retained in this process batch which helped to reduce the hydrogen bubbles and enhance the etching process.

Temperature variation results are shown in Sentex-015, 017, and 018 at 80°C, 70°C, and 60°C respectively for the 10% NaOH to water solution. Low short circuit current, $I_{SC}$, is found for batches 017 and 018 processed at low temperatures which is due to degraded pyramidal structures. The best temperature for the 10% NaOH to water solution is 80°C as shown in Sentex-015. The surface macrostructure obtained with the Sentex 015 sequential process is shown in the SEM photograph in Figure14 at 2000X magnification and in Figure 15 at 20,000X magnification. The surface appears with slightly rounded peaks but with very good pyramidal definition.

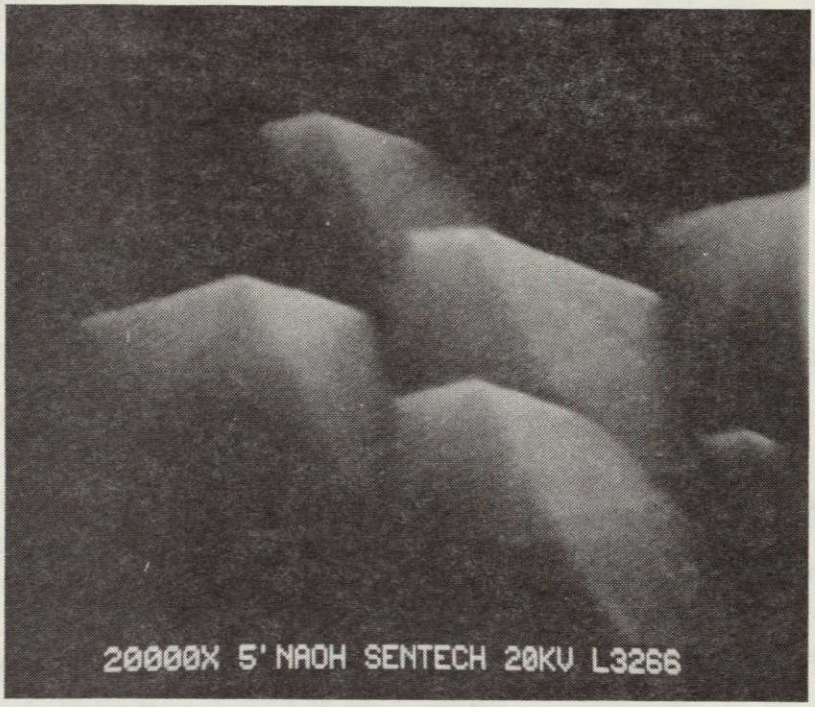



Figure 15 Surface macrostructure SEM photograph at 20,000 X magnification for a silicon wafer processed in a 10% NaOH by weight to deionized water followed by a water rinse and then a 1% NaOH by weight to water solution.

The effect of ultrasonic frequency variation is shown in batches 018 and 019. Low frequencies produce undeveloped texturized regions which are probably due to the clinging of hydrogen bubbles to the surface structure. This problem is reduced at higher ultrasonic frequencies.

Sentex 032 shows the results incurred from producing surface macrostructures on surface etched wafers. Improved energy conversion efficiencies can be obtained with the addition of the surface etching process step.

Experiments which are not part of this program were performed with the results reported in Sentex 027 and 029. Higher efficiencies can be obtained with the addition of intermediate process steps. It is recommended that future work be performed on the surface macrostructure process for producing high light collection and energy conversion efficiencies.

## SPIN-ON ANTI-REFLECTIVE COATING STUDY

The primary function of antireflective coatings is to increase the photovoltaic energy conversion efficiency of solar cells. There are presently several diverse varieties of anti-reflective coatings in common usage ranging from single to multi-layer. The standard method for depositing single layer A.R.coatings such as silicon monoxide, silicon nitride and titanium oxide to an approximate thickness of 800 Å is by means of vacuum deposition. The technological level of the equipment currently available in today's market precludes the method of vacuum deposition from being cost-effective and is thus a significant deterrent towards the attainment of a high volume low-cost throughput. With this drawback in mind, Sensor Technology has proposed the alternative procedure of spin-on anti-reflective coatings.

The solutions used in this study are titaniumsilicafilm A, B and C from Emulsitone Company, Whippany, New Jersey. Titaniumsilicafilm is a spin-on formulation which yields glassy films containing $TiO_2$ and $SiO_2$. The

indices of refraction for titaniumsilicafilm A, B and C are respectively 1.80, 1.90 and 1.96.

The Titaniumsilicafilms A, B and C were spun on textured and chemically etched wafers which were subsequently encapsulated with RTV encapsulants. Studies of spin speed vs. thickness for a given viscosity, uniformity of wafer coatings, and batch to batch reproducibility have been conducted. Spin-on equipment currently available in today's market were investigated. Automatic handling equipment made by Headway Research Inc, Macronetics and Solitec Inc., were studied for cost versus performance. The Model C-1000 wafer coating system with single track, load/unload facilities was purchased from Macronetics in Sunnyvale, California.

The Model C-1000 coater utilizes a single plane transport mechanism to convey silicon wafers through an electronically controlled process station. Push button switches control the application of power, select an operating mode (manual, semi-automatic or automatic) and control the start, stop and emergency stop, reset and carousel functions. A three digit L.E.D. indicator provides an accurate

indication of spin motor speed. Two tanks of 5 gallon capacity feed the dispense nozzles; one contains isopropyl alcohol and the other contains the A.R.film.

Each wafer is individually processed during the fully automated process sequence. In a typical coating operation a wafer is removed from the input carrier and placed on a vacuum chuck for processing. Nitrogen is initially blown against the wafer surface to remove dust and foreign material. An A.R. film is dispensed onto the wafer which is then spun at low speed to disperse the solution. The wafer is next spun at high speed to remove any excess coating solution which results in a completely uniform A.R.coating film. At the completion of the process cycle, the wafer is removed from the vacuum chuck and loaded into the output carrier.

The Model C-1000 coater used for this contract has been specifically designed to process 90mm or 3.54 inch diameter silicon wafers. The system also has the capability of processing 1.5 to 5.0 inch diameter wafers. The maximum rated throughput from this equipment is 300 wafers per hour. The mechanical yield was found to be 98%.

The experimental studies which have been formulated to investigate the viability of the spin-on-anti-reflective coating technique utilized by the Model C-1000 coater were performed on batches consisting of approximately twenty-five 90 mm diameter wafers. The experimental results obtained for any batch signify the average experimental value of its constituents.

The initial experiments were designed to study the effect of isopropyl alcohol as a solvent to reduce the A.R.solution viscosity. Various percentages of isopropyl alcohol, typically 10%, 25% or 50% by volume were mixed with the A.R. solution. The spinning speed of the Model C-1000 coater was maintained at 2000 RPM for 30 seconds and 5 cc of A.R.solution was dispensed on each wafer. It was found that by increasing the percentage of isopropyl alcohol in titaniumsilicafilm A (viscosity 30 cp), the film developed drying cracks and circles. It was therefore concluded that the addition of isopropyl alcohol to titaniumsilicafilm A did not lead to acceptable results. It was found experimentally however, that the adherence quality of the film was greatly enhanced by spinning the isopropyl alcohol prior to dispensing the A.R. film and consequently, all subsequent experiments were performed with an alcohol wetted surface.

Experiments were performed to establish the electrical characteristics and adherence quality of titaniumsilicafilm A. Titaniumsilicafilm A was spun on a surface etched batch and a texturized batch. The thickness of the A.R.coating was mathematically estimated to be 7.5 μm. This choice was based upon the height of the pyramidal surface structure engendered during the texturizing process. Under high magnification it was observed that the pyramidal surface structure was not uniformly coated with the A.R. film. In order to correct this situation, the spin speed was reduced from 2000 RPM to 1000 RPM, whereas the total spin time was maintained at 30 seconds. The representative I-V curves which portray the electrical characteristics of a cell with and without the titaniumsilicafilm A A.R.coating is shown in Figure 16 in order to accentuate the effect of the silica film. The I-V curves indicate that the solar cell which has a titaniumsilicafilm A anti-reflective coating maintains a higher energy conversion efficiency relative to the cell without an A.R. coating.

The photovoltaic energy conversion efficiencies resulting from the application of spin-on titaniumsilica films A, B, and C with respective indices of refraction of 1.80, 1.90 and 1.96 were comparatively evaluated with respect to vacuum deposited silicon monoxide and silicon nitride A.R. coatings on the basis of experimental evidence. Both the spin-on, and vacuum deposited A.R. coatings had been applied to various texturized wafers with and without encapsulation. The I-V curves of cells containing titaniumsilicafilm A, B and C and SiO are respectively presented in Figures 16, 17, 18 and 19.

Table 6 summarizes the important electrical characteristics which have been directly derived from the experimental data.

Despite the fact that titaniumsilica-film C had yielded the highest efficiency relative to the spin-on coatings, SiO and $Si_xN_y$ resulted in much more favorable efficiencies and thus comply with the stipulation set forth in this contract to develop densely packed solar cell modules with high efficiencies. Since the maximum module efficiency exhibited by the titaniumsilicafilms was in the 9% range, the SiO process was chosen for this contract.

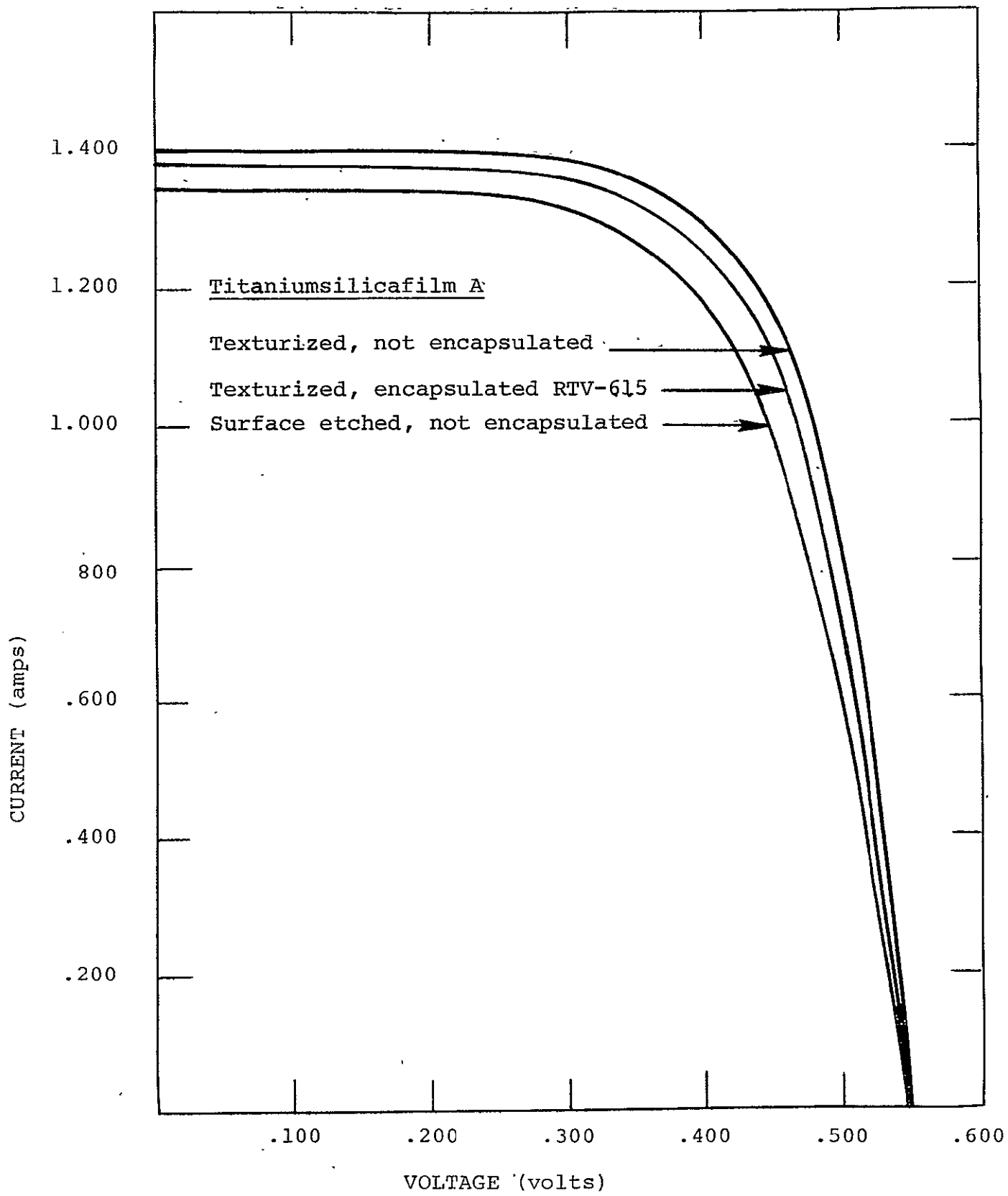



Figure 16. Titaniumsilicafilm A, $TiO_2$ + $SiO_2$, antireflective coating for three groups of solar cells. The first group is surface etched with no encapsulant. The second group is texturized and encapsulated with RTV-615. The third group is texturized with no encapsulant. The solar cells are hexagonal with 50.8 $cm^2$ active area. They are tested at 28°C, 100 $mW/cm^2$ under tungsten light.

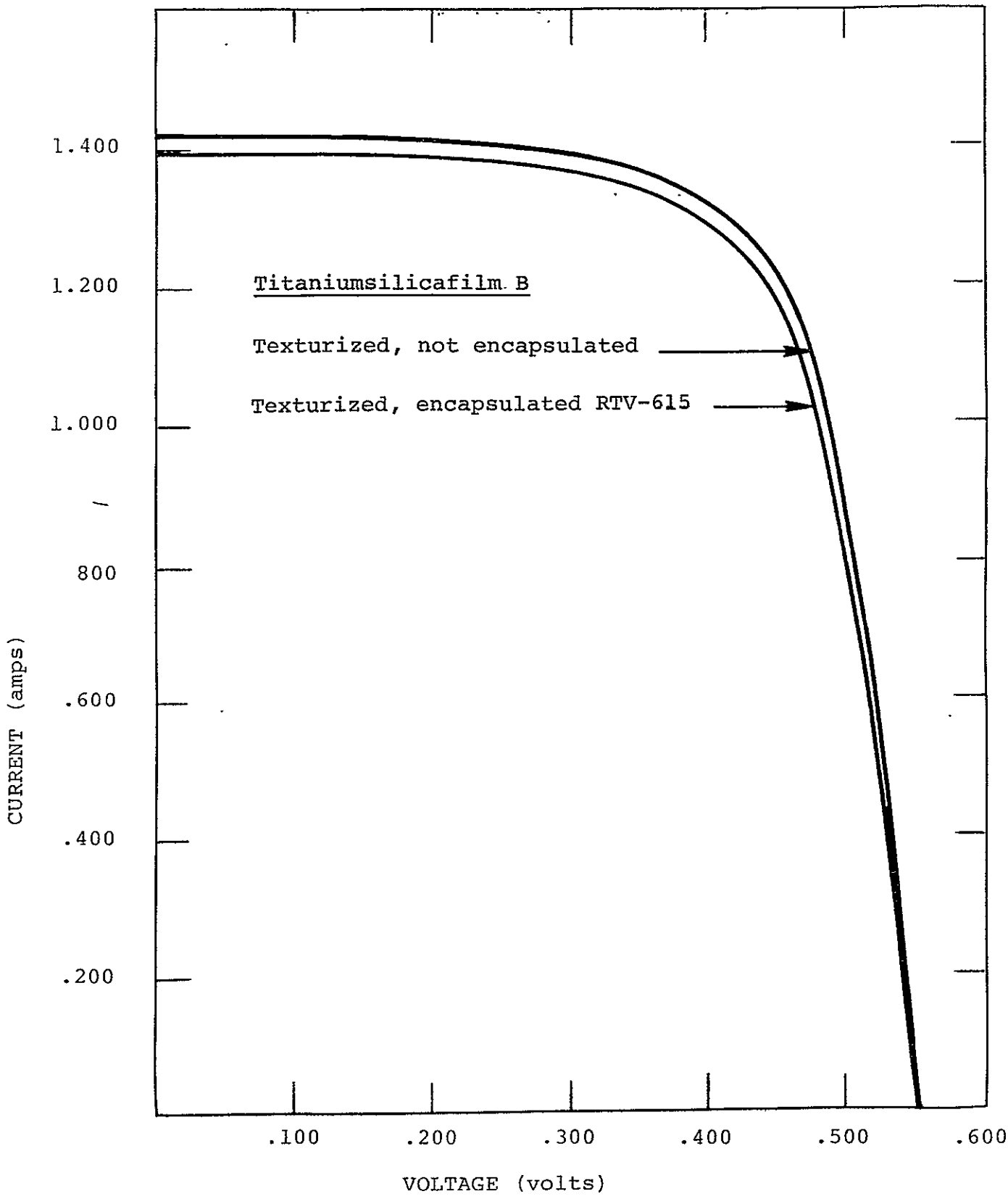



Figure 17. Titaniumsilicafilm B, $TiO_2$ + $SiO_2$, antireflective coating for cell groups without encapsulation and with RTV-615 encapsulation. The solar cells are hexagonal with 50.8 $cm^2$ active area and are texturized. They are tested at 28°C, 100 $mW/cm^2$ under tungsten light.

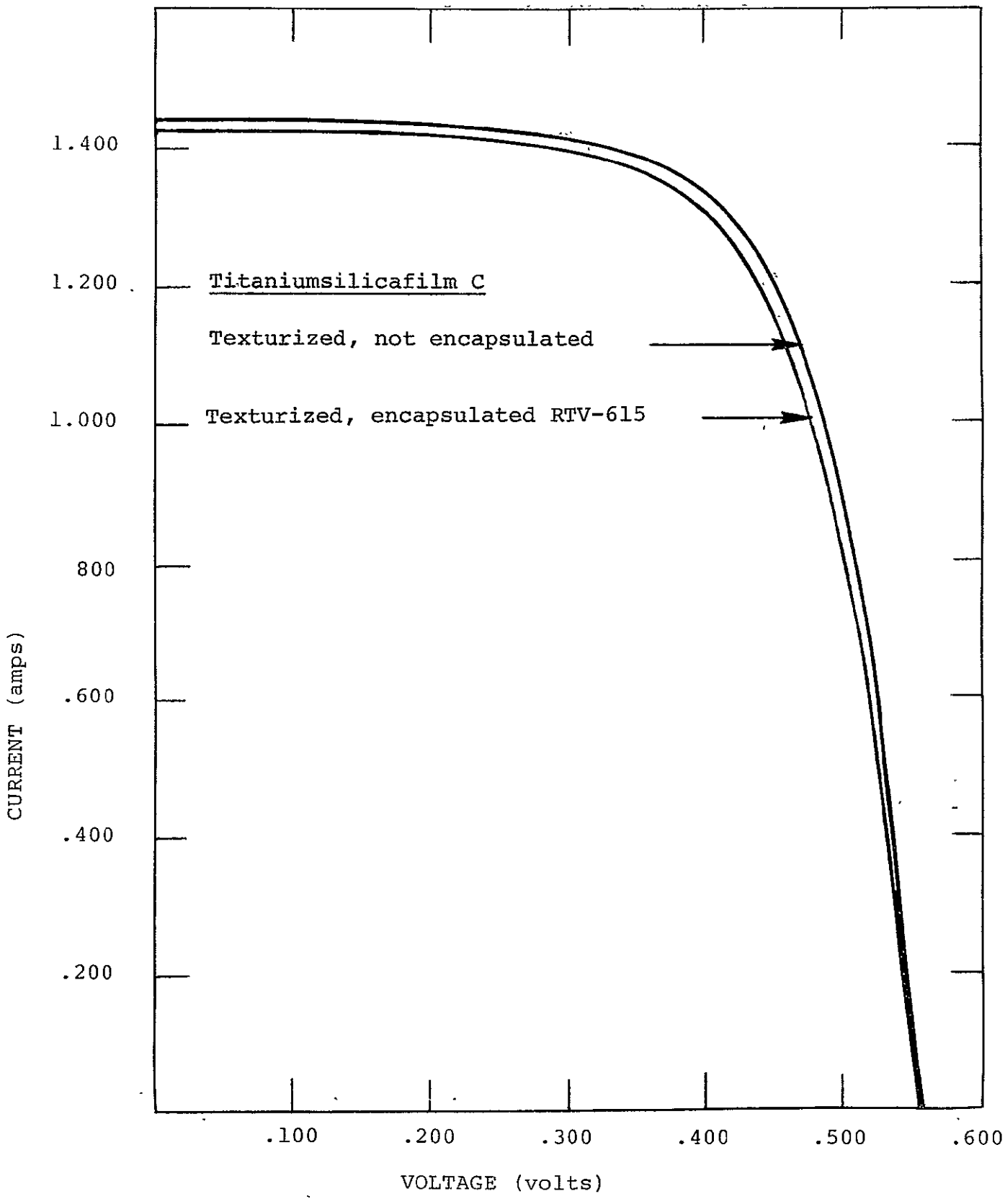



Figure 18. Titaniumsilicafilm C, $TiO_2$ + $SiO_2$, antireflective coating for cell groups without encapsulation and with RTV-615 encapsulation. The solar cells are hexagonal with 50.8 $cm^2$ active area and are texturized. They are tested at 28°C, 100 $mW/cm^2$ under tungsten light.

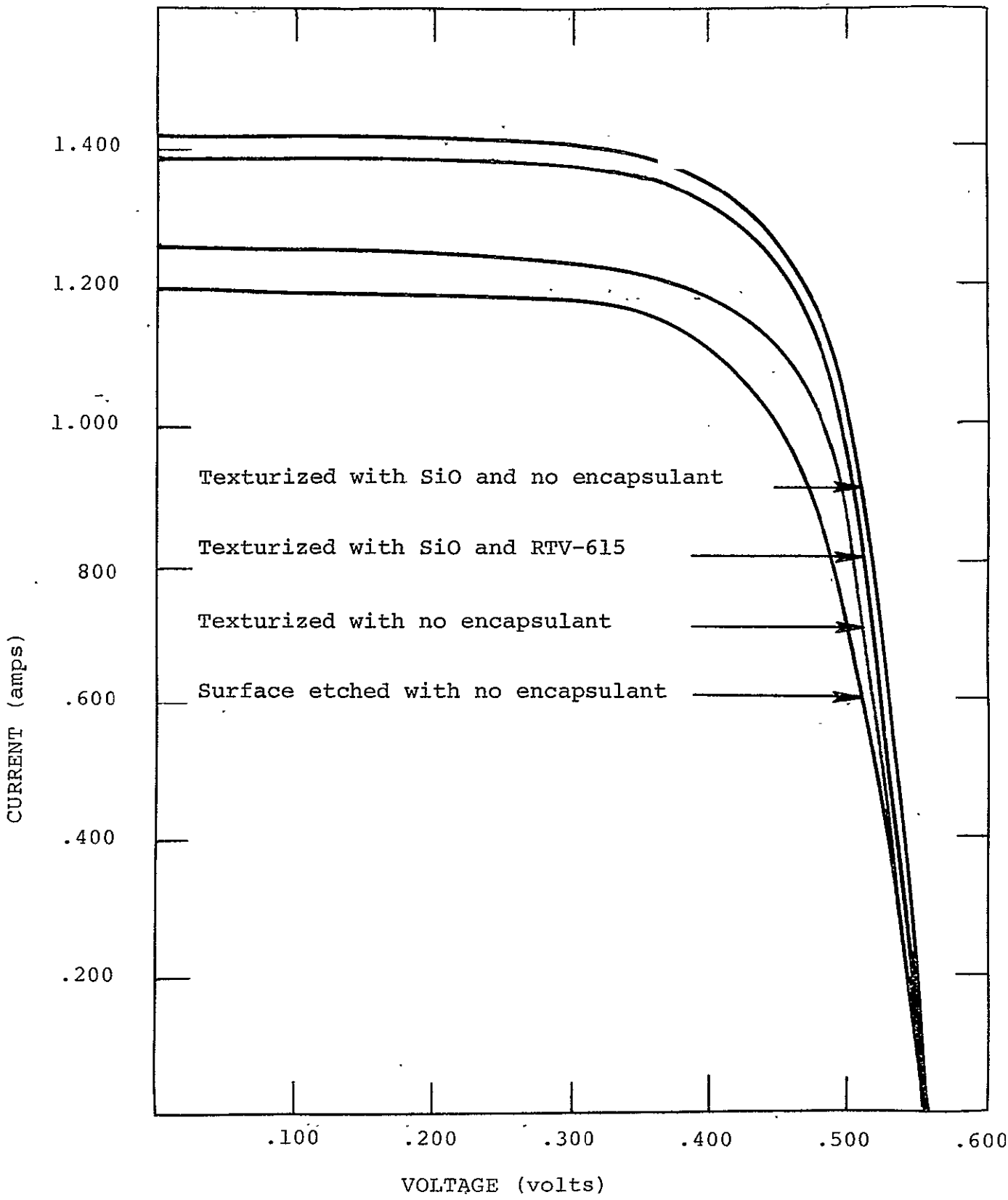



Figure 19. Electrical performance curves for four cell groups. The cells are (1) surface etched, (2) texturized, (3) texturized with SiO anti-reflective coating and (4) texturized with SiO and RTV-615 encapsulant. The solar cells are hexagonal with 50.8 $cm^2$ active area and are texturized. They are tested at 28°C, 100 $mW/cm^2$ under tungsten light.

Table 6. Comparison of the electrical performance of spin-on anti-reflective coatings with SiO and $Si_xN_y$ and with surfaced etched and texturized silicon wafers.

| Batch No. | No. of wafers | Type of film | Spin speed rpm | Type of surface | Condition of cell | $\overline{V_{oc}}$ (volts) | $\overline{I_{sc}}$ (amps) | $\overline{Eff.}$ % | Expected thickness |
|---|---|---|---|---|---|---|---|---|---|
| 1A | 10 | Tit. sil. A | 2,000 | surface etched | Un-encp. | .55 | 1.35 | 9.3 | 7.5μ |
| 1B | 10 | Tit. Sil. A | 2,000 | texturized | Un-encp. | .55 | 1.40 | 10.4 | 7.5μ |
| 2A | 25 | Tit. Sil. A | 1,000 | " | " | .55 | 1.40 | 10.4 | 15μ |
| 2B | 24 | Tit. Sil. A | 1,000 | " | Encp. | .55 | 1.37 | 10.1 | 15μ |
| 2C | 22 | Tit. Sil. B | 1,000 | " | Un-encp. | .560 | 1.42 | 10.54 | 15μ |
| 2D | 22 | Tit. Sil. B | 1,000 | " | Encp. | .555 | 1.39 | 10.2 | 15μ |
| 2E | 22 | Tit. Sil. C | 1,000 | " | Un-encp. | .555 | 1.42 | 10.75 | 15μ |
| 2F | 25 | Tit. Sil. C | 1,000 | " | Encp. | .555 | 1.4 | 10.5 | 15μ |
| 3A | 10 | SiO | Vacuum | " | Un-encp. | .555 | 1.42 | 11.15 | 800Å |
| 3B | 10 | SiO | Deposited | " | Encp. | .555 | 1.38 | 10.8 | 800Å |
| 3C | 10 | $Si_xN_y$ | Vacuum | " | Un-encp. | .555 | 1.42 | 11.3 | 785Å |
| 3D | 9 | $Si_xN_y$ | Deposited | " | Encp. | .555 | 1.40 | 11.1 | 785Å |
| 4A | 5 | ---------- | --------- | surface etched | Un-encp. | .550 | 1.20 | 8.7 | ---- |
| 4B | 5 | ---------- | --------- | texturized | Un-encp. | .550 | 1.25 | 9.9 | ---- |

## HIGH PRESSURE WAFER CLEANING EQUIPMENT

The Ultratech Plate Cleaner Model 600 manufactured by Ultratech Corporation in Santa Clara, California has been specifically designed to perform the task of cleaning masks both before and after contact printing. The two-stage cleaning cycle employed by the Ultratech Plate Cleaner Model 600 consists of (1) a high pressure stream of D.I. water which serves to extract any protruding particles which might be lodged on the plate and (2) a drying cycle which utilizes a heat lamp and the air pumped by the spinning chuck to dry the plate.

In-house experimentation pertaining to the cleaning technique utilized by the Model 600 Plate Cleaner was conducted for the purpose of establishing its throughput capability, overall cleaning performance, and adaptability to production line applications. Two potential production line applications were considered during the experimental procedure; one was the removal of printing ink residue lodged on silicon wafers, and the other was the removal of flux residue from silicon wafers. The complete removal of all printing ink residue

protruding from silicon wafers is an essential prerequesite for the establishment of good adherence characteristics from both the silicon monoxide and spin-on anti-reflective coatings. Since the Model 600 Plate Cleaner emanates a high pressure stream of D.I. water, a test was conducted to determine its cleaning capability and effect on the pyramidal surface structure engendered during the surface texturizing process. The results appeared to indicate that even though the wafers were thoroughly cleaned, the cleaning process had a much more beneficial effect on the adherence characteristics of the spin-on anti-reflective coating than with the silicon monoxide anti-reflective coating. Evidently, the adherence quality of the spin-on anti-reflective coating depends heavily on the initial cleanliness of the wafer surface. The overall process yield was 90% for 15 mil thick wafers, since the remaining 10% had been broken or cracked during the process sequence. The two-stage cleaning cycle requires ninety seconds for completion since the spray cleaning cycle required sixty seconds and the drying cycle required thirty seconds. Since the Model 600 Plate Cleaner is manually operated, the ninety-second figure advanced above will in actuality be significantly

enhanced due to the fact that only one wafer at a time can be processed, and an excessive amount of time is expended during the loading and unloading operations. The time limitations imposed by the loading and unloading operations along with the slow processing rate of this laboratory wafer cleaning equipment thus severely limits its throughput capability. The equipment, however, was adequate to demonstrate that silicon wafers can be cleaned by a high pressure stream of D.I. water. Automated wafer cleaning equipment is currently available which can process 300 wafers per hour which is acceptable for moderately large scale production.

## HEXAGONAL SOLAR CELL GRID PATTERNS

Hexagonal solar cells with the four distinct grid patterns are shown in Figure 20, 21, 22 and 23; a comparison was made between their electrical performances, shown in Figures 24, 25, 26 and 27. The solar cells have the same surface area, 50.8 $cm^2$, were processed from the same batch of silicon wafers, and were tested under the same conditions, 100 $mw/cm^2$ tungsten light at 28°C. The grid line coverage or cell shadowing loss is the same for all four patterns. All four patterns were processed the same using Sensor Technology's standard commercial process that utilizes electroless nickel plating and no special "high efficiency" process techniques. Three grid patterns were silk screen printed and one grid pattern utilized photolithography. The results are summarized in Table 7 and are discussed below:

(1) Solar cells processed under the same conditions that have the same grid line coverage are relatively insensitive to the grid line pattern used.

(2) The photolithographic process was able to produce thin grid lines and produce more grid lines per unit area than the silk screen printing process but only a slight, one-half percent, increase in efficiency was achieved which was also matched by the redundant parallel track pattern that was processed with the silk screen printing method.

(3) A single contact point or a redundant contact point produces very nearly the same electrical performance. While a half percent increase in efficiency was observed in the parallel track pattern over the 6 grid and 10 grid hexagon patterns, it was matched by the pine tree pattern that utilized a single contact point.

The electrical performance analysis of the hexagonal solar cell grid patterns was made to check the sensitivity to the grid pattern designs. An exhaustive study was not made. No large advantage was found for utilizing one pattern over another. Therefore, modules were fabricated utilizing each of the four grid pattern designs.

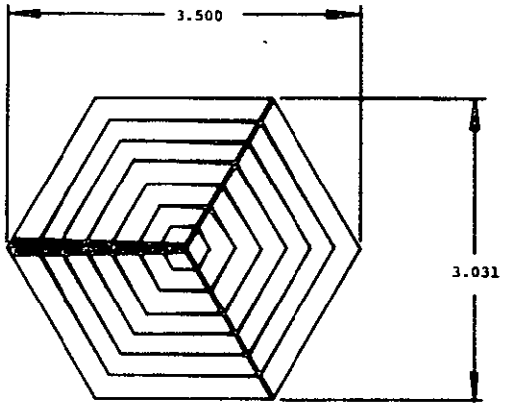



Figure 20 "Sensagon" six grid hexagonal solar cell.

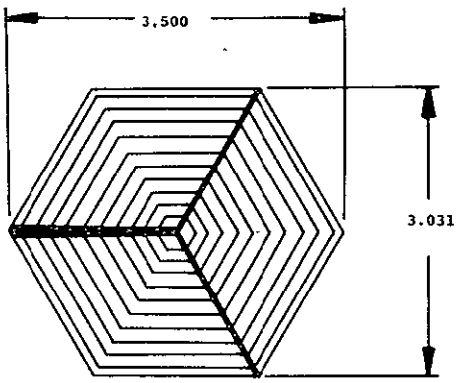



Figure 21 "Sensagon" ten grid hexagonal solar cell.

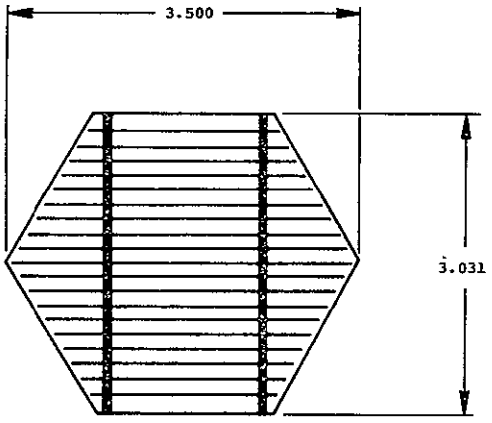



Figure 22 "Sensagon" parallel track hexagonal solar cell.

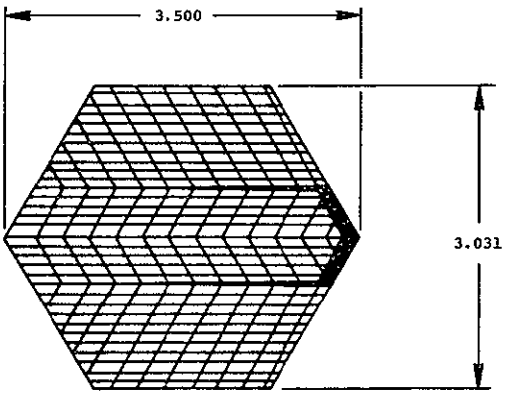



Figure 23 "Sensagon" pine tree hexagonal solar cell.

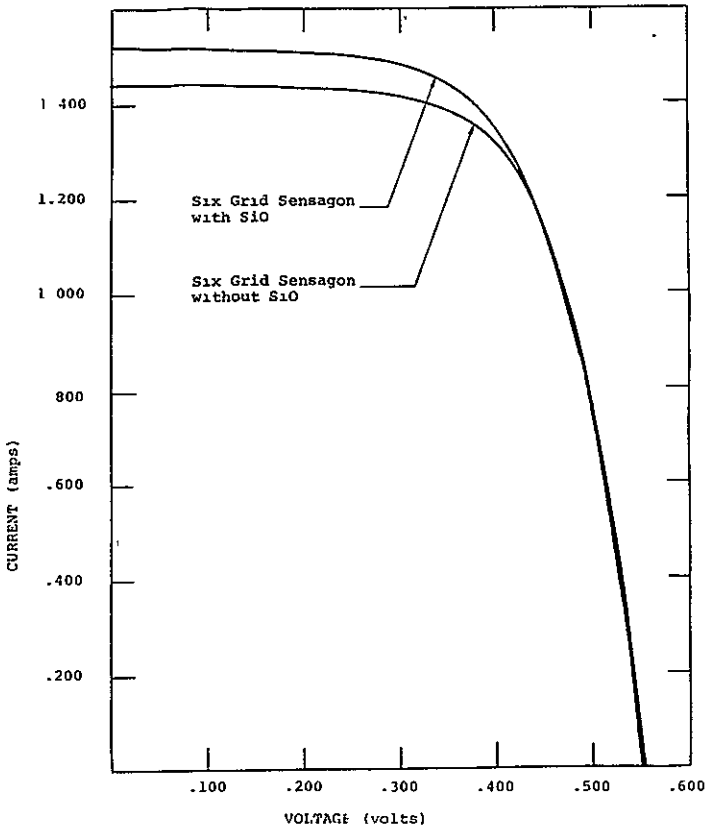



Figure 24 Electrical performance curves of a "Sensagon" six grid hexagonal solar cell, 50.8 $cm^2$, with and without S.O anti reflective coating under tungsten light at 28°C and at 100 mw/cm .

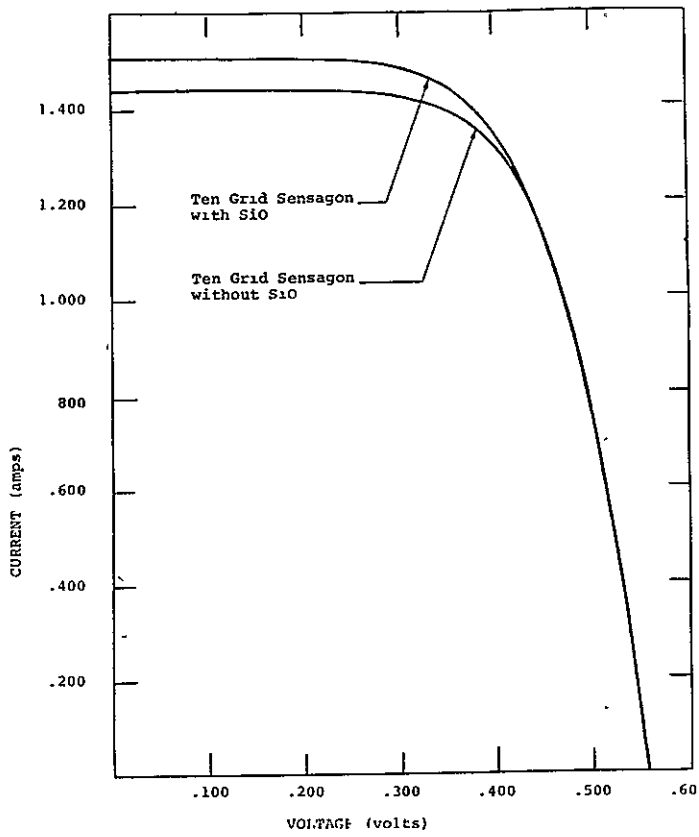



Figure 25 Electrical performance curves of a "Sensagon" ten grid hexagonal solar cell, 50.8 $cm^2$, with and without SiO anti-reflective coating under tungsten light at 28°C and at 100 mw/$cm^2$.

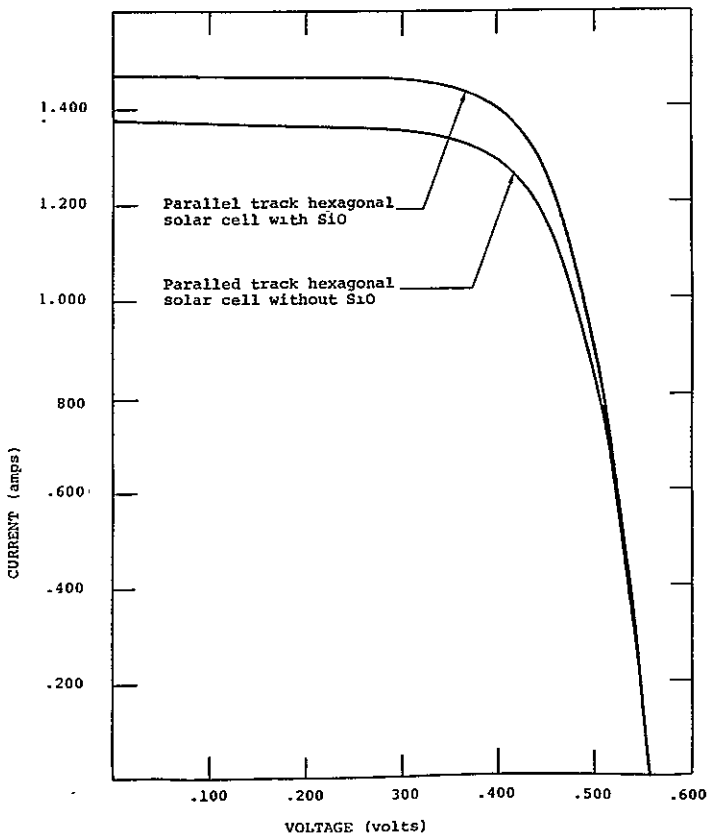



Figure 26 Electrical performance curves of a "Sensagon" Parallel Track hexagonal solar cell, 50.8$cm^2$, with and without SiO anti-reflecrive coating under tungsten light at 28°C and at mw/$cm^2$.

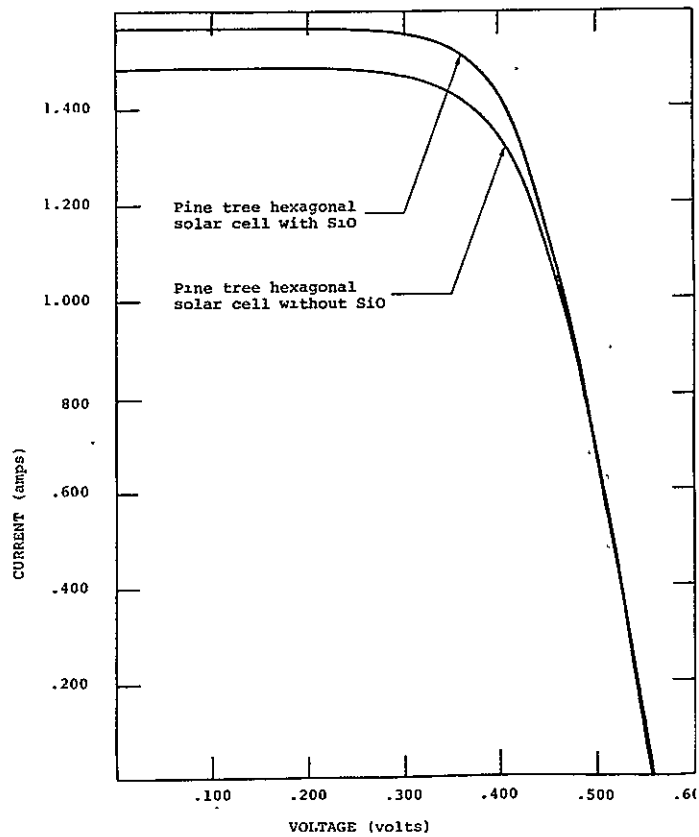



Figure 27 Electrical performance curves of a "Sensagon" Pine tree hexagonal solar cell, 50.8 $cm^2$, with and without SiO anti-reflective coating under tungsten light at 28°C and at 100 mw/$cm^2$.

Table 7. Comparison of four hexagonal solar cell grid patterns. The solar cells have the same surface area, 50.8 $cm^2$, were processed from the same batch of wafers, and were tested under the same conditions, 100 $mw/cm^2$ tungsten light at 28°C.

| PATTERN | SURFACE | PROCESS | A. R. COATING | $I_{SC}$ (amp) | $V_{OC}$ (volts) | $\eta$ (%) (average) | $\eta$ (%) (max) |
|---|---|---|---|---|---|---|---|
| Pine Tree | Texturized | Photoresist | --- | 1.47 | .56 | 10.7 | 10.9 |
| | | | SiO | 1.57 | .56 | 11.3 | 11.6 |
| Parallel Track | Texturized | Silkscreen Resist | --- | 1.38 | .56 | 10.5 | 10.8 |
| | | | SiO | 1.47 | .56 | 11.2 | 11.7 |
| 10 Grid Hex | Texturized | Silkscreen Resist | --- | 1.44 | .56 | 10.1 | 10.8 |
| | | | SiO | 1.50 | .56 | 10.8 | 11.5 |
| 6 Grid Hex | Texturized | Silkscreen Resist | --- | 1.43 | .55 | 10.0 | 10.9 |
| | | | SiO | 1.52 | .56 | 10.7 | 11.4 |

## HEXAGONAL SOLAR CELL MODULE

### A. Hexagonal Solar Cells

Two types of hexagonal solar cells were developed in this program. A hexagonal solar cell with a point to point diameter of 3.500 inches and a side to side diameter of 3.031 inches was used in Phase I. The surface area of the hexagonal solar cell is 7.956 $in.^2$ or 51.33 $cm^2$. The hexagonal solar cell production process sequence for Phase I, which was described in an earlier section, utilized Sensor Technology's commercial process with the addition of a hexagonal solar cell laserscribing step. The "Sensagon" hexagonal solar cell is shown in Figure 20 and 21. The solar cell is adaptable to being cut into halves and arranged in a unique solar cell interconnection pattern. The average electrical performance of a hexagonal solar cell is shown in Figure 28. The average maximum power is .45 watts with a photovoltaic energy conversion efficiency of 8.8% under tungsten light at 28°C and at 100 $mw/cm^2$. Sensor Technology's commercial process is used on 2.15 inch diameter solar cells with a resulting average photovoltaic energy conversion efficiency in excess of 11% at 28°C and at 100 $mw/cm^2$. Results from Phase I of this program show that 3.54 inch diameter silicon

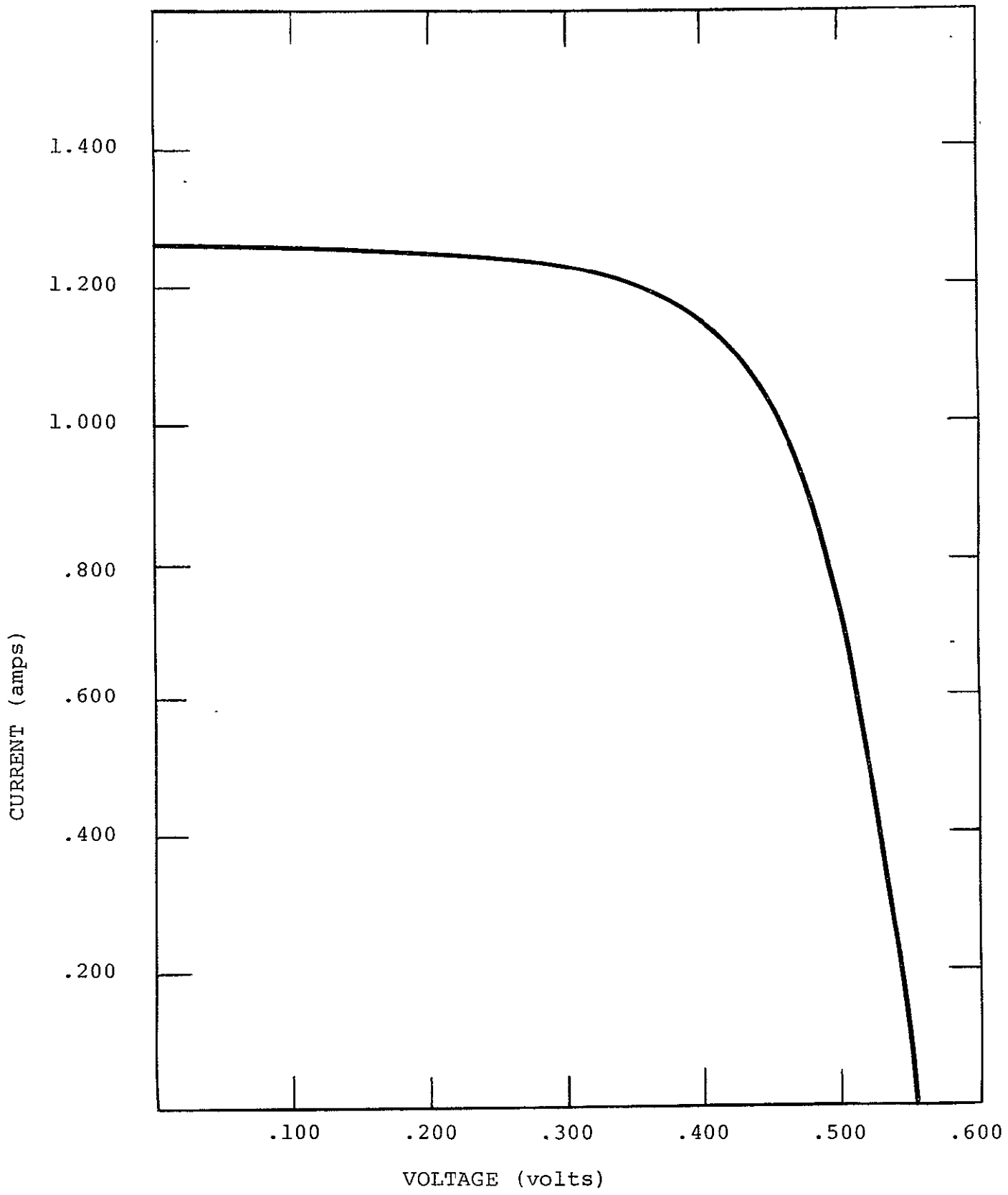



Figure 28. Electrical Performance curve of a "Sensagon" hexagonal solar cell under tungsten light at 28°C and at 100 mw/cm$^2$ developed in Phase I of this program.

solar cells have approximately 2.2% lower efficiencies than the smaller 2.15 inch diameter solar cells. Since the solar cells were made from identical processes and the percent grid line coverage to active area were kept the same, the larger solar cells had lower efficiencies primarily due to series ohmic losses. Improvement in photovoltaic energy conversion efficiency was reserved for Phase II.

A modified hexagonal solar cell with a point to point diameter of 3.500 inches and a side to side diameter of 3.031 inches was used in Phase II. The surface area of the modified hexagonal solar cell is 7.874 $in^2$ or 50.8 $cm^2$. The hexagonal solar cell production process for Phase II which was described in an earlier section, utilized Sensor Technology's commercial process with a surface macro-structure process replacing the surface etching sequence and with the addition of a hexagonal solar cell laser-scribing step. The "Sensagon" hexagonal solar cell is shown in Figures 20, 21, 22 and 23. The electrical performance of the modified hexagonal solar cells is shown in Figure 29. The average minimum power is .590 watts with a photovoltaic energy conversion efficiency of 11.6% under tungsten light at 28°C and at 100 $mw/cm^2$.

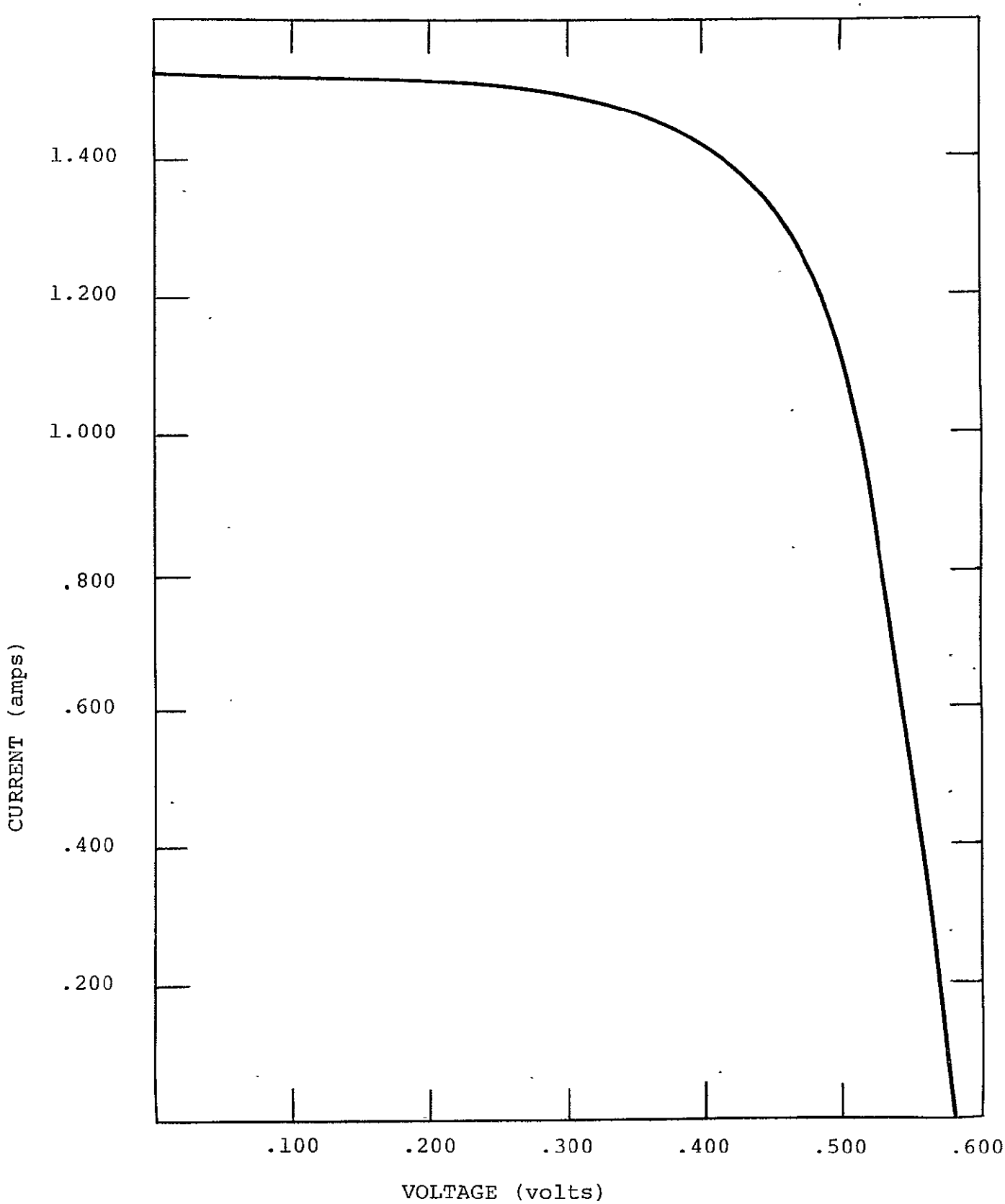



Figure 29. Electrical Performance curve of a "Sensagon" modified hexagonal solar cell under tungsten light at 28°C and at 100 mw/cm$^2$ developed in Phase II of this program.

B. Hexagonal Solar Cell Nesting Efficiency

The hexagonal solar cell nesting efficiency is defined as the ratio of the total hexagonal solar cell surface area to the nesting surface area that contains the solar cells which includes the total solar cell surface area plus the solar cell spacing area. The nesting area contains 28 hexagonal solar cells which are spaced 0.050 inches apart. Refer to Figure 30 top view for the following listed dimensions and calculations:

| | |
|---|---|
| Solar cell nesting length | = 21.67 inches |
| Solar cell nesting width | = 10.77 inches |
| Nesting surface area | = 233.39 $in^2$ |
| Total solar cell surface area | = 222.77 $in^2$ |
| Solar cell spacing area | = 10.62 $in^2$ |
| Solar cell nesting efficiency | = 95.5% |

C. Hexagonal Solar Cell Module Packing Ratio

The hexagonal solar cell module packing ratio (or efficiency) is defined as the ratio of the total hexagonal solar cell surface area to the total solar cell module surface area. The module contains 28 hexagonal solar cells as shown in Figure 30, top view.

| | | |
|---|---|---|
| Module length | = | 22.90 inches |
| Module width | = | 11.179 inches |
| Module surface area | = | 256.00 $in^2$ |
| Total solar cell surface area | = | 222.77 $in^2$ |
| Module packing ratio | = | 87% |

D. Hexagonal Solar Cell Module Fabrication

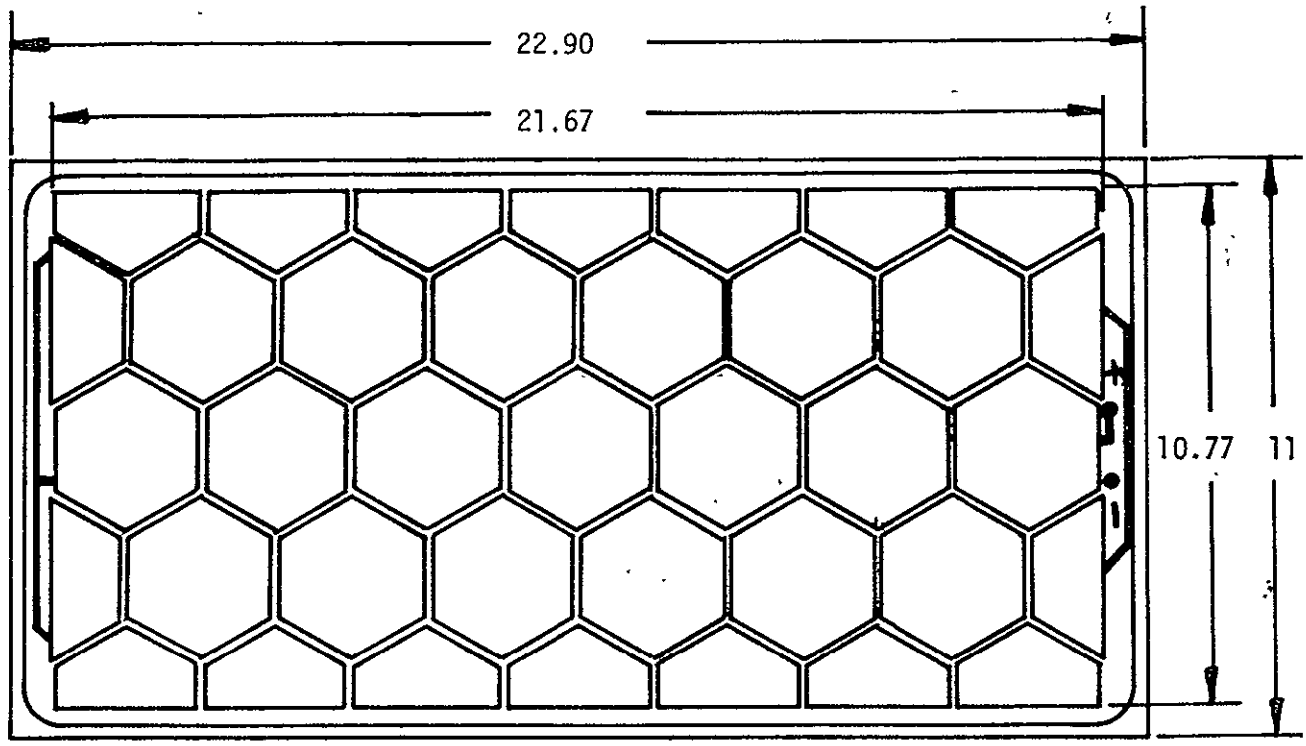
1) Module Substrate

Sensor Technology utilized a JPL approved module substrate that was available in stock for the three modules produced in Phase I. The module substrate is a stamped aluminum pan. Minor additions to the stamped aluminum pan to meet our specific requirements are shown in Figure 30, bottom view, and are listed as follows:

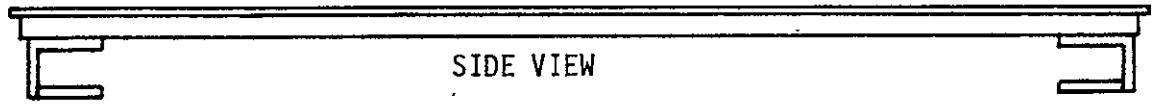
a) Additional aluminum sheet to cover the top of the aluminum pan. It covers the terminal holes and mounting spacer holes that are presently on the pan. The aluminum sheet and pan are spot welded together.

b) Aluminum mounting brackets are spot welded to the aluminum substrate pan.

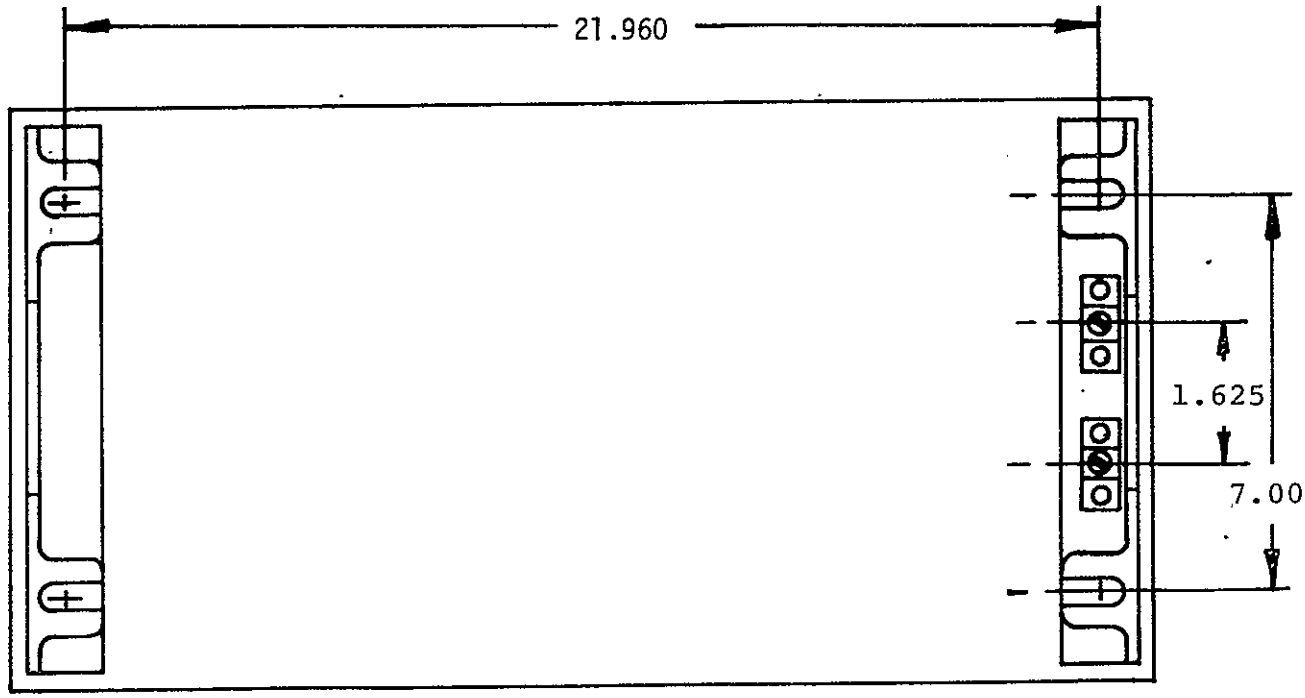
c) Two single wire terminals are utilized.




TOP VIEW



SIDE VIEW




BOTTOM VIEW

Figure 30. Hexagonal solar cell module. Shown are the front view, back view and side view of the module including the aluminum substrate pan, terminals, terminal connections, mounting brackets, and arrangement of the solar cells.

2) Hexagonal Solar Cells and Interconnections

Twenty eight solar cells are utilized in the module. They consist of 19 hexagons and 18 half hexagons. Of the eighteen half hexagons, fourteen are cut side to side and four are cut point to point. Nine series connected half hexagons are paired in parallel with nine other half hexagons which are connected in series with eighteen hexagonal solar cells. The interconnection pattern is schematically shown in Figure 31.

3) Encapsulation Material

The encapsulation material used is General Electric RTV-615.

E. Module Electrical Performance

Two types of hexagonal solar cell modules were developed in this program. Phase I utilized full hexagonal solar cells as described in Part A of this section. Three modules were produced. The electrical performance of the three hexagonal solar cell modules is shown in Figure 32 A, B and C. The average maximum power is 11.77 watts with a photovoltaic energy conversion efficiency of 7.13% under the Jet Propulsion Laboratory Xenon solar simulator at 28°C and at 100 mw/cm$^2$. These Phase I modules

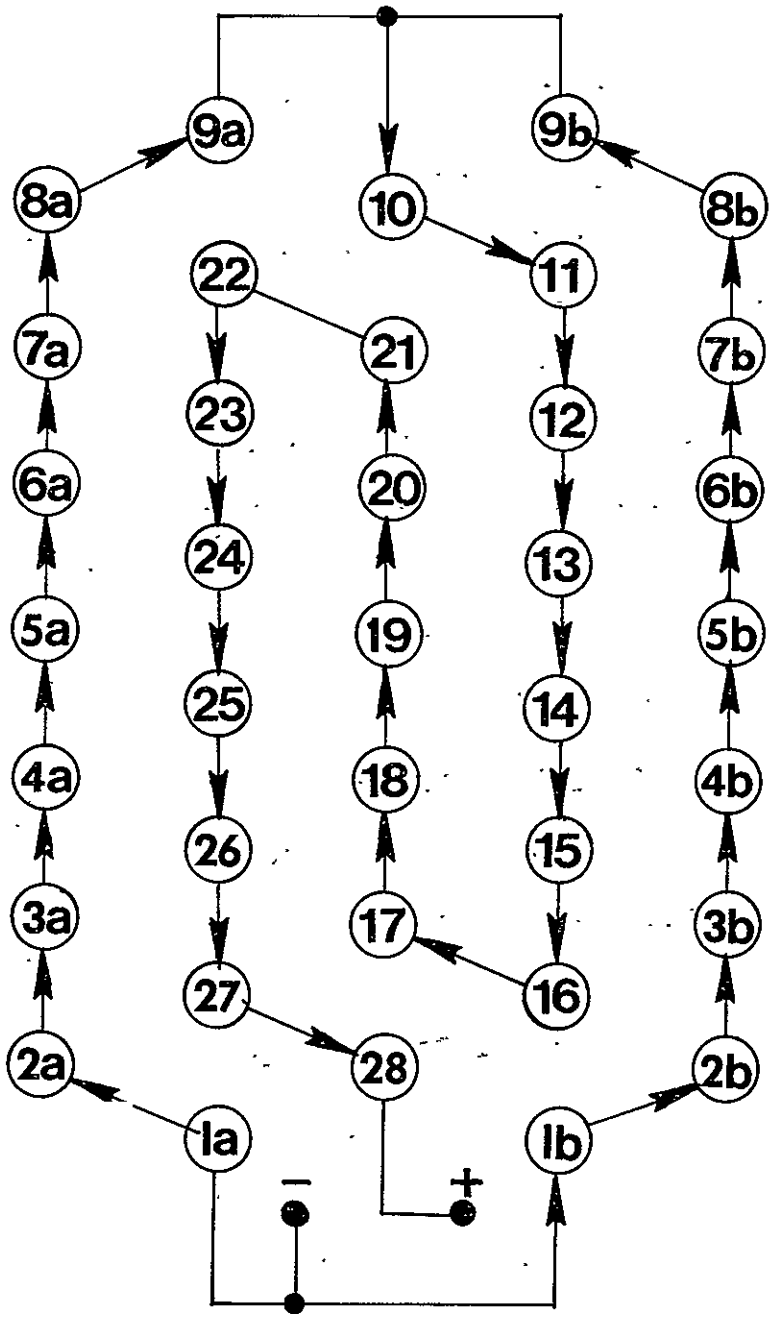



Figure 31. Schematic diagram of the interconnection pattern for the hexagonal solar cell module.

2A.

Y25S - 1117
AMB 22°C

I-V CHARACTERISTIC CURVE
BY Cm DATE 10/5/78
☐ CELL ☐ SUBMODULE ☐ PANEL
SERIAL No. 2 TYPE VH
TEST COMP TEST
TEST TEMP ☒ 28°C ☐ °C
INTENSITY 1.02 MW/CM² ☐ SUNLIGHT
SIMULATOR: ☒ X25L ☐ X25 MK 2
☐ TUNGSTEN OTHER LAPSS
Isc 1.0924 MA Imp 9.558 MA
Voc 1.5933 MV Vmp 10.828 MV
mv MA Pmax MW

FIGURE 32 A.

Pm = 10.40

CURRENT (MILLIAMPS x )

10

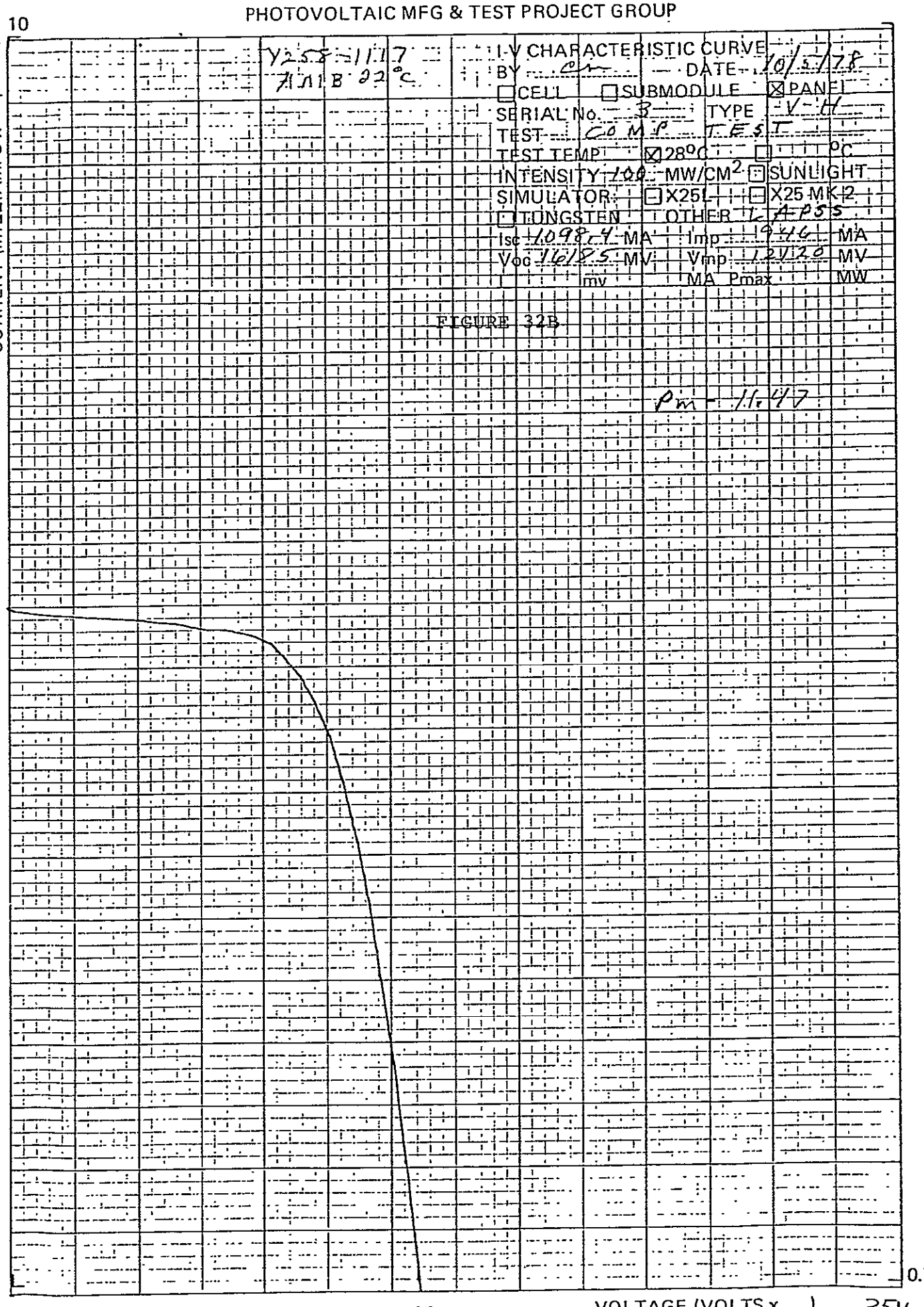
0.7

VOLTAGE (VOLTS x )



35Y

JET PROPULSION LABORATORY
PHOTOVOLTAIC MFG & TEST PROJECT GROUP




HEWLETT-PACKARD 9270 1004

JET PROPULSION LABORATORY
PHOTOVOLTAIC MFG & TEST PROJECT GROUP

2A

10

Y258-1117
AMB. 22°C

I-V CHARACTERISTIC CURVE
BY Cm DATE 10/5/78
☐ CELL ☐ SUBMODULE ☒ PANEL
SERIAL No. 4 TYPE VH
TEST COMP TEST
TEST TEMP ☒ 28°C ☐ °C
INTENSITY 100 MW/CM² ☐ SUNLIGHT
SIMULATOR: ☒ X25L ☐ X25 MK 2
☐ TUNGSTEN OTHER ~AM1.5
Isc 1148.4 MA Imp 1203.4 MA
Voc 1528 MV Vmp 1112.8 MV
mv MA Pmax MW

FIGURE 32C

Pm 13.45

CURRENT (MILLIAMPS x )

0.7

81

VOLTAGE (VOLTS x )

35V

HEWLETT-PACKARD 9270-1006

demonstrate that modules can be made from hexagonal solar cells cut by laserscribe. They also show that module efficiency can be significantly improved by use of hexagonal solar cells replacing round solar cells due to the increased solar cell packing efficiency.

Phase II utilized modified hexagonal solar cells as described in Part A of this section. Three modules were produced. The electrical performance of the three modified hexagonal solar cell modules is shown in Figure 33 A, B, C. The average maximum power is 15.68 watts with a photovoltaic energy conversion efficiency of 9.5% under the Jet Propulsion Laboratory's Xenon solar simulator at 28°C and at 100 mw/cm$^2$. These Phase II modules demonstrate that module efficiencies can be significantly improved by use of hexagonal solar cells processed with surface macrostructures. The Phase II modules are suitable for commercial production. The results of the work performed in Phase II of this program have been utilized for moderately large scale commercial production of hexagonal solar cell modules.

JET PROPULSION LABORATORY
PHOTOVOLTAIC MFG & TEST PROJECT GROUP

10

2A

Y258-1147
AMB 22

I-V CHARACTERISTIC CURVE
BY cm DATE 10/5/78
☐ CELL ☐ SUBMODULE ☒ PANEL
SERIAL No. 7 TYPE V-M
TEST COMP TEST
TEST TEMP ☒ 28°C ☐ °C
INTENSITY 100 MW/CM² ☐ SUNLIGHT
SIMULATOR: ☒ X25L ☐ X25 MK 2
☐ TUNGSTEN OTHER ELAPSS
Isc 1518.2 MA Imp 1309.2 MA
Voc 1618.5 MV Vmp 1179.9 MV
mv MA Pmax MW

FIGURE 33A

Pm - 1545

CURRENT (MILLIAMPS x )

0.7

35V

VOLTAGE (VOLTS x )

JET PROPULSION LABORATORY
PHOTOVOLTAIC MFG & TEST PROJECT GROUP

NEW CAL

Y258 1117
AM3 21°C

I-V CHARACTERISTIC CURVE
BY [illegible] DATE 10/24/78
☐ CELL ☐ SUBMODULE ☒ PANEL
SERIAL No. MB-H6 TYPE VH
TEST SPEC TEST
TEST TEMP ☒ 28°C ☐ °C
INTENSITY 100 MW/CM² ☐ SUNLIGHT
SIMULATOR: ☐ X25L ☐ X25 MK 2
☐ TUNGSTEN OTHER SAP55
Isc 1.956 MA Imp 1.254 MA
Voc 16.185 MV Vmp 12.809 MV
mv MA Pmax MW

FIGURE 33B

Pm 15.69

2A

CURRENT (MILLIAMPS x )

0.7

84

VOLTAGE (VOLTS x )

35V

HEWLETT PACKARD 9270-1006

JET PROPULSION LABORATORY
PHOTOVOLTAIC MFG & TEST PROJECT GROUP

10

2A

Y258-1117
AM8-22°C

I-V CHARACTERISTIC CURVE
BY cm DATE 10/5/78
☐CELL ☐SUBMODULE ☒PANEL
SERIAL No. 6 TYPE V-H
TEST COMP TEST
TEST TEMP. ☒28°C ☐ °C
INTENSITY 100 MW/CM² ☐SUNLIGHT
SIMULATOR ☐X25L ☐X25 MK-2
☐TUNGSTEN OTHER 4 AP5S
Isc 1.5 7.8 MA Imp 1.2 0.2.8 MA
Voc 16233 MV Vmp 11.8 2.3 MV
mv MA Pmax MW

FIGURE 33C

Pm = 14.12

CURRENT (MILLIAMPS x )

85

VOLTAGE (VOLTS x )

0.7

35V

## OPTIMUM SILICON UTILIZATION BY MODIFIED HEXAGONAL SOLAR CELLS FOR LOW-COST, HIGH ENERGY-PER-UNIT-AREA, SOLAR CELL MODULES

### A. Optimum Silicon Utilization

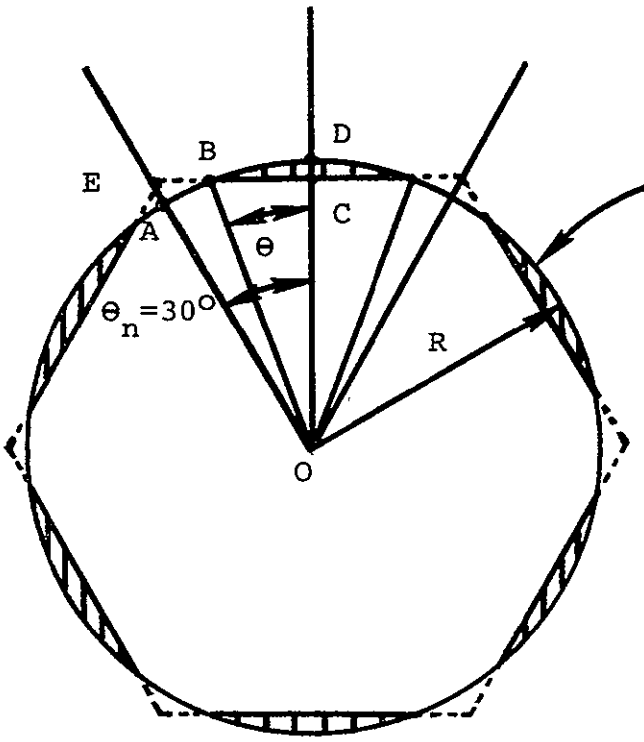
Solar cell module design goals that combine low-costs with high energy-per-unit-area require trade-offs between silicon utilization and solar cell nesting or module packing efficiency. Hexagonal solar cells can be packed together to maximize the solar cell nesting efficiency which in turn reduces the module packing material and surface area for a given designed power output. Unfortunately, hexagonal solar cells are cut from round silicon wafers causing a loss of 17.3% of the costly silicon wafer material. This hexagonal solar cell design, therefore, will maximize the nesting space utilization but will also minimize the silicon wafer material utilization. Conversely for module designs that include round silicon solar cells, maximum silicon wafer material utilization is achieved, but minimum space utilization occurs sacrificing module energy-per-unit-area causing at least 9.3% extra module packing material to be used. A compromise can be made through use of a modified

hexagonal solar cell as shown in Figure 34; it will optimize silicon utilization.

An analysis will be made to determine optimum silicon utilization or the best modified hexagonal solar cell which will lead to minimum module costs under various combinations of material costs.

B. Definition of Modified Hexagonal Solar Cell

A modified hexagonal solar cell is the figure resulting when a hexagon is cut from a round silicon wafer with a smaller diameter than the point to point diameter of the hexagon as shown in Figure 34. The cell consists of six straight edges and six original wafer edges. The degree of scribed area can be defined by a half secant angle $\Theta$ for a given side of a modified hexagon as shown in the figure. If the $\Theta$ value equals 30 degrees ( $\pi/6$ radian) or $\Theta$ equals $\Theta_n$ the cell will be a full hexagonal solar cell. If $\Theta$ is zero then no silicon material is lost and one has a circular solar cell. The $\Theta$ value for all modified hexagonal solar cells will be between 0 and 30 degrees.




R = radius of silicon wafer

θ = half secant angle of a modified hexagon

$\theta_n$ = 30°, half angle of a full hexagon

Figure 34. Definition of a modified hexagon

C. Silicon Wafer Material Utilization Factor

It is convenient to define a silicon wafer material utilization factor, $\eta_s$, as a ratio between the area of the modified hexagonal solar cell to the area of the original round silicon wafer. By using geometrical symmetry and Figure 34, this can be expressed as follows:

$$\eta_s = \frac{\text{Area (OABC)}}{\text{Area (OABD)}} \tag{1}$$

where

$$\text{Area (OABD)} = \tfrac{1}{2}R^2\theta_n,\ \theta_n = \pi/6 \text{ radius}$$
$$\text{Area (OABC)} = \text{Area (OABD)} - \text{Area (BCD)} \tag{2}$$
$$\text{Area (BCD)} = \tfrac{1}{2}R^2(\theta - \sin\theta\cos\theta)$$

Substituting equation (2) into (1), we have

$$\eta_s = \frac{\tfrac{1}{2}R^2\theta_n - \tfrac{1}{2}R^2(\theta - \cos\theta\sin\theta)}{\tfrac{1}{2}R^2\theta_n}$$

$$\boxed{\eta_s = 1 - (\theta - \sin\theta\cos\theta) / \theta_n} \tag{3}$$

where $\theta_n = \pi/6$ radians

For example, if $\theta$ for a full hexagon equals $\theta_n = \pi/6$, then $\eta_s = 0.827$ or the silicon material utilization is 82.7%. For the other extreme case, if $\theta$ is zero as for a round wafer then $\eta_s = 1.000$ or the silicon material utilization is 100%. For $\theta$

between zero and $\pi/6$ one has a modified hexagonal solar cell where the silicon material utilization is represented in Figure 35.

D. Nesting Space Utilization Factor

The other useful term is the nesting space utilization factor, $\eta_{sp}$, which is defined as a ratio between the area of the modified hexagonal solar cell and the cell nesting area or area of a full hexagon. For simplification it was assumed that the module is packed with the straight edges of adjacent cells touching each other so that a full hexagonal solar cell could cover the module nesting area. With this assumption and the definiton of a modified hexagon shown in Figure 34 the space utilization factor can be expressed as follows:

$$\eta_{sp} = \frac{\text{Area (OABC)}}{\text{Area (OEC)}} \tag{4}$$

where

$$\text{Area (OABC)} = \tfrac{1}{2}R^2 \left[\theta_n - (\theta - \sin\theta\cos\theta)\right] \tag{2}$$

$$\text{Area (OEC)} = \tfrac{1}{2}R^2 \cos^2\theta \tan\theta_n \tag{5}$$

Substituting equations (2) and (5) into (4), we have

$$\eta_{sp} = \frac{\theta_n}{\tan \theta_n} \cdot \frac{1}{\cos^2\theta} \left[1 - (\theta - \sin\theta \cos\theta)/\theta_n\right]$$

$$\eta_{sp} = \frac{\theta_n \cdot \eta_s}{\tan \theta_n \cos^2\theta} \qquad (6)$$

where $\theta_n = {}^{\pi}/_{6}$ radius

For example, if $\theta$ is zero as for a round silicon wafer, $\eta_s = 1.000$ and $\eta_{sp} = 0.907$ or the nesting space utilization equals 90.7%. For the other extreme case, if $\theta = \theta_n = {}^{\pi}/_{6}$ as for a full hexagon then $\eta_s = 0.827$ and $\eta_{sp} = 1.000$ or the nesting space utilization equals 100%. For $\theta$ between zero and ${}^{\pi}/_{6}$ one has a modified hexagonal solar cell where the nesting space utilization is represented in Figure 35.

## E. Incremental Cost Analysis

The total cost of a solar cell module can be subdivided into three cost elements. The first one is the cost related to silicon wafer material utilization. The second element depends on nesting space utilization, such as encapsulant material. The

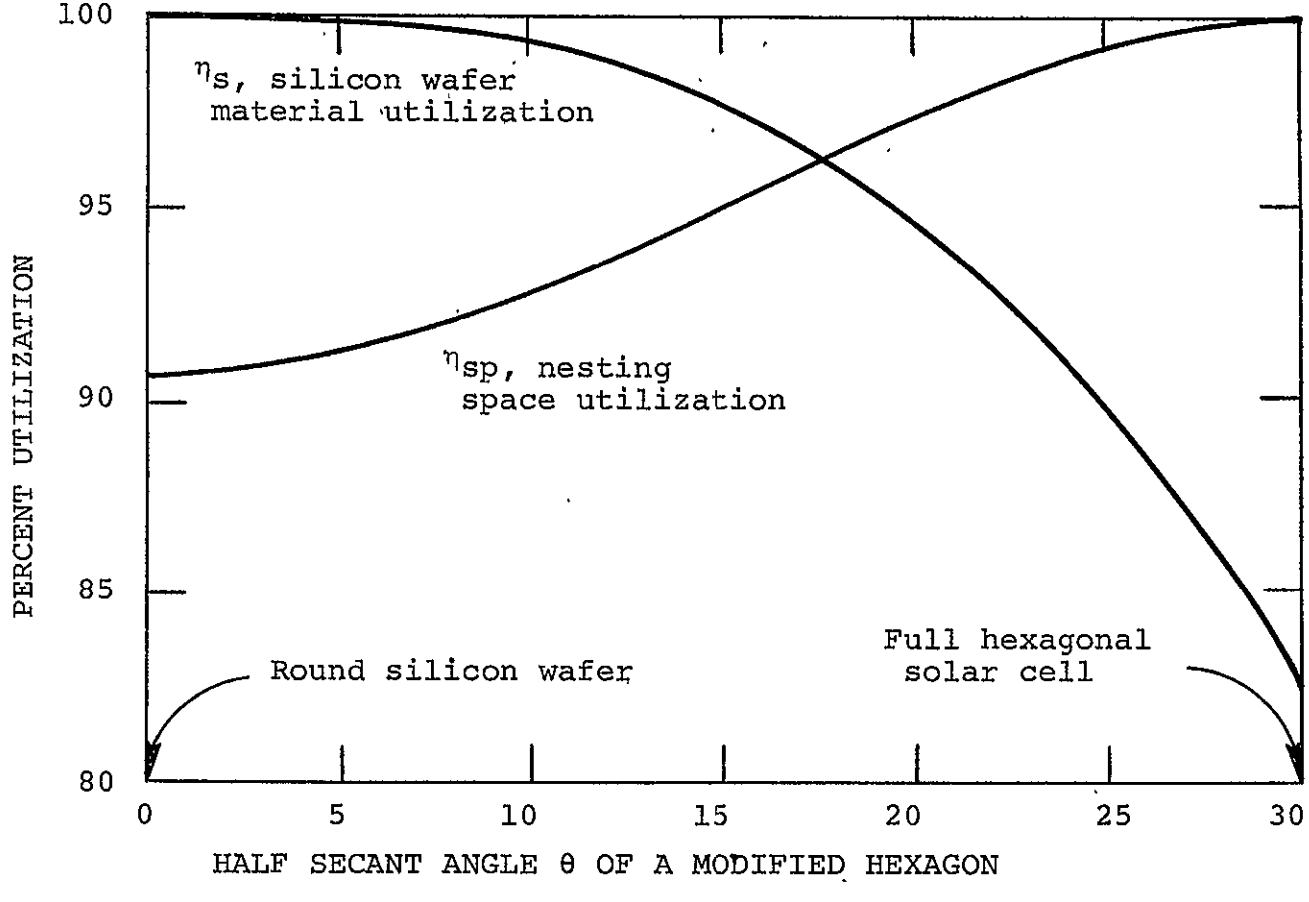



Figure 35. Percent utilization of silicon wafer material and nesting space versus half secant angle θ of a modified hexagon.

third element are the costs which are not affected directly by either silicon utilization or space utilization, such as direct labor on cell processing. All of these cost elements will depend on the cell and module design.

In order to make a generalized cost analysis, simple cost structures are assumed based on the following:

(1) The total solar cell module cost can be subdivided into two cost elements. The first cost element depends only on silicon wafer material utilization. And second, the remaining costs depend only on nesting space utilization. This assumption is good for the case that the labor cost is very small and only the predominant cost factors are silicon cost and encapsulant material cost.

(2) The two cost elements, i.e. silicon utilization costs and space utilization costs, are inversely proportioned to their respective utilization factors. This means that the module costs can be reduced if more silicon material and more nesting space is utilized.

The comparative cost analysis will utilize the circular solar cell module as a reference module and the cost of modified hexagonal solar cell modules will be presented in terms of the fractional cost increment with respect to this reference module.

The first assumption will give the following results for the circular solar cell module:

$$P_O = P_{SO} + P_{SPO} \tag{7}$$

where $P_O$ is the cost of the circular solar cell module (reference module), $P_{SO}$ is the silicon wafer material cost element and $P_{SPO}$ is the remaining cost element including all costs other than for silicon wafer material.

From the second assumption, the total cost of any modified hexagonal solar cell module can be expressed as follows:

$$P(\Theta) = P_{SO} \cdot \frac{\eta_s(0)}{\eta_s(\Theta)} + P_{SPO} \cdot \frac{\eta_{sp}(\Theta)}{\eta_{sp}(\Theta)} \tag{8}$$

where $\eta_s(\Theta)$ is the silicon utilization factor for a modified hexagonal solar cell defined by the half secant angle $\Theta$ and $\eta_{sp}(\Theta)$ is the nesting space utilization factor. Notice that $\eta_s(0) = 1.000$ and $\eta_{sp}(0) = 0.9069$.

The fractional cost increment for a modified hexagonal solar cell module is defined by

$$\Delta P^* = \frac{P(\theta) - P_O}{P_O} \tag{9}$$

Substituting equation (7) and (8) into equation (9) one has

$$P^*(\theta) = \gamma_S \left[ \frac{1}{\eta_s(O)} - 1 \right] - \gamma_{SP} \left[ 1 - \frac{\eta_{sp}(O)}{\eta_{sp}(\theta)} \right]$$

where

$\gamma_S = \frac{P_{SO}}{P_O}$ the fractional cost of silicon material

$\gamma_{SP} = \frac{P_{SP}}{P_O}$ the fractional cost for all elements other than silicon material

From equation (7)

$$\gamma_{SP} = 1 - \gamma_S$$

Substituting this relation into equation (10) one obtains the fractional cost increment for a hexagonal solar cell module:

$$P^*(\theta) = \gamma_S \left[ \frac{1}{\eta_s(\theta)} - 1 \right] - (1 - \gamma_S) \left[ 1 - \frac{\eta_{sp}(O)}{\eta_{sp}(\theta)} \right] \tag{11}$$

where $\gamma_s$ is the fractional cost of silicon material, $\gamma_{sp}(0) = 0.9069$ is the nesting space utilization factor for a circular solar cell module, and $\gamma_s(\theta)$ and $\gamma_{sp}(\theta)$ is respectively the utilization factors for silicon wafer material and nesting space for the modified hexagon given respectively by equations (3) and (6).

The fractional cost increment for a modified hexagonal solar cell module for various fractional silicon costs, $\gamma_s$, are computed using equation 11 and then plotted in Figure 36. The negative values in the figure indicate a cost savings with respect to the circular solar cell module. For example, if $\gamma_s = 0.5$, then the full hexagonal solar cell module will increase the cost by 5.8% but a modified hexagonal solar cell mdoule ($\theta = 17^o$) will reduce the costs by 2%. Figure 36 shows a minimum cost point for each given fractional silicon cost curve, $\gamma_s$.; this represents the optimum solar cell design geometry or the optimum silicon utilization.

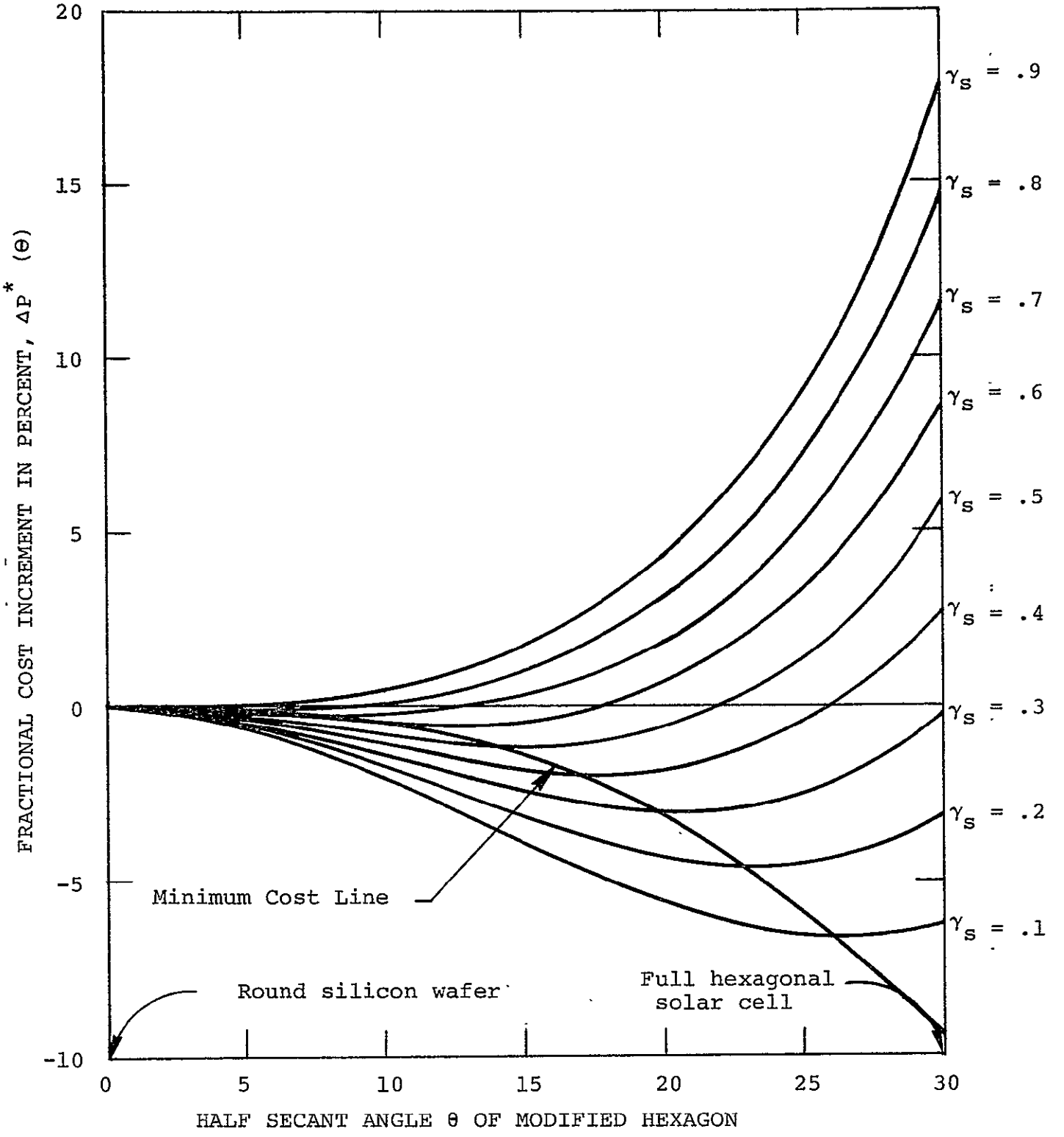



Figure 36. Fractional cost increment of silicon with minimum cost line and cost savings of an optimized modified hexagonal solar cell module.

From Figure 36 the following conclusions can be made:

(1) An optimum modified hexagonal solar cell module exists for a given fractional cost of silicon ( $\gamma_s$ ).

(2) Utilization of an optimum modified hexagonal solar cell module will produce a cost savings compared with a circular solar cell module.

(3) The smaller the fractional cost of silicon ( $\eta_s$) is then the higher the cost savings will become which will be governed primarily by the nesting space utilization factor. Also the smaller s is, the larger the half secant angle, $\theta$, of a modified hexagon is which represents that the optimum solar cell module design geometry approaches a full hexagonal solar cell module.

(4) The maximum possible savings will be 9.3% when the full hexagonal solar cell module is utilized and the fractional cost of silicon is negligibly small.

(5) When the fractional cost of silicon is greater than 0.5 or the silicon wafer cost is 50% of the module cost, the cost savings is less than 1% even though an optimized modified hexagonal solar cell is used. It is, therefore, better to use a circular solar cell module than to use the optimized hexagonal solar cell module to avoid the scribing process.

## SAMICS - A COST ANALYSIS OF THE HEXAGONAL SOLAR CELL MODULE PROCESS SEQUENCE

All Low-Cost Silicon Solar Array (LSSA) projects require a thorough cost analysis to meet certain specific price goals. Since the process cost estimation methods differ from one company to the next, Solar Array Manufacturing Industry Costing Standards (SAMICS) are recommended. SAMICS allows one to make a relative comparison between potential prices attributable to competing processes and to obtain the best possible process price estimate.

All process steps under this program for the development of low-cost, high energy-per-unit-area solar cell modules have had a cost analysis performed using SAMICS. Since only a few of the process steps required detailed development, and since SAMICS requires a complete process sequence to obtain the final cost of the product, a number of Sensor Technology's current proprietary process steps were used to complete the process sequence. The current process steps utilize manual process methods; which can easily be adjusted to accomodate production load variations and product demand. However, these production process steps are not necessarily the best for use in the IPEG [10].

standard industry which requires minimum module cost under the assumption of mass production.

The hypothetical industry used in this SAMICS is a 1978 standard industry defined in Reference 11. The input data preparations and process cost computations are performed according to the methods described in Reference 10, 11 and 13. All the expense items in the process are evaluated with the cost account catalog in Reference 12. If the cost of expense items are not given in Reference 12, the current purchased price was used.

## A. Description of Industry

The structure of the industry is assumed to be the 1978 standard industry defined in Reference 11. This model industry is composed of a sequence of companies, each of which is an independant financial entity. Five sequential companies are considered in the industry. Among these five companies, only the cell and module manufacturing companies are considered in this study. The remaining companies are assumed to perform according to the current price goals defined in Reference 10. The names of these two companies are defined as CELLCO and MODULCO which are manufacturing photovoltaic cells and solar cell modules respectively. It was assumed that both companies are sharing 40 percent of their corresponding market. The

CELLCO will purchase the wafers from WAFERCO with the price of the 1978 LSSA goal. The MODULCO will buy photovoltaic cells from the CELLCO at the current price goal instead of the cell price computed from the CELLCO; in this manner the module price due to the MODULCO alone is determined.

The product of the industry is a packed hexagonal solar cell module, which was developed in this program. A description of the module is presented below:

(1) The module has 19 full hexagonal solar cells and 18 half hexagonal solar cells. The interconnection pattern is equivalent to 28 full hexagonal solar cells connected in series.

(2) Each hexagonal solar cell is cut by laserscribe from a 90 mm round silicon wafer. The silicon wafer material yield is 81 percent.

(3) The solar cell efficiency after encapsulation is assumed to be 12.7 percent. Each module will produce 18.3 watts peak power at 28°C and a 100 $mW/cm^2$ solar insolation.

(4) The solar cell nesting efficiency is 95.5 percent. The module packing efficiency is 87 percent.

(5) The solar cell area is 7.956 square inches. The total solar cell active area is 222.8 square inches. The module area is 256 square inches.

The annual production quantities of the industry and each of the two companies are obtained from the above data and Reference 11. The results are as follows:

INDUSTRY = 1860 $KW_{pk}$/yr = $2.8 \times 10^6$ cells/yr

MODULCO = 732 $KW_{pk}$/yr = $4.0 \times 10^4$ modules/yr

CELLCO = 732 $KW_{pk}$/yr = $1.12 \times 10^6$ cells/yr

The production quantities per unit area depend upon company yield and hardward performance. Since the modules used in this study have different performances, as assumed in Reference 11, the annual production quantities per unit area have to change accordingly. After the SAMICS study, the production yield of CELLCO was 83.6 percent, and the yield of MODULCO was 98.8 percent. From the company yields, the production quantities per unit area for each company can be computed and are shown in Table 8. The LSSA Interim Price Estimation Guidelines (IPEG) goals are presented for the purpose of comparison. The key efficiencies are also presented which clearly illustrate the difference between the current model and the IPEG model.

Table 8. Annual Production Quantities of the 1978 Standard Industry

| DESCRIPTIONS | IPEG MODEL ANNUAL QUANTITY | IPEG MODEL EFFICIENCIES ASSUMED | CURRENT MODEL ANNUAL QUANTITY | CURRENT MODEL EFFICIENC ASSUMED |
|---|---|---|---|---|
| Photovoltaic Module Market ($MW_{pk}$) | 1.83 | | 1.83 | |
| 1000's of $m^2$ of modules | 18.8 | $\eta_{pk} = 0.75$ | 16.76 | $\eta_{pk} = 0.$ |
| MODULCO (40% of market) in $MW_{pk}$ | 0.73 | | 0.73 | |
| 1000's of $m^2$ of modules | 7.50 | | 6.61 | |
| Photovoltaic Cell Market | | | | |
| 1000's of $m^2$ of modules | 14.1 | $\eta_c = 0.13$ | 14.58 | $\eta_c = 0.127$ |
| CELLCO (40% of market) in $MW_{pk}$ | 0.73 | Ym = 1.0 | 0.73 | Ym = 0.988 |
| 1000's of $m^2$ of cells | 5.60 | | 5.83 | |
| Silicon Wafer Market (Solar Cell Grade) | | | | |
| 1000's of $m^2$ of wafers | 17.6 | Yc = 0.80 | 21.53 | Yc = 0.83 |
| | | Ycut = 1.0 | | Ycut = 0. |
| WAFERCO (30% of market) in $MW_{pk}$ | 0.55 | | 0.55 | |
| 1000's of $m^2$ of wafers | 5.30 | | 6.46 | |

$\eta_{pk}$ = packing ratio

$\eta_c$ = cell efficiency

$Y_m$ = yield of MODULCO

$Y_c$ = yield of CELLCO

$Y_{cut}$ = yield of silicon area cutting

B. CELLCO Firm

1. Company Description, Format B

The CELLCO firm is a model company for the 1978 standard industry which produces photovoltaic cells from silicon wafers. The annual production quantity of this company is 1.12 million cells per year, which is equivalent to a peak power of 730 $KW_{pk}$. The detailed definition of CELLCO within the industry is given in the previous section. The products are described in detail in other sections of this report.

The silicon wafers are purchased from WAFERCO with the price defined by IPEG in Reference 10. The price per wafer is $2.878 after converting to a wafer diameter of 90 mm. It is assumed that the company will operate 24 hours per day, seven days a week, and 345 days per year as defined by IPEG Standard Industry. It is further assumed that four shifts will be required so that three shifts will be used during each weekday and one shift is used to fill in on weekends and vacations.

The process steps used by CELLCO consist of current process steps utilized by Sensor Technology and three new process steps developed in this program; they are as follows:

(1) Surface macrostructure process

(2) 400 wafer per hour diffusion process

(3) Hexagonal solar cell laserscribing process

A block diagram showing the process sequence is given in Figure 2. The seventeen process steps are given in Table 9 where the process referents and intermediate product referents are also defined.

Table 9. Definitions of Process Steps, Process Referents and Intermediate Product Referents

| Process No. | Process Referents | Descriptions | Product Referents | Descriptions |
|---|---|---|---|---|
| 1. | SMTEX | Surface Macrostructure Texturizing | TSW | Texturized Silicon Wafer |
| 2. | PDCL | Prediffusion Cleaning | PDSW | Prediffused Silicon Wafer |
| 3. | POCLD | Phosphorus Diffusion | DSW | Diffused Silicon Wafer |
| 4. | FSP | Front Surface Printing | FSPW | Front Surface Printed Wafer |
| 5. | BSE | Back Surface Etching | BSEW | Back Surface Etched Wafer |
| 6. | ALEV | Aluminum Evaporation | ALEVW | Aluminum Evaporated Wafer |
| 7. | ALFI | Aluminum Fire-In | ALFIW | Aluminum Fire-In Wafer |
| 8. | SCLI | Surface Cleaning | SCLW | Surface Cleaned Wafer |
| 9. | FSPP | Front Surface Pattern Printing | FSPPW | Front Surface Pattern Printed Wafer |
| 10. | ENPL | Electroless Nickel Plating | PLC | Plated Cell |
| 11. | SCL2 | Surface Cleaning | SCLC | Surface Cleaned Cell |
| 12. | HEXLS | Hexagon Laser Scribing | HEXC | Hexagonal Cell |
| 13. | SD | Solder Dipping | SDSC | Solder Dipped Solar Cell |
| 14. | FLCL | Flux Cleaning | FLCLC | Flux Cleaned Cell |
| 15. | SGE | Silicon Glass Etching | SGEC | Silcion Glass Etched Cell |
| 16. | ARC | A.R.Coating | ARCC | A.R.Coated Cell |
| 17. | EPT | Electrical Performance Test | PVCELL | Photovoltaic Cell |

2. Process Description, Format A

A process description was written for each step in the form of a Format A form, Reference 13 for use in the cost computations and the results are discussed in the next two sections. Each process step has a production rate and process yield and has quantitative values for all expense items such as equipment, direct labor, floor space, commodities and materials. The data is taken from average values determined from the actual performance data, and none of the processes are assumed to be optimized or automated to meet the current price goal.

Direct labor consists of four quality control inspectors, four maintenance men and one production planner. These direct laborers are assumed to be divided equally into seventeen process steps. For a process step which utilizes more than one machine, the direct labor required is formed by dividing the total number of man years by the number of process steps (seventeen) and by the number of machines required for the process step.

The equipment cost is just the purchased price. However, for equipment that is constructed internally, the cost of this equipment is estimated by using in-house direct labor costs and material costs. Other input data are prepared according

to the information presented in Reference 13.

3. Price Computation

The price of the photovoltaic cell is determined after all data in Format A is complete. It is computed by following the procedures outlined in the process work sheets and company work sheets described in Reference 11. The only additional information needed is the price of expense items which are not covered in the cost accounting catalog in Reference 12. For these items, the currently available purchase prices are used.

The results in 1975 dollars closely compare to the LSSA price goals of $\$5.53/W_{pk}$ as shown by the following:

Inflated price (1978 dollars)

\$6.97 / cell

$\$10.665 / W_{pk}$

$\$1357.9 / m^2$ cell

Deflated price (1975 dollars)

\$5.795 / cell

$\$8.865 / W_{pk}$

$\$1128.8 / m^2$ cell

## 4. Discussion of Results

The cell price results were computed and compared in Table 10 with the LSSA current price goals in terms of cell price per peak watt and cell price per unit area. The total cell price is also shown; it is subdivided into wafer cost and added value by CELLCO. A direct comparison between cell price per unit area was not compared due to the fact that the cell performances are different between those used in the computation and those used in the LSSA IPEG assumptions. Therefore, in comparing results, only the prices per peak watt are compared.

Table 10 shows that the cell price per peak watt by CELLCO is 60% higher than the 1978 IPEG price goal. The added value price by CELLCO is 70% higher than the 1978 IPEG goal. An interesting note can also be made about the purchased wafer price. It is 56% higher than the 1978 IPEG price goal which is due to the discovery that the IPEG price goal does not consider the company overhead and production yield. In the standard SAMICS industry the company overhead was assumed to be 30% and the CELLCO production yield was assumed to be 83.6% - thus, the operation of the independent company becomes 56% over the 1978 IPEG price goal.

Table 10. Summary of SAMICS results for CELLCO in 1978 based on 1975 dollars

| | IPEG 1978 GOAL $/m$^2$ cell | IPEG 1978 GOAL $/$W$_{pk}$ | CELLCO PRICE $/m$^2$cell | CELLCO PRICE $/$W$_{pk}$ | PRICE RATIO BASED ON PEAK WATT |
|---|---|---|---|---|---|
| TOTAL CELL PRICE | 719 | 5.53 | 1128.8 | 8.865 | 1.603 |
| COST OF WAFER | 476 | 3.66 | 1109.10 | 5.695 | * 1.555 |
| (added value) price | 243 | 1.87 | 617.97 | 3.172 | 1.696 |

* Cost for the silicon wafer is high in CELLCO due to 30% company overhead and 83.6% of company yield.

In order to meet the 1978 price goals, the added value by CELLCO has to be reduced by $\$1.30/W_{pk}$. It is very informative to analyze the cost factors of each process step that contribute to the cell price. A summary of the process cost breakdown in 1975 dollars per peak watt is shown in Table 11. The process steps are listed in order from the highest cost to the lowest cost for nine of the most costly steps. The equipment and floor space costs are not given because they are small and the process costs for all other process steps, each having only a small cost contribution are compiled together.

The summary of the cell process cost breakdown in Table 11 shows that the labor cost is the highest factor for each process step. This is due to a manual production type system. The material is the second highest cost factor and the remaining costs are small.

The low pressure metal vapor deposition method is the most expensive process step. This is due to the slow production rate and high material and utility costs. It is recommended that other methods be utilized such as spin-on or spray-on dopants.

TABLE 11. Summary of the process step cost breakdown in 1975 dollars per peak watt.

| | PROCESS REFERENTS | PROCESS NO. | TOTAL | TLAB. | TMAT | UTIL |
|---|---|---|---|---|---|---|
| 1. | ALEV | 6 | 0.6189 | 0.2128 | 0.1436 | 0.2079 |
| 2. | ARC | 16 | 0.5625 | 0.2318 | 0.0975 | 0.1738 |
| 3. | HEXLS | 12 | 0.2800 | 0.1938 | 0.0405 | 0.0114 |
| 4. | BSE | 5 | 0.2648 | 0.038 | 0.2225 | 0 |
| 5. | FLCL | 14 | 0.2347 | 0.0646 | 0.1664 | 0 |
| 6. | FSP | 4 | 0.1755 | 0.1384 | 0.0253 | 0 |
| 7. | FSPP | 9 | 0.1687 | 0.1373 | 0.0253 | 0 |
| 8. | SD | 13 | 0.1398 | 0.0988 | 0.0215 | 0.0215 |
| 9. | PDCL | 2 | 0.1339 | 0.008 | 0.0973 | 0 |
| | ALL OTHERS | 8 | 0.58214 | 0.423 | 0.31002 | 0.0137 |
| | | PROCESSES | | | | |
| | TOTAL | | 3.172 | 1.551 | 1.0556 | 0.4286 |

Contributions by floor space and equipment is 0.263

A similar process procedure to the metal vapor deposition process is the anti-reflective coating process. This process step is second highest in cost. It too can reduce costs through use of spin-on or spray-on A.R.coating techniques.

The next most expensive process step is the hexagonal solar cell laserscribing method. The major cause for higher costs in this process step is a slow production rate and high labor cost. An automatic load and unloading system with a multiple head laser-scribing system can reduce costs significantly.

The material costs are the predominant factors for high process costs in the back surface etching and flux cleaning processes. Both process steps use a manual nitrogen blow drying method which is expensive. This procedure can be eliminated through the utilization of a spin dryer or a clean oven-dryer method.

The solar cell production methods outlined in this report using the improved production recommendations above could meet the 1978 IPEG price goal without any problem.

C. MODULCO Firm

1. Company Description, Format B

The MODULCO firm is a model company for the 1978 standard industry which produces solar cell modules. The company is assumed to share 40% of the solar cell module market. Its annual production is 730 KWpk.

The products of the company are densely packed hexagonal solar cell modules which have 28 equivalent full hexagonal solar cells. Each module produces 18.3 Wpk at 28°C and at 100 $mW/cm^2$ insolation The module area is 256 $in^2$.

The photovoltaic solar cells are purchased from CELLCO with the price set at the 1978 LSSA price goal (instead of the value obtained in CELLCO IPEG). Therefore, the purchased cell price, as given in Reference 10, is $4.38 per cell.

The module assembly methods used by MODULCO are presently used in production by Sensor Technology, Inc., without any modification. The module assembly flow chart is shown in Table 12 with the process Referents defined in Table 13. Two parallel flows are used in the company. The first line is the main module assembly line and the second line is for the substrate pan preparation. The first two pre-

assembly steps are performed outside the company. Therefore, the preassembled pans are assumed to be part of the purchased items and the prices of the preassembled pans are obtained by summing up all the expenses for labor and material outside the company.

It is assumed that the company will operate 24 hours per day, seven days a week, and 345 days per year as defined by IPEG Standard Industry. It is further assumed that four shifts will be required so that three shifts will be used during each weekday and one shift is used to fill in on weekends and vacations.

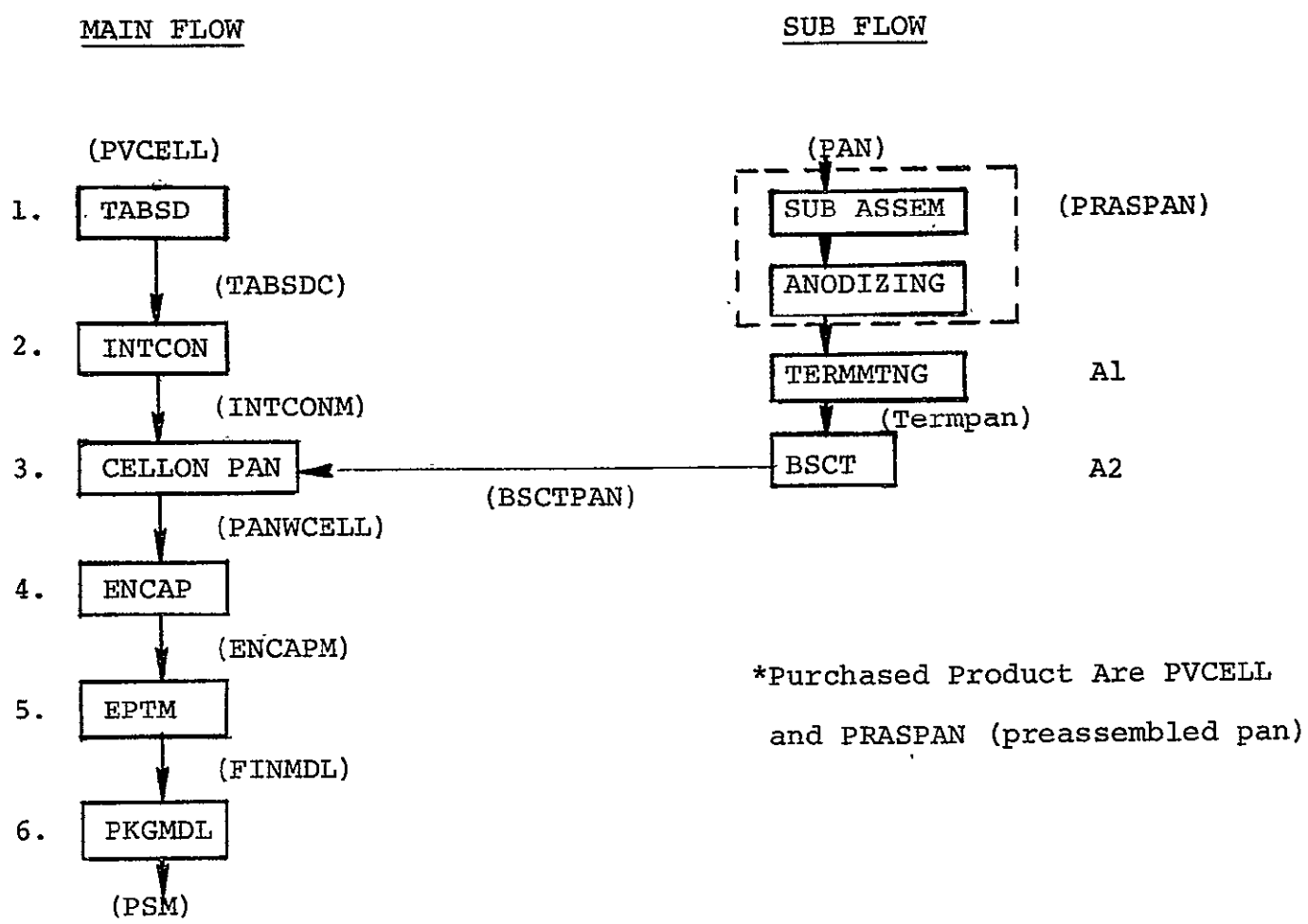



TABLE12. Solar Cell Module Assembly Flow Chart

Table 13. Definitions of referents for module assembly

A. MAIN FLOW

| | | |
|---|---|---|
| 1. TABSD | : | Tab soldering on cells. |
| 2. INTCON | : | Solar cell interconnection. |
| 3. CELLONPAN | : | Place the interconnected cells on the based coated pan. |
| 4. ENCAP | : | Module encapsulation. |
| 5. EPTM | : | Electrical performance of modules. |
| 6. PKGMDL | : | Pack modules for shipping. |

B. SUB-FLOW

| | | |
|---|---|---|
| AO PRASPAN | : | Pan pre-assembly. |
| A1 TERMMTNG | : | Terminal mounting on pans. |
| A2 BSCT | : | Base coating the pan. |

* Sub flow will be joined with main flow at process step 3 (CELLON PAN).

2. Process Description, Format A

An assembly process description was written for each step in the form of a Format A from Reference 13 for use in the cost computations and the results are discussed in the next two sections. Each module assembly process step has a production rate and process yield and has quantitative values for all expense items, such as equipment, direct labor, floor space, commodities and materials. The data is taken from average values determined from the actual performance data. No automation steps or process improvements are assumed.

The cost estimation for direct labor, quality assurance inspectors, maintenance personnel, and for a production planner are considered in the same manner as for the CELLCO company. The direct labor is assumed to be equally divided into each of the process steps.

3. Price Computation

The price of the hexagonal solar cell module is determined after all the data in Format A is complete. It is computed by following the procedures outlined in the process work sheets and company work sheets described in Reference 11. The only additional information needed is the price of the expense items which are not covered in the cost accounting catalog in Reference 12. For these items, the current purchase prices are used.

The results of the computations are presented as follows:

Inflated price in 1978 dollars

$238.82 per module

$13.05 per peak watt

$821.05 per $m^2$ modules

Deflated prices in 1975 dollars

$198.35 per module

$10.85 per peak watt

$682.50 per $m^2$ module

The production yield of the MODULCO was 98.8%

## 4. Discussion of Results

The module price results were computed and compared in Table 14 with the LSSA current price goals in terms of module price per peak watt and module price per unit area. The total module price is also shown; it is subdivided into cell price, encapsulated material and added value by MODULCO. The encapsulation cost used in the overall module process cost estimation was taken out and added to the purchased aluminum substrate pan to obtain a total cost for encapsulation. It should be noted, however, that the encapsulation cost in the IPEG price goals does not include costs for substrate materials.

Based on the information presented in Table 14 for MODULCO in 1978 one obtains the following results:

(1) The computed hexagonal solar cell module price is 53% over the LSSA price goal.

(2) The added value by MODULCO is 35% over the current LSSA price goal which is not significantly high when one considers all the manual assembly process steps.

(3) The encapsulant material, which includes the aluminum substrate, is eight times larger than the LSSA price goal. The encapsulant material not including the aluminum substrate is about twice the LSSA price goal for 1978.

(4) The purchased cell price is 32% higher than the current LSSA price goal. This is due to the IPEG industry structure assumption that the company receives a 30% price increase to cover overhead.

TABLE 14. Summary of SAMICS results for MODULCO in 1978 based on 1975 dollars

| | IPEG GOAL $/m²MDL | IPEG GOAL $/$W_{pk}$ | MODULCO PRICE $/m²MDL | MODULCO PRICE $/$W_{pk}$ | PRICE RATIO BASED ON PEAK WATT |
|---|---|---|---|---|---|
| TOTAL MODULE PRICE | 682.50 | 7.00 | 1202.18 | 10.85 | 1.55 |
| COST OF CELL | 539.00 | 5.53 | 805.52 | 7.27 | **1.315 |
| COST OF ENCAP.MTL. | 21.00 | 0.22 | 209.41 | *1.89 | 8.59 |
| (ADDED VALUE) PRICE | 122.00 | 1.25 | 187.25 | 1.69 | 1.352 |
| $\eta_e$ | 13% | | 12.7% | | |
| $\eta_{pk}$ | 75% | | 87% | | |

* Price of encapsulant consists of a pan and RTV 615 which is $1.09 and $0.802 respectively.

** Cell price is taken from IPEG goal but due to company overhead and production yield factor according to SAMICS gives 31.5% increase in MODULCO price.

If CELLCO and MODULCO were divisions of the same company then this 30% cost for overhead would not be necessary.

(5) The largest contribution to the module price is the cell cost which is 70% of the total module price.

The results above show that the major factors that cause the module price to be high is the cell cost followed by the encapsulant cost and added value by MODULCO.

Automation of the assembly process, therfore, will not significantly lower the module cost; the maximum reduction in price is estimated to be thirteen percent. The encapsulation and substrate material costs are primary factors in the high module cost; a new module design is needed to reduce these costs.

The solar cell costs can be reduced by merging the CELLCO and MODULCO. This will develop a continuous process from silicon wafer to finished module and will save the company overhead and reduce the selling price.

The final module selling price is largely dependent on the industrial structure assumed. By simply varying two parameters, purchased cell price and CELLCO/MODULCO merger/nonmerger, four different module prices can be obtained. The corresponding four cases are defined in Table 15. The module

TABLE 15. Module price per peak watt for various industrial structures in 1975 dollars.

Case (A) Cells are purchased from CELLCO ( Sensor Technology, Inc.)

Case (B) Purchase price of cells is taken from IPEG price.

Case (C) Assumed CELLCO and MODULCO are the same company, Sensor Technology, Inc., so that the process continues from wafer to module.

Case (D) Assumed IPEG CELLCO and MODULCO (Sensor Technology, Inc.) are combined to process continuously from wafer to module.

| | Case (A) | Case (B) | Case (C) | Case (D) |
|---|---|---|---|---|
| Module Price Per Peak Watt | $15.24 *($18.41) | $10.85 *($13.11) | $12.55 *($15.16) | $9.11 *($11.00) |
| Ratio w.r.t. ** Goal price | 2.177 | 1.55 | 1.793 | 1.301 |

* ( ) : Conversion to 1978 dollars

** : IPEG goal of module price is $7.00/$W_{pk}$ in 1975 dollars

prices outlined in the table show a variation from $\$9/W_{pk}$ to $\$15/W_{pk}$ depending on the industrial structure. Case (A) is the worst case. It is the current process method applied to the IPEG standard industry and gives a final module price of $\$15.24/W_{pk}$ in 1975 dollars. Case (B) is the purchase price of the cells taken from the IPEG price. The price is $\$10.85/W_{pk}$ in 1975 dollars. Case (C) is presented by Sensor Technology,Inc., based on SAMICS analysis and includes the final module price for a merger of CELLCO and MODULCO. It gives $\$12.55/W_{pk}$ in 1975 dollars. The best case is Case (D) where the cell price is assumed to be the IPEG goal and CELLCO and MODULCO are assumed to be one company like Sensor Technology. It gives a selling price of $\$9.11/W_{pk}$ in 1975 dollars.

Table 16 summarizes the module cost breakdown in 1975 dollars. The results show, upon excluding material costs for the aluminum substrate pan, the RTV-615 encapsulant, and the solar cell, the labor cost is the predominant cost factor at each step and the costs are uniformly distributed throughout the assembly process. The costs for module fabrication are more for manual assembly. Total automation will reduce the labor cost to a negligibly small value. However, automation by itself will only reduce the

Table 16. Summary of module process cost breakdown in 1975 dollars per peak watt.

| | PROCESS REFERENT | PROCESS NO. | TOTAL | TLAB | TMAT | FLOOR SPACE COST | UTIL |
|---|---|---|---|---|---|---|---|
| 1. | INTCON | 2 | 0.310 | 0.275 | 0.017 | 0.009 | 0 |
| 2. | TABSD | 1 | 0.283 | 0.257 | 0.017 | 0.001 | 0 |
| 4. | ENCAP | 4 | 0.2686 | 0.217 | 0.0 | 0.0506 | 0.0013 |
| 3. | BSCT | A2 | 0.2771 | 0.217 | 0.008 | 0.0506 | 0.0015 |
| 5. | PKGMDL | 6 | 0.2403 | 0.148 | 0.089 | 0.010 | 0 |
| 6. | TERMMNG | A1 | 0.1482 | 0.1222 | 0.0231 | 0.0024 | 0 |
| 7. | CELLONPAN | 3 | 0.1155 | 0.1037 | 0.0003 | 0.0064 | 0.002 |
| 8. | EPTM | 5 | 0.0381 | 0.0329 | -- | 0.00244 | 0.0011 |
| | SUBTOTAL | | 1.681 | 1.372 | 1.1506 | 0.1405 | 0.0061 |
| | PAN | | 1.092 | | | | |
| | RTV-615 | | 0.802 | | TOTAL $10.85 | | |
| | CELL | | 7.273 | | | | |
| | TOTAL | | 10.85 | | | | |

total module cost by approximately thirteen percent. Achieving the LSSA goals will require reduction of labor costs through automation technology and reduction of material costs through development of low-cost silicon solar cell, encapsulation, and substrate materials.

## D. SAMICS Conclusions and Recommendations

All process steps under this program for the development of low-cost, high energy-per-unit-area solar cell modules have had a cost analysis performed. The SAMICS method was applied to the new hexagonal solar cell module using Sensor Technology's current proprietary process steps and three new process procedures described in this report. The results of the computations give the following conclusions:

(1) The final price for the module in 1975 dollars for the year 1978 was approximately $\$15/W_{pk}$, while the LSSA current price goal is $\$7/W_{pk}$.

(2) Silicon wafer material is the single most cost intensive parameter for high module cost. While silicon wafers are purchased by CELLCO (Analysis of wafer cost is beyond the scope of this report), it is a major parameter through which efforts should be directed for cost reduction.

(3) Encapsulant materials cost is a major parameter for high module cost. This is because the current materials for cell encapsulation, i.e. RTV-615 and aluminum substrate material, are expensive. Encapsulant development for cost reduction is needed.

(4) Labor is a major parameter for high module cost. This is because the current labor intensive process methods are best suited for changes in module design, changes and improvements in production procedures and variations in production load. It is not the best method for achieving a minimum module price.

(5) The labor cost in CELLCO is the major factor for a high module price. It is also an important factor for high costs in MODULCO. Changes in process procedures and automation of process steps can easily reduce the module price to meet the current LSSA 1978 price goal. Achieving the 1978 price goal can best be expedited by merging the CELLCO and MODULCO.

## CONCLUSIONS AND RECOMMENDATIONS

This program for the development of low-cost, high energy-per-unit-area solar cell modules has led to a number of conclusions and recommendations.

Modified hexagonally shaped solar cells can be scribed by laser from 90 mm diameter round silicon solar cells. It was demonstrated that a laser can cut through a p-n junction without damaging the junction. The junction current leakage for Sensor Technology's commercial process round solar cells with edge rings are primarily due to edge losses. Junction current leakage for round solar cells can be significantly reduced by cutting around the edge of the solar cell with a laserscribe. The junction current leakage caused by edge effects from the laserscribe is uniform, consistent, and very small. The technique for scribing a silicon wafer, however, is very important. The laserscribing technique includes wafer alignment, laserscribing methodology, and wafer breaking. The present technique requires manual wafer loading and aligning, automated laserscribing, and manual wafer unloading and breaking.

Development of a fully automated laserscribing system is recommended to increase wafer throughput and reduce costs.

Four hundred 90 mm diameter silicon wafers can be diffused in a 38 inch flat zone furnace at 900°C ± 5°C with the use of a buffered mixture to obtain a uniform sheet resistivity within 20%. This diffusion process allows one to process solar cells in large quantities with less than 1% variation in photovoltaic energy conversion efficiency.

Two surface macrostructure processes suitable for large scale production of silicon solar cells have been developed. Silicon wafer surface preparation and etching time, temperature, and concentration was optimized relative to surface macrostructure that trap light efficiently. The process procedures were defined for manual large scale production. The process equipment is capable of processing two hundred 90 mm diameter silicon wafers in five minutes or up to 2400 wafers in one hour. The silicon wafers have black anti-reflective surfaces which are uniformly etched and are batch to batch reproducible. Intermediate

steps in the surface macrostructure process have indicated that higher photovoltaic efficiencies can be obtained. It is recommended that future investigative work be performed on the surface macrostructure process for producing higher photovoltaic energy conversion efficiencies and for reducing costs.

A spin-on anti-reflective coating study demonstrated that low-cost methods can be utilized effectively to increase the photovoltaic energy conversion efficiency of solar cells. The spin-on A.R. coated solar cells showed significant electrical performance improvement over solar cells without A.R.coatings, but it was also shown that the spin-on A.R.coated solar cells were not as efficient as vacuum deposited SiO and silicon nitride solar cells. It is recommended that a rigorous study be made on low-cost anti-reflective coating methods, such as, spin-on, spray-on (see Reference 14), and low pressure vapor deposition.

Solar cell electrical performance curves were analyzed for four different grid pattern designs which led to the following results: Solar cells processed under the same conditions that have the same grid line coverage are relatively insensitive to the grid pattern used. No significant electrical

performance advantage was found for using a photolithographic process over a silk screen printing process for solar cells. A single contact point and dual redundant points produce very nearly the same solar cell electrical performance.

The six hexagonal solar cell modules fabricated in this program demonstrated that module efficiency can be significantly improved by the utilization of hexagonal or modified hexagonal solar cells replacing round solar cells due to increased solar cell packing ratio and increased solar cell photovoltaic energy conversion efficiency.

A detailed theoretical analysis on the optimum silicon utilization by modified hexagonal solar cells for low-cost, high energy-per-unit-area solar cell modules arrived at the following conclusions: An optimum modified hexagonal solar cell module exists for a given fractional cost of silicon. The utilization of an optimum modified hexagonal solar cell module will produce a cost savings compared with a circular solar cell module. The smaller the fractional cost of silicon is then the higher the cost savings becomes which is governed primarily by the nesting space utilization factor. The maximum possible savings will be 9.3% when the full hexagonal solar cell module is utilized and the

fractional cost of silicon is negligibly small.

The SAMICS method was applied to the hexagonal solar cell module using Sensor Technology's current proprietary process steps and three new process procedures: surface macrostructure, diffusion, and laserscribe. The conclusions show that the 1978 LSSA cost goal of $7/Wpk for solar cell modules is achievable. It is recommended, however, that significant development efforts be directed toward low-cost silicon wafer materials, low-cost encapsulant materials and process automation.

## LIST OF REFERENCES

The following references were used as background material in preparation for the work performed during this program:


1. Laserscribe 603-2 Operation Manual 1976 Quantronix Corporation, Santa Clara, California.

2. R.A.Kaplan, "Breaking Characteristics of Laserscribed Wafers." Circuits Manufacturing, September, 1973, p.58.

3. J.W.Thornhill, Automated Fabrication of Back Surface field Silicon Solar Cells, Spectralab, Inc., NASA/Lewis Contract NAS3-20029, Final Report (August 1977), NASA-CR-135202.

4. D.B.Lee, Journal of Applied Physics, Vol. 40 No. 11 by 4569, 1969.

5. A.E.Stoller, RCA Review, Vol. 31, No. 2. pg. 271, 1970.

6. Spectralab report on "High Efficiency Solar Panel", AF APL-77-36.

7. J.B.Price, in "Semiconductor Silicon 1973," Howard R. Huff and Ronald R. Burgess, Editors, pp 339-353, The Electrochemical Society Softbound Symposium Series, Princeton, N.J. (1973).

8. J.W.Faust, Jr., The Surface Chemistry of Metals and Semiconductors, pg. 151, Wiley, New York, 1970.

9. R. M. Finne and D. L. Klein, A Water-Amine-Complexing Agent System for Etching Silicon, J. Electrochem Soc., Solid State Science, Vol. 114, No. 9, Sept. 1967.

10. JPL 5101-33 "Interim Price Estimation Guidelines".

11. JPL 5101-15 "SAMICS Workbooks".

12. JPL-954800-77/21 "Cost Account Catalog".

13. JPL 5101-44 "SAMICS Input Data Preparations".

14. G.T.Jones, S.S.Rhee, K.L.Allison, DOE/JPL-954865-78/2; Phase 2 Array Automated Assembly Task, Quarterly Report No. 2, JPL Contract 954865; LSSA Project, Array Automated Assembly Task, March 1978, by Sensor Technology, Inc.