THE ESTABLISHMENT OF A PRODUCTION-READY MANUFACTURING PROCESS UTILIZING THIN SILICON SUBSTRATES FOR SOLAR CELLS

QUARTERLY TECHNICAL REPORT NO. 1

MOTOROLA REPORT NO. 2364/1

DRD NO. SE-4

1 FEBRUARY 1979 - 31 MARCH 1979

JPL CONTRACT NO. 955328

PREPARED BY

R. A. PRYOR

MOTOROLA INC. SEMICONDUCTOR GROUP
5005 EAST MCDOWELL ROAD
PHOENIX, ARIZONA 85005

THE JPL LOW-COST SOLAR ARRAY PROJECT IS SPONSORED BY THE U. S. DEPARTMENT OF ENERGY AND FORMS PART OF THE SOLAR PHOTOVOLTAIC CONVERSION PROGRAM TO INITIATE A MAJOR EFFORT TOWARD THE LOW-COST SOLAR ARRAYS. THIS WORK WAS PERFORMED FOR THE JET PROPULSION LABORATORY, CALIFORNIA INSTITUTE OF TECHNOLOGY BY AGREEMENT BETWEEN NASA AND DOE.

PROJECT NO. 2364

DOE/JPL-955328-79/1
DISTRIBUTION CATEGORY UC-63

DRL NO. 99
DRD NO. SE-4

THE ESTABLISHMENT OF A PRODUCTION-READY MANUFACTURING PROCESS UTILIZING THIN SILICON SUBSTRATES FOR SOLAR CELLS

QUARTERLY TECHNICAL REPORT NO. 1

MOTOROLA REPORT NO. 2364/1

DRD NO. SE-4

1 FEBRUARY 1979 - 31 MARCH 1979

JPL CONTRACT NO. 955328

PREPARED BY

R. A. PRYOR

MOTOROLA INC. SEMICONDUCTOR GROUP
5005 EAST MCDOWELL ROAD
PHOENIX, ARIZONA 85005

THE JPL LOW-COST SOLAR ARRAY PROJECT IS SPONSORED BY THE U. S. DEPARTMENT OF ENERGY AND FORMS PART OF THE SOLAR PHOTOVOLTAIC CONVERSION PROGRAM TO INITIATE A MAJOR EFFORT TOWARD THE LOW-COST SOLAR ARRAYS. THIS WORK WAS PERFORMED FOR THE JET PROPULSION LABORATORY, CALIFORNIA INSTITUTE OF TECHNOLOGY BY AGREEMENT BETWEEN NASA AND DOE.

PROJECT NO. 2364

TABLE OF CONTENTS

SECTION	TITLE	PAGE
1.0	Summary	1
2.0	Technical Progress	1
2.1	Objectives	1
2.2	Thin Substrate Procurement	3
2.3	Baseline Processing Sequences	9
3.0	Conclusions and Recommendations	9
4.0	Plans	9
5.0	New Technology	11
6.0	Program and Documentation Milestones	11

PROGRESS REPORT FOR FEBRUARY AND MARCH 1979

1.0 SUMMARY

During the months of February and March, work toward the goals of this contract has been started as scheduled in the Program Plan. The first shipments of thin substrates have been received and wafer processing has been initiated.

Some of the very thin (4 mil) substrates have been received ahead of schedule; these show the practicality of $2/watt modules at a polysilicon cost of about $25/kg, and the possibility of 50¢/watt modules at a polysilicon cost of $7.50/kg.

2.0 TECHNICAL PROGRESS

2.1 OBJECTIVES

This contract is for the investigation, development, and characterization of methods for establishing a production-ready manufacturing process which utilizes thin silicon substrates for solar cells. These thin substrates will be 3 inch diameter, p-type Czochralski wafers of approximately 1 Ω cm resistivity. These wafers are being purchased from the Motorola Semiconductor Group Materials Operation and will be prepared by sawing directly to thicknesses of 8 mils and 5 mils. To ensure removal of residual saw damage, most substrates will be chemically etched to final thicknesses of 7 mils and 4 mils. Some substrates will be received as-sawed in order to evaluate the optimum thickness of saw damage removal.

The thin substrates will be used to fabricate solar cells by standard processing techniques. In all cases of thin cell processing, standard substrates which are nominally 15 mils thick will be processed simultaneously to serve as controls for performance and yield comparisons. Moreover, the processing itself

will be closely monitored, and when substrate thinness causes particular problems, processing will be modified to accommodate the thin substrates. One goal will be to modify processing as required to develop a high-yield pilot line process which is production worthy.

Based on yield and performance information developed for 15, 7, and 4 mil wafers, extrapolations will be made to estimate the cost effectiveness of substrates thinner than 4 mils (or to estimate the optimum substrate thickness if it should happen that 4 mils is already too thin).

Another goal of the contract is to demonstrate, by process verification tests and analyses, that at an annual production volume of 15 megawatts and a 5-year factory life, the following add-on capital and labor costs per peak watt (from crystal growing through sawing) can be achieved:

Wafer Thickness Before Saw Damage Removal (mils)	Capital Cost/Watt ($)	Labor Cost/Watt ($)
15 (12 mil kerf)	0.35	0.135
8 (7.5 mil kerf)	0.20	0.080
5 (7.5 mil kerf)	0.16	0.065

The costs in this table are obtained by considering the structure of a factory producing 15 megawatts annually with sliced Czochralski substrates. The most capital intensive operations in this factory are associated with the ingot growth and wafer preparation processes. Approximately 2/3 of total capital equipment costs are in those areas. By utilizing thinner wafers, more wafers may be realized from a given volume of silicon, resulting in more silicon area for solar cells being obtained from each piece of equipment and each operator in the crystal growth and sawing areas. This effectively reduces the capital and labor costs per watt by this increased silicon area realization. Of course, it must be determined that high process yields can be maintained regardless of slice thinness.

The possibility of using wafers sawed at 5 mils with a 7.5 mil kerf makes the attainment of 1 m^2 of solar cells per kg of starting silicon a realistic short term proposition.

A square meter of silicon t mils thick weighs:

$$100 \text{ cm} \times 100 \text{ cm} \times t \text{ mils} \times \frac{10^{-3} \text{ in}}{\text{mil}} \times \frac{2.54 \text{ cm}}{\text{in}} \times \frac{2.33 \text{ gm}}{\text{cm}^3} = 59\ t \text{ gm}$$

Allowing for kerf loss, the thinner (5 mil) wafers utilize 12.5 mils of crystal; this produces 32 wafers per cm of crystal. Hence, a square meter of silicon utilizes 59 x 12.5 = 737.5 gm of silicon. This allows a budget of 262.5 gm of silicon for losses including crystal growing, slicing, and solar cell processing. Such a loss - 35% - is well within the bounds of practicality.

At current prices for polycrystalline silicon, about $60/kg, the silicon cost per square meter of silicon would be $60. Assuming 15% encapsulated efficiency, which is now a generally accepted goal for single crystal silicon solar cell modules, one square meter of silicon would produce 150 watts. This results in a cost of $60/kg / 150 watts/kg = 40¢/watt. At a projected intermediate polycrystalline silicon price of $25/kg, the silicon content of a solar module will be less than 17¢/watt, which is well within the budget for a $2/watt module. At a projected long term polycrystalline silicon price of $7.50/kg, the silicon content of a solar module will be 5¢/watt. This figure is not out of line for a 50¢/watt budget of about 15¢/watt each for the silicon substrate, wafer processing, and encapsulation.

2.2 THIN SUBSTRATE PROCUREMENT

Initial orders have been placed with the Motorola Semiconductor Group Materials Operation for thin silicon substrate samples. Sample substrates will be sawed to nominally 8 mil and 5 mil thicknesses using a wire saw. After sawing,

most samples will be chemically etched to remove approximately one-half mil from each side to eliminate residual sawing damage. Final thickness values will, therefore, be nominally 7 mils and 4 mils. A number of the 8 mil as-sawed substrates will be delivered before etching and used in experiments to determine the optimum thickness of saw damage removal.

In addition to the thin substrates, wafers with the standard thickness of 15 mils will be used as processing controls. These wafers will be processed with the thin substrates to monitor the effects of thickness reductions.

It was originally anticipated that the 7-8 mil wafers would be received first, with some delay before receiving the 4-5 mil wafers. Moreover, it would be convenient to learn to process 7-8 mil wafers before working with thinner substrates. However, initial deliveries of both 8 mil as-cut wafers and 4 mil sawed and etched wafers have been received, allowing earlier processing of the thinner wafers. Sample measurements from these wafer deliveries are given in Tables 1, 2, and 3.

Tables 1 and 2 show thickness measurements made at five positions on each wafer tested. The five positions include a center position and four edge positions as shown in Figure 1. The average for all thickness measurements on the nominally 8 mil as-cut wafers is 8.24 mils (standard deviation is 0.18 mils). The average for the nominally 4 mil sawed and etched wafers is 4.27 mils (standard deviation is 0.10 mils).

Table 3 shows resistivity measurements made at the center of each wafer tested. The average thicknesses stated above were assumed for calculating wafer resistivity. Wafers of either thickness have resistivities averaging near 1.2 Ωcm.

Additional deliveries of thin wafers as well as standard thickness control wafers will be forthcoming. Data for an analysis of yields and the cost effectiveness of preparing thin substrates are being collected. These data will be discussed in future reports.

TABLE 1

Test wafer thickness measurements for nominal 8 mil, as-cut wafers.

Test Wafer Number	Thickness In Mils				
	Center Position	Edge Positions			
1	8.10	8.00	7.93	8.18	8.08
2	8.21	8.12	8.33	8.21	8.39
3	8.14	8.05	8.29	8.19	8.17
4	8.25	8.13	8.38	8.58	8.13
5	8.50	8.63	8.54	8.53	8.68
6	8.03	8.12	8.00	8.00	7.99
7	8.19	8.08	8.02	8.23	8.29
8	8.22	8.12	8.15	8.19	8.15
9	8.42	8.42	8.40	8.28	8.27
10	8.39	8.52	8.41	8.25	8.24

	Center Readings	All Readings
Mean	8.25	8.24
Standard Deviation	0.15	0.18
% Standard Deviation	1.8%	2.2%

TABLE 2

Test wafer thickness measurements for nominal 4 mil, sawed and etched wafers.

Test Wafer Number	Thickness In Mils				
	Center Position	Edge Positions			
1	4.37	4.30	4.41	4.12	4.41
2	4.33	4.20	4.25	4.21	4.32
3	4.32	4.35	4.10	4.32	4.05
4	4.28	4.15	4.41	4.08	4.18
5	4.39	4.28	4.39	4.28	4.37
6	4.35	4.38	4.36	4.30	4.30
7	4.38	4.28	4.27	4.40	4.23
8	4.34	4.20	4.30	4.33	4.21
9	4.32	4.24	4.38	4.18	4.26
10	4.41	4.30	4.44	4.48	4.49
11	4.25	4.10	4.26	4.19	4.11
12	4.20	4.12	4.28	4.11	4.10
13	4.31	4.51	4.12	4.17	4.19
14	4.37	4.22	4.18	4.39	4.12
15	4.28	4.31	4.22	4.11	4.19
16	4.32	4.33	4.23	4.21	4.27
17	4.37	4.47	4.24	4.28	4.27
18	4.41	4.19	4.47	4.05	4.49
19	4.36	4.25	4.38	4.20	4.29
20	4.22	4.09	4.14	4.23	4.28
21	4.37	4.35	4.27	4.32	4.21
22	4.31	4.12	4.22	4.26	4.18
23	4.38	4.40	4.19	4.24	4.23
24	4.35	4.21	4.42	4.18	4.26
25	4.36	4.31	4.43	4.12	4.31

	Center Readings	All Readings
Mean	4.33	4.27
Standard Deviation	0.05	0.10
% Standard Deviation	1.2%	2.3%

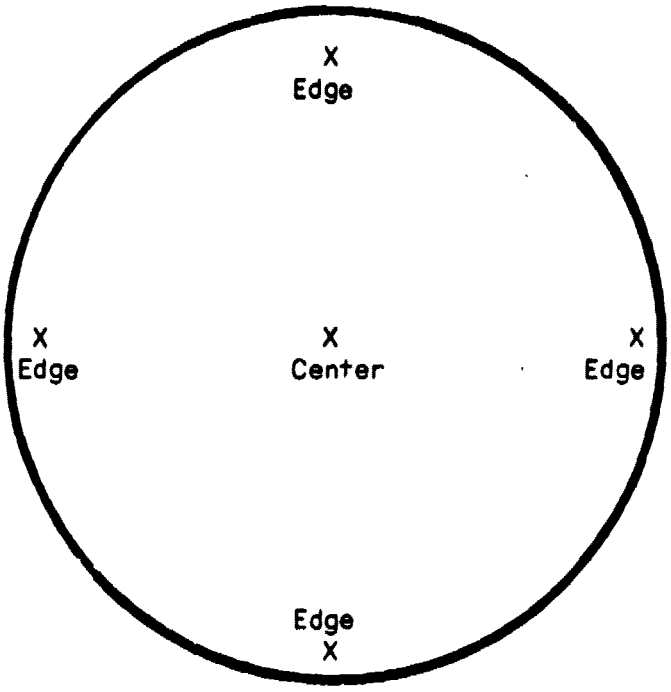

Figure 1: Diagram showing positions where thickness measurements were made on sample wafers.

TABLE 3

Test wafer resistivity, measured at wafer center with four point probe.

Test Wafer Number	Resistivity in Ω cm	
	8 mil Wafers	4 mil Wafers
1	1.29	1.30
2	1.31	1.35
3	1.31	1.18
4	1.23	1.13
5	1.38	1.21
6	1.25	1.21
7	1.34	1.15
8	1.20	1.14
9	1.24	1.16
10	1.19	1.17
11	1.22	1.16
12	1.24	1.24
13	1.23	1.30
14	1.21	1.23
15	1.06	1.25
16	1.10	1.15
17	1.07	1.16
18	1.22	1.31
19	1.23	1.32
20	1.15	1.32
21	1.06	1.23
22	1.12	1.20
23	1.12	1.17
24	1.08	1.21
25	1.27	1.17
Mean	1.20	1.22
Standard Deviation	0.09	0.07
% Standard Deviation	7.5%	5.4%

2.3 BASELINE PROCESSING SEQUENCES

The primary emphasis of this contract is on near term cost reduction achieved by implementing the use of thinner silicon substrates. Since these substrates are to be sawed directly to near the desired thinness, more wafers will be obtained from a given ingot of Czochralski silicon, thus reducing the cost per wafer. This can lead to an overall cost reduction if these thin wafers can be processed as effectively as standard thickness wafers.

Since near term cost reductions are desired, near term processing sequences centered on diffusion techniques will be considered first. Process sequences employing phosphorous diffusions with phosphine (PH_3) sources will be used for n-type junction layer formation. An example of a simple baseline process is given in Table 4. This sequence is short and does not incorporate a back surface field (BSF) which may be very desirable if the maximum performance is to be obtained with the thin substrates.

After comparing cell performance versus thinness with the non-BSF processing sequence, boron doped (BCl_3) BSF layers and perhaps aluminum BSF layers will be introduced. The attendant performance gains will be evaluated with respect to the additional processing complexity.

3.0 CONCLUSIONS AND RECOMMENDATIONS

There are no appropriate conclusions or recommendations at this time.

4.0 PLANS

For the coming quarter the program plan is expected to proceed on schedule for the most part and ahead of schedule in some areas. Early delivery of some of the 4 mil wafers has allowed the option of processing 4 mil substrates at an

TABLE 4

A diffused junction, baseline process which does not incorporate a back surface field (BSF).

Start with sawed and etched wafer

1. Texture etch - both sides
2. PH_3 diffuse, 900°C - both sides
3. Etch back surface, mesa etch front
4. AR coat with LPCVD silicon nitride (simultaneous back and front)
5. Strip back surface, pattern front with ohmic contact grid (simultaneous back and front)
6. Metallize by plating (simultaneous back and front)

earlier than scheduled date. The initiation of 4 mil processing will depend on initial success of 8 mil substrates in process.

During the next quarter, it is expected that all substrate material deliveries will be completed and that solar cell processing will be well under way.

5.0 NEW TECHNOLOGY

No reportable items of new technology have been identified, as yet.

6.0 PROGRAM AND DOCUMENTATION MILESTONES

Activities associated with the total program are shown in the Program and Documentation Milestone Charts Figures 1 and 2 contained in Appendix 1.

APPENDIX I

Program Milestone Chart

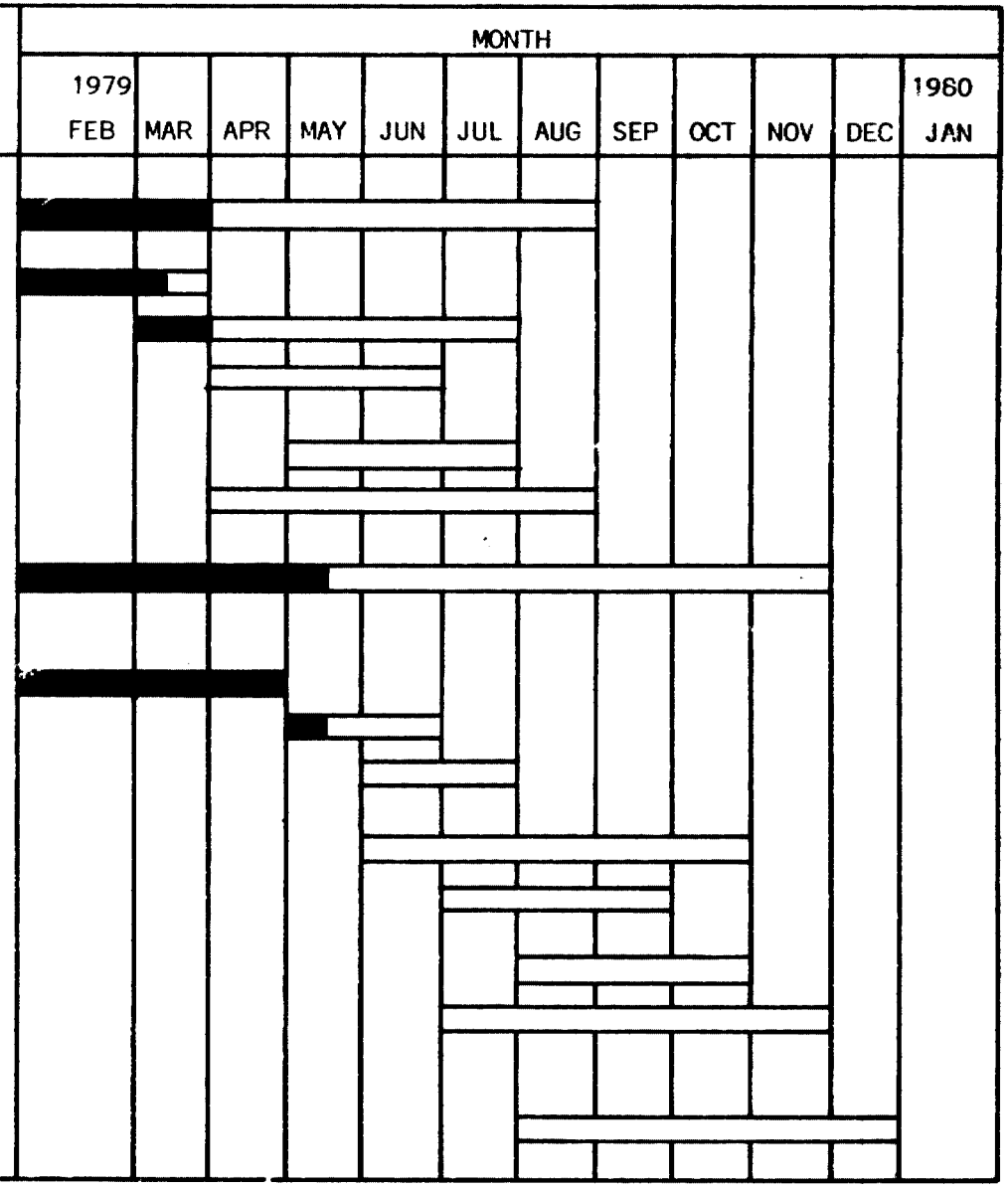

Figure 1

Program Milestone Chart (Continued)

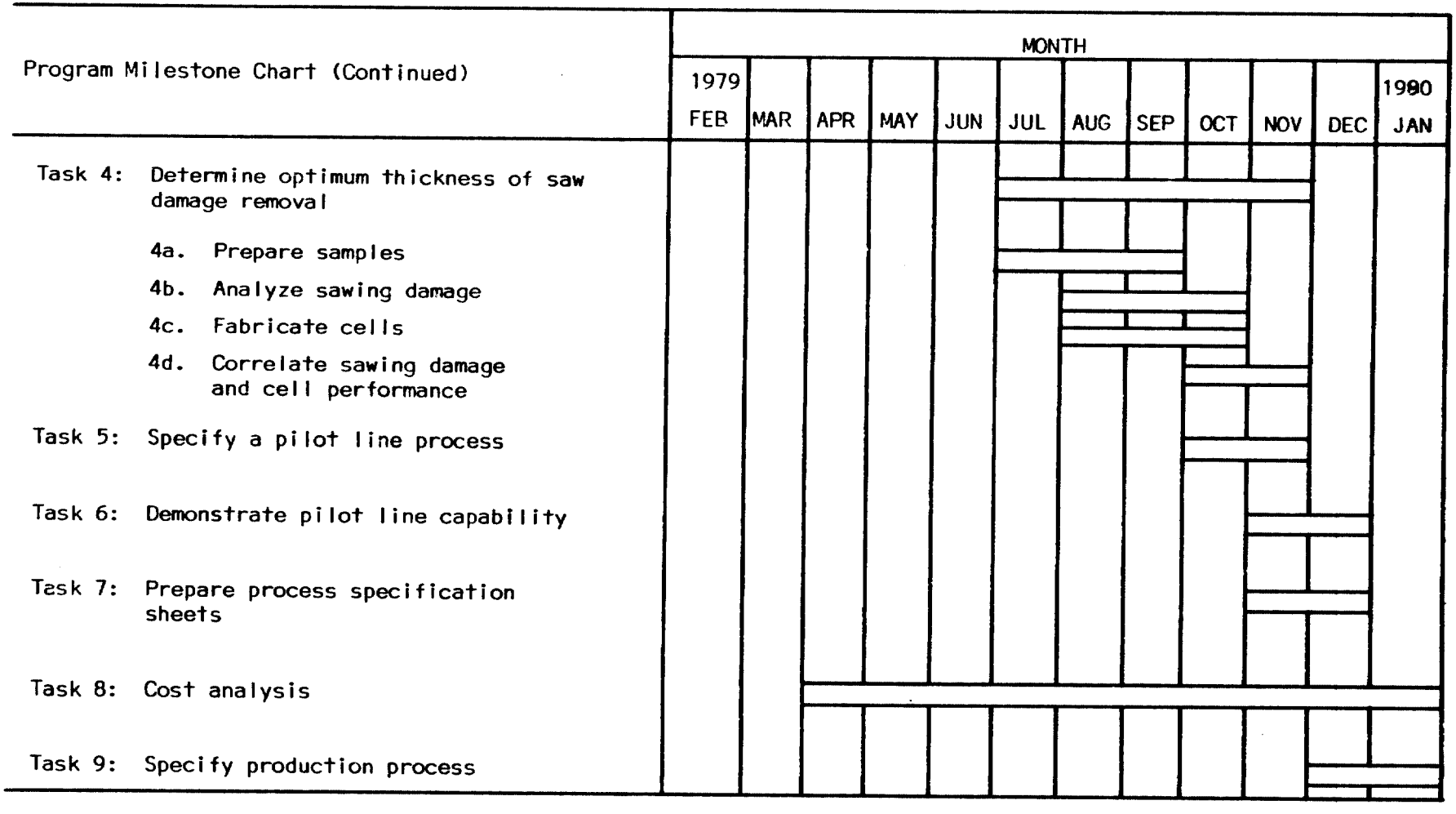

Figure 1 (Continued)

Documentation Milestone Chart

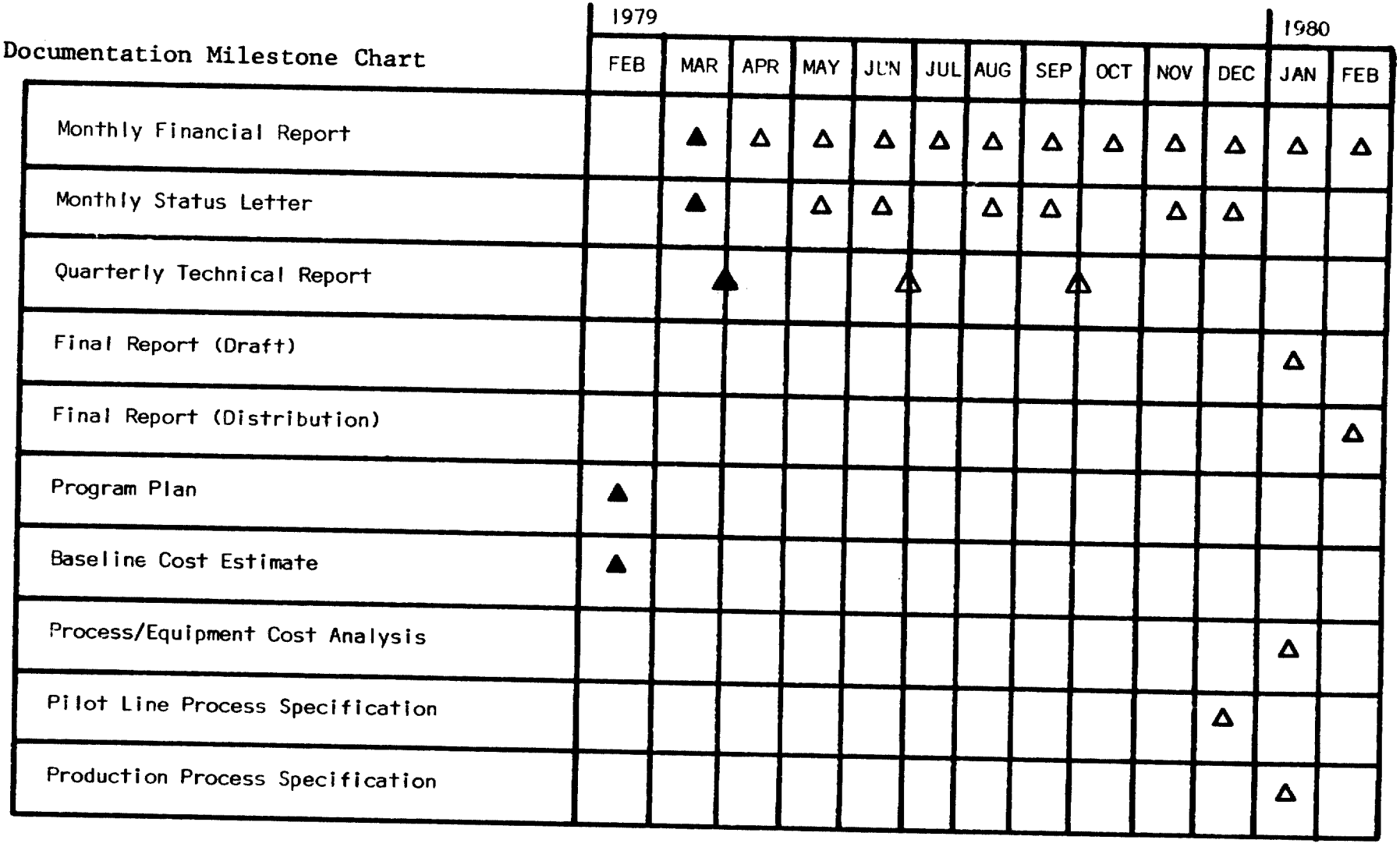

Figure 2