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AUTOMATED ARRAY ASSEMBLY PHASE 2

Texas Instruments Report No. 03-79-28

Quarterly Technical Progress Report

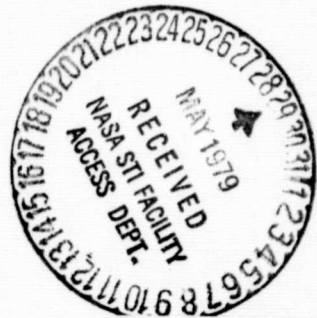
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SECTION I

INTRODUCTION

The Automated Array Assembly Task, Phase 2 of the Low Cost Silicon Solar Array (LSSA) Project is a process development task. This contract provides for the fabrication of modules from large area tandem junction cells (TJC). The key activities in this contract effort are a) Large Area TJC including cell design, process verification and cell fabrication and b) Tandem Junction Module (TJM) including definition of the cell-module interfaces, substrate fabrication, interconnect fabrication and module assembly. The overall goal is to advance solar cell module process technology to meet the 1986 goal of a production capability of 500 megawatts per year at a cost of less than \$500 per peak kilowatt. This contract will focus on the Tandem Junction Module process.

During this quarter, effort was focused on the design of a large area, $\sim 36\text{cm}^2$, TJC and process verification runs. The large area TJC design was optimized for minimum I^2R power losses. In the TJM activity, the cell-module interfaces were defined, module substrates were formed and heat treated and clad metal interconnect strips were fabricated. All activities are on or ahead of schedule.

SECTION II

TECHNICAL DISCUSSION

Both major task areas are in progress. A brief description of the activities in each area follows.

I. Large Area Tandem Junction Cell

1. Cell Design

A cell design has been chosen on the basis of minimum power loss that consists of two interposed finger patterns, one is the N-contact and the other is the P-contact. The N+ and P+ bond pads are located along opposing sides of the cell. The contact fingers will be stepped in width to accomodate increasing current as the finger appraoches the bond pad area. Trunk lines will not be used. A schematic of the cell contact pattern is shown in Figure 1. The stepping of finger width is shown in the figure.

Finger widths and spacings have been set. A worst case loss analysis has been calculated for series resistance and P area on the back side. Total series resistance losses are projected to be 4 - 7% depending on Ag plating thickness and P+ contact resistivity. The corresponding limits on fill factor are calculated to be 0.78 - 0.75, assuming a low nKT current.

I^2R power losses are calculated using equations 1 and 2 to calculate the fractional loss in the P+ fingers and in the base, respectively.

$$F_F = \frac{J_{sc} d m L^2}{24 V_{oc} T_1} + \frac{J_{sc} d m L^2}{24 V_{oc} T_2} \quad (1)$$

and

$$F_B = \frac{J_{sc} d^2}{12 V_{oc}} P_s \text{ (base)} \quad (2)$$

where

J_{sc} = short circuit current density = 0.035 A/cm²

d = center-to-center finger spacing = .102 cm

m = metallization resistivity ($\Omega/\square$) = .005 $\Omega/\square$

L = finger length - 6 cm

T_1 = finger width narrow section = .0076 cm

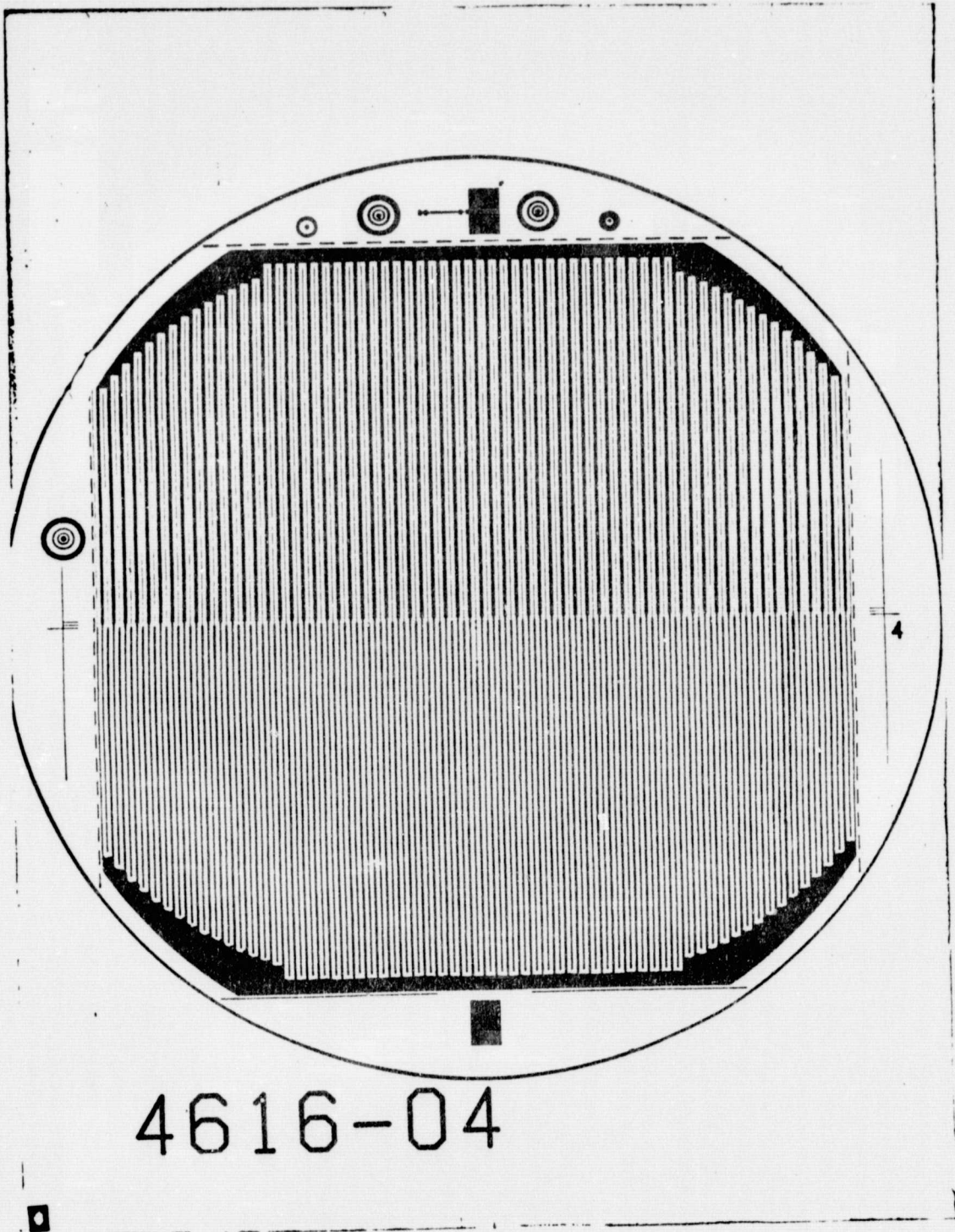


FIGURE I. TJC METAL PATTERN

T_2 = finger width wide section = .0254 cm

V_{oc} = Open circuit voltage = 0.6 V

ρ_s = Base sheet resistivity ($\Omega/\square$) = 533 $\Omega/\square$

The fractional power loss in the fingers, F_F is ~1.7% and in the high resistivity base region is ~2.6% for this design. Other design options using internal plated metal bus bars would give larger fractional power losses.

Bond pad sizes were chosen to facilitate module interconnections using condensation or IR solder techniques and clad metal interconnect ribbon. Bond pad spacing from the cell edge has been defined. The N+ bond pad is located further from the cell edge than the P+ bond pad. This is to protect the N+/P junction from possible damage in the scribe and break operation.

This cell design uses the relatively massive interconnect bar to reduce I^2R power losses in the bonding pad along the cell edge. In this fashion, normal power losses associated with the plated metal bus bars are eliminated.

The design has been coded and plotted at 10X for visual check and verification. The test sites around the edges of the wafer allow testing of the N+ and P+ sheet resistivity, contact resistivity and plated metal sheet resistivity were checked at 100X. Glass masters, at 10X, have been obtained and photomasks are on order.

The design activity will be complete as soon as photomasks are received.

2. Process Verification

Process verification test lots are being run on 2 x 2 cm TJC's. Probe testing is done before sawing into squares by using back side illumination (the light shines between the metal contacts). Only preliminary conclusions can be drawn from these probe tests.

In the variations on back side boron implant, the standard process, 1×10^{14} atom/cm² dose, appears best with the reduced dose levels, 5×10^{13} atom/cm² and 2×10^{13} atom/cm², both giving about 25% lower short circuit current. These cells were sawed and gold ribbon tabs were thermal compression bonded to allow normal front side illumination measurements.

Alloying Al P+ contacts at 650°C or 850°C gives virtually identical results at backside probe. Both temperatures are effective.

Front side illumination after attaching gold tabs gave the following results. In the back side boron implant experiment only the 1×10^{14} atom/cm² implant gave good results, $V_{oc} = 0.586V$, $J_{sc} \approx 35mA/cm^2$ at AM1. The implants at 2 and 5×10^{13} atom/cm² gave very poor results, $V_{oc} \sim 0.5 V$, $J_{sc} \sim 10mA/cm^2$ indicating a severe lifetime degradation during processing. These experiments are being repeated.

Front side illumination tests on cells where the P+ region was created by alloying evaporated Al at 850°C and 650°C showed that the 850°C alloy condition gave slightly better results with V_{oc} rising to 0.595V and J_{sc} increasing to 38mA/cm² at AM1. The 850°C alloy step will be considered for inclusion in the baseline process.

The lot of TJC's run on 150µm thick material show very poor response similar to the lower boron implant cells. The very low photoresponse indicates a severe lifetime degradation. The cause of this degradation is not known at this time.

Contact resistivity on the P+ regions was measured after alloying Al at 650°C and 850°C. The concentric ring pattern described in earlier reports on this contract was used. Contact resistivity between the evaporated Ti-Pd-Ag contact metallization and the alloyed Al P+ layer is shown below. In all cases 4000Å of evaporated Al was used.

	650°C/30 min.	850°C/30 min.
ρ_c (Ω -cm ²)	$2 - 4 \times 10^{-3}$	$.4 - 2 \times 10^{-3}$

Further sinterin of the contacts at 450°C did not appreciably change ρ_c . The ρ_c obtained with the 850°C alloyed Al region is acceptable for cell fabrication.

II. Tandem Junction Module

1. Define Cell - Module

A design review was held in January to review and define the critical items in the cell and module design. The module will be a parallel (5) - series (6) array of 30 cells. The external cell dimension, a nominal 6.2 cm, is shown in figure 1. The N+ and P+ bond pads will be 0.127 cm wide with a 0.025 cm separation from the opposite conductivity metal finger.

The clad metal interconnect strip will span from the P+ bond pad on one cell to the N+ bond pad on the next (series) cell. The interconnect will be designed to fall 0.025 cm from the inside dimension of the bond pad to allow for the solder fillet. The connection will be made using condensation or infrared soldering.

2. Modify Tooling

An analysis of the minimodule size indicates that embossing is not necessary to assure substrate rigidity. On larger substrates, 1.2 x 0.6 m, embossing would be recommended. The embossed groove also provides

recess for the back side interconnects. In the series-parallel configuration chosen for this work, the interconnect thickness is only 0.002 inch (0.0051 cm) and recessing is unnecessary. Therefore tooling modification was not necessary and was eliminated.

Sheet steel has been cut, Figure 2, and formed to shape. Twenty (20) substrates were formed using 20 gauge (0.0359 inch, 0.0912 cm) cold rolled steel and twenty (20) substrates were formed using 22 gauge (0.0299 inch, 0.0759 cm) cold rolled steel. Top and front views of the formed cold rolled steel for the substrate are shown in Figure 3.

3. Define Heat Treatment

Ten (10) formed substrates of each gauge cold rolled steel were stress relieved at 600°F (316°C) for one hour in air. The substrates were shipped to Ervite Corporation, Erie, Pennsylvania, for porcelainizing. Evaluation of the heat treatment will be made after porcelainizing.

4. Porcelainize Substrates

See paragraph II. 3 above. The porcelainized substrates should be received in April.

5. Design and Form Bus Bars

As demonstrated earlier in this contract, copper/Invar/copper laminates can be fabricated to match the thermal expansion coefficient of silicon. The tandem junction module interconnect scheme will use thin ribbons of this clad metal material. Copper/Invar/copper has been bonded with a 12.5/75/12/5 ratio, and rolled to a thickness of 0.0102 cm. The bus bar material will subsequently be rolled to a final thickness of 0.0051 cm.

The minimum allowable bus bar thickness can be calculated by defining the minimum allowable power loss in the bus bar. If we allow a 1% I²R power loss and assume a cell output of 1.0A at 0.5V, then minimum bus bar thickness is calculated as follows:

$$\Delta P = I^2 R_C \quad (3)$$

where

$$\Delta P = \text{allowable loss} = .01 \times 1.0 \times .5 = .005W$$

$$I = \text{Cell output}$$

$$R_C = \text{Resistance of clad bus bar}$$

then

$$0.005 W = (1.0)^2 R_C$$

$$R_C = .005 \Omega$$

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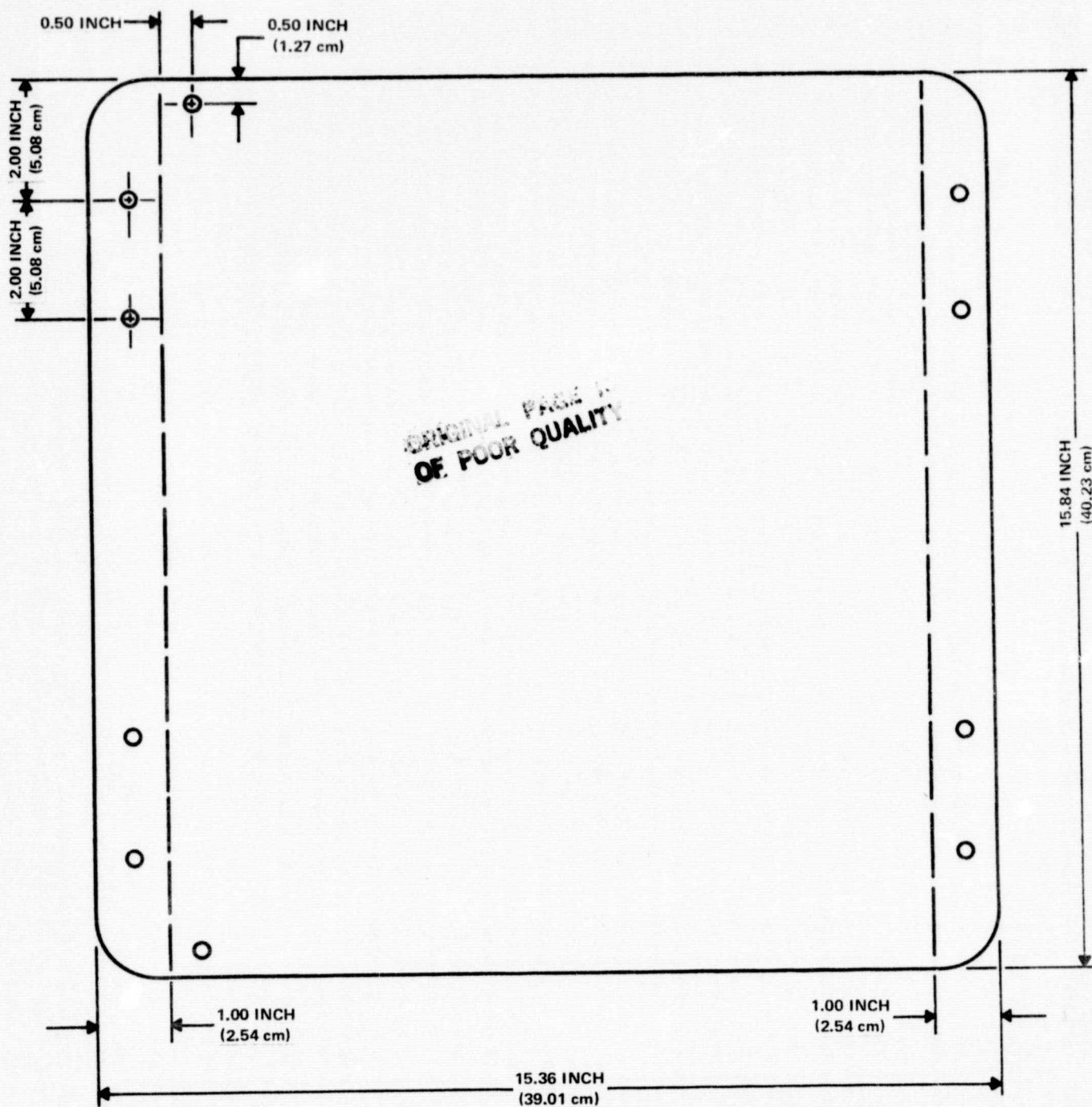


FIGURE 2. TOP VIEW OF SUBSTRATE BLANK

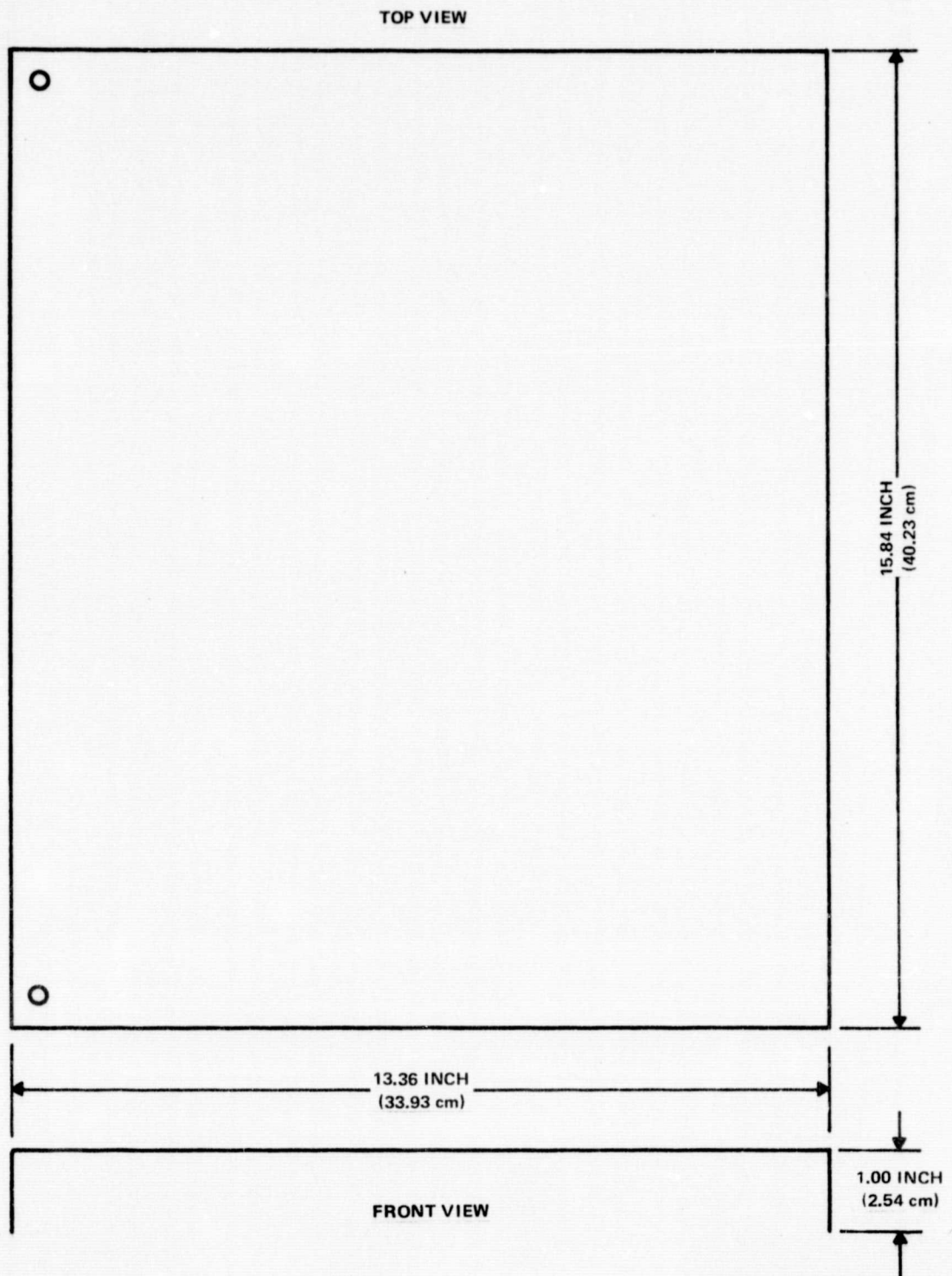


FIGURE 3. FORMED SUBSTRATE

The resistance of the composite clad metal conductor can be calculated as a set of parallel layers

$$\frac{1}{R_c} = \frac{1}{R_1} + \frac{1}{R_2} + \dots + \frac{1}{R_n}$$

where $R_1, R_2, \dots, R_n$ are the respective resistances of the clad metal layers.

By combining the top and bottom copper layers into one term we get.

$$\frac{1}{R_c} = \frac{1}{R_{Cu}} + \frac{1}{R_{Invar}} \quad (4)$$

or

$$\frac{1}{R_c} = \frac{W \times t_{Cu}}{\rho_{Cu} \times L} + \frac{W \times t_{Invar}}{\rho_{Invar} \times L} \quad (5)$$

where

- W = width of bus bar = 4 cm
- L = length of bus bars = 0.2 cm
- t_{Cu} = Total copper thickness = 0.25 T_B
- t_{Invar} = Invar thickness = 0.75 T_B
- ρ_{Cu} = Resistivity of copper = $1.7 \times 10^{-6} \Omega\text{-cm}$
- ρ_{Invar} = Resistivity of Invar = $5.0 \times 10^{-5} \Omega\text{-cm}$
- T_B = Thickness of bus bar

Solving for T_B we get

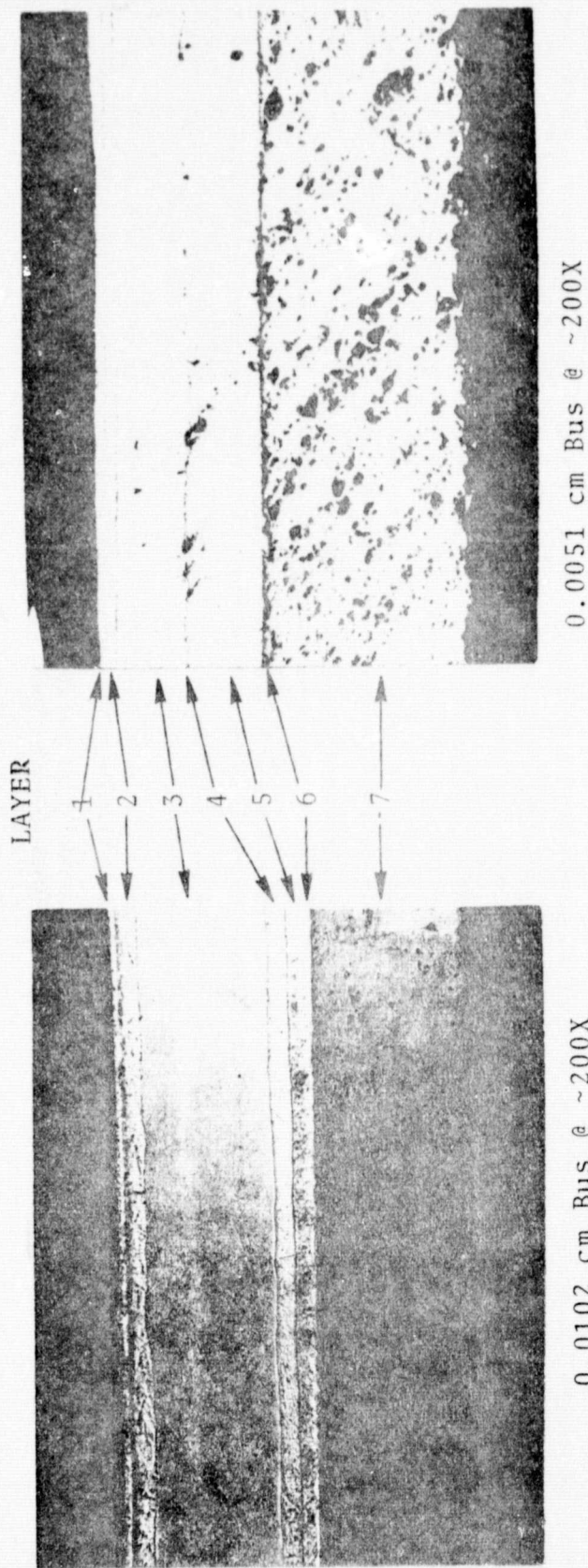
$$T_B = 6.2 \times 10^{-5} \text{ cm}$$

Therefore one would expect a negligible loss in the bus bar interconnects of 5.1×10^{-5} cm thickness.

6. Solder Fixture

Soldering evaluations were conducted with bus bar thickness of 0.025 cm, 0.0102 cm, and 0.0051 cm using 2 x 2 cm TJC's. Cross sections of the soldered interconnects are shown in figure 4. No problems were encountered nor are expected with the bond integrity at the bus bar - plated Ag interface. The thin, 0.0051 cm, clad metal interconnects perform as expected.

A vacuum chucked soldering fixture has been designed for module fabrication. The fixture is ~70% complete and should be ready for evaluation as soon as large area TJC test samples are ready.



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FIGURE 4. CROSS SECTIONS OF CLAD METAL INTERCONNECTS SOLDERED TO TJCS.

SECTION III

CONCLUSIONS AND RECOMMENDATIONS

- Solar cell - module interrelations were defined prior to finalization of the TJC or TJM design. The TJC will have N+ and P+ metal contact pads, one each, on opposite edges of the cell. The cell-to-cell interconnects will provide the collecting bus bar function.
- In the TJC structure, a back side boron implant dose of 1×10^{14} atom/cm² appears to be near optimum as a psuedo back surface field.
- Sample TJMs will contain 30 cells in a parallel (5) - series (6) array. Interconnection will be made using copper clad Invar ribbon. The clad metal ribbon thickness will be 0.005 cm. Soldering experiments have shown that the ribbon can be readily soldered to plated Ag contacts.

SECTION IV
NEW TECHNOLOGY

No areas of new technology were identified this quarter.

SECTION V

PROGRAM SUMMARY

Figure 5 shows the current work plan status. All scheduled activities are in process. No problems are apparent at present that will prevent attaining the indicated milestones.

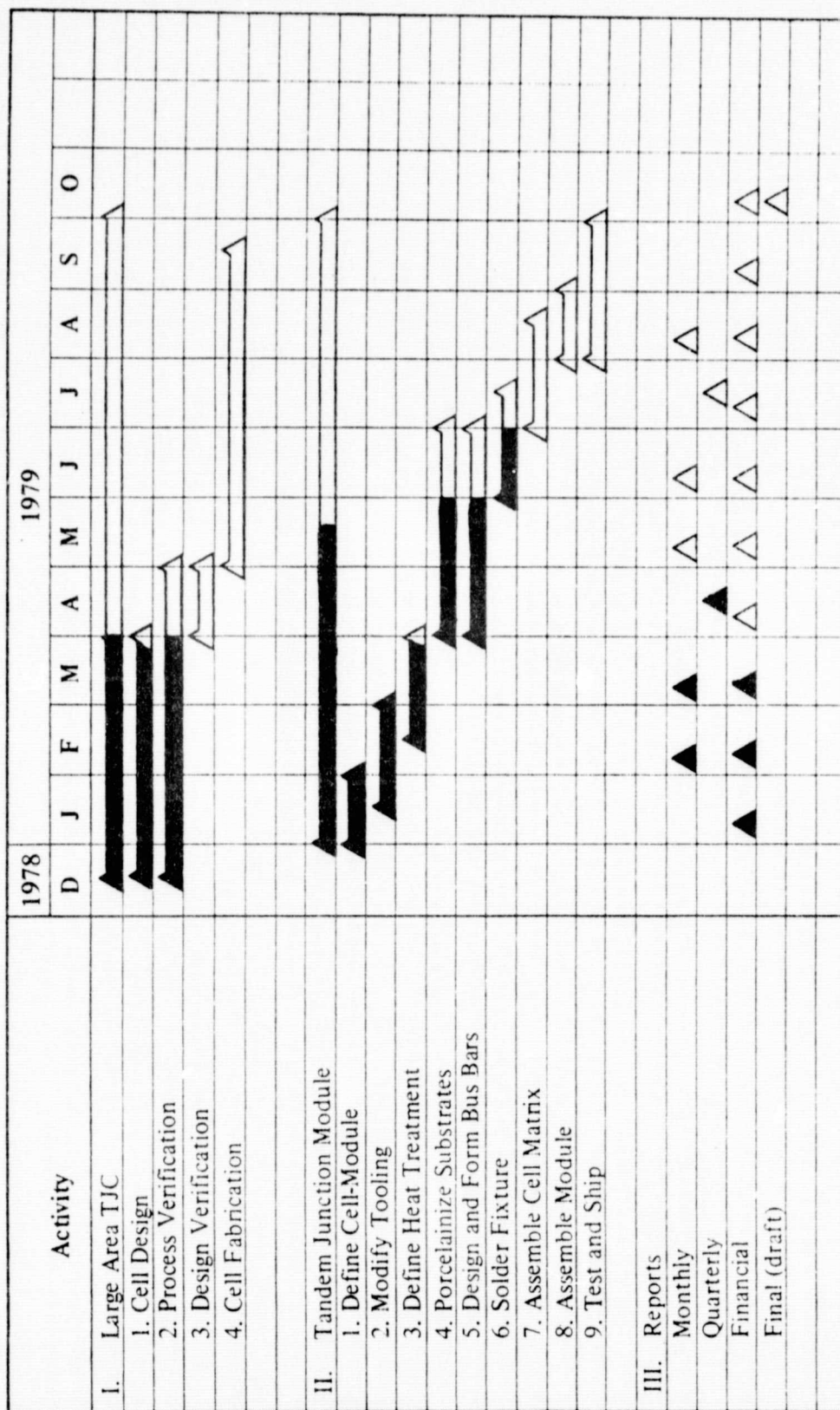


Figure 5. Work Plan Status