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ELECTRICAL CHARACTERIZATION OF HUGHES HCMP 1853D AND RCA CDP1853D N-BIT, CMOS, 1-OF-8 DECODER MICROCIRCUITS

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AEROSPACE GROUPS
HUGHES
HUGHES AIRCRAFT COMPANY
CULVER CITY, CALIFORNIA

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TEST ABSTRACT

Twenty-five Hughes HCMP 1853D and 25 RCA CDP1853D microcircuits were subjected to electrical characterization tests. The devices were subjected to functional and AC and DC parametric tests at ambient temperatures of -55°C, -20°C, 25°C, 85°C, and 125°C. All measurements were performed on a Tektronix S-3260 Test System located at the Hughes Aircraft Company Technology Support Division in Culver City, California. Temperature environment was provided by a Temptronic thermal airstream system under program control.

All 50 devices passed the functional tests and yielded nominal values in the AC and DC parametric tests.

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1.0 INTRODUCTION

This report documents the results of electrical characterization tests performed to determine the electrical performance characteristics of 25 RCA CDP1853D and 25 Hughes HCMP 1853D CMOS integrated circuits. The performance characteristics were measured under various electrical conditions at five temperatures. The data was analyzed and tabulated to show the effect of operating conditions on performance and to indicate parameter deviations among devices in each group. This information can be used in evaluating typical device performance and in determining specification limits. Accuracy was given precedence over test-time efficiency where practical, and tests were designed to measure worst-case performance.

The tests were divided into three categories: functional, AC parametric, and DC parametric. The functional tests were performed on a pass/fail basis to verify that the device under test (DUT) was logically correct. All voltage and timing conditions (except supply voltage) were set to nominal values to distinguish between functional failures and statistically unusual devices. The AC parametric tests consisted of propagation delays and transition times. These were measured either by a one-shot technique or by a moving strobe method, depending on the nature of the measured parameter. The DC parametric tests were simple static measurements made by forcing specified conditions on the DUT and measuring a voltage or current.

All of these tests were performed under computer program control on a Tektronix S-3260 Automated Test System. All devices were subjected to the full set of tests at ambient temperatures of -55°C, -20°C, 25°C, 85°C, and 125°C. The temperature environment was provided by a Temptronic thermal airstream unit (TP450A) under program control.

Twenty-five devices from each manufacturer (RCA and Hughes) were tested. The data was tabulated and analyzed separately for each lot. There were no functional failures or significantly deviant devices in either lot.

2.0 DEVICE DESCRIPTION

The RCA CDP1853D and Hughes HCMP 1853D are N-bit (expandable) 1-of-8 decoders for use in 1800-series microprocessor systems. They are designed to interface directly with the 1802 microprocessor and to function properly at its maximum operating speed. They use static, silicon-gate, CMOS circuitry with a single voltage supply. They are compatible with 4000-series microcircuits and can be used as general-purpose, 1-of-8 decoders. They are supplied in hermetic, 16-lead, dual-in-line ceramic packages.

A brief functional description of the 1853 device is given in Paragraph 2.2. Pin connections are shown in Figure 1, and a functional diagram appears in Figure 2.

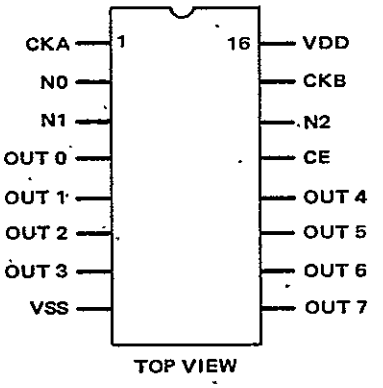


Figure 1. 1853 Pin Connections

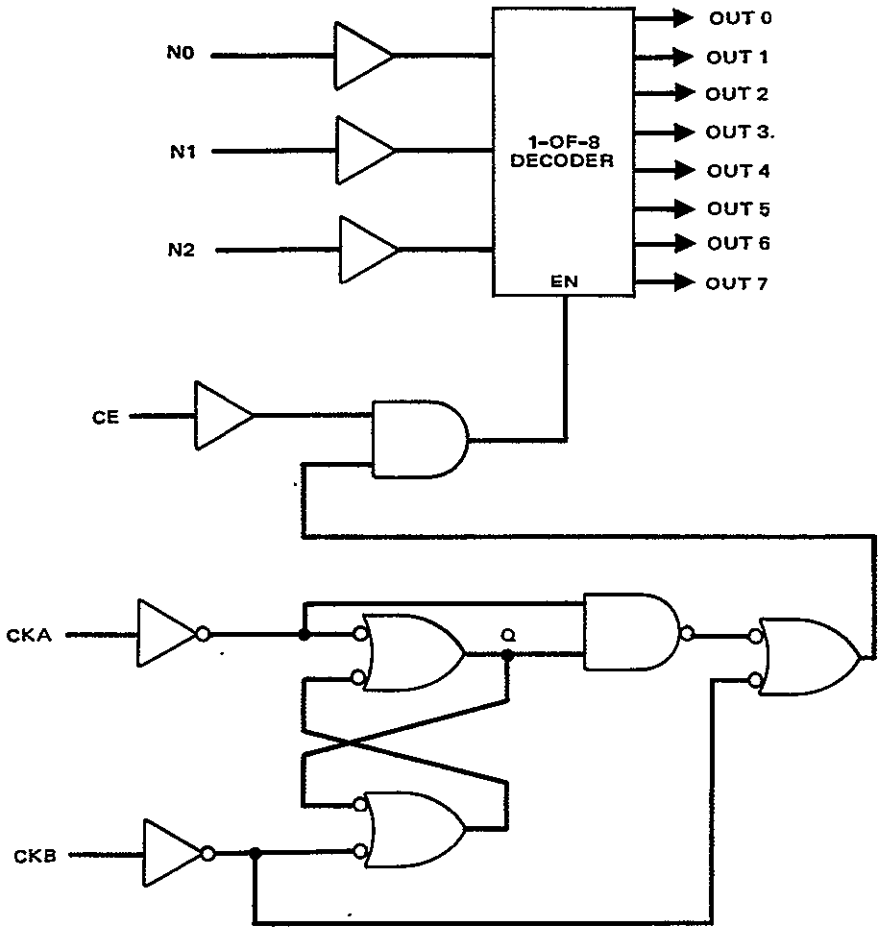


Figure 2. 1853 Functional Diagram

2.1 PIN DESCRIPTIONS

2.1.1 N Inputs (N0, N1, N2)

The N inputs provide a 3-bit binary code to select one of the eight outputs (refer to Table 1).

2.1.2 Chip Enable Input (CE)

The chip enable input provides multibit capability. All outputs are low when CE is low.

TABLE 1. TRUTH TABLE

CE	CLA	CLB	EN*	Q*
1	0	0	Q	Q_{n-1}**
1	0	1	1	0
1	1	0	0	1
1	1	1	1	1
0	X	X	0	-

*Q and EN are internal signals, provided here for reference only.

**Remains in previous state.

N2	N1	N0	EN	0	1	2	3	4	5	6	7
0	0	0	1	1	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0	1	0	0
1	1	0	1	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1
X	X	X	0	0	0	0	0	0	0	0	0

The clock inputs determine output timing when CE is high (refer to Table 1).

2.1.4 Outputs (OUT0 through OUT7)

Outputs OUT0 through OUT7 are the eight selectable outputs.

2.2 OPERATION

The N inputs select one of the eight outputs to be high under certain conditions of the chip enable and clock inputs. When the chip enable input is low, all outputs are low. The two clock inputs operate a latch which determines output behavior when CE is high. Refer to Table 1 for details.

3.0 DESCRIPTION OF TESTS

Testing any parameter of an 1853 device involves applying input stimuli to the device and observing its response. The details of these two actions define the specific test or measurement. Microcircuit tests can be divided into functional tests, AC parametric tests, and DC parametric tests. The following are brief explanations of the methods used with the Tektronix S-3260 to perform these tests.

3.1 FUNCTIONAL TESTS

Functional tests are performed on a pass/fail basis using a pattern of logic "1"s and "0"s. The pattern defines a series of stimuli to be presented at the DUT inputs and a series of results to be expected at the outputs. The input levels are provided by drivers whose voltage levels can be programmed individually for each input and whose state (1, 0, or inhibited) are controlled by the pattern. The expected DUT output levels are checked by comparators which are also individually programmable and under pattern control. The comparators are strobed so that the output is sampled only during a specific time interval. An error is detected under the following conditions:

1. During comparison for a 1, if the DUT output is less than the logic "1" compare level at any time during the compare window

2. During comparison for a 0, if the DUT output is greater than the logic "0" compare level at any time during the compare window (see Figure 3).

The placement of the compare window and the frequency at which the pattern is run are under program control.

The functional tests were performed using the pattern shown in Table 2. The test conditions are shown in Table 3.

3.2 AC PARAMETRIC TESTS

AC parametric tests performed on the 1853 devices include propagation delays and transition times. There are two ways to measure propagation delays on the S-3260. The most efficient is the one-shot (real time) method, which makes a direct measurement of the time between two transitions. The trigger levels at which the measurement clock starts and stops are determined by comparator settings and are programmable. The other method for propagation delay measurements is the moving-strobe method. This method involves running a functional test pattern (see Paragraph 3.1) while varying the placement of the compare window. If the strobe is moved from a failing condition (short starting time) to a passing condition (longer starting time), the difference between the input transition and the start time at which the output first

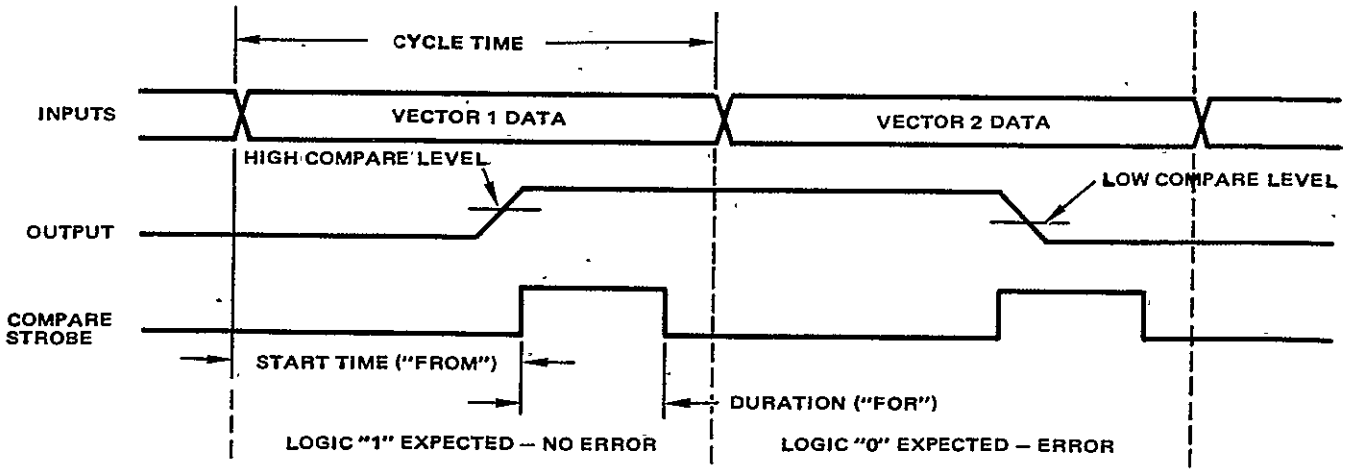


Figure 3. Functional Test Timing

TABLE 2. FUNCTIONAL TEST PATTERN

	Name	Pin	Time Slots															
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Inputs	CLA	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	0
	CLB	15	1	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0
	CE	13	1	1	1	1	0	1	1	1	1	0	1	1	1	1	1	1
	N0	2	0	1	0	1	1	0	1	0	1	1	0	0	0	0	1	1
	N1	3	0	0	1	1	1	0	0	1	1	1	0	0	0	0	1	1
	N2	14	0	0	0	0	0	1	1	1	1	1	0	0	0	0	1	1
Outputs	0	4	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0
	1	5	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	2	6	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	3	7	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	4	12	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	5	11	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	6	10	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	7	9	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

TABLE 3. FUNCTIONAL TEST CONDITIONS

Conditions	At 3V	At 15V
Drivers, high (Logic "1")	3V	15V
Drivers, low (logic "0")	0V	0V
Comparators, high	1.5V	7.5V
Comparators, low	1.5V	7.5V
Cycle time (period)	16 μs	16 μs
Compare window: Start	15.95 μs	15.95 μs
Duration	8 ns	8 ns

passes is the propagation delay. Voltage levels for this method can be controlled as in the functional tests.

Transition times are measured indirectly. Propagation delays are measured to the output-under-test at two levels (usually 10 percent and 90 percent of swing). The difference between the two delays is the transition time between the two levels.

The following AC parameters were measured at VDD voltages of 5V and 10V (refer to Table 4 for test conditions):

Propagation Delays (Figure 4)

1. Chip enable high to output high (TEOH)
2. Chip enable high to output low (TEOL)
3. N input change to output high (TNOH)
4. N input change to output low (TNOL)
5. Clock A low to output high (TAO)
6. Clock B low to output low (TBO).

Transition Times (Figure 5)

1. Output transition, low to high (TTLH)
2. Output transition, high to low (TTHL).

TABLE 4. AC-PARAMETRIC TEST CONDITIONS

Parameters	At VDD = 5V	At VDD = 10V
Drivers high	5V	10V
Drivers low	0V	0V
Comparators:		
High (prop. delays)	2.5V	5V
Low (prop. delays)	2.5V	5V
High (trans times)	4.5V	9V
Low (trans times)	0.5V	1V
Cycle time	5μs	5μs
Output loads - Figure 6	200kΩ, 50 pF	200kΩ, 50 pF

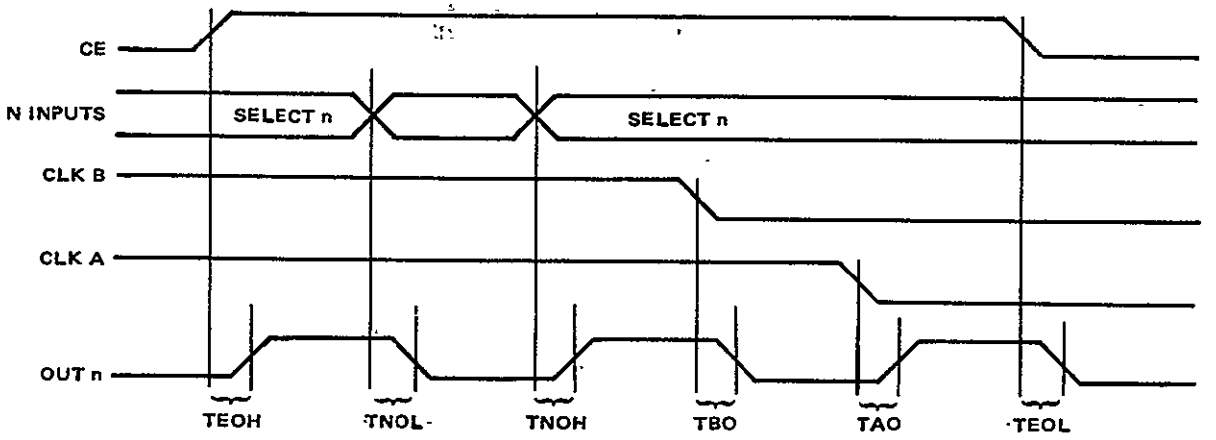


Figure 4. Propagation Delay Timing.

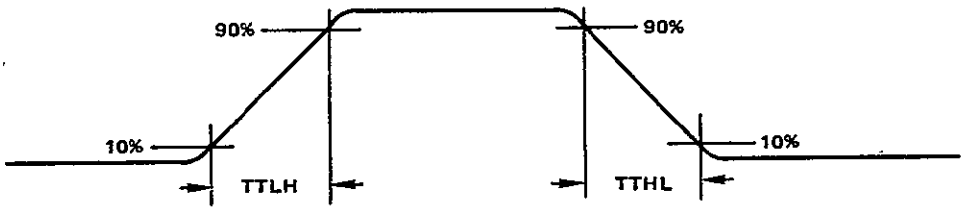
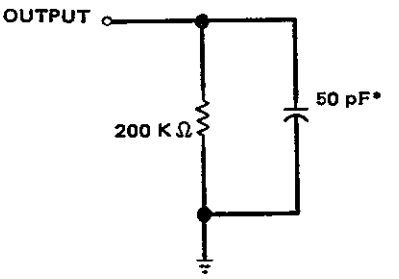


Figure 5. Transition Time



*INCLUDES SYSTEM CAPACITANCE

Figure 6. Output Load

All AC parametric measurements except TNOH and TNOL were measured using the one-shot method. TNOH and TNOL were measured using the moving-strobe method with a pattern similar to a memory ping-pong read. In this pattern, the N inputs were switched so that the outputs were enabled as follows: 0, 1, 0, 2, 0, 3, 0, 4...0, 7, 1, 2, 1, 3...1, 7, 2, 3... etc. This pattern ensures that the worst delay to a given state will be recorded.

3.3 DC PARAMETRIC TESTS

Most of the DC parametric tests were performed in a straightforward manner. Input conditions were applied using the drivers as in the functional and AC tests, and the pin under test was forced with a regulated voltage or current supply (depending on the specific parameter). The desired parameter was then measured and recorded.

The exceptions were the VIH (minimum logic "1" input voltage) and VIL (maximum logic "0" input voltage) tests. These were similar to the walking-strobe propagation delay tests, except that input voltages were moved instead of output compare windows.

In the VIH test, all inputs except the one under test had drive levels of VDD and 0V. Timing conditions were generous. The logic "0" level of the input under test was set at 0V, and the logic "1" level was set to a low enough to ensure voltages that the device would fail to function properly. The functional test was run repeatedly, with the logic "1" level on the input under test raised each time, until the device passed. The voltage at which the device first passed was the minimum logic "1" voltage for the input under test. The VIL test was performed in a similar manner.

Table 5 lists the DC parameters measured, with the exception of VIH and VIL. These two parameters were measured using the functional test pattern of Table 2. The timing and output comparator conditions were the same as those for the functional tests (refer to Paragraph 2.2). The input voltages were varied in 0.1-volt increments as shown in Table 7. Each input was tested separately at each voltage.

TABLE 5. DC-PARAMETRIC TESTS

Symbol	Parameter	Pin	Voltage/Current Forced	VDD-VSS (Volts)	Comments
VICP	Positive input clamp voltage	Each input	1mA	0	VDD and VSS tied to ground
VICN	Negative input clamp voltage	Each input	-1mA	0	VDD and VSS tied to ground
IIH	Input current, high	Each input	15V	15	0V on other inputs
IIL	Input current, low	Each input	0V	15	15V on other inputs
IOH	Output current, high	Each output	4.6V 4.5V 9.5V 9.0V 10.5V	5 5 10 10 12	Output under test is in high (logic "1") state
IOL	Output current, low	Each output	0.4V 0.5V 0.5V 1.0V 1.5V	5 5 10 10 12	Output under test is in low (logic "0") state
ISS	Quiescent supply current	VSS	0V 0V	10 15	Inputs forced per Table 6. Logic "1" = VDD, Logic "0" = VSS. Outputs open. Ten tests at each voltage.

TABLE 6. ISS PATTERN

Inputs	CLA	CLB	CE	N0	N1	N2
I_{SS1}	1	1	1	0	0	0
2	1	1	1	1	0	0
3	1	1	1	0	1	0
4	1	1	1	1	1	0
5	1	1	1	0	0	1
6	1	1	1	1	0	1
7	1	0	1	0	1	1
8	0	0	1	0	1	1
9	0	1	1	1	1	1
10	0	1	0	1	1	1

TABLE 7. VIH AND VIL TEST CONDITIONS

Parameter	Varied		Input Under Test		Other Inputs		Output Compare	
	From (V)	To (V)	VIH (V)	VIL (V)	VIH (V)	VIL (V)	High (V)	Low (V)
VIH (5V)	0	5		0	5	0	2.5	2.5
VIL (5V)	5	0	5	-	5	0	2.5	2.5
VIH (10V)	0	10	-	0	10	0	5	5
VIL (10V)	10	0	10	-	10	0	5	5
VIH (12V)	0	12	-	0	12	0	6	6
VIL (12V)	12	0	12	-	12	0	6	6

4.0 TEST RESULTS

4.1 SUMMARY

All of the devices in both groups passed the functional tests and yielded nominal values in the parametric tests.

4.2 DATA TABULATION

For each parameter, the data was tabulated by device serial number and temperature. The sign "<*" to the right of a value was used to indicate an out-of-range measurement. The minimum, maximum, mean, standard deviation, and median values were listed at the bottom of each temperature column. Out-of-range measurements were excluded from the statistics.

The RCA parts were numbered 3 through 27; the Hughes parts were numbered 28 through 52. The statistics for each group were calculated separately.

In addition to the printed data, histograms of some parameters were provided. Each histogram displays data for one or more parameters at all five temperatures, in ascending order (-55°C, -20°C, 25°C, 85°C, 125°C). The histograms illustrate clearly both the effect of temperature and the distribution of devices for each parameter. RCA and Hughes parts were plotted separately. Table 8 is a list of the parameters plotted. The histograms are provided in Appendix A.

TABLE 8. LIST OF HISTOGRAMS

Parameter	Conditions	
ISS	VDD = 15V	
IOH	VDD = 5V, VO = 4.6V	
	VDD = 10V, VO = 9.5V	
IOL	VDD = 5V, VO = 0.4V	
	VDD = 10V, VO = 0.5V	
TEOH and TEOL	VDD = 5V	
	VDD = 10V	
TNOH	VDD = 5V, 10V	Two histograms
TNOL	VDD = 5V, 10V	
TAO	VDD = 5V, 10V	
TBO	VDD = 5V, 10V	
TTLH and TTHL	VDD = 5V, 10V	

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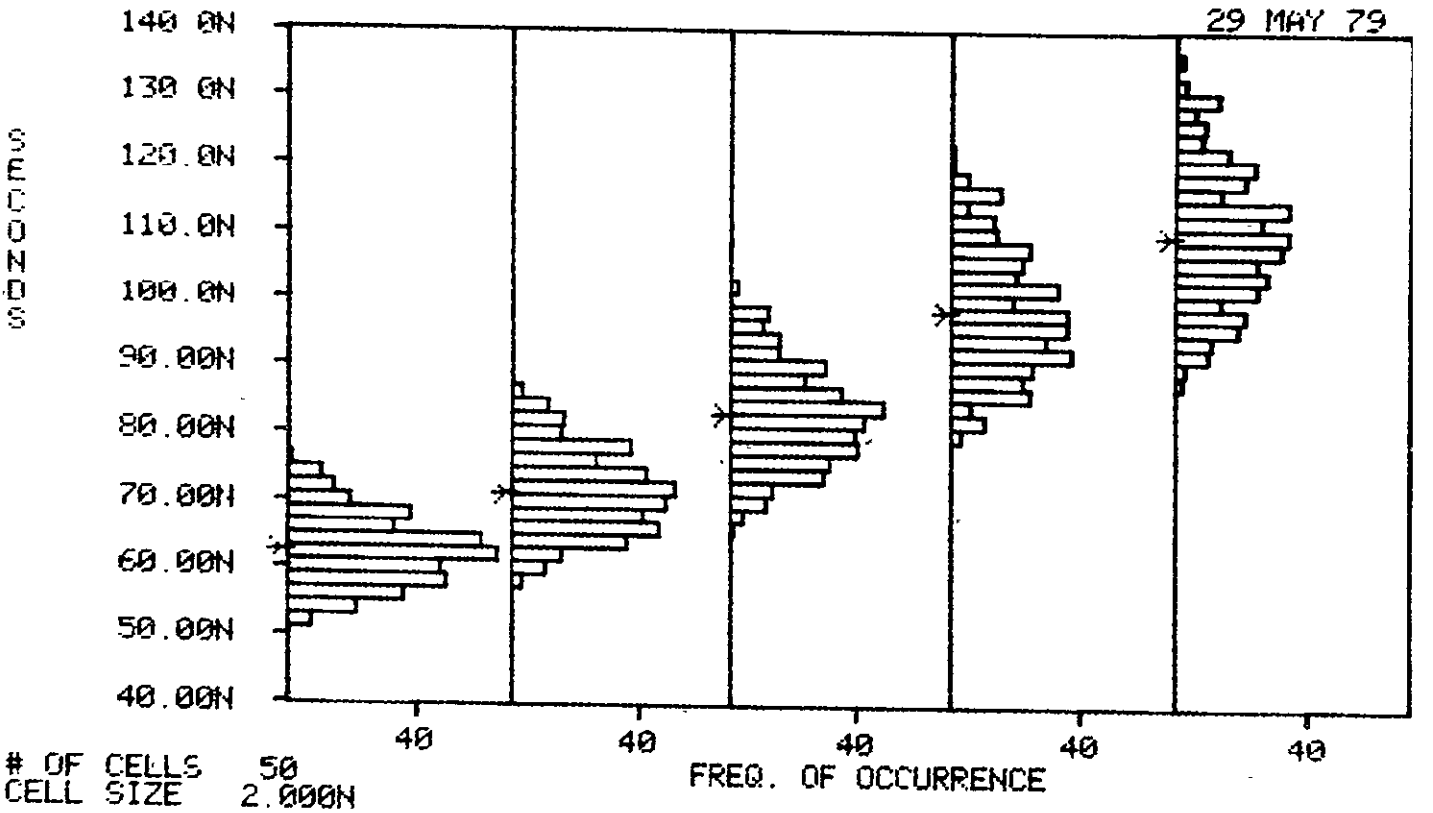
APPENDIX A

HISTOGRAMS

HUGHES HCMP1853D

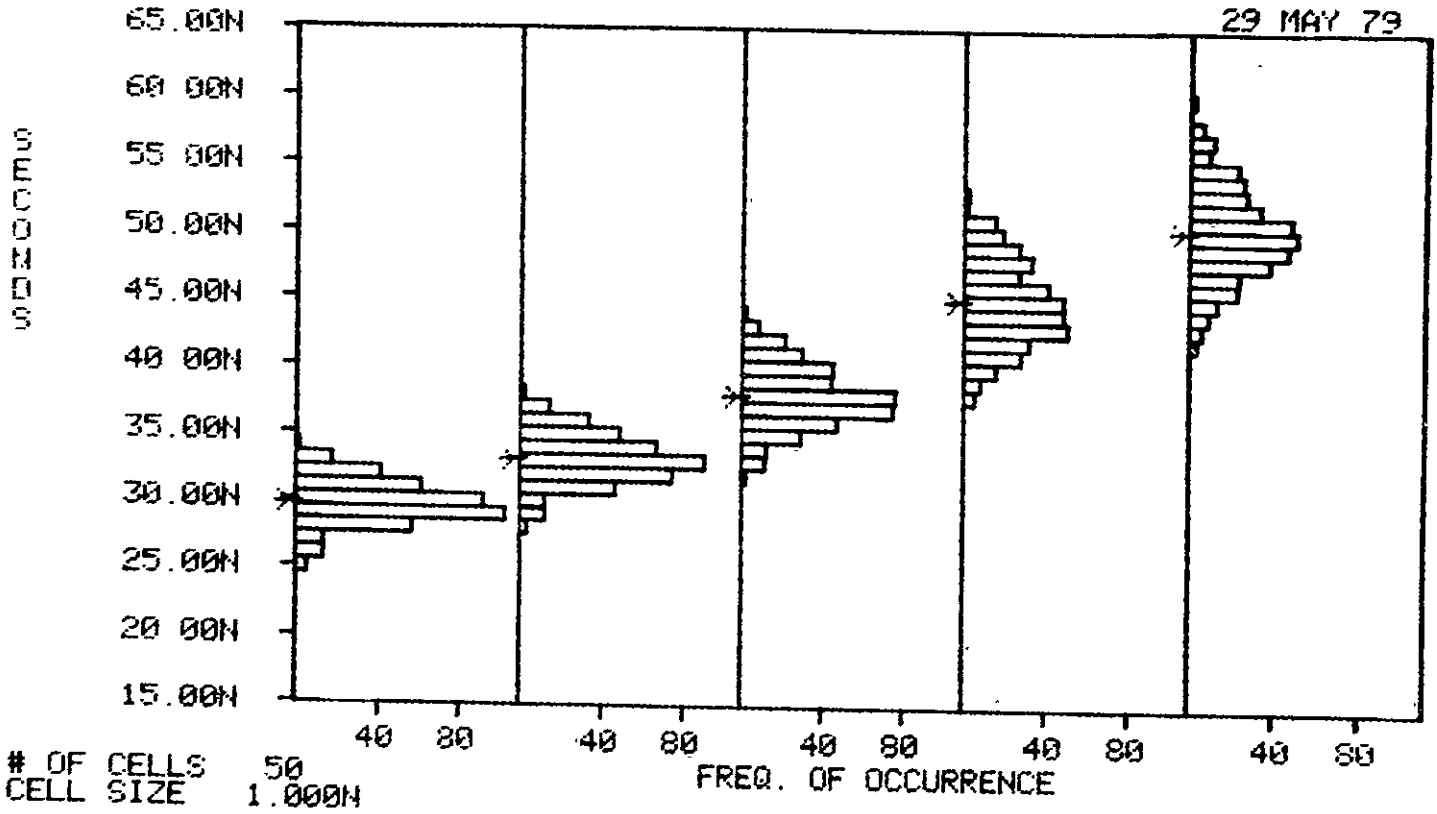
S-3260 DATA FOR TE01 TEOH/TEOL: VDD=5V



OF CELLS 50
CELL SIZE 2.000N

READINGS	400	400	400	400	400
MAXIMUM:	75.25N	86.25N	102.0N	121.0N	136.0N
MEAN:	62.40N	71.29N	82.74N	98.18N	109.8N
MINIMUM:	51.10N	57.85N	66.80N	79.15N	87.85N
STD DEV.:	5.126N	6.032N	7.166N	8.955N	10.03N

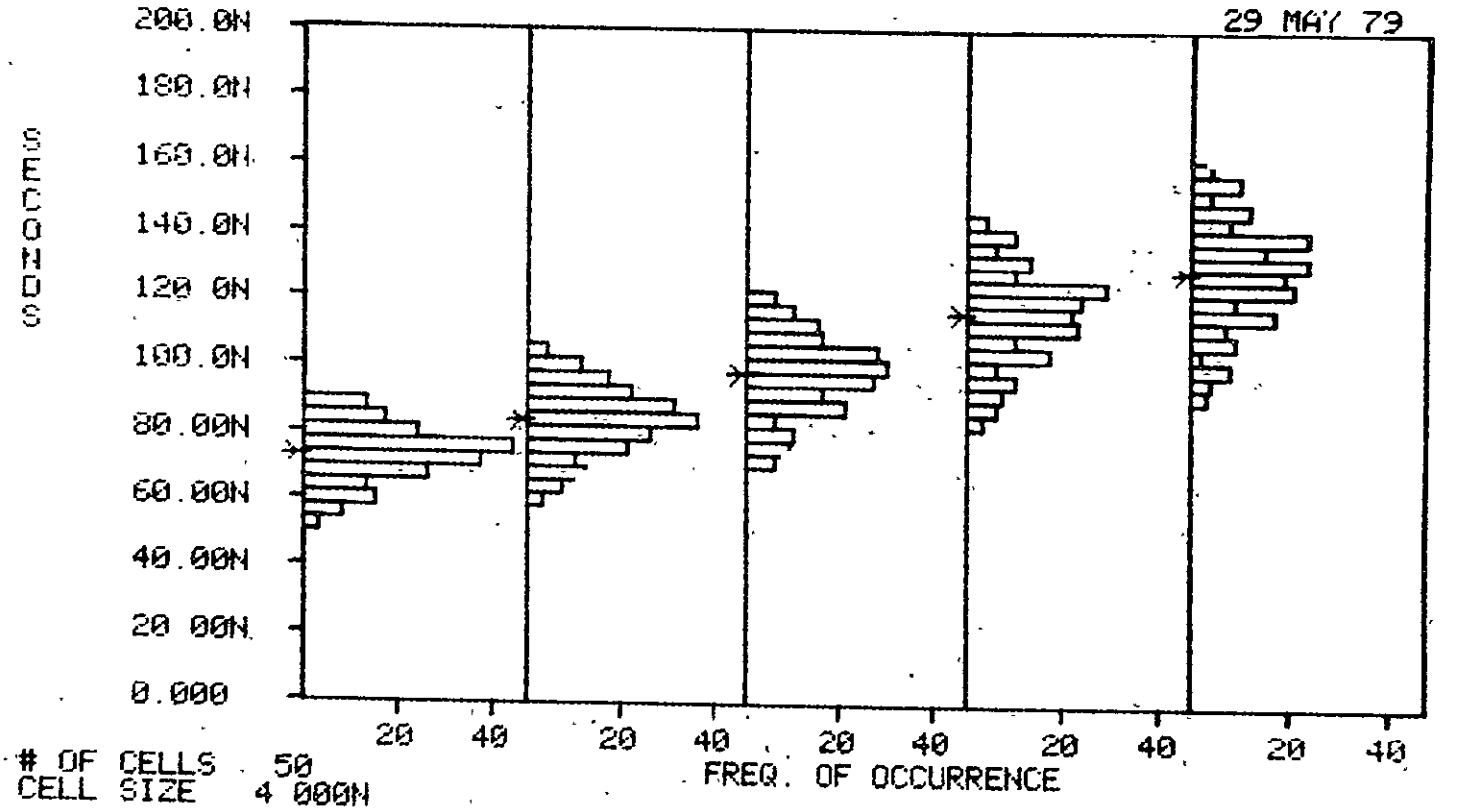
5-3260 DATA FOR TE02 TEOH/TEOL: VDD=10V



OF CELLS 50
CELL SIZE 1.000N

READINGS	400	400	400	400	400
MAXIMUM:	33.60N	37.70N	44.20N	52.85N	60.00N
MEAN:	29.66N	33.12N	37.93N	44.95N	50.32N
MINIMUM:	24.55N	27.65N	31.70N	37.50N	42.00N
STD.DEV.	1.656N	1.897N	2.322N	3.151N	3.432N

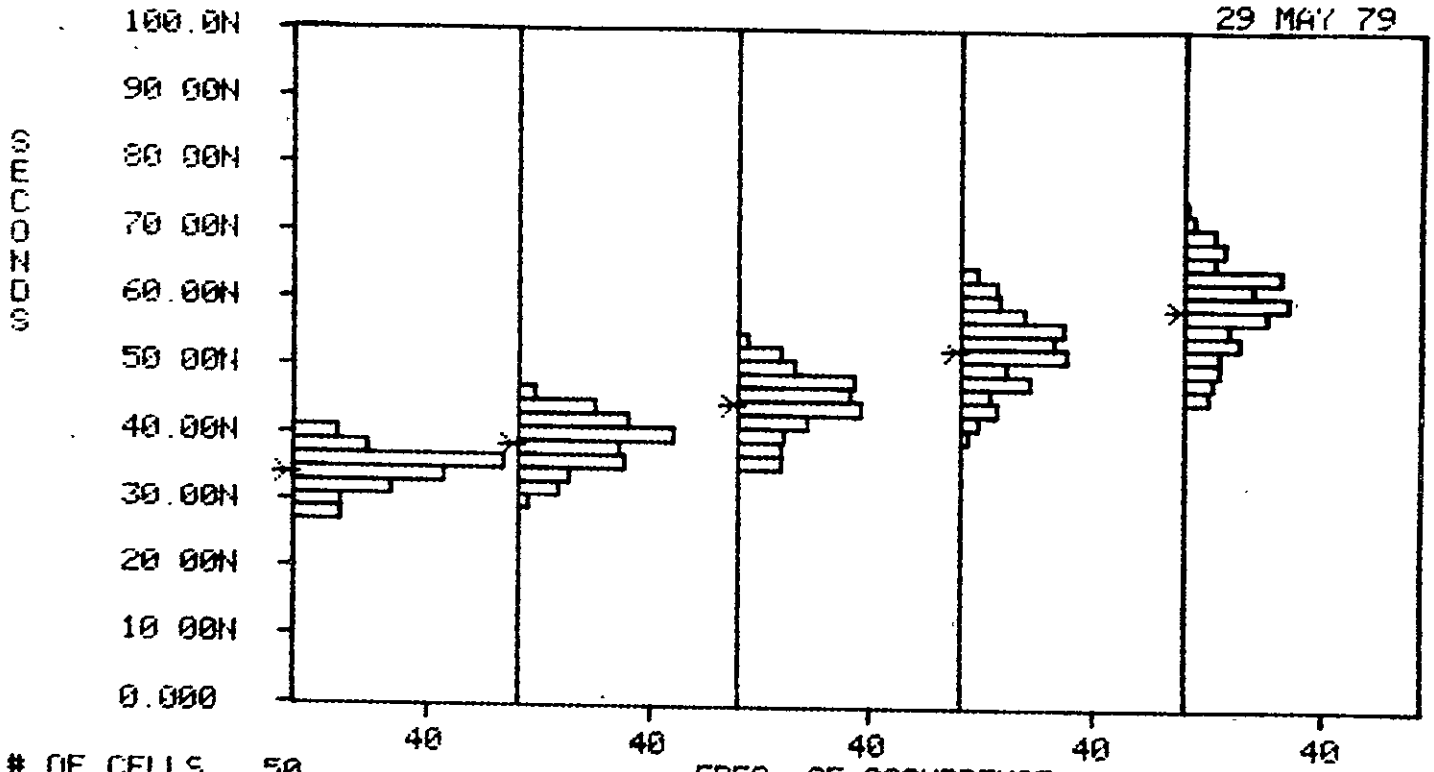
S-3260 DATA FOR TNOH1 TNOH: VDD=5V



OF CELLS 50
CELL SIZE 4.000N

READINGS:	200	200	200	200	200
MAXIMUM:	89.00N	103.0N	121.0N	145.0N	161.0N
MEAN:	72.64N	83.51N	97.50N	115.8N	128.8N
MINIMUM:	53.00N	61.00N	71.00N	83.00N	92.00N
STD.DEV :	8.298N	9.735N	11.65N	14.06N	15.77N

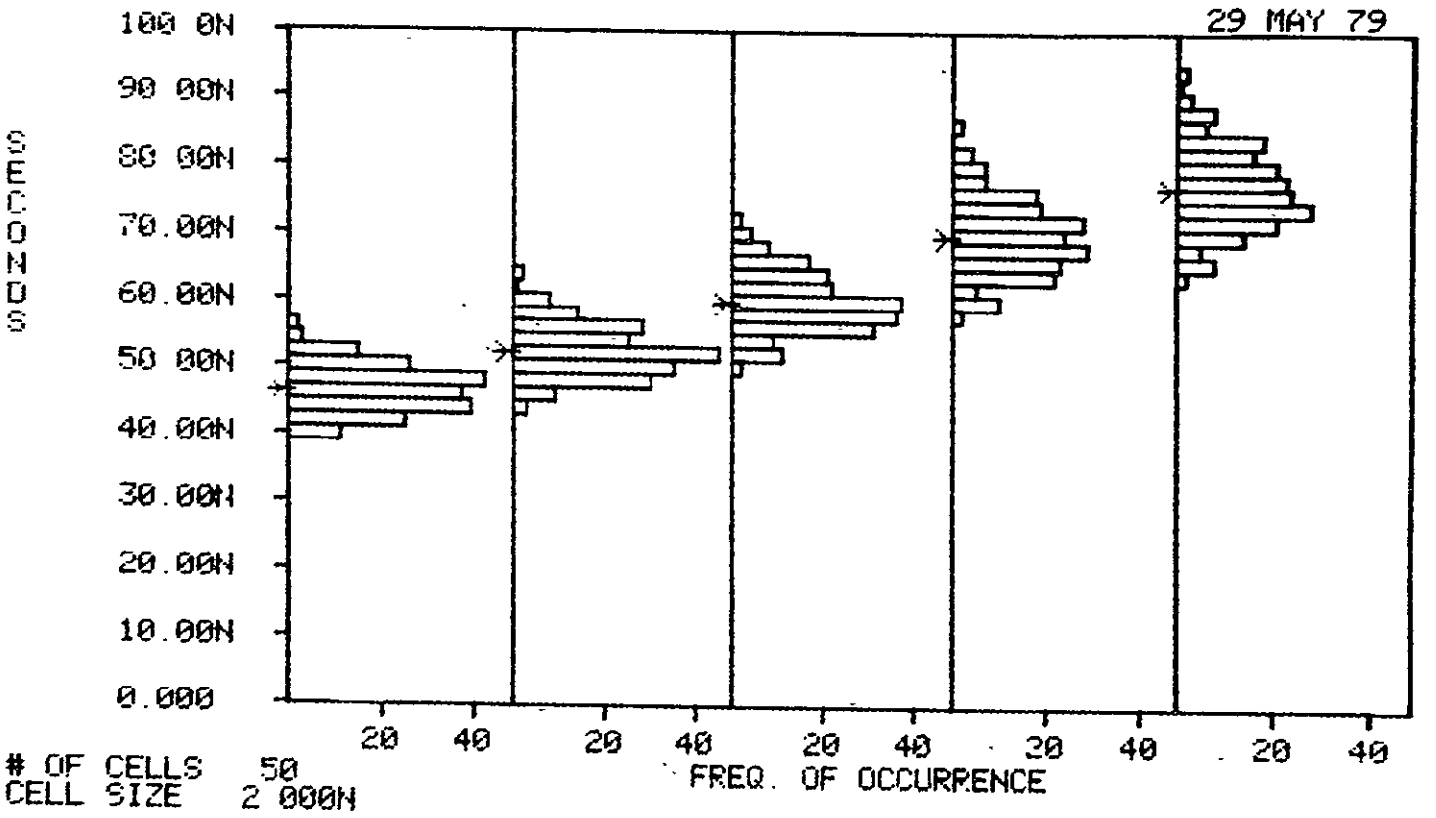
S-3260 DATA FOR TNOH2 TNOH. VDD=10V



OF CELLS 50
CELL SIZE 2.000N

READINGS:	200	200	200	200	200
MAXIMUM:	40.00N	46 00N	54.00N	64.00N	73.00N
MEAN.	33.98N	38.33N	44.35N	52.58N	58.84N
MINIMUM:	27.00N	30.00N	35 00N	40.00N	45.00N
STD DEV.	3.102N	3.626N	4.406N	5 413N	6.294N

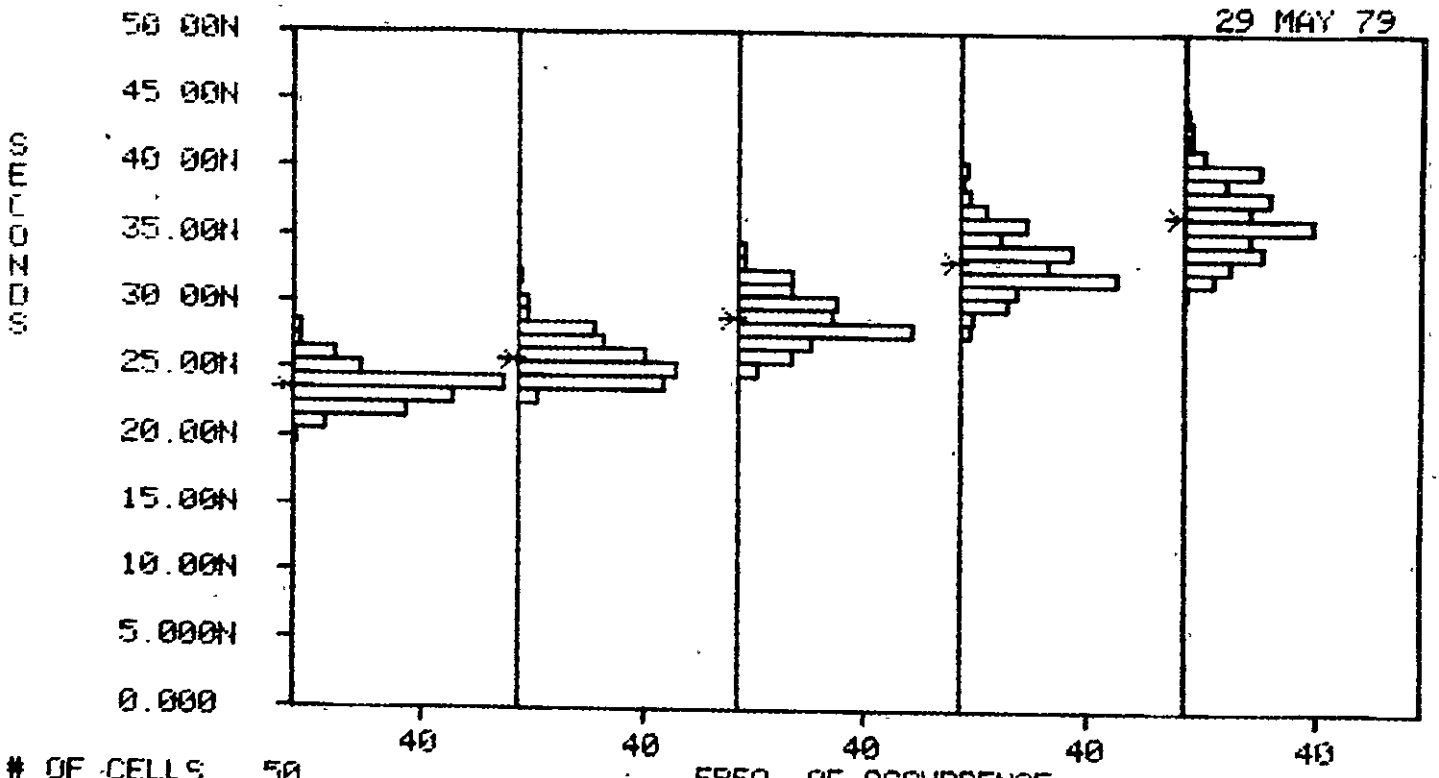
S-3260 DATA FOR THOL1 TNOL: VDD=5V



OF CELLS 50
CELL SIZE 2 000N

READINGS:	200	200	200	200	200
MAXIMUM:	56.00N	64 00N	72.00N	85 00N	94.00N
MEAN:	46.05N	51.99N	59.54N	69.59N	76.78N
MINIMUM:	39 00N	44.00N	50.00N	58 00N	64.00N
STD DEV.:	3.441N	3.884N	4.538N	5.519N	6.158N

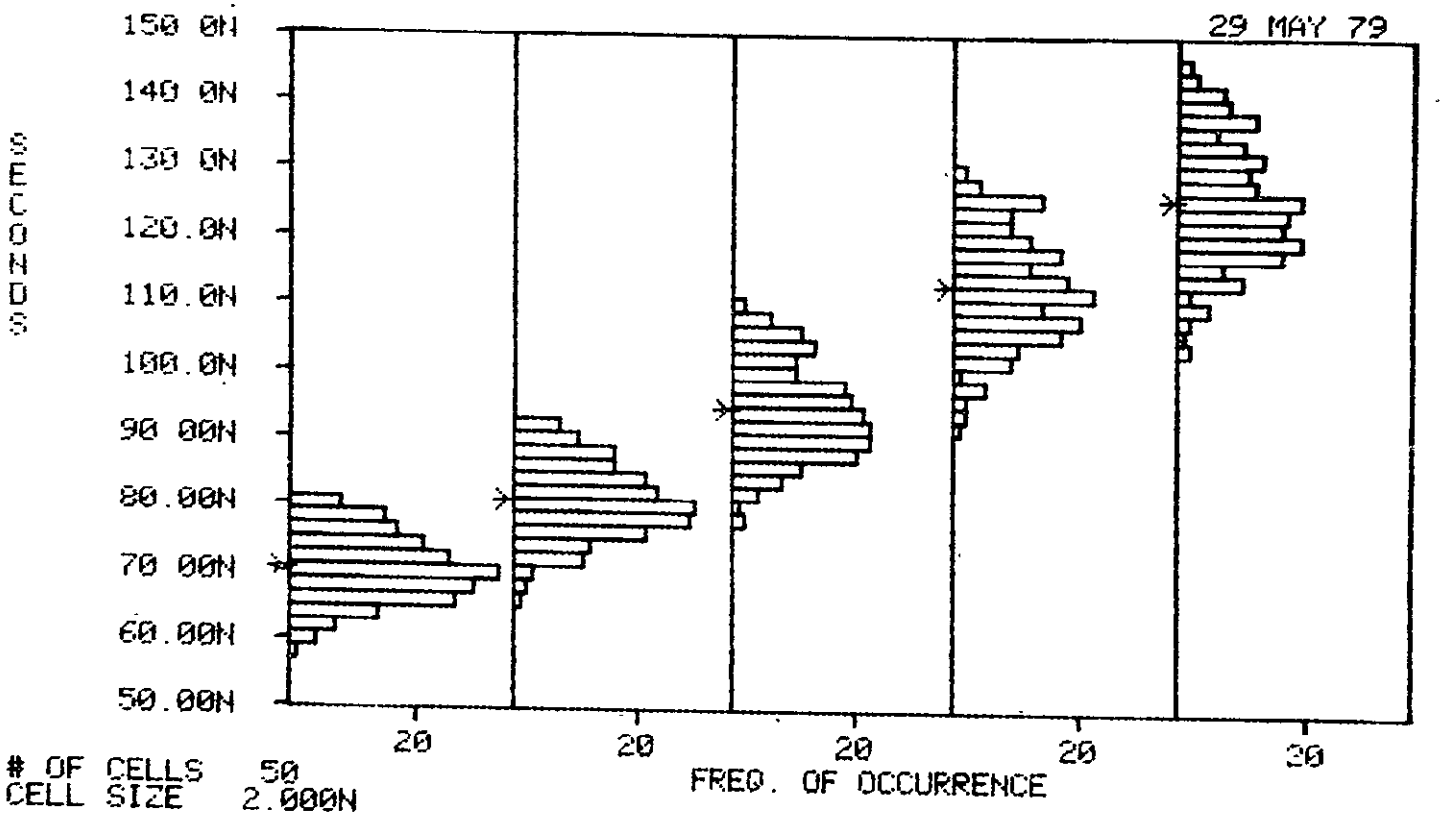
S-3260 DATA FOR TNOL2 TNOL: VDD=10V



OF CELLS 50
CELL SIZE 1.000N

READINGS:	200	200	200	200	200
MAXIMUM	28.00N	32.00N	34.00N	40.00N	44.00N
MEAN:	23.54N	25.71N	28.79N	33.15N	36.58N
MINIMUM	20.00N	23.00N	25.00N	28.00N	31.00N
STD.DEV.	1.374N	1.593N	1.904N	2.245N	2.591N

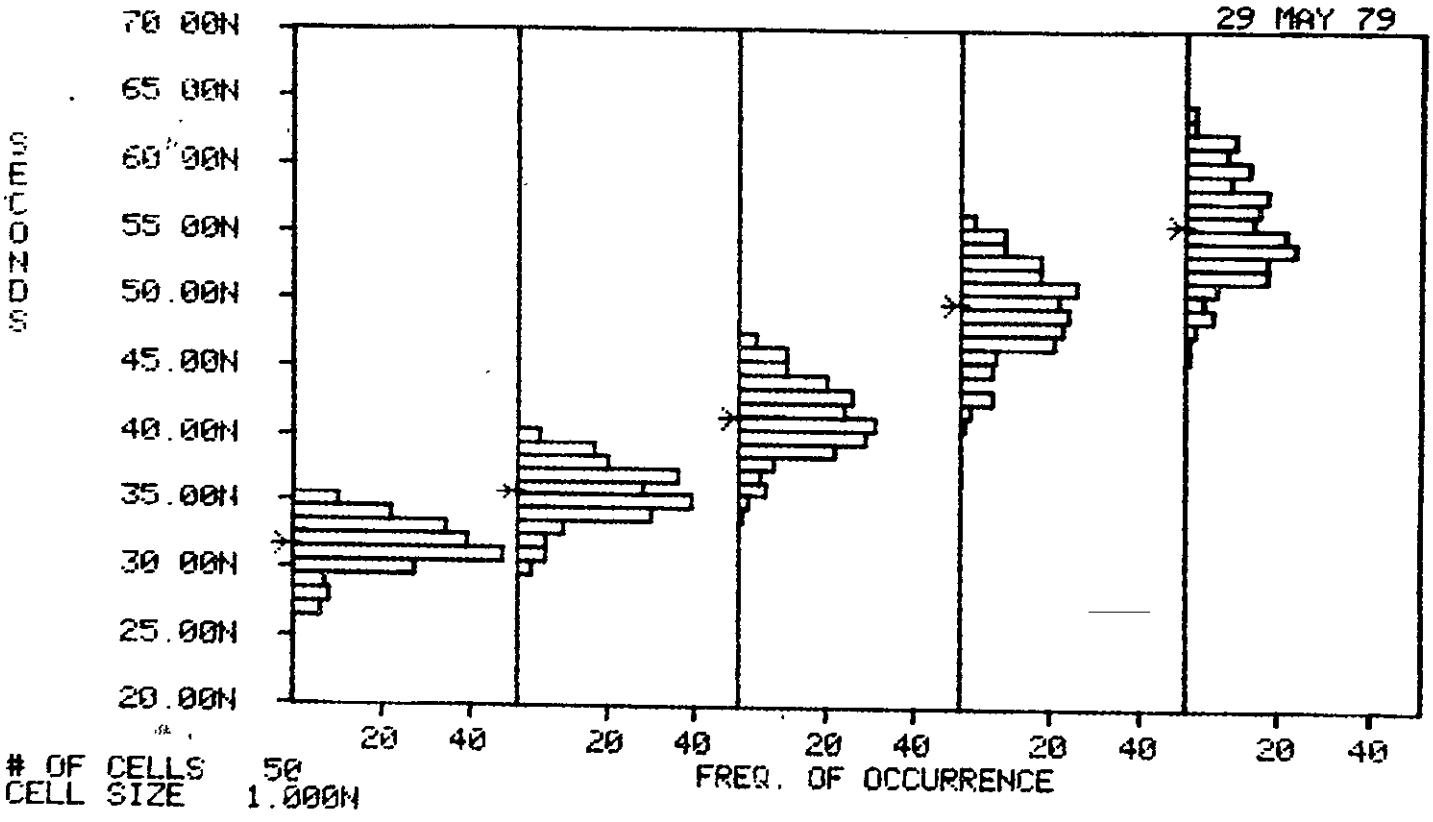
5-3260 DATA FOR TH01 TA0: VDD=5V



OF CELLS 50
CELL SIZE 2.000N

READINGS:	200	200	200	200	200
MAXIMUM:	80.05N	91.75N	109.5N	129.5N	146.0N
MEAN:	70 36N	80.77N	94 51N	112.9N	125.9N
MINIMUM	58.10N	66.35N	77 10N	91.35N	103.0N
STD.DEV..	4 870N	5.644N	6 939N	8.208N	9 175N

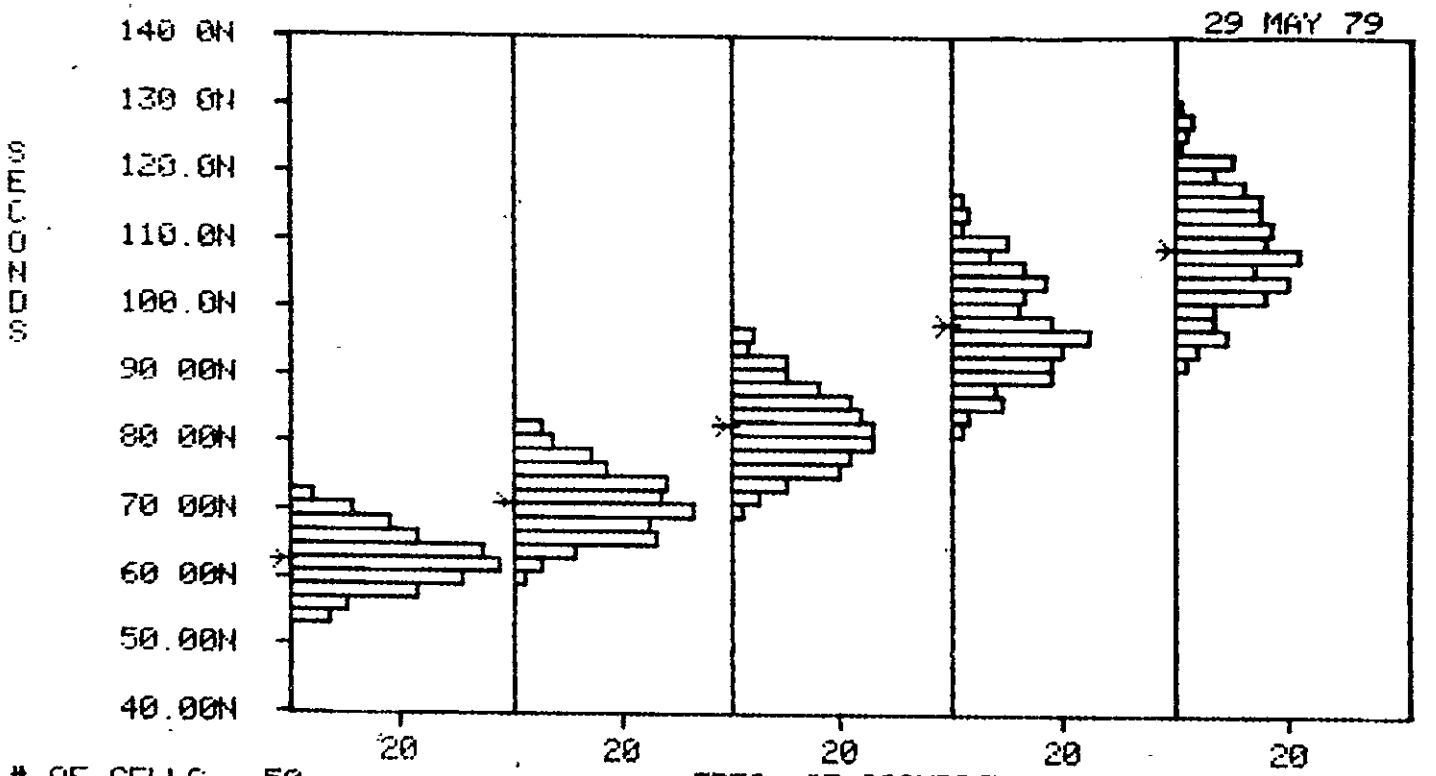
S-3260 DATA FOR TA02 TA0: VDD=10V



OF CELLS 50
CELL SIZE 1.000N

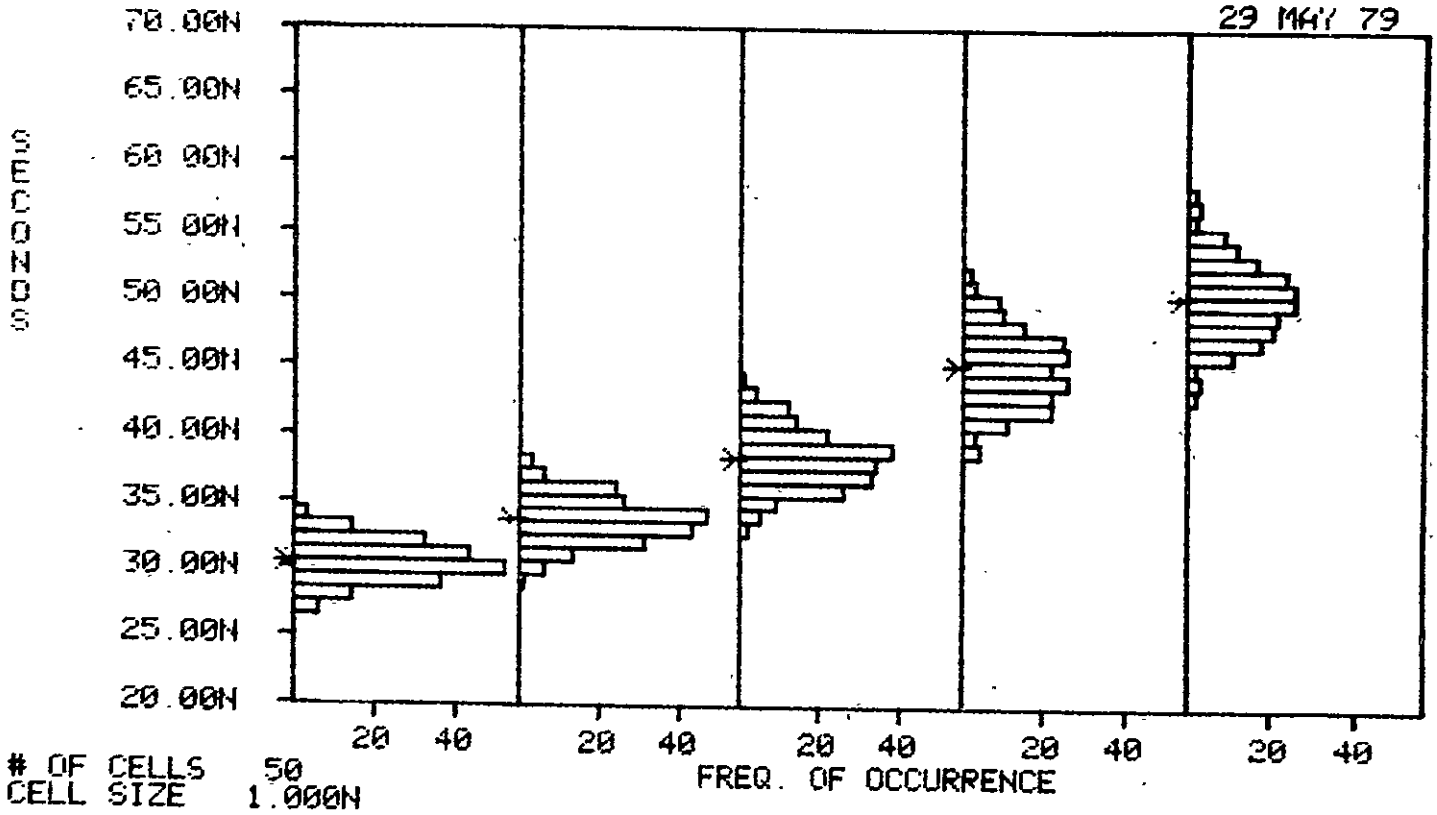
READINGS:	200	200	200	200	200
MAXIMUM:	35.25N	39.85N	47.40N	56.15N	63.90N
MEAN:	31.60N	35.67N	41.44N	49.71N	55.71N
MINIMUM:	26.60N	29.85N	34.35N	40.90N	46.25N
STD DEV:	1.801N	2.115N	2.634N	3.092N	3.660N

S-3260 DATA FOR TB01 TB0: VDD=5V



READINGS:	200	200	200	200	200
MAXIMUM:	72.25N	82.85N	96.25N	115.5N	129.0N
MEAN:	62.55N	71.10N	82.44N	97.57N	109.1N
MINIMUM:	53.30N	60.80N	69.95N	82.75N	91.80N
STD.DEV.:	4.124N	4.855N	5.660N	7.229N	7.996N

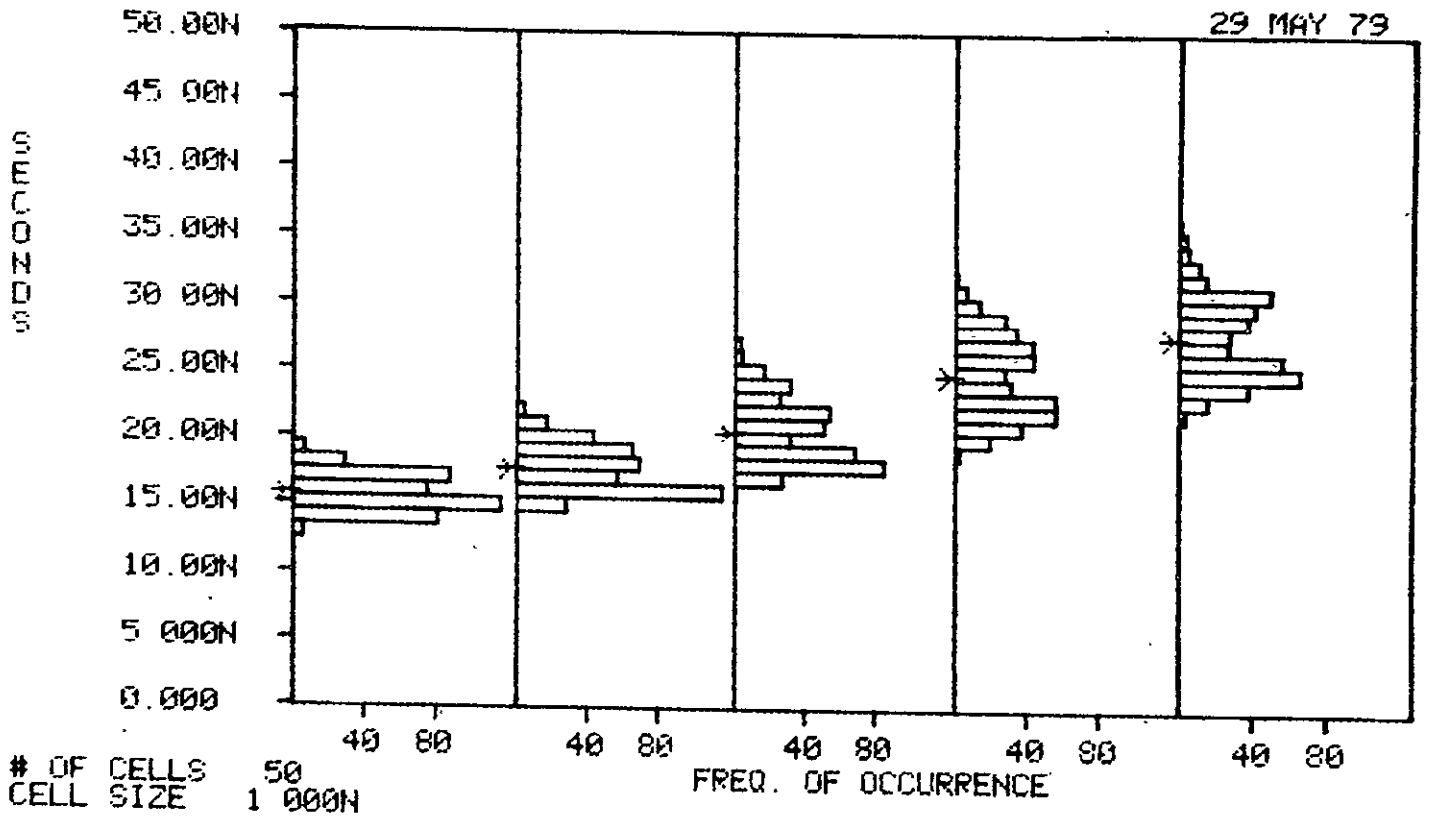
S-3260 DATA FOR TB02 TB0: VDD=10V



OF CELLS 50
CELL SIZE 1.000N

READINGS:	200	200	200	200	200
MAXIMUM:	34.15N	38.15N	43.35N	52.05N	58.25N
MEAN:	30.36N	33.64N	38.25N	45.07N	50.27N
MINIMUM:	26.60N	29.40N	33.30N	38.70N	42.95N
STD.DEV	1.490N	1.721N	2.084N	2.799N	2.949N

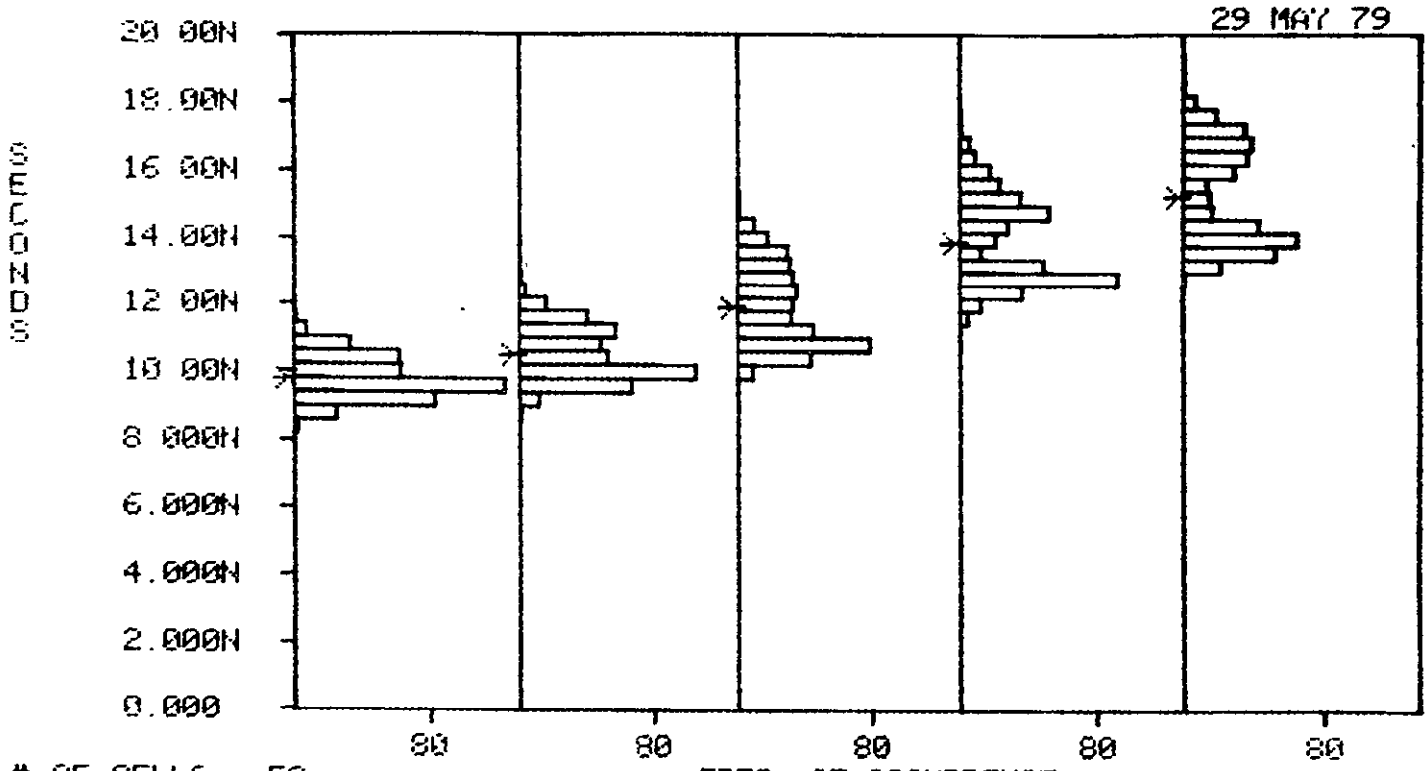
S-3260 DATA FOR TT1 TTLH/TTHL: VDD=5V



OF CELLS 50
CELL SIZE 1.000N

READINGS	400	400	400	400	400
MAXIMUM	19.30N	22.20N	27.15N	31.50N	35.50N
MEAN	15.68N	17.59N	20.41N	24.71N	27.62N
MINIMUM	13.20N	14.50N	16.40N	19.20N	22.10N
STD.DEV	1.286N	1.687N	2.385N	2.913N	2.935N

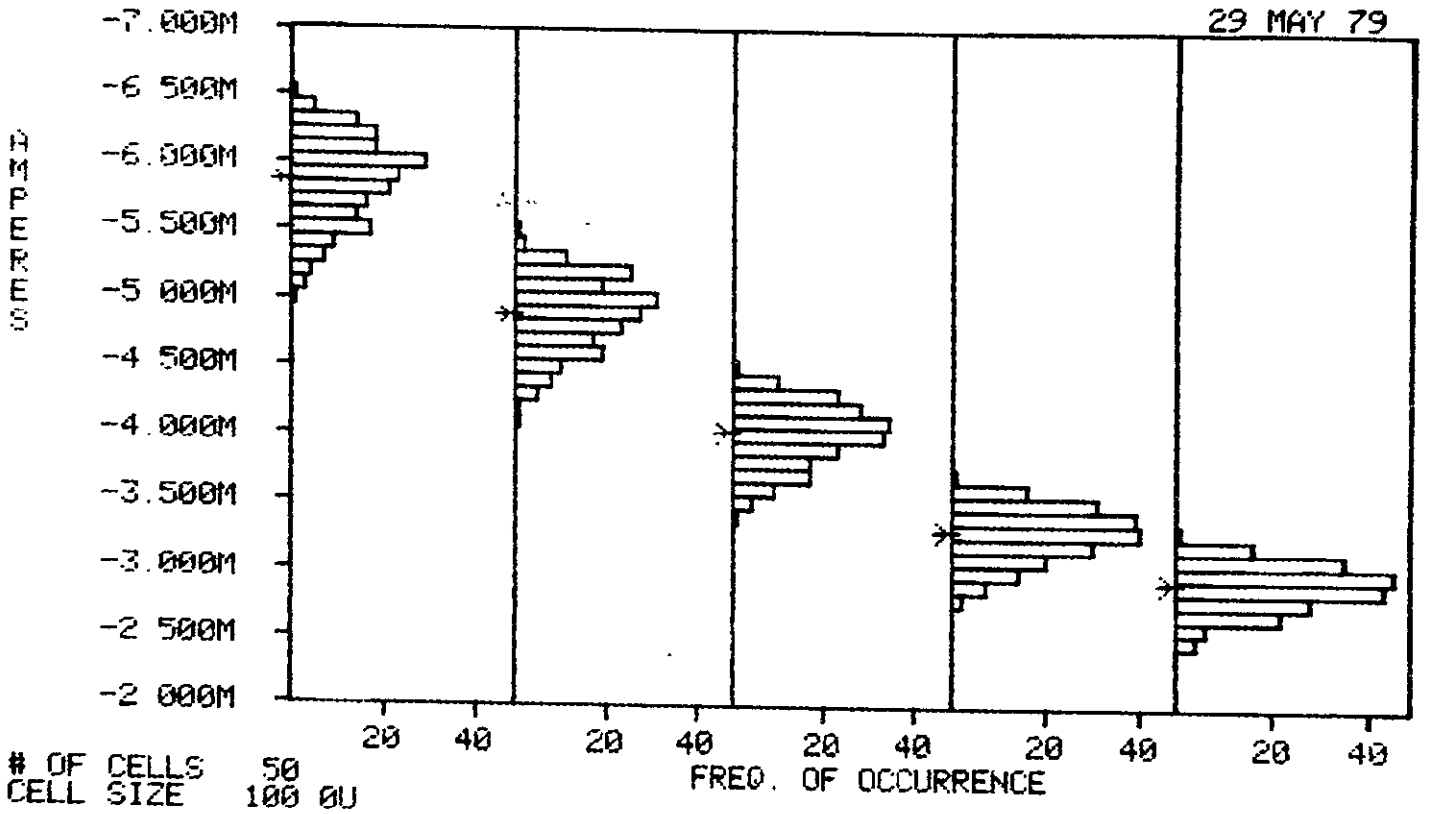
S-3350 DATA FOR TT2 TTLH/TTHL: VDD=10V



OF CELLS 50
CELL SIZE 400.0P

READINGS:	400	400	400	400	400
MAXIMUM	11.55N	12.95N	15.10N	17.70N	19.05N
MEAN:	9.748N	10.47N	11.88N	13.90N	15.26N
MINIMUM:	8.400N	8.950N	9.900N	11.40N	13.00N
STD DEV :	579.0P	764.1P	1.198N	1.290N	1.469N

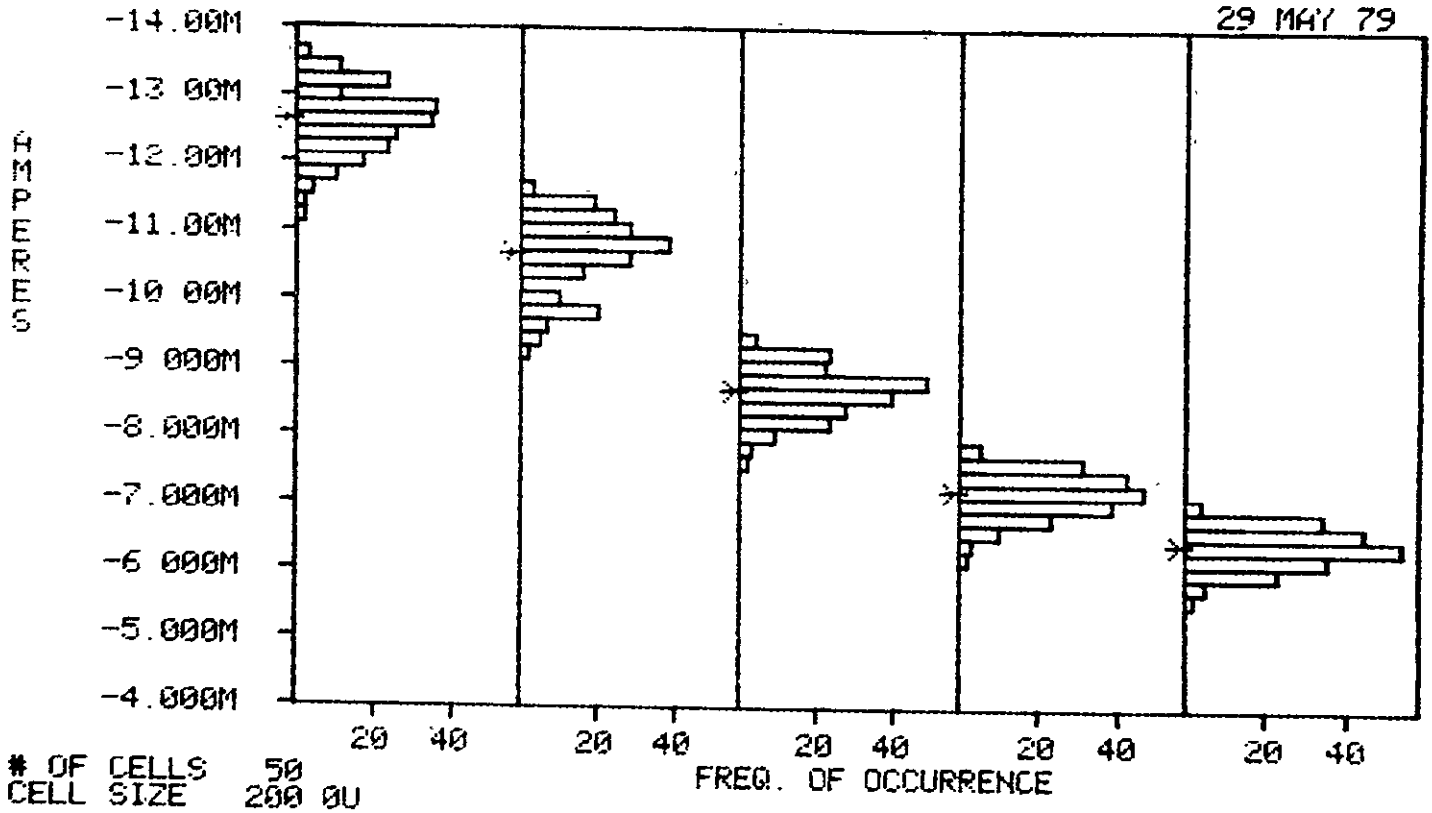
S-3260 DATA FOR IOH1 IOH. VDD=5V VO=4.6V



OF CELLS 50
CELL SIZE 100.0U

READINGS:	200	200	200	200	200
MAXIMUM:	-4.980M	-4.150M	-3.420M	-2.800M	-2.480M
MEAN:	-5.852M	-4.884M	-4.023M	-3.303M	-2.932M
MINIMUM:	-6.540M	-5.475M	-4.480M	-3.710M	-3.280M
STD.DEV..	318.1U	273.4U	230.6U	187.1U	165.7U

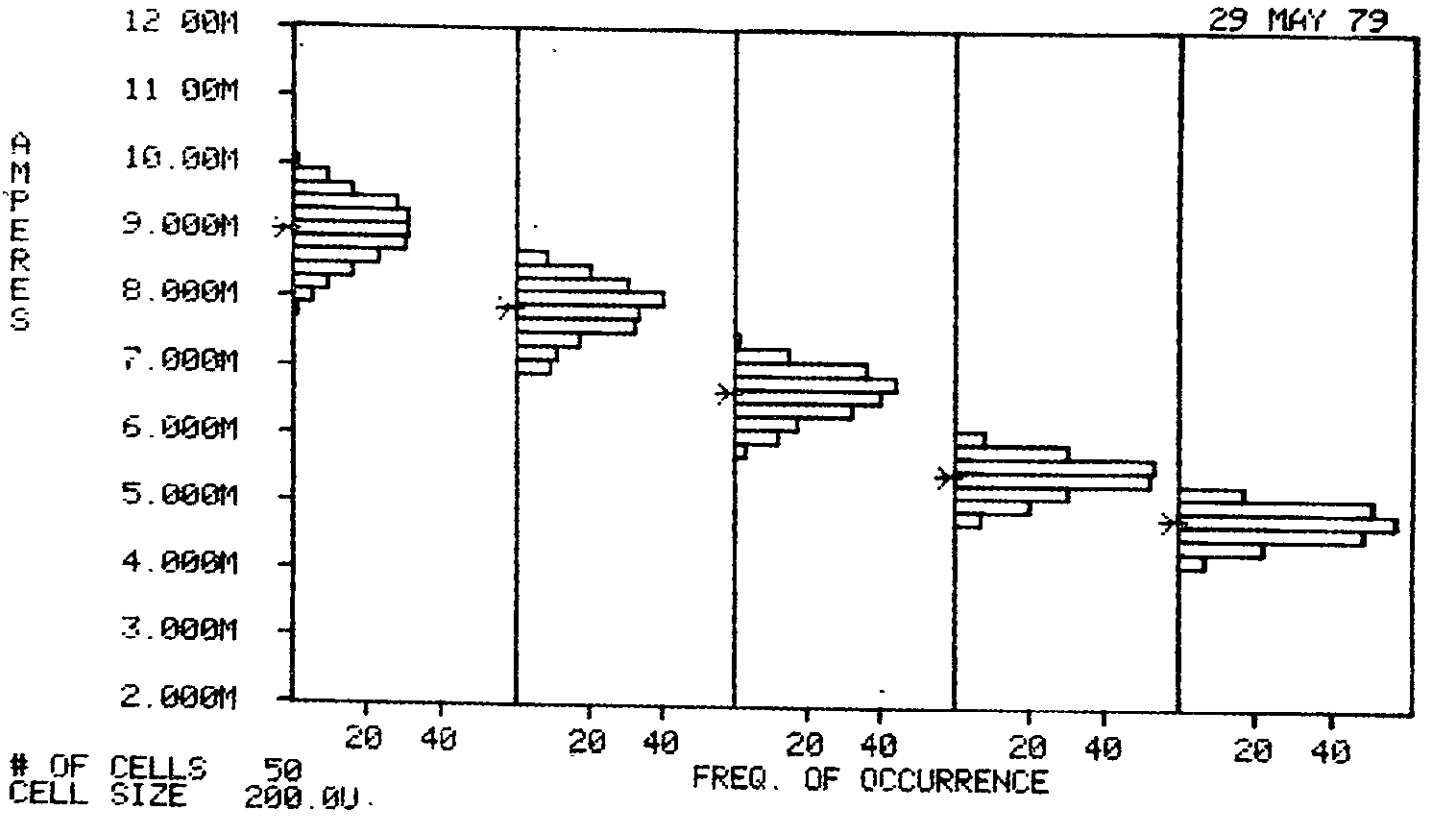
S-3260 DATA FOR IOH3 IOH: VDD=10V VO=9 5V



OF CELLS 50
CELL SIZE 200 0U

READINGS:	200	200	200	200	200
MAXIMUM:	-11 25M	-9 150M	-7.620M	-6.290M	-5.600M
MEAN:	-12.59M	-10 67M	-8.659M	-7 191M	-6.416M
MINIMUM:	-13 60M	-11 70M	-9.375M	-7.870M	-7.030M
STD.DEV.:	490 8U	574.4U	365.6U	311.8U	282.7U

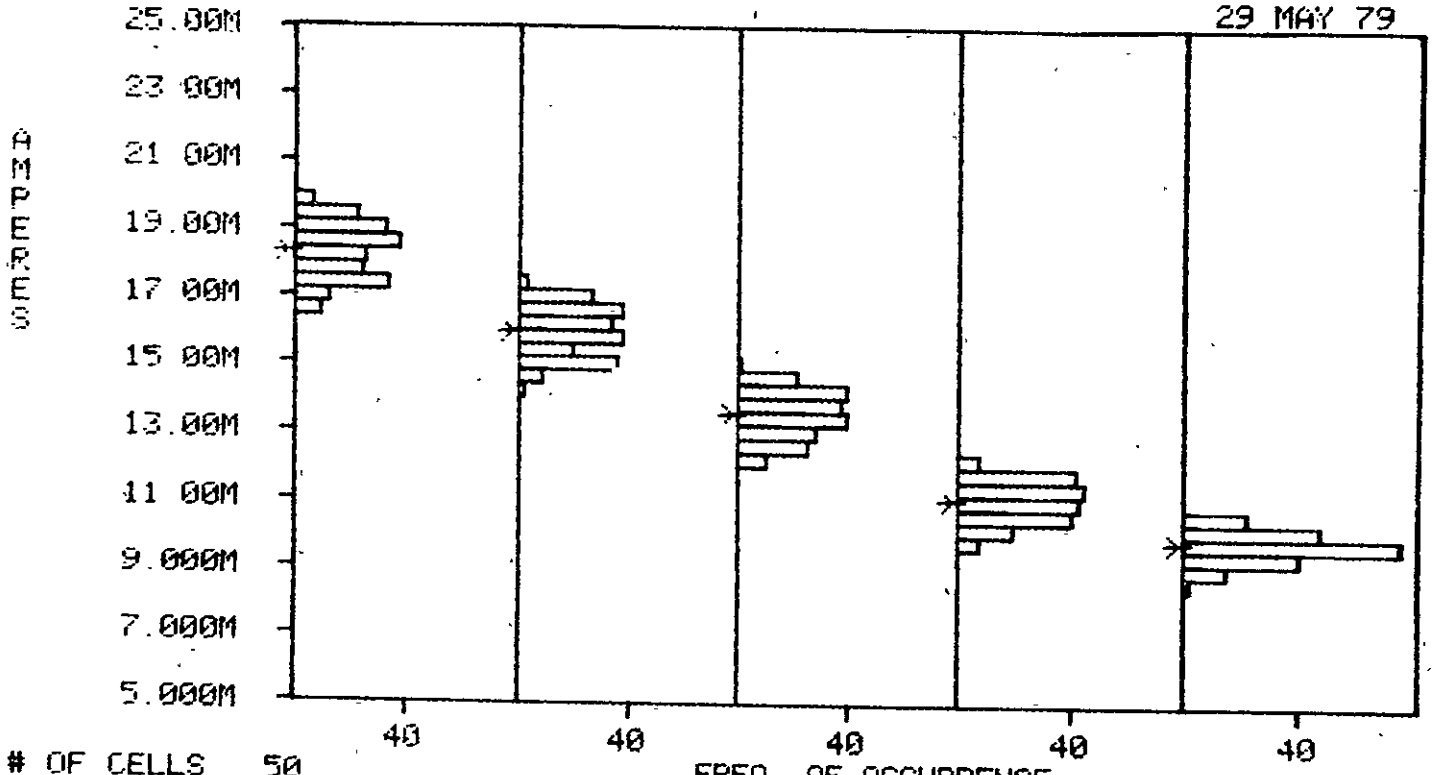
S-3260 DATA FOR IOL1 IOL: VDD=5V VO=0 4V



OF CELLS 50
CELL SIZE 200.0U.

READINGS:	200	200	200	200	200
MAXIMUM:	9.900M	8.630M	7.300M	5.980M	5.260M
MEAN:	8.981M	7.847M	6.648M	5.441M	4.783M
MINIMUM:	7.850M	6.900M	5.795M	4.705M	4.120M
STD.DEV.:	455.5U	398.0U	341.8U	284.8U	251.9U

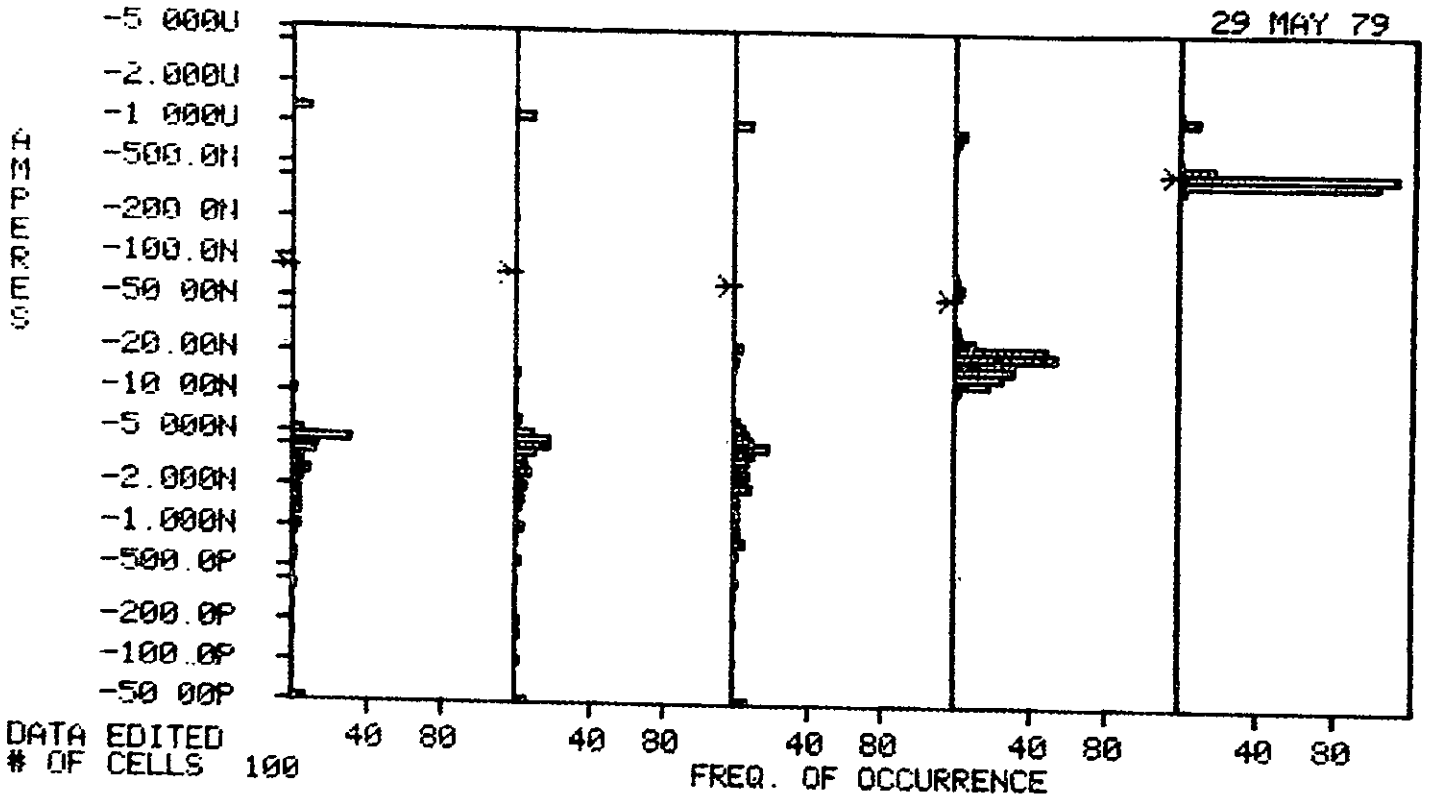
S-3250 DATA FOR IOL3 IOL: VDD=10V VO=0.5V



OF CELLS 50
CELL SIZE 400.0U

READINGS:	200	200	200	200	200
MAXIMUM:	19.80M	17.40M	14.80M	12.15M	10.70M
MEAN:	18.29M	15.98M	13.54M	11.09M	9.838M
MINIMUM:	16.50M	14.30M	12.00M	9.800M	8.725M
STD DEV:	826.3U	757.5U	672.3U	564.9U	441.5U

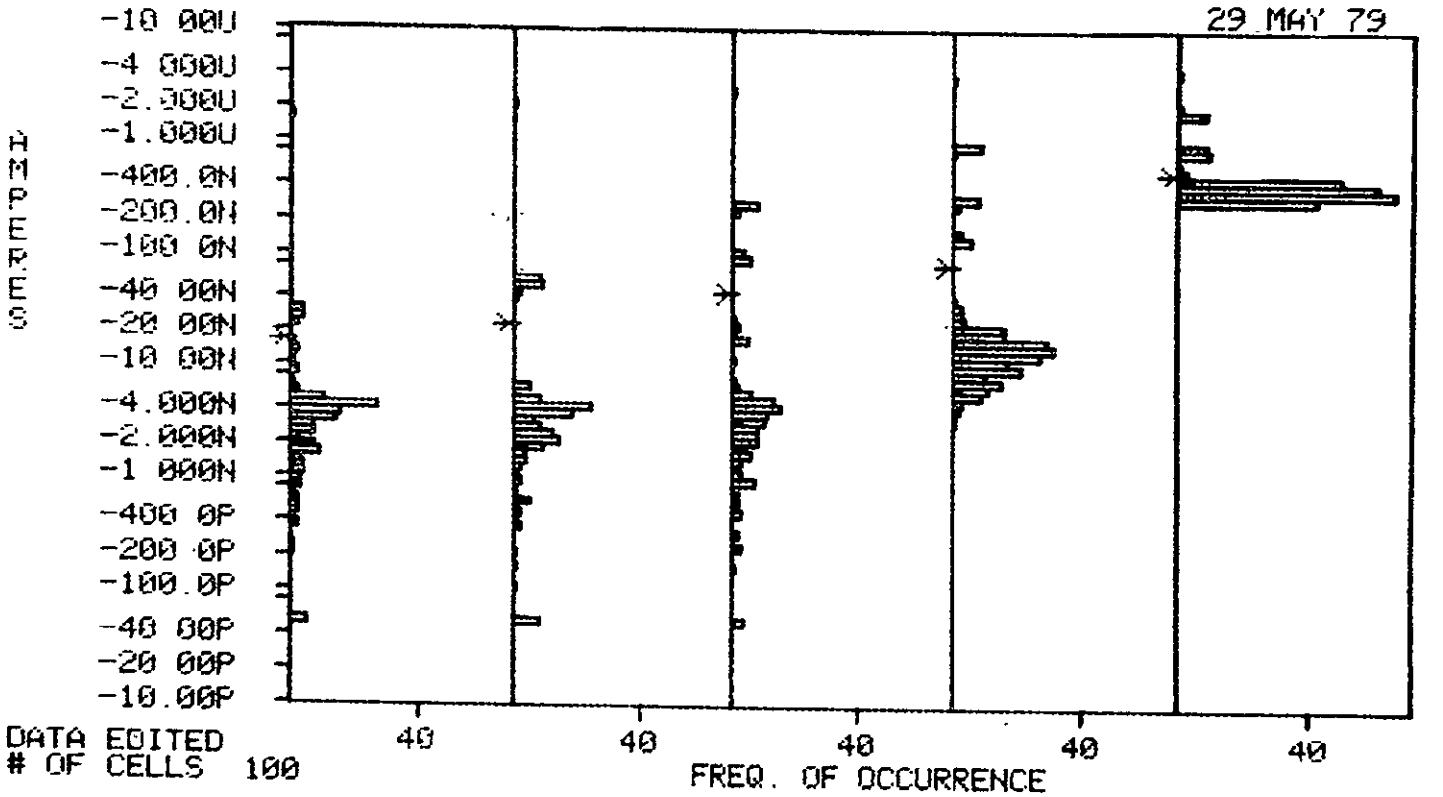
S-3260 DATA FOR ISS ISS: VDD=15V



READINGS:	145	137	145	243	243
MAXIMUM:	-50.00P	-50.00P	-50.00P	-9.450N	-365.5N
MEAN:	-82.29N	-77.69N	-65.29N	-53.30N	-457.3N
MINIMUM:	-1.280U	-1.120U	-960.0N	-855.0N	-1.300U
STD.DEV.:	307.1N	276.5N	231.7N	161.2N	154.4N

RCA CDH1853D

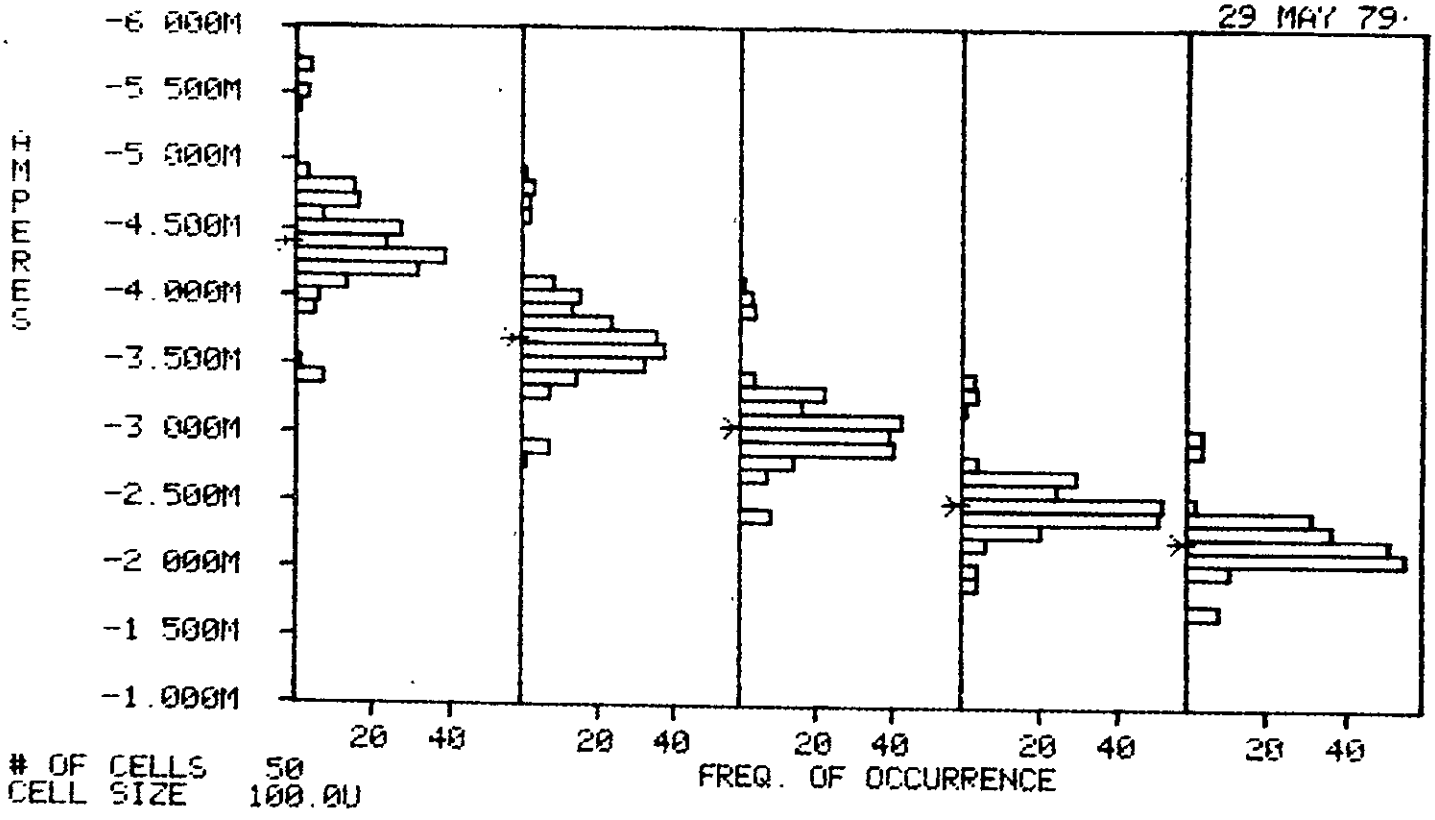
S-3260 DATA FOR ISS ISS: VDD=15V



DATA EDITED
OF CELLS 100

READINGS:	152	162	156	250	250
MAXIMUM	-50.00P	-50.00P	-50 00P	-3.150N	-314.5N
MEAN:	-16.07N	-22.84N	-44.71N	-81.10N	-518.5N
MINIMUM:	-1.705U	-2.220U	-2.850U	-3.655U	-4.655U
STD.DEV.:	138.1N	174.5N	335.4N	292.2N	430.2N

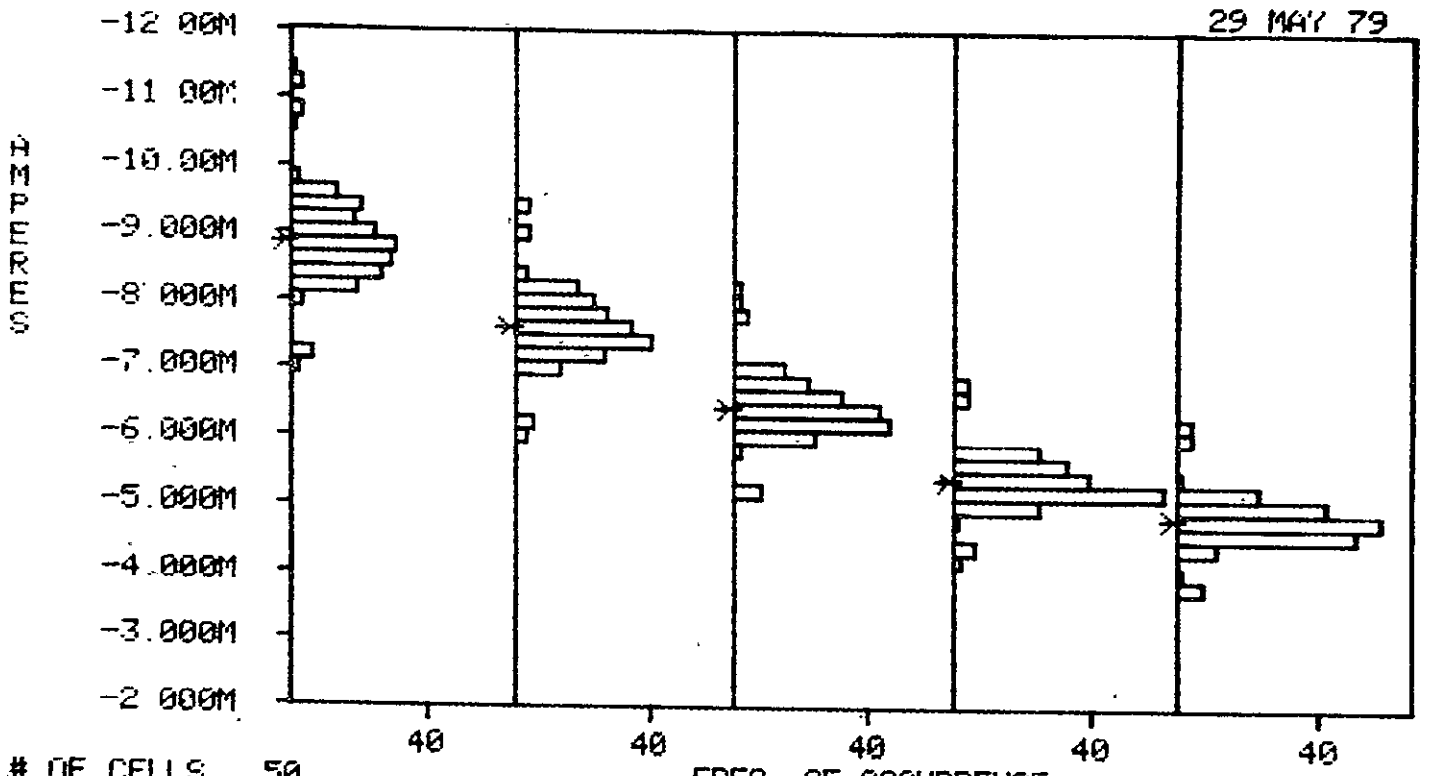
S-3260 DATA FOR IOH1 IOH VDD=5V VO=4.6V



OF CELLS 50
CELL SIZE 100.0U

READINGS:	200	200	200	200	200
MAXIMUM:	-3.410M	-3.845M	-2.355M	-1.930M	-1.715M
MEAN:	-4.394M	-3.682M	-3.045M	-2.502M	-2.224M
MINIMUM:	-5.730M	-4.870M	-4.065M	-3.370M	-3.005M
STD DEV	381.6U	328.7U	277.6U	233.5U	208.2U

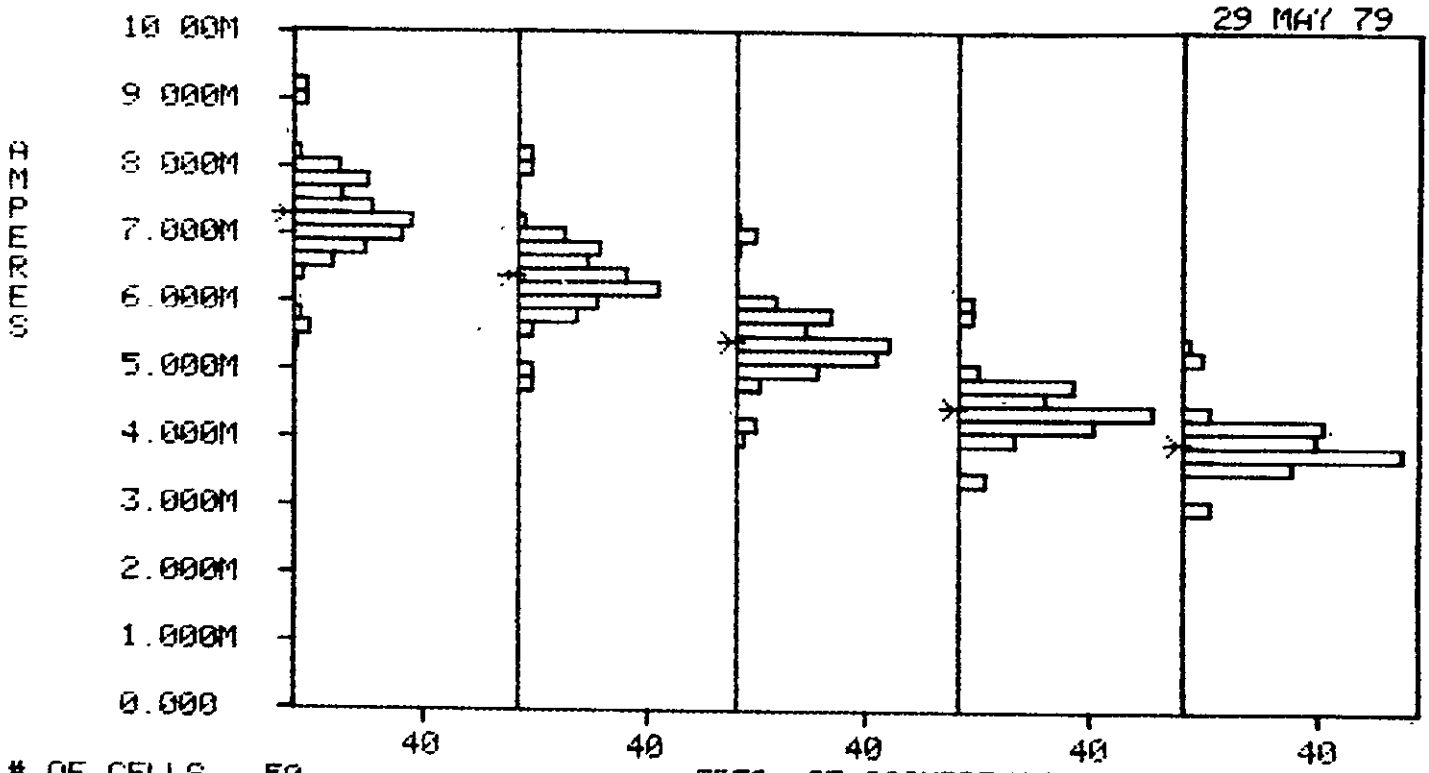
S-3260 DATH FOR IOH3 IOH VDD=10V VO=9.5V



OF CELLS 50
CELL SIZE 200.0U

READINGS:	200	200	200	200	200
MAXIMUM:	-7.040M	-6.080M	-5.140M	-4.275M	-3.840M
MEAN:	-8.839M	-7.604M	-6.428M	-5.380M	-4.827M
MINIMUM:	-11.30M	-9.480M	-8.135M	-6.870M	-6.220M
STD DEV	687.0U	561.7U	488.3U	420.4U	383.5U

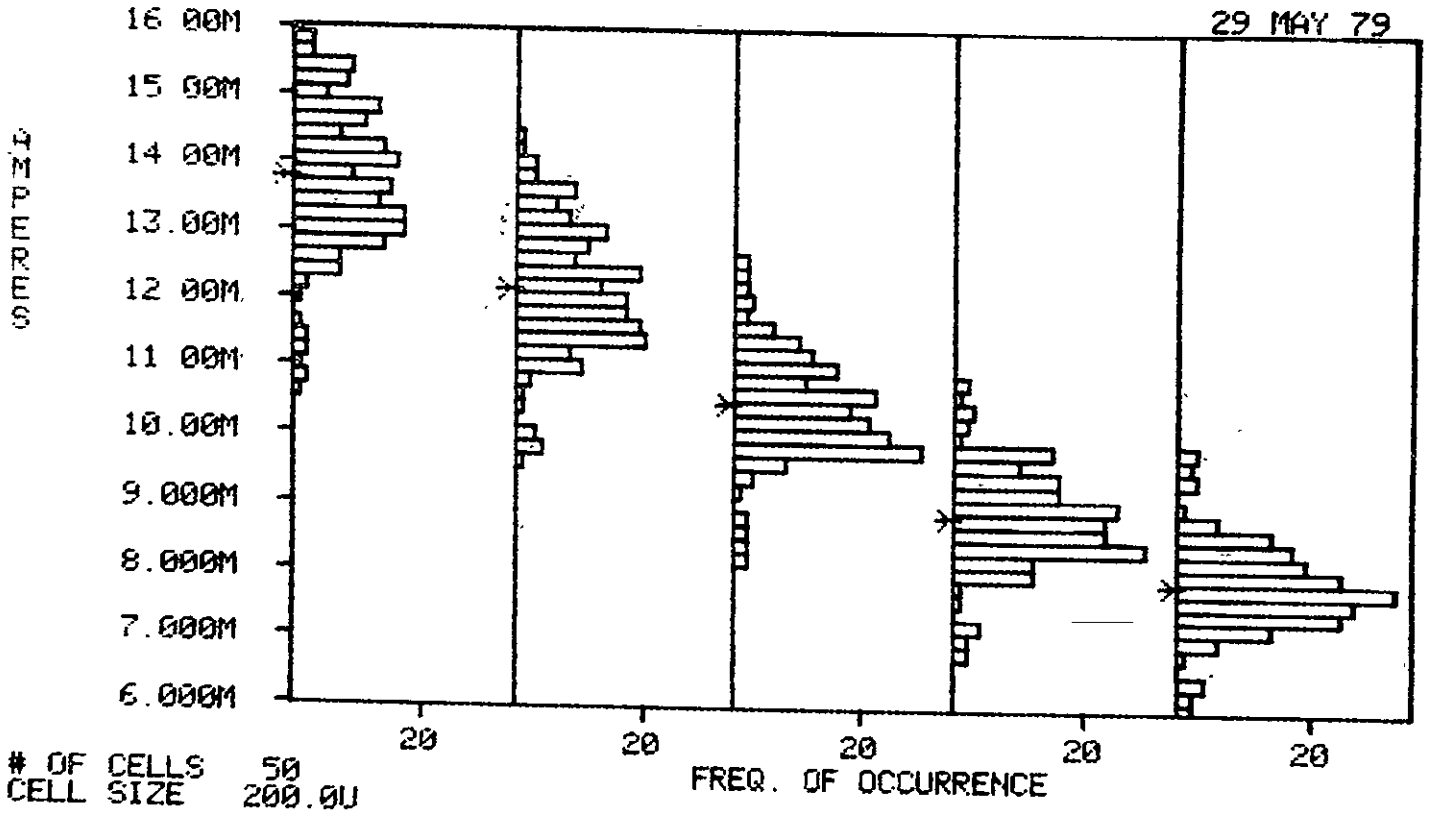
S-3260 DATA FOR IOL1 IOL: VDD=5V VO=0.4V



OF CELLS 50
CELL SIZE 200.0U

READINGS:	200	200	200	200	200
MAXIMUM:	9.280M	8.270M	7.170M	6.040M	5.390M
MEAN:	7.272M	6.370M	5.413M	4.463M	3.934M
MINIMUM	5.435M	4.755M	4.035M	3.340M	3.135M
STD.DEV	642.4U	577.3U	504.8U	431.7U	389.1U

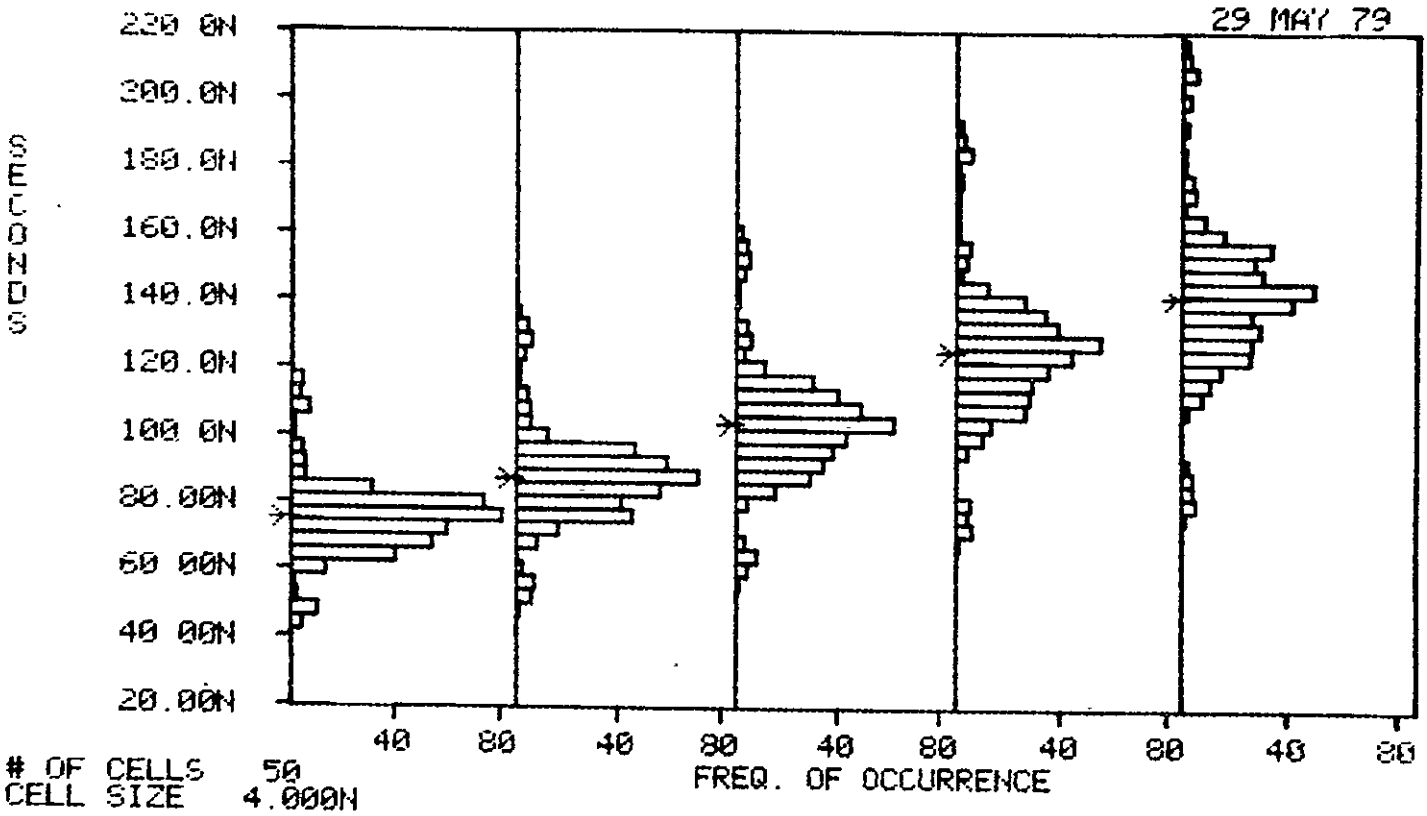
S-3260 DATA FOR IOL3 IOL.. VDD=10V VO=0 5V



OF CELLS 50
CELL SIZE 200.0U

READINGS:	200	200	200	200	200
MAXIMUM:	15.90M	14.35M	12.65M	10.85M	9.850M
MEAN.	13.74M	12.15M	10.46M	8.849M	7.865M
MINIMUM:	10.60M	9.520M	8.145M	6.800M	6.030M
STD DEV.	1.056M	940.5U	791.0U	705.5U	647.7U

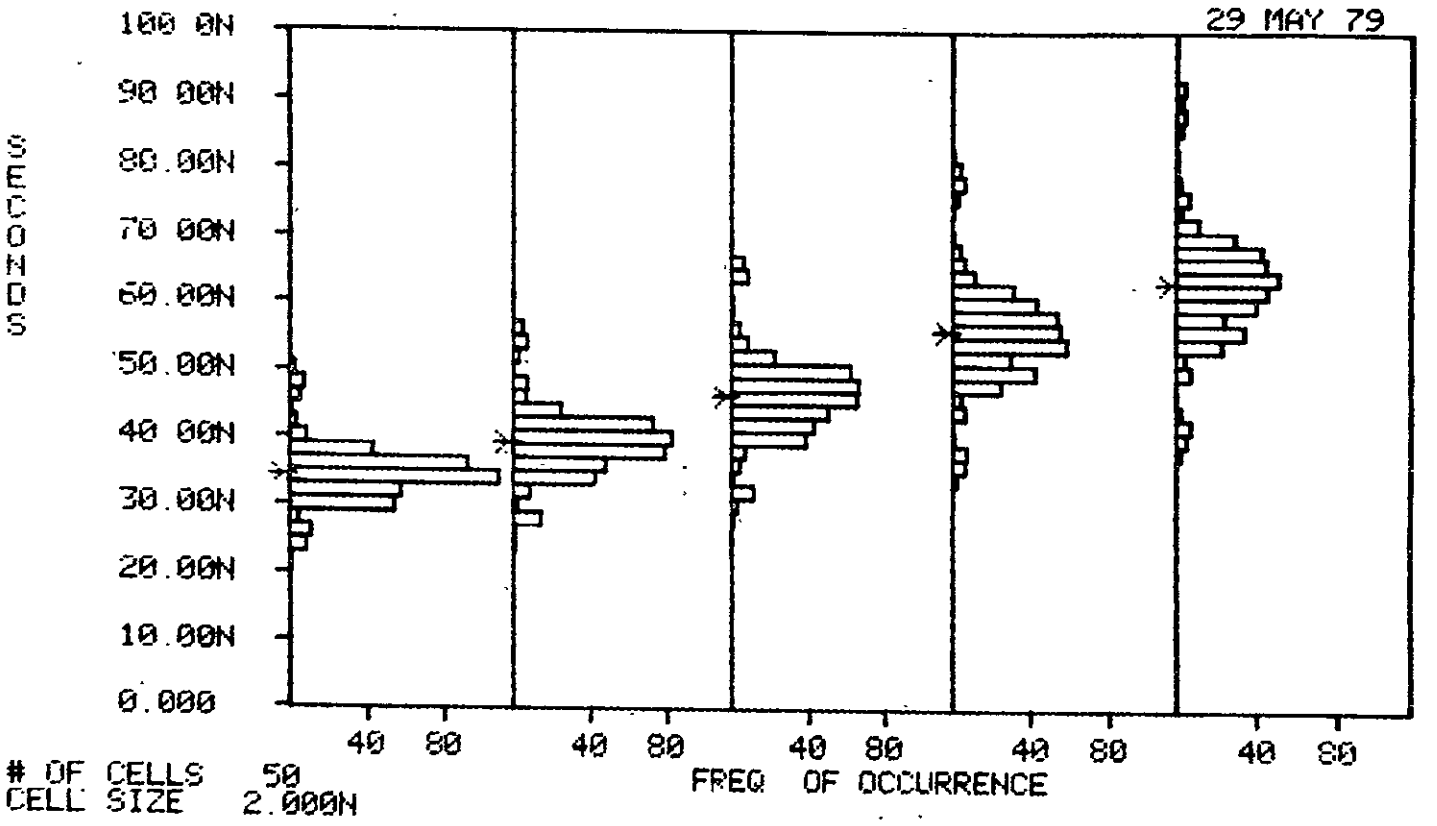
S-3260 DATA FOR TE01 TEOH/TEOL: VDD=5V



OF CELLS 50
CELL SIZE 4.000N

READINGS:	400	400	400	400	400
MAXIMUM:	114.5N	135 0N	160.0N	193.5N	217.5N
MEAN:	74.68N	87 06N	103.4N	125.0N	141.0N
MINIMUM	43 20N	49 70N	57.40N	68.05N	76.35N
STD DEV	11.28N	13 42N	16.20N	19.59N	22 09N

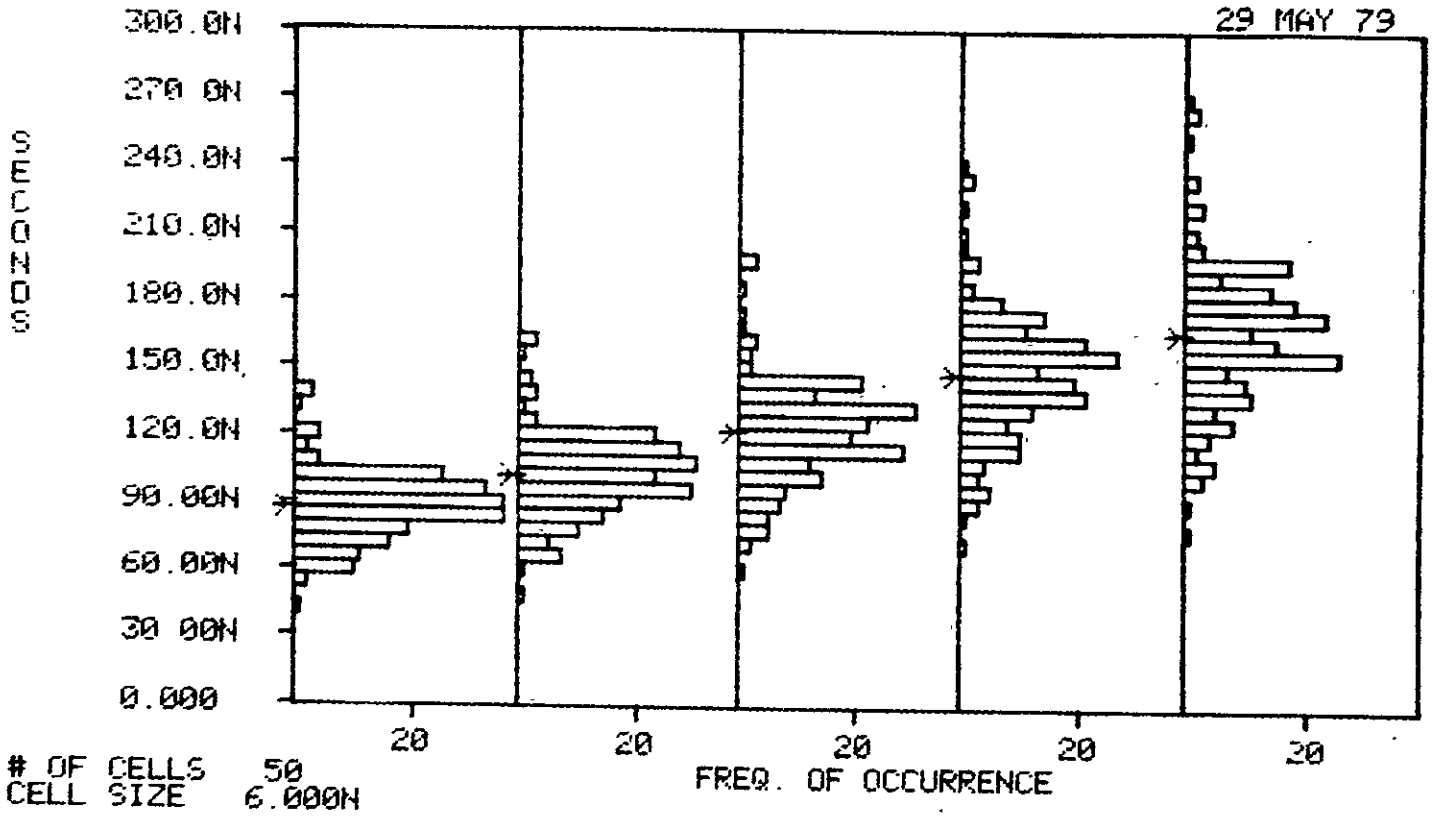
S-3260 DATA FOR TE02 TEOH/TEOL VDD=10V



OF CELLS 50
CELL SIZE 2.000N

READINGS	400	400	400	400	400
MAXIMUM	49.70N	56.70N	66.90N	81.35N	92.70N
MEAN	34.23N	39.12N	46.19N	55.72N	63.07N
MINIMUM	21.60N	24.45N	28.35N	33.40N	37.45N
STD DEV	4.129N	4.872N	6.056N	7.503N	8.658N

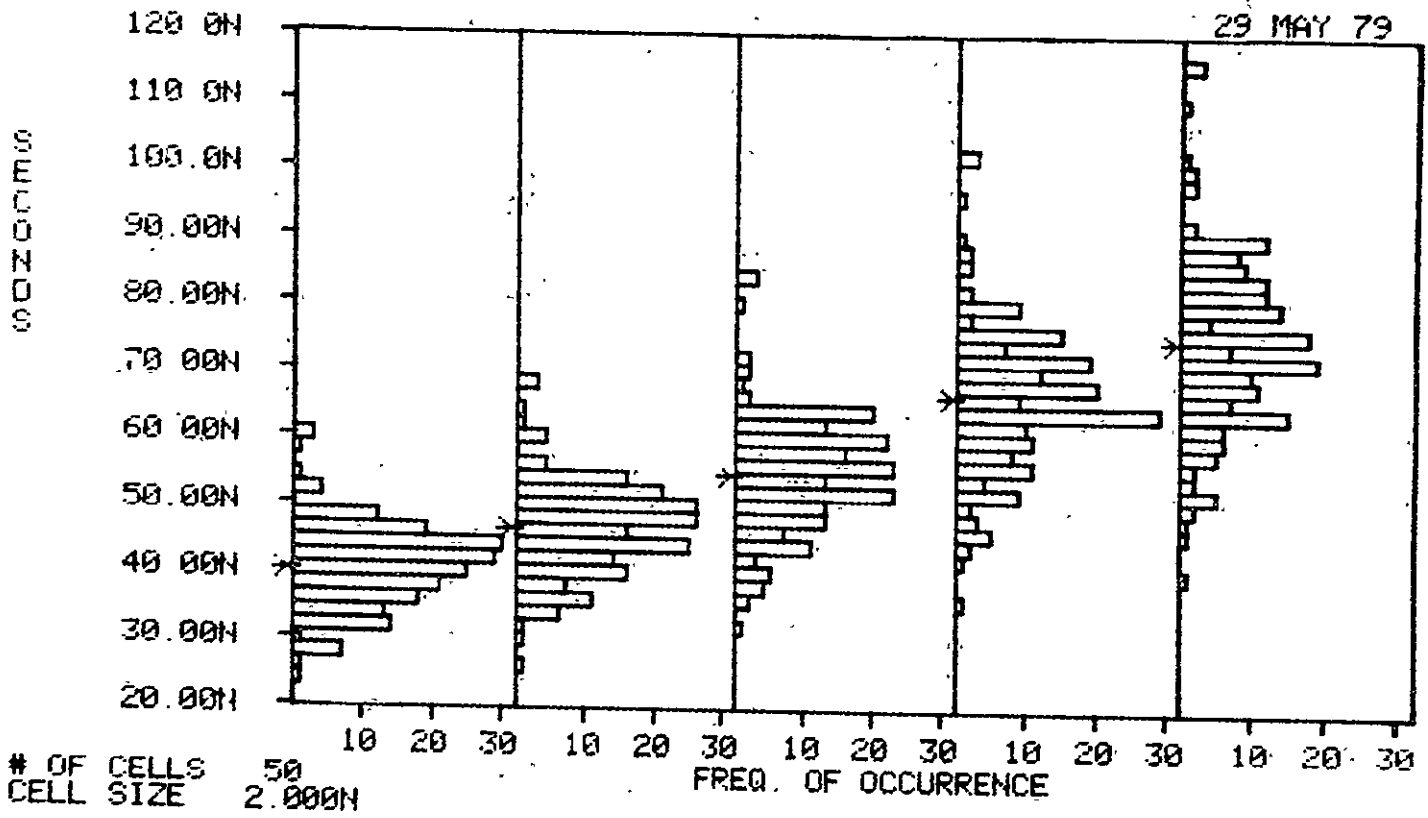
S-3260 DATA FOR TNOH1 TNOH: VDD=5V



OF CELLS 50
CELL SIZE 6.000N

READINGS:	200	200	200	200	200
MAXIMUM	139.0N	165.0N	196.0N	238.0N	268 0N
MEAN:	87.12N	102.2N	121.8N	147.3N	166 0N
MINIMUM:	44.00N	51.00N	59.00N	69.00N	78.00N
STD DEV	15.57N	18.61N	22.50N	27.51N	31.11N

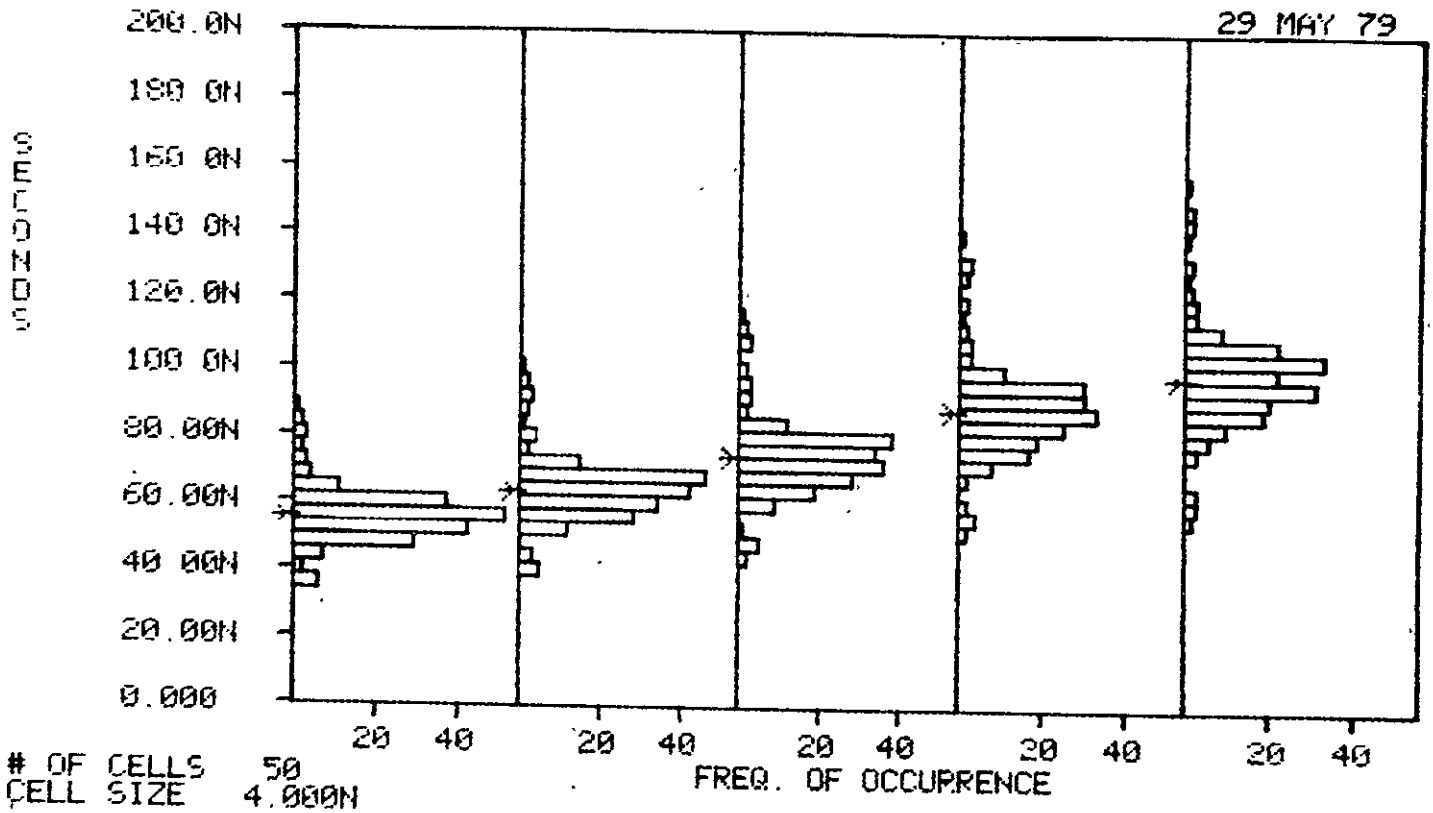
S-3260 DATA FOR TNOH2 TNOH: VDD=10V



OF CELLS 50
CELL SIZE 2.000N

READINGS:	200	200	200	200	200
MAXIMUM:	60.00N	69.00N	83 00N	102.0N	116.0N
MEAN:	40 02N	46.13N	54.59N	66.10N	74.85N
MINIMUM:	24.00N	27.00N	31.00N	36.00N	40.00N
STD DEV.	5.982N	7.020N	8.720N	10.94N	12.64N

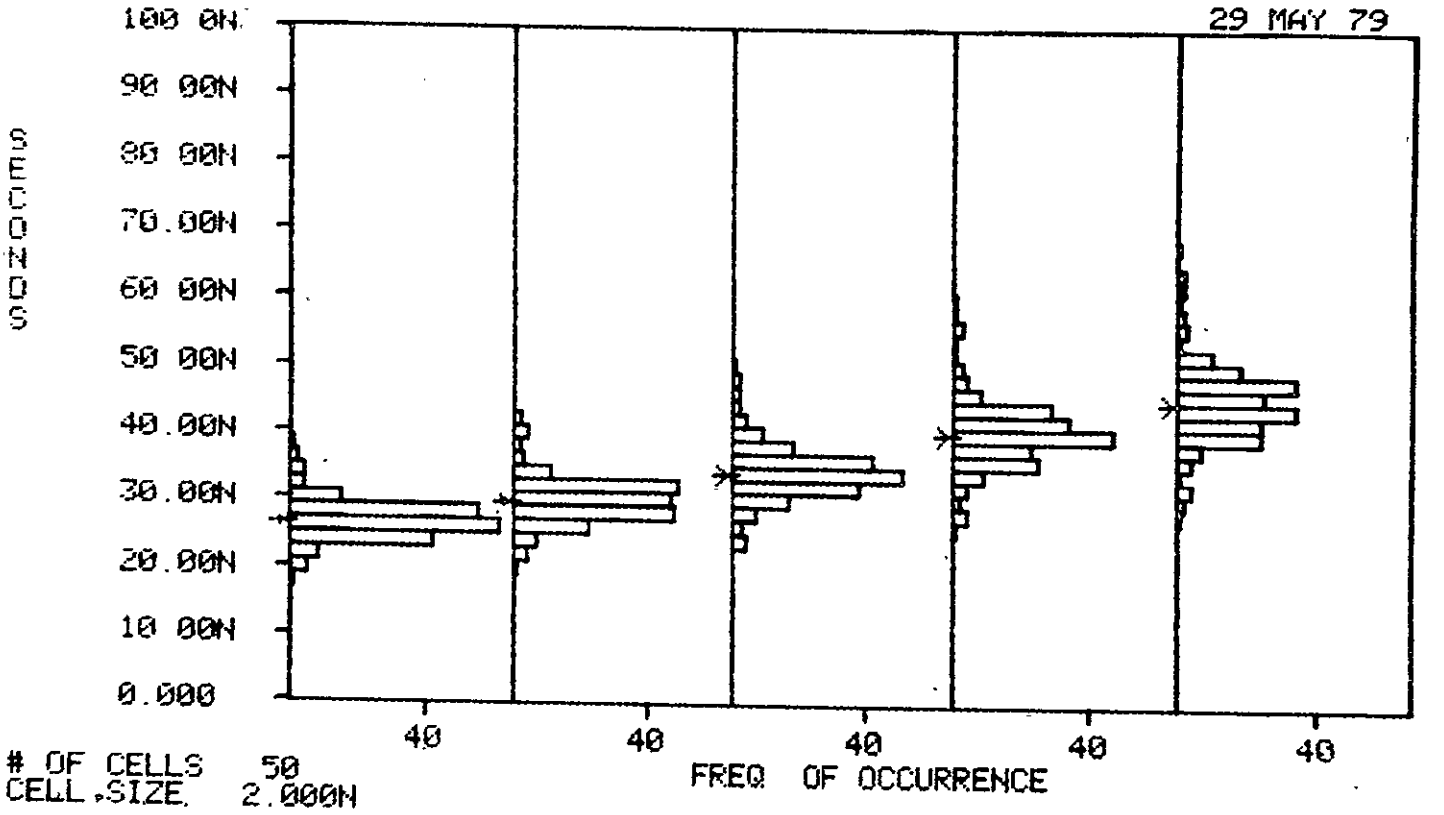
S-3260 DATA FOR TNOL1 TNOL. VDD=5V



OF CELLS 50
CELL SIZE 4.000N

READINGS	200	200	200	200	200
MAXIMUM:	87.00N	100.0N	117.0N	139.0N	155.0N
MEAN:	55.04N	63.34N	74.10N	88.23N	98.56N
MINIMUM:	34.00N	38.00N	43.00N	51.00N	56.00N
STD DEV	8.295N	9.648N	11.36N	13.65N	15.26N

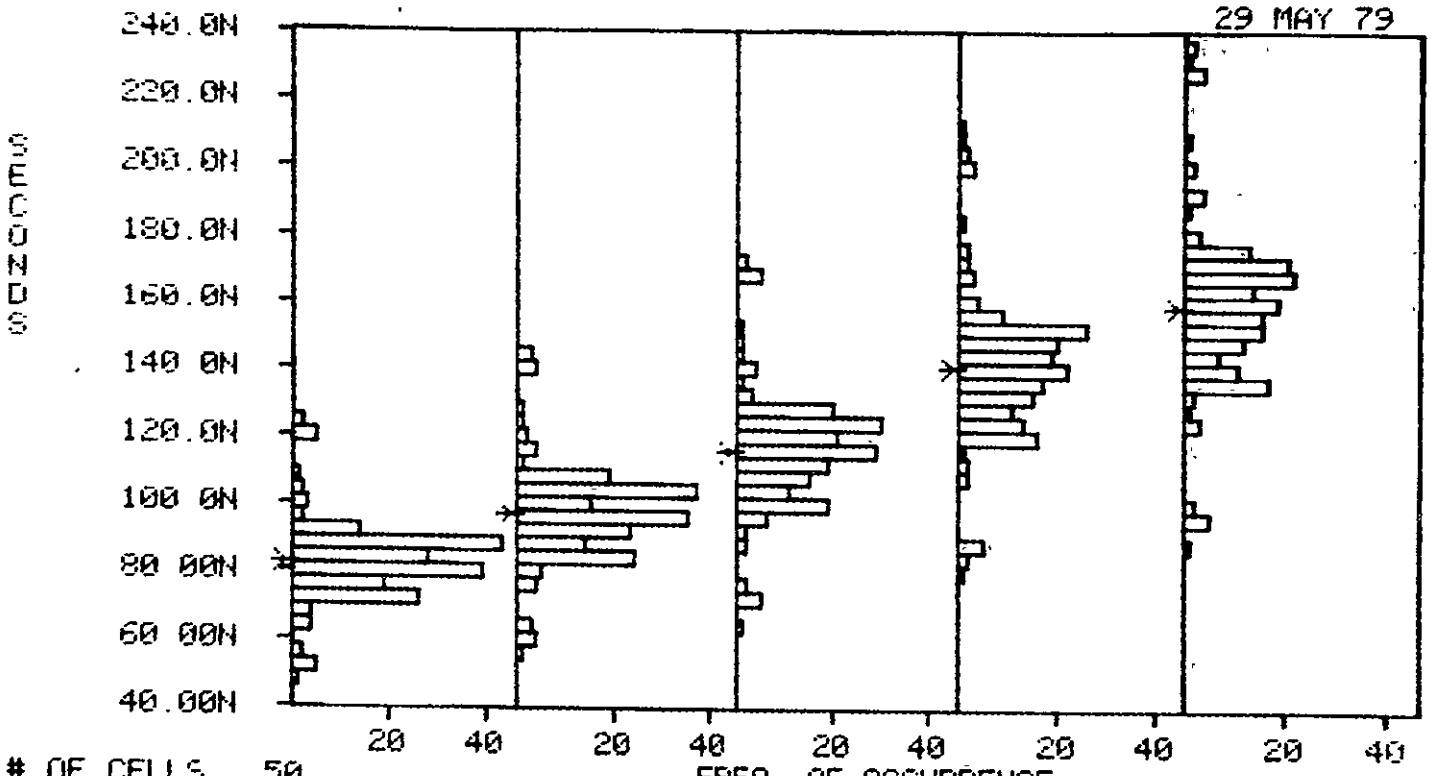
S-3260 DATA FOR TNDL2 TNOL: VDD=10V



OF CELLS 50
CELL SIZE 2.000N

READINGS:	200	200	200	200	200
MAXIMUM:	38 00N	42.00N	50.00N	59.00N	67.00N
MEAN:	26.13N	29.43N	33.93N	40.03N	44.79N
MINIMUM:	18 00N	20.00N	23.00N	26.00N	28.00N
STD DEV.	2 885N	3.468N	4.127N	5.132N	5.904N

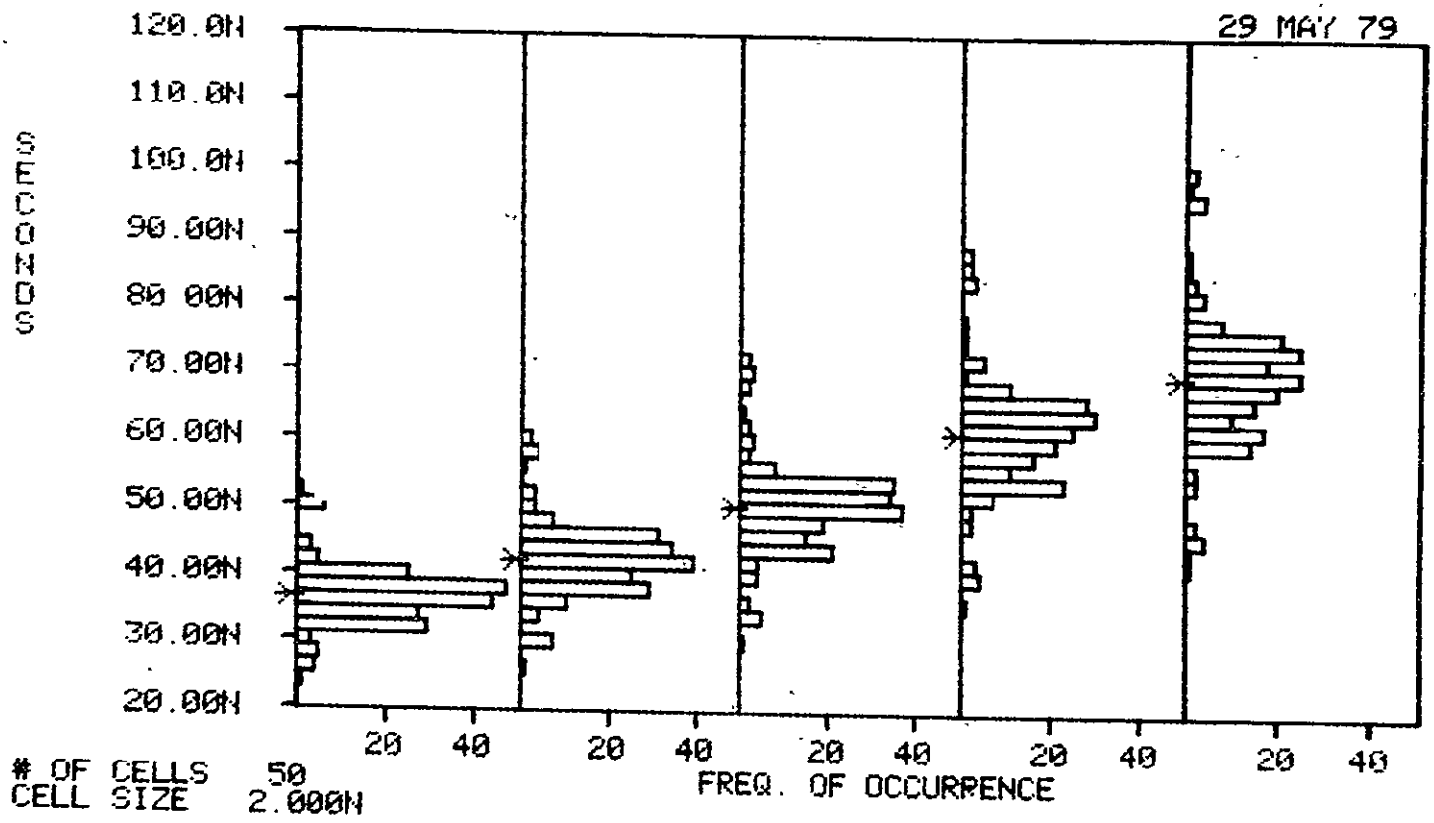
S-3260 DATA FOR TA01 TA0: VDD=5V



OF CELLS 50
CELL SIZE 4.000N

READINGS:	200	200	200	200	200
MAXIMUM	123.5N	145.5N	173.5N	210.5N	236.5N
MEAN	82.21N	96.63N	115.7N	140.4N	158.6N
MINIMUM	48.60N	56.75N	65.55N	78.30N	87.85N
STD.DEV.	11.94N	14.39N	17.31N	21.03N	23.67N

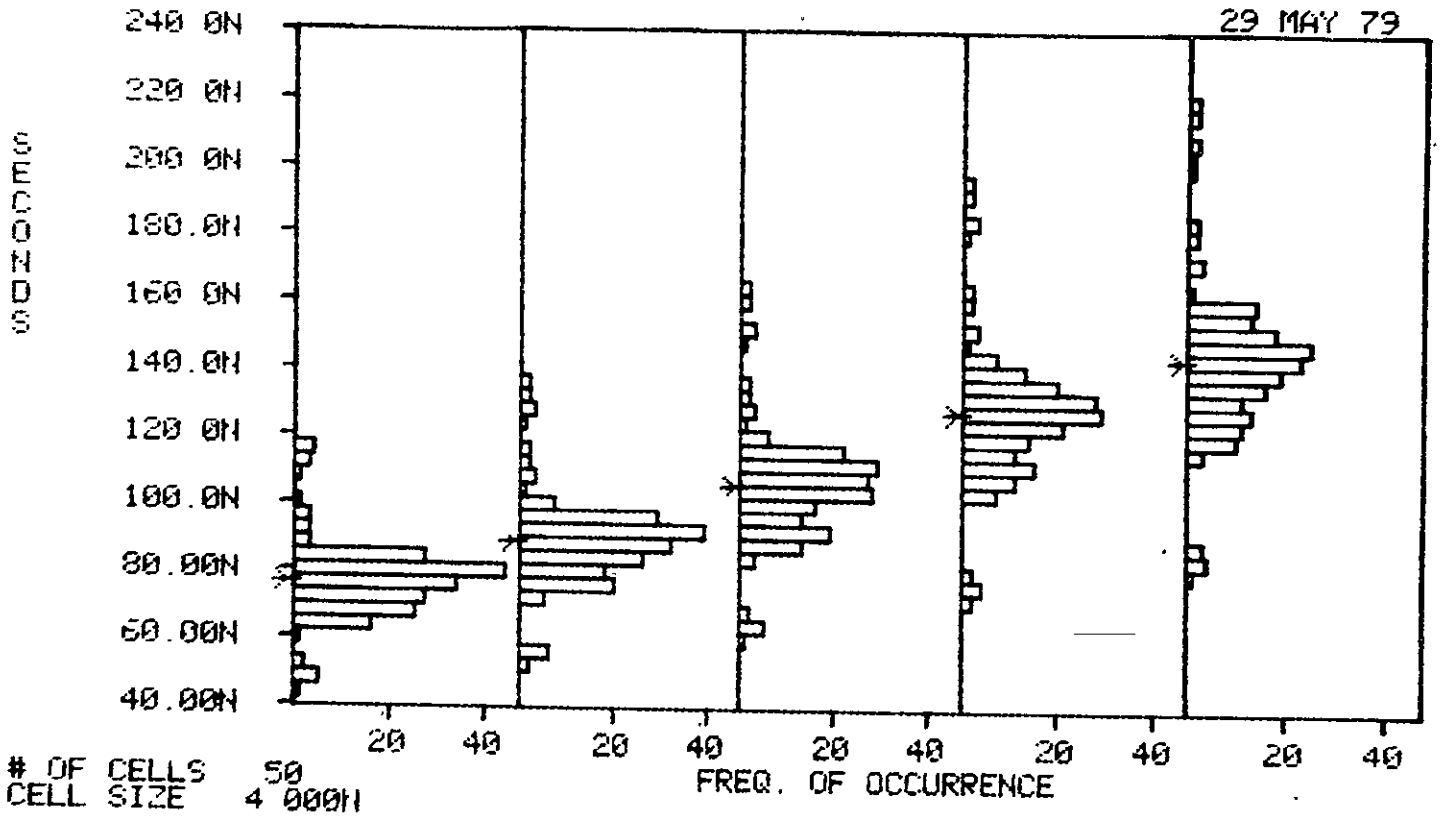
S-3260 DATA FOR TAO2 TAO: VDD=10V



OF CELLS 50
CELL SIZE 2.000N

READINGS:	200	200	200	200	200
MAXIMUM:	51.20N	60.10N	71.70N	88.00N	100.0N
MEAN:	36.37N	42.14N	50.32N	61.23N	69.63N
MINIMUM:	23.45N	26.70N	30.80N	36.60N	41.10N
STD.DEV..	4.369N	5.330N	6.479N	8.175N	9.326N

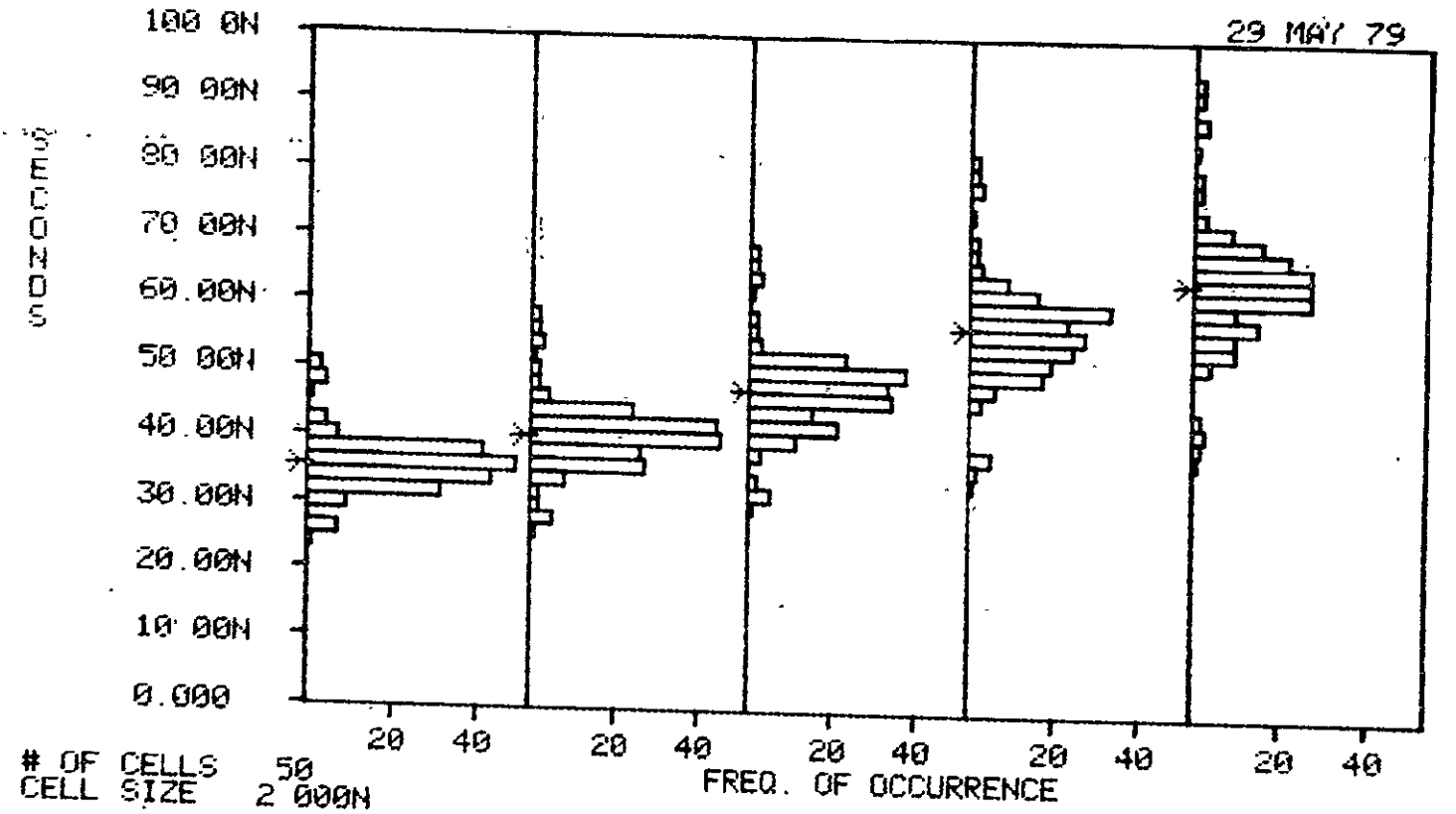
S-3260 DATA FOR TB01 TB0: VDD=5V



OF CELLS 50
CELL SIZE 4.000N

READINGS:	200	200	200	200	200
MAXIMUM:	117.5N	136.5N	162.5N	195.0N	219.5N
MEAN:	76.52N	88.82N	105.6N	127.5N	143.4N
MINIMUM:	45.60N	51.90N	60.55N	71.70N	80.40N
STD DEV :	11.59N	13.66N	16.47N	19.80N	22.29N

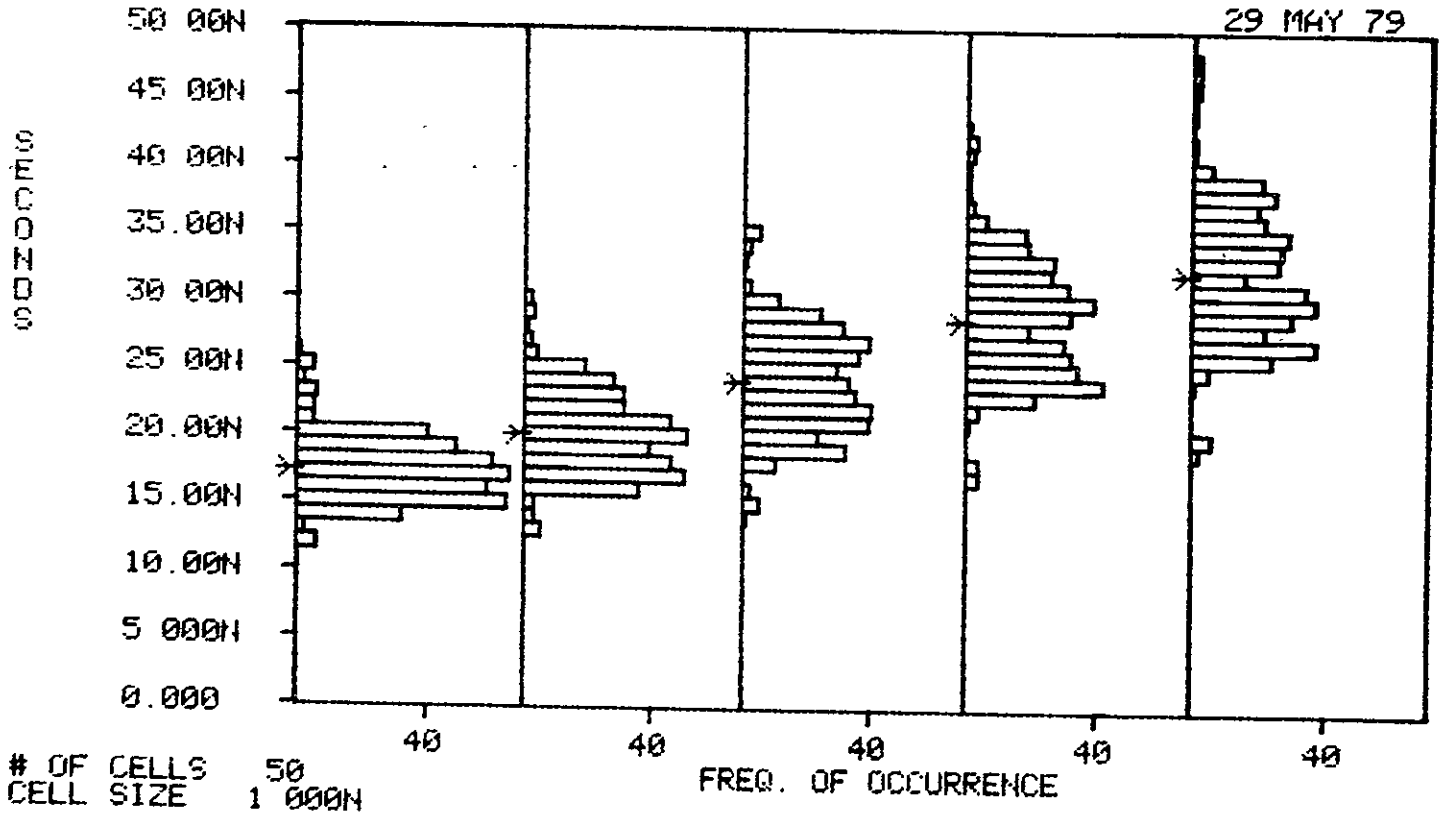
S-3260 DATA FOR TB02 TB0: VDD=10V



OF CELLS 50
CELL SIZE 2 000N

READINGS:	200	200	200	200	200
MAXIMUM:	50.35N	57.70N	68.15N	82.60N	93.65N
MEAN:	35.41N	40.20N	47.25N	56.77N	64.04N
MINIMUM:	23.90N	26.55N	30.10N	34.95N	38.75N
STD DEV.:	4.175N	4.966N	6.130N	7.623N	8.758N

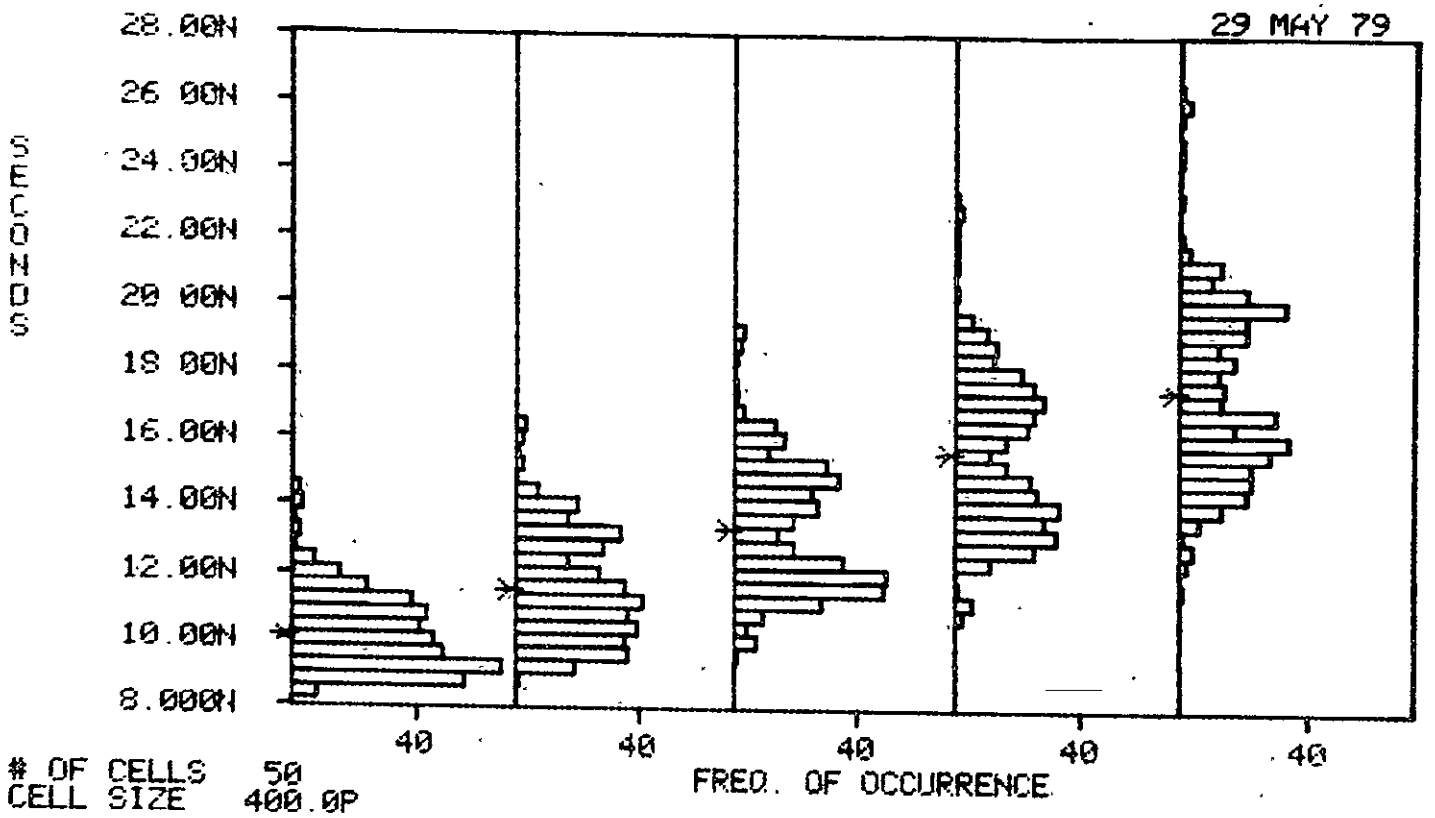
S-3260 DATA FOR TT1 TTLH/TTHL: VDD=5V



OF CELLS 50
CELL SIZE 1.000N

READINGS:	400	400	400	400	400
MAXIMUM:	25.60N	30.00N	35.00N	43.50N	47.50N
MEAN:	17.22N	20.02N	24.00N	28.60N	32.12N
MINIMUM:	11.90N	12.80N	14.45N	16.75N	19.20N
STD.DEV.:	2.368N	3.078N	3.699N	4.367N	4.869N

S-3260 . DHTH FOR TT2 TTLH/TTHL: VDD=10V



OF CELLS 50
CELL SIZE 400.0P

READINGS:	400	400	400	400	400
MAXIMUM:	14.40N	16.40N	19.15N	23.25N	26.55N
MEAN:	10.13N	11.53N	13.32N	15.59N	17.48N
MINIMUM:	8.350N	8.900N	9.750N	10.60N	11.70N
STD.DEV.	1.134N	1.537N	1.827N	2.253N	2.532N