A DC MODEL FOR POWER SWITCHING TRANSISTORS SUITABLE FOR COMPUTER-AIDED DESIGN AND ANALYSIS

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ABSTRACT

There exists a need for a reasonably accurate model for bipolar junction power switching transistors whose parameters can be readily obtained by the circuit design engineer, and which can be conveniently incorporated into standard computer-based circuit analysis programs. This paper presents such a dc model whose formulation results entirely from measurements which may be made with standard laboratory equipment. Measurement procedures, as well as a comparison between actual and computed results, are presented.

INTRODUCTION

During the past decade, computer-aided design and analysis (CADA) programs have begun to emerge as powerful tools for the design and analysis of power electronic circuits. In many applications it is desirable to utilize a model for a bipolar junction power switching transistor. The degree of accuracy required of such a model, of course, may vary from one application to another, but in many applications the accuracy of the desired network simulation result is directly proportional to the accuracy of the device model employed. One example where this is true is in the simulation of the voltage and current stresses placed on the power switching transistor itself when it is embedded in an electronic power circuit.

The diversity of various transistor models usually leaves open for decision by the circuit design engineer the question as to which transistor model should actually be used. When choosing a transistor model, one is generally faced with three trade-offs: (1) The desired accuracy of the model in the intended region of operation; (2) the availability, from measurements or otherwise, of model parameters necessary for the successful implementation of the model; and (3) the adaptability of the chosen modeling approach to the particular type of CADA program one wishes to utilize.

This paper addresses the task of modeling the nonlinear dc characteristics of a power switching transistor, paying special attention to those nonlinearities which may prove to be of particular importance to power electronics design. The approach is essentially a "black box" approach. Of particular interest is the fact that the formulation of this dc model results from measurements which may be made with standard commonly-available laboratory equipment. Measurement procedures are discussed in detail, a model formulation adapted for use with SUPER*SCEPTRE is presented, and a comparison between actual and computer-generated results is made.

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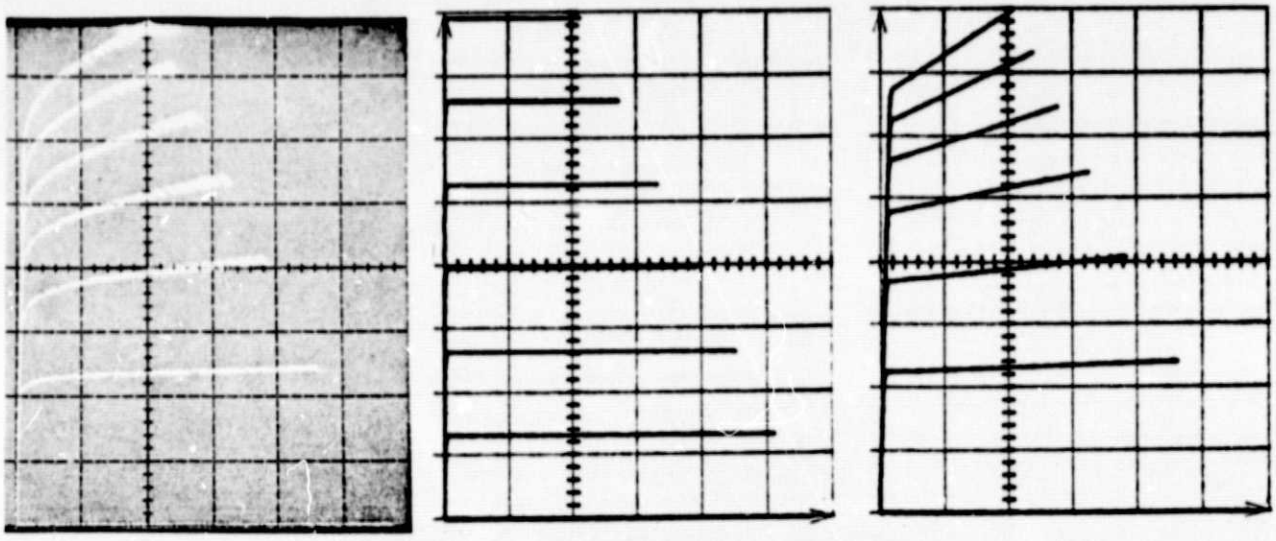
DISCUSSION OF TRANSISTOR MODELS AND DEVICE CHARACTERISTICS

Because transistor models have been around almost as long as transistors themselves, a great deal has been published on various approaches to modeling transistor characteristics. These various approaches, in many cases, were developed with a specific application in mind, be it integrated circuit analysis or device development. References 1 to 7 comprise a list of sources which were found to be very helpful in developing the dc modeling approach to be presented. Few of the models, however, appear to lend themselves well to predicting the types of nonlinearities encountered in power switching transistors, and, of the subset that do, even fewer are readily adaptable for use in conjunction with CADA programs.

Regardless of the approach which is undertaken, a common denominator among all transistor modeling approaches is that various values of model parameters or other specific information about the device under consideration must be made available before the model can be successfully implemented. One fact which is often overlooked when various modeling approaches are being considered is simply that transistor characteristics vary from transistor to transistor. Therefore, no power transistor model, regardless of formulation, can be expected to accurately predict the characteristics of any transistor other than the one from which the model parameters were obtained. The circuit design engineer is therefore confronted with a tradeoff. If he uses "typical" parameter values for his model, he can expect no more than a "typical" model. If, however, his application demands a more accurate characterization of a particular device, the ease with which the parameters for that device can be obtained becomes of primary importance.



(a) (b) (c)

Figure 1. Collector characteristics for 2N6354 transistor as (a) taken from curve tracer, (b) as predicted by simple Ebers-Moll model, and (c) as predicted by this modeling approach, with scale factors V_{CE}, 5V/div; I_C, 1A/div; and I_B, 50mA/step.

Thus, the purpose of the dc modeling approach presented here is to predict, with reasonable accuracy, the dc characteristics of a power switching transistor, and yet keep the measurement scheme used in the formulation of the model simple enough to allow the characterization of individual devices in a practical manner. It should be emphasized that this is a dc model only, and in that sense it is not a complete model. However, this dc model should provide a foundation upon which to build a complete model including dynamic characteristics.

Figure 1(a) is an oscillogram of the collector characteristics of a 2N6354 transistor in its high current region. Two important effects to be recognized from this photograph are that the dc current gain h_{FE} (or β), defined as the ratio of collector current I_C to base current I_B, depends not only in a nonlinear way on I_B, but also is functionally related to collector-emitter voltage V_{CE}. Observe that these two nonlinear dependencies become more pronounced with increasing base current levels. The dependence of h_{FE} on I_B and V_{CE} has long been recognized. The variation of h_{FE} with respect to base current is often referred to as the Webster effect [8], and the variation of h_{FE} with respect to V_{CE} is often referred to as the Early effect [9].

Because h_{FE}, at any point in the V_{CE}-I_C plane, is a function not only of I_B but also of V_{CE}, and because these relationships between h_{FE} and I_B, and between h_{FE} and V_{CE}, are nonlinear in nature, the collector characteristics in the V_{CE}-I_C plane are difficult to model accurately. The most well known of transistor models, the classical Ebers-Moll model [2], does not predict the observed variation of h_{FE} with respect to either I_B or V_{CE}. For comparison purposes, Fig. 1(b) portrays a computer-generated family of collector characteristics for this same 2N6354 transistor as predicted by a simple Ebers-Moll model. Also shown, Fig. 1(c), are collector characteristics for this transistor as predicted by the model presented in the next section. Several variations of modified Ebers-Moll models have been formulated taking either one or both of the above h_{FE} dependencies into account [3-6]. To date these modified Ebers-Moll models have been principally developed for low-power signal transistors, and they do not lend themselves well to predicting the type of h_{FE} variation occurring in power switching transistors. The basic Ebers-Moll model has the dual advantage of being relatively simple to understand and easy to work with; it is a modified Ebers-Moll model with which this paper is concerned.

DESCRIPTION OF MODIFIED EBERS-MOLL MODEL AND MEASUREMENT SCHEME

The complete modified Ebers-Moll equivalent circuit model developed in this paper for an NPN transistor is shown in Fig. 2. Note that the gain of the forward dependent current generator, controlled by the base-emitter junction diode current I_F and identified by the symbol α_F, is a function of both I_B and V_{CE}. Also included in the model are base, collector, and emitter series resistances $R_{BB'}$, $R_{CC'}$, and $R_{EE'}$, respectively, as well as the familiar pair of ideal diodes and the reverse dependent current generator with constant gain α_R. Nonlinear junction capacitances C_C and C_E, which are not characterized in this paper, are shown for explanatory purposes. This section describes the methods by which the components of the model are measured and characterized.

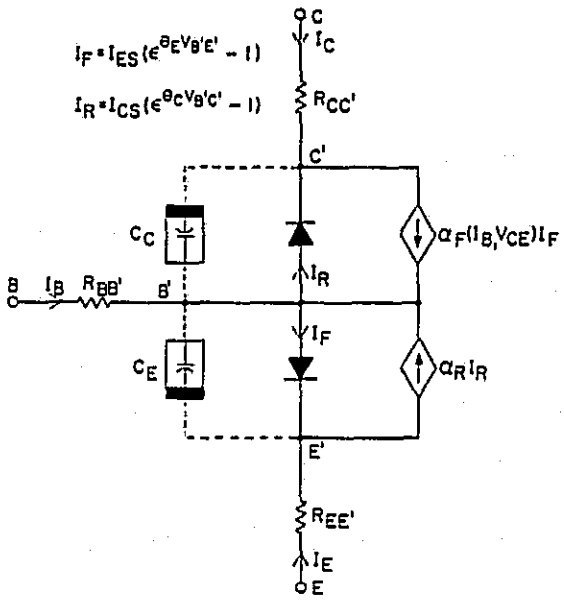


Figure 2. Proposed modified Ebers-Moll model for an NPN transistor. The nonlinear capacitances C_C and C_E (shown dashed) have been included for explanatory purposes.

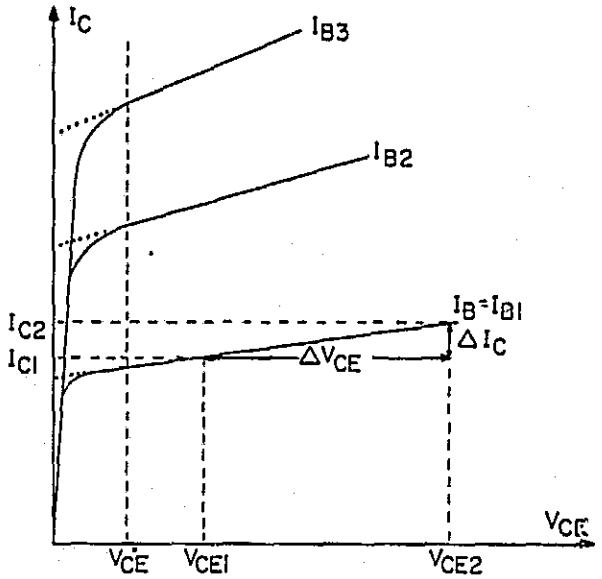


Figure 3. Expanded view of a family of three constant I_B collector characteristics showing measurement of $\Delta I_C/\Delta V_{CE}$.

As previously mentioned, the nonlinear relationships between h_{FE} and I_B, and between h_{FE} and V_{CE}, are difficult to characterize, simply because any measured value of h_{FE} in the high current region is simultaneously affected by both the Webster and Early effects. However, if one of these effects can be distinguished from the other effect, h_{FE} can be characterized as having two components; one component due to h_{FE} variation with respect to I_B (Webster effect), and one component due to h_{FE} variation with respect to V_{CE} (Early effect). The technique used here is to first characterize the Early effect and then to use the results of this characterization when characterizing the Webster effect.

An expanded view of a family of three constant I_B characteristics is shown in Fig. 3. Referring to this figure, it can be seen that for collector-emitter voltages greater than some value of collector-emitter voltage V_{CE}^*, the constant I_B curves in the V_{CE}-I_C plane can be characterized as straight lines with a slope which is dependent on the particular value of I_B under consideration. Thus, for a single I_B characteristic, the slope of the straight-line portion of the curve can be approximated from two points as

$$\frac{\Delta I_C}{\Delta V_{CE}} = \frac{I_{C2} - I_{C1}}{V_{CE2} - V_{CE1}} \qquad (1)$$

From the relationship $I_C = h_{FE} I_B$, one may define a change in h_{FE} for a constant I_B as

$$\Delta h_{FE} \triangleq \frac{\Delta I_C}{I_B} \qquad (2)$$

Dividing both sides of equation (1) by I_B, and using the results of equation (2), one can define a new constant M which is a function of I_B, given by

$$M(I_{B1}) \triangleq \frac{\Delta h_{FE}}{\Delta V_{CE}} = \frac{\Delta I_C/I_B}{\Delta V_{CE}} = \frac{(I_{C2} - I_{C1})/I_{B1}}{V_{CE2} - V_{CE1}} \qquad (3)$$

If one makes measurements to determine M over a range of values of I_B, and then plots M as a function of $\log_{10} I_B$, an approximately exponential relationship between M and $\log_{10} I_B$ is recognized. Figure 4 shows the results of such measurements for the 2N6354 and 2N6544 transistors.

The measured values of M and the corresponding values of $\log_{10} I_B$ are then used to find a least squares fit to a function of the form

$$M = A\exp(B\log_{10} I_B) + C \qquad (4)$$

where A, B, and C are determined from the least squares fit [10]. Depending on the shape of the plotted results of the M vs. $\log_{10} I_B$ measurements, a bit of trial and error may be in order to determine whether or not the inclusion of the constant C will improve the overall fit. The

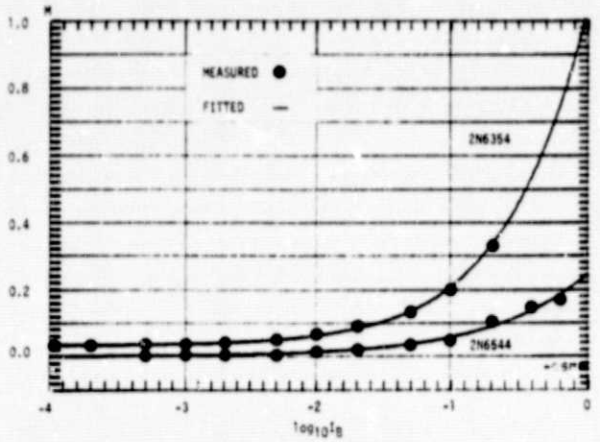


Figure 4. Measured values of M as a function of $\log_{10} I_B$ along with results of exponential least-squares fit for the 2N6354 and 2N6544 transistors. Numerical values for the coefficients used are given in Table 2.

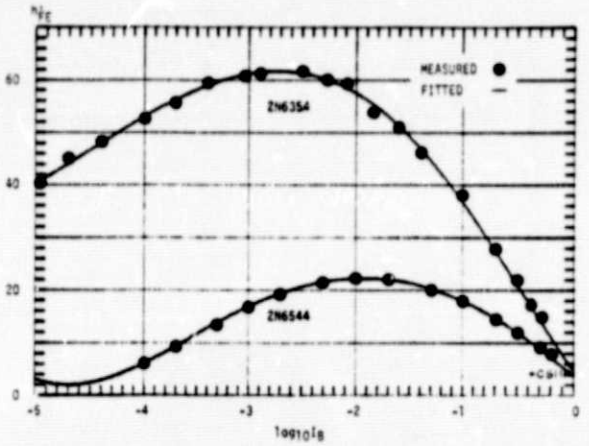


Figure 5. Measured values of h'_{FE} as a function of $\log_{10} I_B$ along with results of polynomial least-squares fit for the 2N6354 and 2N6544 transistors. Numerical values for the coefficients used are given in Table 2.

results of the least-squares fit compared with the measured values are shown in Fig. 4 for the 2N6354 and 2N6544 transistors.

The second step in characterizing α_F is then undertaken. From curve tracer measurements, values of h_{FE} are obtained over a range of I_B values and and at a single value of $V_{CE} = V_{CE1}$. The only restriction on the choice of V_{CE1} is that $V_{CE1} \geq V_{CE}^*$, so that the characterization of h_{FE} as a function of I_B may be compatible with the straight-line approximations used previously in characterizing the Early effect. In practice, as long as the above restriction is met, factors influencing the choice of V_{CE1} are convenience and the power limitations of the curve tracer as well as the safe operating area of the transistor.

Because each measurement of h_{FE} is made at a known value of $V_{CE} = V_{CE1}$, the contribution of the Early effect to the value of h_{FE} at each measurement point can be calculated from the preceding least-squares fit of M as a function of $\log_{10} I_B$. In other words, the results of equation (4) may be used to adjust each measured value of h_{FE} by an amount determined by the contribution of the Early effect at that particular value of $I_B = I_{B1}$ and $V_{CE} = V_{CE1}$.

For a pictorial explanation, the reader is again referred to Fig. 3. Considering a single collector characteristic associated with $I_B = I_{B1}$, the straight-line approximation used in characterizing the Early effect is extrapolated backward to the axis corresponding to $V_{CE} = 0$. A measurement of $h_{FE} = h'_{FE}$ is made at the point where the extrapolated line (the dotted line in Fig. 3) crosses this axis. The value of h'_{FE} determined in this manner is now independent of V_{CE}.

In practice, it is unnecessary to actually perform this extrapolation. Suppose a value of $h_{FE} = h_{FE1}$ is obtained at $I_B = I_{B1}$ and $V_{CE} = V_{CE1}$. The following steps are then performed to determine h'_{FE}:

(1) Knowing $I_B = I_{B1}$, and thus $\log_{10} I_{B1}$, use equation (4) to determine M;
(2) Calculate $h'_{FE_1} = h_{FE_1} - MV_{CE1}$.

This procedure is equivalent to the pictorial one described above.

The above procedure is repeated for a range of I_B values, and h'_{FE} is plotted versus $\log_{10} I_B$. The resulting plots for h'_{FE} vs. $\log_{10} I_B$ for the 2N6354 and 2N6544 transistors are shown in Fig.5. Note that because of the shape of the measured data, the function h'_{FE} may be approximated conveniently by a polynomial in $\log_{10} I_B$, which is the procedure used for this model. While the order of the polynomial may vary depending on the nature of the data obtained for a specific transistor, or on the degree of accuracy required of the least squares polynomial fit [11], it has been found that a good fit of h'_{FE} as a function of $\log_{10} I_B$ can usually be obtained with a polynomial of degree five or less.

It should be noted that in general the results of the curve fitting procedures previously described are valid only over the range of values in which measurements were made. Attempting to utilize the model outside this range may produce erroneous results. This fact is evident from the left-most portion of the fitted curve shown in Fig. 5 for the 2N6544 transistor where the resultant mathematical function begins to ascend.

The forward dependent current generator parameter α_F can now be described as consisting of two parts; one, a polynomial in $\log_{10} I_B$, and two, an exponential function of I_B multiplied by V_{CE}. Symbolically, this process can be described as follows:

$$h_{FE} = h'_{FE} + MV_{CE} \tag{5}$$

or h_{FE} = (a polynomial in $\log_{10} I_B$)

$$+ \text{(an exponential in } \log_{10} I_B) V_{CE} \tag{6}$$

α_F is then calculated from h_{FE} as

$$\alpha_F(I_B, V_{CE}) = \frac{h_{FE}}{h_{FE} + 1} \tag{7}$$

where the symbol $\alpha_F(I_B, V_{CE})$ is used as a reminder of the functional dependence of α_F on I_B and V_{CE}.

A FORTRAN subroutine was written to implement this process, and this subroutine, in conjunction with the circuit analysis program SUPER*SCEPTRE [12], is used to calculate the value of α_F at each solution point in the transient solution. The FORTRAN subroutine written to evaluate α_F for a particular 2N6354 transistor appears at the bottom of the SUPER*SCEPTRE input listing shown in Fig. 6.

The remaining elements of the transistor dc model may now be characterized. Referring to the schematic diagram of the model shown in Fig. 2, the two diodes are characterized by the following two equations:

$$I_F = I_{ES} (\epsilon^{\Theta_E V_{B'E'}} - 1) \tag{8}$$

and

$$I_R = I_{CS} (\epsilon^{\Theta_C V_{B'C'}} - 1) \tag{9}$$

The techniques used for measuring Θ_E, Θ_C, I_{ES}, and I_{CS} are standard, and rather then presenting a detailed discussion here, the reader is referred to Reference 6 for an excellent presentation of one method for determing these parameters. It is necessary to note that the type of measurement information needed for the methods of [6] can be obtained from curve tracer information, although other measurement schemes may be preferable to different individuals. One difference, however, between the measurement procedure described in [6], and the procedure used in formulating the present model involves the condition of the collector (emitter) terminal when making base-emitter (base-collector) measurements. The values of Θ_E, Θ_C, I_{ES}, and I_{CS} were determined under short-circuit conditions, i.e., when measuring the base-emitter (base-collector) junction, the collector (emitter) terminal was short-circuited to the base.

The value of α_R is calculated from measure-

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MODEL DESCRIPTION
MODEL RCA6354 (C-B-E)
UNITS-AMPS-VOLTS-OHMS-UF-UH-USEC
ELEMENTS
RB,B-Y=.114
RC,C-X=.037
RE,Z-E=.077
JBC,Y-X=DIODE EQUATION(7.401E-10,27.7)
JBE,Y-Z=DIODE EQUATION(6.805E-12,36.9)
CBE,Y-Z=.01
CBC,Y-X=.01
JN,X-Y=FGEN(JBE,IRB,PCE)
JI,Z-Y=.89*JBC
DEFINED PARAMETERS
PCE=X1 (VCBE-VCBC+VRC+VRE)
CIRCUIT DESCRIPTION
**************************************************
CURVE TRACER SIMULATION CIRCUIT
**************************************************
UNITS-AMPS-VOLTS-OHMS-UF-UH-USEC
ELEMENTS
T1,2-1-G = MODEL RCA6354
RL,3-2=2.25
J2,G-1 = TABLE 1 (TIME)
EVCC,G-3 = TABLE 2 (TIME)
OUTPUTS
J2
IEVCC, PLOT(PCET1)
FUNCTIONS
TABLE 1
0,0,1E4,0,1.001E4,.05,2E4,.05,
2.001E4,.10,3E4,.10,3.001E4,.15,
4E4,.15,4.001E4,.20,5E4,.20,5.001E4,
.25,6E4,.25,6.001E4,.30,7E4,.30
TABLE 2
0,0,5E3,28.5,1E4,0,1.5E4,28.5,2E4,0,
2.5E4,28.5,3E4,0,3.5E4,28.5,4E4,0,
4.5E4,28.5,5E4,0,5.5E4,28.5,6E4,
0,6.5E4,28.5,7E4,0
RUN CONTROLS
STOP TIME = 7E4
MINIMUM STEP SIZE = 1.0E-20
MAXIMUM STEP SIZE = 50.0
MAXIMUM PRINT POINTS = 501
INTEGRATION ROUTINE = IMPLICIT
END
***    FORTRAN SUBROUTINE    ***
       FUNCTION FGEN(JBE,IRBB,PCE)
       REAL JBE,IRBB,M
       IF (IRBB) 1,1,2
     1 BETA=.10
       GO TO 3
     2 Y=ALOG10(IRBB)
       BETA=4.695-32.06*Y+4.777*Y*Y
      1+5.669*Y*Y*Y+1.060*Y*Y*Y*Y
      1+.06348*Y*Y*Y*Y*Y
       M=1.009*EXP(1.745*Y)+.032
       BETA=BETA+M*PCE
     3 ALPHA=BETA/(BETA+1.0)
       FGEN=ALPHA*JBE
       RETURN
       END
```

*Figure 6. Input listing in SUPER*SCEPTRE format used to produce a family of collector characteristics for the 2N6354 transistor which was studied. Listing includes model description, curve tracer simulation circuitry, and FORTRAN subroutine.*

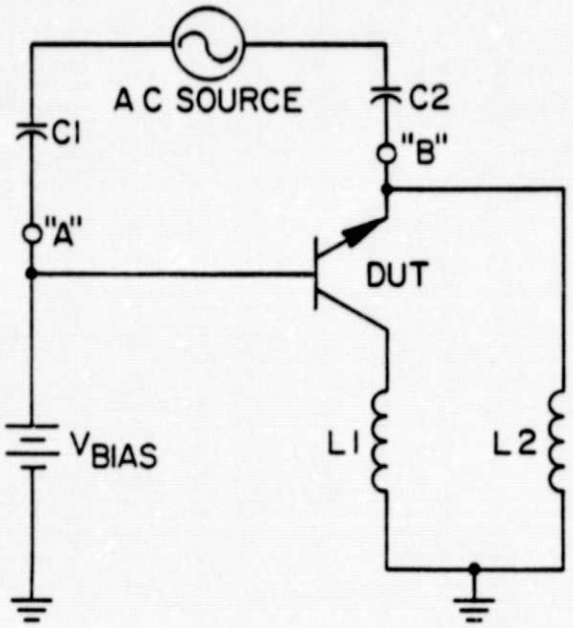

Figure 7. Test circuit used to determine $R_{BB'}$, $R_{EE'}$, and $R_{CC'}$, with component values L1=L2=14.7mH; C1=C2=220μF. Configuration shown used to measure $R_{BB'}$+$R_{EE'}$.

ments in a standard manner [13]. Although the actual value of α_R, in fact, is dependent on the value of I_B at which the measurement is taken, the value of α_R has been found to remain fairly constant over a wide range of I_B, decreasing significantly only for large values of I_B. Consequently, a mid-range calculation of α_R is used as a first order approximation to the behavior of the reverse current generator.

The measurement of the three series resistances $R_{BB'}$, $R_{CC'}$, and $R_{EE'}$ presents a special measurement problem, particularly because non-negligible values of α_R are usually measured for power switching transistors. A measurement scheme was devised which utilized the special properties of the nonlinear capacitances C_E and C_C, shown dashed in Fig. 2, normally associated with each transistor junction. Under high forward bias conditions these capacitances have what initially seems to be surprisingly high values [14]. In the case of power switching transistors, these capacitances often measure in the hundreds of microfarads range.

Therefore, by placing both junctions in a condition of high forward bias, the capacitances appear essentially as short circuits to ac voltages and currents, thus allowing small-signal ac measurements of the series resistances without the effects of the ideal diodes and current generators being present. The series resistances are determined from a series of three measurements. Small-signal ac measurements at the collector-emitter, base-collector, and base-emitter terminals correspond to values for $R_{CC'} + R_{EE'}$, $R_{BB'} + R_{CC'}$, and $R_{BB'} + R_{EE'}$, respectively. Once these values are measured, the values of the respective series resistances are determined by solving the resulting set of three simultaneous linear equations in three unknowns.

The test circuit shown in Fig. 7 is used to make these measurements with the ac signal source terminals labelled "A" and "B" connected to the appropriate transistor terminals for the three separate measurements. The purpose of the large inductors L_1 and L_2 is to block the ac path through the bias supply V_{BIAS}, while the purpose of capacitors C_1 and C_2 is to insure that the ac source is truly ac-coupled at the transistor terminals.

While observing the ac current and voltage waveforms on an oscilloscope, V_{BIAS} is increased to the point where a further increase in V_{BIAS} produces no observable change in the ac waveforms. A frequency is then found for which the ac current and voltage waveforms are approximately in phase with one another. Three measurements are then taken, one at the frequency where the ac current and voltage waveforms are approximately in phase, and two others at an octave above and below this frequency. The results of these measurements, as well as other pertinent test conditions, are shown in Table 1 for the three junctions of the 2N6354.

The values of all the parameters measured for the 2N6354 and 2N6544 transistors are shown in Table 2. It should be emphasized that these results are for one particular transistor of each type, and these results will not necessarily be valid except for the particular transistors measured.

COMPARISON OF COMPUTED AND OBSERVED COLLECTOR CHARACTERISTICS

Figure 6 is an input listing in SUPER*SCEPTRE format for the resultant 2N6354 transistor embedded in a circuit used to simulate a transistor curve tracer. Figures 8(b),(d) and 9(b),(d) are predicted output characteristics for the 2N6354 and 2N6544 transistors, respectively, over two different ranges of base current which were produced from the output of SUPER*SCEPTRE. Figures 8(a),(c) and 9(a),(c) are oscillograms of collector characteristics, taken from a Tektronix Type 577 curve tracer under pulsed conditions, corresponding to the predicted collector characteristics beside them. From these figures, good agreement between predicted and observed results can be seen. In order to provide more detailed comparison, the predicted results shown in Figs. 8 and 9 were not directly produced by SUPER*SCEPTRE, which normally produces line printer plots and tabulated output data. Instead, the tabulated output data from SUPER*SCEPTRE was used in conjunction with another plotting routine to produce the predicted collector characteristics on a Tektronix Type 4013 graphics display terminal.

TABLE 1

Results of measurements of series resistances for the 2N6354 transistor under study.

Base-Collector Junction Measurements			
f=20kHz	V_{BC}=0.772V	ϕ=+9°	$R_{BB'}+R_{CC'}$=0.153Ω
f=40kHz	V_{BC}=0.772V	ϕ=0°	$R_{BB'}+R_{CC'}$=0.150Ω
f=80kHz	V_{BC}=0.772V	ϕ=-13°	$R_{BB'}+R_{CC'}$=0.146Ω
Base-Emitter Junction Measurements			
f=10kHz	V_{BE}=0.786V	ϕ=+9°	$R_{BB'}+R_{EE'}$=0.198Ω
f=20kHz	V_{BE}=0.786V	ϕ=0°	$R_{BB'}+R_{EE'}$=0.190Ω
f=40kHz	V_{BE}=0.786V	ϕ=-6°	$R_{BB'}+R_{EE'}$=0.179Ω
Collector-Emitter Junction Measurements			
f=20kHz	V_{BE}=0.792V	V_{BC}=0.779V	
	ϕ=+9°	$R_{CC'}+R_{EE'}$=0.117Ω	
f=40kHz	V_{BE}=0.803V	V_{BC}=0.783V	
	ϕ=0°	$R_{CC'}+R_{EE'}$=0.113Ω	
f=80kHz	V_{BE}=0.793V	V_{BC}=0.778V	
	ϕ=-22°	$R_{CC'}+R_{EE'}$=0.110Ω	

$R_{BB'}+R_{CC'}$=0.150Ω	$R_{BB'}$=0.114Ω
$R_{BB'}+R_{EE'}$=0.190Ω	$R_{EE'}$=0.077Ω
$R_{CC'}+R_{EE'}$=0.113Ω	$R_{CC'}$=0.037Ω

One area where the predicted and observed collector characteristics do not show close agreement is the high current, low collector-emitter voltage region, where the actual collector characteristics deviate most from the straight-line approximations used to characterize the Early effect. Also, it should be recognized that by utilizing the curve tracer as the measurement device, a slight tradeoff between ease and accuracy of measurement is introduced.

CONCLUSION

The major feature of the dc model presented here is that it allows the circuit design engineer to characterize the collector characteristics of a power switching transistor from a relatively low number of measurements which can be performed with standard laboratory equipment. Although two separate least-squares fits are necessary to implement this approach, once computer programs have been either located or written for this purpose, the task becomes one of simple data substitution.

One point which cannot be emphasized strongly enough is the fact that no two transistors, even of the same type, are exactly alike, and in fact, their dc characteristics may greatly differ. Therefore, no dc model can be expected to accurately predict the dc characteristics of a particular transistor unless the data used in implementing the model has been measured for that particular transistor. Hence, in many circumstances, it is desirable to be able to characterize a particular transistor quickly without the availability of an automatic test set-up dedicated to that purpose. The approach presented here lends itself well to that goal.

TABLE 2

Summary of model information for the 2N6354 and 2N6544 transistors under study.

2N6354 Data Summary

$R_{BB'}$=0.114Ω $R_{CC'}$=0.037Ω $R_{EE'}$=0.077Ω

θ_E=36.9V^{-1} I_{ES}=6.805x10^{-12} A

θ_C=27.7V^{-1} I_{CS}=7.401x10^{-10} A

α_R=0.89 $M=1.009\exp(1.745\log_{10}I_B) + 0.032$

$$h'_{FE}=4.695 - 32.06(\log_{10}I_B) + 4.777(\log_{10}I_B)^2 + 5.699(\log_{10}I_B)^3 + 1.060(\log_{10}I_B)^4 + 0.06348(\log_{10}I_B)^5$$

2N6544 Data Summary

$R_{BB'}$=0.095Ω $R_{CC'}$=0.060Ω $R_{EE'}$=0.090Ω

θ_E=30.1V^{-1} I_{ES}=3.880x10^{-11} A

θ_C=29.5V^{-1} I_{CS}=4.890x10^{-10} A

α_R=0.50 $M=0.2470\exp(1.463\log_{10}I_B)$

$$h'_{FE}=3.697 - 19.40(\log_{10}I_B) - 5.371(\log_{10}I_B)^2 - 0.4697(\log_{10}I_B)^3 - 0.2353(\log_{10}I_B)^4 - 0.04006(\log_{10}I_B)^5$$

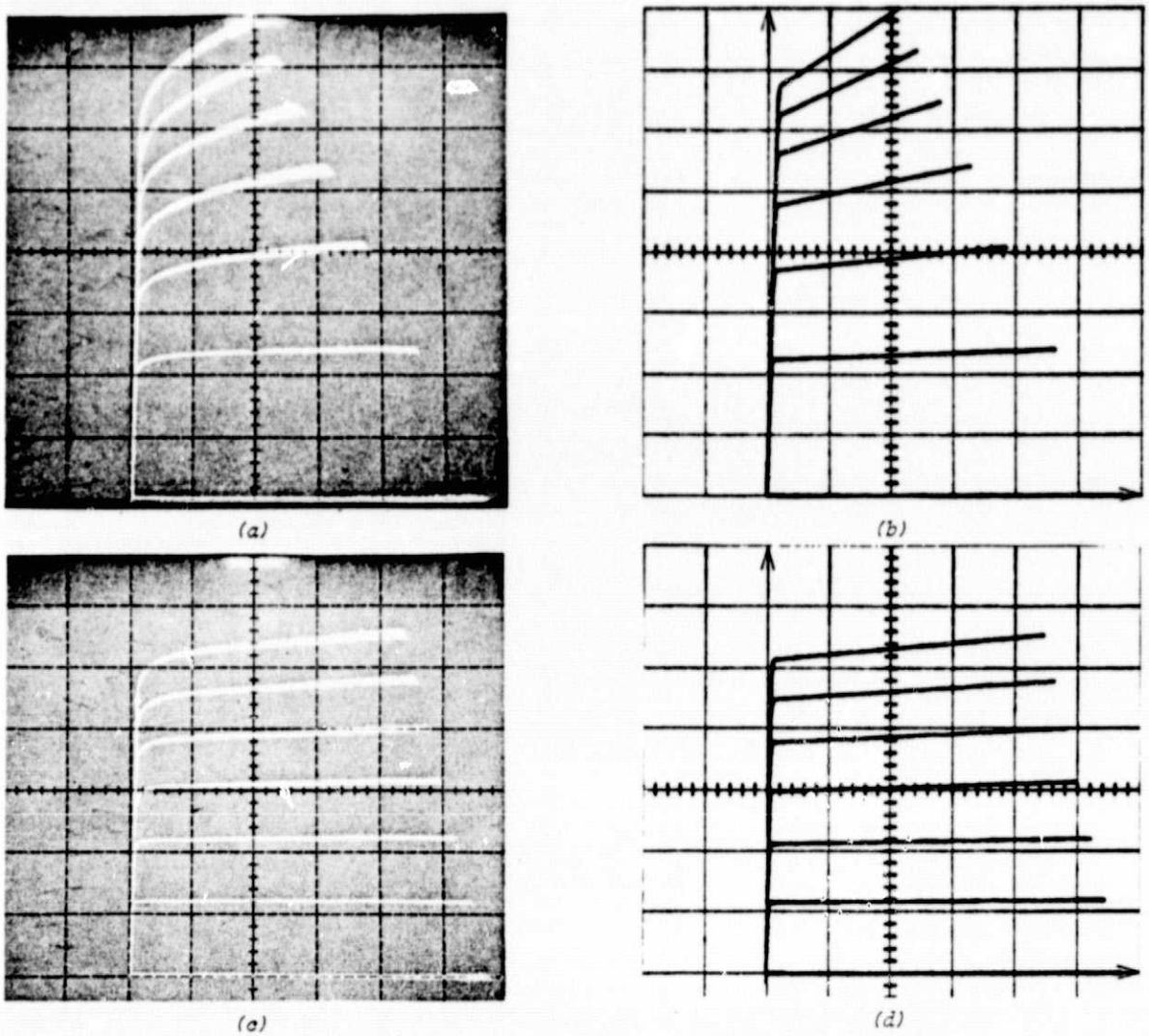

Figure 8. Collector characteristics of I_C vs. V_{CE} with I_B as a parameter for the 2N6354 transistor.
(a)-(b) High current region with scale factors V_{CE}, 5V/div; I_C, 1A/div; and I_B, 50mA/step.
(c)-(d) Medium current region with scale factors V_{CE}, 5V/div; I_C, .5A/div; and I_B, 10mA/step.

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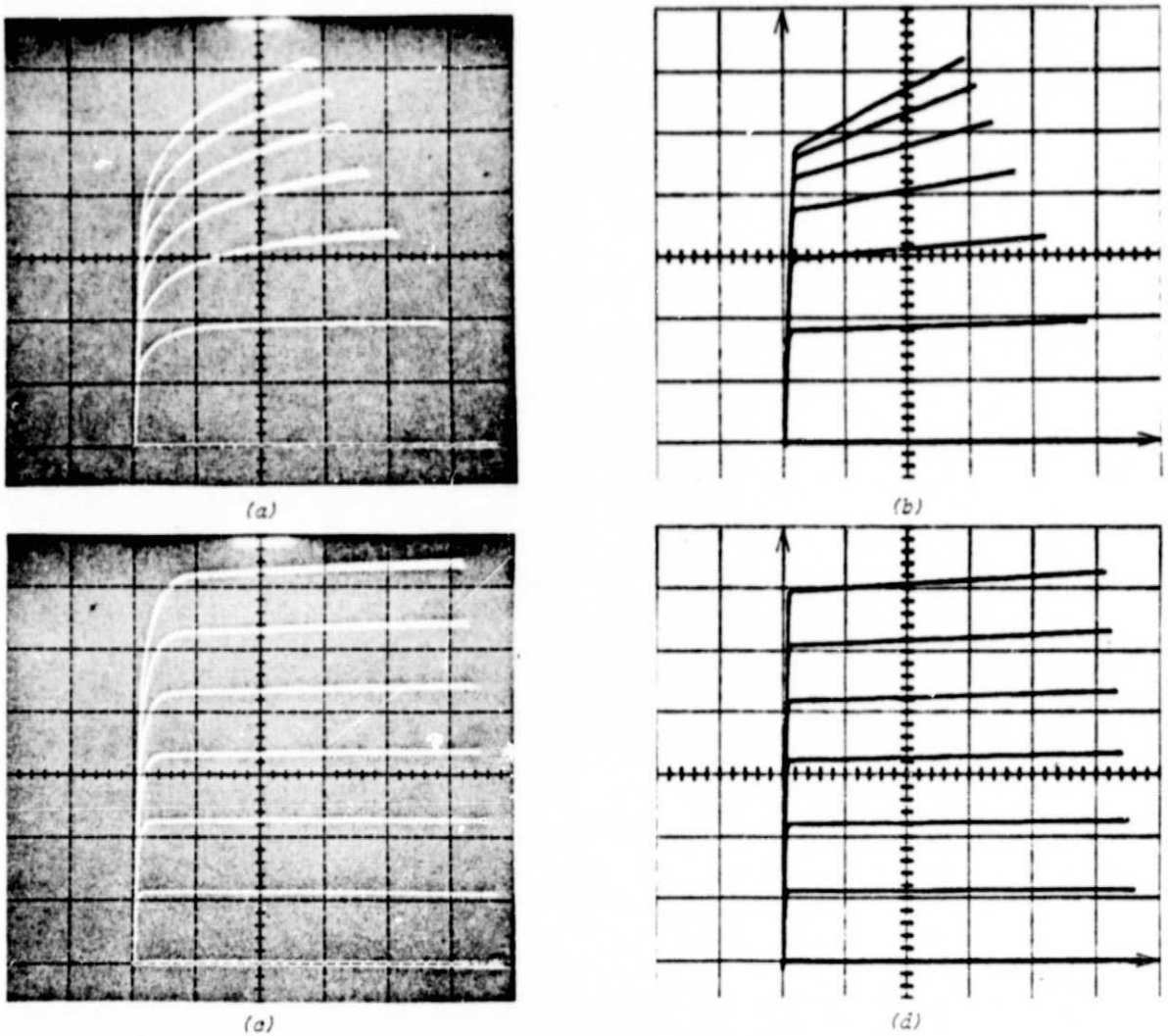

Figure 9. Collector characteristics of I_C vs. V_{CE} with I_B as a parameter for the 2N6544 transistor. (a)-(b) High current region with scale factors V_{CE}, 5V/div; I_C, 1A/div; and I_B, 100mA/step. (c)-(d) Medium current region with scale factors V_{CE}, 5V/div; I_C, .2A/div; and I_B, 10mA/step.

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