NASA CONTRACTOR
REPORT

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# DESIGN RULES FOR RCA SELF-ALIGNED SILICON-GATE CMOS/SOS PROCESS

By Advanced Technology Laboratories
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NASA - GEORGE C. MARSHALL SPACE FLIGHT CENTER
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## STANDARD ABBREVIATIONS

| Symbol | Definition |
|---|---|
| s | second |
| m | meter |
| l | liter |
| g | gram |
| V | volt |
| A | ampere |
| K | kelvin |
| Hz | hertz |
| $cm^3$ | cubic centimeter |
| min | minute |
| in. | inch |
| mil | $10^{-3}$ inch |
| C | Celsius |
| k | kilo, $10^3$ |
| M | mega, $10^6$ |
| c | centi, $10^{-2}$ |
| m | milli, $10^{-3}$ |
| $\mu$ | micro, $10^{-6}$ |
| n | nano, $10^{-9}$ |

## NONSTANDARD ABBREVIATIONS

| Symbol | Definition |
|---|---|
| PMOS | P-channel Metal Oxide Semiconductor |
| IC | Integrated Circuit |
| MSFC | George C. Marshall Space Flight Center |

NONSTANDARD ABBREVIATIONS (Concluded)

| Symbol | Definition |
|---|---|
| NASA | National Aeronautics and Space Administration |
| LSI | Large Scale Integration |
| LSIC | Large Scale Integrated Circuit |
| MSI | Medium Scale Integration |
| MSIC | Medium Scale Integrated Circuit |
| SSI | Small Scale Integration |
| SSIC | Small Scale Integrated Circuit |
| CAD | Computer Aided Design |
| CMOS | Complementary Metal Oxide Semiconductor |
| SOS | Silicon on Sapphire |
| SSTC | RCA Solid State Technology Center |
| PR2D | Two-Dimensional Automatic Placement and Routing Program |
| MP2D | Multiport Two-Dimensional Automatic Placement and Routing Program |
| $I^2$ (N/N) | Single-Epitaxial, Ion-Implanted Process |
| epi | Epitaxial Level |
| I/O | Input/Output |
| $V_{DD}$ | Power Supply Voltage |
| GND | Ground |
| poly | Polysilicon Level |
| BPM | Bonding Pad Metal |

## Section I

# INTRODUCTION

This report describes the CMOS/SOS design rules prepared by the RCA Solid State Technology Center (SSTC). These rules specify the spacing and width requirements for each of the six design levels, the seventh level being used to define openings in the passivation level. An associated report, entitled "Silicon-Gate CMOS/SOS Processing," provides further insight into the usage of these rules.

## Section II

## TECHNICAL DISCUSSION

In addition to the first seven standard rules, rule 8 has been added to facilitate the design of chip I/O pads for both the PR2D and the MP2D programs.

Since it is SSTC policy to endeavor to maintain mask set compatibility for all of the major SOS processes, it is possible for SOS standard cell arrays to be fabricated with any of a wide spectrum of processes. These include the double-epitaxial diffused processes through the single-epitaxial, ion-implanted ($I^2(N/N)$) process. For radiation-hardened applications, the double epitaxial, double-ion-implanted process is also an available option. Out of a basic set of seven masks, all of these processes can be used to fabricate the standard cell CMOS/SOS arrays or indeed any design laid out with the SSTC design rules. It is with these design rules that the NASA SOS Standard Cell families have been laid out. Process development and maturation are still taking place, while simultaneously mask compatibility is ensured.

## Section III

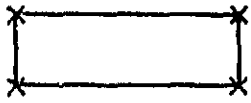
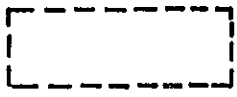
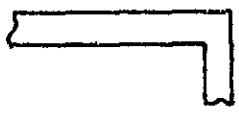
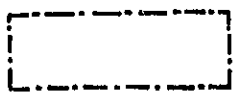
## DESIGN RULES

These design rules for silicon-gate CMOS integrated circuits are compatible with state-of-the-art technology, and have been modified along with process developments.

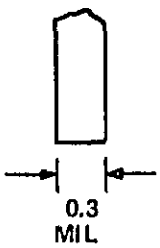
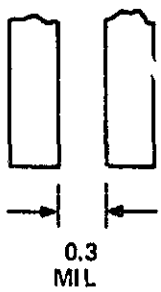
The design of contact layouts has been a key problem, since there are so many possible arrangements and also various sizes and shapes of contact openings. Therefore, examples for both in-line and right-angle contacts have been studied and presented here in order to give the designer a better insight as to what the problems are, and what contacts should and should not be used.

The composite drawing layout takes seven levels for the silicon-gate CMOS/SOS integrated circuits. A standard color code and standard symbols have been adopted and are presented in Table 1.

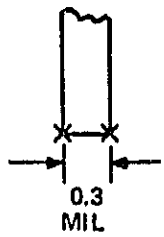
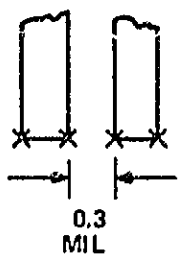
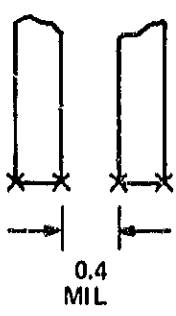
TABLE 1. STANDARD COLOR CODE FOR CMOS/SOS DESIGN LAYOUT

| Mask Level | Color Code | Symbol |
|---|---|---|
| Level 1: p-epi Island | Red |  |
| Level 2: n-epi Island | Blue |  |
| Level 3: Polysilicon | Purple |  |
| Level 4: $n^+$-diffusion | Brown |  |
| Level 5: Contact | Green |  |
| Level 6: Metal | Black |  |
| Level 7: Protective Oxide | Orange |  |

## 1. Level 1: p-epi Island

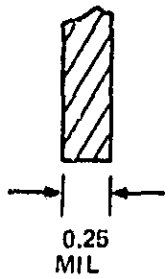
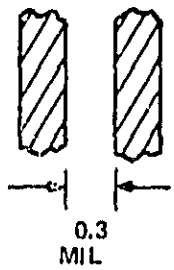
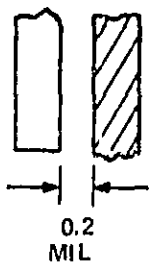
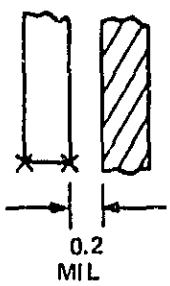
| Rule # | Item | Minimum Value(mil) | |
|---|---|---|---|
| 1.1 | Width of p-epi Island | 0.3 |   |
| 1.2 | Spacing, p-epi Island to p-epi Island | 0.3 |   |
| NOTE | Contour lines of p-epi island must be orthogonal to match with crystal orientation | | |

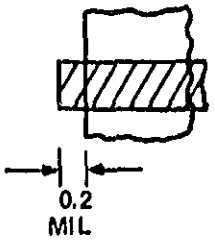
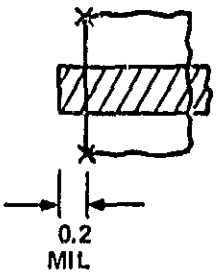
## 2. Level 2: n-epi Island

| Rule # | Item | Minimum Value(mil) | |
|---|---|---|---|
| 2.1 | Width of n-epi island | 0.3 |   |
| 2.2 | Spacing, n-epi island to n-epi island | 0.3 |   |
| 2.3 | Spacing, n-epi island to p-epi island | 0.4 |   |

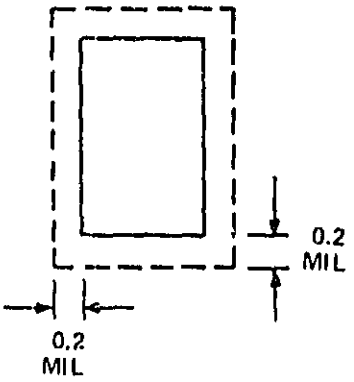
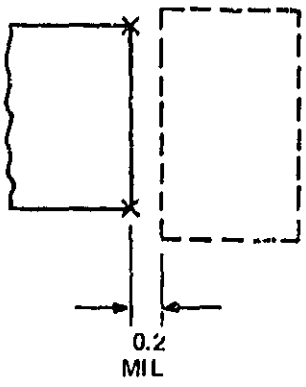
NOTE Contour lines of n-epi island must be orthogonal

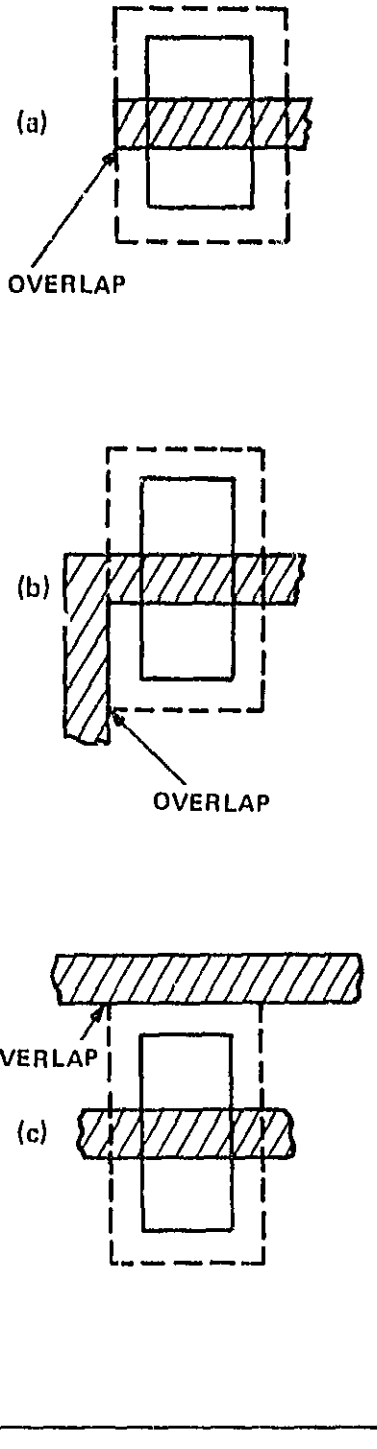
## 3. Level 3: Polysilicon

| | Item | Minimum Value(mil) | |
|---|---|---|---|
| 3.1 | Width of Polysilicon | 0.25 |   |
| 3.2 | Spacing, Polysilicon to Polysilicon | 0.3 |   |
| 3.3 | Spacing, Polysilicon to p-epi Island | 0.2 |   |
| 3.4 | Spacing, Polysilicon to n-epi Island | 0.2 |   |

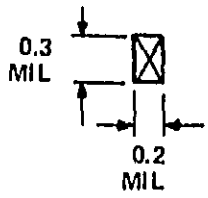
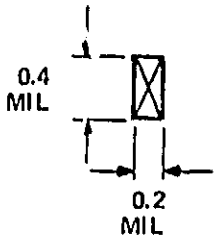
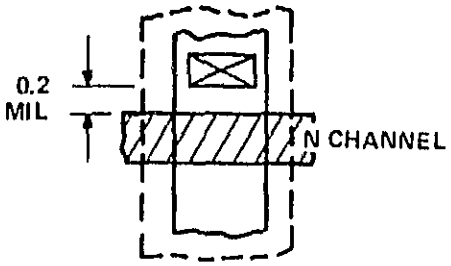
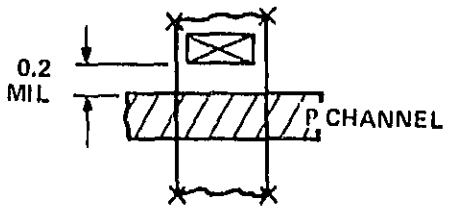
| Rule # | Item | Minimum Value(mil) | |
|---|---|---|---|
| 3.5 | Polysilicon Extension Beyond p-epi Island | 0.2 |   |
| 3.6 | Polysilicon Extension Beyond n-epi Island | 0.2 |   |

## 4. Level 4: $n^+$ Diffusion

| Rule # | Item | Minimum Value(mil) | |
|---|---|---|---|
| 4.1 | Overlap, $n^+$-Diffusion to p-epi Island | 0.2 |   |
| 4.2 | Spacing, $n^+$-Diffusion to n-epi Island | 0.2 |   |

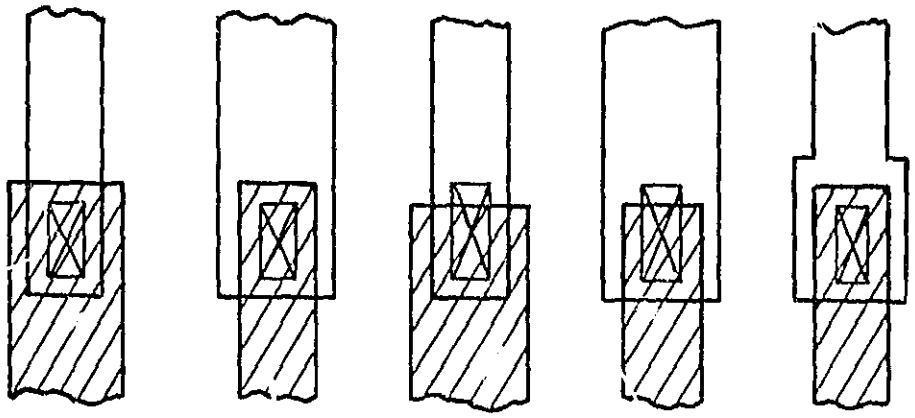
| Rule # | Item | Minimum Value(mil) | |
|---|---|---|---|
| 4.3 | Overlap of $n^+$ - Diffusion and Polysilicon is allowed | |   |

## 5. Level 5: Contact

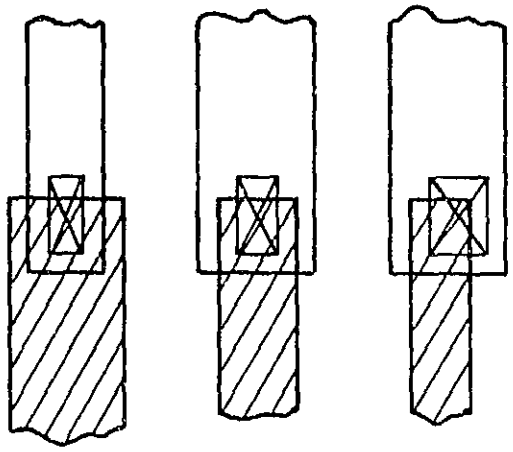
| Rule # | Item | Minimum Value(mil) | |
|---|---|---|---|
| 5.1 | Active Contact Area (Considering Possible Worst Case) | 0.2X0.3 |   |
| 5.2 | Contact Area in Level 5 Mask | 0.3X0.3 or 12X.4 |   |
| 5.3 | Spacing, Contact to Polysilicon Gate | 0.2 |     |
| NOTE | Contact of Polysilicon over Active Transistor is not Allowed. | | |

## Contacts (In-Line)

### ACCEPTABLE



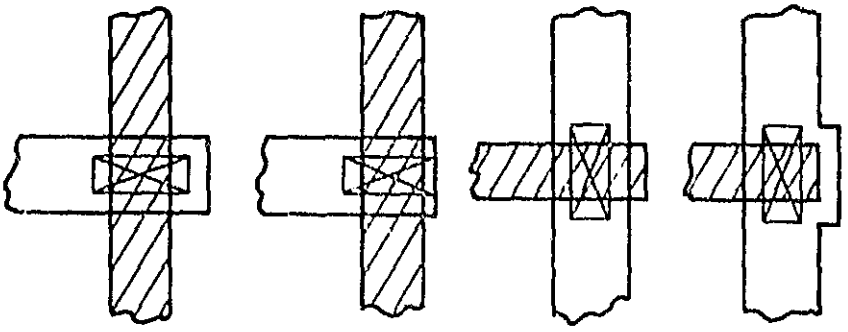
### NOT ACCEPTABLE



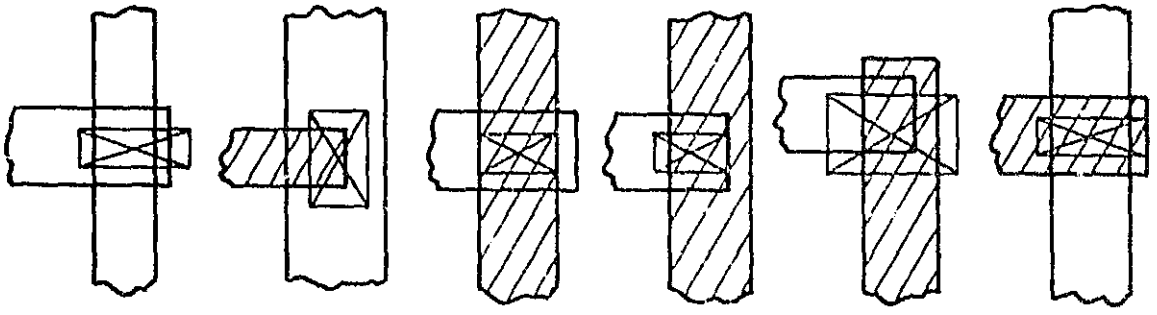
## Contacts (Right-Angle)

### ACCEPTABLE

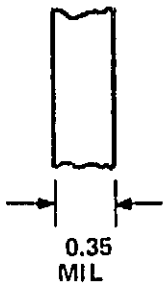
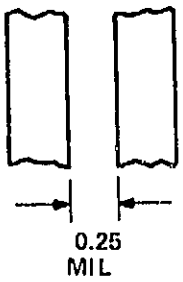
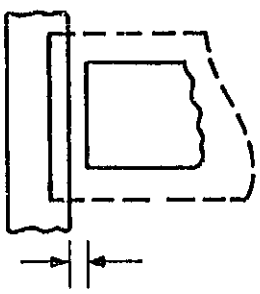
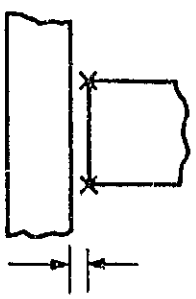
SPECIAL CASE

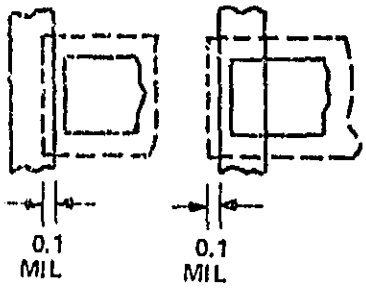
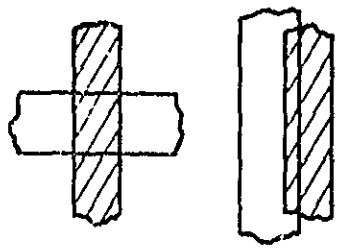
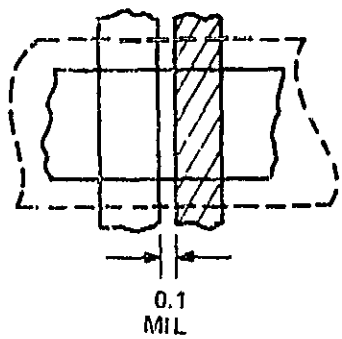
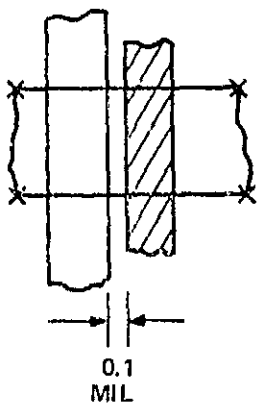


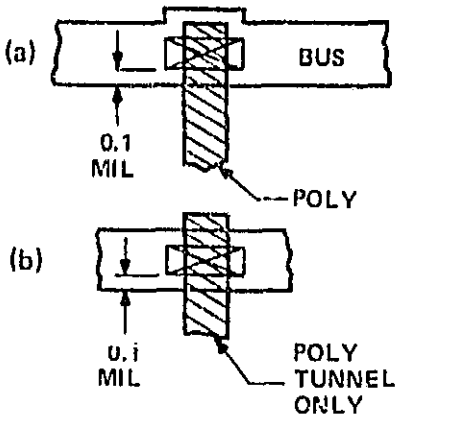
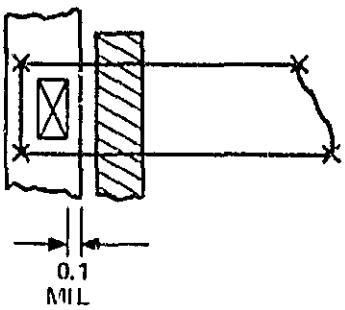
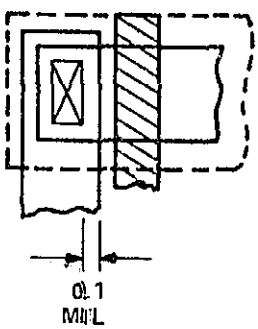
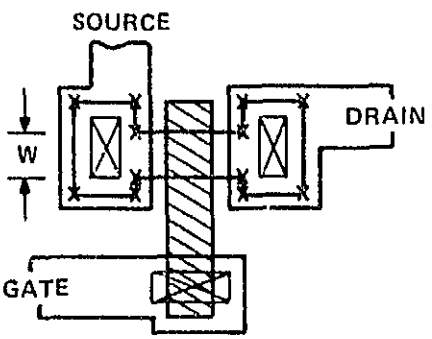
### NOT ACCEPTABLE

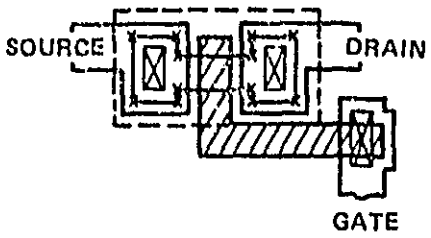
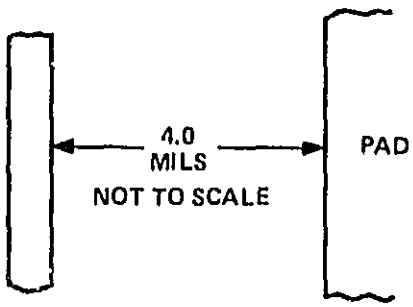
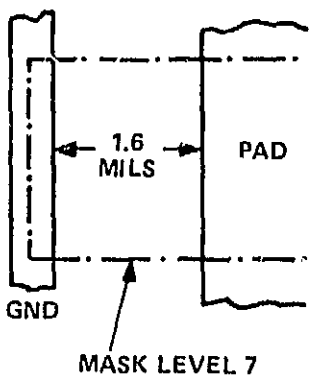


## 6. Level 6: Metal

| Rule # | Item | Minimum Value(mil) | |
|---|---|---|---|
| 6.1 | Width of Metal | 0.35 |   |
| 6.2 | Spacing, Metal to Metal | 0.25 |   |
| 6.3.1 | Spacing, Metal to p-epi to Island | 0.1 |   |
| 6.3.2 | Spacing, Metal to n-epi Island | 0.1 |   |
| NOTE | Metal should not be coincident with any edge. | | |

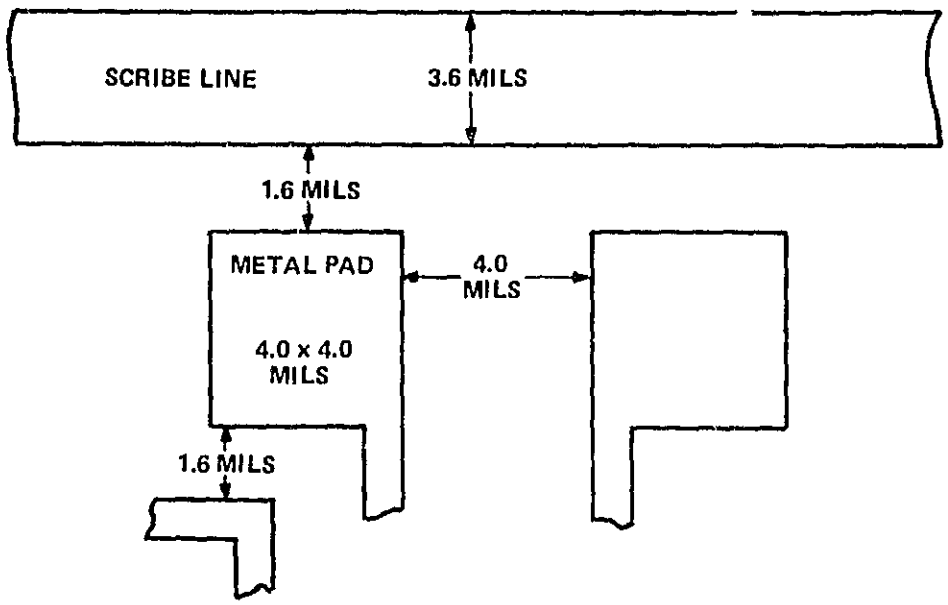
| Rule # | Item | Minimum Value(mil) | |
|---|---|---|---|
| 6.4 | Spacing, Metal to n-Diffusion | 0.1 |   |
| 6.5 | Metal and Polysilicon Edge Should not be Coincident | |  |
| 6.6.1 | Spacing, Metal to Polysilicon Gate (n-channel) | 0.1 |   |
| 6.6.2 | Spacing, Metal to Polysilicon Gate (p-channel) | 0.1 |   |

| Rule # | Item | Minimum Value(mil) | |
|---|---|---|---|
| 6.7 | Metal should Encompass Completely | |   |
| | Spacing, Metal to (Poly Tunnel) Contact | 0.1 | |
| 6.7.1 | Spacing, Metal to (n-epi) Contact | 0.1 |   |
| 6.7.2 | Spacing, Metal to (p-epi) Contact | |   |
| 6.7.3 | p-channel Transistor when $0.3 \leq W \leq 0.6$ | 0.1 |   |
| NOTE | Metal encompasses contact completely. | | |

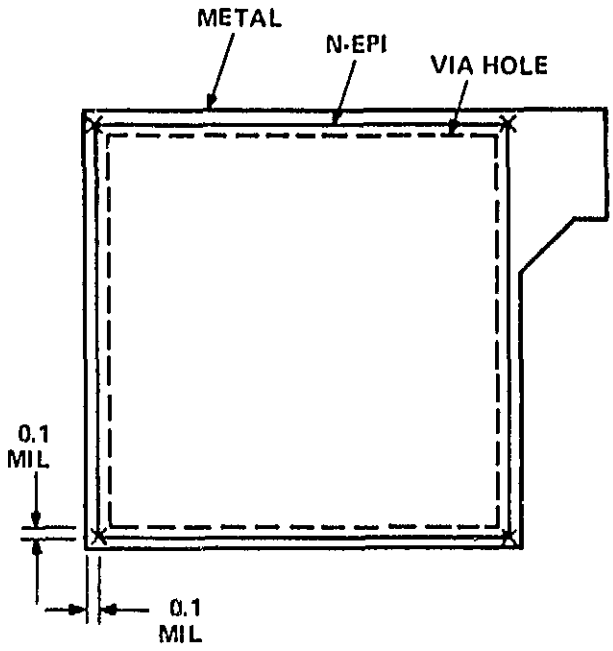
| Rule # | Item | Minimum Value(mil) | |
|---|---|---|---|
| 6.7.4 | n-channel Device when $0.3 \leq W \leq 0.6$. | |   |
| NOTE | Metal encompasses contact completely. | | |
| 6.8 | Spacing, Outside Metal to Pad (where metal bus is outside of pad area) | 4.0 |   |
| 6.9 | Air Gap between Ground Metal to Pad for Protective Device is 1.6 mils | |   |
| 6.10 | Pad Metal Overlap to n-epi Island is 0.1 mil (See Rule 7.1) | | |

| Rule # | Item | Minimum Value(mil) | |
|---|---|---|---|
| 6.11 | Pad Size | 4.0 X 4.0 | |
| 6.11.1 | Spacing, Pad to Pad | 4.0 | |
| 6.11.2 | Spacing, Pad to Metal Line | 1.6 | |
| 6.12 | Width of Scribe Line | 3.6 | |
| 6.12.1 | Spacing, Scribe Line to Pad | 1.6 | |

Metal Pad and Scribe Line



## 7. Level 7: Protective Oxide

| Rule # | Item | |
|---|---|---|
| 7.1 | n-epi Overlap to Via Hole is 0.1 mil |  |

8. Standard I/O Bonding Pad Cell Rules

This design rule and accompanying figure specify those rules which must be adhered to, in addition to the standard SOS processing rules, in order to provide PR2D and MP2D program compatibility for all standard-size input/output bonding pad cells. These I/O pads are nominally 8 mils wide by 9 mils high. This specified height is from the pad origin to the top of the bonding metal; part of the standard cell is actually as much as -2.7 mils below the origin as shown in the figure and indicated by rule 8-F. Conformity to these rules will result in proper alignment and interconnection of the bonding pads. Nonstandard bonding pads may be used but must be handled specially by the user at a minimum by specifying fixed pad locations and more probably by manual modification of the program output data. Therefore, nonstandard bonding pads should be avoided.

Distances from cell origin:

A. To center of outside bus, $V_{DD}$ or GND = 0.0 mil

B. To center of inside bus, $V_{DD}$ or GND = -1.3 mils

C. To bottommost epi = -2.4 mils max

D. To center of 0.2 mil high I/O contact = 2.4 mils max

E. To bottommost metal = -2.6 mils max

F. To bottommost poly = -2.7 mils max

G. To bottom of bonding pad metal (BPM) = 5 mils

H. To top of bonding pad metal (BPM) = 9 mils

I. To left edge of I/O bonding pad metal (BPM) = 0.2 mil*

J. To right edge of I/O bonding pad metal (BPM) = 4.2 mils*

K. To origin of adjacent I/O pad = 8.0 mils

Other:

L. Proximity of epi to cell boundary = 0.2 mil min

M. Standard bus width (routed by program) = 0.8 mil

N. Minimum spacing bonding pad metal 4x4 area to nonconnecting cell metal = 1.6 mils

O. Minimum spacing bonding pad metal 4x4 area to connecting metal = 1.0 mil

P. Minimum spacing BPM to epi = 1.0 mil
($N^+$ - diffusion and polysilicon to standard rules from this dimension)

Q. Level 1 3.8x3.8 mils centered in bonding pad metal

R. Level 7 3.6x3.6 mils centered in bonding pad metal

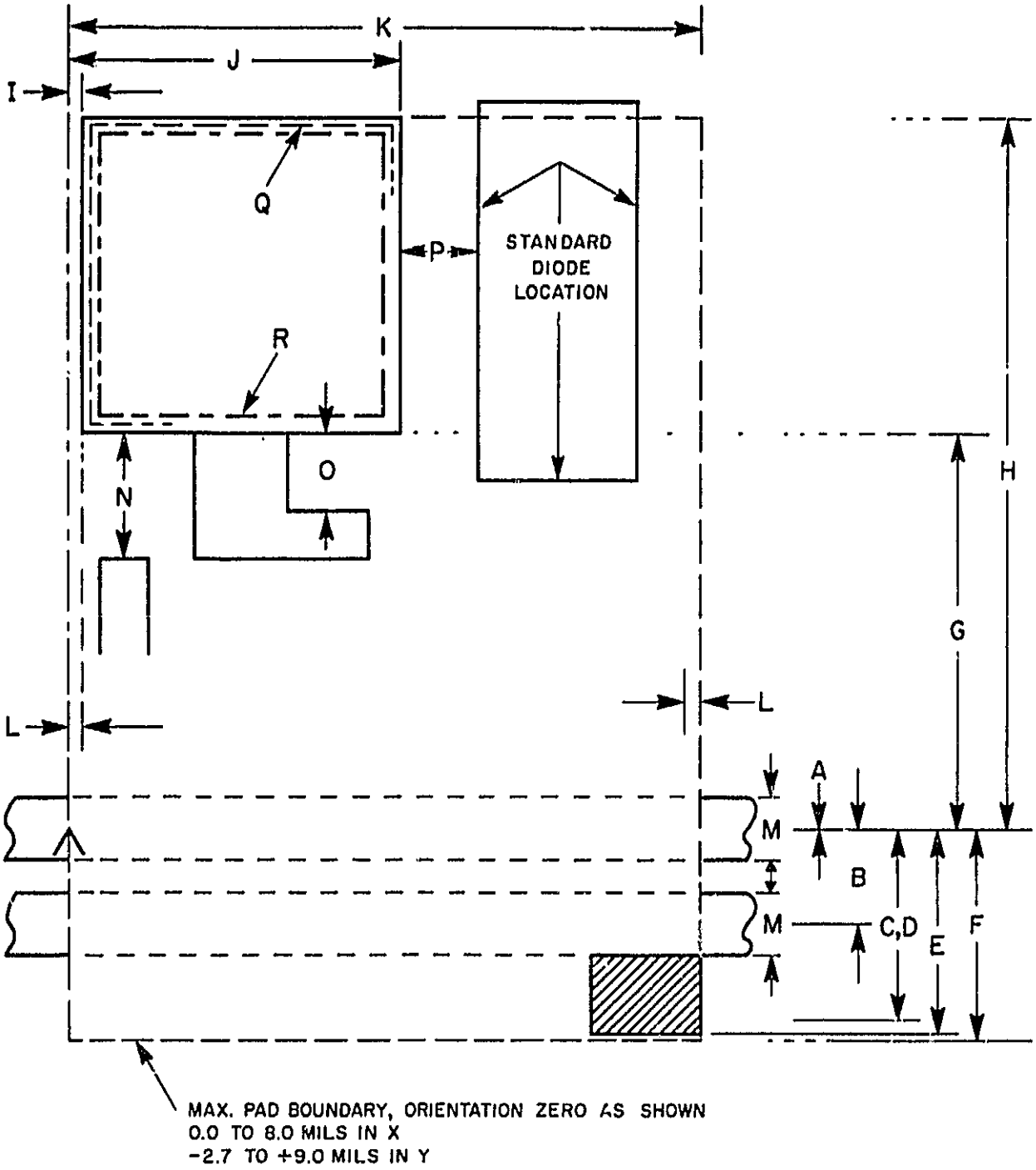
S. Minimum BPM area = 4.0x4.0 mils

T. Minimum bonding pad area to bonding pad area (adjacent cell) = 4.0 mils
(Guaranteed by Rule K and standard format with bonding pad cells)

U. Top of bonding pad metal to edge of street (chip border) = 1.6 mils

*For conformity to existing cells

## Standard FR2D and MP2D Bonding Pad Cell Rules



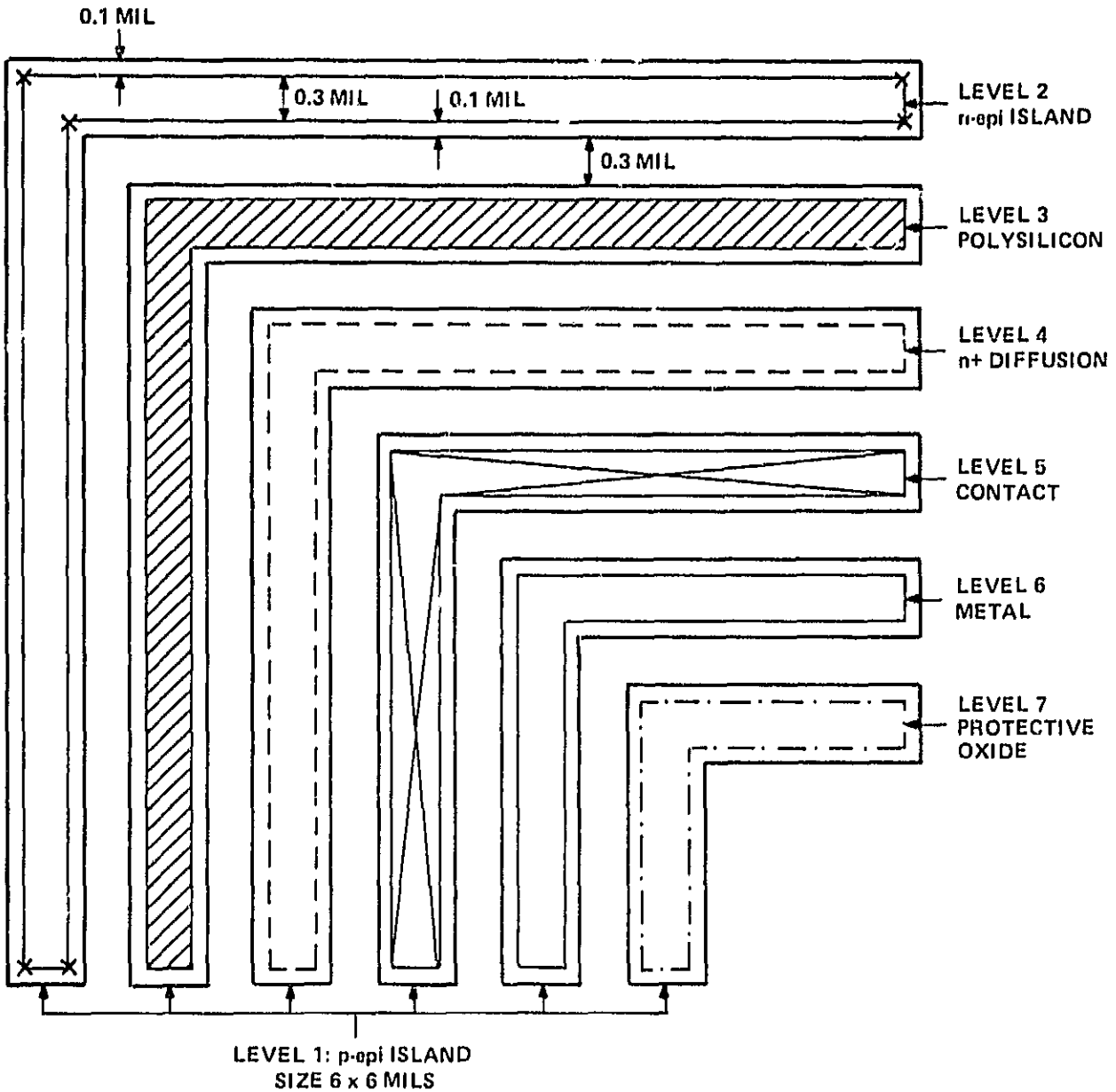

NOTE:

CARET INDICATES CELL ORIGIN

INTERNAL CELL METAL FORBIDDEN. THIS AREA IS RESERVED FOR CONNECTION OF PERIPHERAL POWER BUS TO CELL ROWS.

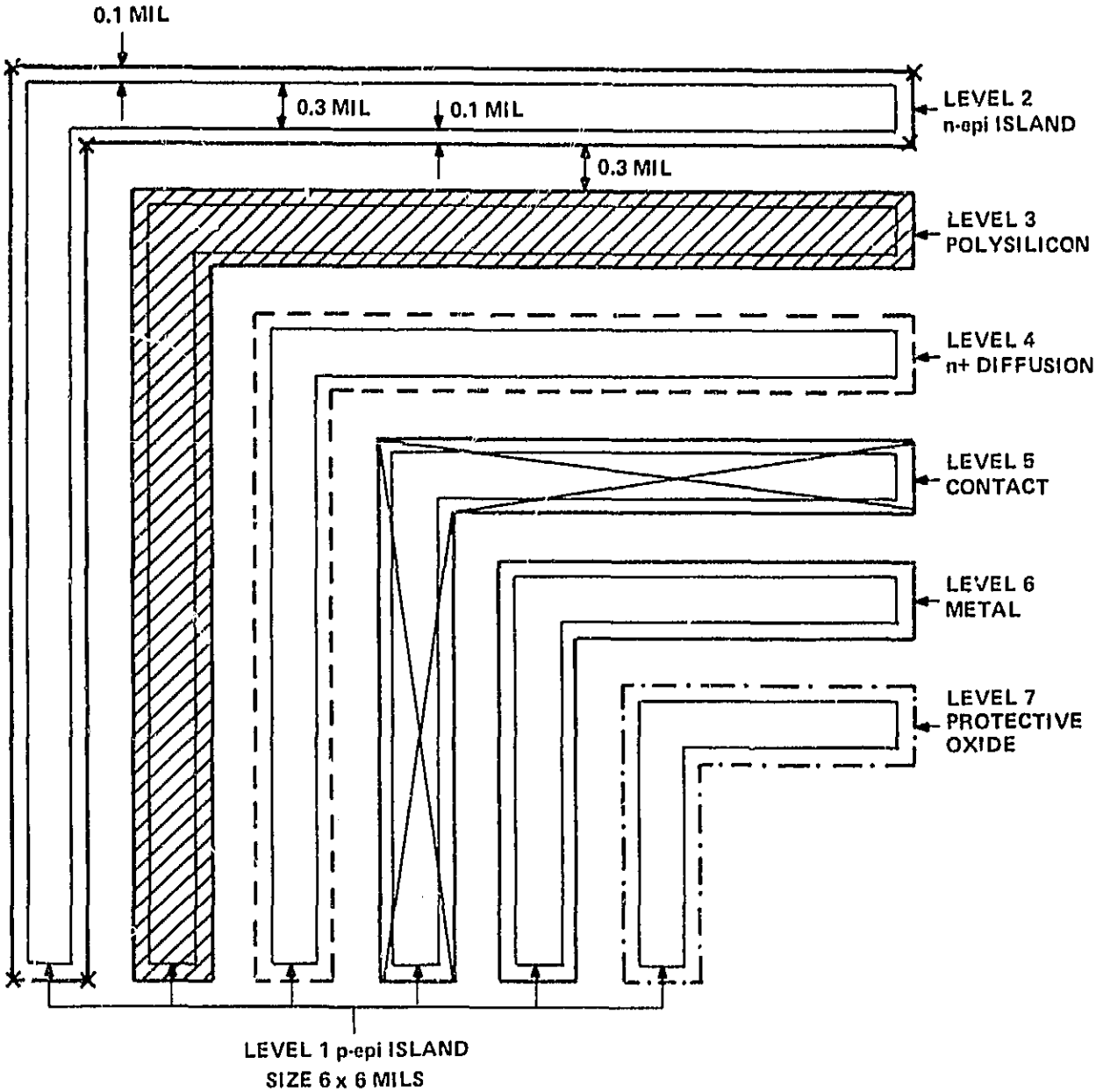
## Light Field Alignment Key

The initial alignment key of level 1 is larger than forthcoming key for light field photo mask.



## Dark Field Alignment Key

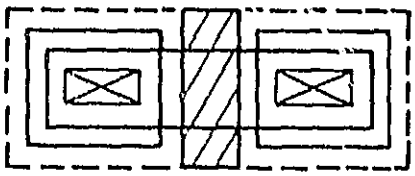
The initial alignment key of level 1 is larger than forthcoming key for dark field photo mask.



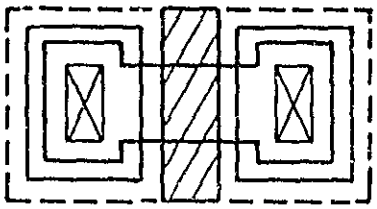
## Small Transistor Layout

In order to comply with the design rule, it takes a special layout for a small transistor ($0.3 \leq W \leq 0.6$ mil). Two layout examples of small n-channel transistors are shown below. Similar layout can be applied to small p-channel transistors.

$0.4 \leq W \leq 0.6$



$0.3 \leq W \leq 0.5$



## Section IV

## CONCLUSION

This report provides a set of CMOS/SOS design rules for a series of RCA compatible processes. By designing with the n-epi and p-epi islands as separate levels, masks developed with these rules maintain complete universality for all major SOS processes at RCA. Among these processes are the $I^2(N/N)$ process (used for the NASA Standard Cell Family) and the RCA Radiation Hardened process.



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