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DIGITAL PHASE-LOCKED LOOP DEVELOPMENT AND APPLICATION TO LORAN-C

A digital phase-locked loop has been developed and implemented for use in a low-cost Loran-C receiver. This paper documents the DPLL design and application to Loran-C.

by

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I. INTRODUCTION

A digital tracking filter for a Loran-C envelope manipulation receiver is presented. A first-order, increment or decrement, CMOS, counting-type of circuit is arranged to generate an 8-pulse replica of the average phase of the Loran-C signal compared to a delay and add type of envelope detector output. A common offset clock oscillator of 1 MHz drives three similar loops locked to a master and two slave stations. A slow-fast circuit allows manual or computer-controlled positioning of the loops for initial signal acquisition. Tracking precision is limited by the RF front-end envelope detector used to about ± 1 microsecond for S/N ratios above 0 dB in a 20 KHz input bandwidth.

II. DIGITAL PHASE-LOCKED LOOP CONCEPT

A. Implementation of the 4029 and 4013. The basic loop is a simple circuit (see Figure 1). The 4013 (type D flip-flop) functions as a phase detector and the 4029 (presettable, up/down, BCD/binary counter) as an increment counter or decrement counter, respectively, depending if the 1 MHz clock is offset negative or positive.

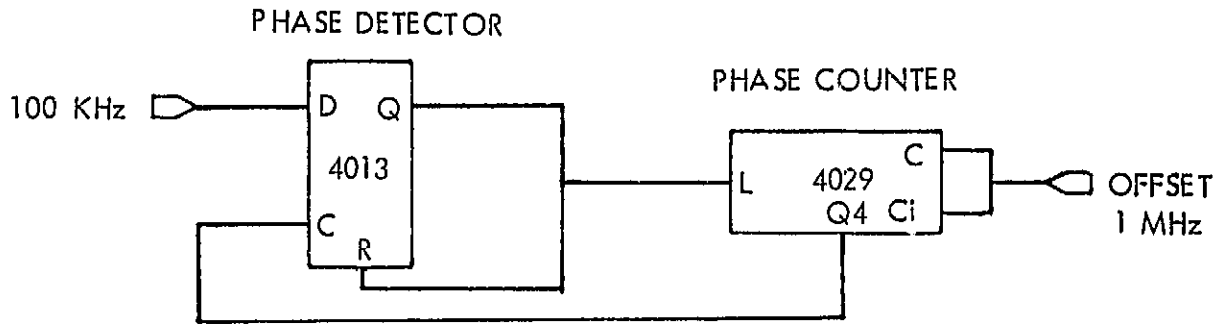
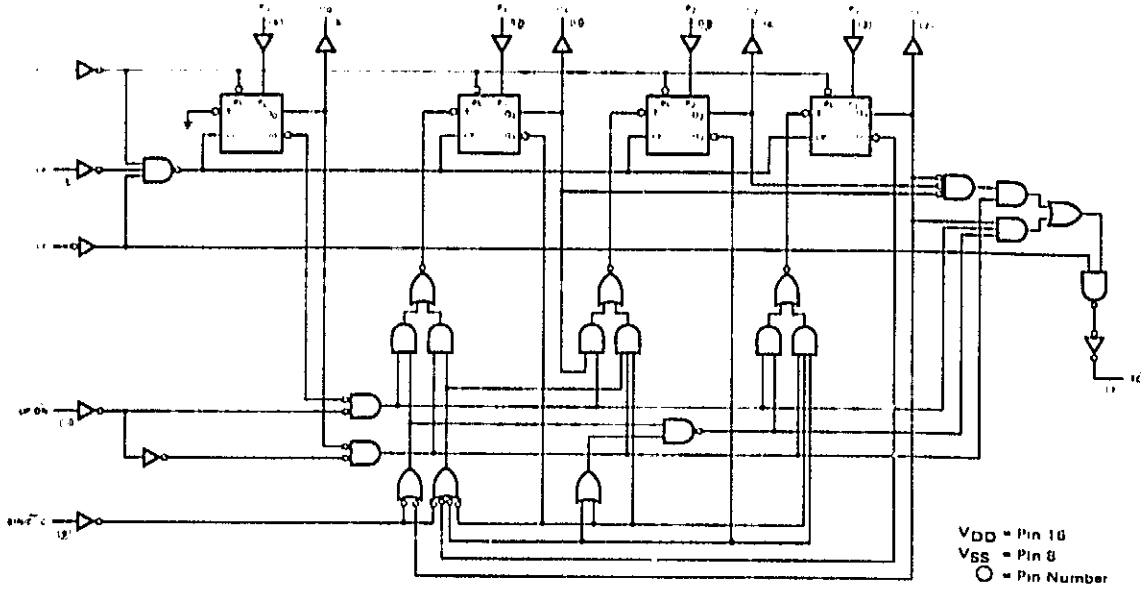


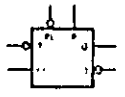
Figure 1. Basic Digital Phase-Locked Loop.

The present enable, sometimes labeled as the parallel load input, can be used to add or eliminate pulses of the offset 1 MHz clock until the offset is eliminated and exactly 1 MHz is obtained and counted by the 4029. As a result, the output Q4 is exactly 100 KHz and is in phase with the desired 100 KHz because the 4013 only generates a correction pulse when the two frequencies are in phase. The circuit of Figure 1 will track input frequencies on either side of the reference clock depending on the programming of the 4029.

III. DETAILED EXPLANATION OF THE DIGITAL PHASE-LOCKED LOOP

A. Working with the 4029. To understand how the 4029 is capable of deleting or adding pulses to correct for the offset of the 1 MHz clock, one must study the internal logic of the integrated circuit (see Figure 2).





$\overline{PL}$ (Parallel Load Input) – Asynchronously Loads P into Q, Overriding all Other Inputs
P (Parallel Input) – Data on this Pin is Asynchronously Loaded into Q, when $\overline{PL}$ is LOW Overriding all Other Inputs
$\overline{T}$ (Toggle Input) – Forces the Q Output to Synchronously Toggle when a LOW is Placed on this Input.
CP (Clock Pulse Input)
Q, $\overline{Q}$ (True and Complimentary Outputs)

Figure 2. Logic Diagram of a 4029 [1].

The specific point of interest is the function of the three input NAND gate driven by the inverted inputs labeled PL (preset enable or parallel load input), CP (clock pulse), and $\overline{CE}$ (clock enable). Because the preset enable, clock pulse, and clock enable are nanded together, the preset enable can function as a clock enable as well as a preset enable when the clock pulse and clock enable are driven by the same source. It is by operating in this manner that pulses can be added or deleted.

A pulse can be injected if in the course of time the clock and clock enable are low and the preset enable goes from a low to a high, then to a low again. The output of the NAND gate produces a complement of the PL, this in turn presets the programmed number of the counter and advances the counter by one count. (See Figure 3.)

Similarly, a pulse can be deleted if,during the time the PL is high, the clock pulse and clock enable go from a high to a low and then to a high again. The deletion occurs due to the fact that the internal flip-flops are continuously preset during the changes from their programmed number and, therefore, the incoming clock pulse is effectively ignored. (See Figure 4.) Because of the logic involved with the preset enable, clock pulse, and clock enable, the designer has the option to develop and use several variations. Some workable variations will be discussed in Section IV.

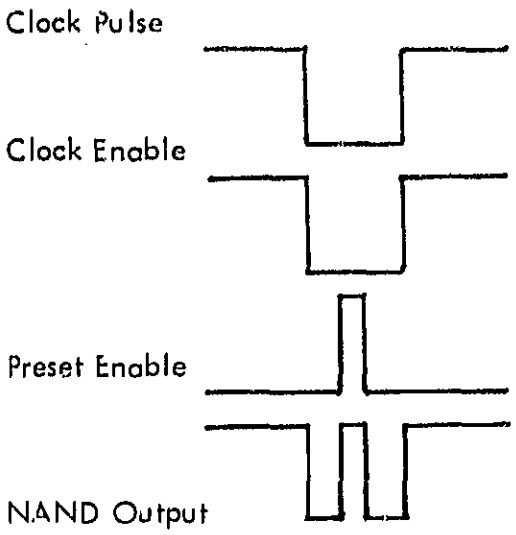


Figure 3. Pulse Injection.

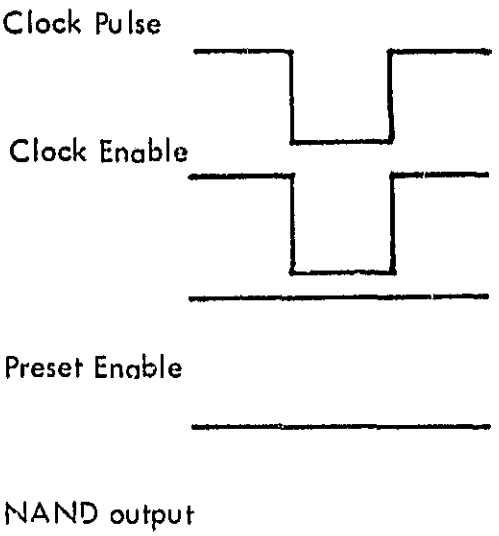


Figure 4. Pulse Deletion

B. Obtaining More Control with the 4013. Because the length of the output of the 4013 is very small (i.e., only one propagation delay), the preset enable of the 4029 can have problems recognizing a correction pulse. In order to lengthen and significantly improve the square shape of the correction pulse, a network of a resistor, diode, and capacitor is added to the output of the 4013 [2]. The network allows the 4013 to function very much like a monostable (see Figure 5). This simple addition of circuitry gives a high degree of control over the deletion and injection of pulses and also creates a pulse the 4029 can easily recognize.

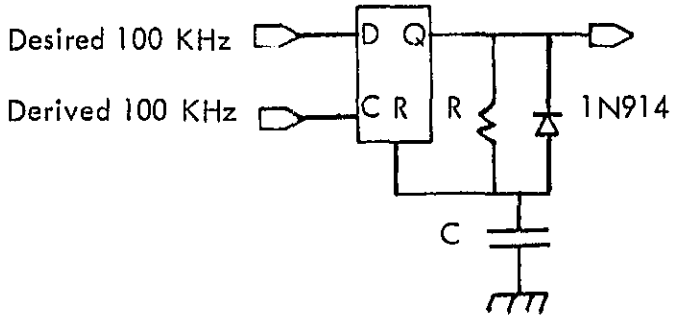


Figure 5. 4013 with Monostable Output.

If the deletion of pulses is desired, then the correction pulse should be slightly greater than the period of the 1 MHz clock. In this case, the correction pulse should be greater than one microsecond in width.

If the injection of pulses is desired, then the correction pulse should be smaller than one-half microsecond so the chances of injecting a pulse are greater. The length of the pulse must not be made too small, otherwise problems will arise with the 4029. A correction pulse that is too short would not allow enough charge or discharge time

for the reset capacitor. The pulse width is also limited by the relatively slow speed of the CMOS 4029 logic.

IV. VARIATIONS OF THE DIGITAL PHASE-LOCKED LOOP

A. Using the Clock Enable. One of the most obvious variations would be to ground the preset enable, feed the correction pulses into the clock enable, and feed the 1 MHz clock into the clock pulse input. This appears to be the most logical approach, in that pulses are injected or deleted by enabling and disabling the clock input. However, as stated before, upon studying the internal logic of the 4029 one finds that the preset enable plays just as important a part in enabling the clock as the clock enable. The only difference in operating with the clock enable is that the counter continuously counts up or down depending upon the programming of the UP/$\overline{\text{DOWN}}$ input. Figure 6 works under the principle of pulse injection and, as a result, has the 1 MHz clock offset one to five cycles low.

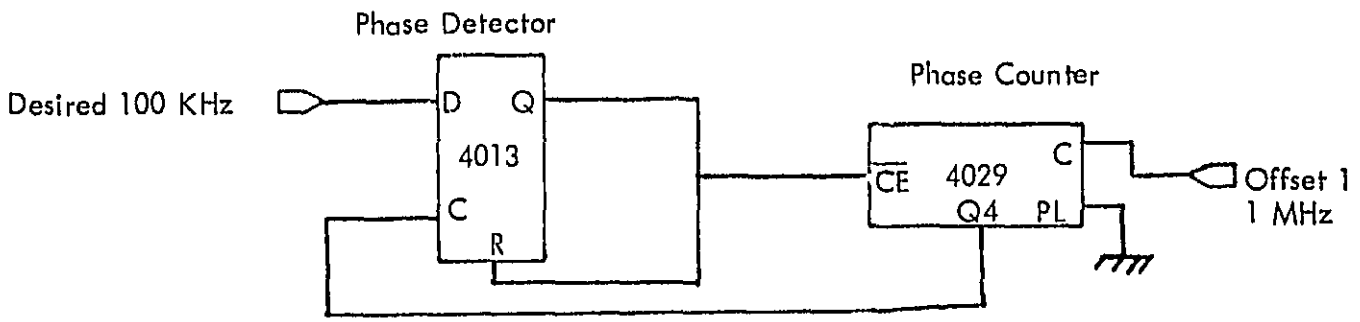


Figure 6. $\overline{\text{CE}}$ Variation of DPLL.

B. 1 MHz Clock Offset. Clock offset is another point of consideration. Is it better to offset the clock high or low? The answer can be found only by considering the application for which the loop is to be used and experimenting with the loop until the proper design has been found. Parameters that may be varied in conjunction with the offset include the programming of the UP/$\overline{\text{DOWN}}$ input, programming of the parallel data inputs, use of the monostable network (which is highly advisable in any case), and varying the RC parameters, or pulsewidth.

4029 4510

Figure 7. Pin Diagram of 4029 and 4510 [1].

C. Using the 4510. Another option is to use a different counter chip. The 4510 is an excellent chip to use to replace the 4029 due to the fact that pin-for-pin the two chips are almost exactly the same. The difference lies in the fact that the 4510 has a master reset in place of the BINARY/DECADE input. Fortunately, if the identical programming for the 4029 is used for the 4510, the 4510 will function exactly as the 4029. The loop might function slightly better because the 4510 is a newer chip than the 4029 with buffered outputs. Using the 4510 also offers another option for an input for the correction pulses. It appears to be possible to use the MR (master reset) to receive the correction pulses as the MR also enables and disables both the clock and the preset enable, thus the MR also has control of injecting or deleting pulses.

V. DIGITAL PHASE-LOCKED LOOP APPLIED TO LORAN-C

One variation of this digital phase locked-loop has been applied to developing a Loran-C prototype receiver at Ohio University. The loop is designed to track a synthesized eight pulse train to a train of eight IRQ pulses. The IRQ pulses are derived from the actual Loran signal at the receiver's RF front end [3].

The Loran-C DPLL can be broken down into five interrelated systems. In addition to the phase detector and counter of the actual loop, a GRI generator, eight pulse generator, and integrator are required.

A. GRI Generator [4]. The Group Repetition Interval (GRI) generator consists of four 4029's cascaded together (see Figure 8). The 4029's are programmed to produce a single pulse (seven to eight microseconds in length) with the same period as the desired Loran chain.

The programming of the first stage of the GRI generator allows the operator of the receiver to speed up or slow down the loops by dividing the incoming 100 KHz by either 9 (to speed up), 10 (to cause no change), or 11 (to slow down). This allows positioning of each loop to agree with the incoming Loran signal. The remaining three stages are programmed to count down from the Loran GRI number set at the GRI switch. If the switch is set for 996, the final three stages will count down from 996 using the 10 KHz signal and effectively count the desired period of 99600 microseconds.

The Terminal Count (labeled Ca in Figure 8) of the MSD of the GRI generator is fed into the same type of monostable network used with the phase detector of the original DPLL. The network is used to obtain control over the length of the GRI pulse for external microprocessor applications. The pulse from the monostable is then inverted and fed to the preset enables of the 4029's controlled by the BCD switches. The pulse is then inverted again, so that a short time delay exists between the GRI pulse and the preset enable pulse, and is fed into the eight pulse generator.

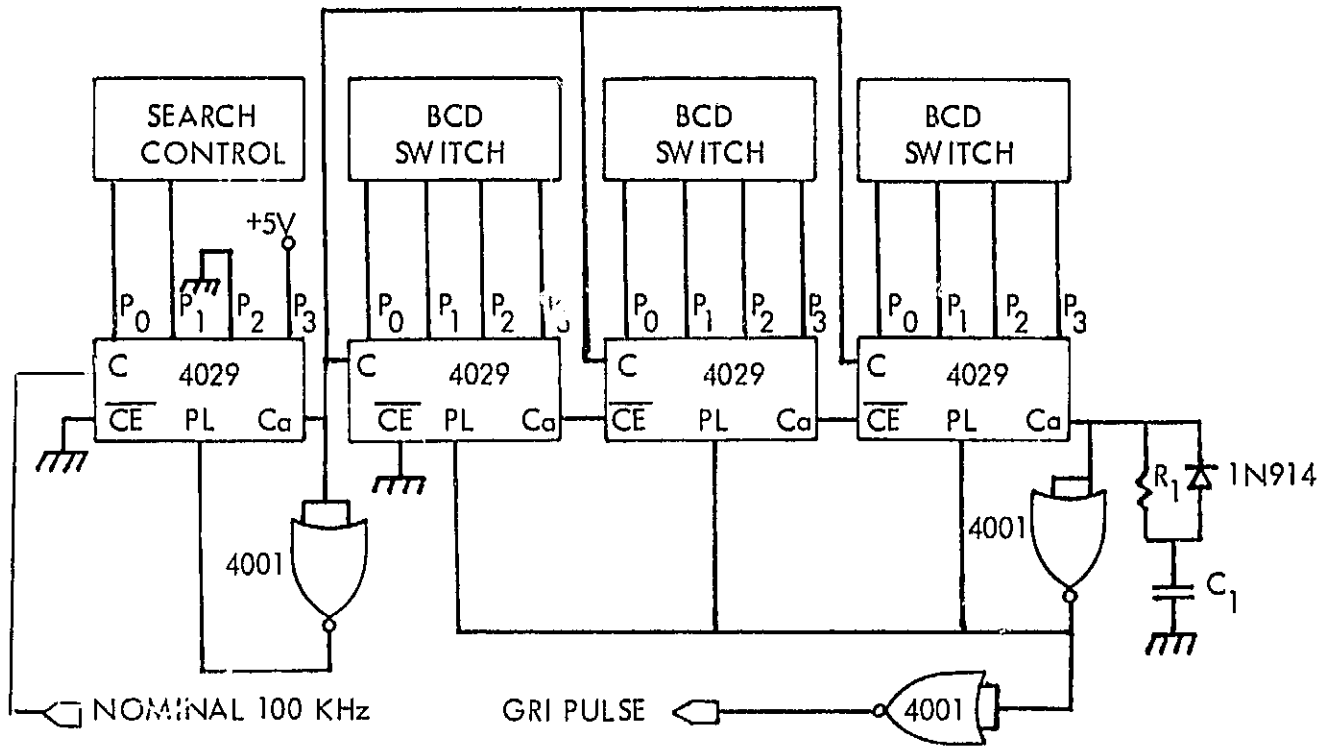


Figure 8. GRI Generator

B. Eight Pulse Generator. The GRI pulse, fed to the clock input of the 4013, is used to activate the eight pulse generator (see Figure 9). When the flip-flop is set, the 4001 is enabled and allows the 1 KHz signal (generated by the second stage of the GRI generator) to pass through the 4001 and at the same time be counted by the 4017. The 4017 counts up to eight and resets the entire eight pulse generator. As a result, the system feeds a synthesized eight pulse train to the phase detector everytime the generator receives a GRI pulse. The eight pulse train will be delayed, after the GRI pulse, 100 microseconds times the LSD of the GRI switch. For example, if the GRI switch is set for 993, the eight pulse train will occur 300 microseconds after the GRI pulse. This is due to the GRI pulse resetting the GRI generator.

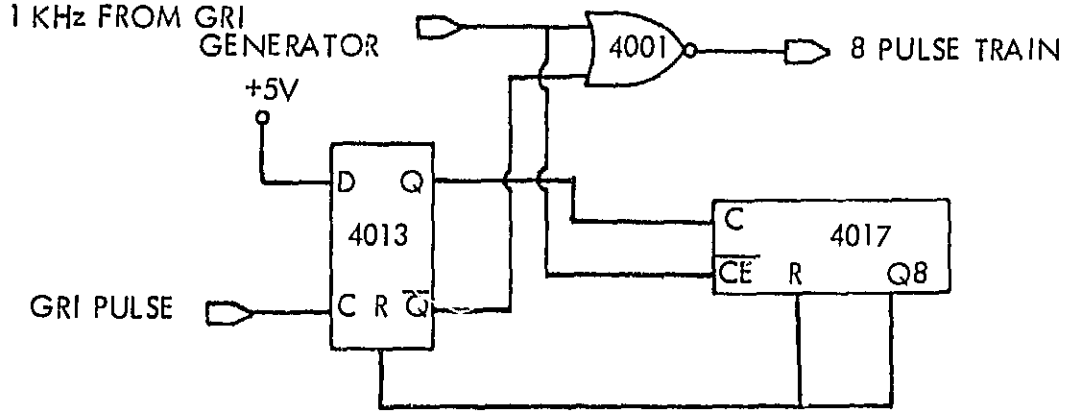


Figure 9. Eight Pulse Generator.

It is very important to note that if the output of the 4001 (the eight pulse generator output) is viewed with an oscilloscope, the train will appear to have only seven pulses. The eighth pulse does exist, but it is only one to two gate propagation delays long. The short pulse is a result of the output of the 4017 directly resetting the eight pulse generator. The short eighth pulse does not create any problems because the clock output of the 4013 (phase detector) is positive edge triggered and effectively ignores the length of the pulse.

C. Correction Pulse Integrator. Using the DPLL to track desired frequencies involved phase comparison and correction of every pulse for every time period. Only one correction pulse could be received for every period of the desired frequency. In dealing with Loran, data is derived from the phase of two eight pulse trains every GRI period. As a result, one could receive as many as eight corrections over the desired GRI period. Since eight corrections every GRI could be too much, and indeed is too much in practice, an integrator is implemented. A 4024 counter, fed directly by the phase detector and driving the monostable network for the phase counter, is used as an integrator (see Figure 10).

By experiment, it has been found that an averaging number (or divide-by number) of 64 works quite well. This allows a maximum of one correction pulse for every eight GRI periods.

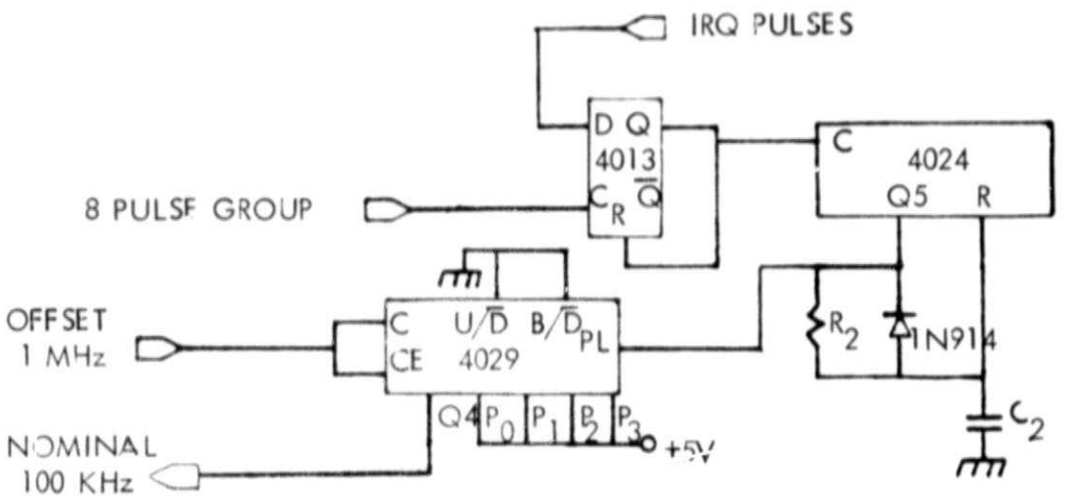


Figure 10. Basic DPLL with Integrator.

The monostable network was added to the output of the 4024 because the PL input of the 4029 phase counter is pulse width sensitive. The network was eliminated from the output of the detector because the input of the 4024 is positive edge triggered.

D. Comments on the Whole System. The Loran DPLL was designed to operate with a 1 MHz clock offset four to five cycles high. The positive offset allows the loop to lock up as early as possible on the signal and, as a result, closer to the desired third cycle of the Loran pulse [4].

The lock indicator circuit, fed by any of the outputs of the 4024 (see Figure 11), can be used to indicate the 1 MHz offset. The recommended output of the 4024 is Q5 (the sixth output stage of the counter) and the recommended offset is approximately 5 cycles.

The integrator (4024) gives a correction pulse for every 64 phase counts; therefore, the LED will flash twice for every correction pulse. In other words, the averaging number for the LED is half the averaging number for the correction pulse. If the clock is offset five cycles high, the nominal 100 KHz will be exactly 100 KHz plus $\frac{1}{2}$ cycle. This comes to five extra cycles every ten seconds or five correction pulses every ten seconds. Because the averaging number provides two flashes for every correction, there will be approximately one flash per second for an offset of five cycles. A similar method could be implemented for determining the offset of a 1 MHz clock if offset negatively.

VI. SUMMARY

The new DPLL has eliminated many of the problems associated with the VCXO type analog loops. Some of the advantages as applied to Loran-C are:

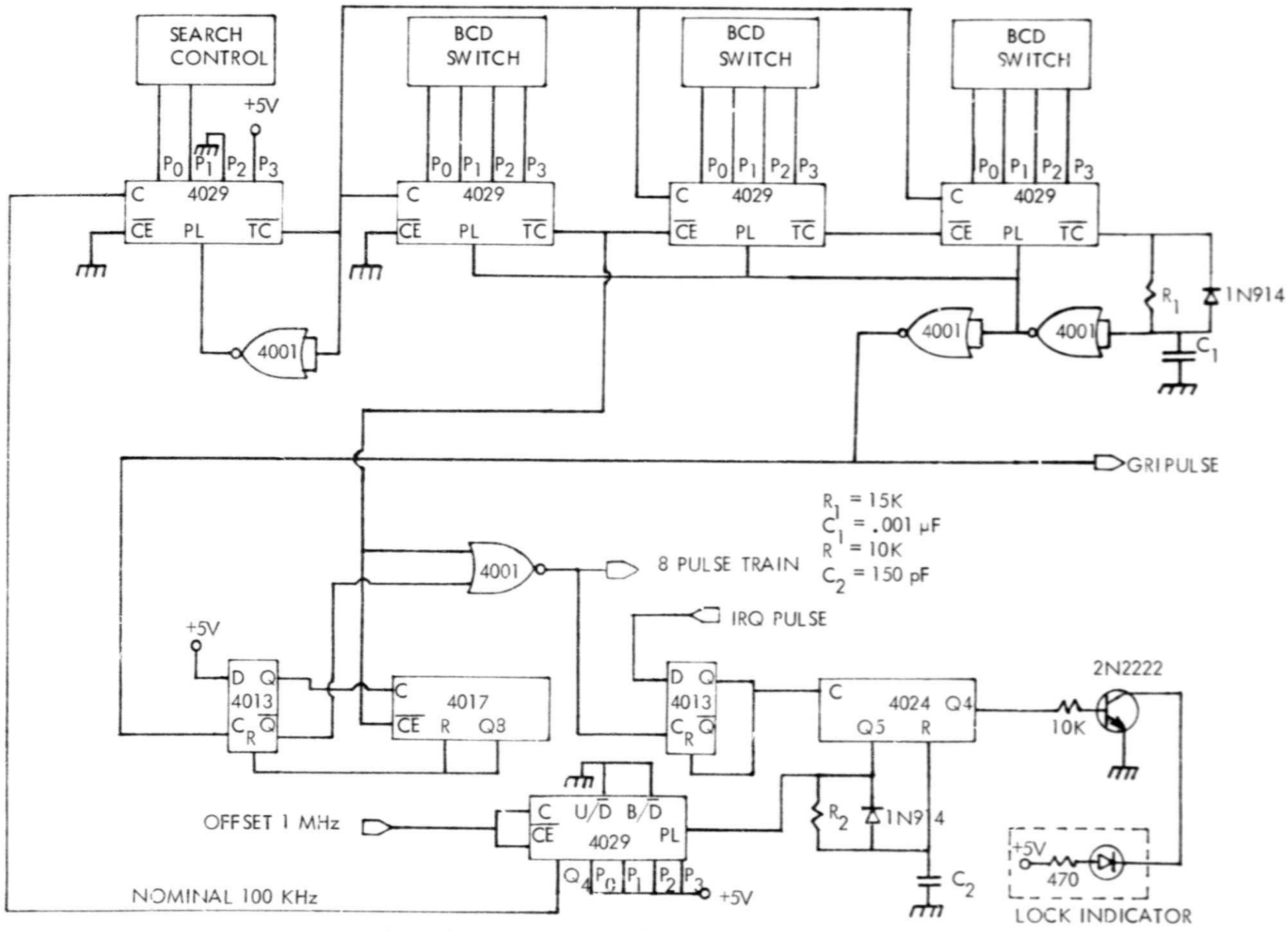


Figure 11. Mini-L 5 Loran-C PLL.

(1) A simple circuit that requires only nine chips.

(2) The DPLL boards require no adjustments.

(3) The three on-board 100 KHz oscillators and the components and adjustments required with them were eliminated.

(4) One central 1 MHz oscillator provides for a common drift rate among the three DPLL boards.

(5) The new DPLL provides for possible auto-sync controls.

(a) UP/$\overline{\text{DOWN}}$ of the 4029.
(b) Monitoring the outputs of the 4024 (integrator).

(6) The DPLL is capable of locking up on low-level signals and remaining locked on standard level signals during periods of severe skywave and spheric interference.

(7) The basic circuit of Figure 1 has application to other types of digital phase-locked loops with longer counting chains capable of tracking offsets as high as $\pm$ 5% of the input signal frequency. A very similar method was applied to one of the early experimental Omega receivers developed at Ohio University [5].

For Loran-C, further improvements could be realized with the addition of a temperature compensated oscillator to use as the offset 1 MHz source.

The Loran-C DPLL described by this report is currently used in a Loran-C prototype receiver at Ohio University. Reports of the receiver's performances will be published later as test flights and data collection allow.

VII. ACKNOWLEDGEMENTS

The DPLL is a continuation of the development of a low-cost, general aviation, navigation receiver funded by the NASA Tri-University Program. The tutoring by Edwin Jones in the initial phases of the DPLL's design is greatly appreciated. Special thanks goes to Ralph W. Burhans, who has been an endless source of information, advice, encouragement, and without whom the development of the DPLL would not have been possible.

VIII. REFERENCES

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IX. APPENDIX

A. An Early DPLL for Loran-C (without the monostable outputs).

Figure A-1. Mini-L [5] DPLL Board without Monostable Outputs.