

FINAL REPORT
FOR
LINEAR APPROXIMATION SAR AZIMUTH PROCESSING STUDY
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ABSTRACT

Planetary orbiting Synthetic Aperture Radars (SAR's) generate large quantities of radar data which currently cannot be processed without wideband transmission to a ground based processing site. Even then, very expensive computers are required to process the data to full resolution in real time. The quantity of data involved is so large that it is clearly advisable to explore ways of reducing it, either by screening it so that the unimportant data is not processed or by some data reduction processing prior to transmission. The projected trends in digital microcircuit technology indicate that the severe weight, size and power obstacles one encounters when considering satellite-borne SAR processing today will be alleviated considerably during the next decade. Even with these microcircuit advances, however, departures from "ideal" processing, if performance objectives permit them, will provide an additional impetus toward on-board SAR processing, i.e., complexity/performance trades are possible.

One approximation possible and the subject of this study is a segmented linear approximation of the quadratic phase function that is used to focus the synthetic antenna of a SAR. Ideal focusing using a quadratic varying phase focusing function during the time radar target histories are gathered, requires a large number of complex multiplications. These can be largely eliminated by using linear approximation techniques. The result is a reduced processor size and chip count relative to ideally focussed processing and a correspondingly increased feasibility for spaceworthy implementation. This study has developed a preliminary design and sizing for a spaceworthy linear approximation SAR azimuth processor meeting requirements similar to those of the SEASAT-A SAR. The study resulted in a design with approximately 1500 IC's, 1.2 cubic feet of volume, and 350 watts of power for a single look, 4000 range cell azimuth processor with 25 meters resolution.

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SUMMARY

The objective of the Linear Approximation SAR Azimuth Study was to perform a theoretical investigation of the merits of using linear approximation techniques to achieve real time low-cost azimuth processing of Synthetic Aperture Radar (SAR) data acquired by earth orbiting satellites. The study was to be accomplished by formulating a preliminary design of a spaceworthy SAR azimuth processor meeting requirements similar to those of the SEASAT-A SAR. The performance capability of this design was to be analyzed, and information was to be provided on the processor interface requirements, implementation to the chip count level, and processor size, weight, and power.

The guidelines for developing the preliminary SAR processor design were to provide a baseline design capable of 25 meters resolution and 4000 range cells with 4 independent azimuth looks and suitable for use on board future earth satellites. The baseline design was to be adaptable to various sets of requirements including resolution (10 to 200 meters), swath width (10 to 400 km), and number of looks. Also the processor design was to be adaptable to an assortment of radar system parameters such as wavelength and radar/target geometry.

The above objectives were satisfied by the development of two designs using linear phase approximation techniques. The difference between these designs (called Baseline and Improved Baseline) lies in the means of implementing the basic processor operations. The Improved Baseline reduces total processor size by a factor of roughly 3. Both designs meet the performance objectives and parametric curves are presented which describe the impact on processor design of varying SAR system requirements. Specifically the processor impulse response sidelobe levels and processor chip count are given as a function of the number of linear phase approximation segments (i.e., accuracy of phase approximation) for 25 meters resolution. Also, for fixed sidelobe suppression requirements, the resolution is given as a function of the number of segments and the chip count is given as a function of resolution.

The Baseline design represents a straightforward implementation of the original piecewise linear concept where continuous non-overlapping segments are combined to form the full azimuth aperture. This minimizes arithmetic operations by using principally delay and add functions within each segment. Multiplications are used only to provide frequency offsets at the input to each segment and to adjust the phase of the segment outputs. In this way multiplication rates are reduced by a significant factor (i.e., 7 for the Baseline) relative to full convolution. A corresponding reduction in the required number of multiplier chip is obtained. The Improved Baseline design makes use of newly available multiplier/accumulator chips to modify the delay and add function to more sophisticated finite impulse response (FIR) filters. The benefit achieved is a reduction of the total chip count by decimating the sample rate within each channel and making possible the use of high density memory chips. These memory chips would not be compatible with the Baseline design due to the higher required access rates.

The conclusions reached in this study include:

- 1) Anticipated integrated Circuit (IC) developments will make possible spaceworthy SAR azimuth processors for 25 meters resolution, 4000 range cells, and single look.
- 2) Estimated size for such a processor is less than 1500 chips, 350 watts, and 1.2 cubic feet.
- 3) The needed IC developments are high reliability, radiation-tolerant versions of current LSI memory devices.
- 4) Processor sizing will vary in direct proportion to the number of looks and swath size.
- 5) Azimuth processor sizing will vary as the inverse of the azimuth resolution squared for resolutions greater than about 5 times the radar wavelength.
- 6) Multi-look requirements impose a significant increase in the required accuracy of input data needed to perform motion compensation within the processor.

- 7) The truncation noise within the processor can be controlled to within acceptable limits (i.e., -45 to -50 dB relative to signal) by using, 8-bit words at the integrate and dump output and 10 bit words at the output of the moving window integrator.

The areas of recommended further development activity include:

- 1) perform a study to determine the FIR design parameters which optimize processor performance and size, preferable including a laboratory breadboard model,
- 2) conduct further simulations and analysis of the effects of finite word size, truncation, and spectral aliasing within the Improved Baseline processor,
- 3) develop detailed concepts for processor control, reference function generation, and timing, and
- 4) construct a laboratory hardware model of a single look, 25 meter resolution azimuth processor.

INTRODUCTION

This report describes an investigation to determine the merits of using linear phase approximation techniques to achieve real time, low-cost azimuth processing of Synthetic Aperture Radar (SAR) data acquired by earth satellites. The work reported here was done by Lockheed Missiles and Space Company, Sunnyvale, California, under the direction of the California Institute of Technology's Jet Propulsion Laboratory, Pasadena, California, under contract 955072.

Section 1 of this Final Report describes the linear approximation concept. It establishes the background and fundamentals necessary to understanding the sections that follow. For clarity, an elementary three segment linear approximation processor is used to describe details of the linear approximation processor operation and signal flow. The effects of phase errors introduced by the approximation on the synthetic array pattern are discussed and illustrated.

Section 2 derives the basic design parameters for an azimuth processor that are necessary to meet the functional requirements and SAR system parameters specified in the contract statement of work. The functional requirements are essentially those associated with a typical earth orbiting satellite SAR and the specific system parameters are based on the SEASAT-S SAR. Design objectives on processor sidelobe performance and processor size are established.

Section 3 presents design considerations and trades that led from a preliminary Baseline design to an Improved Baseline design. The rationale is presented for a reduction in arithmetic and storage requirements in the Improved Baseline processor.

Section 4 presents the implementation details of the two azimuth processor designs down to chip count level. Timing requirements and their match to component device data rate capabilities are established. Details on digital

filtering designs, a critical function in the Improved Baseline Processor, are presented.

Section 5 establishes the requirements for processor control. The auxiliary signal inputs to the processor for this function are identified and the precision of these inputs are derived.

Section 6 provides the estimates on size and power requirements for a space-worthy implementation of the Improved Baseline SAR processor. The preliminary Baseline processor is also sized for purpose of comparison. These data are presented such that estimates for a linear approximation processor meeting other mission or performance requirements can easily be made. Section 6 also presents the expected performance capability of the Improved Baseline processor based on computer analysis and simulation.

Appendix A, which follows Section 6, is a description of an investigation conducted jointly by LMSC and the Institute for Advance Computation (IAC), Sunnyvale, California, into the effects of quantizing noise on the performance of the Linear Approximation Processor. IAC was funded separately by NASA for their portion of this work. An algorithm was developed to simulate the preliminary Baseline processor (the Improved Baseline had not evolved at initiation of this simulation work) in the time domain and to analyze the effects of employing differing digital word sizes at various stages within the processor. The saving of a single bit per word at some stages had a great impact size and cost, and the results of this simulation study were used in the implementation work of Section 4. A description of the simulation methodology and results appear in this appendix. The results, although obtained for the Baseline design, are considered applicable for the Improved Baseline and were applied to that design as well as the Baseline.

Section 1

THE LINEAR APPROXIMATION CONCEPT

The Linear Approximation Concept is an approximation to ideal Synthetic Aperture Radar (SAR) processing originally conceived as a means of trading economy and processing speed against processor sidelobe levels, area coverage, and resolution. The concept to date has been applied only to the azimuth dimension of a SAR image although conceptually, it can be extended to range processing. This approach to SAR processing is based on linear phase approximations to the quadratic phase function required for ideal focusing as shown in Fig. 1-1a. The number and length of linear phase functions (only three shown in the figure) impact the processor complexity and cost, as well as performance. In its simplest form, the array of segments can be made up of an array of unfocused processors (each focused at infinity), but their individual response patterns directed so as to intersect at a specified distance from the radar, the focal distance R . If the center segment of Fig. 1-1a is implemented by an unfocused processor to approximate the phase history as a constant between $-\tau/2$ and $\tau/2$ the resulting phase error at the ends of this segment is $\pi/2$ (Fig. 1-1b). The other two segments of Fig. 1-1a are also implemented by unfocused processors, but the input signal histories to these processors must be modified to have a linear phase progression during the processing intervals between $-t_2$ and $-t_1$ and t_1 to t_2 . This is accomplished by a constant frequency offset (linear phase) applied to the signal phase histories of these segments. This frequency offset must be introduced with a precise phase which is referenced to the center of the segments. The residual phase error for the three unfocused processors following this linear phase correction is as shown in Fig. 1-1b, with $\pi/2$ phase error at the ends of the individual sub-apertures. The three processors each produce a synthetic antenna pattern, with a resolution of $1/2 \sqrt{R\lambda}$ if the maximum unfocused sub-aperture (segment) length $\sqrt{R\lambda}$ is used, spaced in time by the sub-aperture integration time T :

$$T = \frac{L_{unf}}{V} = \frac{\sqrt{R\lambda}}{V} \quad (1)$$

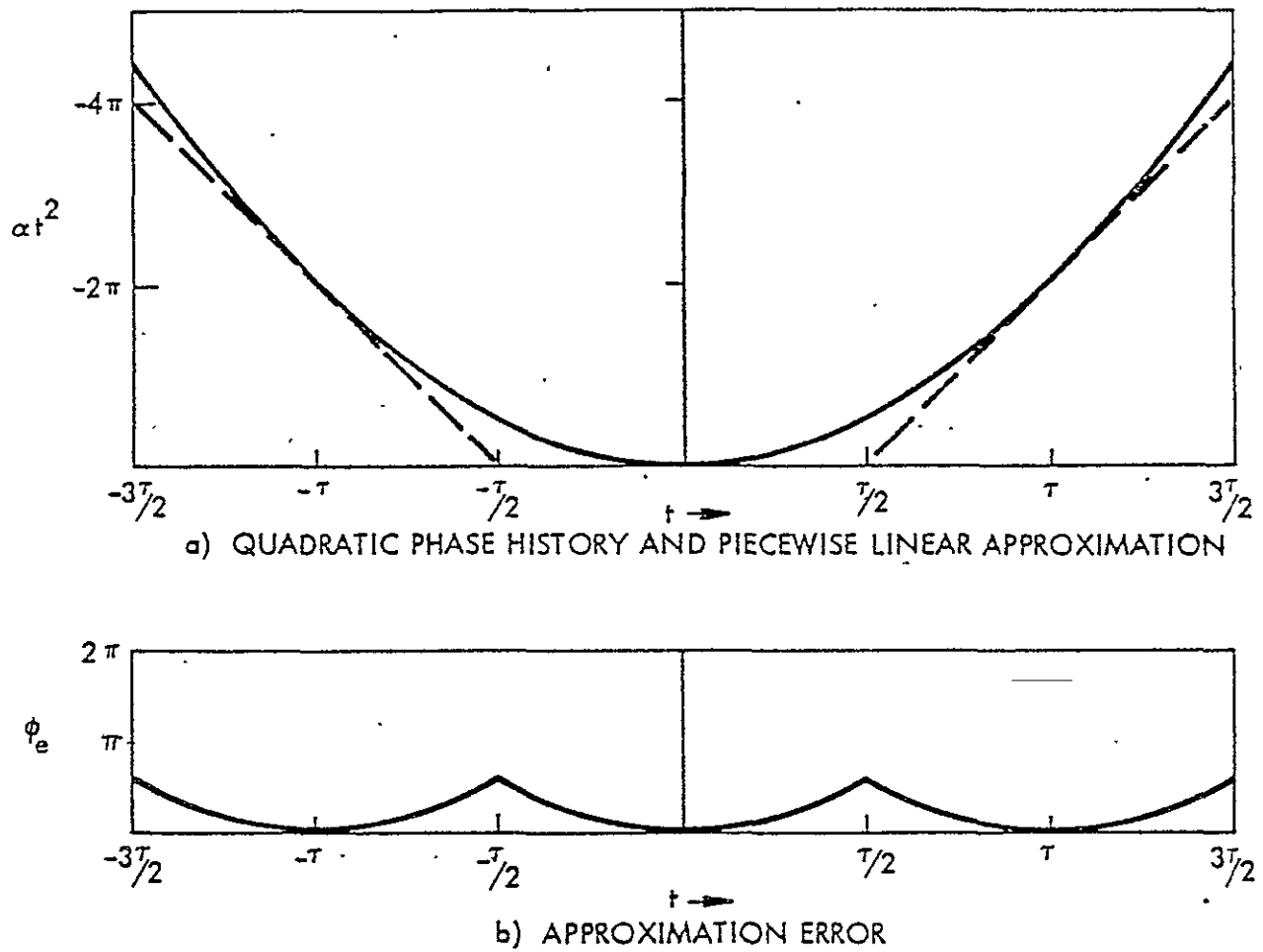


Fig. 1-1 - Piecewise Linear Approximation for Phase History

Output samples from the sub-aperture processors are aligned in time and summed to produce a pattern for the total synthetic aperture, now consisting of the three sub-apertures (unfocused processors), or a total length $3\sqrt{\lambda R}$. The new azimuth resolution now is,

$$\Delta Az = \frac{\lambda R}{2L_{\text{total}}} = \frac{\lambda R}{2 \cdot 3 \sqrt{\lambda R}} = \frac{\sqrt{\lambda R}}{6} = \frac{L_{\text{unf}}}{6} \quad (2)$$

This concept can be extended to a larger number of segments, other segment lengths, and other segment spacings. While using sub-aperture lengths equal to or shorter than the unfocused processor length is attractive because it minimizes the requirement for sub-aperture phase correction, the concept outlined here can be extended to longer sub-apertures with appropriate phase adjustments. For this introductory discussion, however, attention will be confined to the unfocused processor length and, for simplicity, to the three segment concept.

A key feature of the Linear Approximation azimuth processor is that it forms the quasi-focused synthetic array beam by repeated use of elementary signal processing functions, namely frequency translation and finite window integration. Taken together, these functions are equivalent to that of cross correlating the received signal against an appropriately chosen reference function. The nature of the signal waveform and the three segment reference function are illustrated in Fig. 1-2. The chirp-like character of the return from a point target, after frequency translation to baseband, is shown (a) with zero frequency occurring at the midpoint in the signal history. Only the in-phase or "real" component is shown. The in-quadrature or imaginary component, also used in the processor, has a similar character but with zero amplitude near zero frequency. The correlation reference function corresponding to a three-segment Linear Approximation processor is shown in (b). The constant value of the reference function in the midsection provides pure integration over a finite time window, while the two end sections provide both frequency translation and integration over a window equal in length to the center segment. The frequency translation can be thought of as producing forward and aft squinted beams for these sub-apertures.

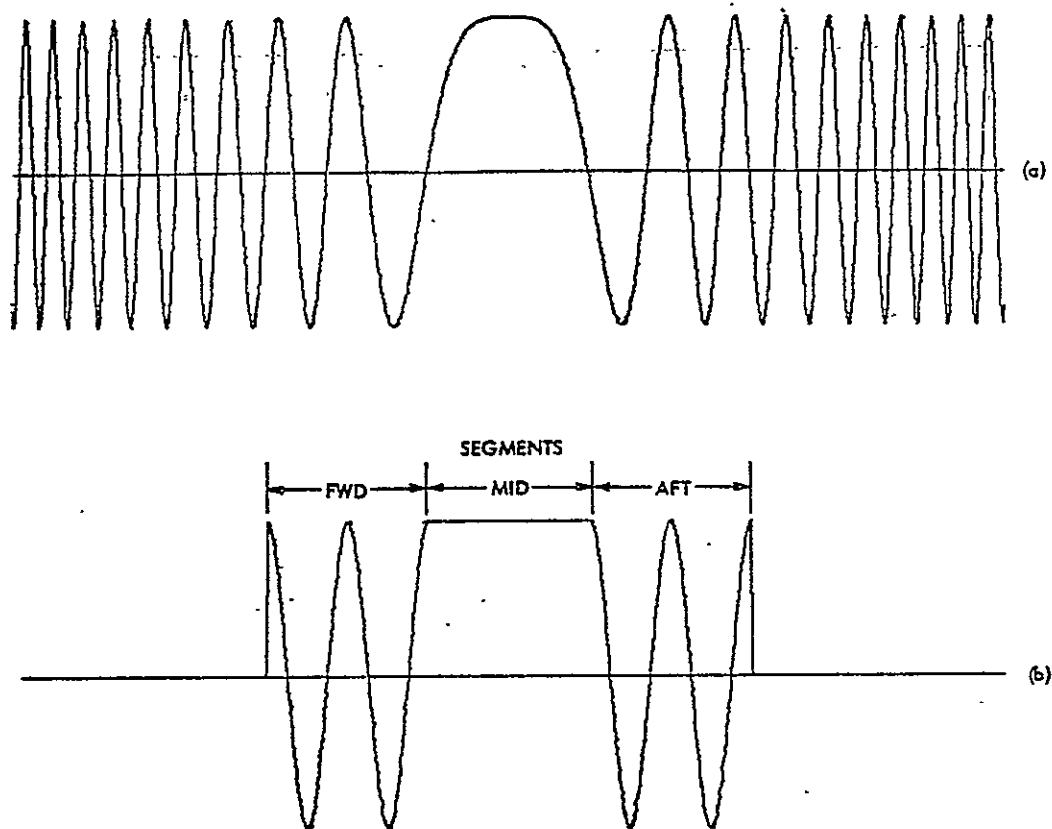


Fig. 1-2 - Point Target Signal History (a) and Effective Reference Function for A Three Segment Processor (b)

The architecture for the basic three segment processor is shown in Fig. 1-3, which shows the makeup of the three segments required for processing the in-phase (I) component of the SAR output signals. A similar configuration is necessary for the quadrature (Q) component. The input signal is complex (I and Q) range compressed radar returns. The six functions performed in each segment as shown, are:

- o Frequency Offset which translates the doppler spectrum containing the phase history of interest down to baseband. The center or zero squint segment is assumed centered at zero doppler and requires no translation.
- o Recirculating Integration which integrates radar returns from each radar range cell of interest over a period equal to one sixth of the unfocused processor integration time. (From equation 2, six outputs must be produced during the time the SAR moves the length of an unfocused aperture). This is essentially a low-pass filtering process that separates the doppler signal of interest to a given segment from the common input signal to all segments.
- o Moving Window Integration which performs a continuing summation on the most recent six outputs from the recirculating integrator. The result is an output of radar returns over the full unfocused aperture delivered every $T/6$ seconds.
- o Phase Shift which restores the proper phase relationship between successive outputs of the Moving Window Integrator such that they will combine properly with the outputs from the other segments. This operation is required in the forward and aft segment channels to provide phase continuity across the entire three segment synthetic aperture. This function can also be regarded as a frequency translation which restores the integrated target energy to its original spectral location within the doppler band from baseband.

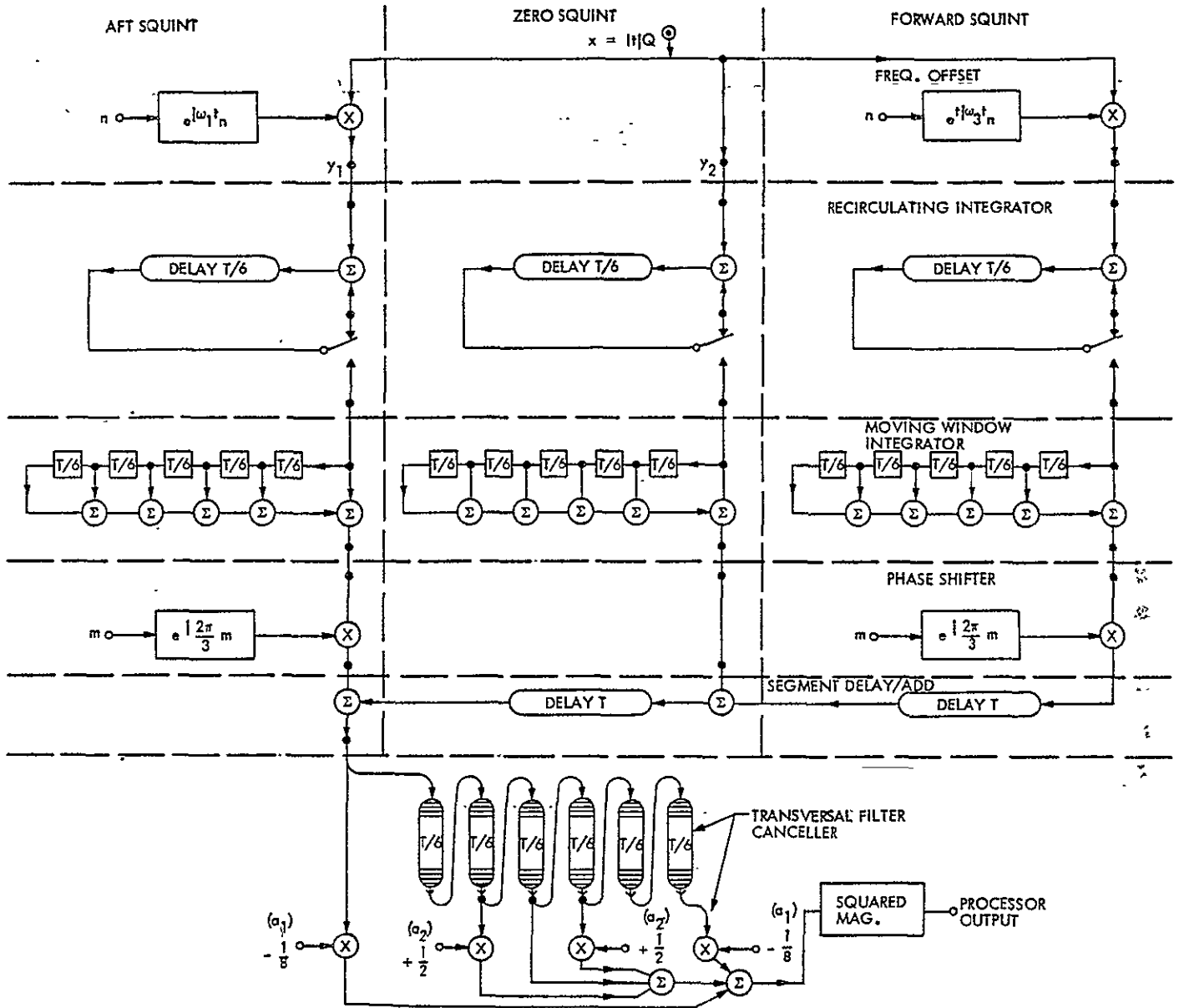


Fig. 1-3 - Basic 3-Segment Processor

- o Segment Delay which aligns the outputs from the three segments prior to summation. Since the synthetic beams from the three segments are viewing a target scene in successive integration periods as the SAR passes the scene, the segment outputs for the same targets are separated by the same period. The forward segment produces outputs that must be delayed $2T$ and the center segment outputs delayed T in order for them to be aligned with the output from the aft segment.
- o Segment Addition which is accomplished along with the segment delay as shown in Fig. 1-3. The summed outputs from the three segments constitutes the output from the three segment I channel. Pixels for each resolution cell are formed by summing the squared values of the outputs from the I and Q channels.

The signal flow through the forward squint segment of Fig. 1-3 is shown in Fig. 1-4. The upper signal plot shows the in-phase component as a solid line with the offset frequency as a dotted line. The output of the mixer at Y_3 is shown next as what appears to be a time shifted version of the original in-phase component of the input signal because of the $\pi/2$ phase difference between the original signal and the offset waveform $\cos \omega_s t$ at $-\frac{T}{2}$. The integrate and dump action of the recirculating integrator is next shown with the build-up signal at X_3 and the output at Z_3 with an output sample appearing every $T/6$ seconds. The build up of the summation of six sub-segment pulses at U_3 is plotted next in Fig. 1-4; this, for the timing of the processor input signal assumed above, produces a maximum at the end of the segment integration time. The sequence of pulses at U_3 is next weighted by the real part of $\exp(j2\pi/3)$ to produce output V_3 , of the forward squint channel. (The imaginary part of the exponent (a) is used in the Q-channel for this segment.)

The I channel outputs from the zero squint and aft squint segments are shown at the bottom of Fig. 1-4 as V_2 and V_1 , respectively. When V_3 is delayed $2T$ seconds and V_2 is delayed T seconds, the addition of the three segments shown at W results. The plots at the bottom of Fig. 1-4 can be

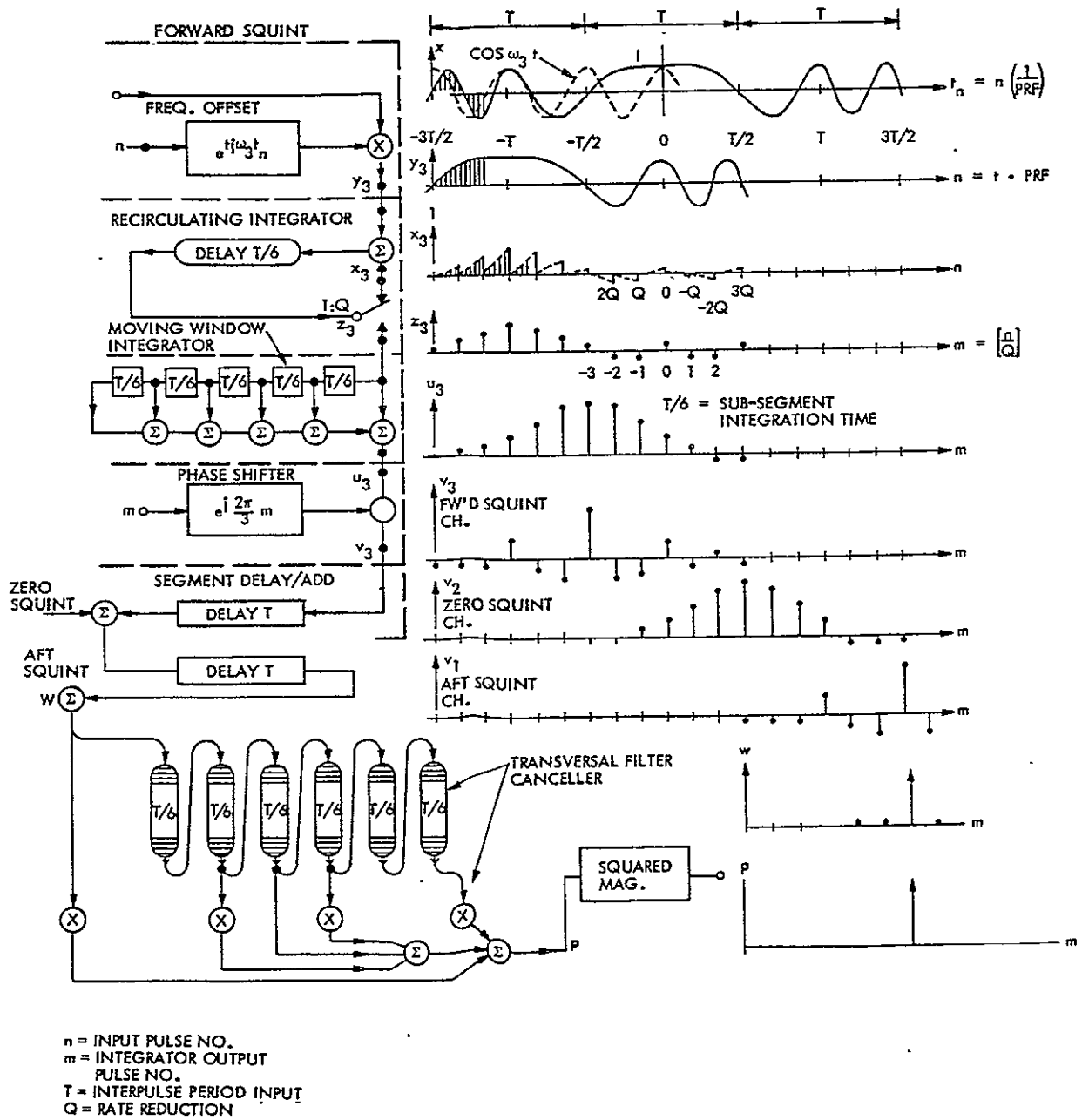


Fig. 1-4 - Basic 3-Segment Processor Signal Flow

used to visualize the cancellation of all pulse outputs from the three segments with the exception of one pulse representing the real channel energy in a resolution element of size $VT/6$. The energy in the same resolution element processed by the quadrature channel is combined with the signal at W to produce a SAR-processed result that is proportional to the radar cross section of that resolution element.

To understand the need for the phase shift multiply just ahead of the alignment delay, consider first the action of the sub-array (segment) processors on either side of the zero-squint segment for the case of two-point targets, one exactly on the array boresight axis and the other displaced from it. The solid and dashed circles in Figure 1-5 represent the wavefronts at the array associated, respectively, with targets (1) and (2). The phase compensation provided by the three sub-arrays is represented by the three solid, straight-line segments. Because each of these segments is a best-fit linear-segment approximation of the wavefront of target (1), maximum response for the entire array will be obtained by integrating over each of the segments and then linearly adding their outputs with zero additional phase shift.

Consider now the segment response to target (2). In order to realize the same overall processor action as that just described for target (1), the phase compensation function would ideally be that shown by the dashed line segments. But because the squint offset oscillators run continuously (as indicated by the dotted extensions of the solid-line segments), the compensation actually is still that represented by the extended solid line segments. Consequently, there is now an error $\Delta \phi$ in the phase compensation, negative for the left segment and positive for the right segment (see Figure 1-5). In order to achieve maximum response for the second target, a positive phase shift $\Delta \phi$ must be introduced into the left segment and an equal negative phase shift into the right segment. The amount of phase correction required increases in proportion to target displacement from boresight, and likewise for array segments at greater distance from the center (zero-squint) segment.

Since the amounts of phase shift required depend upon target position in the target field, the phase shifters must step through a series of values to cover a given field. Thus, the overall action of the processor is analogous to that of a phase-shift-scanned array antenna with the squinted segments playing the role of the elements of a conventional array antenna. Alternatively, the effect of the progressive phase shift increments applied to the segment processor output can be regarded as a frequency offset. It can be shown that this offset is just the negative of the squint frequency offset. This latter point of view is taken later in this report in the discussion of the improved baseline design.

An imperfect cancellation of the pulses near the main response is shown in W (bottom plot of Fig. 1-4). These sidelobes are due to processing limitations inherent even in a fully focussed processor but are more pronounced in the Linear Approximation approach. A reduction of these sidelobes is important not only to minimize the distortion of target images but also to reduce the level of "clutter" at a given image element due to the integrated effect of nearby targets. A measure of this integrated clutter effect is provided by the so-called integrated sidelobe ratio (ISLR) which is the ratio of the energy in the sidelobes to that in the main lobe target response. Figure 1-6 shows the azimuth response patterns obtained by computer simulation for the cases of a point target processed by a synthetic aperture having a single segment (a) and three segments (b). Each segment is of length $\sqrt{\lambda R}$, the maximum length for a single unfocused segment. The width of the main lobe in Fig. 1-6b is one-third that of Fig. 1-6a, as predicted. The prominent sidelobe, two removed from the main lobe in (b) is unique to an aperture that has been segmented. Theoretical analysis has shown that these are attributable to the phase error at the ends of the individual segments ($\pi/2$ for the unfocused case in Fig. 1-6). Shortening the array reduces this phase error as shown in Fig. 1-7. Here the segment lengths have been reduced to $.6 \sqrt{\lambda R}$ and the number of segments increased to five to make the overall array length remain at $3 \sqrt{\lambda R}$ as in Fig. 1-6. The result is a reduction in predominant sidelobes (now 4 out from the main lobe) to -19 dB, down from the -10 dB in Fig. 1-6. The phase error at the ends of the $.6 \sqrt{\lambda R}$ segments is 32.4° .

With this reduction of the sidelobes due to phase error at the segment junctions (side lobes caused by segmented real antennas are referred to as

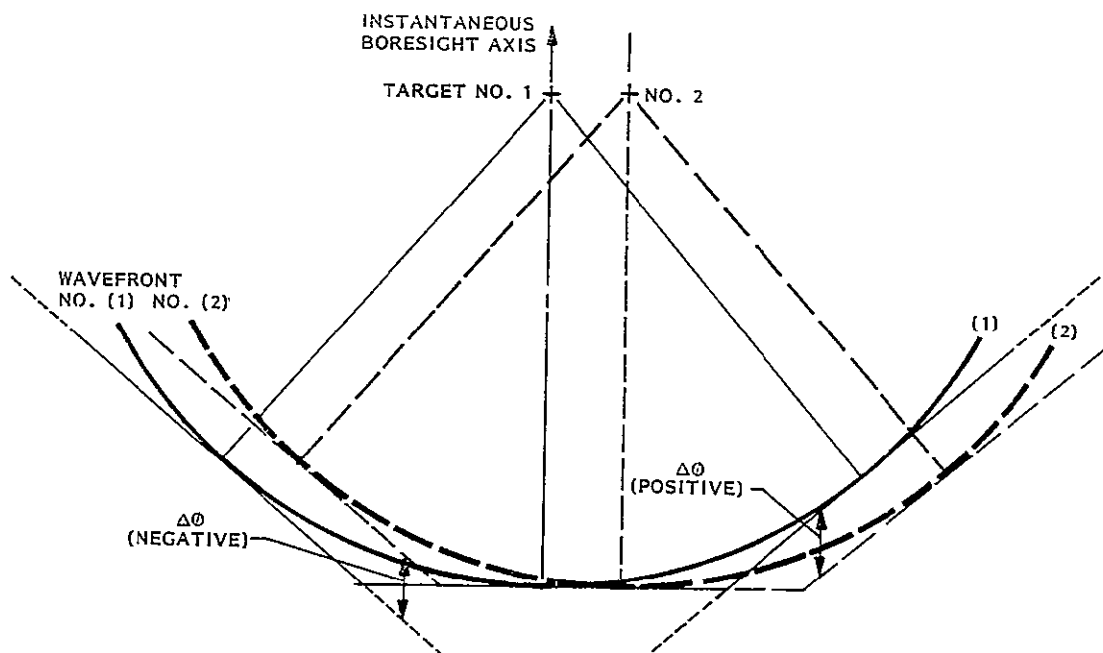
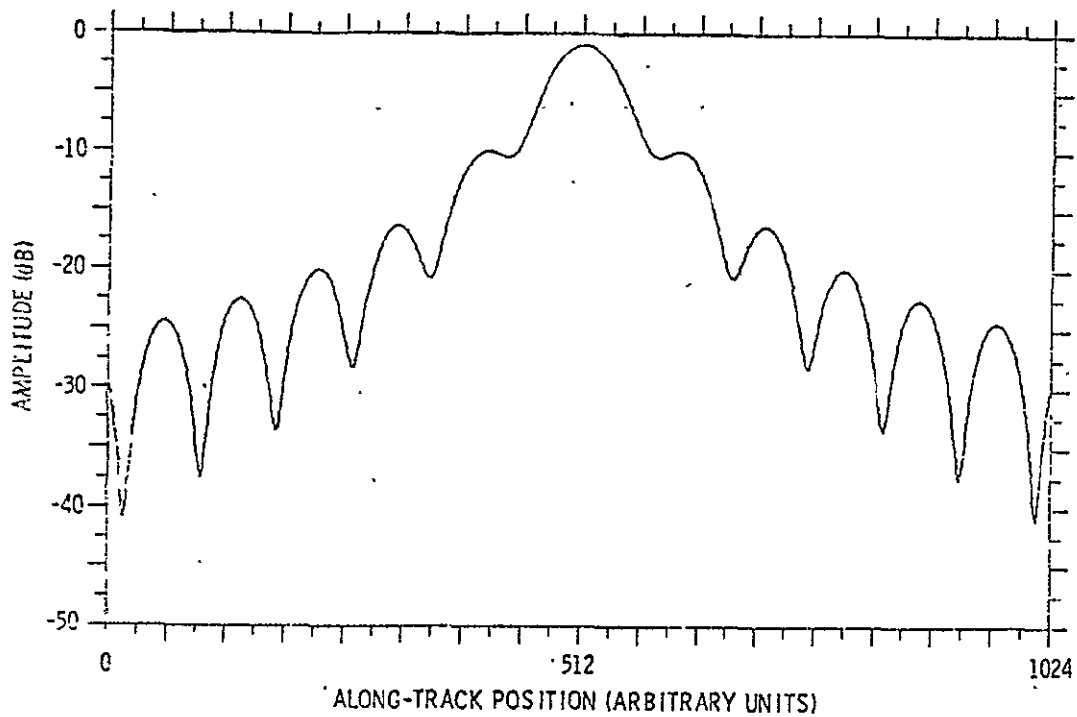
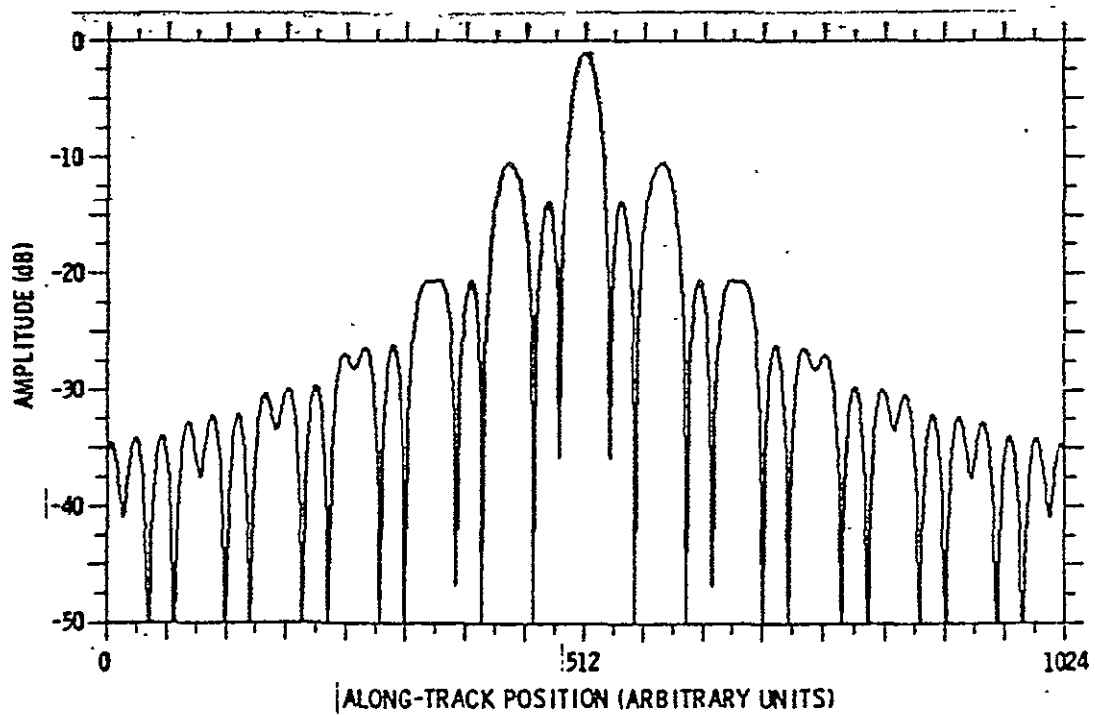


Fig. 1-5 Illustrating phase errors $\Delta\phi$ between segments when target No. (2) is received by a linear segment approximation processor focused for target No. (1). The phase shifters following segment delays cancel these errors.



(a) Single "Unfocussed" Array Segment



(b) Three Segment Quasi-Focused Array. (ISLR = 4.23 dB)

Fig. 1-6 - Point target Azimuth Response Patterns

"grating lobes" and we will adopt the term here) the ISLR was reduced from -4.23 db to -8.61 db, and the major contributor to the new ISLR became the sidelobes between the main lobe and the grating lobes. These side lobes can be controlled by conventional aperture weighting.

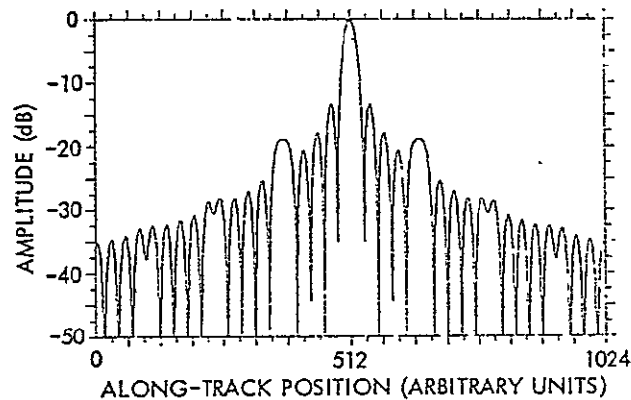


Fig. 1-7 Point target azimuth response of 5-segment processor with segment lengths shortened to $0.6 L_1$. ISLR = -8.61 dB

Computer simulation of a large number of versions of the Linear approximation concept similar to those that produced Figs. 1-6 and 1-7, where the segment length and number of segments are varied and different aperture weightings employed have resulted in design curves that predict both ISLR and peak sidelobe ratio PSLR. Those that resulted in the final design for this report are shown in the next section of this report. A few other comments resulting from these studies are warranted here:

- o Just as an array of identical real radiating elements produces a directivity pattern that is a product of the element pattern and an array factor pattern consisting of grating lobes, so can the synthetic azimuth response pattern of Fig. 1-6b be viewed as a product of the subarray pattern of 1-6a times a grating lobe pattern.

- o The number of aperture sidelobes between grating lobes is $N-2$ where N is the number of segments.
- o Amplitude of the grating lobes is equal in magnitude to the nulls of the single segment response pattern (See Fig. 1-6).

These comments are valid when the segment length, L , is equal to the segment spacings, S . A more general case permits a processor with overlapping segments so that L and S are independent of each other. Then the grating lobe pattern has a periodic spacing determined by S and the grating lobes do not necessarily fall on the null of the single-segment response pattern. Nevertheless, the single-segment response still determines the magnitude of the side lobes resulting from the grating lobe pattern.

Section 2

CHOICE OF PARAMETERS FOR A LINEAR APPROXIMATION
SAR AZIMUTH PROCESSOR

The purpose of this section is to develop a rationale for the choice of the three key parameters of a Linear Approximation SAR Azimuth Processor of the type described in previous section that will satisfy the SEASAT performance requirements. These parameters are (1) total array length, (2) linear-approximation segment length, and (3) length of the subsegments that compose the full segments. These parameters must be chosen so as to yield a specified azimuth (along-track) resolution at the processor output while maintaining sidelobe peak and integrated values at acceptably low levels. The term "length" is used to refer to both a physical length and the number of samples in a data array constituting the synthetic array, or a segment thereof.

For convenience in analytical development, the parameters are considered in the order (1), (3), (2). The application of analytical results is then illustrated by means of a numerical example. Definitions of the symbols used are given in Table 1.

Array Length (P)

The total number of radar repetition periods, P, in the entire array must be chosen large enough so that the main beam resolution, after allowing for beam broadening due to aperture weighting, or "windowing", is less than a specified resolution distance, Δx . For a focused (or quasi-focused) array of length L, we have (for the broadside case):

$$x = B \frac{\lambda R_t}{2L} \quad (1)$$

TABLE I
Definition of Symbols

P	= total number of radar repetition periods (pulses) used in forming synthetic array (integer)
Q	= number of pulses integrated by 1st stage (recirculating) integrator per integrate and dump cycle (integer)
S	= number of 1st stage integrator outputs integrated by 2nd stage (moving window) integrator to form segment output (integer).
I	= number of segments (integer)
D_r	= distance traveled by radar between pulses, i.e., in pulse repetition period (m)
T_r	= pulse repetition period (sec)
V	= vehicle velocity (msec^{-1})
L	= synthetic array length (m)
Δx	= specified along-track resolution at 3 dB points (m)
B	= beam broadening factor relating actual 3 dB beamwidth to peak-to-null beamwidth for uniformly weighted, focused array
R_t	= target slant range at closest approach (m)
θ_t	= target squint angle, assumed to be 90°
b	= segment physical length $\pm \sqrt{R_t \lambda}$
λ	= radar wavelength (m)

where the symbols are as defined in Table I.

Using

$$L = P \cdot D_r = P T_r V \quad (2)$$

in Eq.(1) and solving for P yields

$$P \geq \frac{B \lambda R_t}{2 T_r V \Delta x} \quad (3)$$

where the inequality sign indicates that the (integer) value of P must be greater than the value of the right-hand side (rhs) of Eq. (3). The choice of P cannot be fixed exactly at this point because P must satisfy the equation

$$P = I \cdot S \cdot Q, \quad (4)$$

in which I , S , and Q (also integer) must satisfy additional constraints, as derived below.

Subsegment Length (Q)

The first stage (recirculating) integrator must produce outputs at the same rate as that required at the processor output since there is no change of sample rate in the processor beyond the first-stage integrator. In order to produce strip map imaging, outputs must be available at least once per resolution cell of the unweighted aperture, namely x/B . Thus, we require

$$Q \cdot T_r V \leq \Delta x / B$$

or

$$Q \leq \frac{\Delta x}{T_r V B} \quad (5)$$

Define q as the factor by which Q is less than the rhs of Eq. (5). Then we can write

$$Q = q \frac{\Delta x}{T_r V B}, \quad q \leq 1. \quad (6)$$

If the output data rate is not required to be minimum, any integer sub-multiple of this q-value, with a correspondingly smaller value of Q could be used.

Segment Length (S)

The number of signal samples S (outputs from the first-stage integrator) that make up a linear approximation segment implies a physical segment length of $SQ T_r V$. This length must not exceed a limit set by tolerable grating lobe and ISLR levels, after allowing for reduction by aperture weighting. We now express the segment physical length as a fraction b of a reference length $\sqrt{\lambda R_t}$, the length for which phase error at the segment ends would be $\pi/2$. The required relation is

$$\begin{aligned} SQ T_r V &= b \sqrt{\lambda R_t} \\ \text{or } S &= b \frac{\sqrt{\lambda R_t}}{Q T_r V}, \quad b \leq b_{\max} \end{aligned} \quad (7)$$

Here, b_{\max} is the largest value of b that will produce acceptable grating lobe and ISLR levels and b is to be chosen to make Q an integer.

Number of Segments (I)

The number of segments I must be chosen large enough that the total number of data samples in the array, namely $I \cdot S \cdot Q$, is not less than P calculated from Eq. (3). That is, we require

$$I \cdot S \cdot Q \geq P \quad (8)$$

Where P is given by Eq. (3)

Therefore we require

$$I \geq \frac{P}{S \cdot Q} \quad (9)$$

where the inequality indicates that I is to be taken as an integer greater than (or equal to) the rhs.

Sample Calculation

For the nominal SEASAT Parameters as follows:

$$V = \text{Vehicle Velocity (msec}^{-1}\text{)} = 7.5 \times 10^3 (\text{msec}^{-1})$$

$$T_r = \text{Pulse repetition period (sec)} = \frac{1}{1600} (\text{sec})$$

$$R_t = \text{Target Slant Range (km)} = 860 \text{ km}$$

$$\Delta x = \text{Specified Along-Track Resolution (m)} = 25.0 \text{ m}$$

$$\lambda = \text{Radar Wavelength (m)} = 0.235 \text{ (m)} \quad (f = 1275 \text{ MHz})$$

Also assume half-cosine weighting corresponding to which $B = 1.20$

From Eq. (3)

$$P \geq \frac{B\lambda R_t}{2T_r V \Delta x} = \frac{(1.2)(0.235\text{m})(8.60 \times 10^5\text{m})}{(2)(1/1600)(7.5 \times 10^3 \text{ m}\cdot\text{sec}^{-1})(25\text{m})}$$

$$\underline{P \geq 1035 \text{ samples per azimuth array}}$$

From Eq. (6)

$$Q = q \frac{\Delta x}{T_r V B}, \quad q \leq 1$$

$$= q \frac{25}{(1/1600)(7.5 \times 10^3)(1.2)} = q(4.444).$$

$$\therefore \text{Largest } q \text{ is } \frac{4}{4.444} = 0.9 \text{ and } \underline{\underline{Q = 4}} \text{ pulses per integrate and dump cycle}$$

From Eq. (7)

$$S = b \frac{\sqrt{\lambda R_t}}{Q T_r V} ; b \leq b_{\max}$$

$$S = b \cdot \frac{\sqrt{(0.235)(8.6 \times 10^5)}}{(4)(1/1600)(7.5 \times 10^3)} = b \cdot (23.98)$$

If we take $b_{\max} = 0.6$, then $b = 0.584$ is the largest value that satisfies the requirement $b \leq b_{\max}$ and makes S an integer. We obtain $S = 14$; integrate and dump outputs integrated to form a segment output.

From Eq. (8)

$$I \geq \frac{P}{S \cdot Q} = \frac{1035}{(14)(4)} = 18.48$$

Therefore, $I = 19$ segments.

In summary, for the SEASAT requirement with an azimuth resolution of 25 m at 860 km,

Q = No. of pulses integrated per dump	= 4
S = No. of dumps integrating by moving window integrator (No. per segment)	= 14
I = No. of segments	= 19
P = Total no. of pulses integrated	= 1064
$= I \cdot S \cdot Q = (19)(14)(4)$	

This value is consistent with the minimum value of 1035 samples calculated above to produce 25 meter resolution.

While cosine weighting across the aperture was assumed in the above example, other weightings can be used but usually at the expense of more segments. Cosine weighting with 19 segments will result in peak sidelobes below -20 db and an ISLR of -16 db. These numbers were obtained by the computer simulation mentioned in Section 1 of this report to produce Figs. 1-5 and 1-6. The results of a series of simulations of a fixed aperture length with the number of sub-aperture a variable and with cosine weighting and cosine squared (Hann) weighting are shown in Fig. 2-1. These plots show the sensitivity of PSLR (a), ISLR (b), and signal-to-noise ratio (c) to the number of segments used. The overall aperture used in the analysis was that required to produce 25 meter resolution. The PSLR curve for cosine weighting of Fig. 2-1a shows a break point which occurs where the peak sidelobe ratio reduction is the maximum that can be achieved with cosine weighting. This happens for 21 or more segments in which case the grating lobe is smaller in amplitude than the largest cosine weighted aperture lobe of -23 dB. For an aperture with fewer than 21 segments, the sidelobe ratio is determined by the phase errors resulting from the linear approximation concept. A corresponding break point occurs for the Hann weighting at -34 db (not shown on the curve).

In order to establish a point design that can be used for the processor sizing objectives of this study, -20 db PSLR and -16 db ISLR were selected as adequate for the SEASAT processor mission and the required number of segments is 19. More segments would be needed to reduce the phase error grating lobes if better sidelobe requirements were to be met. More aperture weighting (and more overall aperture length to maintain the required resolution) is required only when the grating lobes have been reduced below the aperture sidelobes. The curves of Fig. 2-2 permit the number of segments to be determined for other resolution and sidelobe requirements when the SAR aperture is to be cosine (a) or Hanning (b) weighted.

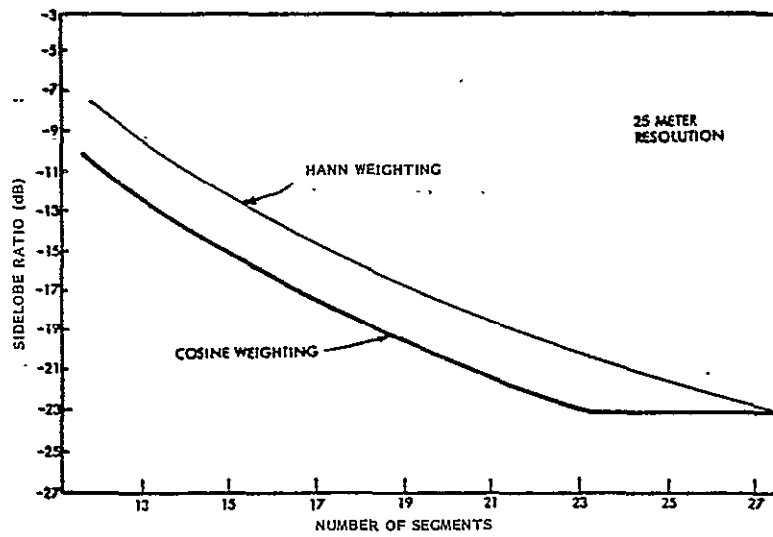


Fig 2-1(a) PEAK SIDELobe RATIO VS. SEGMENTS

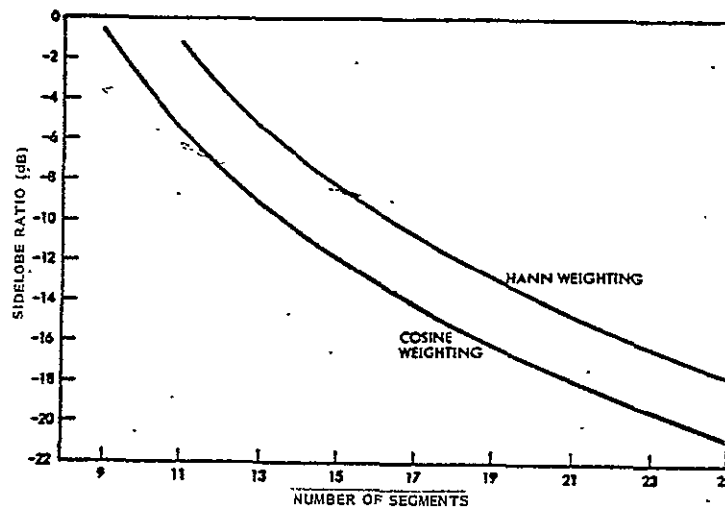


Fig 2-1(b) INTEGRATED SIDELobe RATIO VS. SEGMENTS

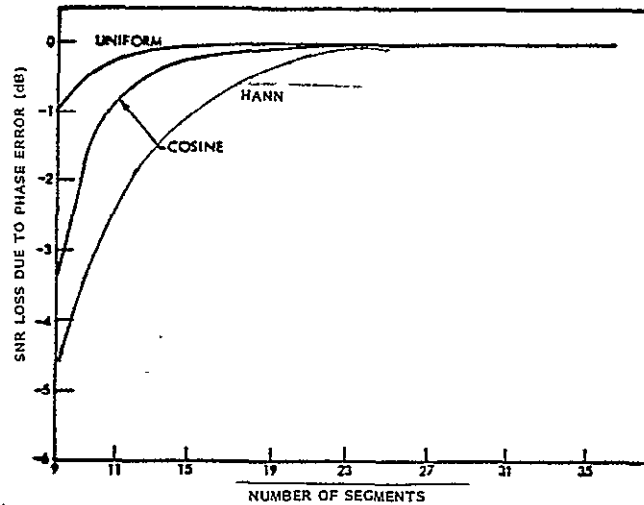
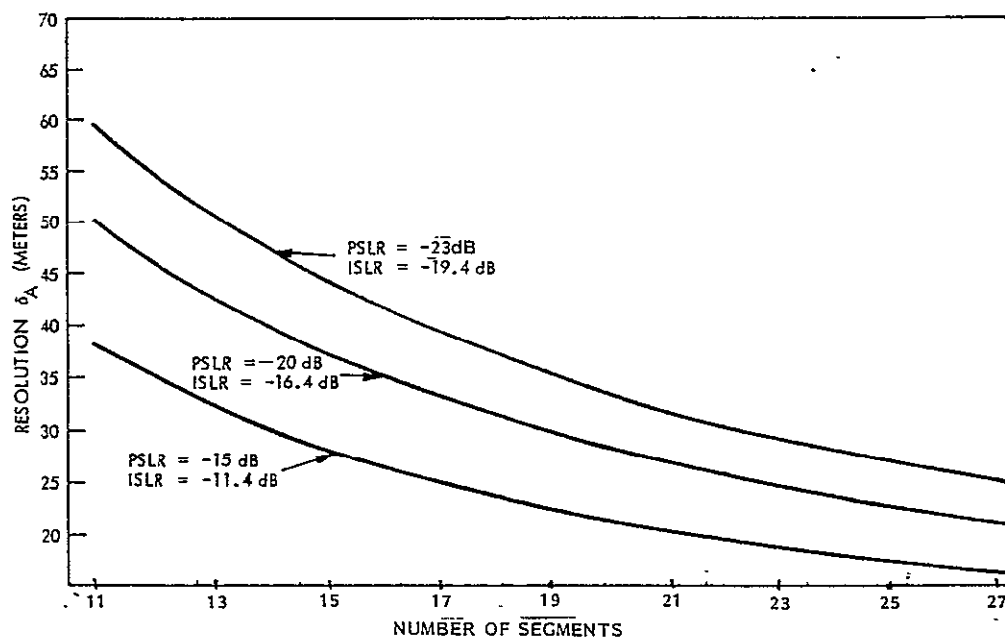
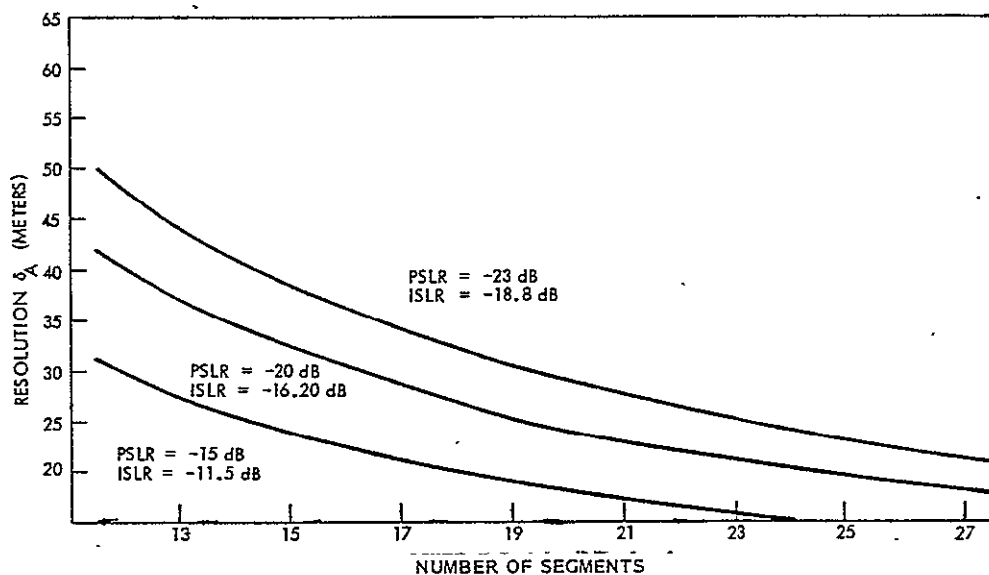


Fig 2-1 (c) SNR LOSS DUE TO PHASE ERROR VS. SEGMENTS



(a) COSINE WEIGHTING



(b) HANN WEIGHTING

Fig. 2-2 RESOLUTION VS. NUMBER OF SEGMENTS (COSINE AND HANNING)

Section 3

DESIGN CONSIDERATIONS

This section describes the design approach and rationale that led to the Improved Baseline Design which is described in detail in Section 4. This final design was preceded by what is referred to as the Baseline Design which is a 19 segment extension of the three segment configuration of Section 1.

A baseline design and study was performed of a 19 segment processor employing the parameters developed in Section 2 and with the sequence of operations within each segment identical to that of the Basic three segment processor shown in Fig. 1-3. The design was performed for three reasons:

1. To provide a preliminary sizing and reference data for an improved design.
2. To provide a baseline configuration which could be used to identify opportunities for size reduction.
3. To provide a configuration early in the study that could be simulated in the time domain in order to determine the impact of digital word sizes within the processor on equipment requirements. This simulation work was performed jointly with the Institute for Advanced Computation (IAC) and is reported in Appendix A.

The implementation details of this Baseline Design are presented in Section 4.

While the performance requirements were successfully met with the baseline design (see Fig. 3-1), it was recognized early in the study that several opportunities existed for a reduction in this processor's memory requirements. The integrate and dump filters employed, for example, besides being duplicated for each segment must operate at the sample rate of the incoming SEASAT information, 1600 pulses at each range cell. While the data rate out of the integrate and dump is reduced to 400 pps, correspond-

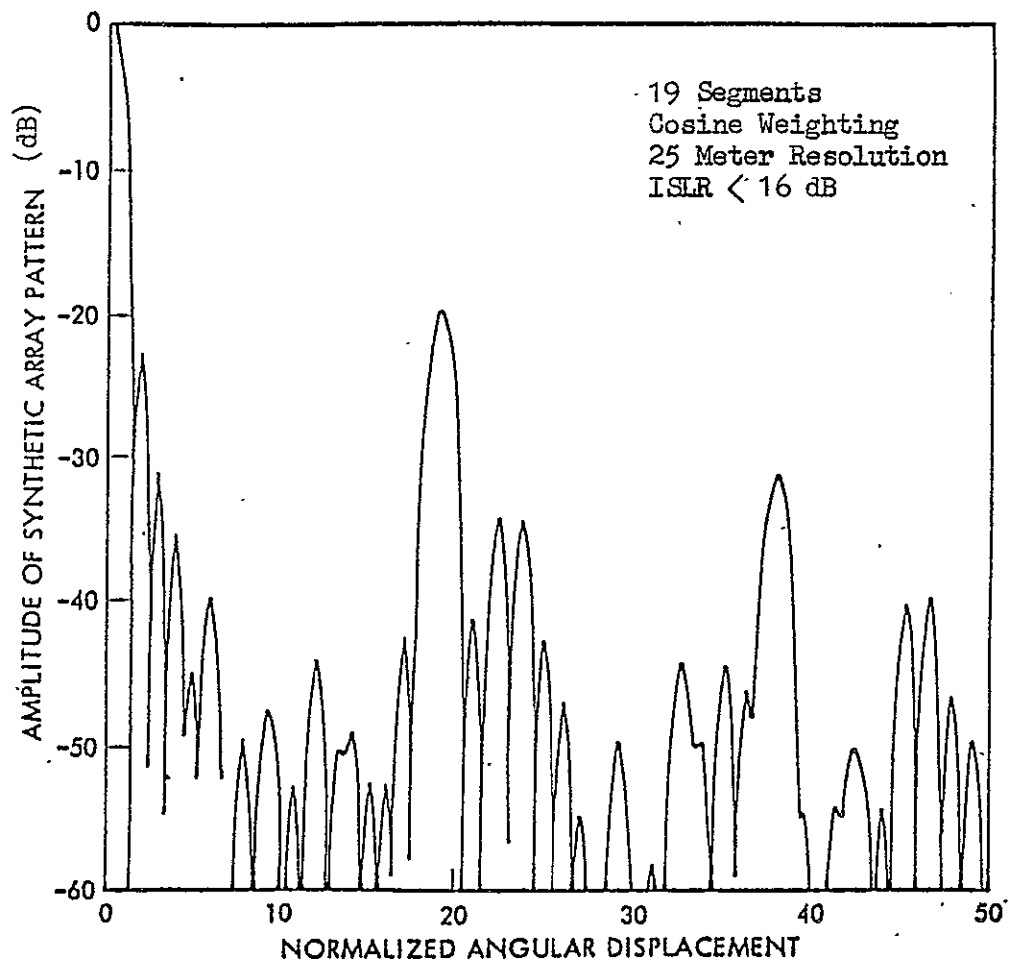


Fig. 3-1 Impulse Response for Baseline Processor

ing to the single look doppler bandwidth of 360 Hertz, the moving window integrator must operate at this rate, not at the rate of 20 Hertz corresponding to the actual information bandwidth of each segment ($360 \div 19$ segments). Operating at this higher rate not only precluded the use of some attractive high density memory chips, but resulted in higher storage requirements and arithmetic rates in the subsequent stages. The delay memories of Fig. 1-3, used to align the data on 4000 range cells from each segment, for example, must have the full 400 Hertz bandwidth capability, much higher than that necessary to support the information bandwidth of 20 Hertz.

In the Baseline design aperture weighting was applied with the data in each segment weighted uniformly but that from segment-to-segment weighted according to a stepped cosine function. Performance with this stepped weighting over the entire aperture was shown to be negligibly different from a continuous cosine weighting for the number of segments considered here. This same stepped cosine weighting was used in the Improved Baseline Design discussed below. The individual segments are also weighted in the Improved Baseline Processor as will be seen in Section 4.

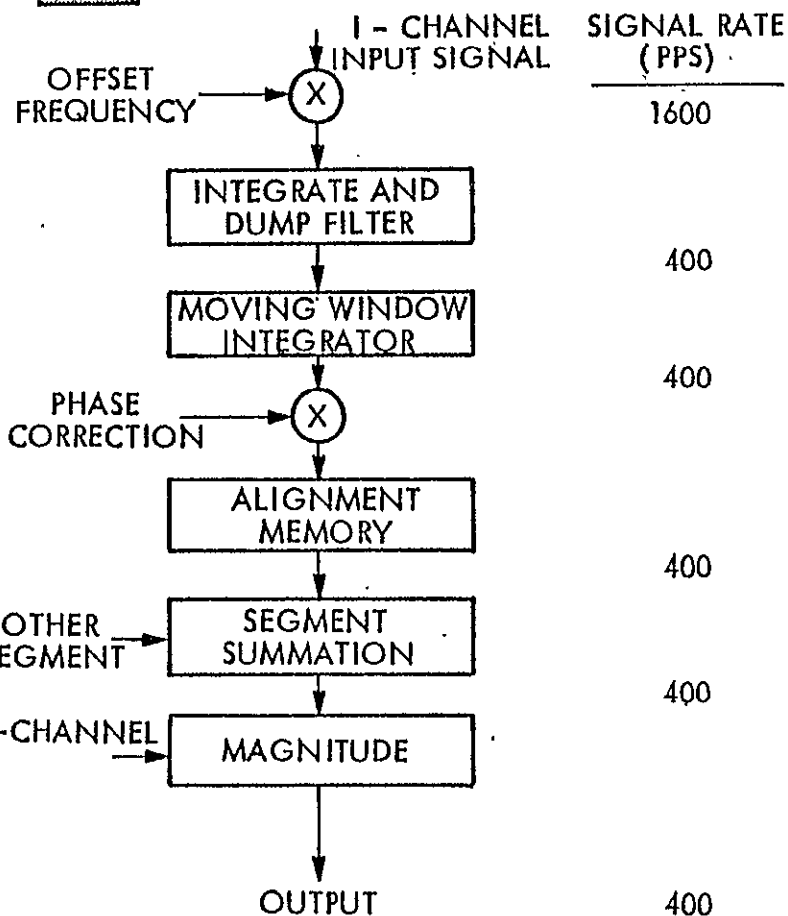
The design of a filter in each segment to reduce the bandwidth to the information bandwidth within each segment (replacing the moving window integrator of the baseline design) presents a severe challenge. The processor's ability to suppress ambiguous targets and spurious signals in the vicinity of a desired target depends on this digital filter design. High stop band rejection and acceptable shape factors place high requirements on the number of input samples, arithmetic rates, and buffer memory needed for its design. As a result compromise and performance trades are unavoidable.

The approach used in the Improved Baseline design incorporates a finite impulse response (FIR) pre-filter design that reduces the sample rate into the 19 segments from 1600 pps to 400 pps. This filter decimation ratio of 4 requires a span factor over 12 rangeline samples. A small corner turn buffer is therefore required. The pre-filter is followed by another FIR

filter in each of the segments which decimates by 14 to produce a data sample rate into the remainder of each segment of 28.5 Hertz. This data sample rate is sufficiently high to handle the information rate within each channel (I&Q) following the required frequency translation of the segments to baseband. This frequency translation, as in the three segment processor of Fig. 1-3 and in the Baseline design, is the frequency offset that separates the incoming data into segment channels. For the Improved Baseline design it is accomplished between the pre-filter and the decimation-by-14 low pass filter in each segment.

The segment alignment memory which handles data at the reduced sampling rate can now be smaller in size. In the Improved Baseline design, therefore, the alignment function is moved ahead of the frequency translation function which is designated "phase correction" in the Basic three segment configuration of Fig. 1-3. This frequency translation (or phase correction) is performed to restore the doppler content of each segment back to their original frequency positions within the overall 360 Hertz doppler band required for 25 meter resolution. Whereas the earlier translation (frequency offset) translated the bands for each segment prior to low-pass filtering, the latter translation following the alignment memory in the Improved Baseline design actually reverses the earlier process. Before this is done, however, the 28.5 Hertz data out of the alignment memory is interpolated to restore the data rate to 400 Hertz. After frequency translation the 400 Hertz output samples are summed, the I and Q channels are combined as illustrated in the signal flow diagram of Fig. 1-4 (for the Basic three segment processor), and output pixels are produced at a 400 pps.

Fig. 3-2 summarizes this discussion by showing comparative segment configurations for the Baseline Design and for the Improved Baseline Design. Signal data rates are indicated at each stage within each configuration.



(a) Baseline Design

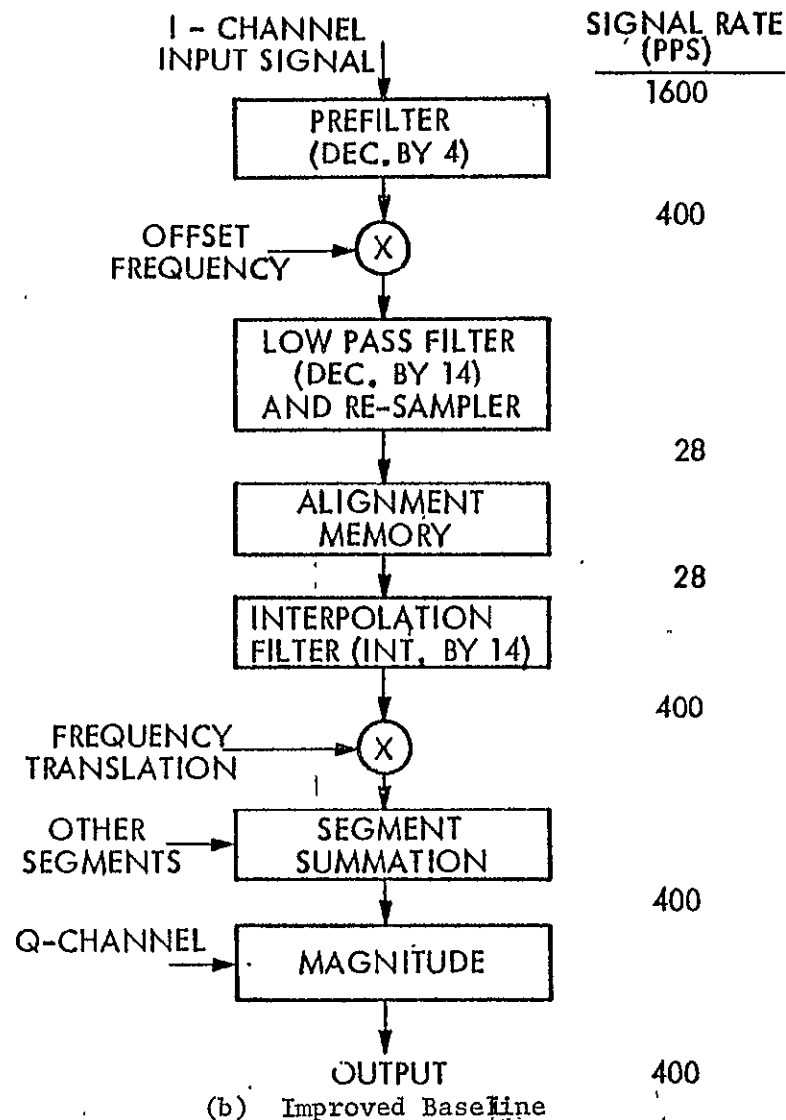


Fig. 3-2. Segment Architectures - (a) Baseline Design; (b) Improved Baseline Design

Section 4

DESIGN DESCRIPTION

This section describes the architecture and design detail for the Baseline and the improved baseline processor design. The improved baseline processor design provides the basis for determining chip count and related sizing discussed in Section 6.

BASELINE PROCESSOR

Baseline Circuit Design Overview. The Baseline architecture of Fig. 3-2 is shown in greater detail in Fig. 4-1. Consider first the frequency domain characteristic of the integrate-and-dump (I&D) filter which is shown in Fig. 4-2. It will be observed that there is a narrow region about the zero frequency axis where the folded-in alias signals are minimized. The baseline processor filters this signal through the use of a moving window integrator. Since the zero frequency region must then be at the center of each of the 19 segments, the frequency translation must precede the I&D filter. The I&D filter must, therefore, be duplicated 38 times (i. e., for the I & D components in each of the 19 segments). A filter with better stop band rejection than the I&D could be implemented prior to the frequency offset, thus reducing the offset multiply rate and avoiding the duplication (38 times) of the I&D function. This is, in fact, what is done in the improved baseline design.

Following the I&D filter in the baseline design is the moving window integrator (MWI) which performs the function of segment filtering. The 6 dB bandwidth of this MWI is about 20 Hertz, but its output sample rate is maintained at 400 samples per second to avoid spectral folding of the alias energy into this 20 Hertz band. As in the case of the I&D filter, a greater stop band rejection in this operation would permit reduction of the sample rate and simplification of succeeding operations. This reduced sample rate would necessarily have to be interpolated back up to the output resolution cell rate. The improved baseline is based upon the use of high stop band rejection. FIR filtering here to allow the use of high density memory chips in the filter output sections.

Baseline Circuit Implementation. The circuit block diagrams for the baseline processor functions are shown in Fig. 4-3, a thru c. A brief discussion of the design given in following paragraphs.

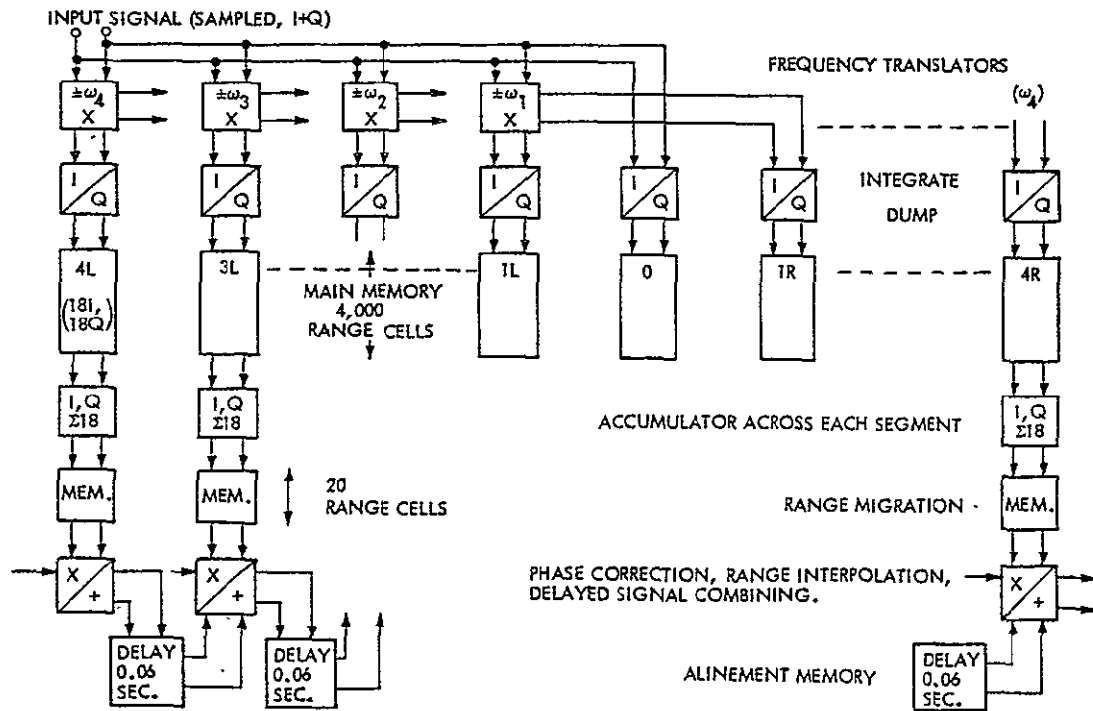


Fig. 4-1. Baseline Nineteen Segment Azimuth Processor

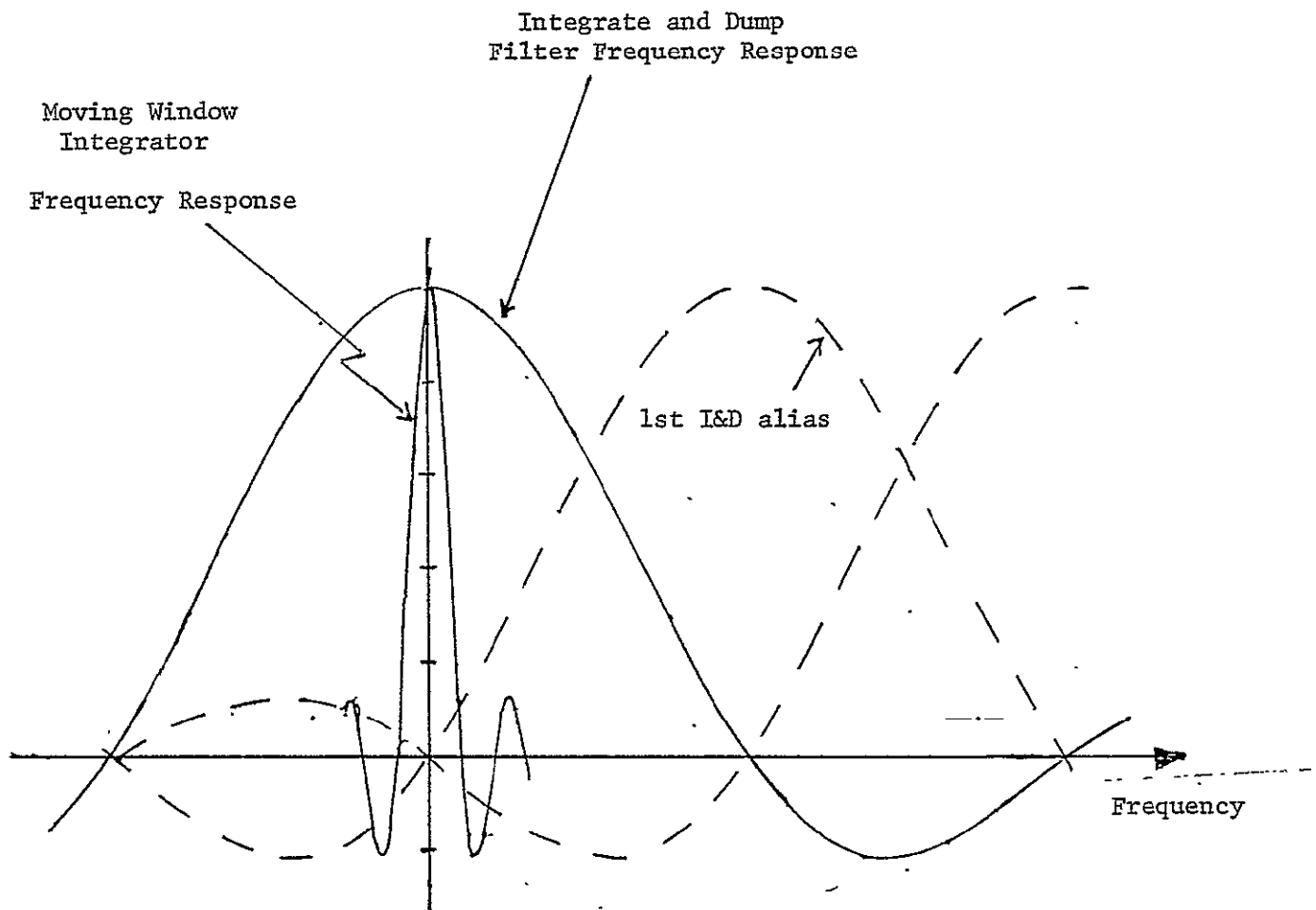


Fig. 4-2. Location of segment filter relative to integrate and dump spectrum to reduce aliased signal components.

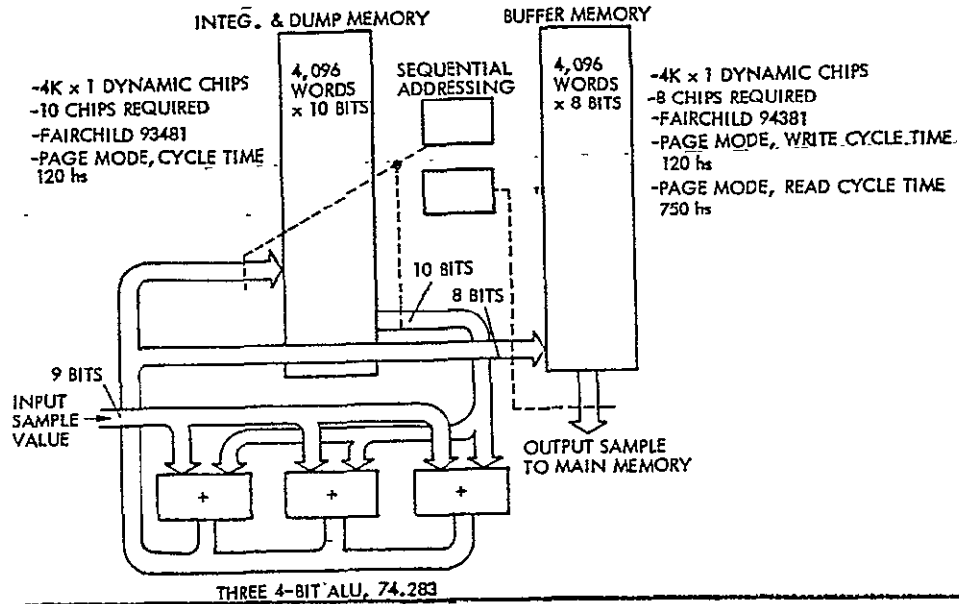
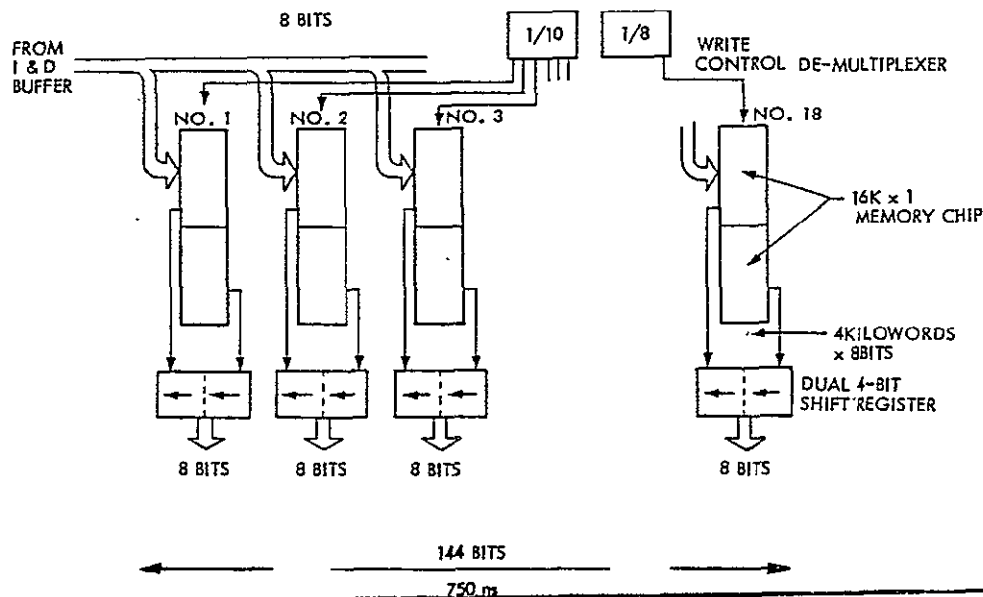


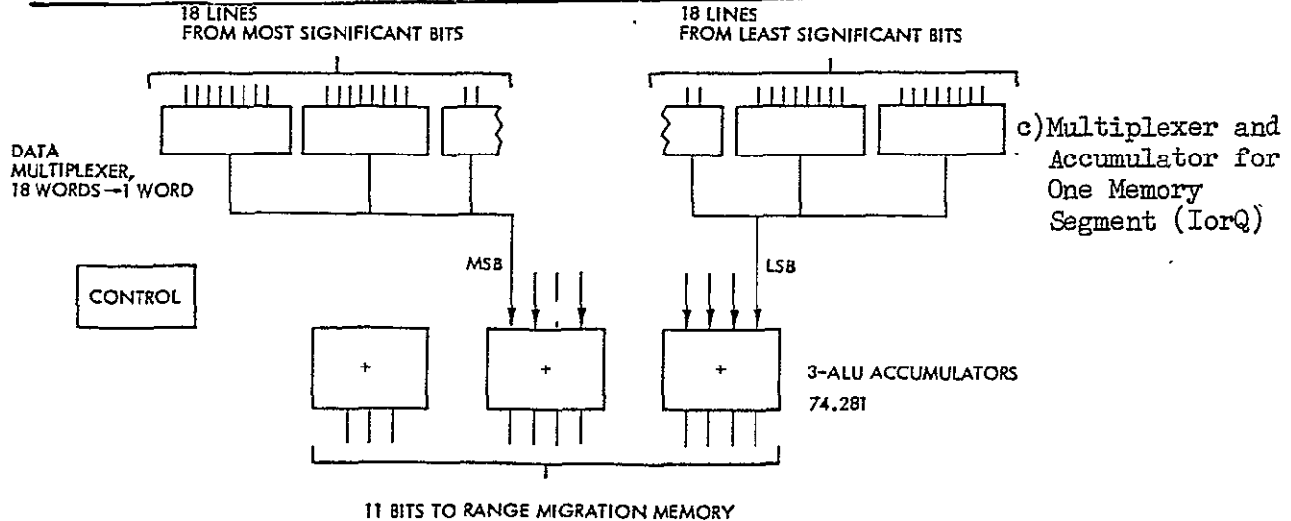
FIG. 4.3

BASELINE PROCESSOR

a) Integrate and Dump Prefilter Block Diagram



b) Main Memory (One Segment)



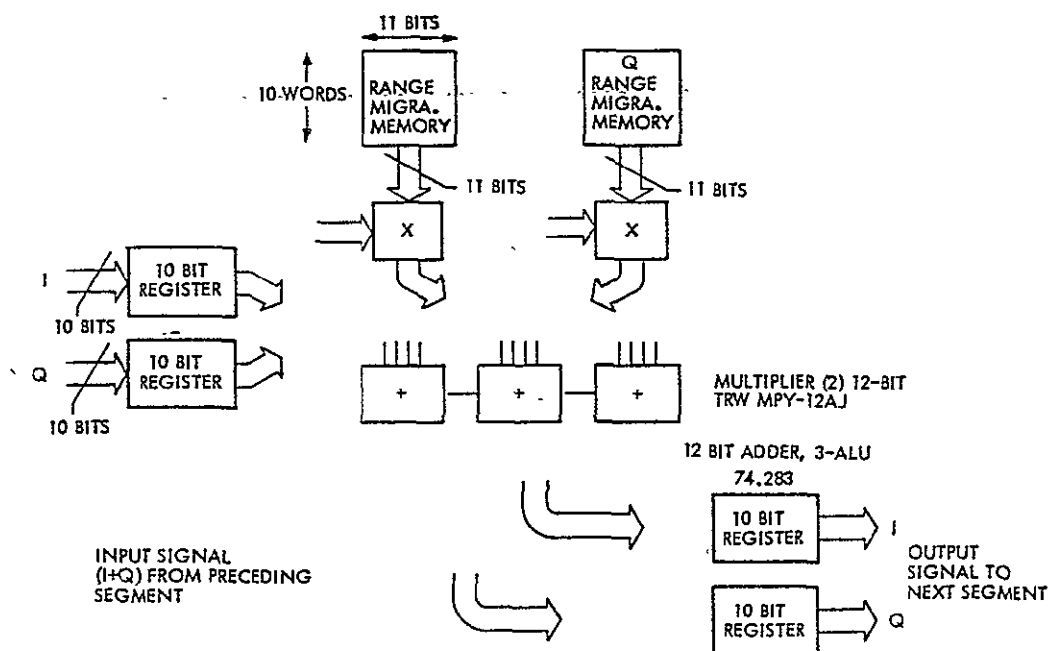
c) Multiplexer and Accumulator for One Memory Segment (IorQ)

Examining the information flow rates in the I&D prefilter of Figs. 4-3 a and the moving window integrator of Figs. 4-3 b and c, we see the data rate into the azimuth processor is 8000-6 bit words per 625 microseconds (one I and one D word into each range cell at the radar repetition rate of 1600 pps). The frequency translation on the incoming data shown in Fig. 4-1 does not alter the word rate and the word size circulated in the I&D has been increased to 10 bits. Therefore, the data flow rate within each of the 38 I&D circuits is 64 bits per microsecond. This high data rate precluded the use of 16K or larger memory chips at the present state-of-the-art.

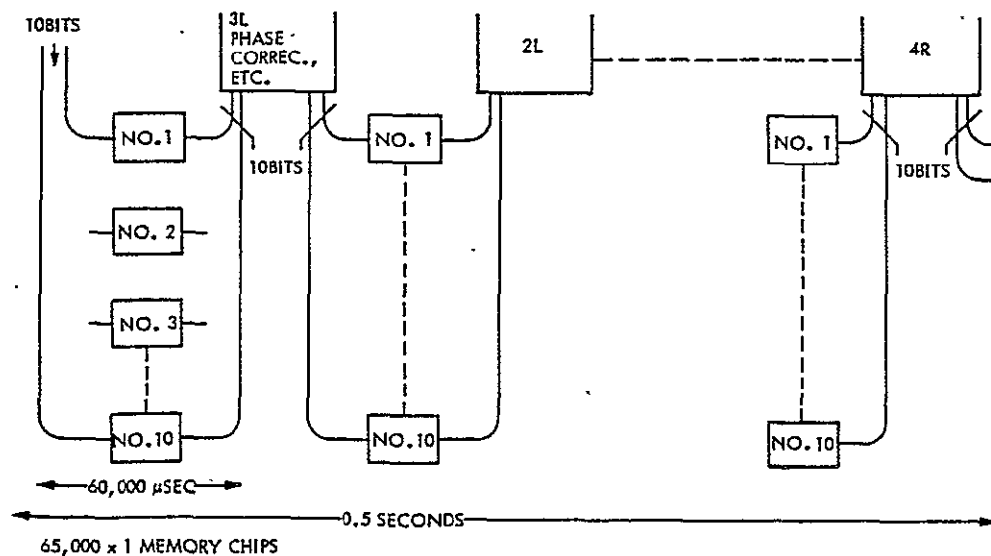
The circuit used in the baseline design employed Fairchild 4K x 1 memory chips based on I²L technology. These chips, designated as 93481, can accomplish a read-write in the requisite 150 nanoseconds when operated in the page mode, where only the column addresses are updated each cycle. The rate disparity between the I&D memory and the moving window integrator memory necessitates the buffer of Fig. 4-3 a, using the same memory chips, but only eight bits wide since no arithmetic is being done. (The time domain simulation and digital noise analysis of Appendix A led to the choice of digital word size for the baseline processor.)

The bit rate out of each of the 38 prefilters in the baseband design is now 13 bits per microsecond. This represents the data rate in only one of 14 lines in a segment, shown in Fig. 4-3 b, each 4000 range cells by 8 bits per cell, which must be read out in the time it takes to replace the contents of the one line. Therefore, the reading rate out of the entire moving window memory of Fig. 4-3 b is 180 bits per microsecond. With a cycle time of about 5 bits per microsecond in 16 Kilobits x 1 bit chips, it is just possible to meet both the reading rate requirement and the number of bits required with about 30 of these chips for each segment. Sixty-four Kilobit chips could not be used as the information bandwidth out of eight of these chips is limited by their characteristics to about 35 bits per microsecond, a factor of five too low. As an aside, the very high reading rate in each segment, effectively a 112 bit word every 0.6 microseconds, necessitates more overhead chips for support services than would a narrower word and lower reading rate. The actual signal integration in the segment is done with the adder circuit shown in Fig. 4-3 c.

The remaining tasks of Figs. 4-3 d and 4-3 e involving the phase correction, range interpolation, segment combining, and alignment memory, are relatively straightforward. After a low-pass filter function of the moving window integrator, a buffer memory is used to enable range walk interpolation to be performed by an arithmetic unit consisting of a 12 bit IC multiplier together with a separate adder as shown in Fig. 3-2 d. The



4.3(d) Phase Correction, Range Interpolation and Segment Signal Combines



4.3(e) Alignment Memory

loading of the interpolation task together with the phase correction (frequency translation) and signal combining from previous segments is sufficient to require allocating one arithmetic unit to each complex segment.

The signal from one segment is combined with the next segment in turn, after a delay of 0.035 seconds, in the arithmetic portion of Fig. 4-3 d. With this approach it is necessary that the alignment memory shown in Fig. 4-3 e have the full bandwidth capability of the signal. The azimuth bandwidth is about 400 Hz. This requires that 400 complex samples/sec must be provided for each of 4000 range cells, with 10 bits per word, for a total information bit rate of 32 bits per microsecond. (The bit capacity requirement between segments is 560 Kilobits.) Using ten 64 Kilobit memory chips between each segment can satisfy the requirement, as their combined capacity is 640 Kilobits and they can produce a bit rate of about 40 bits per microsecond.

IMPROVED PROCESSOR

Improved Design Overview. The block diagram of Fig. 4-4 retains the approach of the multi-segment processor but differs from the baseline design in the task sequencing and in the circuit design used for particular tasks. A single prefilter is used, followed by the needed frequency translation to bring the various segments down to baseband. At baseband a low-pass filter is used for each segment. With the information bandwidth reduced, the sample rate of the information can also be reduced, by a factor of fourteen. The segment information is now delayed by separate delay lines, in contrast to the 'tapped delay-line' concept used in the baseband processor. Before recombining the segment signals it is necessary to restore the sample rate from 28.6 Hertz to 400 Hertz, and this operation must be performed in conjunction with another low-pass filter acting as a signal sample interpolator. The segment signals must also be translated back to their original spectral location. Finally the segment outputs are combined in an accumulator.

The preceding short summary of the improved processor block diagram of Fig. 4-4 calls out three filters in the signal processing sequence: a prefilter, a low-pass filter, and an interpolating filter. A finite-impulse-response (FIR) design based on the McClellan-Parks* algorithm was used. Although the functional requirements on the low-pass the interpolation filters differed in details, there is enough similarity that for this first design the same parameters were used.

The FIR configuration employed is simply a sum-of-products approach, $\sum_{k=1}^{N_i} h_k x_k$, where the filter performance is determined by the length of the impulse response N_i ; and the particular set of multiplying coefficients h_k chosen. A filter impulse response length $N_i = 12$ for the prefilter is sufficient to provide a peak signal-to-reject band ratio of 30 db with the set of coefficients listed in Table 4-1. The corresponding filter impulse response and frequency response are shown as Fig. 4-5 a and b. It will be observed in Fig. 4-5b that the passband shape, while smooth by varying in a fashion corresponding to some particular windowing function, does not correspond to the cosine weighting function called for elsewhere in the report. The multiplicative factor difference between the window function of Fig. 4-5b and a cosine function can be readily included in the FIR coefficients for the low-pass filter.

* J. McClellan and T. Parks, "A Computer Program for Designing Optimum FIR Linear Phase Digital Filters", I III Trans. Audio Electroacoust., Vol. AU-21, pp 506-526, Dec. 1973

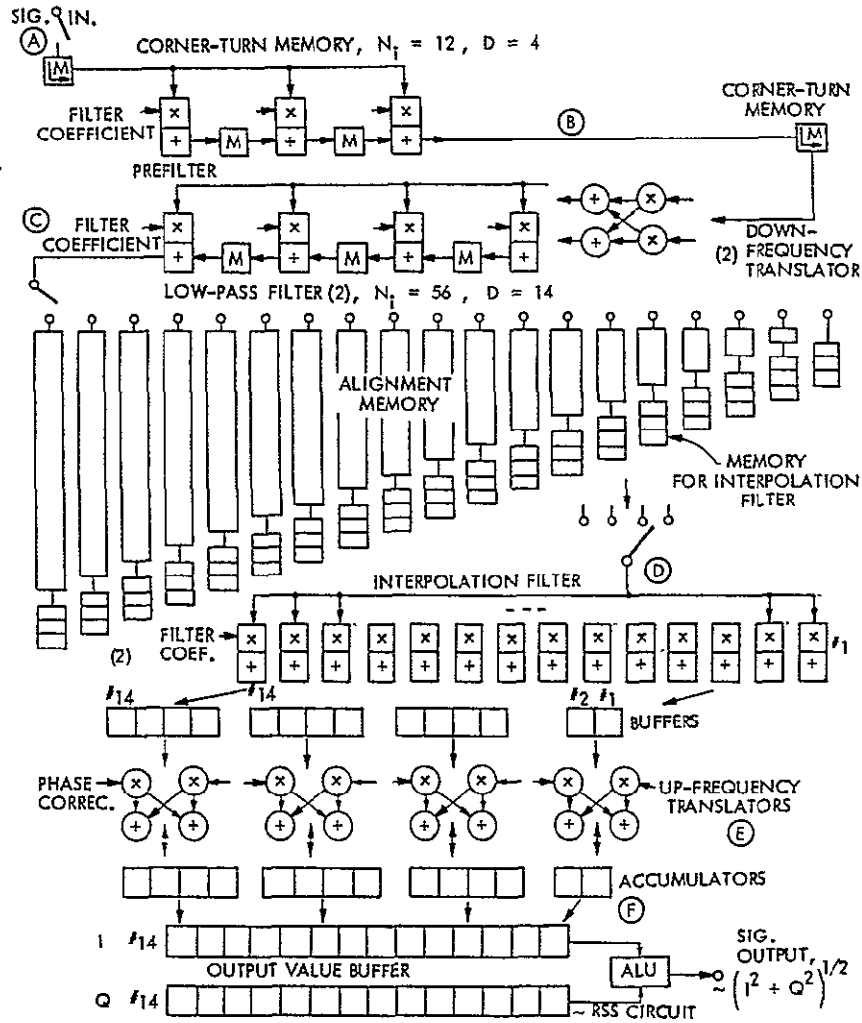


Fig. 4-4. Improved 19-Segment Processor

Table 4-1. Set of Coefficients Used for the Prefilter Design

(1)	=	0.2120	=	(12)
(2)	=	0.3421	=	(11)
(3)	=	0.5423	=	(10)
(4)	=	0.7437	=	(9)
(5)	=	0.9078	=	(8)
(6)	=	1.000	=	(7)

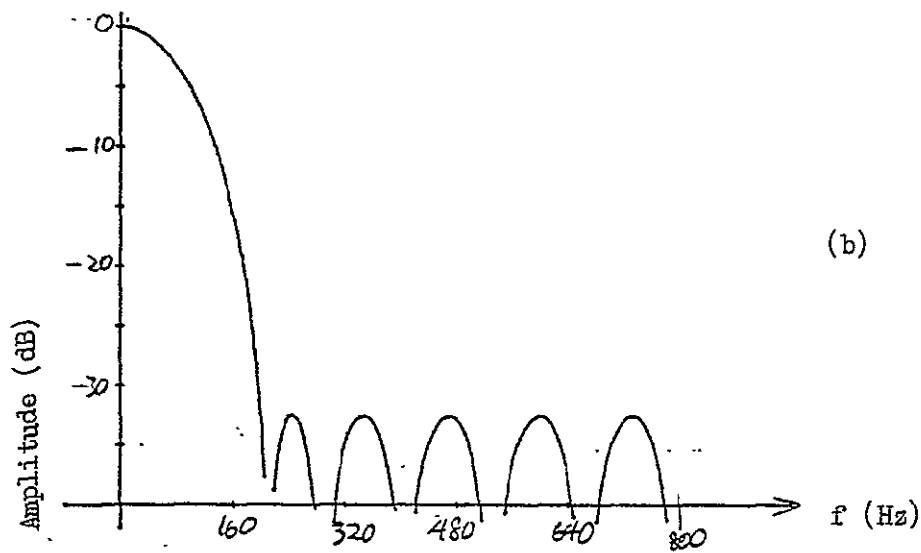
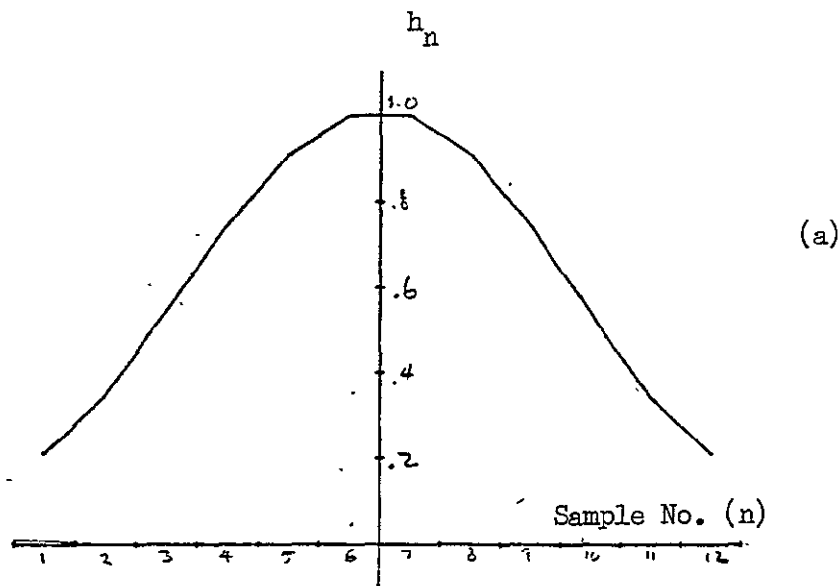


Fig. 4-5 Impulse Response (a) and Logarithmic Amplitude Frequency Response (b) of FIR Prefilter

The low-pass filter impulse response length must be considerably greater than that of the prefilter to provide the desired steeper cut-off rate and smaller fractional bandwidth. A figure of $N_1 = 56$ was used. The filter coefficients are listed in Table 4-2. The corresponding logarithmic and linear amplitude responses are shown in Fig. 4-6.

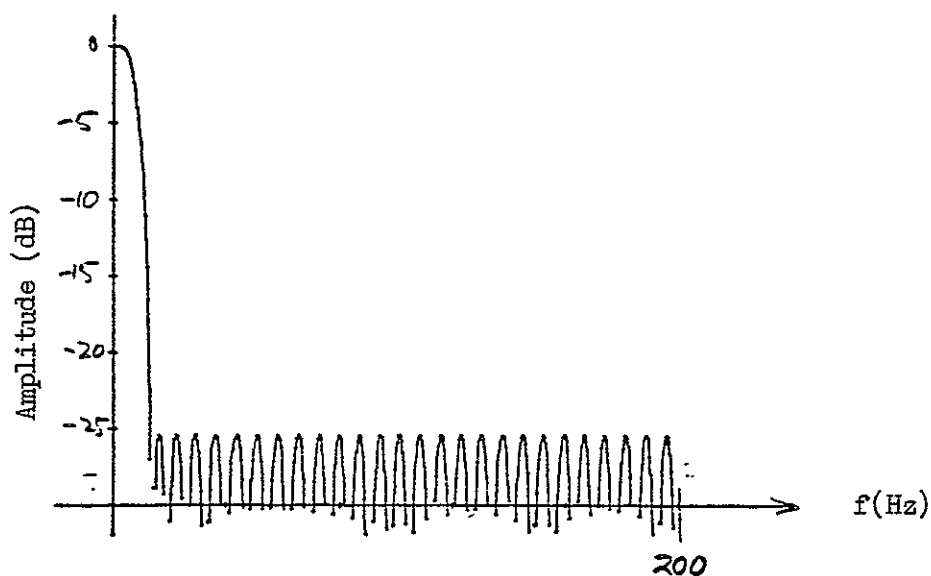


Fig. 4-6 Logarithmic Amplitude vs. Frequency Response of Low-pass and Interpolation Filters

Table 4-2. Set of coefficients used in the low-pass and interpolation filters

(1)	=	-0.5830	=	(56)
(2)	=	-0.0957	=	(55)
(3)	=	-0.0970	=	(54)
(4)	=	-0.0935	=	(53)
(5)	=	-0.0846	=	(52)
(6)	=	-0.0698	=	(51)
(7)	=	-0.0487	=	(50)
(8)	=	-0.0211	=	(49)
(9)	=	0.0131	=	(48)
(10)	=	0.0537	=	(47)
(11)	=	0.1004	=	(46)
(12)	=	0.1527	=	(45)
(13)	=	0.2100	=	(44)
(14)	=	0.2723	=	(43)
(15)	=	0.3390	=	(42)
(16)	=	0.4065	=	(41)
(17)	=	0.4768	=	(40)
(18)	=	0.5471	=	(39)
(19)	=	0.6162	=	(38)
(20)	=	0.6833	=	(37)
(21)	=	0.7467	=	(36)
(22)	=	0.8055	=	(35)
(23)	=	0.8582	=	(34)
(24)	=	0.9038	=	(33)
(25)	=	0.9414	=	(32)
(26)	=	0.9704	=	(31)
(27)	=	0.9904	=	(30)
(28)	=	1.0000	=	(29)

Improved Baseline Circuit Implementation. The circuit block diagrams for the improved baseline processor are given in Figs. 4-7 a thru g. The design of these circuits is discussed in the following paragraphs. The filter shown in Fig. 4-7 a is intended to decimate by four as well as to perform as a low-pass filter. The correspondingly low sample rate reduces multiplication and storage requirements in the prefilter by a factor of four also, allowing the use of $12 \div 4 = 3$ multiplier/accumulator chips shown in Fig. 4-7 a. After accumulating the four products associated with the four adjacent values read out from the corner-turn, the sum is stored in memory before reading the next range cell values. The stored intermediate accumulated sums are read back into the accumulator of the next multiplier/accumulator chip just before the next corner-turn memory bank reads the next set of four azimuth values for that range cell.

Figure 4-7 b shows a block diagram for the three functions of corner-turn, frequency translation, and low-pass filtering. The corner-turn and low-pass filtering functions are similar to the same functions in the prefilter. The filter impulse response length has been implemented for 56 samples as previously discussed; however, this should be considered to be a preliminary design point subject to later optimization. In addition it is necessary to have 38 low-pass filtering operations (19 each of I and Q) instead of the two in the prefilter, for each range cell. Thus, Fig. 4-7 b shows the circuit blocks necessary to implement 150,000 distinct low-pass filtering operations, reducing an input information bandwidth of about 120 Hertz down to about 10 Hertz, both at the -6 db point. In this process the sampling rate of the information is reduced from 400 Hertz down to 28.6 Hertz, making the scheme possible through the associated decimation.

Interposed between the corner-turn memory and the bank of multiplier/accumulator chips of Fig. 4-7 b is a frequency translator shown as a multiplier block and an adder block. In operation, 14 successive complex azimuth values would be read from the corner-turn memory. These values would be multiplied by the complex sampled reference frequency associated with each of the 19 complex segment filters. These filters are all at baseband and the frequency translation would bring contiguous 20 Hertz bandwidth sections of the input band down to baseband. The prefilter and low-pass filters serve to reduce and separate the input signal frequency bands. It remains to introduce a time delay to the 19 complex frequency bands, all now located at baseband. This is done in the alignment memory shown as Fig. 4-7 c. In this figure each box represents a single 64 Kilobit chip. With a complex sample rate of 28.6 Hertz in each segment, for 4,096

range cells (the use of 4096 rather than 4000 range cells is done for convenience of clocking the alignment memory) and a word size of 8 bits, the requisite bit clock rate for the alignment memory is 1.87 MegaHertz. The delay increment between adjacent segments is 35 milliseconds ($1/28.6$ Hertz) representing the time interval between appearance of signal energy from a resolution cell in adjacent segments. The low sample rate associated with a minimum chip count alignment memory will not allow reassembly of the segment information without increasing the sampling rate and removing alias signals from the output of each segment channel. This function is performed by the circuit block diagram of Fig. 4-7 c. To restore the segment sample rate from 28.6 Hertz back to 400 Hertz, it is necessary to generate 14 values for each sample value received from the alignment memory. The circuit of Fig. 4-7 d shows the 14 interpolated output values being generated from the last four data samples. The corresponding impulse response length is 56, the same as the low-pass filter preceding the alignment.

Shown in Fig. 4-7 d is switched connection between the data storage chips and the multiplier/accumulator banks. This may be implemented by the means shown in Fig. 4-7 e. After assembling a few bits from the serial output of the data buffer chips, a four bit nibble is written into a 19 word x 64 bit fast memory, from whence it is delivered to the bank of multiplier/accumulators as needed.

The task of frequency translation is performed in two places, once to bring the segment information down to baseband and again to restore it to its original spectral location. The block diagram of Fig. 4-7 f shows the scheme used at the up-translator. It is not possible to use multiplier/accumulator chips in this function as the time needed to get the sums and differences in and out of the accumulator section of the chip nullifies the chips' advantages, making separate realization of the two operations of multiplying and summing more desirable.

In order to maintain acceptable quantizer noise levels, 12 bit multiplier chip is used. The accumulator in Fig. 4-7 f now will hold the correlated azimuth values for 14 points after scanning and translating the 19 complex segment filter outputs. Following this circuitry must be an I, Q combiner as shown in Fig. 4-4.

The task of range-walk variation has not been addressed in the preceding discussion and circuit block diagrams. With a maximum variation of less than 20 range cells across the synthetic aperture duration of 0.65 seconds it is evident that signal information from a single point target will not

move more than one range cell during the 14 sample corner-turn duration in the circuit of Fig. 4-7b. Depending on the results of an interpolation error analysis, it may be sufficient to use a linear interpolation between two adjacent range-cell sample values in each of the 14 azimuth positions. Unfortunately this interpolated value is unique to only one of the 19 segment filters, although it seems likely that fairly coarse interpolation would be adequate at this point in the system.

With a fine interpolation being performed right after the 14 sample corner-turn memory, a coarse interpolation must still be performed. A convenient location for this function is between the alignment memory and the interpolation filter, as shown in Fig. 4-7g.

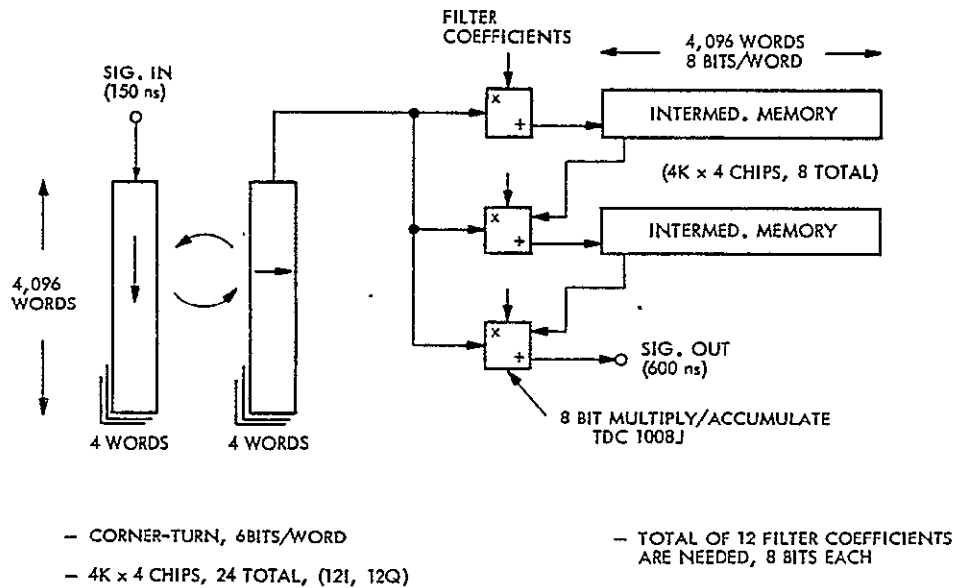


Fig. 4-7(a) Prefilter ($\div 4$)

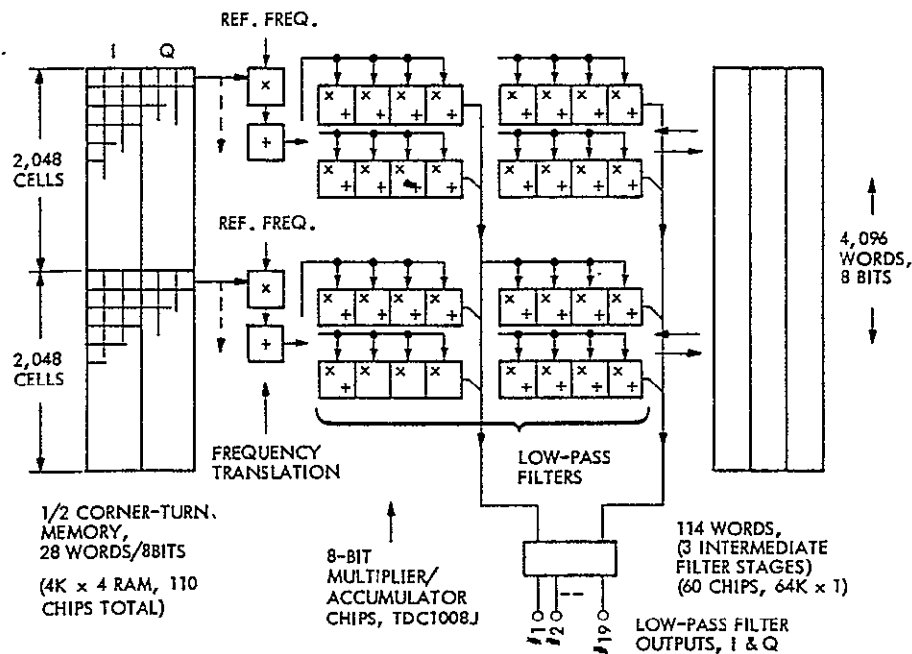


Fig. 4-7(b) Corner-Turn Frequency Translation and Low Pass Filter

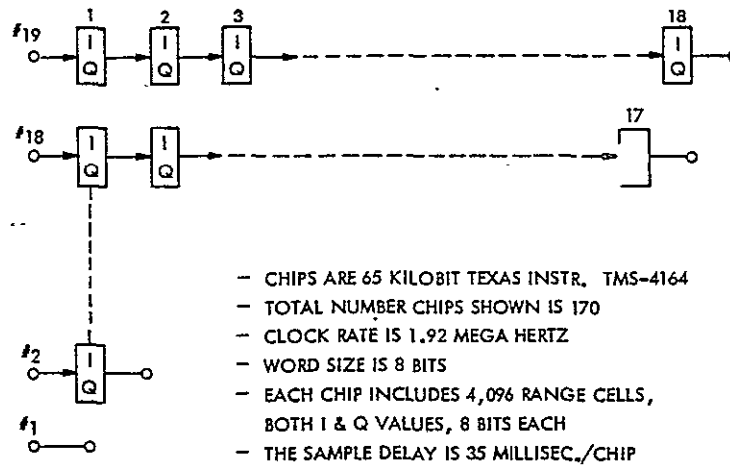


Fig. 4-7(c) Alignment Memory

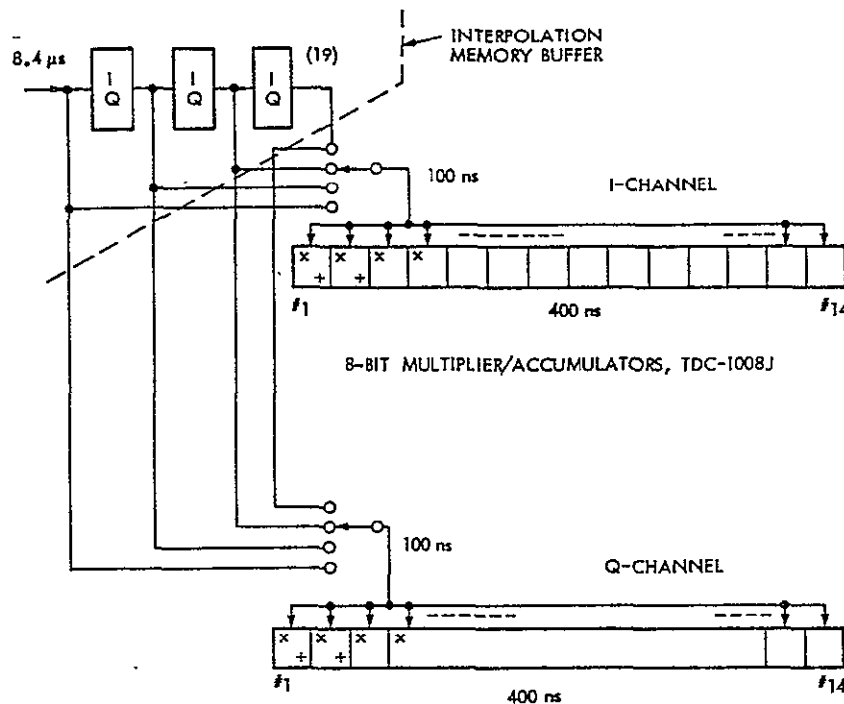


Fig. 4-7(d) Interpolation Filter

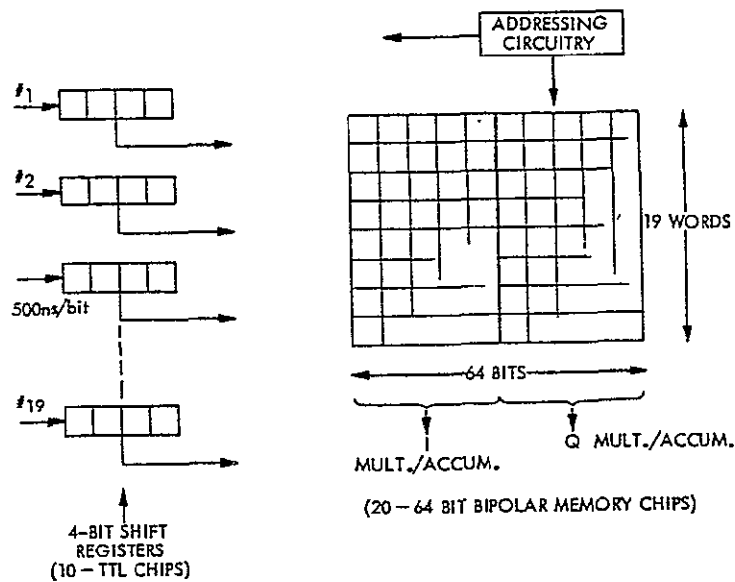


Fig. 4-7(e) Interpolation Filter Buffer

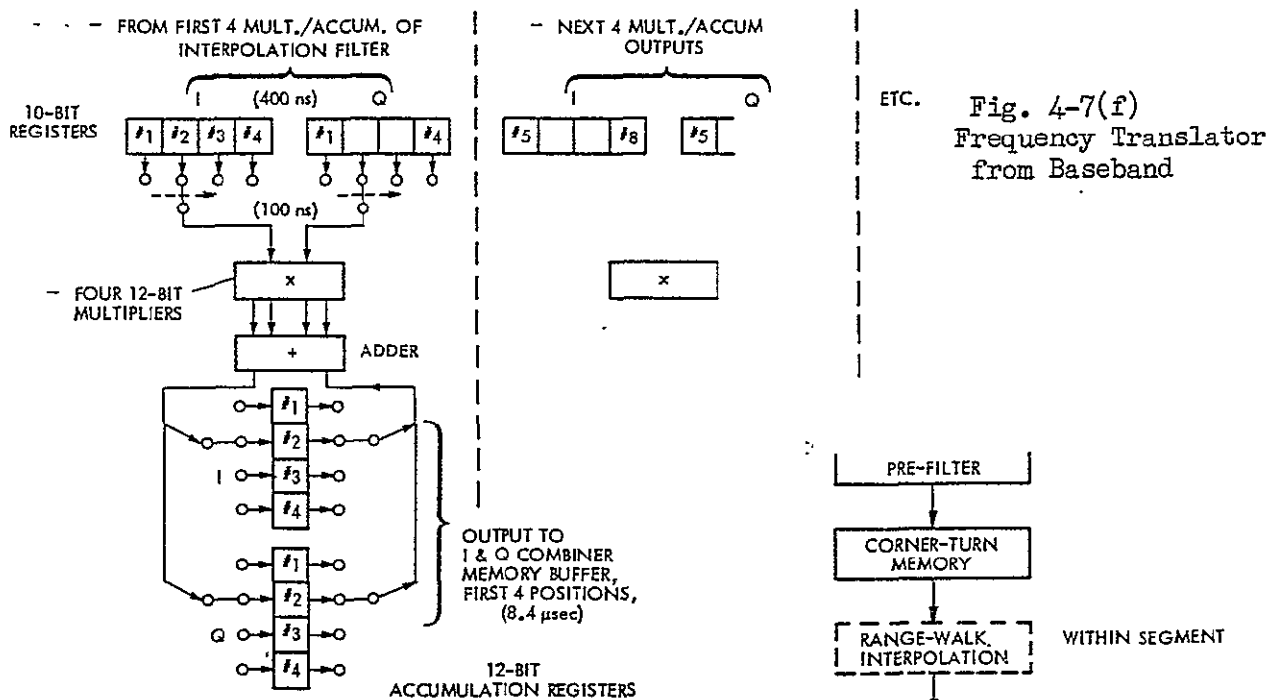


Fig. 4-7(g) Range-Walk Implementation

- WORST-CASE IS 20 RANGE CELL VARIATION OCCURRING AT THE EQUATOR.
- INTERPOLATION MUST BE DONE WITHIN AND BETWEEN SEGMENTS.

Section 5

PROCESSOR CONTROL REQUIREMENTS

The auxiliary signal inputs needed to control the linear approximation azimuth processor are identified and the required precision for these parameters is derived. The function of these auxiliary data is to provide parameters for adjustment of the processor reference function and to establish timing references for data flow within the processor.

The need to adjust the processor reference function arises from orbital variation in the relative velocity vector between the spacecraft and the target or image area. Specific causes of these variations are orbit eccentricity, gravitational field anomalies, antenna attitude errors, and target latitude. Since the processor is an approximate matched filter to the phase versus time history of each target point, its performance depends on the accuracy with which the phase history is known. This dependence is generally independent of the processor algorithm or architecture and the requirements derived below for auxiliary data apply to any processor satisfying the requirements defined in the statement of work. The types of auxiliary data needed in the azimuth processor are determined by the need to: 1) point the processor to the area illuminated by the radar antenna; 2) focus the processor to match the signal phase curvature; 3) correct for range migration of targets; and 4) register multiple independent looks at the same target area. These processor functional requirements can be satisfied only if the linear and quadratic phase versus time is accurately known for the collected radar data. The processor performance requirements used to derive the needed auxiliary data accuracy were as follows:

1. Processor Pointing - less than 1 dB signal to noise ratio loss in worst of four independent azimuth looks (i.e., the look which corresponds to the lowest gain portion of the real antenna beam)
2. Processor Focus - less than 2 percent spreading of azimuth impulse response (IPR) width (25 m)

3. Range Migration - less than 1/4 range IPR cell migration across 4 contiguous azimuth looks
4. Multi-Look Registration - less than 1/4 image cell misregistration between any 2 of 4 independent contiguous azimuth looks

The processor pointing requirement dictates the accuracy with which the doppler centroid of the collected radar data must be known. This doppler centroid is determined by the azimuth squint angle of the radar antenna and by the Earth rotation velocity at the intersection of the antenna beam with the Earth surface. Error in the knowledge of this doppler centroid would cause the processor to be matched or pointed to targets away from the antenna boresight, thus causing loss in antenna gain and image signal to noise ratio. Furthermore, since the radar PRF folds the sidelobe doppler towards the main doppler beam, any error in centering the imaged area boresight will tend to increase the ambiguous clutter in the image. The requirement for less than 1 dB signal to noise ratio loss in the worst azimuth look corresponds to roughly 10 percent of the antenna 3 dB doppler beamwidth in the case of SEASAT-A where 4 looks are obtained across a 1500 Hz doppler beamwidth. The resulting requirement on the auxiliary data is knowledge of the doppler centroid to within ± 150 Hz.

The processor focus requirement dictates the needed accuracy of the quadratic phase curvature of the signal history. This corresponds to the doppler chirp rate for the collected data. A 2 percent spreading in the IPR width due to focus error requires that the quadratic phase error be less than $\pi/4$ radians at the aperture ends. This corresponds to ± 2.3 Hz/sec doppler chirp rate error. It is shown below that registration of adjacent azimuth looks places a much tighter constraint on knowledge doppler chirp rate; therefore, questions of depth of focus will be deferred to the discussion of registration error.

Correction for range migration effects consists of maintaining the response due to each target within a single range cell over the entire integration

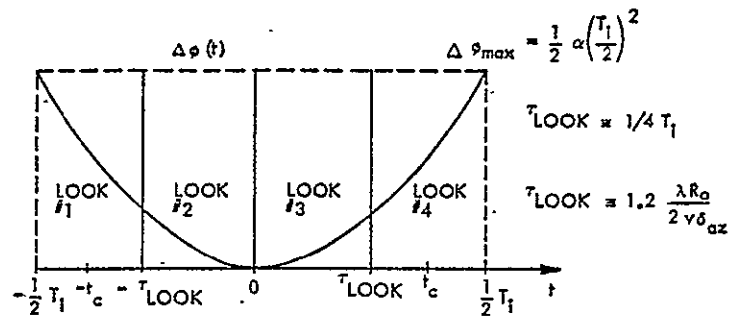
time. The extent of a range cell in the slant plane is about 9.5 m for SEASAT-A, and the integration for a single look is .66 seconds. Control of a target's range bin to within 1/4 IPR cell over this time period requires knowledge of the line-of-sight velocity to within 3.6 m/sec. The constraint to within 1/4 cell minimizes the amplitude modulation (i.e., less than one dB) introduced into the signal history as the target migrates across a range cell and is corrected back to its original position.

Registration in range of four independent looks leads to a more stringent requirement on line of sight velocity. In this case a target must be maintained in the same cell for 2.64 seconds requiring knowledge of line of sight velocity to within 0.9 m/sec. Since the velocity is continuously varying as the target latitude changes the line of sight, velocity must be updated frequently. The line of sight component of Earth rotation velocity for the reference SEASAT-A, type of orbit is:

$$V_{\text{Los}} \approx 169.5 \sin \omega_s t \text{ (m/sec)}$$

where t is time from the northern most point of the orbit and $\omega_s t$ is the orbit angular rate. This leads to a requirement to update the latitude every five seconds when operating near the poles and less often elsewhere.

Registration in azimuth of multiple independent looks requires geometric distortion within each look to be less than 1/4 IPR cell and that the relative location of a given point within each image be known to within 1/4 IPR cell. The piecewise linear approximation processor does not introduce any geometric distortion. The relative location of points within the image format is determined by linear phase versus time errors across each aperture. If the linear phase error in each aperture is within a certain bound of each other aperture, a given point will appear at the same IPR cell in each look. The principle cause of a difference in the linear phase error in each look is an uncertainty in the overall (4 look) phase curvature. Figure 5-1 illustrates that where it can be seen that a given uncertainty is quadratic phase versus Time, to equal focus (or curvature) error in



- CONSIDER DOPPLER CHIRP RATE ERROR ($\Delta \alpha \text{ rad/sec}^2$):

$$\text{PHASE ERROR} = \Delta \phi(t) = 1/2 \Delta \alpha t^2$$

t = TIME FROM CLOSEST APPROACH

- EXPAND IN SERIES ABOUT CENTER TIME OF 4TH LOOK (t_c):

$$1/2 \Delta \alpha t^2 = \underbrace{1/2 \Delta \alpha (t-t_c)^2}_{\text{FOCUS}} + \underbrace{\Delta \alpha t_c (t)}_{\text{SQUINT}} + \underbrace{1/2 \Delta \alpha t_c^2}_{\text{CONSTANT}}$$

Fig. 5-1 Doppler Chirp Rate

PARAMETER	DOMINANT ERROR CRITERION	CONSTRAINT
DOPPLER CENTER FREQUENCY - f_c	SNR LOSS IN 1ST OR 4TH LOOK ≤ 1 dB	$\Delta f_c \leq \pm 150$ Hz
DOPPLER CHIRP RATE - \dot{f}	MISREGISTRATION OF 1ST AND 4TH LOOKS $\leq 1/4$ AZIMUTH CELL	$\Delta \dot{f} \leq \pm 0.25$ Hz/SEC
LINE-OF-SIGHT TARGET VELOCITY - V_{LOS}	MISREGISTRATION OF 1ST AND 4TH LOOKS $\leq 1/4$ RANGE CELL	$\Delta V_{LOS} \leq 0.9$ M/SEC
DEPTH OF FOCUS IN RANGE - DOF	ALL RANGE CELLS IN EACH DOF HAVE $\Delta \dot{f}$ WITHIN 0.25 Hz/SEC OF EACH OTHER	DOF ≤ 40 RANGE CELLS
SYSTEM TIMING ACCURACY Δt	TIMING ERROR LESS THAN ONE RANGE CELL (9.6M)	$\Delta t \leq 64$ n/SEC

Table 5-1 Processor Control Requirement Summary

each look results but with different squint (or pointing) error. This is further illustrated by the series expansion of phase error about the center of each aperture, also shown in Fig. 5-1, where a linear phase term is seen to be proportional to the error, $\Delta \alpha$, in the phase curvature and to the distance of aperture center from time of closest approach. The focus constraint on $\Delta \alpha$ is less than 2.3 Hz/sec as discussed previously. The registration constraint requires that $\Delta \alpha$ is less than 0.25 Hz/sec to register the first look with the fourth look to within 1/4 IPR cell.

An additional factor which must be recognized in the processor design is that the phase curvature is a function of range and must be known to within the desired accuracy at all points within the range swath. The basic relationship for phase curvature or doppler chirp rate is

$$\dot{f} = \frac{2V^2}{\lambda R}$$

where V is the Satellite Velocity, R is the slant range, and λ is the radar wavelength. The differential of this relation versus ΔR is

$$|\Delta \dot{f}| \approx \frac{2V^2}{R^2} |\Delta R|$$

This relation should be constrained by the maximum doppler chirp rate error derived for registration of multilook: 0.25 Hz/sec. This gives a maximum ΔR of 386 meters for SEASAT-A parameters of $V = 7500$ m/sec and $R = 860$ km. This result says that a different reference phase curvature is required for each 386 meters of slant range swath. This is about every 40 range IPR cells; therefore, a 4000 cell range swath would require 100 different phase reference functions across the swath. Since the processor is particular about which set of 40 cells to apply a given reference function, the system clock must be accurate to within 64 ns - the round trip propagation time for one range cell.

A summary of the derived requirements auxiliary data for processor control is given in Table 5-1. The driving factor in the difficulty of these requirements is the desire to register 4 independent azimuth looks to with-

in $1/4$ IPR cell. This increases the needed accuracy processor control by an order of magnitude. If these looks were to be registered on the ground rather than in space at the output of a 4-look processor other methods could be applied. In that case the parameter accuracy requirements would be considerably easier to achieve.

Section 6

AZIMUTH PROCESSOR SIZING AND PERFORMANCE

The real time SAR azimuth processor is required to be suitable for use in a space vehicle hence the IC chips must be space qualified. Factors in IC chip selection are high reliability, low power operation, thermal stability and radiation tolerance. In general, the first two qualities are not currently associated with LSI chips. The principal thrust in the development of LSI chips is from commercial, rather than military or space applications. Low power operation, while very important in space equipment, is of little concern in most commercial ground applications, and is usually not associated with LSI.

The semiconductor of most importance with respect to low power operation is CMOS-on-sapphire. However, there is not much interest in this category for commercial applications at present - the primary thrust is in N channel MOS. The LSI devices currently manufactured with N MOS technology are deficient in tolerance to the radiation environment present in space applications. Bipolar and CMOS-on-sapphire devices are much more radiation tolerant.

Conventional current or soon to be available LSI devices are not well suited to the low power, radiation resistant, and high reliability requirements of a spaceborne SAR processor. The use of parts that are suitable would lead to excessive processor size or reduced performance. An exception to the above is the line of arithmetic chips made by TRW which satisfy the requirements: they are, LSI, bipolar, comparatively low power, Mil-Spec, and very fast. In addition the federal government sponsored Very High Speed Integrated Circuit (VHSI) program is expected to develop space qualified functionally equivalent versions of currently available commercial LSI chips. Since the VHSI development is anticipated to produce space qualified components of characteristics similar to current conventional LSI, implementation estimates were based on conventional LSI parameters where components from the TRW line were not available (mainly in the memory area).

Since the processor performance is most closely related to chip count, and, via this measure, to size-weight-and-power, the measurable parameter of most importance is the chip count for a given processor performance. For purposes of estimating the size it is assumed that the chip packing density is 1,300 chips per cubic foot, representative of commercial wire-wrap construction. Power can be estimated from a rough rule of 0.3 watts per IC. This figure is adequate for LSI and TTL devices, and is not satisfactory for CMOS, or chips packaged with more than 16 pins. No CMOS is used in the two architectures considered in this study, but a correction factor can be included in the chip count to account for the larger chips if their percentage use becomes significant.

In the baseline design, essentially all chips used were bipolar. The exception was the use of 64K MOS memory devices for the alignment function. The Improved Baseline Design was implemented with LSI chips throughout, which are representative of anticipated spaceworthy microcircuits in the 1980's.

The Baseline and Improved Baseline designs described in Section 4 were sized to the chip count level for 19 segments, 25 meters resolution, and 4000 range cells. The allocation of memory, arithmetic, and overhead chips to each processor function is given in Table 6-1. Although neither design is fully optimized, the value of the design improvements is evident by the reduction of chip count by a factor of 2.5.

The performance for these two designs are represented by Figures 6-1 and 6-2 which plot the normalized impulse response of the 19 segment processors. It can be seen by comparison of these figures that the 19 segment Improved Baseline has both its 1st and 2nd sidelobes degraded by about 4 dB relative to the Baseline Design. The integrated sidelobe ratio would be degraded by a similar amount. This difference in performance can be remedied by increasing the number of segments in the Improved Baseline. This is illustrated in Figures 6-3 and 6-4 where 21 and 23 segment impulse responses are plotted. Also Figure 6-5 gives PSLR versus the number of segments for

IMPROVED BASELINE

	MEMORY	ARITHMETIC	OVERHEAD
PREFILTER	32	6	26
LOW-PASS CORNER-TURN	110	-	20
FREQUENCY TRANSLATE, DOWN	-	16	150
LOW-PASS FILTER	60	32	46
ALIGNMENT MEMORY	170	-	25
INTERPOLATION	90	28	70
FREQUENCY TRANSLATE, UP	<u>30</u>	<u>28</u>	<u>110</u>
	490	110	450

TOTAL CHIP COUNT = 1200

(INCLUDES 150 CHIPS FOR RANGE WALK FUNCTION)

Table 6-1A

IMPROVED BASELINE

	MEMORY	ARITHMETIC	OVERHEAD
FREQUENCY TRANSLATION	20	70	80
INTEGRATE AND DUMP	630	80	70
MAIN MEMORY	1100	-	400
ACCUMULATOR AND MULTIPLEXOR	-	80	280
PHASE CORRECTION, RANGE INTERPOLATION, AND SIGNAL COMBINING	110	120	80
ALIGNMENT MEMORY	<u>350</u>	<u>-</u>	<u>40</u>
	2200	350	950

TOTAL CHIP COUNT = 3500

Table 6-1B

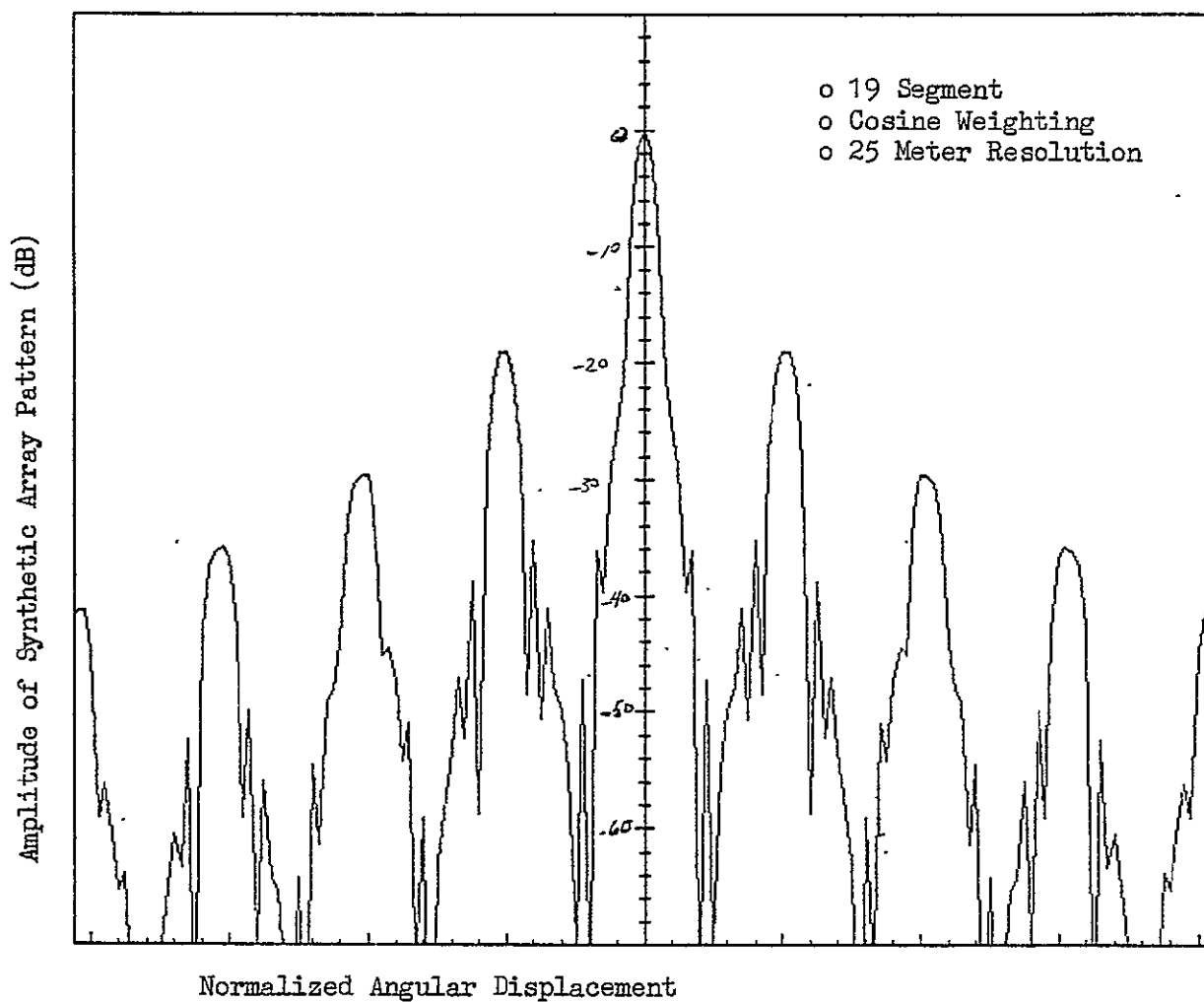


Figure 6-1 Impulse Response for Baseline Processor

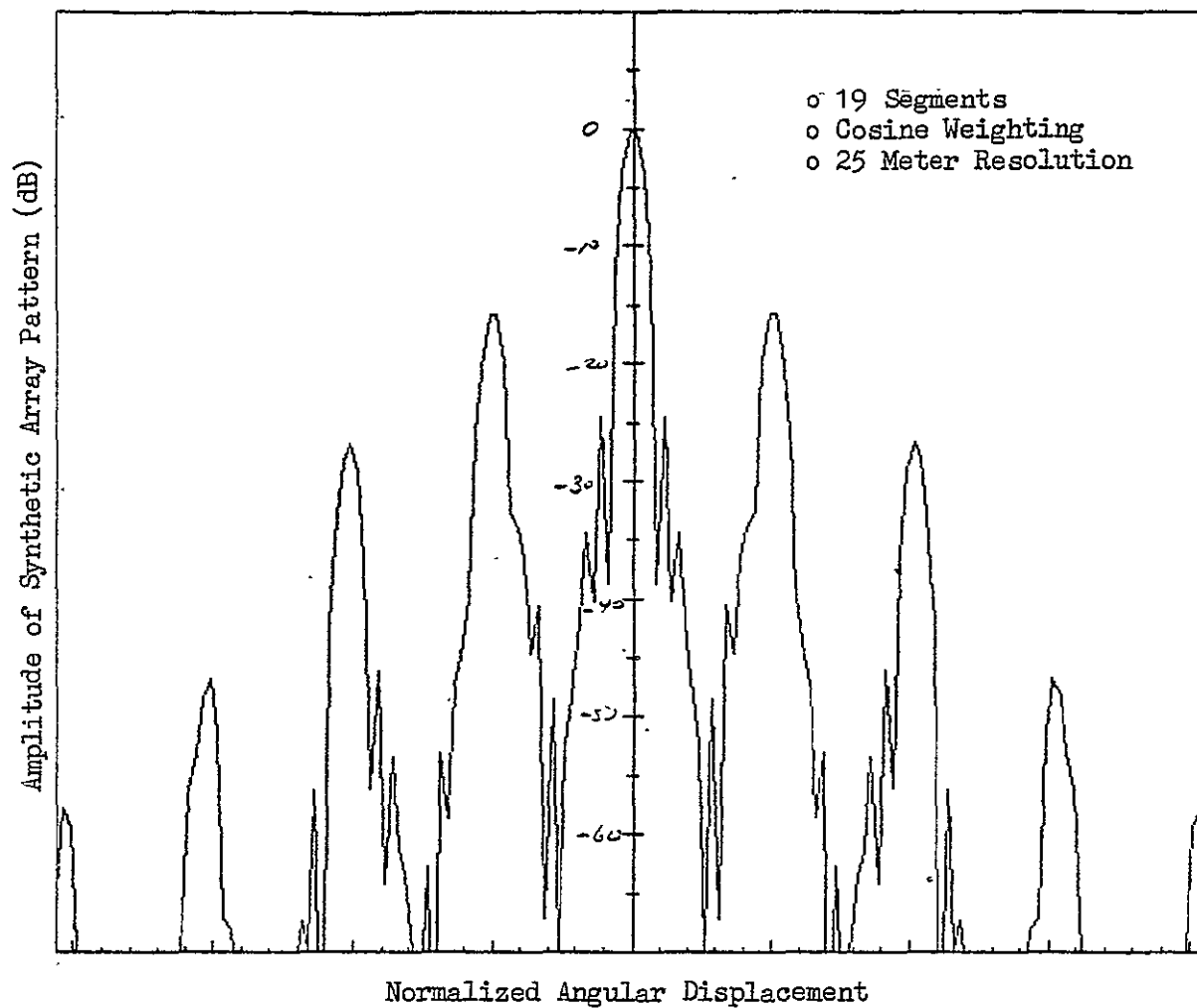


Figure 6-2 Impulse Response for Improved Baseline Processor

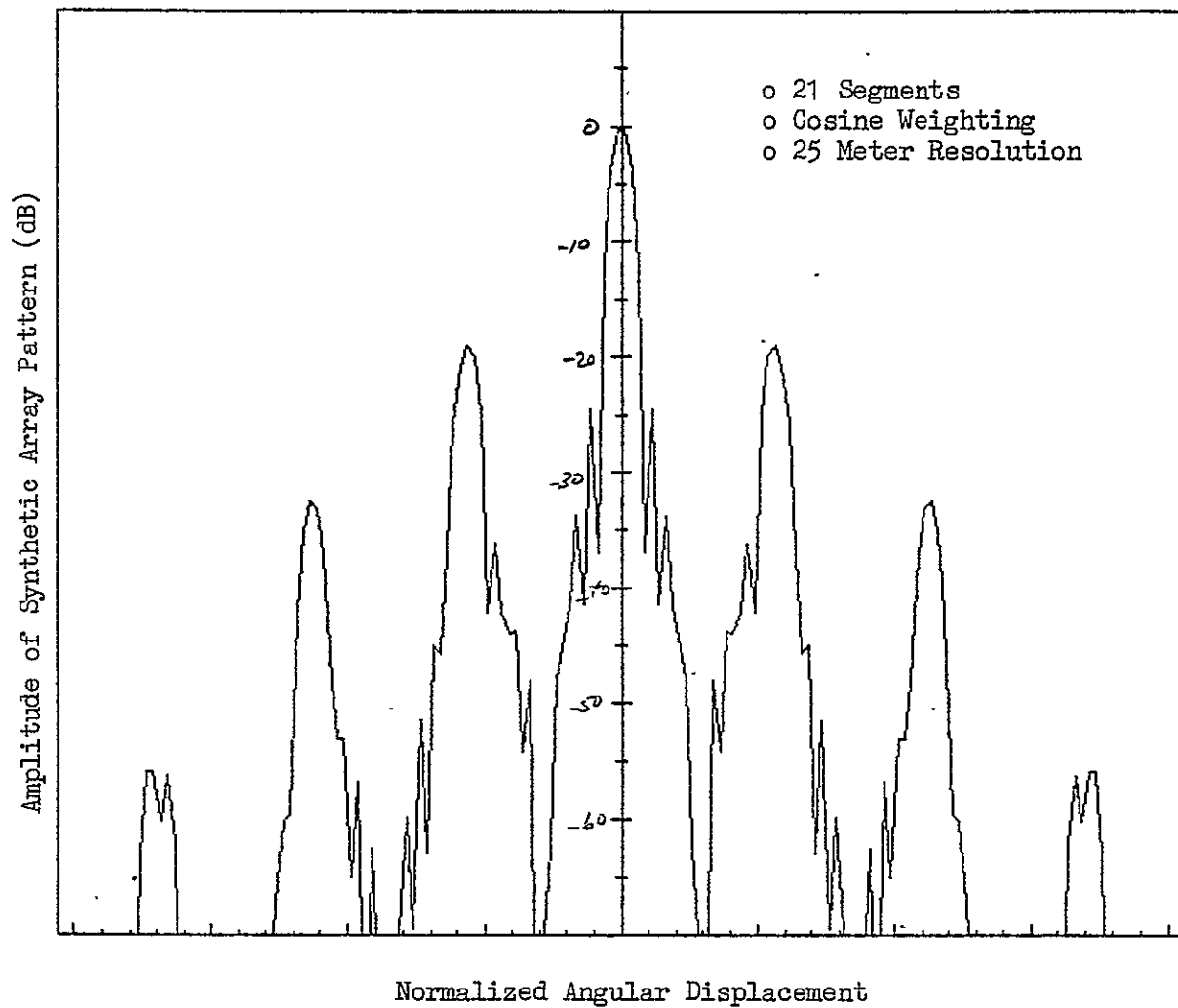


Figure 6-3 Impulse Response for 21 Segment Improved Baseline

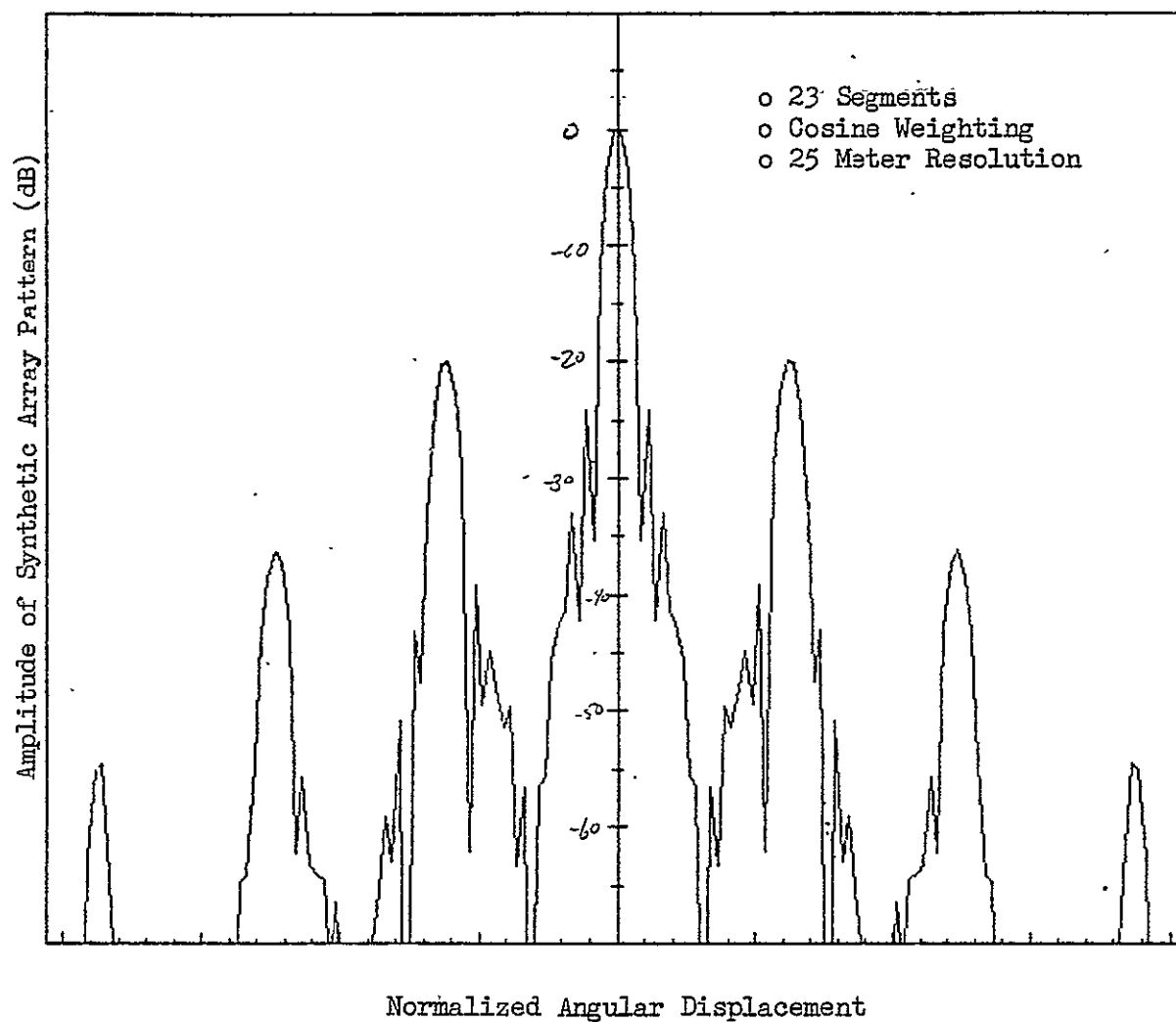


Figure 6-4 Impulse Response for 23 Segment Improved Baseline

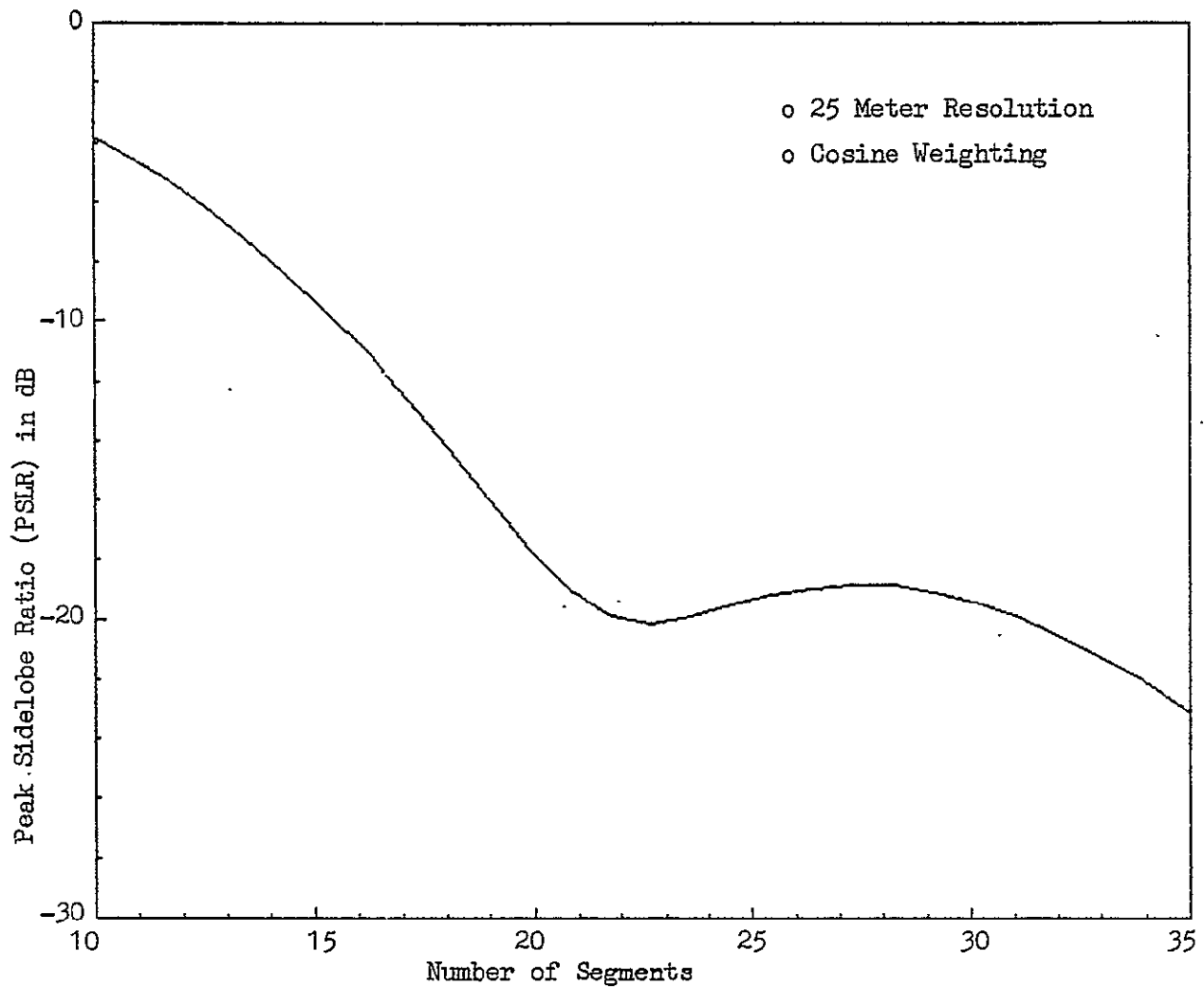


Figure 6-5 Peak Sidelobe Ratio vs. Number of Segments for Improved Baseline Processor Design

the Improved Baseline. The 22 and 23 segment Improved Baseline cases are equivalent in performance to the Baseline 19 segment design. The addition of these extra 3 to 4 segments to the Improved Baseline would raise the chip count by about 100 to 200 chips to a value of about 1400 chips total - still much reduced relative to the Baseline 19 segment design.

Estimates of the processor size scaling for other numbers of segments (fixed resolution) and for other resolutions (fixed number of segments) are given in Figures 6-6 and 6-7 respectively.

Scaling the sizing relationships of Figure 6-6 to other swathwidth requirements can be, to a first approximation, considered linear except for extreme departures from the 4000 range cell swathwidth requirement used in the point design. There is a slight preference for range swaths which are powers of 2 or slightly less in size; however, this is not a very significant design driver. That is, halving the swathwidth reduces the processor size by an approximate factor of 2. A similar linear relationship exists for the number of looks required; the chip count is negligibly larger than four times as great for a four-look processor over that required for a one-look processor; an incremental chip count being required for the additional processor control necessary to meet the multi-look registration requirements.

The scaling of the processor size to other radar system parameters can be seen by the relationship for the azimuth compression ratio (i.e., time-bandwidth product).

$$TB = \frac{\lambda R}{2\delta_a^2}$$

Thus the processor size would scale in a roughly linear manner relative to changes in wavelength (λ) or slant range (R). An exception to this would occur if the ratio of resolution (δ_a) to wavelength were to be less than a factor of five. In that case higher order phase corrections would be required and the processor complexity would grow nonlinearly with increased wavelength.

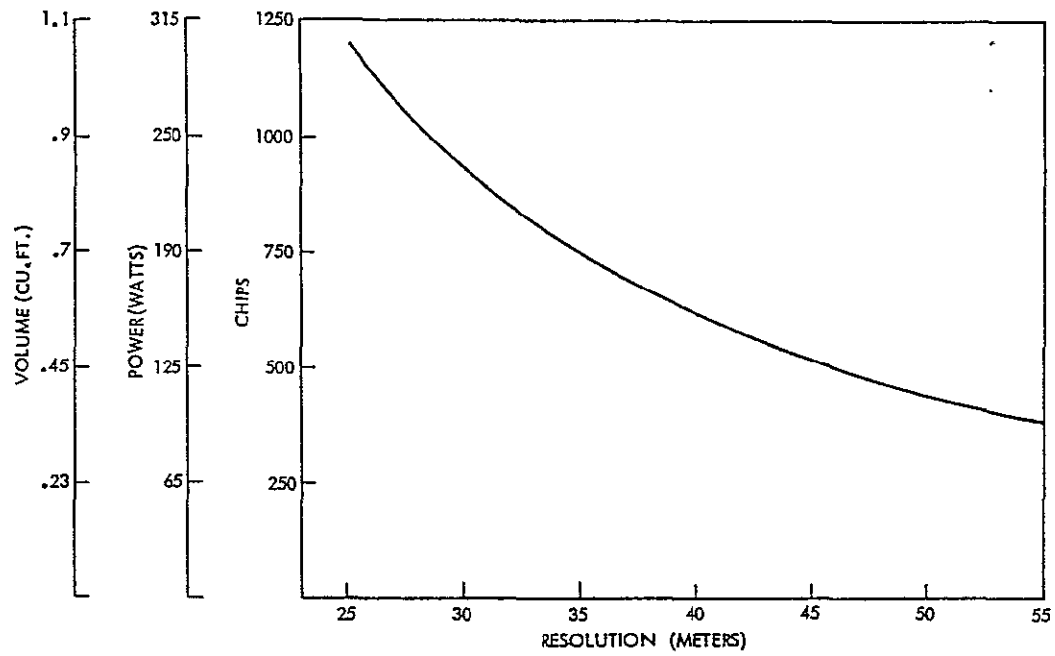


Figure 6-6 Improved Baseline Processor - Chip Count vs. Resolution
19 Segments - 4,000 Range Cells

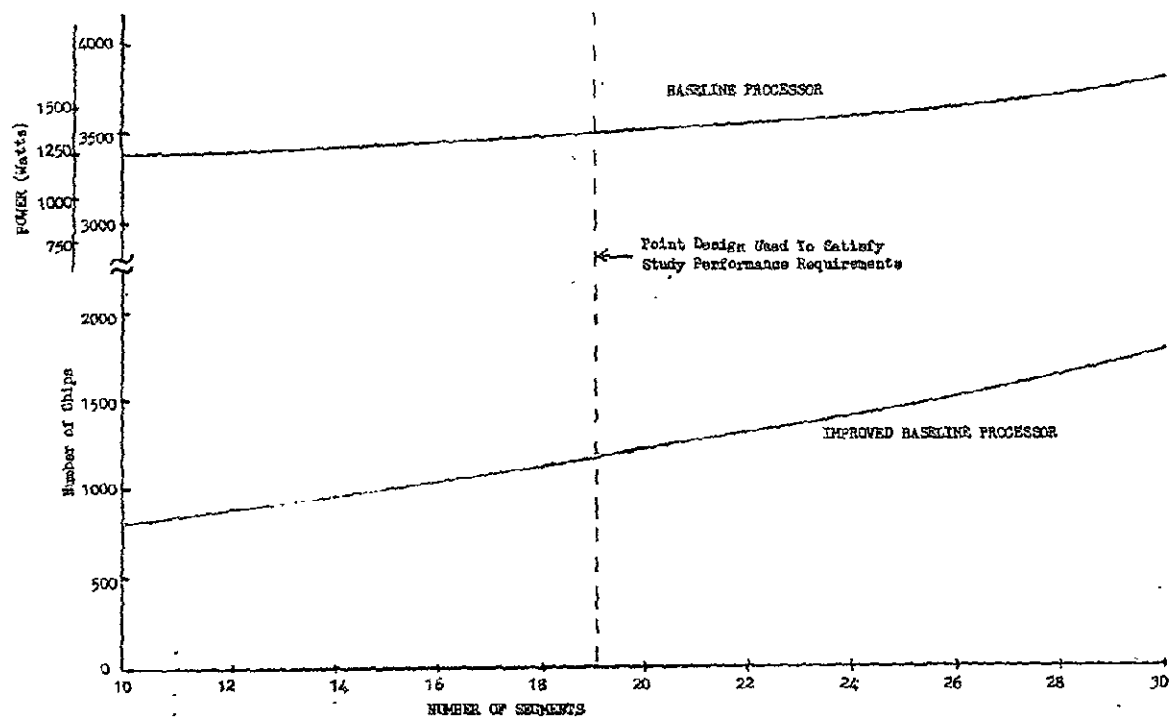


Figure 6-7 Chip Count/Power vs. Number of Segments for 25 Meter Resolution

APPENDIX A

THE QSARP TIME-DOMAIN SIMULATION

The purpose of this report is to describe the Baseline processor time-domain simulation carried out jointly by the Institute for Advance Computation (IAC) and LMSC.

OBJECTIVES

The objectives of the simulation study were:

1. To realize a reasonable detailed simulation of the Linear Approximation processing concept in the time domain; i.e., using the same algorithm proposed for the hardware design of the Baseline processor. Previous Linear Approximation simulations have used a mathematically equivalent but functionally different frequency domain or "matched filter" algorithm.
2. To include in the simulation a means for restricting accuracy of the computations to any desired number of bits precision.
3. To investigate parametrically the effects of restricted accuracy computations on SAR image quality.

Since SAR considerations affecting range or cross-track performance are not an issue so far as the Linear Approximation concept is concerned, it was decided at the outset that only a single range bin would be simulated. The reduction of the processing problem to a single dimension (along-track) simplifies programming and, even more important, reduces computer core memory requirements to a manageable size.

Thus, the total simulation package required not only that Baseline design hardware be suitably modeled on the computer, but also that a program to generate simulated input data relevant to a single range bin be written. These programs were developed by IAC implementing algorithms supplied by LMSC. The total package also includes programs to analyze the simulated processor output data generated by the above programs and produce quantitative measures of its quality. These were developed at LMSC using techniques developed in the course of previous SAR studies.

SIMULATION BLOCK DIAGRAM

The Linear Approximation Processor hardware simulation program is shown in simplified block diagram form, Fig. A-1.

Fig. A-1 shows only a single segment of the complete synthetic array. It must be imagined that the entire simulation includes some number I of parallel segments (10 in the baseline systems) all brought into correct time alignment by the "alignment delays" and summed to obtain the processor output. The "integrate and dump" (ID) operation sums several (say, Q): input pulses (4 in the baseline system) so that the data rate is reduced by the factor Q beyond this point. The "moving window integrator" (MWI) sums the last S ID outputs (14 in the baseline system). The total number of pulse integrated is therefore IQS (1,064 for the baseline system). The parameters are all inputs to the processor simulation program. The baseline system values indicated were used for most simulations, though a few tests were made using other values. A fully focused output, i.e., one that does not involve the piece-wise linear approximation to the SAR quadratic phase function, can be obtained by setting $Q = S = 1$.

The program for generating simulated input signal superposes any desired number of point-target responses, each with adjustable amplitude, phase, and along-track position. Simulated signals actually used in the various runs included:

1. A single point target (mainly for purposes of program test and verification)
2. A single point target of interest plus 16 others representing clutter. The clutter points were randomly placed in the region 600-1600 m downrange from the target of interest. Amplitudes were chosen to provide signal/clutter power ratio of 0 db.
3. Same as 2, but with signal/clutter of -10 db.

Amplitude distributions of both the real and imaginary parts of the two

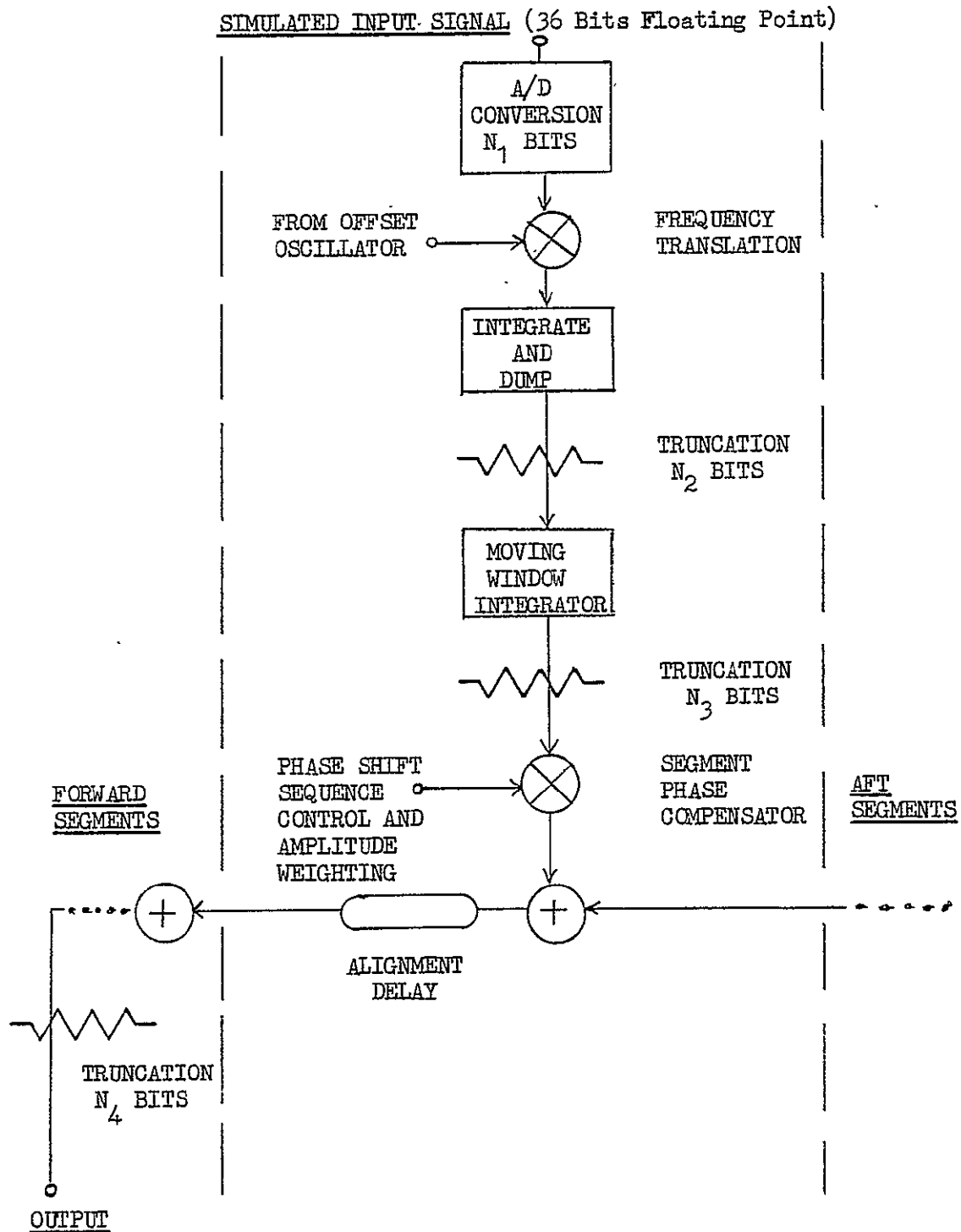


Figure A-1 Segment Processor Truncation Points Used in IAC QSARP Simulations

"signal plus clutter" input signals were approximately normal except on the tails of the distribution (i.e., beyond 3 standard deviations). This is exactly as would be expected for the -10 db S/C case at least, since addition of only 17 sinusoids would not be expected to produce values extremely large in magnitude. That the 0 db S/C case produced almost identical distributions is probably fortuitous.

The A/D conversion at the input to the processor program is to a sign-magnitude representation of the simulated signal with N_1 bits precision, including sign. Such conversion results in an odd number of possible output values -- specifically $2^{N_1} - 1$. The three truncation points indicated in the figure each occur after integration has produced higher output levels corresponding to increased bits precision. At these points precision can be scaled back to N_2 , N_3 , and N_4 bits precision by simply dropping the least significant bits. Such truncation is accompanied by the introduction of a non-linearity in the vicinity of zero, but has the advantage of introducing no bias.

No claim is made that either the A/D conversion or the truncation is optimum. In both cases a choice had to be made and these are presumed to be representative insofar as their influence on processor accuracy is concerned. It should perhaps be noted that for the baseline parameters (4 pulses summed per sub-segment, 14 sub-segments per segment, and 19 segments in the synthetic array) the increase in number of bits resulting from integration is bounded as follows:

$$\begin{aligned} N_2 &\geq N_1 && + 2 \\ N_3 &\geq N_2 && + 4 \\ N_4 &\geq N_3 && + 5 \end{aligned}$$

will be equivalent to no added truncation. In the simulation runs, N_1 was usually 6 bits but for some purposes full machine precision (36 bits floating point) was used. For $N_1 = 6$ bits, N_2 was varied between 2 and 8 bits,

SIMULATION PARAMETER	SYMBOL					
1. INPUT SIGNAL/CLUTTER	S/C	0 dB	← 0 dB and -10 dB →			
2. INPUT A/D LOADING FACTOR	K	1-12	3.5	3.5	3.5	3.5
3. INPUT A/D CONVERSION BITS PRECISION	N ₁	6	6	6	6	6
4. TRUNCATED WORD SIZE AT OUTPUT OF THE INTEGRATE/ DUMP, BITS	N ₂	F.P.	2-8	4	6	8
5. TRUNCATED WORD SIZE AT OUTPUT OF THE MOVING WINDOW INTEGRATOR, BITS	N ₃	F.P.	F.P.	4-7	6-9	8-11

F.P. = FULL PRECISION, 36 BITS FLOATING POINT

Table A-1 - Summary of the Simulation Runs

the last corresponding to no truncation. On grounds that it is implausible one would retain accuracy at the N_2 truncation point only to discard it later, N_3 was varied from N_2 to $N_2 + 4$. In this study, the N_4 truncation was not used, which is equivalent to $N_4 = N_3 + 5$ in all cases. Table A-1 summarizes the truncation parameters for the simulation runs.

PROGRAM VERIFICATION

Program verification was accomplished primarily by means of two runs using system parameters chosen expressly for the purpose:

1. Simulated signal from a single point target was used.
2. The effect of full focus was simulated by "summing" only one pulse in the ID and only one ID output in the MWI.
3. The synthetic aperture was uniformly weighted.

With the above choices, the processor output should approximate a $\sin X/X$ function where X is, up to a multiplicative constant, the along-track coordinate.

4. The PRF was reduced to provide exactly one sample value per secondary lobe of the $\sin X/X$ function (in general, two on the primary lobe). This data rate corresponds to sampling the signal at exactly the Nyquist (hence, absolute minimum) rate.

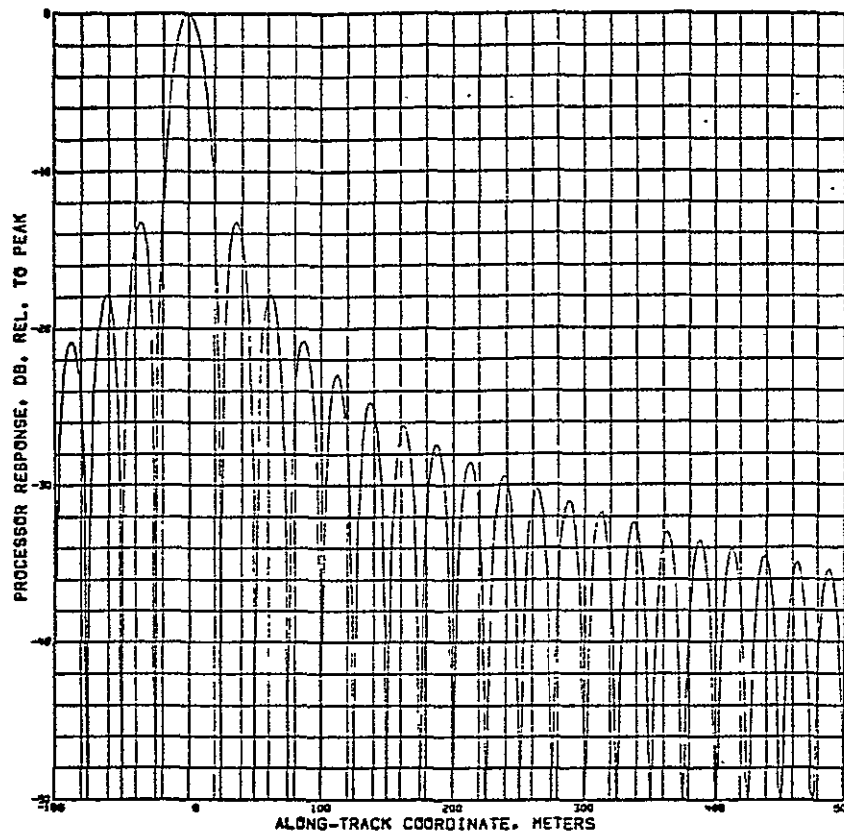
In one simulation, the single target point was placed exactly at a resolution cell center. With the target so positioned the simulated processor output would ideally be a single non-zero value (at the center of the principle lobe) and all the others zeroes (since all would be at nulls of the $\sin X/X$ pattern). In the actual simulation, the outputs that should have been zero were all at least 100 db below the single maximim, in excellent agreement with what was expected.

In the second simulation, the single target point was moved 1/2 resolution cell width down track, to the boundary between two resolution cells. For

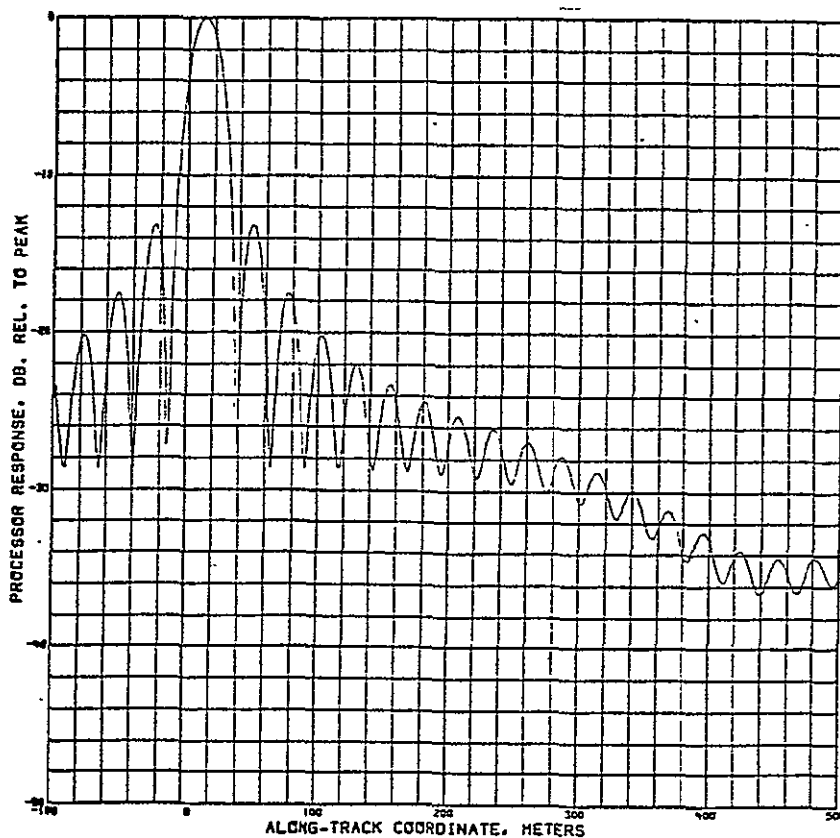
this position, expected processor output is two equal adjacent maximum values (on either side of the principle lobe) with the remaining values very near the secondary maxima of the $\sin X/X$ pattern, and hence decreasing as $1/X$ approximately. For this case several data samples near the maximum were compared with HP-97 calculations. Again agreement was excellent, the differences that were found being fully attributable to greater accuracy of the HP-97 calculation.

Besides verifying most features of the processor simulation program, the above two test runs were intended also to test a vital portion of the analysis programs. By its nature, the Baseline processor (or any) digital SAR processor outputs data points that are comparatively sparse on the point-target response function, though not at the limit of sparseness as in these test runs. Considerably denser data points are needed to locate accurately the 3 dB points on the applicable response function, to calculate ISLR, and to calculate mean square difference between similar patterns as examples. Thus a major problem in the overall simulation was to develop a suitable interpolation subroutine that could intersperse several sample values (typically eight) between each of the output points provided by the processor.

Fig. A-2 shows the results of plotting the two runs just described after FFT interpolation, the technique that was selected. It can be seen that when the target is at resolution cell center (Fig. A-2a) the $\sin X/X$ function is realized with excellent fidelity -- i.e., the lobes can be reconstructed from the zeroes very accurately. When the target is at a resolution cell boundary, however, (Fig. A-2 b) the zeroes are not sharply defined; i.e., zeroes can not be so accurately reconstructed from the maxima. However, the zeroes are some 30 db below the peak, whereas they would not have appeared at all using algebraic interpolation. Since an actual Baseline Processor output contains more dense sample points and consequently makes less demand on the interpolation subroutine than these test cases, the interpolation routine is considered acceptable.



a. Target at Resolution Cell Center



b. Target at Resolution Cell Boundary

Fig. A-2 Test Runs of Time Domain Simulation of The Linear Approximation Baseline Design

DATA ANALYSIS

Two main programs were generated at LMSC for data analysis. The first of these, called QSARP-MAIN, operates on a single simulation output data set and is useful primarily for studying point target response. After interpolating the data as described above, it determines 3 db beamwidth, calculates ISLR, and plots the processor point target response using sub-routines previously developed for these purposes. Fig. A-3 shows an example of the point target response for the baseline processor. In this example, the 3 dB beamwidth is 25.4 meters and the first-null ISLR is -15.7 dB for 6 bit data followed by truncation to 6 bits at the ID output.

Several similar cases computed verified features of the simulation not tested by the first two test runs. These include operation of the ID and MWI summers and the generation of amplitude weighting coefficients. Point target responses were essentially the same as those previously obtained using the earlier frequency domain simulations referred to at the beginning of this report, and agreed well with independently derived analytic results.

The main analysis program written expressly for this project, called SIG-NOISE, is one intended to measure the effects of limited accuracy computations on the performance of the Linear Approximation processor. Fig. A-4 shows the most important features of this program. The most difficult problem proved to be to define precisely a suitable measure of processor performance. A signal/noise type of measure was decided upon, in which noise power is associated with the mean-square difference between outputs obtained with and without the particular noise source under investigation.

Two data sets are inputs to this program, the first of which (the reference) excluded digital noise sources. The second (test case) includes the noise effects of finite word length. After interpolation, the peak signal values of the two data sets are aligned in time by shifting one entire data array as needed. The effect of scale changes that result from A/D conversion and possibly from subsequent truncations are removed by scaling the test data to match reference data as closely as possible in the least

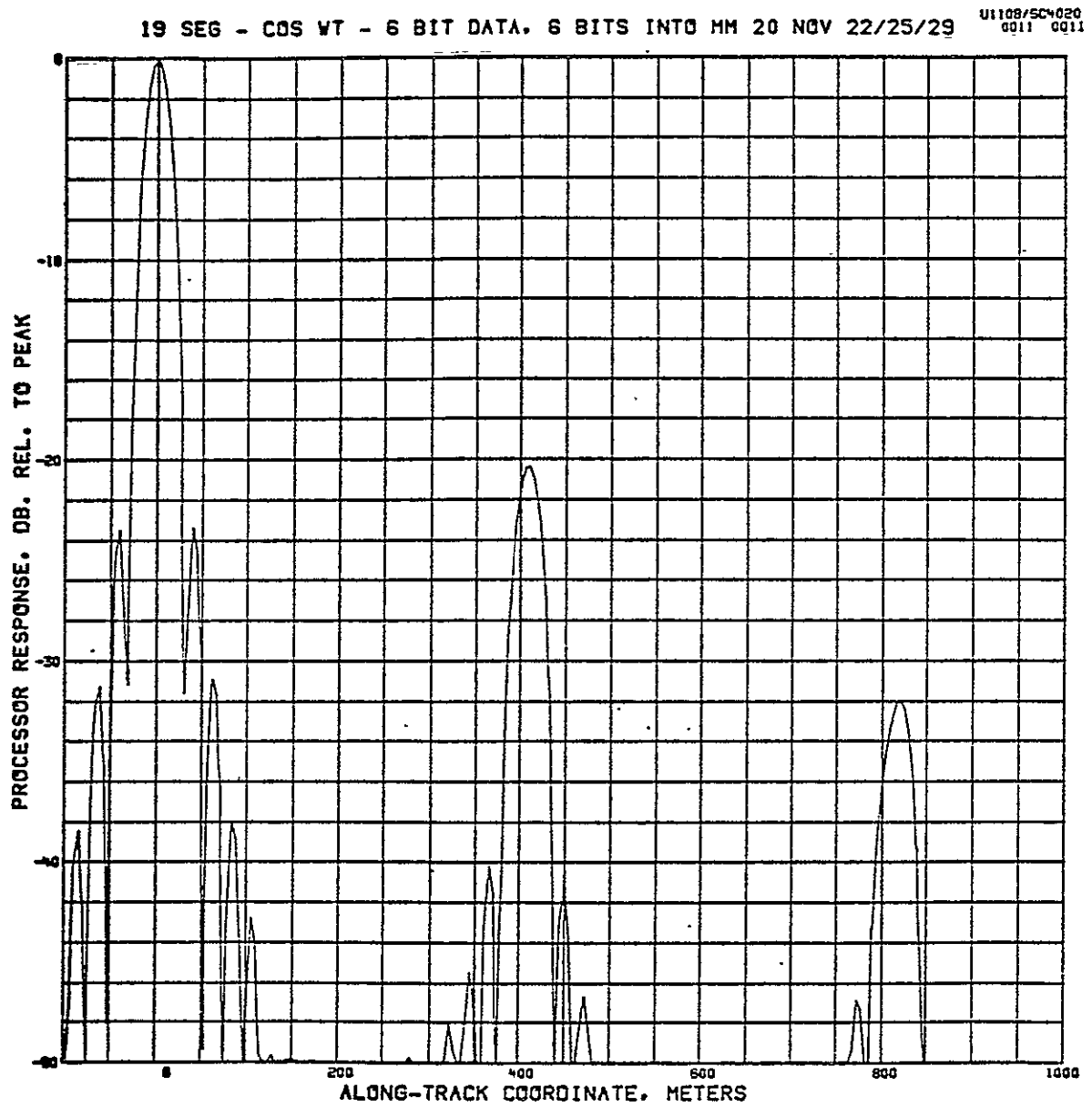


Figure A-3 Example of Point Target Response

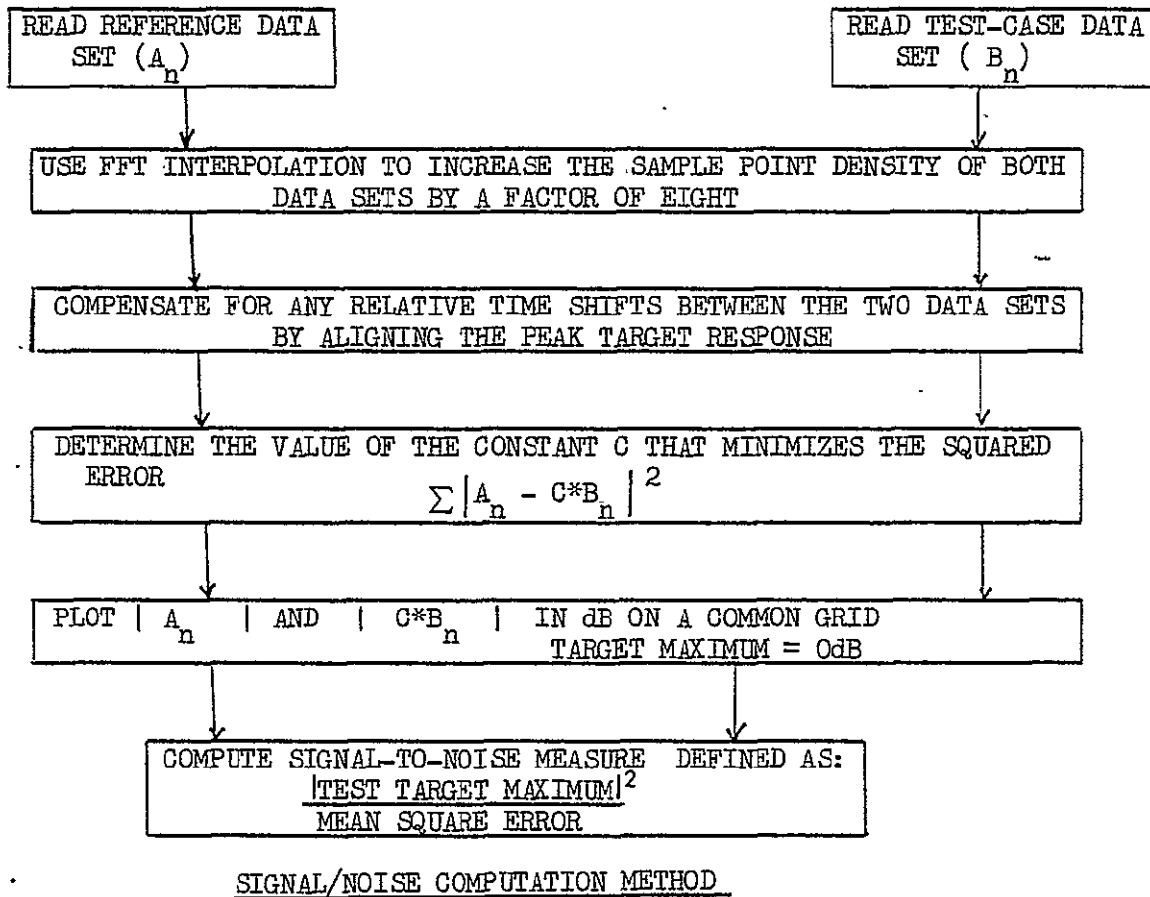


Figure A-4 Major Operations Performed by Analysis Program SIG-NOISE

squares sense. The residual (or minimum) mean square error is what is identified as noise power.

Specifically, with the set of reference data values designated $\{A_n\}$ and the set of test data values $\{B_n\}$, the program computes both SE_{min} and the complex constant C defined by:

$$SE_{min} = \left[\min_{\text{over all } C} \right] \sum_{n=1}^N \left[A_n - C * B_n \right]^2$$

The value of C is used to define signal power as:

$$S = \left[\max_{\text{over some } n} \right] \left[C * B_n \right]^2$$

where the maximization is carried out over a range of n restricted to the area where the target of interest is known to be. The signal/noise is then obtained as:

$$\text{Signal/Noise} = \frac{S-N}{SE_{min}}$$

This measure of processor performance undeniably has some problems associated with it. To obtain realistic A/D performance, it is essential to include clutter along with the target of interest, however, since the signal peak must be readily identifiable, clutter too close to the signal of interest must be excluded and the signal/clutter power ratio may not be too small. Other measures of processor performance were considered briefly but appeared too difficult to implement in the limited time available.

SIMULATION RESULTS

The major results of the various simulation runs carried out are shown on Fig. A-5, A-6 and A-7. In all three the signal/noise as defined in the preceeding section is the ordinate. In Fig. A-5, the variation in signal/

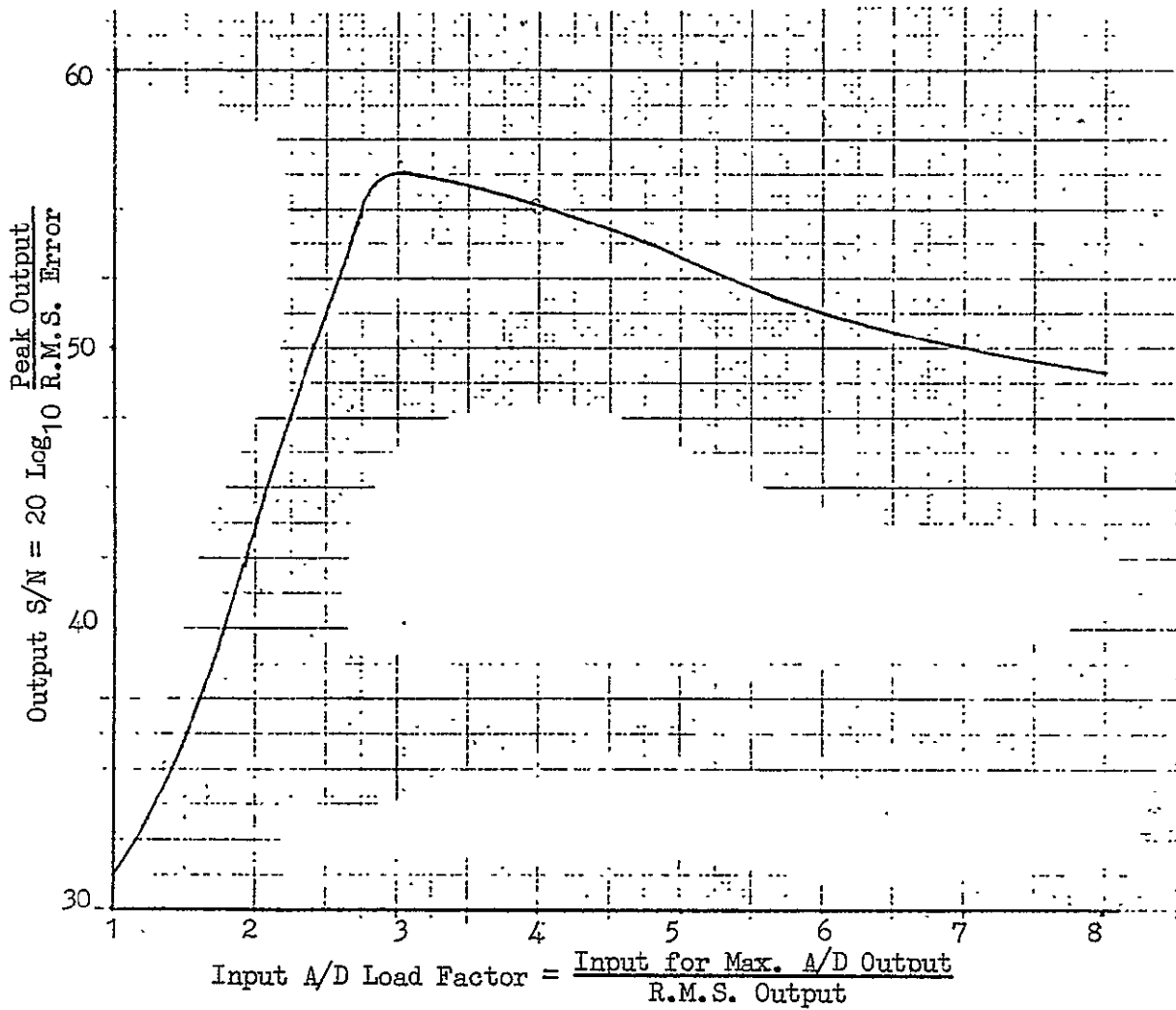


Figure A-5 Output Signal-to-Noise vs. Input A/D for 6-Bit Quantization

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noise as a function of the input A/D load factor is shown. The A/D load factor determines what range of input signal values is translated to the A/D output range. In a simulation run, the A/D load factor is determined by input SCALE, which specifies the value of input signal that is converted without rounding to maximum A/D output, (i.e., to $2^{N_1-1} - 1$). For the purposes of this project, load factor means precisely the ratio of SCALE to the RMS input signal value. Since I and Q channels are A/D converted separately, the appropriate RMS value is that applicable to either channel separately. Numerically this is the square root of 1/2 the complex input signal power. The close agreement between Fig. A-5 and previously reported analytic results for Gaussian signal statistics* is both striking and reassuring.

Fig. A-6 summarizes how the signal/noise varies for various combinations of the truncation parameters. A comparison between no quantization (i.e., full machine precision) and input A/D with 6 bit accuracy (no additional truncation) establishes an upper bound on available output signal/noise. The curves then show signal/noise as a function of input truncation variable N_2 (see Fig. A-1), with truncation parameter N_3 as a parameter. It may be seen, not surprisingly, that whenever precision is restricted, some price must be paid.

Fig. A-7 shows the same kind of data as Fig. A-6 except that the input signal/clutter ratio was -10 dB rather than 0 dB. It may be seen that all signal/noise ratios have dropped somewhat less than 10 dB. The quantitative relationship between signal/noise and signal/clutter is not clear at this time.

*Schoderbeck, J. J., "An Analysis of the Noise Introduced by Quantization and Clipping," LMSC TM 62-54-74-5.1 May 6, 1974, especially Fig. 37,
P. 16

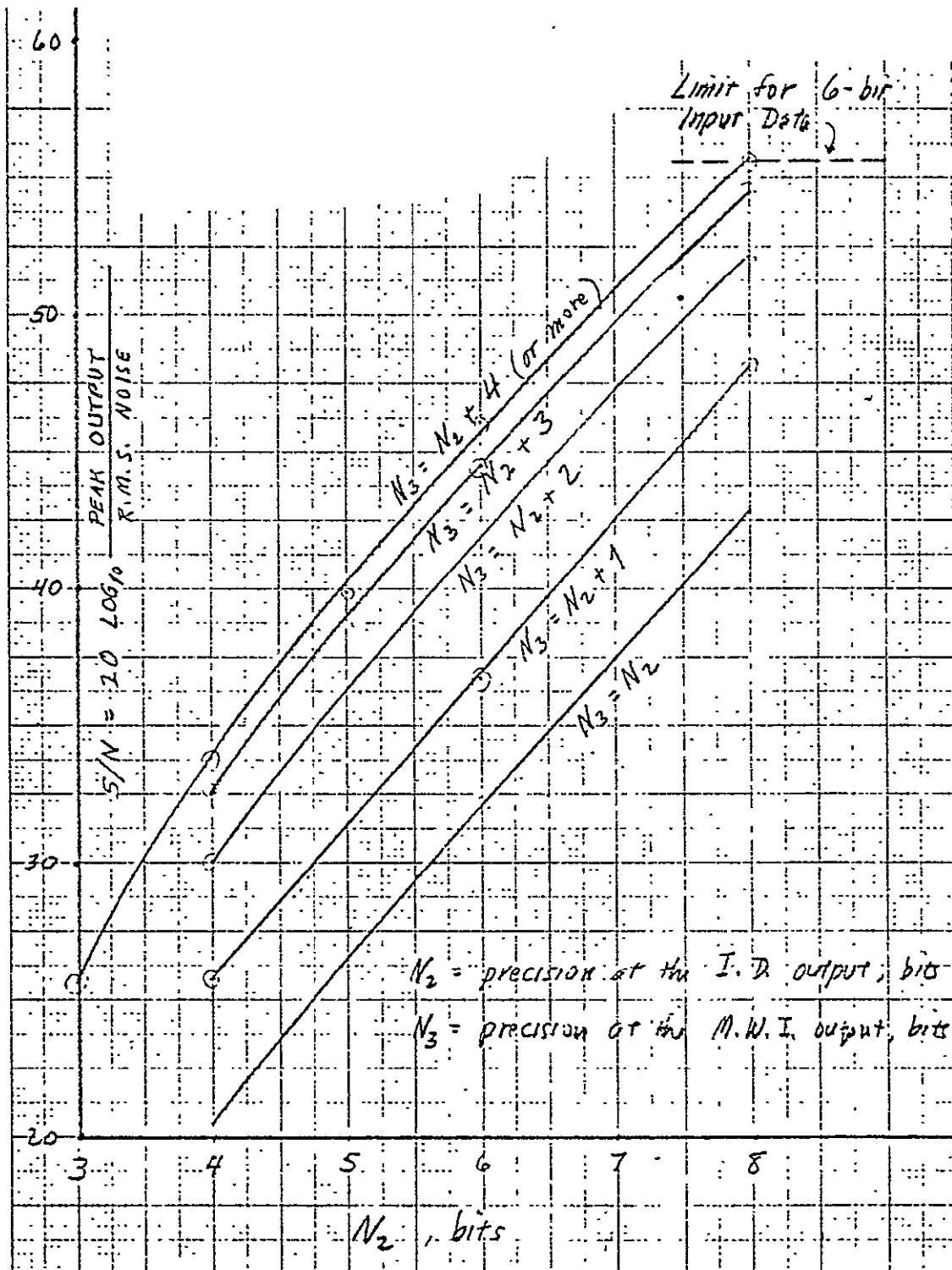


Figure A-6 Output S/N (dB) vs. N_2 (Bits) Input Data Quantized to 6 Bits
Signal/Clutter = 0dB Load Factor = 3.5

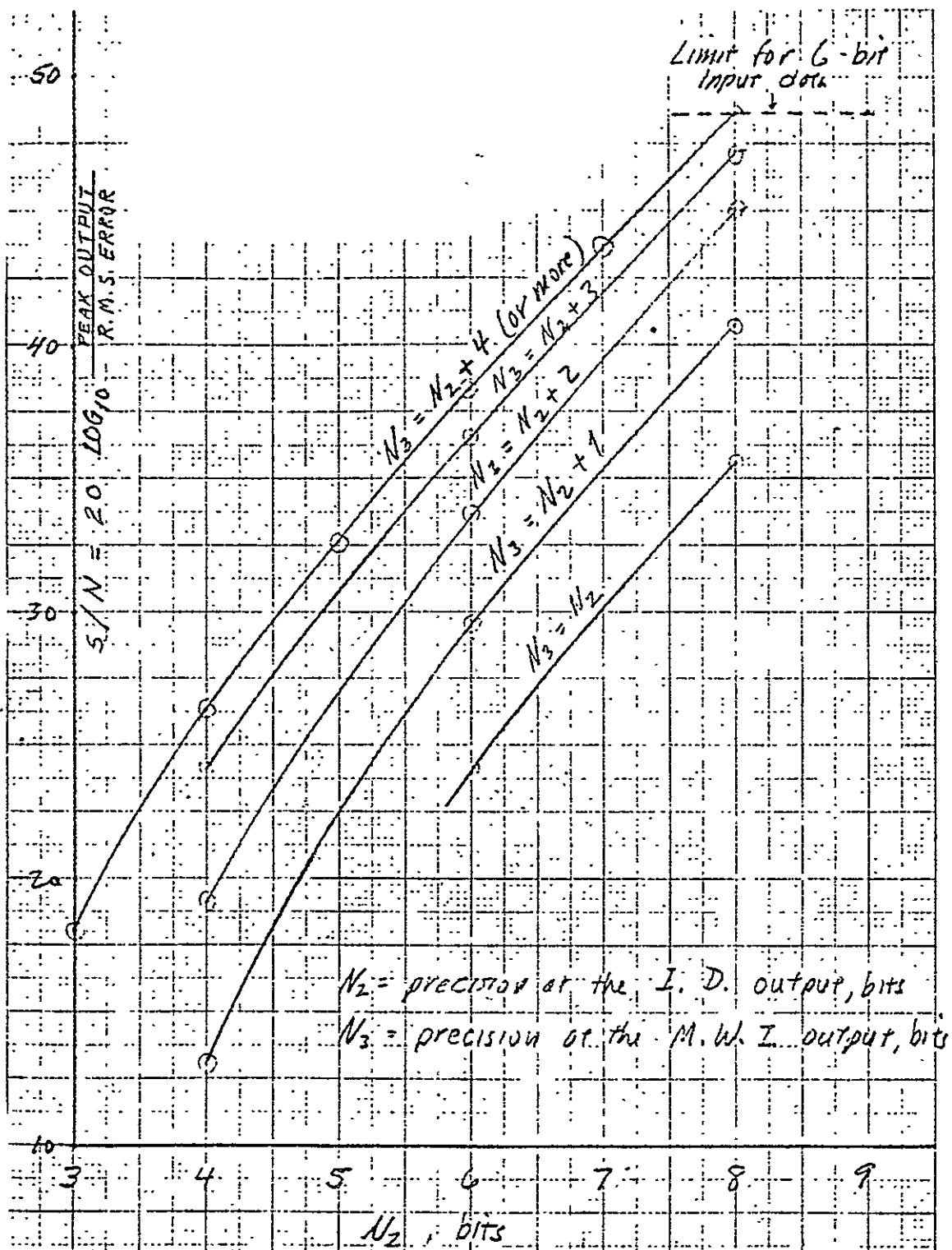


Figure A-7 Output S/N (dB) vs. N_2 (Bits) Input Data Quantized to 6 Bits
 Signal/Clutter = -10 dB Load Factor = 3.5

Figs A-6 and A-7 each present the results of some 20 simulation runs. The results of these runs do depend on the statistics of the input data. Solid conclusions could be drawn if the processor input data is similar to the input model of signal plus clutter used in this simulation. This input model is considered to be reasonably representative and to the extent that it is, a conclusion can be made that if the output of the integrate and dump integrator were truncated at 8 bits and the output of the moving window were truncated at 10 bits, the signal to processor quantizing noise would be 47.6 dB. Stated another way, the Baseline processor introduces only slightly more noise power (1.2 times) than the 6 bit A/D converter introduces into the system. Based on this reasoning, the Baseline processor truncates the integrate and dump at 8 bits and the moving window integrator at 10 bits.