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HIGH EFFICIENCY, HIGH DENSITY TERRESTRIAL PANEL

FINAL REPORT

FEBRUARY, 1979

BY

JOHN WOHLGEMUTH

MANFRED WIHL

THOMAS ROSENFIELD

JPL CONTRACT NO.: 954822

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SOLAREX CORPORATION
1335 PICCARD DRIVE
ROCKVILLE, MD 20850

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"The JPL low-cost Silicon Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE."

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SECTION I

INTRODUCTION

Most commercially available photovoltaic modules employ the standard round cells. Because of the geometry limitations the packing density in these panels is typically 60 to 70%. The low packing density results in total area panel efficiencies of 6 to 7%. With these low efficiencies, excess encapsulation, framing and mounting materials are required per watt of power delivered, thereby significantly increasing the cost per watt to the consumer. In addition, because of the low panel efficiency many potential applications, with limited area available for array deployment, are not feasible. Solarex has developed the technology for producing large area square and rectangular cells with high (14 to 15%) conversion efficiencies at AM1 ($1kW/m^2$) at 28°C. In this program terrestrial panels have been fabricated using these rectangular cells resulting in the achievement of packing densities in excess of 90% with panel conversion efficiencies greater than 13% being obtained. Most importantly, higher density panels can be produced today on a cost competitive basis with the standard salami panels, with bright prospects of significant cost reductions in the near future.

The high density panel technology is not only valuable for today's technology using single crystal silicon, but is exceeding important in light of recent developments in silicon substrate research. Many of the techniques now being developed for producing silicon such as the casting of poly-crystalline bricks and the production of silicon ribbons would result in square or rectangular pieces for incorporation into panels. Therefore, work on the development of the high density panel will promote advancements in such technologies as:

- development of interconnect schemes that are reliable, provide the required redundancy, allow for close spacing, are cost effective and can be easily automated.

- optimization of metallization patterns for use with the designed interconnect scheme to reduce series resistance losses and minimize shadowing for the rectangular or nearly rectangular geometry.

- development of encapsulation techniques for optimum reliability at minimum cost.

- study of thermal properties of the high density system to ascertain if the higher packing density results in any changes in operating temperature.

Our initial design considerations resulted in the choice of the rectangular cell because of the inherent simplicity in manufacturing and interconnecting. Other shapes which also produce higher packing densities such as hexagonal cells, require more alignment and fabrication time as well as much more elaborate interconnecting schemes. Indeed, the simplicity of the rectangular symmetry leads to lower production costs with today's technologies and lends itself more easily to future automation. Finally, the rectangular geometry is the one which prepares us for the future silicon developments.

In this program Solarex has employed 5cm x 5cm square cells as shown in Figure 1. Large quantities of these cells have been fabricated with average efficiencies in excess of 14% AM1 at 28°C. These cells have been used in the panels designed for this program. Figure 2 is a picture of one of the panels fabricated for this program. Twelve of these panels have been fabricated with each producing approximately 25 watts at a panel efficiency of nearly 13% (12W/ft^2 power density) at AM1 and 28°C.

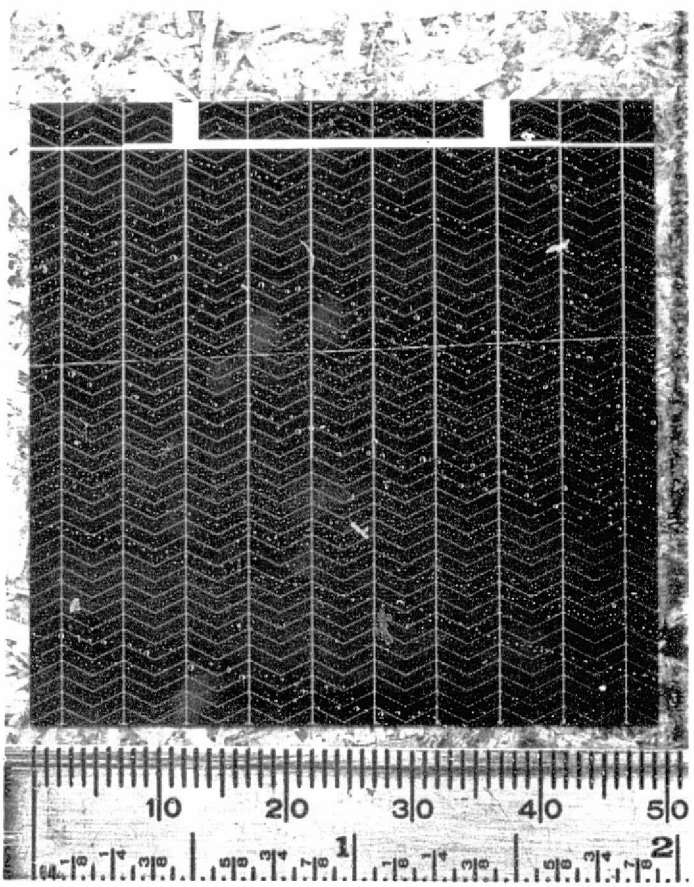

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Figure 1. 5 cm x 5 cm Solar Cell

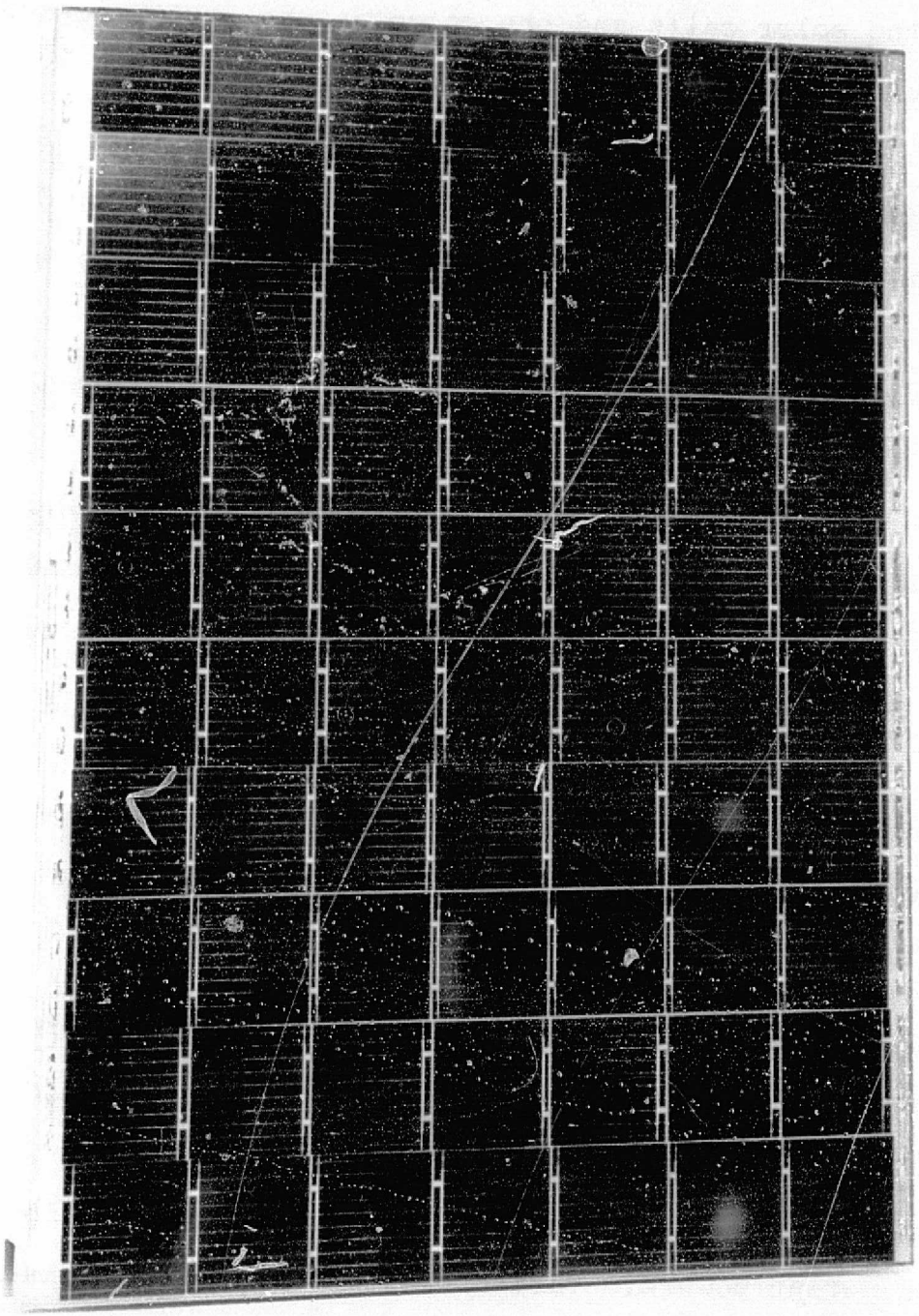

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Figure 2.

High Density Panel

The cell design and expected cell performance are described in Section II. This includes the basic properties of the solar cells and the calculations performed during the design stage and to predict the expected results.

A description of the module design, the rationale for and the specifications of the components to be used in the modules, is given in Section III. This section also includes an estimate of the expected module performance.

The test results are given in Section IV. This includes the results of pre-production humidity and thermal cycling testing, as well as the final test results from measurements both at Solarex and at JPL.

Section V includes an economic analysis of high density panel production, as well as design recommendations and conclusions drawn from this program.

This program met the contract goals of producing 12 high density modules with outputs in excess of 25 watts (AM1 at 28°C), as measured against Solarex internal standards. Measurements of the same modules at JPL resulted in lower reported output powers. Various reasons for this discrepancy have been identified as:

- NASA/Lewis manufactured standard cells resulted in a 6.3% error due to a light piping effect that erroneously raised the output of the standard cell.
- A change of 2.1% in the international radiometric standard in 1977.
- The difference between the pyranometer measurements used at Solarex at that time and the accepted pyrheliometer standard used by JPL.

Therefore, the time reading is probably half way between the Solarex and JPL measurement. The results in this report are based upon the Solarex measurement, so it should be scaled down by approximately 6% to agree with present day standards. Even scaling the power down by 6% most of the modules meet the goal of 25 watts per module.

SECTION II

CELL DESIGN

A. General Cell Properties

The 5cm x 5cm square cell developed by Solarex and used in this program was based upon standard Solarex solar cell technology. The cell was designed for use, using silicon wafers with the following specifications.

- p-type
- 100 oriented single crystal
- CZ grown
- boron doped
- 1.0 to 3.0 Ω-cm resistivity
- 3" diameter
- 10 mil thick wafers
- alkaline etched surface

The cells are processed using Solarex technology which produce cells with...

- phosphorous doped n^+ region
- sheet resistance 50 to 100 Ω/□
- aluminum p^+ back

- back contact Solarex Trimet™ contacts
- front contacts applied by photolithography
- front contacts Solarex Trimet™ contacts
- tantalum oxide anti-reflective coating.

Cells from this type process have been supplied to JPL for the National Procurement Program under Blocks II and III, and have been found to provide optimum humidity resistance and meet the cell requirements set forth in JPL Document 5-342-1 "Silicon Solar Cell Performance, Environmental Test and Inspection Requirements", Rev. B.

B. Front Pattern Design

The cell design for this program involves the derivation of a front grid pattern for optimum collection efficiency with sufficient redundancy to allow for high production yields. An initial criteria was the need for dual pads to allow for redundant interconnection for long term reliability. The number of interconnections was limited to two, because of the increased complexity and cost involved in the use of more numerous interconnects.

The spacing and thickness of the finest lines are determined by the limits of photolithography and a balance between power loss due to resistance and power loss due to shadowing. The Solarex chevron pattern chosen for this program is an initial line width of 0.35 mil, which will grow to approximately 1 mil after plating.

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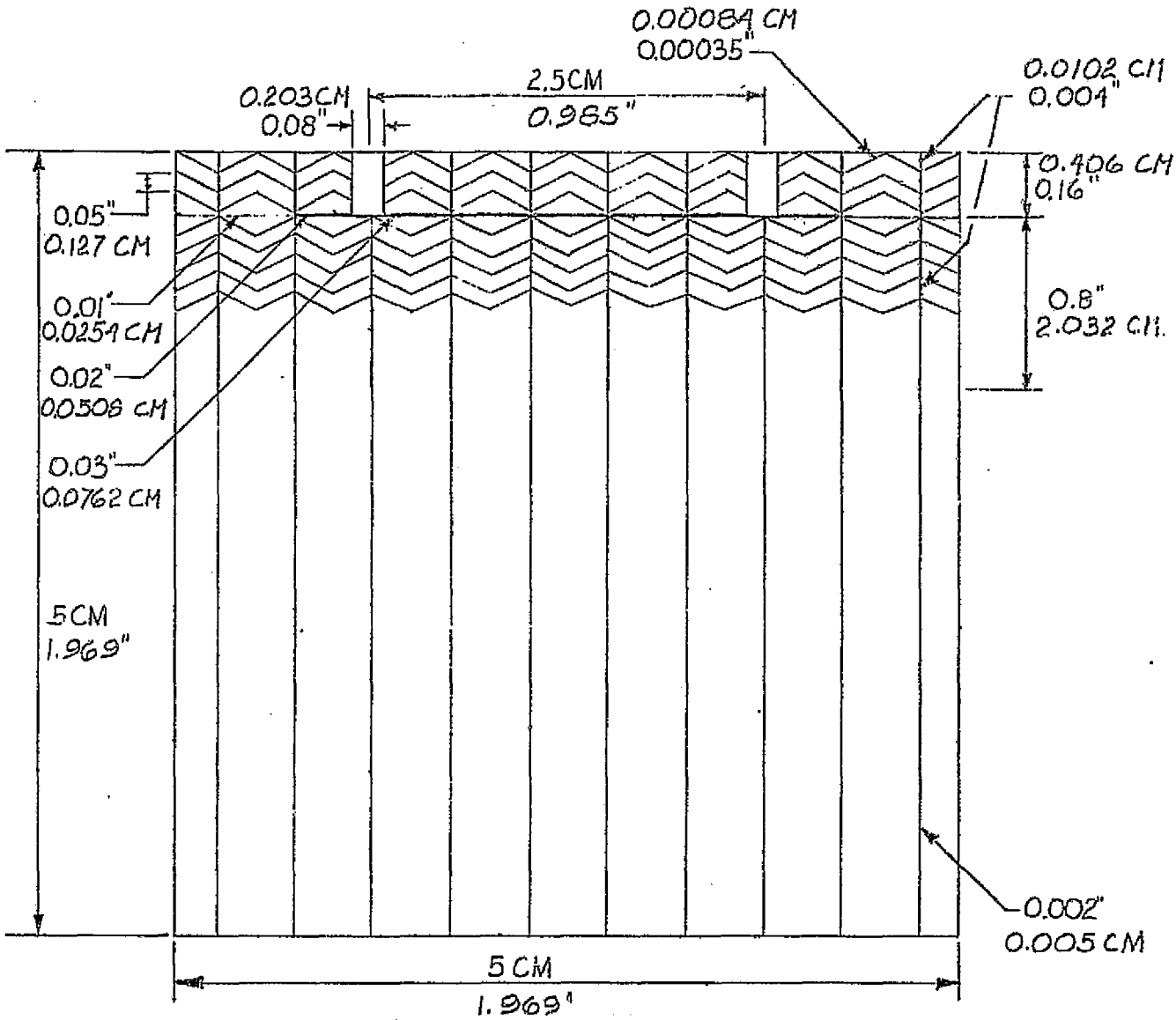

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reinforcement. These pattern with lines spaced 0.05 inches apart has proved to be optimun for 1 sun applications.

To assure sufficient processing yield and redundancy the main busses have been spaced 0.5cm apart leaving 10 busses for the 5cm x 5cm cell. To optimize the trade-off between series resistance loss in the busses and shadowing by the metal, finer line busses have been employed on the half of the cell farthest from the interconnect pads while thicker busses are used to carry more current near the interconnect pads. The choice of two different sizes is purely arbitrary and picked for simplicity and because of the diminishing gain from a more complicated arrangement. The widths of the busses are determined by minimizing the total power loss associated with the busses, balancing the series resistance loss with the shadowing loss. The buss widths of 2 mils and 4 mils respectively were derived by such a calculation. The size of the pads must be minimized with the restraint that it be physically possible to interconnect to them. The width of the inter-pad buss is determined by the degree of interconnect redundancy required. A value of less than 5% cell output power degradation was used, yielding an inter-pad buss width of 30 mils.

Figure 3 is a drawing of the front pattern design for this cell.

C. Expected Cell Performance

The expected cell performance can be calculated from the expected performance of such Solarex processed 2 Ω-cm silicon minus the losses due to shadowing and series resistance. This type of cell processing at Solarex on 2 Ω-cm silicon typically yields cells with:

$$R_{\text{sheet resistance}} = 50 \text{ to } 100\ \Omega/\square$$
$$J_{sc} = 35\ \text{mA/cm}^2 \qquad \text{at AM1 } 28°\text{C}$$
$$V_{oc} = 585\ \text{mV}$$

If series resistance and shunting are ignored fill factors of approximately 0.82 are expected. So, before accounting for losses due to series resistance or shadowing the cell output power would be approximately

$$P_A = .42 \text{ Watts}$$

The power loss components have been calculated in Appendix I and are given by

$$\Delta P_{\text{shadowing}} = (0.021 \text{ Watts})$$

$$\Delta P_{\text{sheet resitance}} = (0.021 \text{ Watts})$$

$$\Delta P_{\text{metal busses}} = 0.013 \text{ Watts}$$

$$\Delta P_{\text{substrate}} = 0.001 \text{ Watts}$$

The total power loss is then

$$\Delta P = 0.056$$

and the expected output power of the cell is given by:

$$P_T = P_A - \Delta P = 0.364 \text{ W}$$

This is a cell efficiency given by

$$\eta = 14.6\%$$

This is indeed approximately the average output power of the cells as will be seen in Section IV.

SECTION III

MODULE DESIGN AND FABRICATION

A. Structural Frame

The frame for the high efficiency, high density panels has been designed to be 20.1" long and 15.0" wide. These dimensions were chosen for maximum packing density of the 5cm x 5cm cells into the panel for current state of the art technology. A drawing of the frame is shown in Figure 4. U-channel and angle construction lend structural rigidity and iridited aluminum was chosen as the engineering material for lightweight, superior weatherability, resistance to harsh environments and relative long term cost effectiveness. Heliarc welds are used for connection to lend structural integrity and strength. The cell pan border is of the same material and is adhered to the frame with spot welds.

B. Cell Pan

Solarex has had long term experience using high deflection temperature polyester panels. Polyester can withstand the temperatures required for the curing of the encapsulants as well as providing 100 megohms isolation to ground and 1500 volts minimum breakdown voltage. The cell pans will be attached and sealed to the frame with a silicon R.T.V. adhesive.

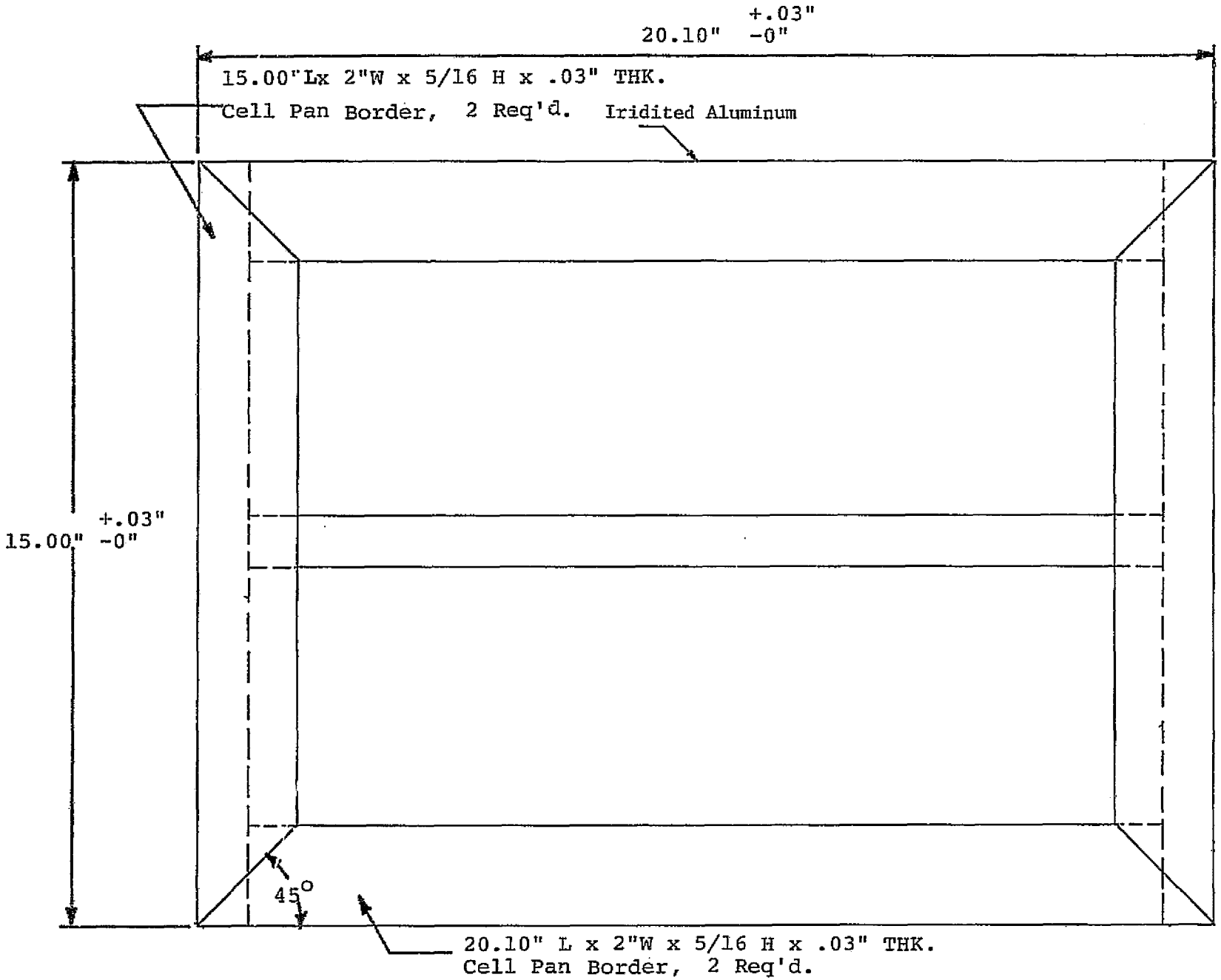

Figure 4. Drawing of Frame

C. Cell Interconnection

The interconnection scheme is shown in Figure 5 and consists of 70 cells arranged in two (2) series strings of 35 cells each. This design provides convenient voltages to charge 12 or 24 volt systems. The cells are designed to be double tabbed with silver mesh interconnects at an intercell spacing of 1 millimeter. Due to its high coefficient of linear expansion silver mesh is an effective stress relieving interconnect material in systems where conventional tab looping may be difficult due to high packing density. The interconnects will be soldered on the front and back of the cell. Turn-around is accomplished by solder connections from the cells onto buss bars at either top or bottom of the panel.

The ends of each string of 35 cells is fed through the polyester substrate into a weatherproof, water resistant junction box mounted behind the panel.

D. Encapsulation

Through extensive research Solarex has found a silicon rubber encapsulation system which performs well with respect to impact resistance, light transmittance, bonding strength, U.V. stability, weatherability and chemical resistance. Due

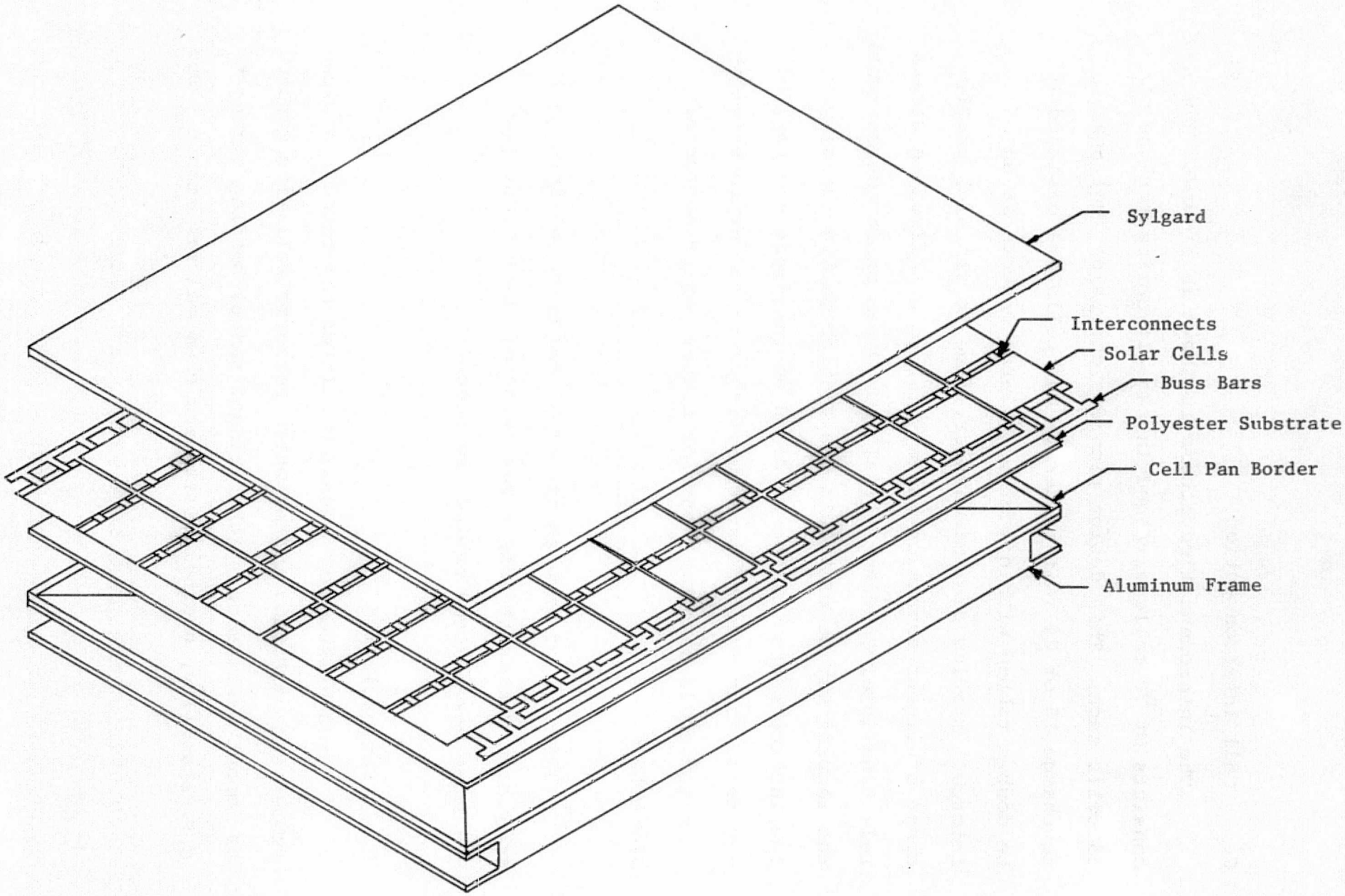

Figure 5. Conceptual View of Module Construction

to the reliability of Solarex panels, including deployment over many years this encapsulant was chosen for use in this project. Figure 5 shows a conceptual view of the module encapsulation.

E. Expected Module Performance

Each 35 cell string is designed to produce at AM1 28°C:

$V_{open\ circuit}$	$\tilde{=}$	20 volts
$I_{short\ circuit}$	$\tilde{=}$	.8 amps
$V_{peak\ power}$	$\tilde{=}$	16 volts
$I_{peak\ power}$	$\tilde{=}$	.78 amps
$Power_{peak}$	$\tilde{=}$	12.5 watts

In this manner, the panels are capable of charging either a 12 or 24 volt system and of meeting the minimum contract requirements.

F. Module Fabrication

The modules were fabricated by the procedures as described in the Engineering Documentation prepared for this contract. Because of the small number of modules required, all processes were performed manually in an R & D setting

SECTION IV

TEST RESULTS

A. Cell Performance

The distribution of efficiencies for the cells made for this program is given in Table 1.

TABLE I

AM1 Efficiency (28°C)	Number of Cells	%
greater 15%	819	41
14 - 15%	977	49
13 - 14%	184	9
12 - 13%	32	1

There are no useable cells with efficiencies less than 12%.

The average efficiency is approximately 14.7% which agrees very well with the estimated efficiency.

B. Pre-production Testing

Testing of the pre-production modules took place at Solarex and the Stanford Technology Corporation, to comply with the inspection requirements of J.P.L. Document No. 5-342-1, Revision B, "Silicon Solar Cell Module Performance, Environmental Test and Inspection Requirements."

These tests were divided as seen below:

At Solarex:

- Electrical Isolation: 100 megohms - passed
- Electrical Breakdown: 1500 Volts - passed
- I-V Characteristics at AM1 (28°C) both before and after thermal cycling and humidity testing. All pre-production modules had efficiencies greater than 25 Watts both before and after testing. Figures 6-8 are I-V curves of modules #100084, 100085, 100087.
- Visual Inspection of all Modules both Before and After Thermal Cycling and Humidity Testing: All pre-production modules passed both visual inspections.

At S.T.C.: (See Appendix II for details)

Thermal Cycling - 50 cycles: "There was no evidence of external physical damage or deterioration as a result of the thermal cycling test."

Humidity Test: "There was no evidence of external physical damage or deterioration as a result of the humidity test."

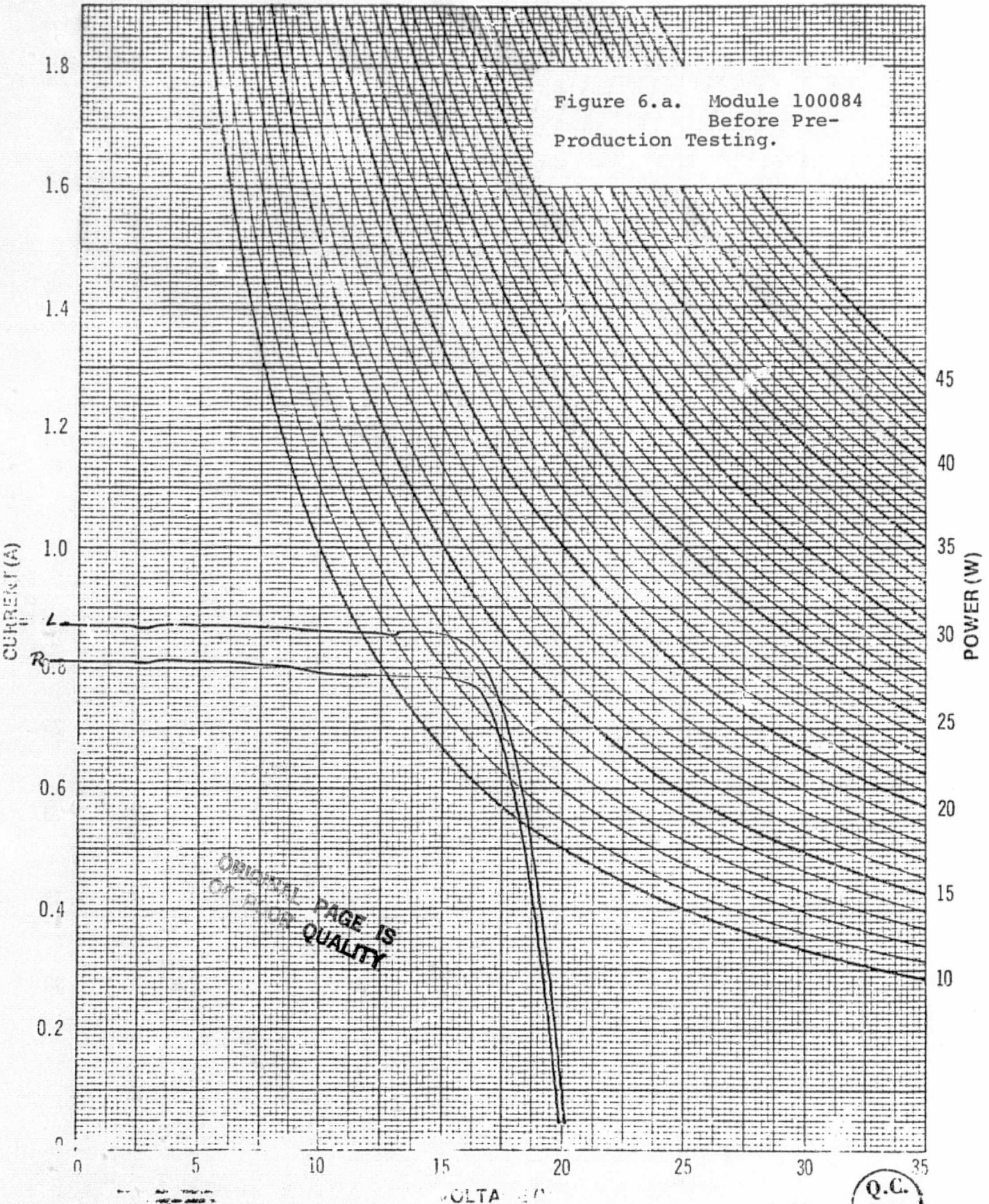

Figure 6.a. Module 100084 Before Pre-Production Testing.

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Panel Type HDR1 Serial No. 100084 Temp. 23c Date 12-14-77 By

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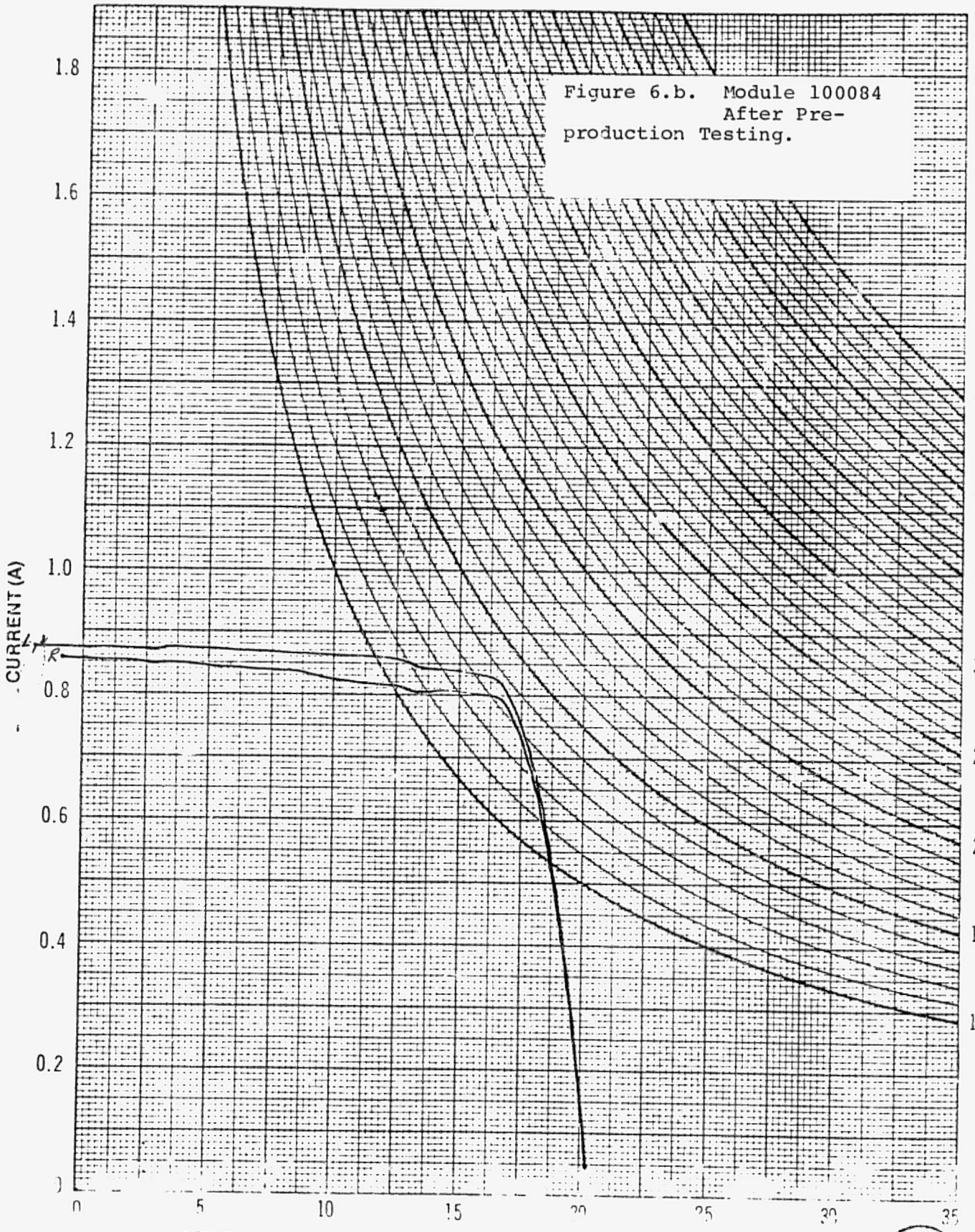

Figure 6.b. Module 100084 After Pre-production Testing.

Panel Type HD Serial No 100084 Temp. 25°C Date 2-14-78 By: [illegible]

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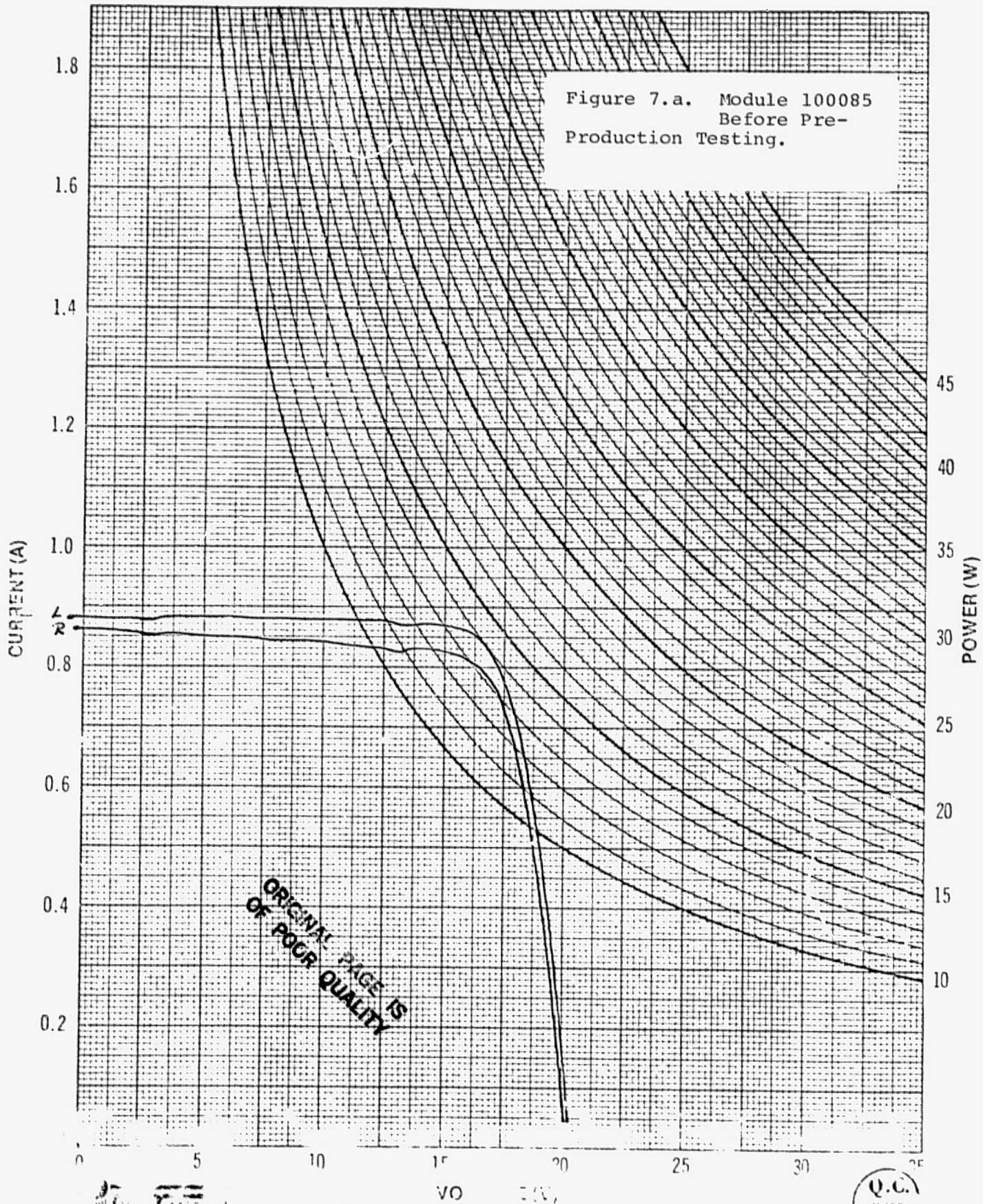

Figure 7.a. Module 100085 Before Pre-Production Testing.

Panel Type HDK1 Serial No. 100085 Temp. 23° Date 12-14-77 By

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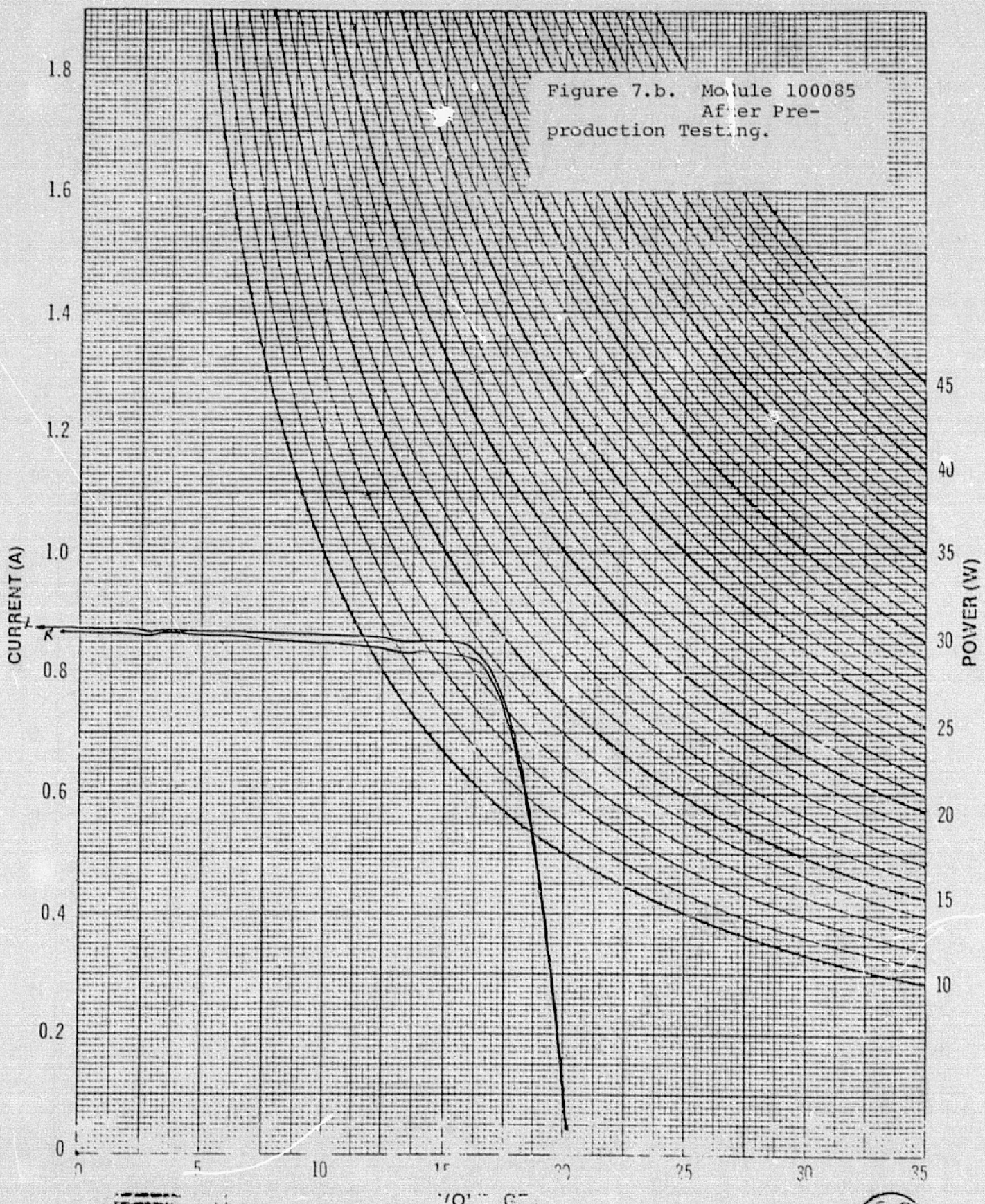

Figure 7.b. Module 100085 After Pre-production Testing.

Panel Type HO Serial No 100085 Temp. 25° Date 2-14-78 By [illegible]

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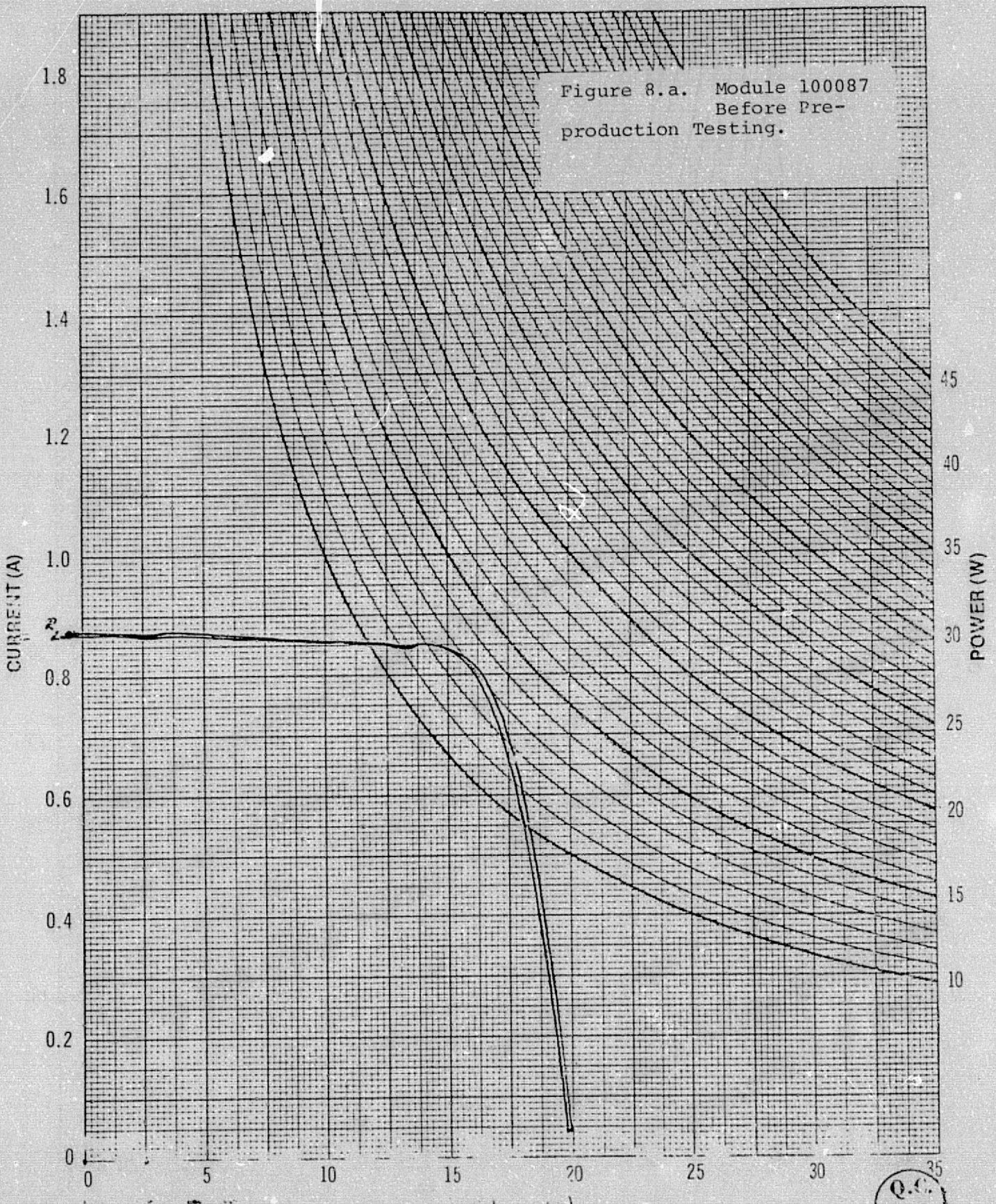

Figure 8.a. Module 100087 Before Pre-production Testing.

Panel Type HDK1 Serial No 100087 Temp. 23° Date 12-14-77 By

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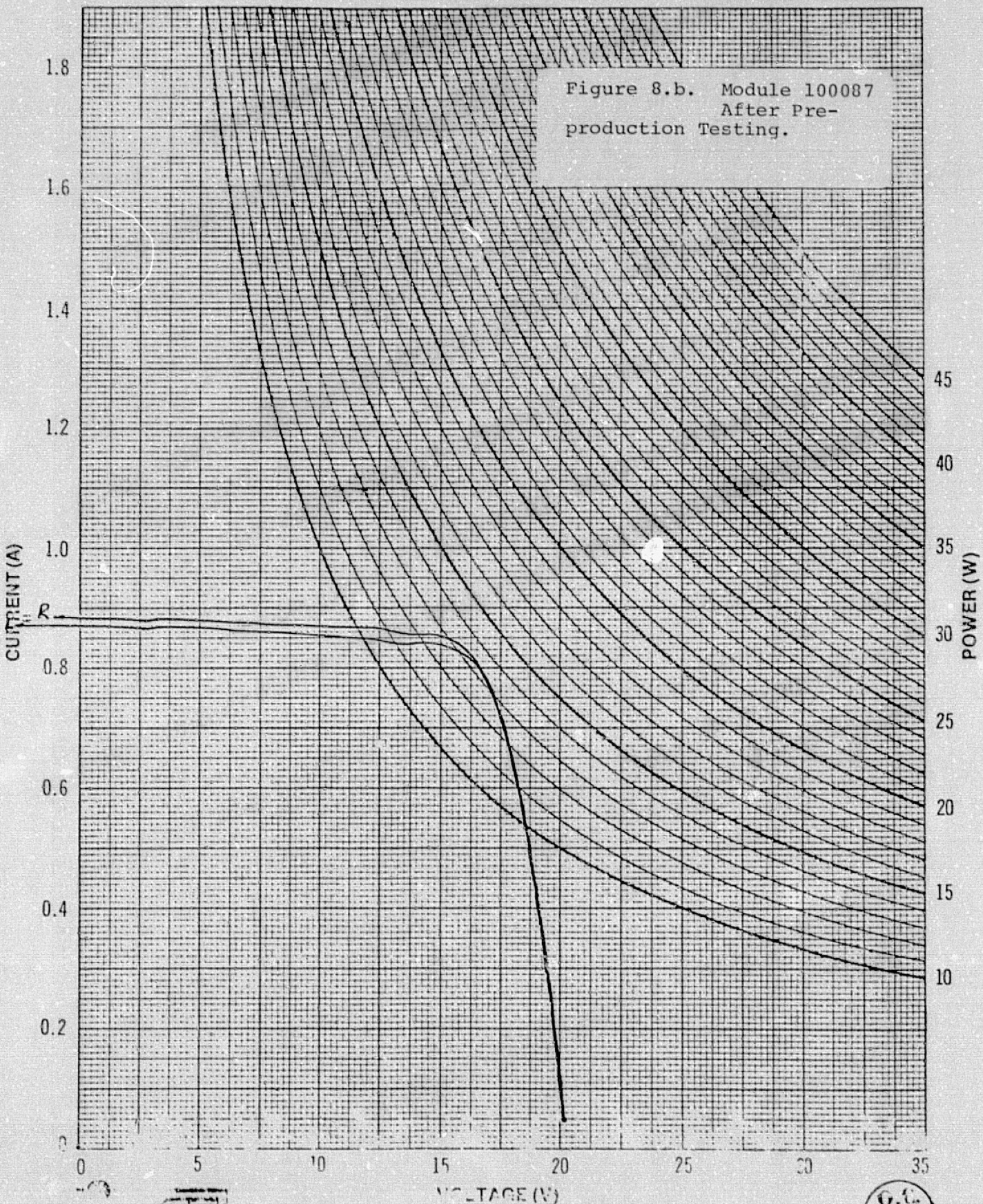

Figure 8.b. Module 100087 After Pre-production Testing.

Panel Type HD Serial No. 100087 Temp. 25° Date 2-14-78 By Q.C. INSP. 9

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C. Testing of Production Modules at Solarex

The twelve modules for delivery to JPL were measured at AM1 (28°C). Figures 6-17 show I-V curves for these modules. Table II summarizes the results on all modules before shipment to JPL. Each of them exceed the minimum requirements for this program of 25 Watts per module. The modules also passed visual quality control, electrical isolation of 100 megohms and 1500 volts stand-off voltage per JPL specifications.

D. Testing of Modules at JPL

The modules were retested at JPL.

Two major areas of difficulty were encountered.

- Junction Box Problems: Due to inadequate tightening of screws and the absence of lockwashers, one string in a panel opened up. This can be solved by taking more care in tightening the screws and by including a lockwasher in the design. This has not been a recurring problem.
- Fractured Interconnects: The silver mesh affords excellent stress relief, except when embrittled by soldering. Several modules developed opens due to interconnect failures after thermal cycling. This appears to be due to lack of solder flow control during the attachement of the tabs. Since silver mesh has

TABLE II - MODULE MEASUREMENTS

MODULE #	V_{oc} R (mV)	V_{oc} L (mV)	Max Power (R) W	Max Power (L) W	Max Power (Total) W
100067	20.4	19.8	14	13.5	27.5
100084	20.3	20.3	13.3	13.7	27.0
100085	20.2	20.2	13.5	13.7	27.2
100086	20.4	19.9	13.0	12.8	25.8
100087	20.2	20.2	13.4	13.3	26.7
100095	20.3	20.3	14.2	13.8	27.0
100097	20.0	20.3	13.1	13.2	26.3
100098	20.1	19.9	14.1	14.0	28.1
100099	20.3	19.9	13.5	13.1	26.6
100100	20.3	20.3	14.6	14.5	29.1
100102	20.5	20.2	14.1	13.5	27.6
100106	20.1	20.3	13.9	14.2	28.1

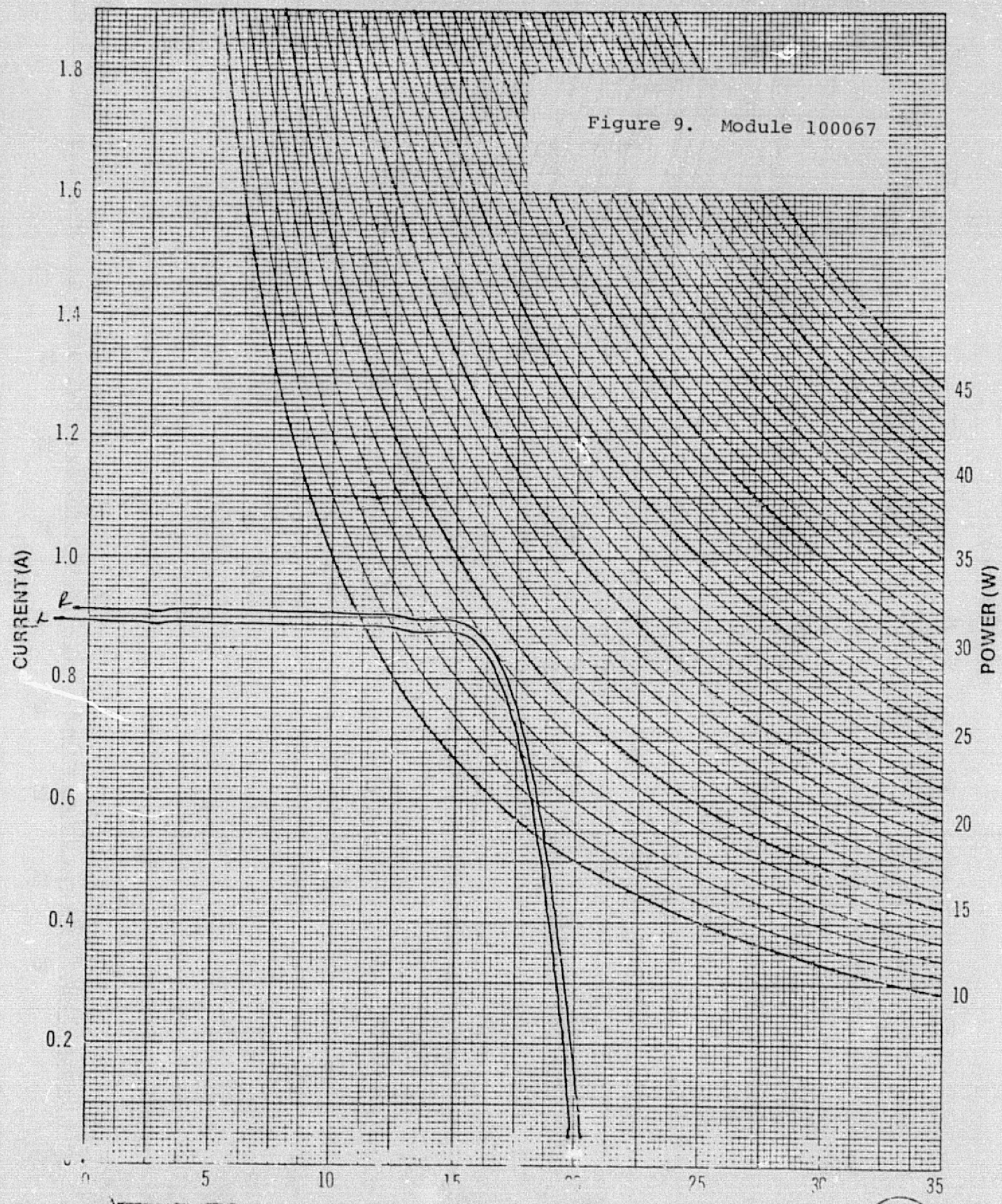

Figure 9. Module 100067

SOLAREX ROCKVILLE, MARYLAND USA

Panel Type HD Serial No. 100067 Temp. 25° Date 2-14-78 By

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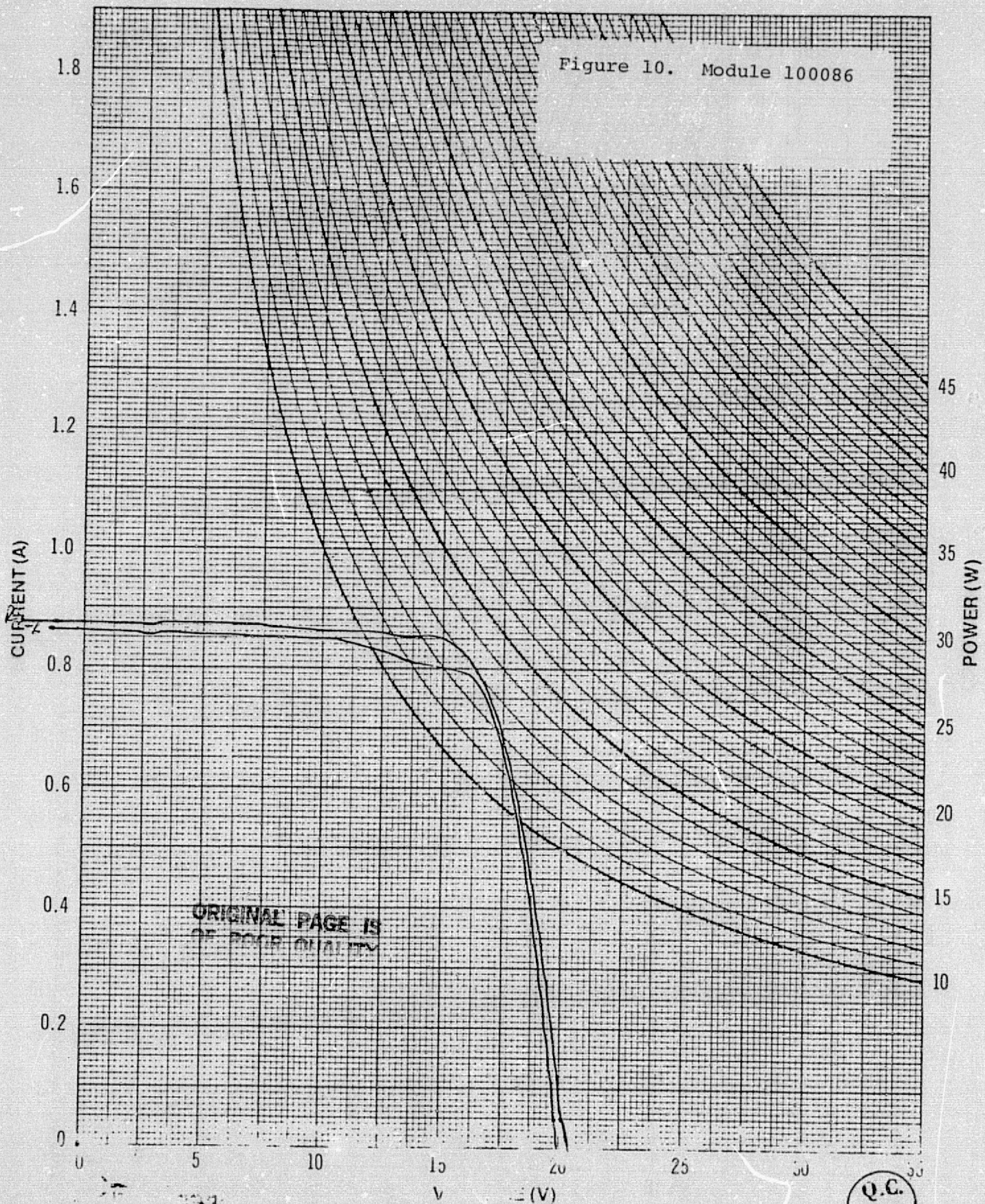

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Panel Type HD Serial No. 100086 Temp. 25°C Date 2-14-78 By

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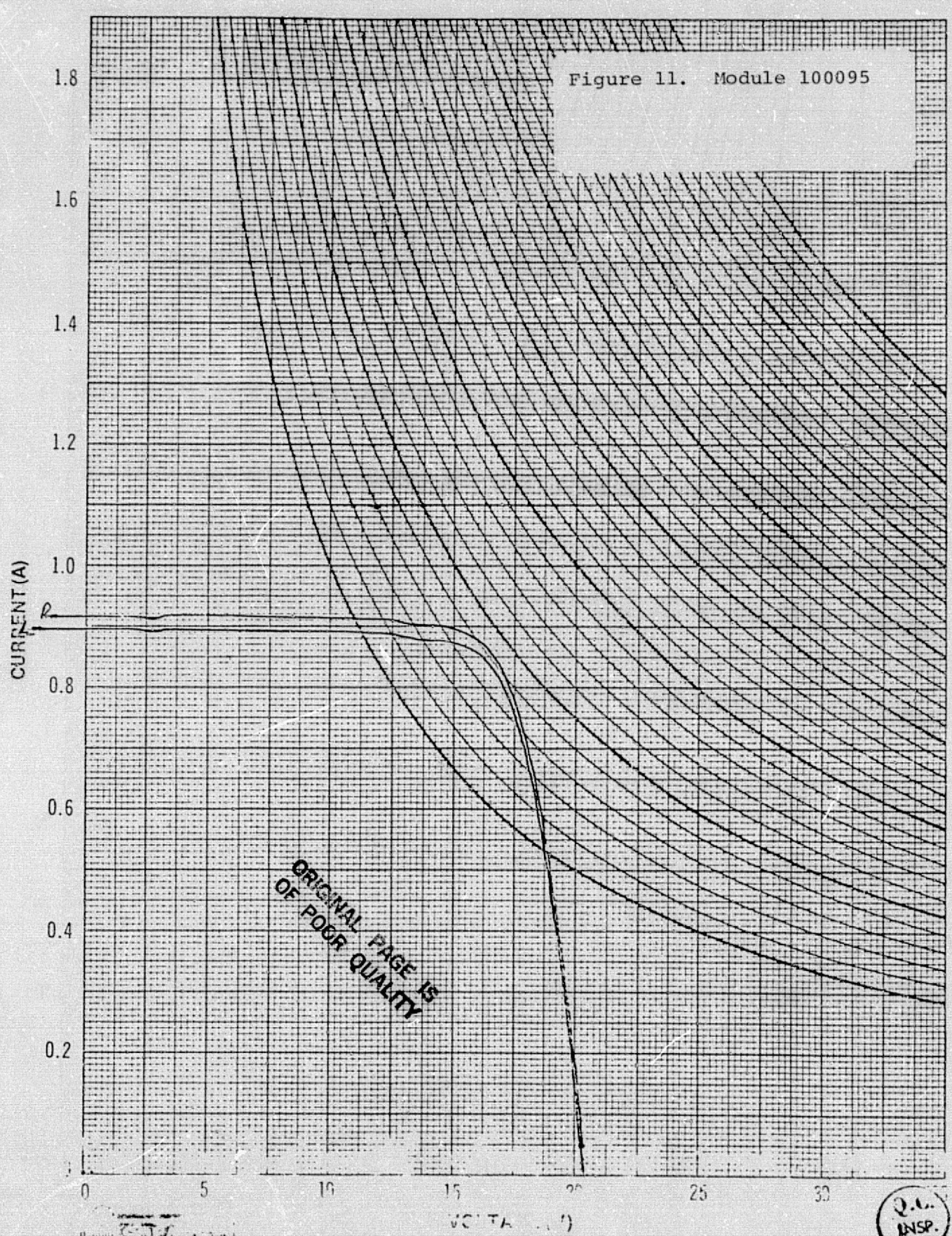
Figure 11. Module 100095
CURRENT (A)
POWER (W)
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
45
40
35
30
25
20
15
10
0
5
10
15
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25
30
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Panel Type HD Serial No. 100095 Temp. 25C Date 2-14-78 By
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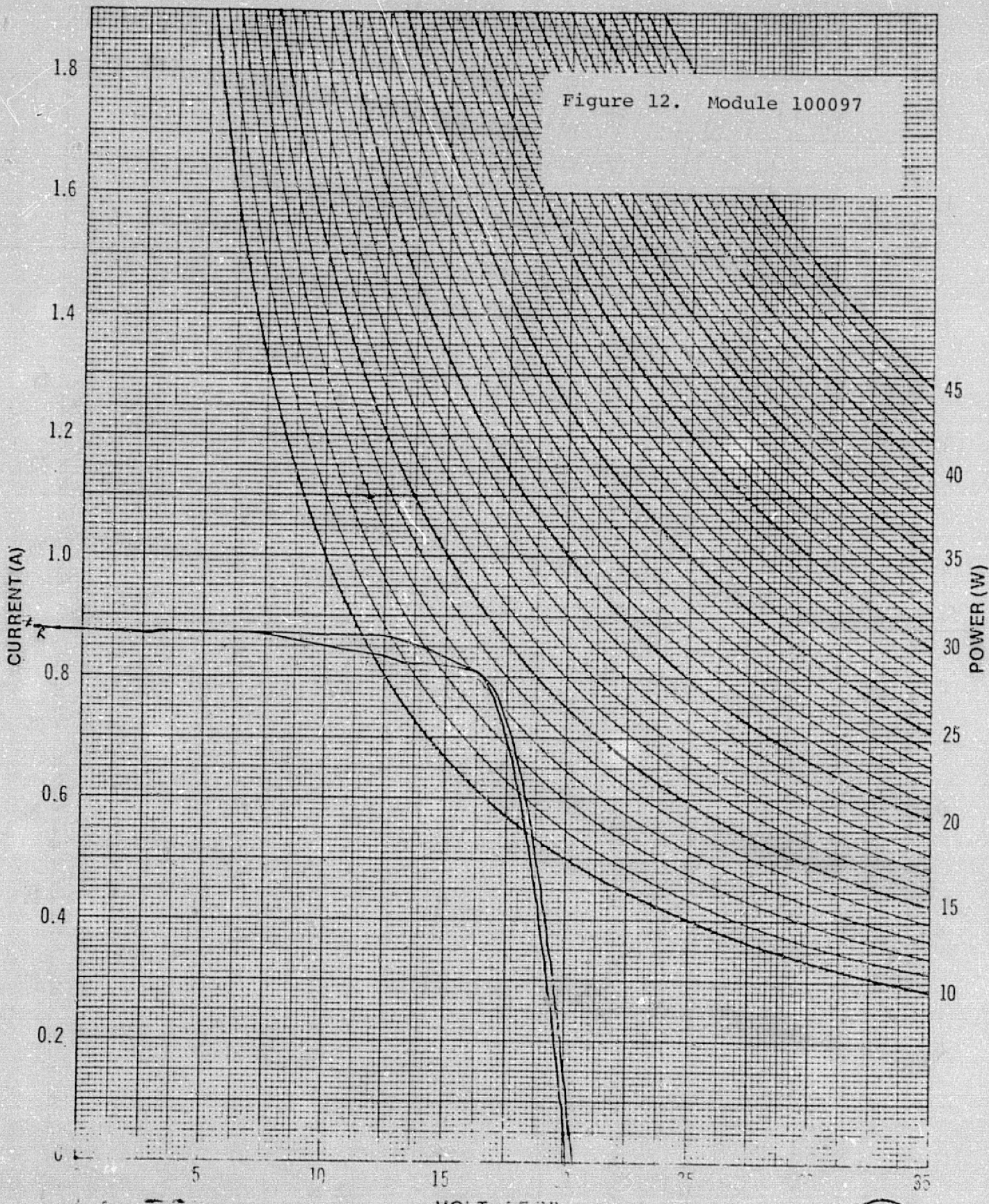

Figure 12. Module 100097

Panel Type HD Serial No 00097 Temp. 25° Date 2-14-78 By

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Figure 13. Module 100098

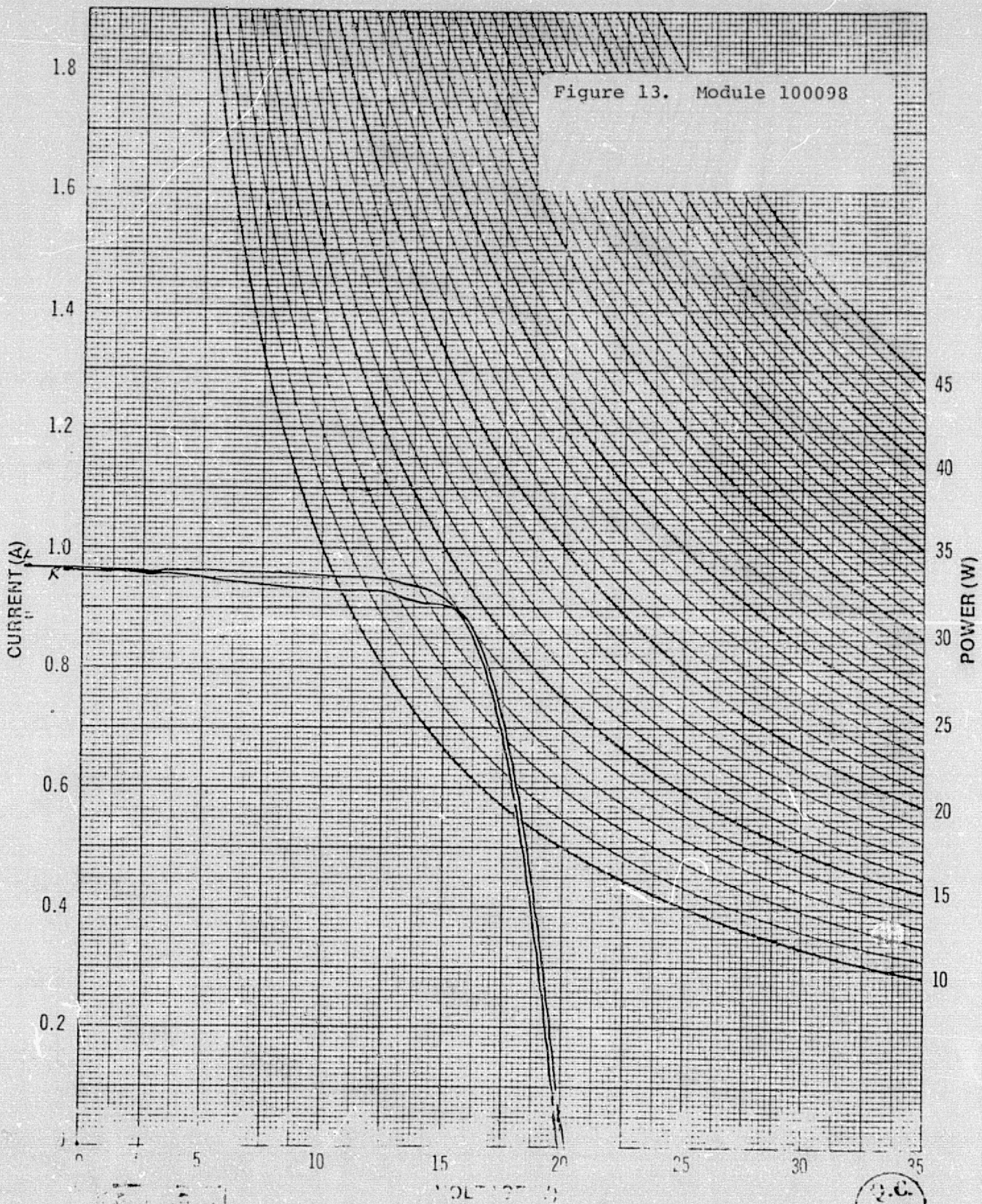

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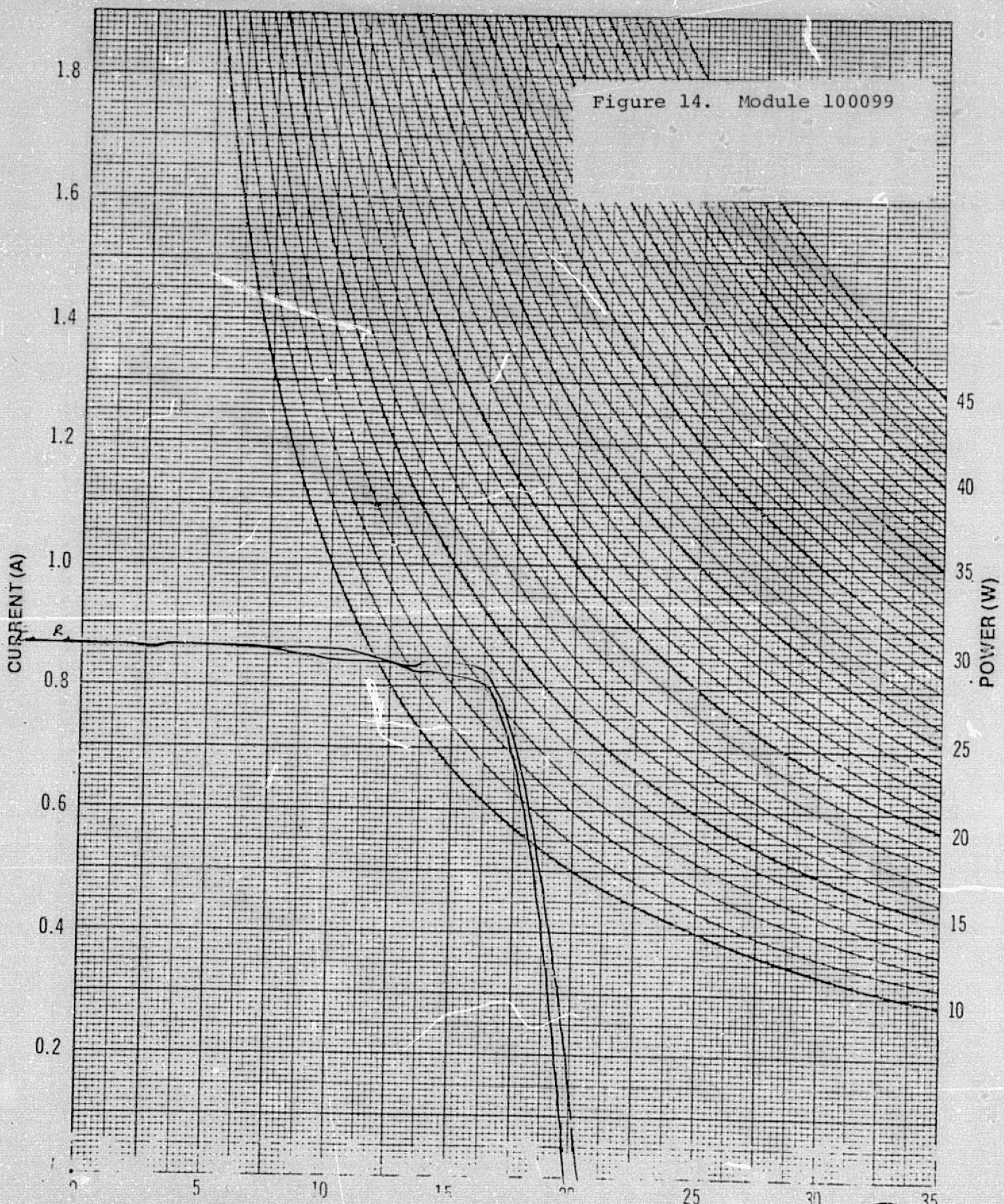
Figure 14. Module 100099



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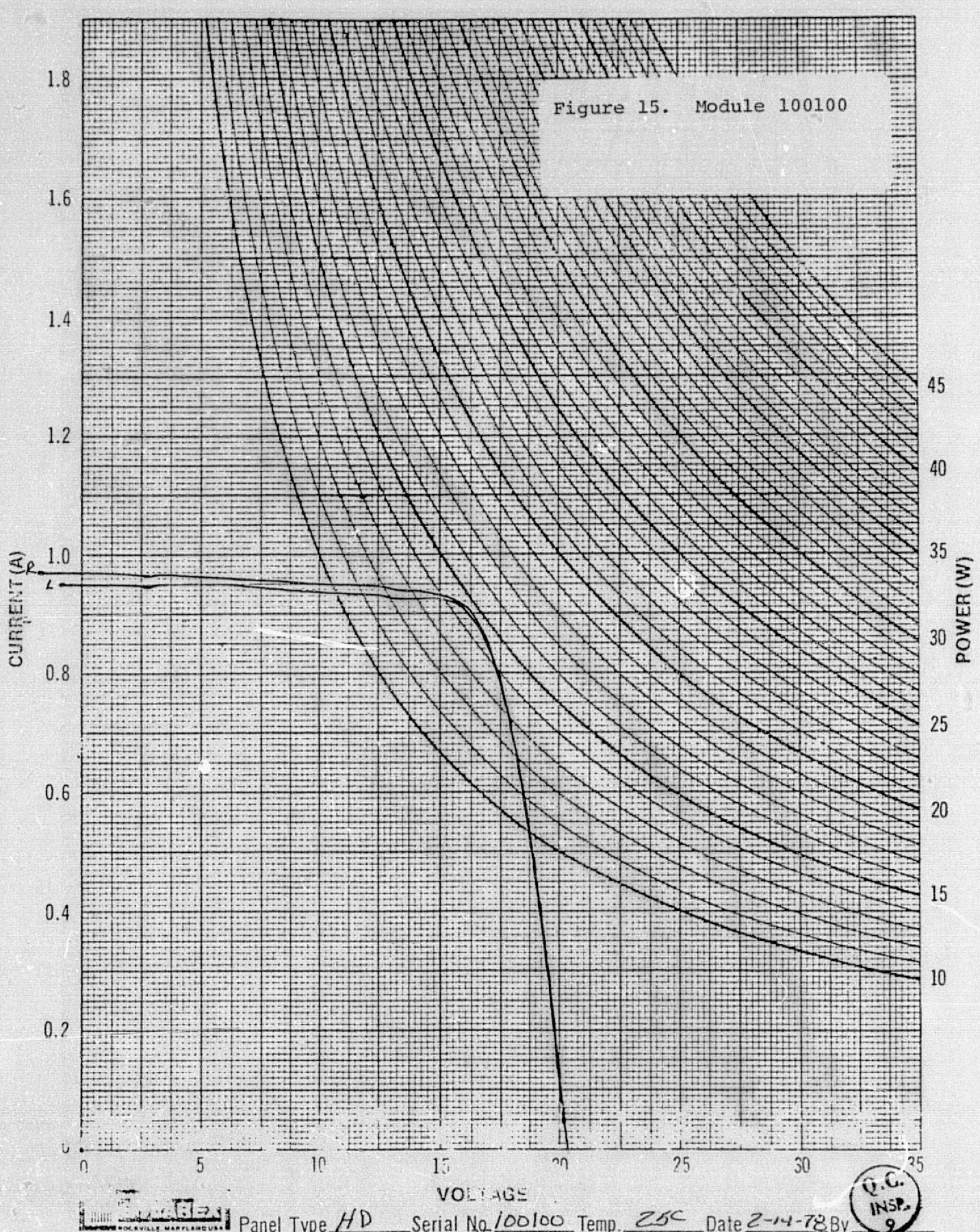

Figure 15. Module 100100

Panel Type HD Serial No. 100100 Temp. 25C Date 2-14-78 By

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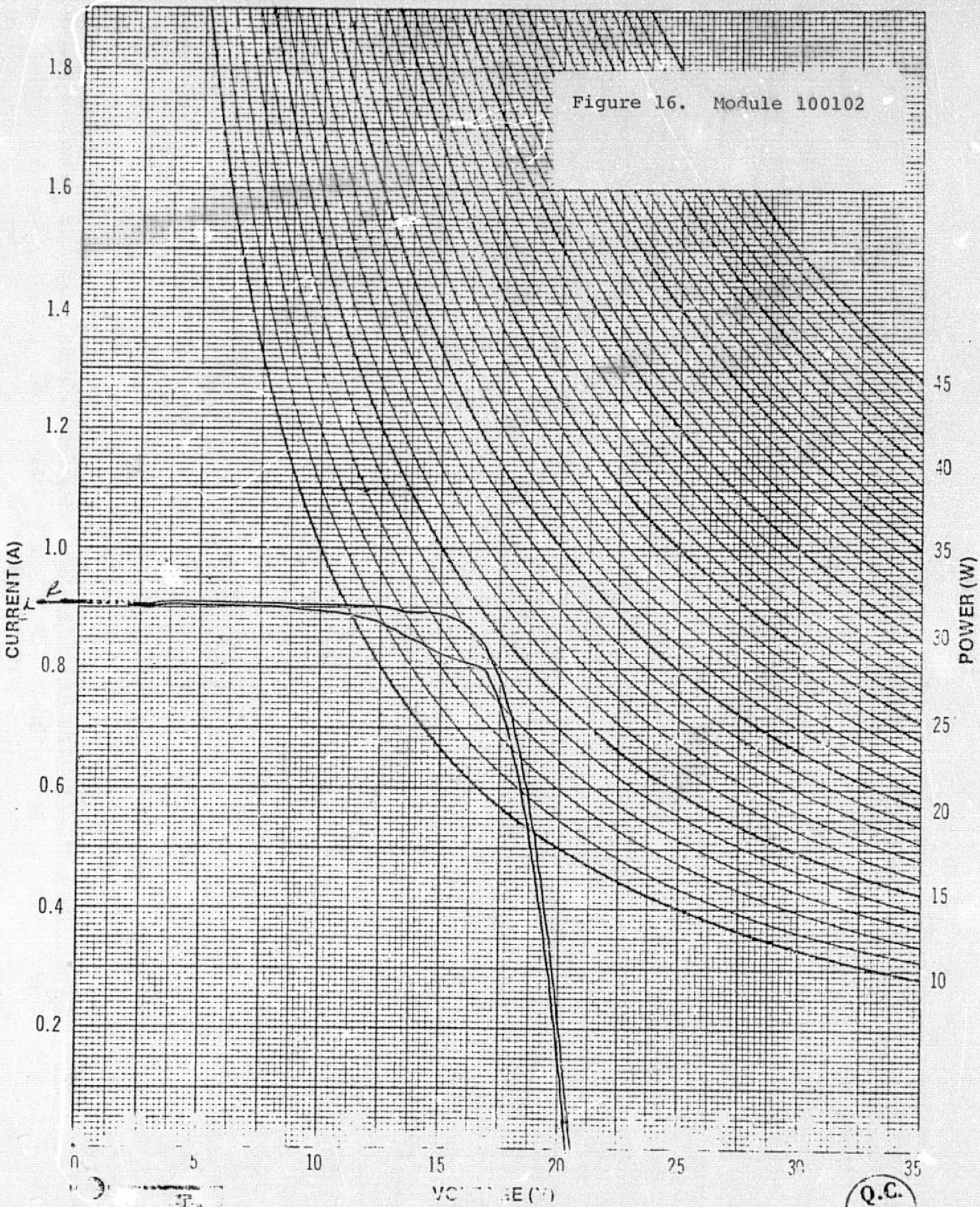
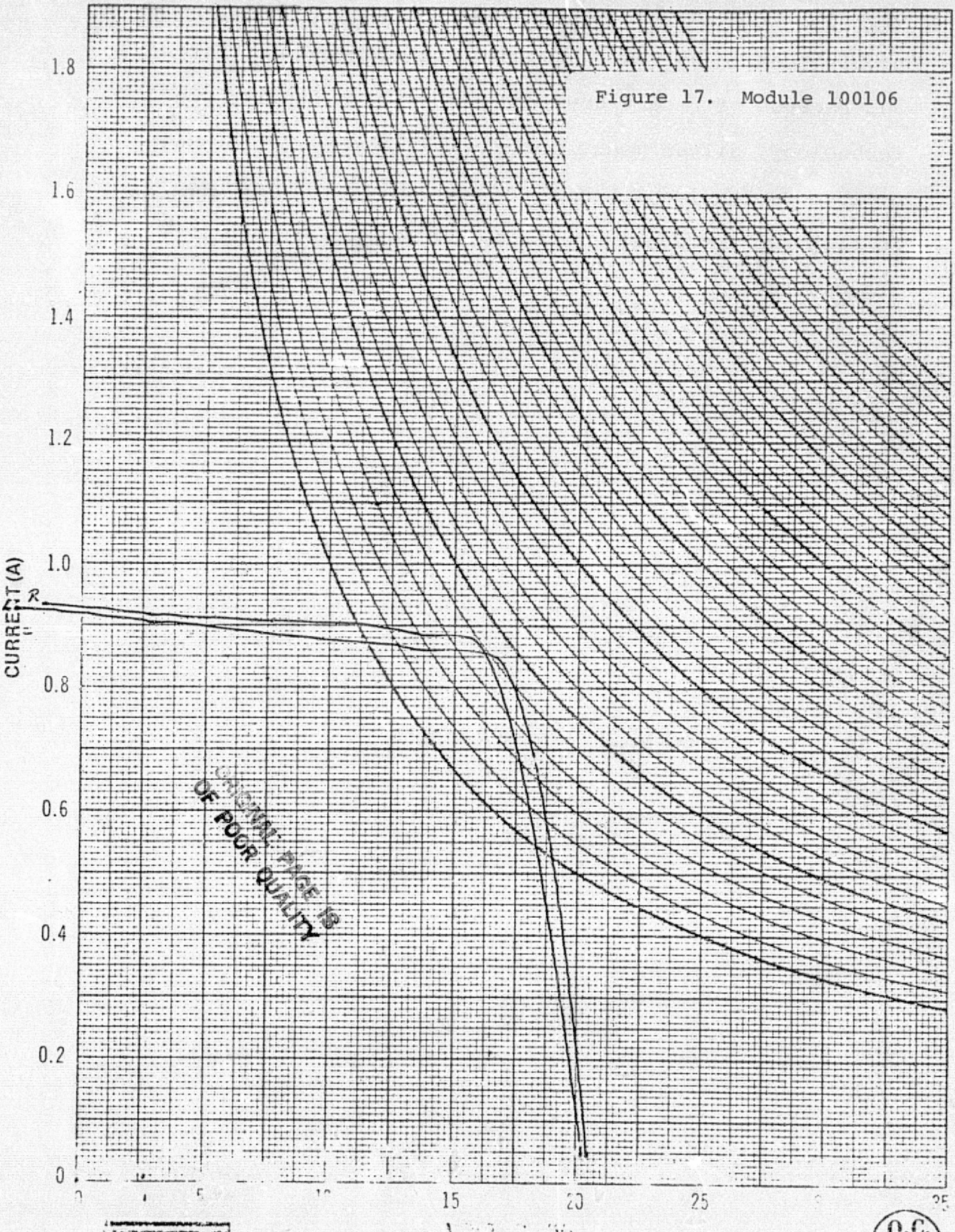


Figure 16. Module 100102

Panel Type HD Serial No. 100102 Temp. 25c Date 2-14-78 By

Q.C. INSP. 9

Figure 17. Module 100106



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SOLAREX ROCKVILLE, MARYLAND U.S.A.

Panel Type HD Serial No 100106 Temp. 23° Date 2-21-78 By

Q.C. INSP. 9

FORM 11133

been employed in the space field for years, this problem can be solved. However, due to economic factors and because of recent developments in high density panel technology, silver mesh interconnects are no longer being employed. Tab looping has now been perfected for use in high packing density systems with superior results at reduced cost.

SECTION V

ECONOMIC ANALYSIS AND CONCLUSIONS

A. Economic Analysis

In order to access the economics of high density panels, calculations have been carried out to determine the effects of the various parameters (not including the limitation of array deployment space) on the total system costs. Figure 18 is a graph of the percentage of utilized cell area used out of a round wafer plotted as a function of packing density in percent for a close packed rectangular array with 1mm spacing between cells and between cells and border. A compromise must be made between complete usage of the silicon and increased packing density. The particular design chosen will depend upon the relative costs of cells and encapsulation-framing material.

Figure 19, 20, and 21 are families of curves of cell area utilization versus cost per watt for the panels for various cost per watt of cells alone. Figure 19 is for a high encapsulation and framing cost, Figure 20 is for an intermediate cost, while Figure 21 is for a low cost of encapsulation and framing. Note that in these curves the framing cost includes the erection of the on-site supports so that it entails all costs to deploy the modules in the field. As the cell cost drops, it becomes more advantageous

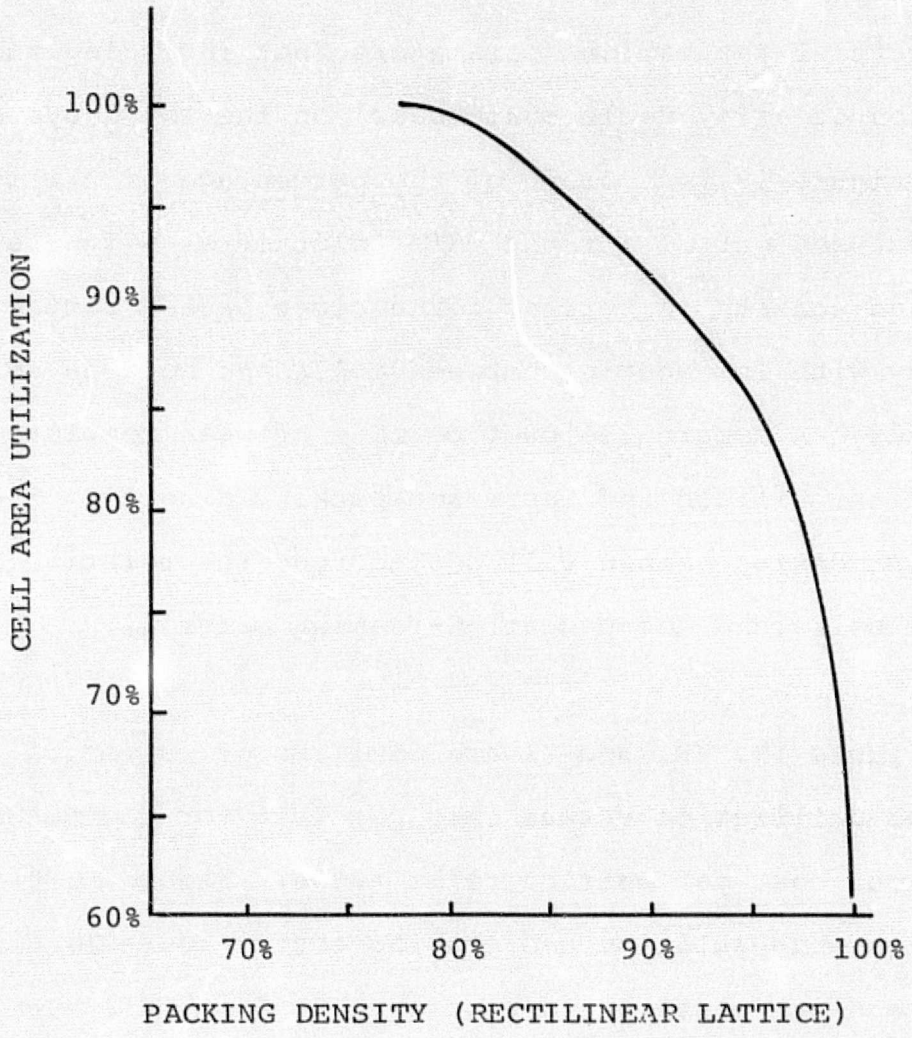

Figure 18. Cell Area Utilization from a Round Wafer Plotted as a Function of Maximum Possible Packing Density for a Rectilinear Lattice with 1mm Spacing.

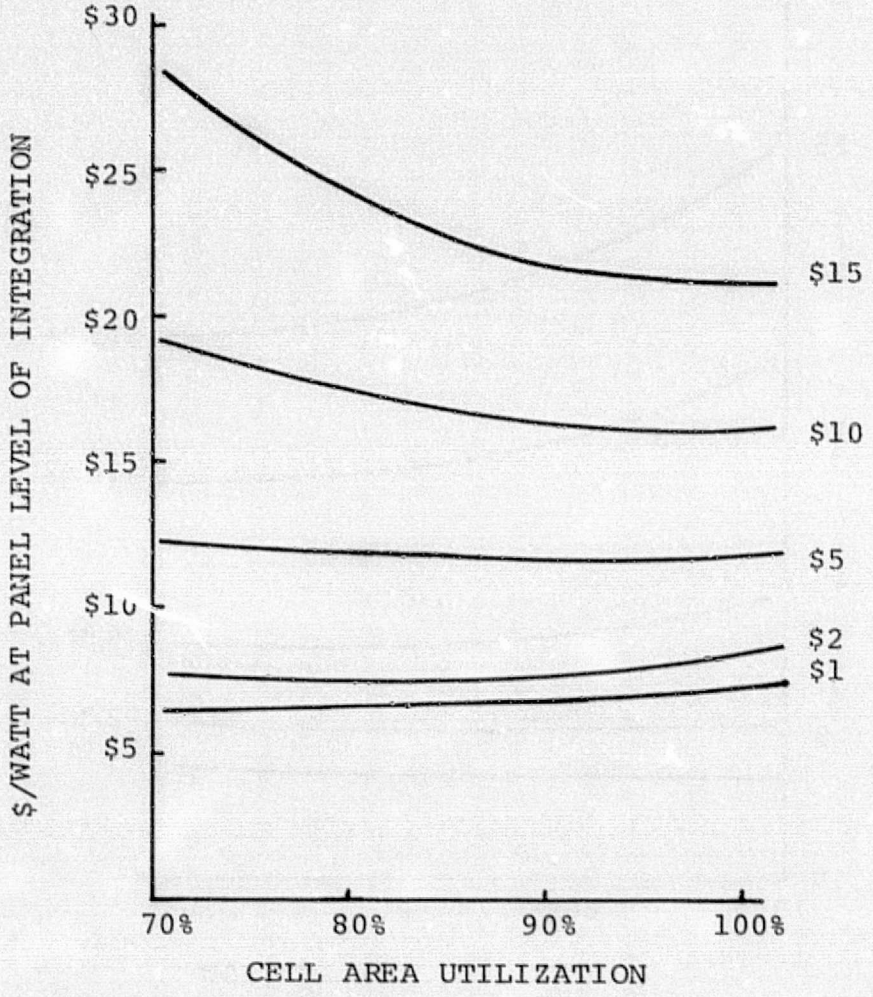

Figure 19. Cost Per Watt of Panels Plotted as a Function of Cell Area Utilization for Various Cell Costs for a Paneling Cost of 6¢/sq. cm.

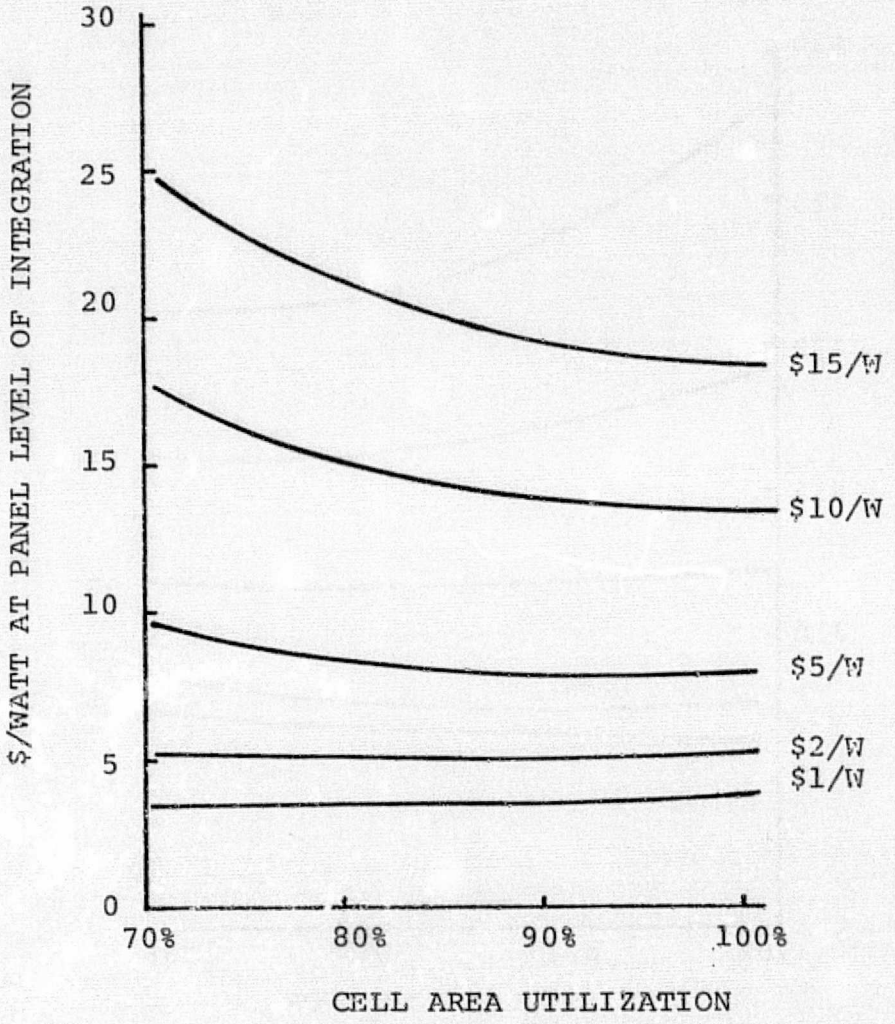

Figure 20. Cost per Watt of Panels Plotted as a Function of Cell Area Utilization for Various Cell Costs for a Paneling Cost of 3¢/sq. cm.

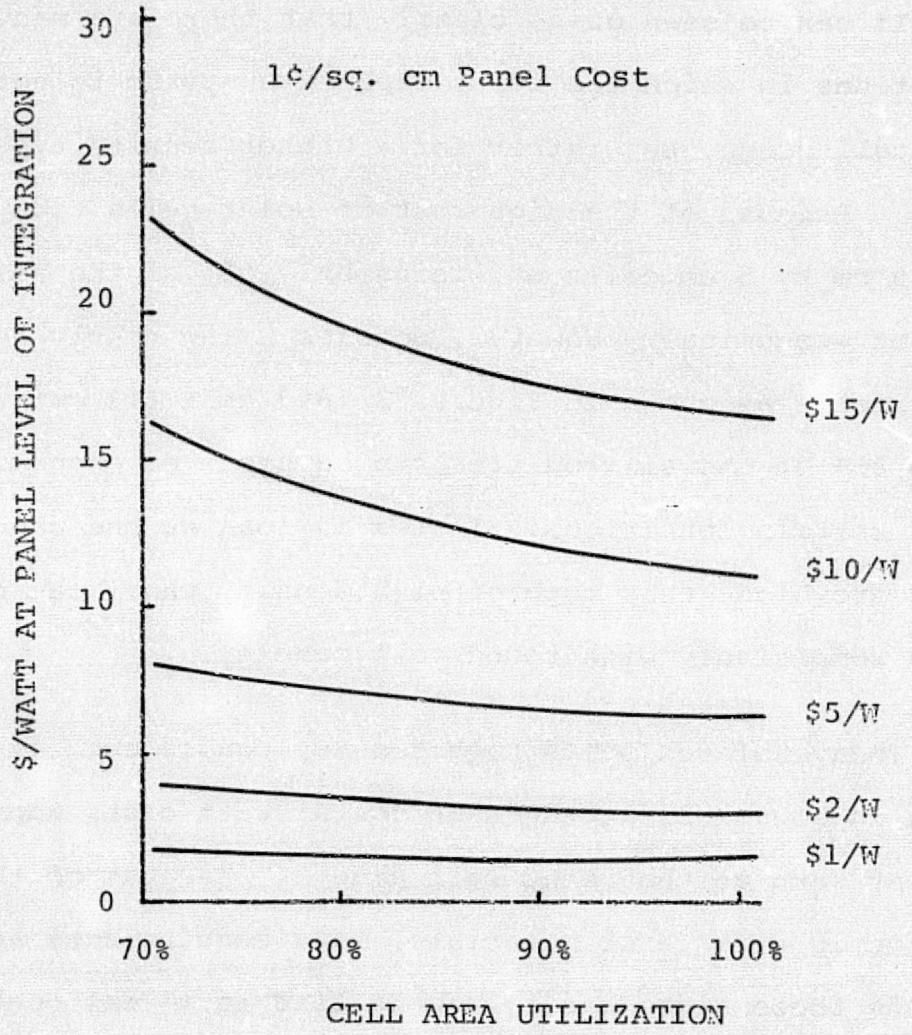

Figure 21. Cost per Watt of Panels Plotted as a Function of Cell Area Utilization for Various Cell Costs for a Paneling Cost of 1¢/sq. cm.

to use higher packing density and lower percent cell utilization to recduce total system cost. Such cost factors as land usage, cleaning, and maintenance will further increase the costs of salami panel systems in relation to high density panel systems.

It can be seen quite clearly that there are many situations in which the least expensive system is not for 100% cell usage, but rather for a higher density type panel. Because of the high cost of solar cells today, with 5 cm by 5 cm cells utilizing only 55% of the cell area are not economical. However, modules using nearly rectangular cells as shown in Figure 22 (6.3 cm x 6.3 cm) utilizing 80 to 85% of the silicon area can be produced economically under certain conditions. Indeed as long as the paneling costs are high, this type of high density panel can be produced competively with round cell panels.

Today Solarex sells high density panels such as the one shown in Figure 23 at the same dollar watt cost, approximately $10 per watt as the round cell panels. Because of the large savings in structural materials, land requirements and maintenance these high density panels lead to a real cost savings for the consumer.

Finally, input cost data was prepared in accordance with JPL Solar Array Manufacturing Industry Costing Standards (SAMICS) displayed in Format A's.

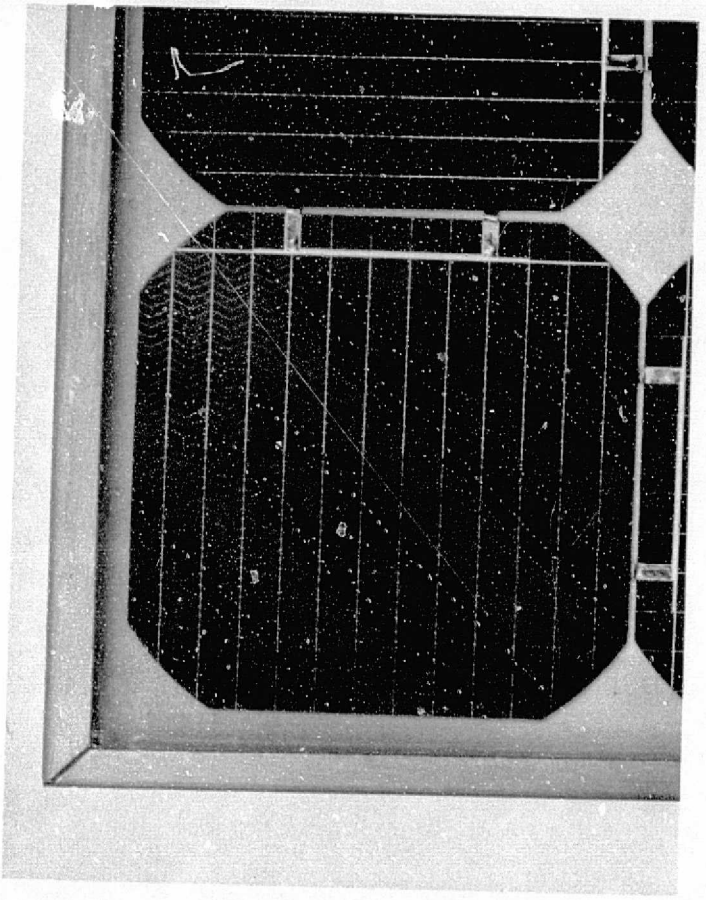

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Figure 22. 6.3 cm x 6.3 cm Solar Cell

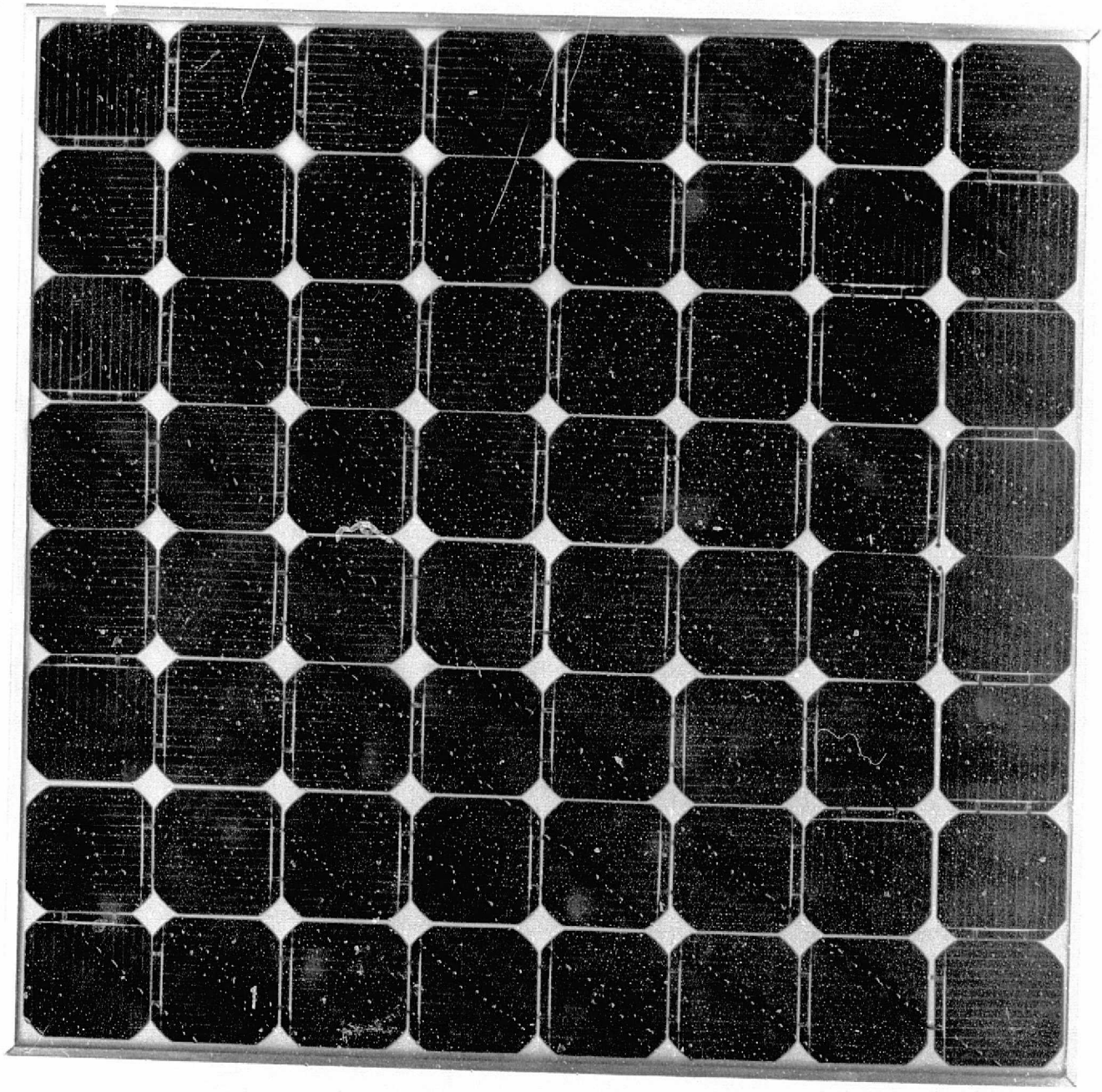


Figure 23.

Commercial High Density Panel

B. Suggestions for Future Developments

High density panel technology has progressed beyond the developmental stage. Future work should be geared toward

- cost reductions resulting from automation
- the use of less expensive materials
- further studies of the reliability of high density modules
- additional studies of the differences in operating conditions between high density and round cell modules.

C. Conclusions

High density panels are available commercially and have proved to be cost effective in today's market at the module level. It is believed that even now the overall systems cost is less for the high density systems. Finally, the high density technology has set the stage for future developments in silicon fabrication.

APPENDIX I

CALCULATION OF CELL PERFORMANCE

A. Power Loss Due to Coverage

Pads = 2 (.203cm) x (.406) = $.165cm^2$

Inter-Pad Buss = (.076cm) (2.5cm - .203cm) = $.175cm^2$

Main Cross Busses = 2(.051cm) (0.5cm - .102 cm) +
2(.0254cm) (.75cm) = $.1cm^2$

Wider Part of Main Busses = 10(.010cm) (2.032cm)
= $.206cm^2$

Smaller part of Main Busses = 10(.0051cm) (2.562cm)
+ 4(.005cm) (.381cm)
+ 4(.0051cm) (.330cm)
= $.145cm^2$

Sub-busses (slope 2 to 1) = $40\left(\frac{4.472}{4}\right)$ (.5cm) (10) .002
= $.447\ cm^2$

Total Area Coverage = $1.238cm^2$

% Area Coverage = 5.0%

Power Loss = (.41 Watts) (.050) = .021 Watts

B. Power Loss Due to Silicon Sheet Resistance

In each inter-grid region the power loss is given by

$$P_d = \frac{(jrw^2)}{12} jA$$

where: j = current density
r = sheet resistance
w = spacing between busses
A = area of collection region

For finger pattern:

$$W = (0.894)d$$

where d = step and repeat of fingers = (.127cm)

so W = 0.114cm
and A = (1.12) W (2)

where z = distance between collection busses = 0.5cm

Therefore, in each region there is a power loss due to sheet resistance at 1 sun 25°C of approximately*

$$P_d = 2.7 \times 10^{-6} \text{ Watts.}$$

There are approximately 780 such regions yielding a power loss in the diffused region of

$$\Delta P_{\text{sheet resistance}} = .0021 \text{ Watts}$$

*This calculation assumes:

1. No current flows directly to the larger busses, so it is an over estimate of sheet resistance due power loss
2. Current density is approximately 32.5 mA/cm^2 at maximum power.

C. Power Loss In Metal Busses

1. Grid Lines Fingers (sub-busses)

In each linear buss the power loss is given by

$$\Delta P_f = \frac{jw(x)^2 \rho}{3\ a\ t} \quad jw(x)$$

where x = length of current path in the buss = $(1.12)(1/2)$

ρ = resistivity of current carrying metal
$= 1.59 \times 10^{-6}$ Ω-cm

a = width of buss = .002cm

t = thickness of buss = .002cm

Each of the grid fingers then has a power loss

$$\Delta P_f = 6.6 \times 10^{-8} \text{ Watts}$$

Once again there are approximately 780 such grid fingers so

$$\Delta P_f = 5.1 \times 10^{-5} \text{ Watts}$$

2. Lower Part of Busses

Assume that the only current entering this region is from the sub-busses. Then, the current increases in a step function. Each sub-buss contributes a current

$$i = jA = j\ (1.12)w(z/2)$$

At each intersection there are 2 busses entering so at each such point

$$i = j\ (1.12)\ wz$$

The current at a position y is then given by:

$$i(y) = (1.12)\ jwzn$$

where $n = 0$ for $y \quad d$

$n = 1$ for $d \quad y \quad 2d$

$n = 2$ for $2d \quad y \quad 3d$

up to $n = \text{Int} \left| \frac{2.1}{d} \right| : nd \leq y \leq 2.1\text{cm}$

In each region

$$\Delta Pn\ (y) = i^2(y)\ R$$

$$\Delta Pn\ (y) = \left[(1.12)\,jwz\right]^2 \frac{\rho d}{at}\ n^2$$

and the total power loss in one lower buss is given by

$$\Delta P = \left[(1.12)\ jwz\right]^2 \frac{\rho d}{at} \sum_{n=0}^{\text{Int}\left|\frac{2.1}{d}\right|} n^2$$

For this pattern:

$n = 16$

$\rho = 1.59 \times 10^{-6}\ \Omega\text{-cm}$

$d = 0.127$ cm

$a = 0.0055$ cm

$t = 0.0012$ cm

so, $\Delta P = 2.0 \times 10^{-4}$ Watts

There are 10 such busses leading to a power loss of

$$\Delta P_2 = 0.002 \text{ Watts}$$

3. Top Region of Buss

The top region above the cross buss is identical to the region just discussed. This region has

$$n = 3$$

yield

$$\Delta P_3 = 1.9 \times 10^{-5} \text{ Watts}$$

4. Thicker Buss Region

The only difference in the calculation between this region and the thinner buss region is the addition of a current flowing into the bottom of this buss from the thinner buss.

So, at a position Y, the current is given by

$$i(y) = (1.12)jwzn + j(2.1)(0.5)cm^2$$

where $n = 0$ for $Y < d$

$n = 1$ for $d \leq Y \leq 2d$

$n = 2$ for $2d \leq Y \leq 3d$

$$n = \text{Int.} \left| \frac{2.5}{d} \right| \qquad nd \leq y \leq 2.5\text{cm}$$

Then in each region

$$\Delta P_n(y) = \left[(1.12)jwzn + j(1.05) \right]^2 \frac{\rho d}{at}$$

and the total power loss is one such buss is given by:

$$\Delta P = \frac{j^2 \rho d}{at} \sum_{n=0}^{\text{Int}\left|\frac{2.5}{d}\right|} \left[(1.12)\ wzn + 1.05\right]^2$$

$n = 20$

so, $\sum = 62$

$\Delta P = .001$ Watts

There are once again 10 of these busses so

$\Delta P_4 = 0.01$ Watts

4. Cross Buss

The current in each cross buss is approximately constant. See Figure 24.

region 1 and 9

$i_1 = j$ (5 cm) (0.5 cm)
l_1 = path length = 0.5 cm
w_1 = width = 0.026 cm

region 2 and 8

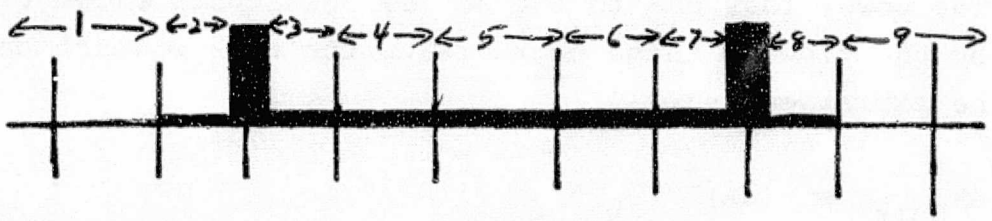
$i_2 = j$ (1.0 cm) (5 cm) for
l_2 = path length = 0.398 cm
w_2 = width = 0.051 cm

region 5

$i_5 \approx 0$ No major busses contributing current

Attached only for redundancy

Figure 24.



region 4 and 6

i_4 = j (5 cm) (0.5 cm)
l_4 = path length = 0.5 cm
w_4 = width = 0.077 cm

region 3 and 7

i_3 = j (5 cm) (1.0 cm)
l_3 = path length = 0.398 cm
w_3 = width = 0.077 cm

so,

$$\Delta P_5 = \frac{\rho}{t}\left[2\frac{l_1}{w_1} i_1^2 + 2\frac{l_2}{w_2} i_2^2 + 2\frac{l_4}{w_4} i_4^2 + 2\frac{l_3}{w_3} i_3^2\right]$$

ΔP_5 = 0.001 Watts

So: $\Delta P_{\text{metal busses}}$ = .013 Watts

D. Power Loss Due to Series Resistance in Substrate

The power loss due to the series resistance encounterd by the flow of these carriers to the back contact can be expressed as:

$$\Delta P_{bulk} = (JA)^2 \frac{\rho_b \ t_c}{A}$$

where: ρ_b = base resistivity = 2Ω-cm

t_c = base thickness = 0.025 cm

Therefore,

ΔP_{bulk} = 0.001 Watts

APPENDIX II

S ANFORD TECHNOLOGY CORP.

THERMAL CYCLING AND HUMIDITY TESTS

STANFORD TECHNOLOGY CORP.
25 PARKER AVENUE • GLENBROOK, CONN. 06906
(212) 478-2010 (203) 348-4080

REPORT OF TEST
ON
SOLAR MODULES
ENVIRONMENTAL TESTS

for

SOLAREX CORPORATION
1335 PICCARD DRIVE
ROCKVILLE, MD. 20850

January 31, 1978 ST-1341

SIGNATURES

FOR STANFORD TECHNOLOGY CORPORATION:

Joseph C. Smith
Test Engineer

2-3-78
Date

Gerald T. Ciccone
Vice President

2-3-78
Date

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Notices

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ADMINISTRATIVE DATA

TEST CONDUCTED:	Thermal Cycling and Humidity
MANUFACTURER:	Solarex Corp. 1335 Piccard Drive Rockville, Md. 20850
MANUFACTURER'S TYPE OR MODEL NO.:	HD Solar Panels
DRAWING, SPECIFICATION OR EXHIBIT:	Solarex Letter Dated 12/27/77
QUANTITY OF ITEMS TESTED:	Various
SECURITY CLASSIFICATION OF ITEMS:	Unclassified
DATE TEST COMPLETED:	January 31, 1978
DISPOSITION OF SPECIMENS:	Returned to Solarex
DATE OF TEST REPORT:	January 31, 1978
MANUFACTURER'S PURCHASE ORDER NO.:	6231
GOVT. CONT. NO.	N/A
ABSTRACT:	Refer to Test Results Section of this report

FACTUAL DATA

1.0 TEST EQUIPMENT

1.1 Temperature Humidity Chamber
Tenney Engineering
Model: T15 UF-100240
Last calibration: 28 July 1977
Next calibration: 1 Feburary 1978

1.2 Temperature Humidity Chamber
International Radiant Corp.
Model: LHH-30
Last calibration: 11 December 1977
Next calibration: 11 June 1978

All instrumentation and equipment calibration conducted in accordance with and as defined in MIL-S-45662A "Calibration Systems Requirements" and are traceable to the National Bureau os Standards.

2.0 TEST SEQUENCE AND COMPLETION DATES

2.1 Thermal Cycling Test - Completed January 20, 1978

2.2 Humidity Test - Completed January 31, 1978

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3.0 TEST PROGRAM

3.1 Thermal Cycling Test

3.1.1 Test Procedure

The Solar Modules were subjected to High and Low Temperature testing per Solarex Specification Purchase Order No. 6231.

The Solar Modules were subjected to a High and Low Temperature test as follows:

The test items were placed in a high and low temperature chamber and the chamber conditions were controlled by a cam at temperatures in the range of +195°F to -40°F for a total of fifty (50) cycles.

Upon completion of the fifty (50) cycles, the chamber temperature was returned to room ambient conditions.

3.1.2 Test Results

There was no visual evidence of external physical damage or deterioration as a result of the Thermal Cycling test. The Solar Cell Modules were returned to Solarex Corporation for further evaluation.

3.2 Humidity Test

3.2.1 Test Procedure

The Solar Cell Modules were subjected to a Humidity test in accordance with MIL-STD-810C, Method 507.1, Procedure V.

Step 1: The test specimens were placed in the test chamber and dried at +54°C (129°F) for twenty-four (24) hours.

Step 2: The test specimens were then conditioned at +23°C (73°F) and 50 ± 10 percent relative humidity for twenty-four (24) hours.

The test specimens were placed in a humidity chamber and subjected to five (5) complete temperature-humidity cycles as described below. The relative humidity was maintained between 90 and 95%.

Step 3: During the first two (2) hour period, the temperature was raised uniformly from 70°F to 105°F.

Step 4: The temperature of 40.5°C (105°F) was maintained for sixteen (16) hours.

Step 5: During the last two (2) hour period, the temperature was decreased uniformly from 105°F to 70°F.

Step 6: The internal chamber temperature was maintained at 21°C (70°F) and the relative humidity at 95% for four (4) hours.

Step 7: Following the fifth cycle the test items were removed from the chamber and visually examined for evidence of deterioration or of adverse effects due to the environment.

3.2.2 Test Results

There was no evidence of external physical damage or deterioration. The Solar Cell Modules were returned to Solarex Corporation for further evaluation.

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