PHASE 2

ARRAY AUTOMATED ASSEMBLY TASK

LOW COST SILICON SOLAR ARRAY PROJECT

ANNUAL TECHNICAL REPORT

1978

Sang. S. Rhee, Gregory T. Jones

Kimberly L. Allison

JPL CONTRACT NO. 954865

Sensor Technology, Incorporated
21012 Lassen Street
Chatsworth, California 91311

"The JPL Low-Cost Silicon Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE".

PREFACE

The information presented in this report on Phase 2 of the Array Automated Assembly Task represents the work performed from September 20, 1977 through December 31, 1978 by Sensor Technology, Inc., in Chatsworth, California. The program was directed by Sang S. Rhee. Principle contributors included Gregory T. Jones, Kimberly L. Allison, Sanjeev Chitre, Charles Snyder, Louis R. Rosinski, Nelson E. David, and A. PeBenito. Also contributing to the work performed on the Laser Trimming and Holing Operation and the Spray-on Dopant Tasks were respectively Robert A. Kaplan from Quantronix Corporation and Jeffrey Dexter from Advanced Concepts Equipment Corporation. The JPL Technical Program Manager during this report period was Paul Alexander. The contents of this report were reviewed by Paul Alexander and Clay Olsen of JPL.

ABSTRACT

This program was conducted to develop and demonstrate those solar cells and module process steps which have the technological readiness or capability to achieve the 1986 LSA goals.

Seventeen process groups were investigated. Very promising results were achieved. A laserscribe computer program was developed. It demonstrated that silicon solar cells could be trimmed and holed by laser without causing mechanical defects (i.e. microcracks) nor any major degredation in solar cell electrical performance. The silicon wafer surface preparation task demonstrated a low-cost, high throughput texturizing process readily adaptable to automation. Performance verification tests of a laser scanning system showed a limited capability to detect hidden cracks or defects in solar cells, but with potential equipment modifications this cost effective system could be rendered suitable. A general review of currently available thick film printing equipment provided the indication that state-of-the-art technology can adequately transform the throughput capability of current printing machines to the elevated rate of 7200 wafers per hour. The LFE System 8000 silicon nitride plasma deposition system with the inclusion of minor equipment modifications was

shown to be consistent with the 1986 LSA pricing goals for the overall cost of the solar cell. The performance verification test of the silicon nitride A.R. coating process provided the result that texturized, A.R.coated solar cells display a 14.1% improvement in electrical performance over identical solar cells without an A.R. coating. A new electroless nickel plating system was installed and demonstrated a low-cost, high throughput process readily adaptable to automation. A multiple wafer dipping method was investigated and operational parameters defined. A flux removal method consisting of a three stage D.I. water cascade rinse system with ultrasonic agitator was found to be very promising.

A fully automated serial flow laser trimming and holing system was identified. It was shown to be a low-cost system which maintains a high volume throughput with large output yields. A computerized solar cell and module test and data storage system was designed and fabricated. This system can store and analyze solar cell and module electrical performance data, as well as group solar cells and modules into predesignated categories. A semi-automated spray-on dopant junction formation process was developed. demonstrated that a low-cost spray-on dopant junction formation technique could be utilized to produce high efficiency solar cells.

An indepth module construction study based on a unique solar cell center hole interconnection concept was performed. This study included a solar cell conceptual design, a module conceptual design and module assembly. A precision solar cell positioning system consisting of robot arms with multiple pick-up heads was deemed suitable for use in module assembly. Two hexagonal solar cell module models were fabricated.

A solar cell and module process sequence was defined for the array automated assembly task. An indepth SAMICS cost analysis based on large volume throughput was performed. The SAMICS results included an assumed silicon wafer selling price of 22 cents per peak watt, a calculated solar cell manufacturing cost of 19.8 cents per peak watt, an estimated encapsulation material cost of 18.85 cells per peak watt and a module assembly cost of 9.29 cents per peak watt. The total 1986 module selling price was determined to be 69.94 cents per peak watt in 1975 cents.

It was concluded that the solar cell process costs and module assembly costs were in line with the 1986 LSA goals. Additional work to reduce the encapsulation material costs was recommended.

TABLE OF CONTENTS

TABLE OF CONTENTS, contd.

TABLE OF CONTENTS. contd.

LIST OF FIGURES

LIST OF TABLES

INTRODUCTION

The work performed by Sensor Technology, Inc., in Phase 2 of the Array Automated Assembly Task is part of the DOE/JPL Low-Cost Solar Array (LSA) Project. The primary objectives of the program are to demonstrate and, where necessary, to develop those solar cells and module process steps which have the technological readiness or capability to achieve the 1986 LSA goals.

Large volume, high throughput rate [1] and automation [2] are very necessary low-cost qualifications for solar cell and module production companies. The 1986 LSA production goals seek 500 megawatts per year at 50 cents per peak watt.[1] [3] A major effort in this contract was applied toward the analysis of solar cell and module process steps for throughput rate, cost effectiveness and reproducibility. The analysis was based on a number of assumptions which are listed below:

(1) 500 MW/year are produced in 1986 (The specific year was not critical to this study) at $.22/watt in 1975 dollars for silicon wafer material and at $.50/watt in 1975 dollars for the finished module.

(2) Two vertically integrated companies, CELLCO a solar cell production firm and MODULCO a module production firm will share 40 percent of the market, 200 MW, and MODULCO will buy 100 percent of its' solar cells from CELLCO.

(3) CELLCO and MODULCO require 4.7 shifts per day, 24 hours per day, 7 days per week, 345 operating days.

(4) The solar cells will have at least a 14.7% encapsulated efficiency and a production yield of at least 95%.

(5) The module will have the dimensions of 2' x 4', will contain 119 equivalent modified hexagonal solar cells (102 full cells and 34 half cells), and will have a power output of 90 watts at 100 mW/cm^2 solar insolation.

As a result of the above, nominal throughput is expected to be as follows:

CELLCO: 278 million solar cells per year
or 210.3 MW per year.

MODULCO: 2.222 million modules per year
or 200 MW per year.

A conceptualized view of an automated process sequence is discussed in the technical sections of this report. Each step in the process sequence was analyzed in one of the seventeen process groups. Major emphasis was placed on the development of two solar cell process steps: laser trimming and holing automation and spray-on dopant junction formation.

The results of the work performed in Phase 2 of the Array Automated Assembly Task form the basic foundation through which fully automated solar cell and module process sequences are conceived. One such sequence is shown in Figure 1 by the artist conception of the spray-on dopant junction formation process. Ultimately, solar cell and module process sequences, such as this one, will be designed and constructed and jointed together to form an array automated assembly facility that achieves the 1986 LSA goals.

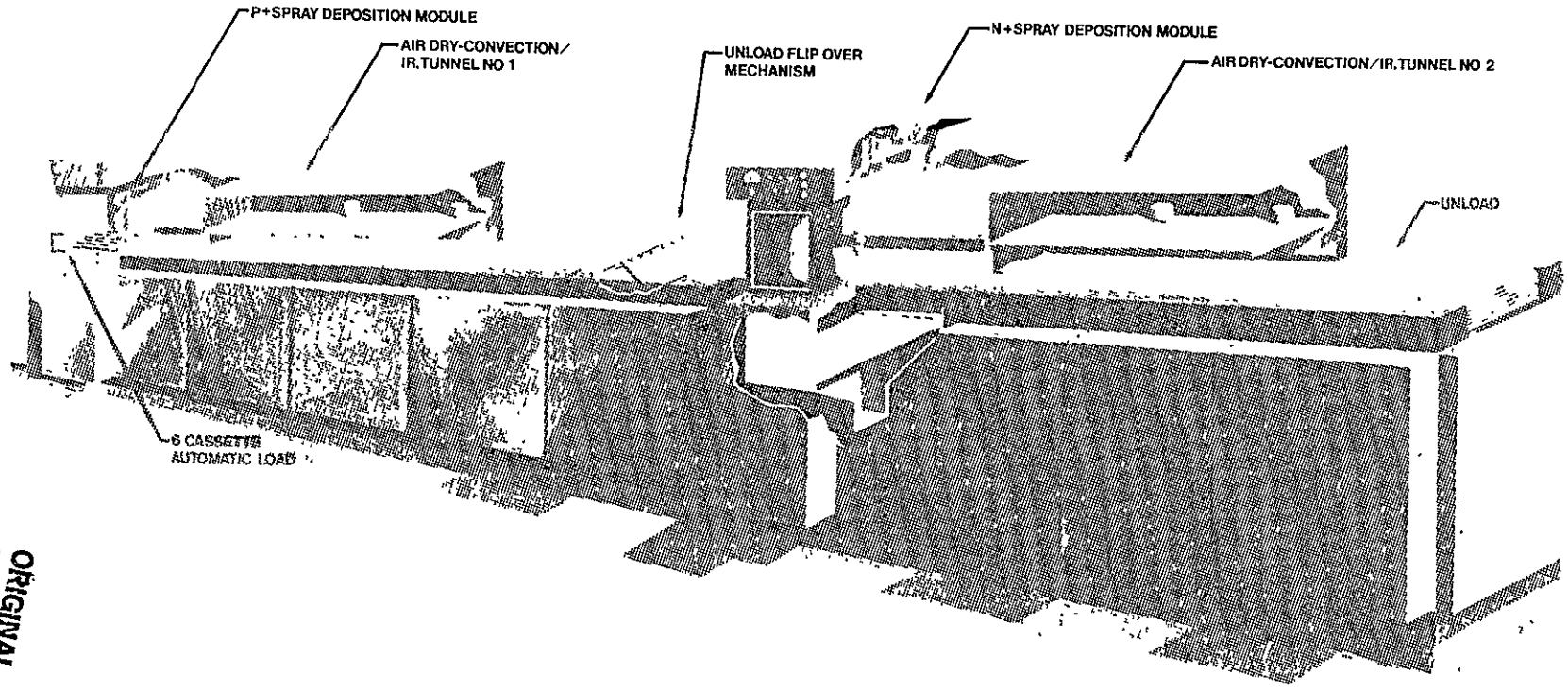


Figure 1. Artist conception of the spray-on dopant junction formation process which will have a throughput rate of 1200 wafers per hour.

TECHNICAL DISCUSSION

1. Cell Test Data Acquisition

Sensor Technology presently utilizes a solar cell module test data acquisition system to measure and record the electrical performance under a pulsed Xenon solar simulator for large scale production contracts. This system automatically samples the module electrical performance and plots the I-V characteristic curve on an X-Y plotter.

A design modification of our electronic equipment was undertaken for the purpose of demonstrating that a single solar cell can be automatically tested and its electrical performance recorded. A sketch of the test equipment is shown in Figure 2. The complete system consists of a pulsed Xenon light tower, a temperature controlled solar cell mounting block with reference cell, an automatic solar cell test data acquisition system, and an X-Y plotter. The equipment demonstrated the capability of measuring the electrical performance of solar cells for use in evaluation of solar cell quality and suitability for module assembly. The cell test data acquisition system samples the Xenon solar simulator at 100 mW/cm^2, and automatically records the solar cell short circuit current (I_{SC}), open circuit voltage (V_{OC}), current at a predetermined voltage (I_V), and the cell current (I_{cell}) and

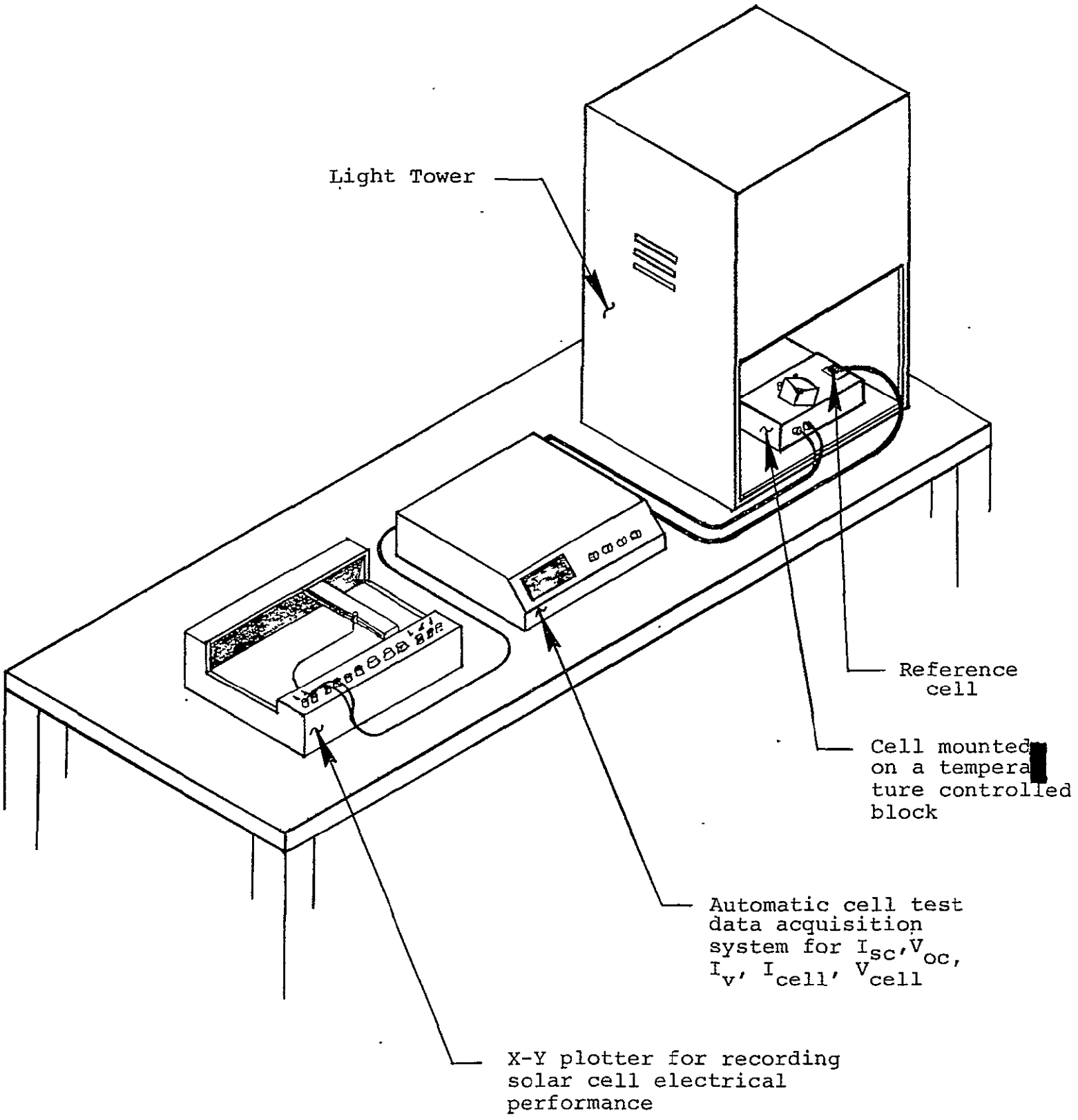


Figure 2. Sketch of experimental apparatus for the automatic cell test data acquisition system.

voltage (V_{cell}).

The equipment utilized in this task showed that an automated system for collecting solar cell electrical performance data is extremely conducive to module assembly. A continuation of this data acquisition system for solar cells on an extension to include solar cell modules for large scale automation was performed in connection with Task 13 and is discussed in detail in that section.

2. Plasma Etching of Resist

Plasma etching is a popular process in the semi-conductor industry and is reportedly more economical than standard chemical methods. Its applicability extends throughout the following five areas: (1) silicon oxide or silicon nitride etching, (2) photoresist etching up to 2 μm thickness, (3) silicon surface cleaning, (4) silicon splatter removal resulting from laserscribing and (5) higher resolution opening photolithography.

No manufacturer to date, has made any attempt to apply this method towards the removal of thick film resist. The major reason for this is simply that the process is much too slow to effect the removal of a thick film resist which is approximately 5 mils thick.

Consequently, no etching rate data has been made available for thick film resist. If it is assumed that the etching rate of photoresist is identical to that of the thick film resist, this would imply that an 8000 Å thick film can be removed within 15 minutes as claimed for LFE Corporation's (Waltham, Massachusetts) PDS-504-AP (4) Model and thus the required process time for a 5 mil thick resist which is used in the photovoltaic industry will be approximately 40 hours. The SAMICS results for this process showed the total cost to be $1.02 per peak watt.

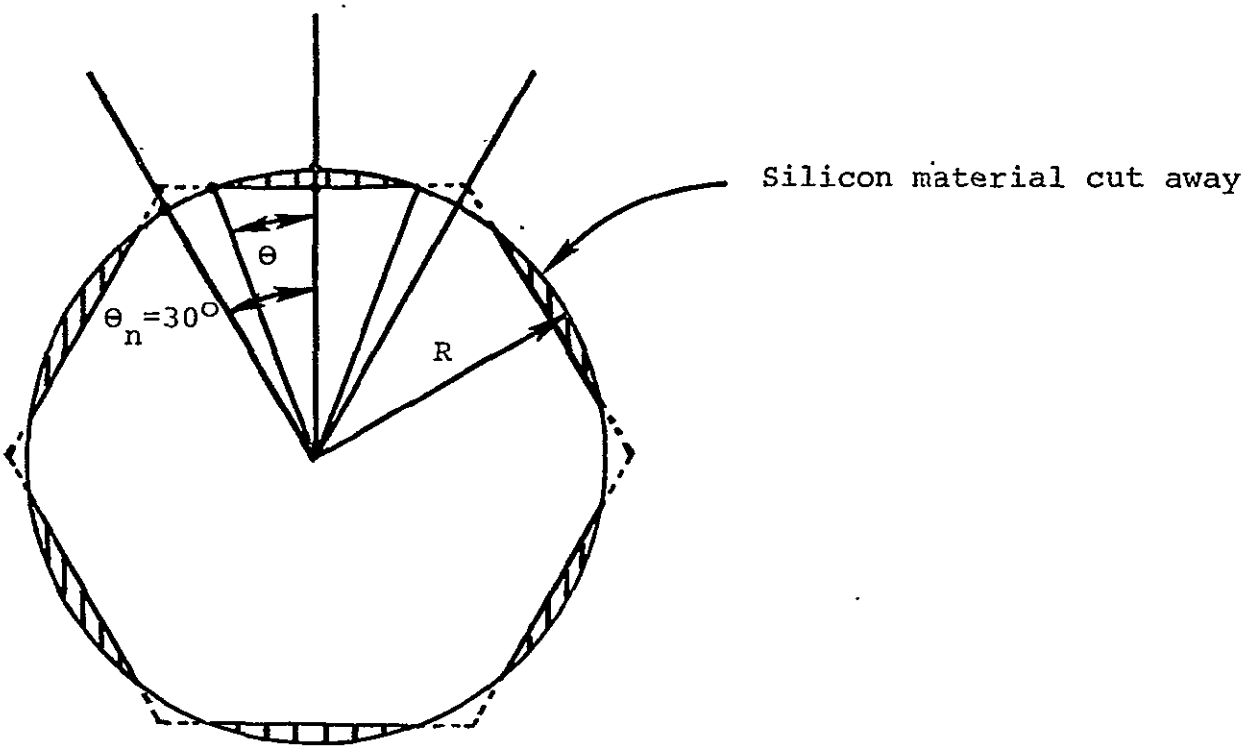
In view of the above considerations, the application of plasma etching to thick film resist removal did not look very promising, and consequently no further effort was expended in this task.

3. Laser Trimming and Holing Operation

The concept of hexagonal solar cell trimming and holing by laser was formulated exclusively by Sensor Technology, Inc., in response to the overwhelming need for high efficiency, low-cost solar cells and solar cell modules.

The advantages derived from using a laserscribe to cut hexagonally shaped solar cells from round solar cells are two-fold. The first advantage lies in the significantly increased solar cell module packing efficiency available from hexagonal solar cells in

relation to round solar cells. This improvement in packing efficiency will serve to reduce the overall module packing material and surface area requirements for any designated module power output. Ostensibly, however, the reduction in space utilization described above will occur only at the expense of silicon wafer material utilization, since the hexagonal wafers are scribed directly from larger area round wafers. To circumvent the disadvantages associated with the trade-off between silicon material utilization and module packing efficiency, it was concluded from a former study (ERDA/JPL-954605-78/5. Final Report)[2] that a compromise in the form of a modified hexagon as shown in Figure 3, will lead to an optimal utilization of silicon material. The second major advantage derived from laserscribing hexagonal solar cells was first discovered in JPL Contract 954605[2]. It was found in that program for the development of low-cost, high energy-per-unit-area solar cell modules that the laser-scribe can reduce junction current leakage losses by trimming the edges of solar cells; it can cut through the p-n junction (without conductive coatings) without damaging the junction; and that the junction current leakage caused by edge effects from the laserscribe is uniform, consistent and very small.



R = radius of silicon wafer

Θ = half secant angle of a modified hexagon

Θ_n = 30°, half angle of a full hexagon

Figure 3. Definition of a modified hexagon

A major new concept developed in this program utilizes the laserscribe to cut a hole in a solar cell. This holing or trepanning operation involves the removal of a circular plug at the wafer center. This technique is imbued with a dual purpose. The central hole is an integral component of a novel solar cell design (see Task 17) which utilizes central hole current collection, as opposed to the conventional method of edge current collection. In addition to enhancing the power conversion efficiency of these solar cells, the central hole will facilitate module fabrication by reducing the number of required solar cell interconnections.

In view of the above considerations, it is evident that the laser trimming and holing operation will lower the overall module processing costs and contribute to an improvement in solar cell power conversion efficiency. The Quantronix Corporation Model 603 laserscribe system shown in Figure 4 had the technological capability of laser trimming and holing, however, a special computer program was required which allowed us to achieve this laser trimming and holing objective. Quantronix Corporation was therefore subcontracted to develop a hexagon/central hole computer program logic board and to program accordingly the model 603 laserscribe.

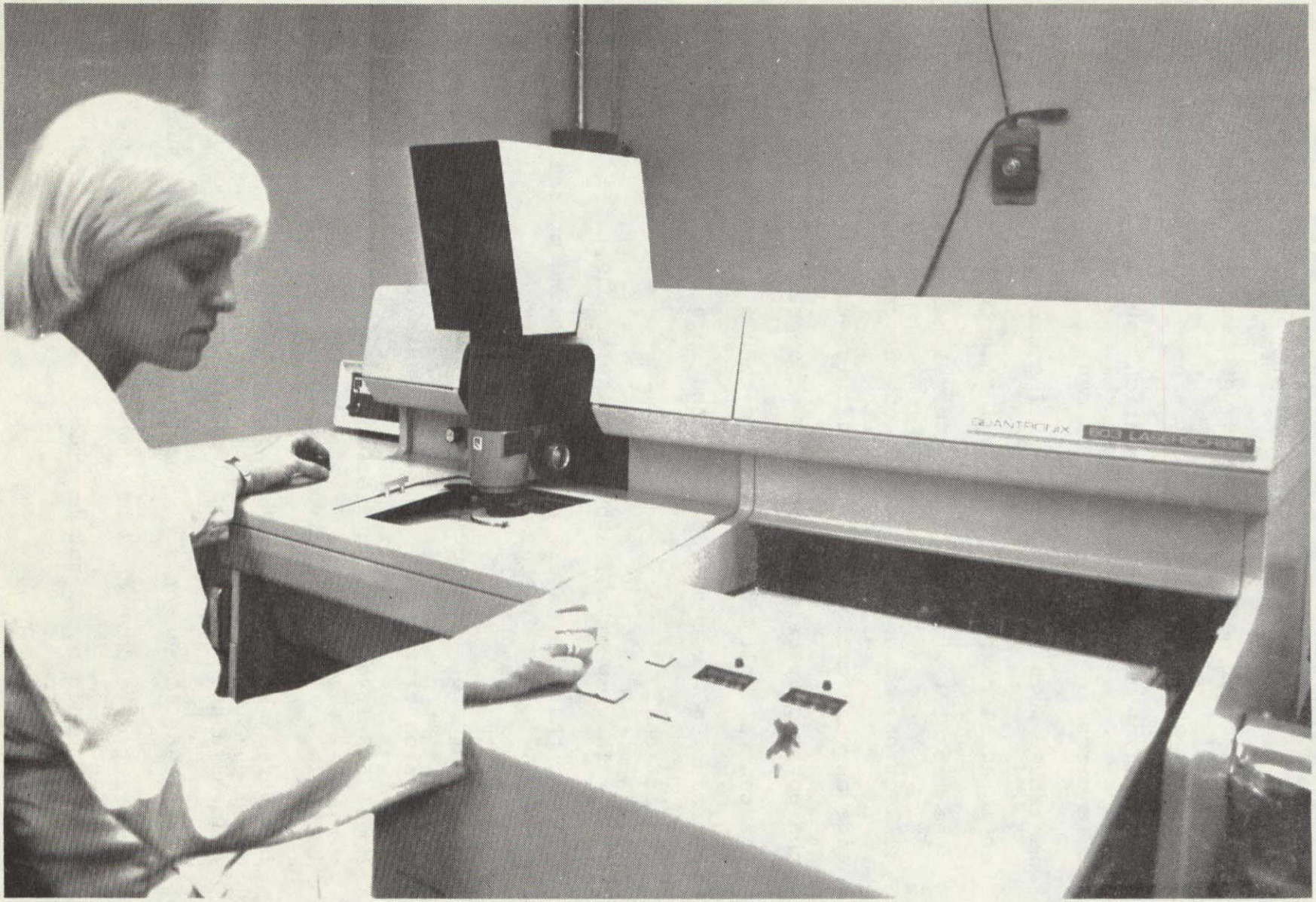


Figure 4. Laserscribe used to cut hexagonal solar cells from circular solar cells. It was programmed to cut a hexagonal solar cell with a center hole.

OPTION 6. Generation of central hole in conjunction with scribed hexagon as specified in Options 2 and 5.

A special monitor program produces the appropriate position coordinates and velocity data. Special hardware enables the above patterns or options to be produced with accuracy at high speeds.

Experiments were performed to demonstrate the capability of the laserscribe with logic board to scribe and trepan (or hole) hexagonal solar cells. In their final report to Sensor Technology, Quantronix Corporation presented documentation of their studies, and concluded that their laserscribe and logic board yield favorable results. This was confirmed by Sensor Technology on our own laserscribe equipment. The results are discussed below.

The silicon solar cells were scribed by laser and cracked in order to investigate the feasibility of mechanically removing all excess wafer material remaining after formation of the hexagonal shape. All wafer samples were inspected for edge quality and found to be acceptable. Of the sample lot of ten wafers which was processed for the mechanical wafer cracking experiment, one wafer was broken across the wafer face, which constitutes a failure. However, the ease with which cracking occurred demonstrated the feasibility of the method.

The viability of laser trepanning silicon solar cells was tested. Quantronix Corporation was completely successful in their experiments. After making some necessary optical adjustments involving the laser focal point depth for cutting a central hole, Sensor Technology achieved very good results. The laser holing operation was tested with twenty-five wafer samples under the following process parameters:

Number of Samples:	25
Laser Power:	17.5 watts
Laser Cycle:	10 KHz
Laser Mode of Operation:	"B"
Table Speed:	2.0 in/sec.
Number of Passes:	12
Cutting Time:	10 seconds
Hole Diameter:	0.2 inches

Twenty-four out of twenty-five wafers were successfully scribed which constitutes a 96% yield factor.

The operational simplicity, high yield factor, and demonstrated technological capability of the laserscribe equipment in trimming and holing solar cells, is indicative of the overwhelming success of the laser trimming and holing operation. This technique is highly recommended, however, in order to comply with the 1986 LSA production goals, it is essential that the laser trimming and holing

operation be fully automated. An indepth discussion of laser trimming and holing automation is presented in Task 12.

4. Wafer Surface Preparation

Wafer surface preparation plays an important role in solar cell power output. In addition to reducing reflection losses from the front surface of solar cells, the texturizing process prepares the silicon wafers for the subsequent junction formation step. From the experimental results of this program and from work reported elsewhere, [2,4] it was demonstrated that the wafer surface preparation process yields silicon wafers which have black antireflection surfaces, which are uniformly etched and are batch to batch reproducible. The wafer surface preparation equipment shown in Figure 5 also demonstrated a high throughput rate; it can process, after the initial start up time, 2400 wafers per hour.

The wafer surface preparation process consists of five steps. They are (1) wafer surface cleaning, (2) surface macrostructure etching, (3) four stage cascade rinse, (4) surface macrostructure final cleaning, and (5) final rinse/spin dry.

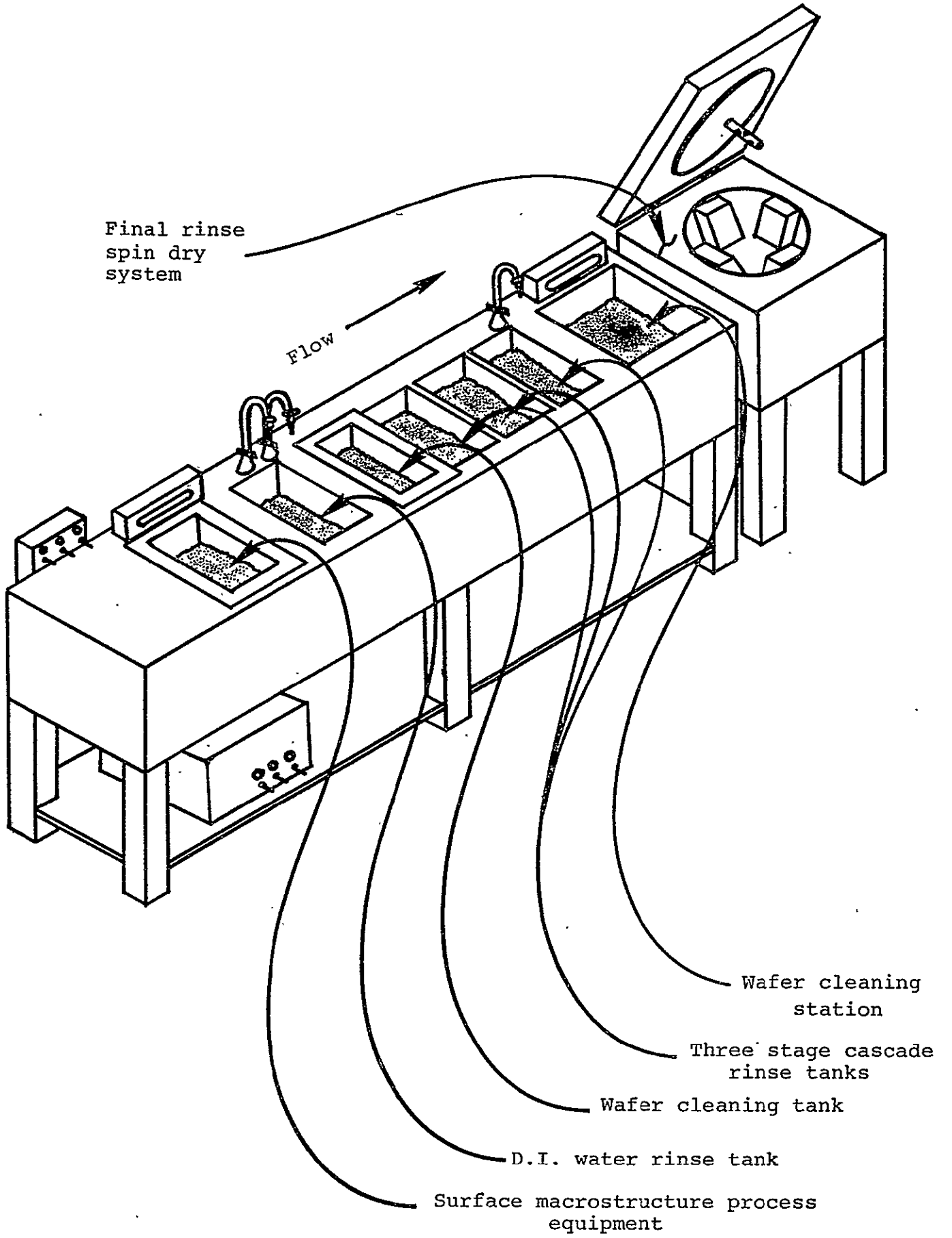


Figure 5. Sketch of surface macrostructure process equipment

Ninety millimeter diameter, Czochralski (100) as cut, round silicon wafers were procured and sample inspected for experimentation. They were manually placed into cassettes which hold twenty-five wafers. Four cassettes or one hundred silicon wafers were manually loaded into a carrier basket ready for the first process step.

The first step in the wafer surface process consists of a two stage wafer surface cleaning procedure. The silicon wafers are placed into hot trichlorethylene (.9cc per wafer) for five minutes (preferably in an ultrasonic tank) followed by a 5 minute methanol dip (.9 cc per wafer). Since 9 liters are used in these processes, it is necessary to replace the solutions every eight hours. This process step cleans any organic contaminants off the wafer surfaces which might otherwise impede the surface preparation etching step.

The second step in the wafer surface preparation process is surface macrostructure etching. The carrier basket containing the silicon wafers is introduced into an ultrasonic stainless steel tank which has been filled with a 10% solution by weight of NaOH to deionized wafer at $85^{o}C \pm 2^{o}C$. Suspended in the tank is a nitrogen bubbler system which is designed to agitate the solution in addition to the ultrasonics. Ten liters per minute of nitrogen gas are required for the bubbler designed by Sensor

Technology, Inc. It is to be noted that the design and placement of the bubbler with respect to the silicon wafers determines the consistency of the surface macrostructure etching process. A large amount of nitrogen bubbles which are small in diameter contribute to uniform surface macrostructures. The process time for this step is five minutes.

The carrier basket is manually removed from the surface macrostructure etching tank and placed into the first ultrasonic stage of a four stage cascade rinse system which make up the third step in the process. The carrier basket remains for five minutes in each of the four stages. Hot deionized water flows at a rate of 3.8 liters per minute from the fourth stage where the D.I. water input temperature is $80^{o}C \pm 5^{o}C$ to the first ultrasonic stage where the D.I. water output temperature is $72^{o}C \pm 5^{o}C$. The silicon wafers get progressively cleaner as they move from the first stage to the fourth stage of the cascade rinse system.

The fourth step in the wafer surface preparation process is final cleaning. The wafer jigs are manually removed from the cascade rinse and introduced into a sulphuric acid/hydrogen peroxide mixture at $70^{o}C \pm 5^{o}C$ for five minutes. This solution removes any remaining deposits of sodium hydroxide

that may be trapped in the wafer surface. The wafers are then rinsed off in running D.I. water for five minutes.

The fourth wafer surface preparation process step, was found to be expensive as is discussed in a later SAMICS section. This step was also found to have only a minor effect on solar cell electrical performance. It is essentially a precautionary measure to ensure the cleanliness of the texturized silicon wafers. Under an optimized wafer surface preparation process, the final cleaning step should not be necessary. Therefore, it is recommended that this process step not be considered in the overall 1986 wafer surface preparation process.

The last step in the wafer surface preparation process is the final rinse/spin dry. The last remaining wafer surface contaminants are removed in this five minute cycle. The wafers are now ready for the junction formation process.

The wafer surface preparation process demonstration equipment was used to process 100 ninety millimeter diameter silicon wafers for each carrier basket or four cassettes carrying 25 wafers each. The system capability is 200 wafers per process step assuming two layers of 100 wafers each. The wafer surface preparation process therefore, can produce, after the initial startup time, 2400 wafers per hour.

A SAMICS cost analysis was performed on this task and showed a total cost of 1.49 cents per peak watt in 1975 cents for a fully automated system with a wafer throughput of 6000 wafers per hour. Included in the analysis is the elimination of the final cleaning step (step 4 above) and the replacement of the final rinse/spin dry step with a clean air blow dry system. A detailed cost analysis is discussed in a later section. It can be concluded that the wafer surface preparation process will contribute significantly to reducing the cost and increasing the solar cell and module efficiency which is in line with the 1986 LSA goals.

5. Laser Scanning Inspection

An investigation of three types of wafer scanning procedures was conducted for the purpose of selecting a suitable method for the detection of mechanical defects in solar cells.

The first method under consideration was the X-ray scanning method which has a demonstrated capability of detecting mechanical failures. There is, however, a serious drawback with this method of scanning silicon wafers for the detection of mechanical defects. The suitable technique for data acquisition of this type of X-ray scanning is not available at the current technology. This data acquisition problem could be eventually overcome but only as the result of extensive study which is well

beyond the scope of this task.

The second method investigated was IR-Micro-Inspection developed by Electrophysics in New Jersey. It was found that with this method, the detection of soldering faults would be extremely difficult, and consequently, this procedure was not suitable for our requirements. The third method investigated was laser scanning. This method for detecting mechanical defects in silicon material is presently being studied at the Jet Propulsion Laboratory, and a commercially available system is being manufactured by Advanced Semiconductor Materials Laboratory in Phoenix, Arizona. The JPL laser scanning system appeared to have favorable prospects. Its potential optimization, however, and its practicality for production line applications requires further study. The ASM laser scanning system is available for production applications and was found to be the most suitable scanning technique of the three methods considered.

An indepth analysis was made of the ASM Automatic Surface Inspection System (ASIS) in order to accurately assess its feasibility for use in production line applications. In this capacity, samples of silicon solar cells with nickel metallization and solder, and also nickel metallization without solder on texturized and untexturized cells were provided for

the performance verification tests of the ASIS equipment. The primary objectives of the performance verification tests were as follows:

(1) Detection of micro-cracks.

(2) Detection of floating metal.

(3) Detection of breaks in metallization which develop during the plating process.

(4) Detection of saw damage.

(5) Detection of soldering defects.

The current equipment is designed specifically for the inspection of 3" diameter wafers, but with the incorporation of minor equipment modifications, its range of applicability can be extended to 90 mm diameter wafers.

The ASM Automatic Surface Inspection System (ASIS) is an MPU-controlled system that quantitatively measures the defect level present on a highly reflective surface. Primarily designed for application in the semiconductor industry, the ASIS system can automatically monitor the wafer surface quality before and after critical processing steps.

During the course of experimental studies, it was shown for polished surfaces that major cracks greater than .15 mils., saw damage, and fingerprints could all be easily detected. Due to the inherent resolution limitations of the laser beam, micro-cracks, floating metal, and poor solder contacts were all undetectable. This same line of reasoning will apply equally well to texturized surfaces with the one exception of fingerprint detection which is precluded as a result of the discontinuity of the fingerprint pattern over the pyramidal surface structure of the texturized solar cell.

The laser beam size which is currently 15 mils wide, has been determined to be the major limiting factor with regard to the ultimate diversity in application of the ASIS equipment. This conclusion is a consequence of the inherent resolution limitations of the laser beam. The ASIS system, as it is currently configured, will not meet our requirements. However, it is expected that with the incorporation of suitable equipment modifications, the ASIS system could offer excellent prospects.

A cost estimate was made for the ASM Automatic Surface Inspection System for the purpose of establishing its cost effectiveness. The throughput of the ASIS system is currently 900 wafers/hr., which falls short of the projected 1986 pricing goals. This figure can, however, be significantly enhanced by utilizing a multitrack system. The resulting process cost corresponding to the ASM system was found to be 0.672¢/watt in terms of 1975 dollars which is low enough to ensure its feasibility for usage in an automated assembly line.

In conclusion, the ASM ASIS system has a potential for use in the inspection of mechanical defects in solar cells in view of process cost. However, it will require further development effort to detect all the types of cracks in the solar cells.

6. Wafer Printing

The current thick film printing technology was reviewed and some of the anticipated problem areas were investigated. The current high-speed automatic thick film printing equipment was found to be completely adequate for standard catalog sold devices such as resistor networks or panel displays. A large size silicon solar cell application would, however, require a special design in order to achieve any degree of automation. An illustrative example of a typical problem area which would be encountered with this process procedure is discussed below along with some suggested modifications.

The wafer printing process entails the following sequential steps: loading, printing, leveling time, drying, and unloading. The printing machine can operate at a potential rate of 7200 wafers per hour with the restriction that small-sized wafers be used. With the double head feature, it can operate at the potential rate of 7200 wafers per hour, independent of wafer size. By using the former option, it was found that the required furnaces and dryers would be prohibitively expensive and large

and would also consume a significant amount of floor space.

An example that illustrates the floor space problem entailed by current thick film printing equipment is presented. Let one assume that a 3.5 inch diameter wafer is printed at the rate of 7200 wafers per hour and that the leveling time and IR drying time require up to five and fifteen minutes respectively. Let it also be assumed that the belt width of the furnace is three feet so that ten wafers can be loaded into one row. If this is the case, then the required speed of the furnace belt will be four feet per minute and the total length of the belt will be eighty feet. Furthermore, make the assumption that the unloading device requires a minimum length of two feet. By taking into consideration the dimensional aspects of the above components, it is clear that the printing speed will be limited by the required floor space.

This problem can be resolved if a trayoven or overhead proofer, which is used extensively in the bakery industry, is applied. This process technique can be utilized in conjunction with a multilayer conveyor. For example, if a four layer tray conveyor

is used, the overall length will be within the 25 foot range with a total oven height of five feet. This arrangement has the beneficial feature of allowing the installation of the drying chamber overhead, thus eliminating the need for excessive bottom floor space which could serve alternate functions. The only difficulty foreseen with this method is the loading and unloading process which will require a special design in order to prevent breakage of the silicon wafers.

There are several varieties of loading devices which are available in today's market such as vibratory bowl feeding, stack-type magazine and shelf-type magazine. The only suitable method found applicable to silicon wafers is the shelf-type magazine. This is the only method which incorporates the prevention of contamination or damage to the wafer surface and also protects the cell from breakage due to mishandling. The problem encountered by this method is that the magazine is unable to hold many wafers. If the printer operates at the rate of 7200 wafers per hour, then one magazine will be cured in only 1.5 minutes. Consequently, multiple magazines would be required in either a multiposition shuttle

arrangement or in a multiple magazine carousel. Similar problems exist at the unloading station where the printed wafers are to be loaded into carriers which are used in the wafer plating process.

A final problem that should be considered in the wafer printing process is screen ware. A typical stainless steel mesh screen with emulsion is capable of enduring between 10,000 and 20,000 printings. Therefore, at the rate of 7200 wafers per hour, the screen will be rendered ineffectual every two hours. Recently a new type of screen has been developed with the capability of performing up to 50,000 printings. As a consequence of this development the problem of screen abrasion is not considered to be a significant deterrent toward the attainment of 1986 production goals.

Most of the technology required for high speed printing is already within present day capabilities. A general review of currently available thick film printing equipment has provided the indication that state of the art technology can adequately transform the throughput capability of the current machines to the elevated rate of 7200

wafers per hour. The manufacturers possessing this capability include Presco Divison of Affiliated Manufacturing Inc., Universal Instrument Company, and Fursland Division of Hutchington Industrial Company. A cost analysis was performed with the Fursland Model 33 since it is an automated version of the equipment currently in use at Sensor Technology, Inc. The Fursland Model 33 has a wafer throughput rate of 3000 wafers per hour. The SAMICS calculation indicates that the printing process cost accounts for 0.77 cents per peak watt and the drying* process cost accounts for 0.44 cents per peak watt. The total printing process cost thus becomes 1.21 cents per peak watt in terms of 1975 dollars, which is consistent with the 1986 LSA pricing goals.

* A tunnel drier, which is 3 feet wide and 26 feet long and has a belt with a speed of 1.7 feet/min., was used to perform the cost analysis.

7. Low Pressure Vapor Metal Depositions

The original plan devised for this task was formulated exclusively to investigate the deposition of copper onto P^+ silicon wafers. The low pressure vapor metal deposition of copper would serve as an ohmic back contact.

Despite the fact that several companies which reportedly possessed vapor metal deposition equipment were contacted, no one could be found during the scheduled time phase of this program task to have successfully performed copper depositions. Consequently, any conclusive results pertaining to the viability of this process were not reported.

8. Silicon Nitride A.R.Coating

Development of high efficiency low-cost solar cells requires the utilization of a low-cost process procedure for applying anti-reflective coatings. The current method utilized by Sensor Technology is silicon monoxide evaporation. This process step is expensive which is primarily due to its low throughput capacity and high electrical power consumption rate. In order to meet future pricing goals, it would therefore be desirable to formulate a new, more efficient and low-cost A.R.coating process method.

a) Current Technology

One of the most technologically advanced A.R. coating methods now in existence is silicon nitride coating by means of plasma deposition. Considerable effort, therefore, was channeled toward the investigation of current technology in the field of silicon nitride plasma deposition.

Initial work was directed toward identifying the most advantageous method available for the plasma deposition of silicon nitride onto silicon solar cells. Four companies were considered. They include Texas Instruments (T.I.), Advanced Material Technology (AMT),

Tegal Corporation, and LFE Corporation. Among the four representative systems the T.I. and AMT system characteristics were almost identical. Due to this similarity the T.I. system will not be considered in this discussion. Although a large number of parameters was used in the evaluation of each system, only the most crucial parameters are discussed below.

The key process information pertaining to the three companies is given in Table 1. It is clear that the LFE system maintains a minimal power and gas consumption rate in relation to the other systems. The concentration of silane gas used by the Company A and B systems approaches the six to eight percent range as opposed to the LFE system which consumes only one and one-half percent.

The wafer throughput of each system is a parameter of far-reaching significance. The throughput comparison of the three companies is given in Table 2. This table displays two throughputs; one is indicative of the recharacterizing process, and the other is not. Both the A and B company systems require recharacterizing processes due to the severe particulate "sandstorm" caused by the batch system design. Often this recharacterizing process is required for MOS applications.

TABLE 1. Comparative Operation and Information of Silicon Nitride antireflective coating manufacturers.

	LFE	A	B
Power Consumption (Deposition Mode)	4.5 KVA	25.0 KVA	10.5 KVA
Water	Not required	6 GPM	1 GPM
Exhaust	1"	2"	1"
Compressed Air	0.05 ft^3/hr.	0.2 ft^3/hr.	0.2 ft^3/hr.
Deposition Gases	1½% Silane / Ar, N_2	Silane, N_2 (1). Ammonia	Silane, N_2 (1), Ammonia
Cleaning	(CF_4 + O_2) (2) (3)	CF_4 (3)	CF_4 + O_2 + N_2 (3)
Vacuum Pump (main)	1100 l/M	990/6600 l/M	720 l/M

(1) Requires special storage area and safety precautions.
(2) LFE Patented Process U.S. Patent # 3,795,557.
(3) LFE - recommended (minimum) cleaning every 4 hours. A & B after every run.

Note: Process must be recharacterized after cleaning. This frequent cleaning is suggested due to significant particulate contamination problems; however, it is only marginally effective.

TABLE 2. Wafer throughput table for silicon nitride antireflective coating manufacturers.

	Max Wafers Per Batch		Batch Cycle (time in min).		Throughput W/O Recharacterizing		Throughput W/Recharacterizing	
	Diameter 3" - 100mm		Without Recharacterizing	With Recharacterizing after Plasma Clean	Wafers/hr. 3"dia.- 100mm dia.		Wafers/hr. 3" dia.-100mm dia.	
LFE	N.A.	N.A.	N.A.	N.A.	40	40	40	40
A	28	28	49	68	34 *	22 *	25 **	16 **
B	35	20	43	62	49 *	28 *	34 **	19 **

Typical throughputs based on customer feedback

N.A. - Not Applicable

* - Throughput computed without recharacterizing

** - Throughput computed with recharacterizing

Even without taking into account the recharacterizing process, the LFE system demonstrates high wafer throughput.

The important direct process costs for each process method have been estimated and a comparison is shown in Table 3. These estimates do not take into consideration such factors as overhead, floor space, and equipment costs. However, the above estimates can be used to elicit a relative comparison among the different systems. The results indicate that the process costs of the LFE system are only one-eighth of that of Company A and only one-third of that of Company B. Even though these estimations yield only approximate results, it is apparent that the LFE system will provide greater cost effectiveness than the other systems.

The results of the silicon nitride plasma deposition systems study discussed above show that the LFE system will provide the greatest efficiency both in terms of technical capability and operating costs.

A comparison will now be made between LFE's System 8000 and Sensor Technology's SiO Kinney evaporation system. The process costs for both systems have been computed in accordance with the SAMICS method which makes the underlying assumption that the wafer diameter is 90mm and the peak watt output is .653 watts. The monetary values are deflated back to 1975 dollars. The results are

TABLE 3. Direct wafer process cost for silicon nitride antireflective coating manufacturers.

	A	B	LFE
GASES	$.238	$ .063	$ .036
ELECTRICAL POWER	$.06	$ .02	$ .006
LABOR	$.06	$ .05	$ .003
COST PER WAFER	$.358	$ .133	$ .045
EQUIPMENT COST *	$75,000	$47,000	$75,000

* Domestic price

Size of wafer is 3 in. ~ 4 in.

specified in Table 4. These results indicate that the evaporation method is approximately twice as expensive as the LFE plasma deposition method. It also shows that the evaporation process will require considerable developmental improvements in order to achieve automation and reduced power consumption, while the LFE system will require a reduction in the equipment cost or an increased wafer throughput.

In view of the above considerations, the LFE System 8000 was selected as a potential mechanism for depositing silicon nitride anti-reflective coatings onto silicon solar cells. Consequently, a detailed description of the LFE System 8000 will be presented along with the proposed equipment modifications designed to elevate the existing silicon wafer throughput.

b) Description of the LFE System 8000

The LFE System 8000 is presently being utilized by semiconductor manufacturers to deposit 5000 Å to 8000 Å of silicon nitride onto silicon wafers, in part to provide a hermetic encapsulant. A simplified diagram which delineates the overall system design can be found in Figure 6. The LFE System 8000 is composed of a vacuum processing chamber which contains five separate process zones with the wafer receiving 20% of its total film in each zone in a sequential manner. The wafer must pass through a vacuum lock at the entrance

TABLE 4. A.R.Coating cost in 1975 dollars per Peak Watt for 3.5 inch diameter silicon solar cells, 0.653 watts per cell

	Kinney's SiO Evaporator	LFE System 8000 Silicon Nitride Plasma Depositor
MATERIALS	0.0975	0.0943
LABOR	0.2318	0.0382
UTILITIES	0.1738	0.0166
EQUIPMENT	0.0229	0.1502
FL. SPACE	0.0254	0.0177
BY-PRODUCT EXPENSE	0.0110	--
TOTAL	0.5624	0.3170

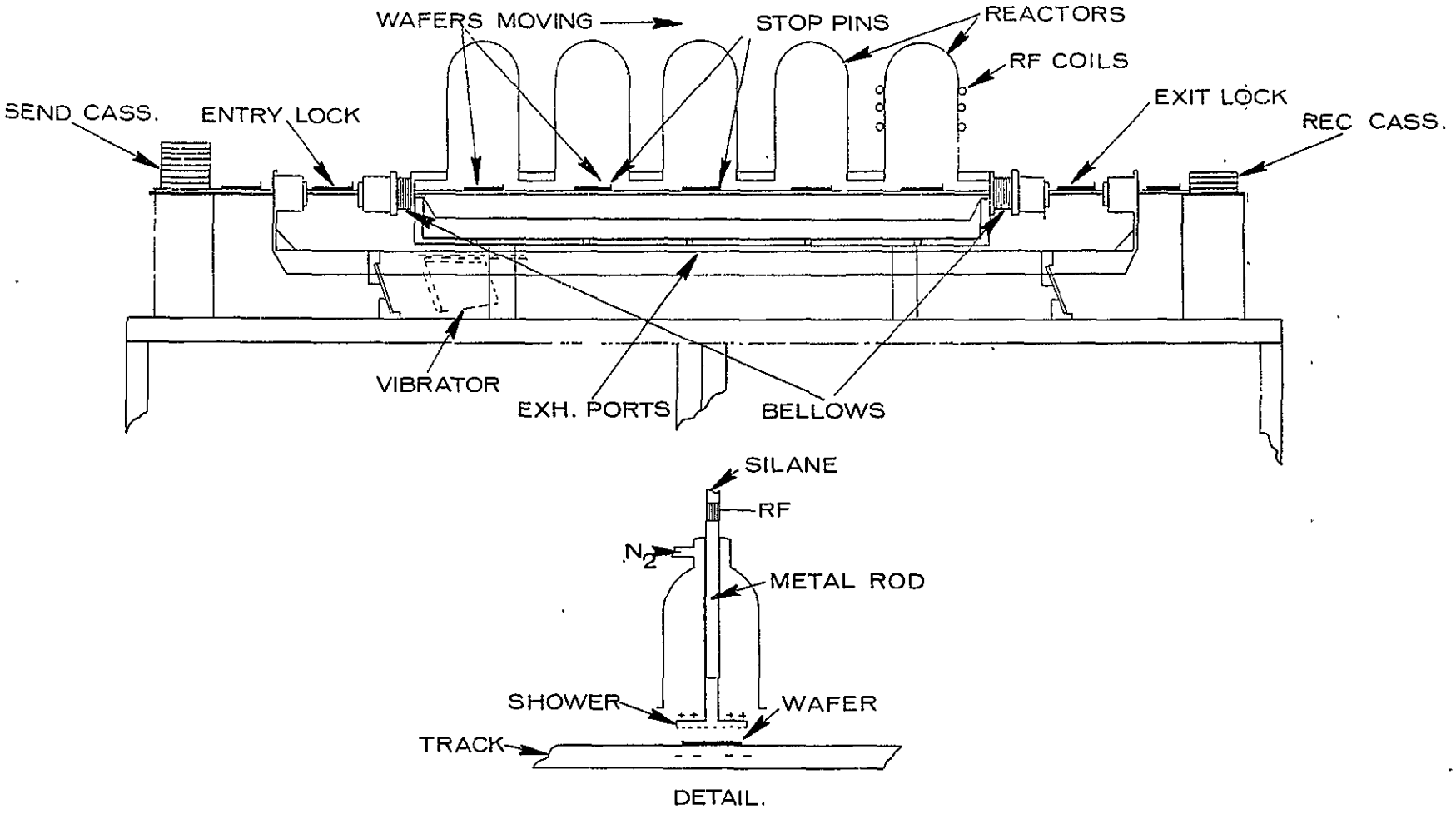


Figure 6. LFE 8000 system for silicon nitride anti-reflective coating.

to the chamber and exit the chamber through an identical vacuum lock after it has been processed at all five process locations. Upon completion of this procedure, a fully coated wafer will emerge every 120 seconds. This figure incorporates the 60 seconds expended for the plasma deposition of 1200 Å of silicon nitride onto the silicon wafers, as well as the 60 seconds required for the wafer movement through a vacuum lock on the main track. The wafer throughput of this systems is, therefore, only 30 wafers per hour. This throughput rate will need to undergo considerable improvement in order to conform to the stipulations set forth in the 1986 LSA pricing goals.

c) Feasible Modifications to the LFE System 8000 for an Enhanced Wafer Throughput

Feasible modifications of the LFE System 8000 silicon nitride plasma deposition equipment could be made which would significantly enhance the wafer throughput beyond the present rate of 30 wafers per hour. A new wafer throughput rate of 300 wafers per hour could be achieved. In order to arrive at this goal the total processing time must be reduced from two minutes to one minute. This reduced processing time includes 40 seconds to deposit 800 Å of silicon nitride (at a rate of 1200 Å per minute) and 20 seconds to load and unload the wafers. Five wafers could be deposited simultaneously, i.e. each wafer will make only one stop within the process chamber

instead of the present requirement of five stops. The system operation would then be divided into two time periods: In the first period movement of five unprocessed wafers into an entry lock from the sender will take place at the same time that five processed wafers are moved out of the exit lock into the receiver. While this wafer movement occurs external to the chamber, wafer depositions will take place within the chamber. In the second time period a sequential movement of five processed wafers from the process chamber into the exit locks and then a movement of five unprocessed wafers from the entry lock into the process chamber will take place. This process sequence would occur within the allowed processing time to achieve the enhanced throughput goal of 300 wafers per hour.

The key design modifications which will facilitate an enhanced wafer throughput are as follows:

(1) The wafer velocity on the process track should be increased and the positioning control improved. It is imperative that the wafer velocity on the process track be increased from 2 inches per second to 3 inches per second. This can be achieved by redesigning the vibratory subsystem so that an upper velocity limit is established. Since each wafer must be accurately positioned in the

process zone in order to obtain the proper degree of film uniformity, it is necessary to provide a "stop pin" on the process track. The stop-pins retreat into the track during wafer movement and then re-surface when the wafer movement ceases. The wafer movement is controlled by a microprocessor which receives wafer positioning data from the capacitive sensors which are imbedded in the process track. The microprocessor controls the turn-on of the vibratory mechanism and the stop-pins in accordance with the particular timing sequence under consideration and wafer positioning information.

(2) The wafer transition time through the vacuum locks should be decreased. The transition time of a single wafer from the sender to the vacuum lock and then from the vacuum lock to the process chamber is 30 seconds for the present system. In order to move five wafers through this sequential transition operation within a 40 second time period a new design is required. This new design has a cassette mechanism

located within the entry lock (and also the exit lock) allowing for a buffer of five wafers in the "ready" zones, namely, the entry and exit locks. As each wafer moves into the lock cassette, the cassette will index up (or down) one notch in preparation for the next wafer until all five wafers are received (or dispatched in the case of the exit lock).

The technical staff at LFE Corporation has accumulated extensive experience with the System 8000 and can foresee no immediate problems associated with the adoption of the state-of-the-art equipment modifications described above.

d) Performance Verification Test of the LFE System 8000 and Analysis of Silicon Nitride A.R.Coatings on Solar Cells

A performance verification test of the LFE System 8000 silicon nitride plasma deposition equipment was made. This test was implemented by comparing the I-V curves of texturized silicon solar cells which had undergone the silicon nitride A.R.coating process with the I-V curves of identically processed (same batch) solar cells without an A.R.coating. Upon analysis of the average I-V curves, which are shown in Figure 7 it was found that the texturized solar cells coated

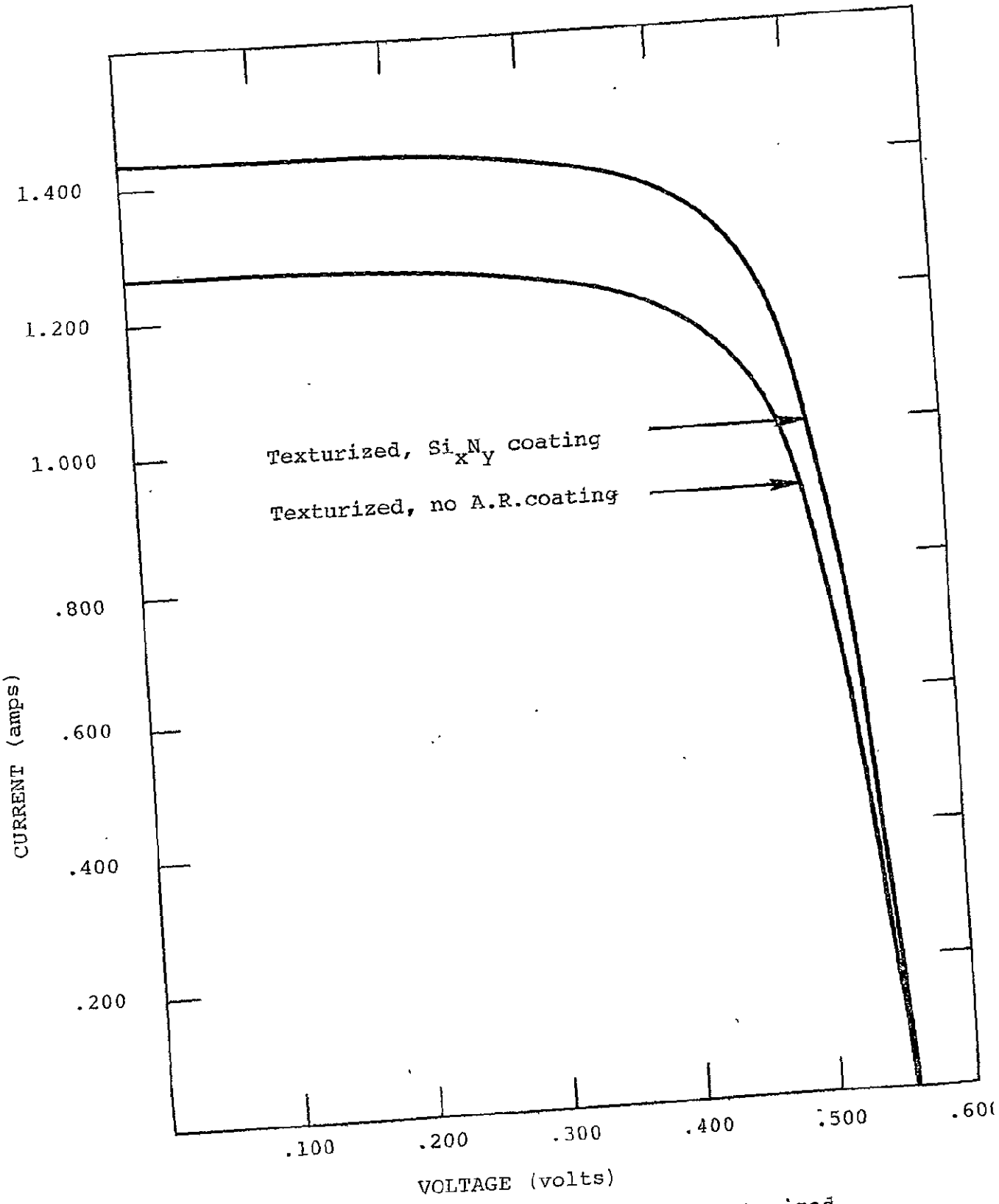


Figure 7. Electrical performance curves of texturized solar cells with and without a silicon nitride (Si_xN_y) anti-reflective coating. The solar cells are hexagonal with 50.8 cm^2 active area. They are tested at 28°C, 100 mw/cm^2 under tungsten light.

with silicon nitride displayed a significantly improved electrical performance over the uncoated texturized solar cells. In order to illustrate this point, I_{SC} for the A.R. coated cells was found to be 1.42 amps with a corresponding efficiency of 11.3% whereas for the uncoated cells, I_{SC} was 1.25 amps with a corresponding efficiency of 9.9%. Therefore a relative improvement in electrical performance of 14.1% was achieved through the application of silicon nitride A.R.coatings to texturized silicon solar cells, thereby verifying the performance of the LFE System 8000 silicon nitride plasma deposition equipment.

A solar cell electrical performance analysis was also conducted to determine the feasibility of inserting an anti-reflective coating step within the overall solar cell process sequence. A silicon nitride A.R.coating was applied to texturized silicon wafers after the $POCl_3$ diffusion step and prior to the metallization process sequence. Immediately after recording the solar cell electrical performance, the anti-reflective coating was removed with HF and then the electrical performance was recorded again. The two sets of data are shown in Figure 8 and are also tabulated in Table 5 for comparison. The difference in photovoltaic energy conversion efficiencies was substantial; a 31% difference was observed between the solar cells with an inprocess silicon nitride

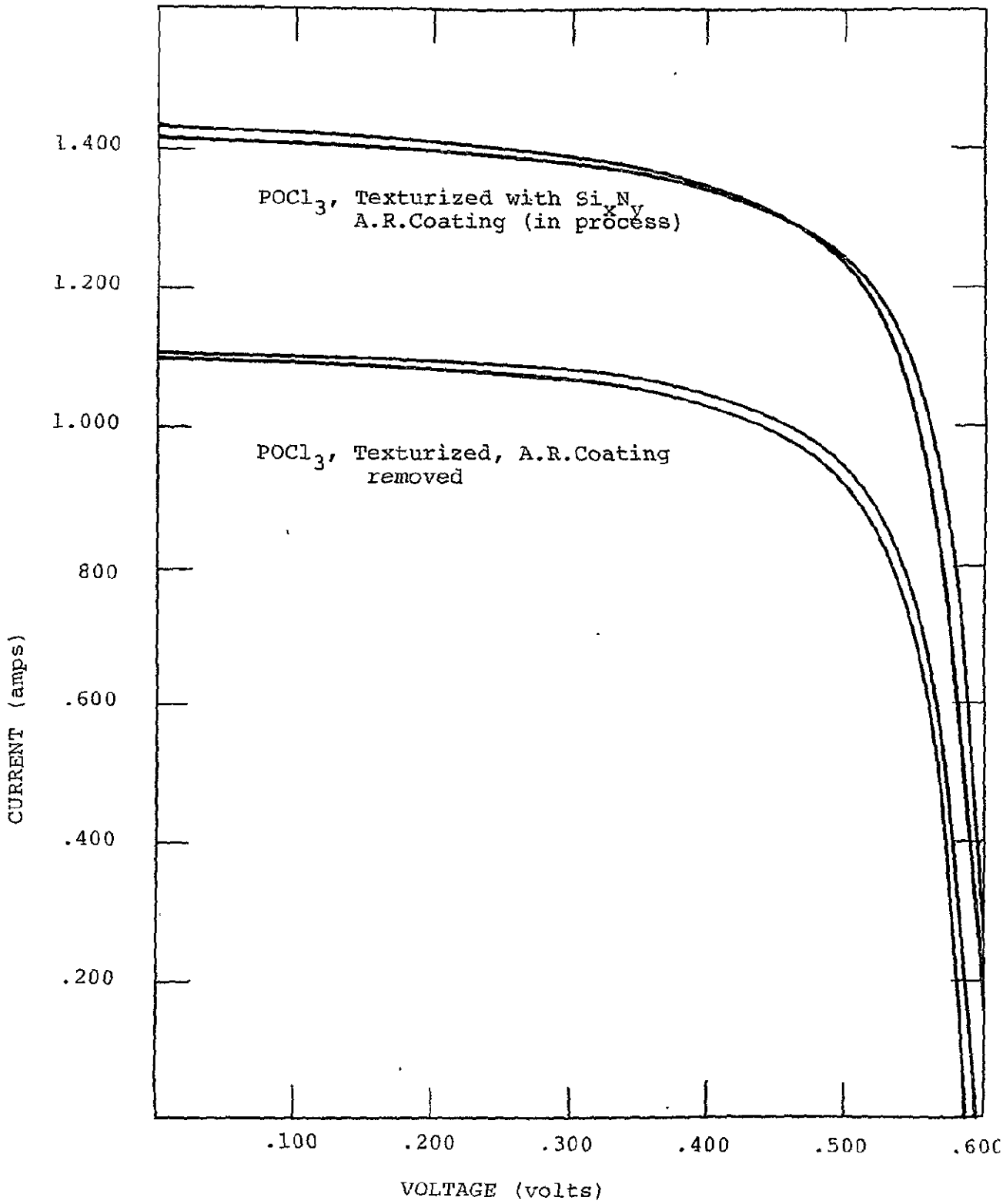


Figure 8. Electrical performance comparison between texturized hexagonal solar cells with and without silicon nitride (Si_xN_y) A.R.Coatings. Si_xN_y was applied in process. Cells have an active area of 45 cm^2 and were tested at 28°C under 100 mw/cm^2 tungsten light.

TABLE 5. Electrical performance comparison between texturized hexagonal solar cells with and without silicon nitride (Si_xN_y) A.R.coatings. Si_xN_y was applied inprocess. Cells have an active area of 45 cm^2 and were tested at 28°C under 100 mW/cm^2 tungsten light.

Cell No.	Isc (a) Hex	Voc (v) Hex	Ipp (a) Hex	Vpp (v) Hex	Ppp (w) Hex	FF Hex	η(%) Hex
$POCl_3$, Texturized, Si_xN_y (in process) Solar Cells							
1	1.43	.61	1.27	.475	.603	.691	13.41
2	1.41	.61	1.27	.475	.603	.701	13.41
Avg.	1.42	.61	1.27	.475	.603	.696	13.41
$POCl_3$, Texturized, A.R.Coating Removed, Solar Cells							
1	1.11	.595	1.00	.465	.465	.704	10.33
2	1.10	.590	.98	.465	.465	.703	10.13
Avg.	1.10	.592	.99	.465	.465	.703	10.23

A.R.coating and the same solar cells with the A.R.coating removed. The number of solar cells tested was too small to formulate any definite conclusions, however, there is an indication that improved solar cell efficiencies are possible by means of an in-process A.R.coating procedure. It is recommended that a detailed and thorough investigation of the application of in-process A.R.coatings for solar cells be performed.

e) Cost Analysis for the Modified LFE System 8000

A SAMICS cost analysis was performed to compare the present LFE System 8000 process sequence with the modified process sequence discussed above. The process cost for the 300 wafer per hour modified silicon nitride plasma deposition system was computed on the basis of the following assumptions:

(1) The electric power consumption rate will increase by 35% due to the power requirement of the vibratory structure.

(2) The equipment cost is expected to increase by approximately 35% of the current price due to the addition of a transition buffer system and larger microprocessor unit.

(3) The material consumption rate is proportional to the deposition rate which will remain identical to that of the current LFE 8000 system.

The results of a detailed SAMICS calculation of the silicon nitride A.R.coating process are shown in Table 6. The SAMICS result of 3.505 cents per peak watt in 1975 cents for the modified LFE System demonstrates a near order of magnitude decrease relative to the unmodified system. Although 3.505 cents per peak watt in 1975 cents is high, this process cost is still consistent with the 1986 LSA pricing goals for the overall cost of the wafer.

Table 6. The 1986 anti-reflective coating process cost in 1975 cents per peak watt

	LFE System 8000	Modified LFE System
Equipment	15.02	1.861
Floor Space	1.770	0.124
Labor	3.820	0.940
Materials	9.430	0.800
Utilities	1.664	0.274
TOTAL	31.704	3.999

9. Wafer Plating

The electroless nickel wafer plating process is utilized in large-scale production by Sensor Technology, Inc., and is considered to be one of the lowest cost metallization processes currently practised by the solar cell industry. It was found in this program, however, that the wafer plating process equipment, while considered to be very low-cost for the present and near term, was not sufficiently cost effective to meet the 1986 LSA cost goals.

The electroless nickel plating process equipment had two aspects which precluded this process from meeting the 1986 LSA cost goals. The first one involved an inadequate synchronization of tank sizes and process times thereby making an uninterrupted production line difficult to achieve. The second dealt with the heating of the plating solution. The electroless nickel plating bath utilized a direct immersion heater which consumed the nickel plating solution due to the deposition of nickel over the heating element. A new, synchronized, high throughput wafer plating system with an indirect heating feature was definitely needed in order to demonstrate that the 1986 LSA cost goals could be achieved.

Wafer plating process equipment was designed and constructed to circumvent the undesirable process aspects of our wafer plating system. A sketch of the electroless nickel wafer plating system is shown in Figure 9. The system has the capability of being fully automated. It has a wafer throughput capacity of 1800 wafers per hour for three to four inch diameter wafers and 3000 wafers per hour for two to two and one-half inch diameter wafers. The size of each tank was determined from the criterion of allowing standard wafer carriers of all sizes to be utilized. The etchant and primer tanks are small because their process times are faster than the other process steps. Four electroless nickel plating tanks with heating elements are included. The four tanks were needed due to the fact that the nickel plating solution consumption rate is large, the process time is long, and the time required to heat the solution up to 83 to 85^{o}C is relatively long (fifteen minutes). By utilizing four plating tanks, no interruption in production will occur as the result of solution preparation, since at least one tank will always be in an operational condition during the time period that another tank is being replenished.

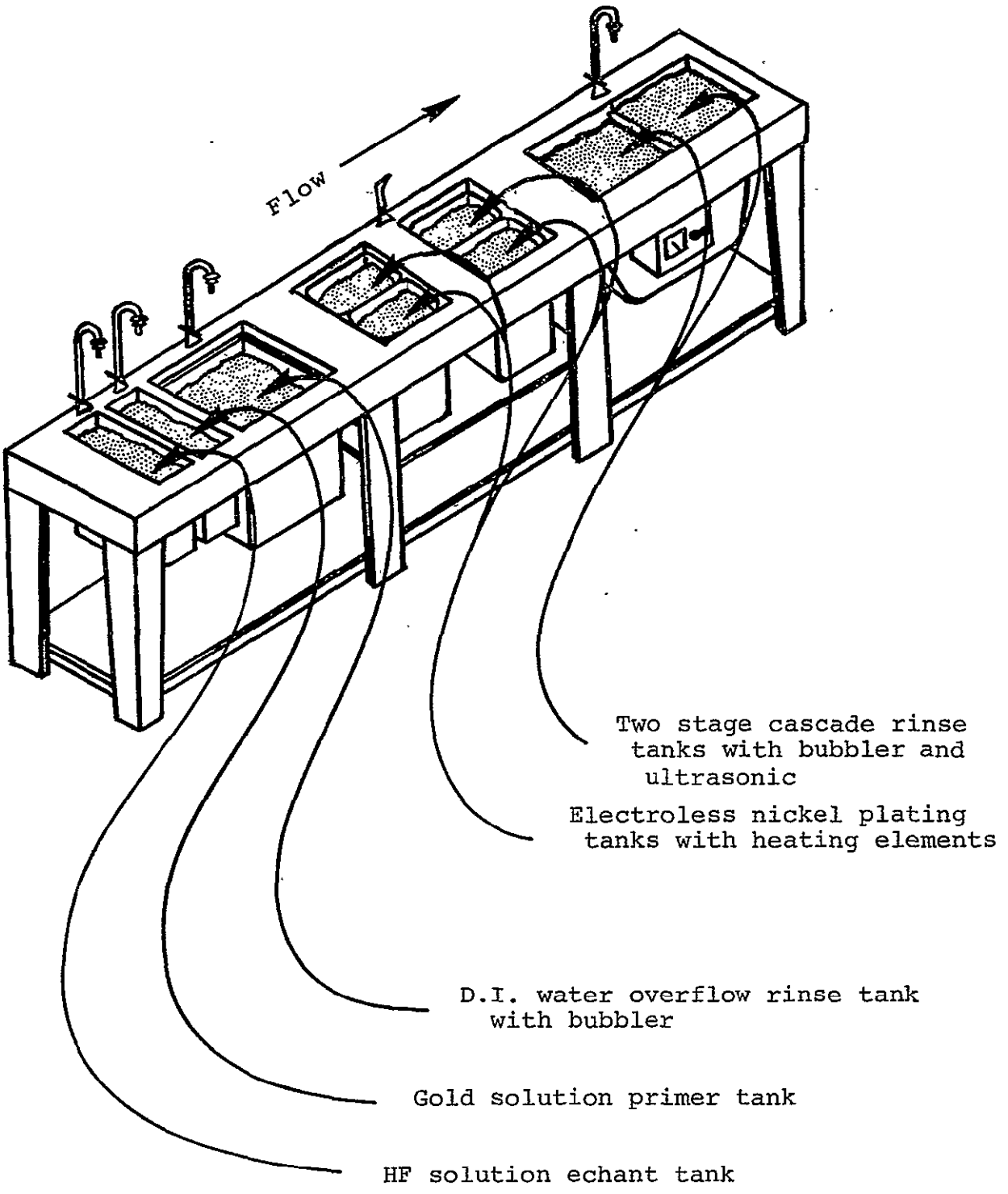


Figure 9. Sketch of electroless nickel wafer plating system.

Initial operation of the process begins when the wafers are placed into a hydrofluoric acid etchant tank for 30 seconds and then moved to the gold solution primer metal bath for 30 seconds. Next, the wafers are stored in the overflow rinse tank. After repetition of three cycles of this process, a total of six wafer carriers are collected at the overflow rinse tank. These six carriers are then placed onto a carrier basket which travels to the electroless nickel plating tanks where the wafers are processed for five minutes. The wafers are then moved into a two stage cascade rinse tank where they remain for ten minutes (five minutes in each tank).

An electroless nickel plating optimizaton study was initiated following the installation of the new wafer plating system. The major problem which had to be overcome in the optimization study was the reduction of the material consumption rate without causing a corresponding degradation in the plating performance capability. Three hundred 90 millimeter silicon wafers were processed in order to establish the feasibility of reducing the material consumption rate. A large portion of these 300 wafers was taken directly from Sensor Technology's solar cell production line.

The important findings resulting from this process study are listed as follows:

(1) The consumption rate of the gold solution was reduced by a factor of one-half.

(2) The nickel solution usage time was extended by a factor of four.

(3) The overall processing time was reduced by 20%.

(4) The plating uniformity due to the new system had reduced the variations in cell power output from 14.7% to 4.6%.

(5) The process yield was significantly increased. All 300 wafers were defect free.

The major contributing factor responsible for the improvements described above lies entirely with the use of the new, large sized bath with uniform solution and precise temperature control. A comparison among various characteristics of the new larger-sized bath and the formerly used bath will further illustrate this point. The new gold bath has an eight liter capacity, whereas the former bath had a gold solution capacity of only three liters. The new nickel plating bath functions by means of indirect heating of the walls, while the former nickel bath used a directly submerged heating element. Consequently, the solution temperature variation in the new bath was $\pm$ 2^{o}C, whereas the former

nickel bath had a $\pm$ 5°C temperature variation. The new nickel bath maintains precise temperature control and hence good solution uniformity. The former nickel bath had localized heat variations in the vicinity of the heater element. The localized heat variation of the former nickel bath was observed to cause breakdowns in the resist, since the resist could not withstand temperatures in excess of 85°C. In spite of the fact that the former nickel bath was maintained at 80°C, the average temperature at the wafer surface may have been higher due to poor convection of the solution. All of these facts make it apparent that the old nickel bath solution became quickly contaminated with resist, which in turn caused the usage time of the solution to be significantly reduced. In addition, a newly installed agitation system underneath the nickel bath proved to be very effective in maintaining the solution uniformity. An increase in bath temperature to 83°C did not lead to resist failure and the reduction in processing time from 5 to 4 minutes has not been found to sacrifice plating performance.

The new electroless nickel plating system which was designed, constructed and tested in this program has been shown to lead to a cost effective metallization process which meets the 1986 LSA goals. The SAMICS results show the cost of this wafer plating process to be 4.18 cents per peak watt in 1975 cents. The electroless nickel wafer plating system is, therefore, highly recommended for the 1986 LSA solar cell industry.

10. Solder Coating and Flux Removal

The two most widely used production line solder coating methods in the current semiconductor industry are solder dipping and wave soldering. The solder dipping method utilizes a single process cycle to solder coat one wafer at a time. The wave soldering method utilizes two process cycles; each cycle solder coats one side of a wafer at a time. The solder dipping method, while found to be more economical than the wave soldering method, was also found to have an insufficient throughput rate when compared to the 1986 LSA goals for solar cell production. A solder dipping method that replaces single wafer dipping with multiple wafer dipping was required.

A teflon carrier was fabricated and tests were performed for the purpose of establishing the solder coating characteristics of silicon solar cells processed by the multiple wafer dipping method. All studies were conducted in an existing 6" x 6" x 6" solder bath with 60/40 lead/tin solder.

The crucial parameters investigated in the experimental study were as follows:

(a) carrier design

(b) dipping direction

(c) wafer surface orientation

(d) pre-heat temperature

(e) cell temperature

The carrier design was dependent upon the size of the available solder pot. A teflon carrier was fabricated to hold ten 90 mm diameter silicon wafers. A wafer stop was added to prevent the wafers from floating out of the slots in the carrier during the dipping process. A ten inch handle was also added to assist in the manual dipping operation.

The carrier dipping direction was always vertical with respect to the solder pot. It was required that the wafers be in a vertical orientation when dipped to prevent breakage. It was also found to be necessary to shake the wafer carrier after dipping and place the solar cells in a horizontal position to prevent nonuniformity of the solder coatings. In the automated P.C.board industry an air knife edge is used to replace the manual technique discussed above to produce uniformly solder coated solar cells. This technique was used in the SAMICS analysis discussed in a later section of this report.

The operating temperature of the solder bath was found to be very important for multiple wafer dipping. A detailed discussion of the experiments performed will now be presented. At a temperature of 450^{o}F (232^{o}C) The solder coagulated on both the front and back surfaces of the solar cells which indicated that this temperature was too cold. When the temperature was raised to 500^{o}F, good solder coating uniformity was observed only after adopting the dipping procedure which involved the removal

of excess solder by shaking the vertically positioned solar cells and then cooling the cells in a horizontal position. When the dipping procedure was carried out at this temperature without utilizing this procedure, the solder coagulated in isolated segments of the back surface of the solar cell, which resulted in non-uniform solder coatings. For temperatures in excess of 600^{o}F, the cells had incurred excessive breakage due to thermal stresses. The thermal stresses could be relieved by preheating the wafers, a common technique used in the P.C.board industry, but this was not investigated in detail in this program. Consequently, it was concluded that the optimum temperature range providing solder coating uniformity for multiple wafer dipping was 500 to 550^{o}F with the restriction that the dipping procedure described above is utilized.

Three flux removal process methods were studied in this program and are listed as follows:

(1) D.I. water rinse tank

(2) D.I. water cascade rinse system with nitrogen bubbler

(3) D.I. water cascade rinse system with ultrasonic agitator

The first method was found to be unsuitable because flux residue was observed on the surface of the D.I. water which coated the solar cells when they were removed from the rinse water. The second method was also found to be ineffective in cleaning the flux off the solar cells. The third method which utilizes a D.I. water cascade rinse system with ultrasonic agitator was found to be an excellent method for flux removal. The process sequence consisted of a three stage D.I. water cascade rinse system with ultrasonic agitator. The process time was two minutes for each stage. The water temperature was 90^{o}C. The high D.I. water temperature will allow one to dry the wafers in a clean room environment and thus eliminate any heater or oven equipment which is typically used in present systems. The D.I. water cascade rinse with ultrasonic agitation in the first tank is a highly recommended flux removal process.

11. Cell Handling for Module Construction

Cell handling for module construction will require precision positioning techniques in addition to an approximate rate of 2 cells per second if the module construction line is to produce 7200 wafers per hour or 60 modules per hour in accordance with the 1986 production goals.

Several varieties of solar cell handling units are available from semiconductor industries and most of them are designed to fit a particular application. For example, the printing machine industry uses cassette to conveyor loading which requires a specialized cell positioning system.

A precision positioning system used throughout the semiconductor industry is the robot arm, which unfortunately operates at a slow rate. This rate is primarily dependent upon the number of degrees of freedom required to locate an object and usually exceeds 2 seconds/cycle.

An alternative cell positioning technique makes use of a hopper dispenser unit. This system has the advantage of being able to simultaneously dispense several cells, thereby permitting a choice of cycle times and/or production rates. However, the hopper dispenser unit is unable to deposit cells within a close enough proximity such that the gap between cells is approximately 50 mils. Since this method does not display the precision positioning capability characteristic of the robot arm, it was determined to be unsuitable for our requirements. Consequently, a conceptual design for a robot arm system with multiple pick-up heads was devised, which appears to hold promise in meeting 1986 production goals.

The module which is to be constructed by the robot arm system with multiple pick-up arms will contain six full cells and two half cells per row, with each alternating row maintaining the same sequential cell arrangement.

The conceptual drawing of the solar cell handling system is shown in Figure 10. Two robot arms will each simultaneously deposit the six full cells and two half cells which are placed in a pre-arranged pattern on their respective cell storage racks.

This system will deposit a total of 16 cells per cycle with good pattern reproducibility. The required cycle time will be six seconds and the conveyor will move by two rows during each cycle.

The technology for fabricating the robot arm system with multiple pick-up heads is well developed, and consequently, this robot arm system is recommended for use in the 1986 array automated assembly system.

12. Laser Trimming and Holing Automation

The utilization of a low-cost, fully automated laserscribe system which maintains a high volume through-put and large output yield, will be of central importance in achieving the 1986 LSA goals. Consequently, a study

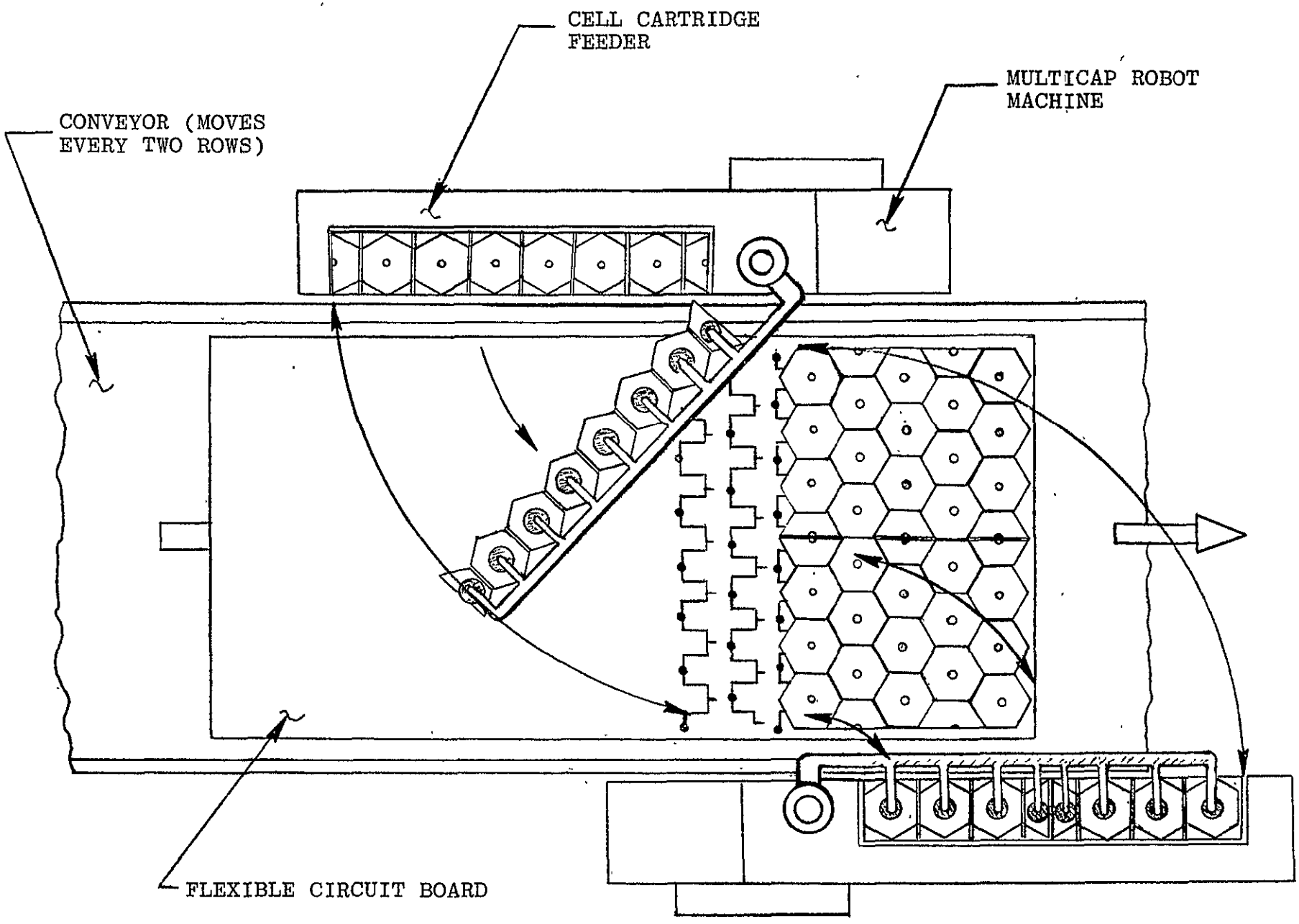


Figure 10. Conceptual drawing of cell handling system for automatic module assembly line.

was devised which set out to identify a system possessing the above mentioned features, with the capability of accepting a batch of wafers in the form of a multiple track conveyor. The system will receive wafers from the conveyor, orient and position the wafers, scribe and trepan the wafers, break along the hexagonal scribes and remove the trepanned plugs, and finally, reload the finished wafers onto the conveyor.

Two potentially automated systems capable of laserscribing silicon wafers to produce hexagonally shaped wafers with central holes were identified and reviewed in order to establish the output capability, maintainability, reliability, and economic characteristics of each system.

The first system considered was the parallel flow laserscribe system. It contains four dual beam lasers aligned as shown in Figure 11. Wafers are off-loaded from cassettes, aligned and loaded onto platens accepting eight wafers each. The loaded platen is moved to the X-Y table where it is keyed and locked in position under the laser beam. The table is programmed to scribe first the hexagon and then the central hole.

The platen containing the scribed and trepanned wafers is next moved to the cracker unit where the edges and the center hole materials are removed from all eight wafers at the same time. The

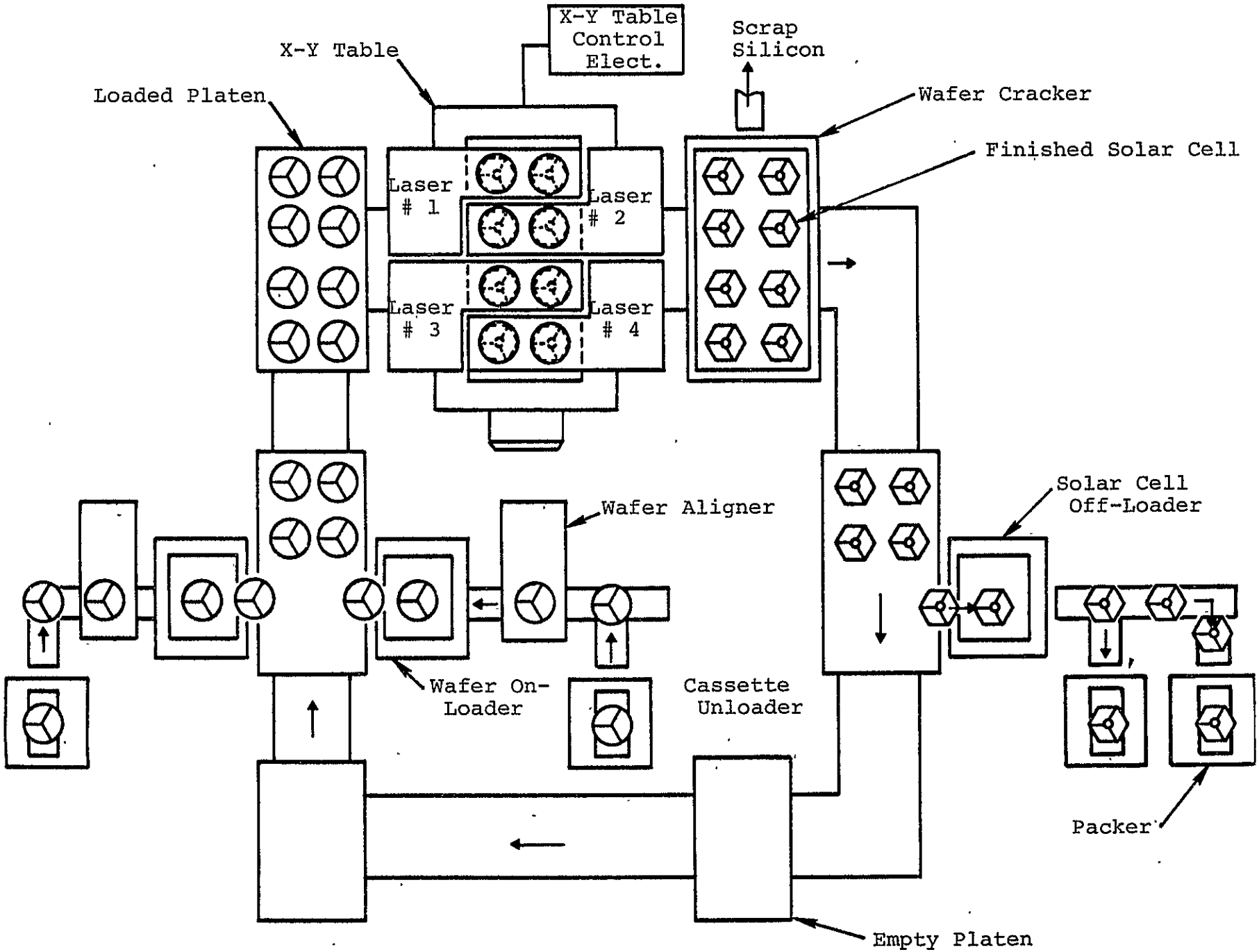


Figure 11. Parallel flow laserscribe system for 4800 wafers per hour.

scribed and trepanned wafers are carried to the packer to be off-loaded from the platen and loaded into cassettes. The scrap is collected and returned by conveyor to the recycling station. Note that the various operations - loading/aligning, scribing/holing, cracking, and packing operations - are simultaneous steps timed so that each operation is accomplished in the same time interval. The time interval between wafer sets depends on scribing time and the time required between moves.

A detailed cost breakdown for the parallel flow laserscribing system with throughput rate of 4800 wafers per hour is presented in Table 7. The total cost per peak watt for the parallel flow laser-scribing system in 1986 and 1975 cents respectively are 1.788 cents and 0.932 cents.

The second system considered was the serial flow laserscribe system. This unit is comprised of 2 loaders, 2 aligners, 3 dual beam lasers, 4 trepanning (holing) lasers, 4 wafer crackers and a moving surface onto which are mounted, at evenly spaced intervals, wafer holding chucks as shown in Figure 12. One wafer at a time is removed from its storage container and transferred onto a holding chuck which carries the wafer through the scribing process. The wafer is moved along by conveyor to the wafer aligner where the wafer grid lines are oriented in preparation

Table 7. Process costs for parallel flow laserscribe system in cents per peak watt

	1986 cents	1975 cents
Equipment	0.5850	0.3049
Floor space	0.0612	0.0319
Labor	0.8449	0.4400
Materials	0.0192	0.0100
Utilities	0.2783	0.1451
TOTAL	1.788	0.932

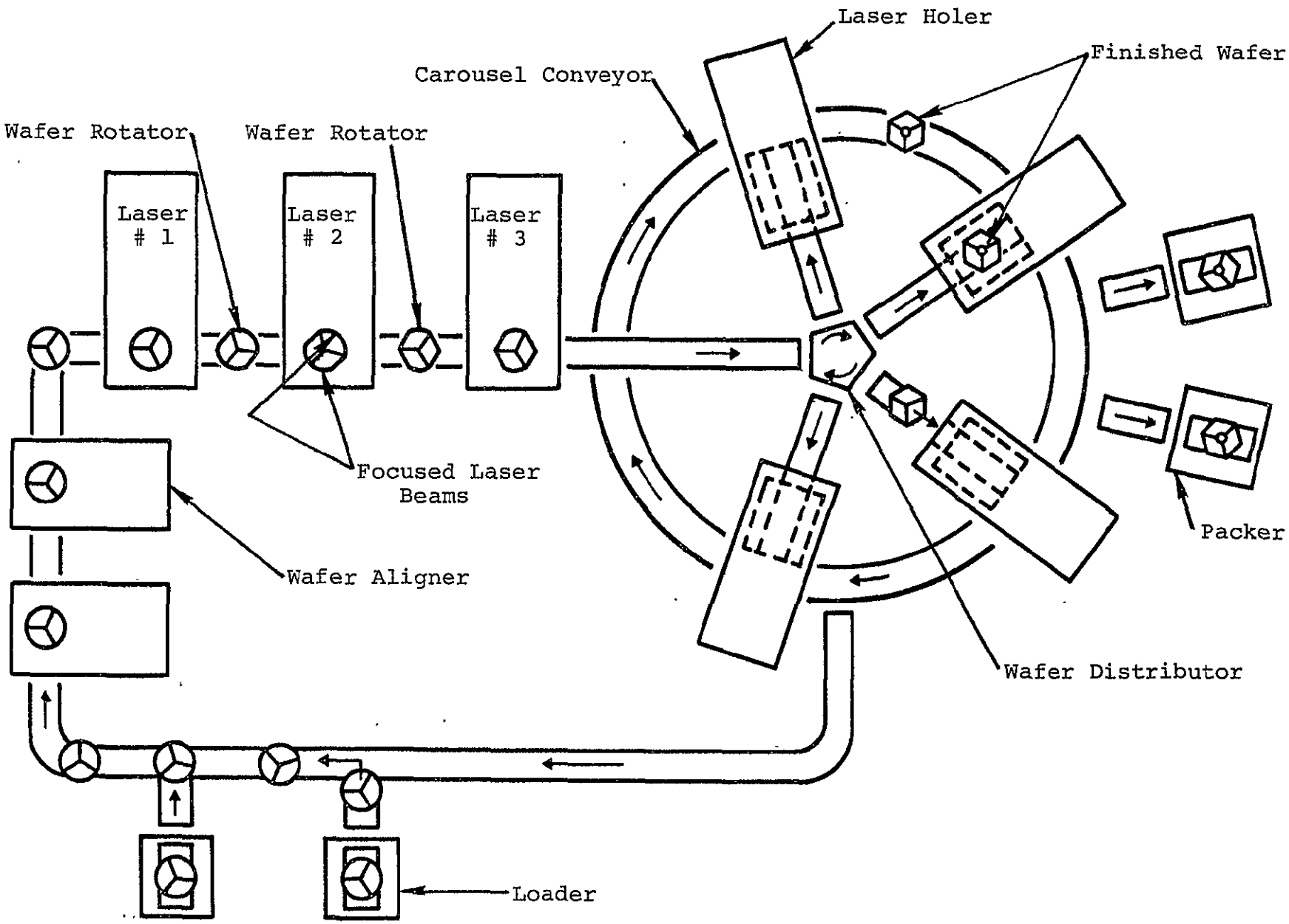


Figure 12. Serial Flow Laserscribe System for 7200 Wafers Per Hour.

for scribing. The wafer is then passed under a dual beam laser whose beams are aligned and focused so that two parallel sides of a hexagon are simultaneously scribed. The wafer is next moved at constant speed to the chuck rotator which is indexed to turn the wafer 60^{o}, and it will then be transferred to laser number 2 where the second pair of parallel sides is scribed. The partly scribed wafer is again rotated 60^{o} and the last pair of parallel sides is scribed by laser number 3. The hexagon scribed wafer will be offloaded from the conveyor and then distributed to the trepanning (holing) scriber/cracker units. Since it takes four times as long to produce holes as to scribe the hexagon, four trepanner/cracker units are needed for each hexagon scriber unit.

The finished wafers are finally off-loaded from the trepanner/cracker and loaded onto the carousel conveyor which carries them to the packer where the scribed wafers are returned to storage containers. The empty chucks are transferred to the return conveyor and to the loader to receive the next wafer. The scrap silicon, meanwhile, is collected and returned to the recycling station.

A detailed cost breakdown for the serial flow laserscribing system with a throughput rate of 7200 wafers per hour, is presented in Table 8. The

Table 8. Process costs for serial flow laserscribe system in cents per peak watt

	1986 cents	1975 cents
Equipment	.5179	0.2700
Floor Space	.0575	0.0300
Labor	.6713	0.3500
Materials	.0077	0.004
Utilities	.2359	0.1230
TOTAL	1.4903	0.7770

total costs per peak watt for the serial flow laser-scribing system in 1986 and 1975 cents are 1.4903 cents and 0.777 cents, respectively.

Upon comparison of the process costs of the two laserscribing systems in Table 7 and Table 8, it is evident that the serial flow laserscribing system is more cost effective than the parallel flow system. The critical cost factors for the serial flow system lie with the equipment and labor costs. On the basis of the analysis presented in this section, it can be concluded that the serial flow laserscribing system displays the characteristics which are essential for achieving the goals of the 1986 Low-Cost Solar Array Program.

13. Cell and Module Test and Data Storage

A computerized solar cell and module test and data storage system was designed and fabricated to perform two important functions in the array automated assembly task. The first function is to store and analyze relevant solar cell and module electrical performance data. This will serve to facilitate statistical analysis and quality control for all aspects of solar cell and module fabrication. The second function of the computerized system is to mechanically group solar cells and modules into predesignated categories on the basis of their peak power output. The benefits of this feature are twofold. One benefit is that solar cells can be grouped to optimize module performance. Another benefit is that mechanical grouping will aid in eliminating rejected solar cells and modules without extensive time utilization, such as, if this task was performed by manual inspection. The following discussion will focus on the function of storing and analyzing solar cell and module electrical performance data.

The solar cell and module test and data storage system required the following components:

(1) Pulsed xenon solar simulator to test at 100 mw/cm^2 and at 28^{o}C.

(2) Electrical performance data acquisition system.

(3) Microprocessor with proper input, output and interface hardware.

(4) Software program and floppy disk storage.

(5) Mechanical actuator and conveyor system (not included in this study).

In order to acquire a microprocessor unit compatible with our requirements, literature pertaining to the microprocessing equipment currently available in today's market was obtained. This literature was thoroughly reviewed and the Motorola M6800 system was subsequently selected. The Motorola M6800 microprocessor development system integrates the CRT display/keyboard with the mainframe of the central processing unit and thus requires no special interfacing. All remaining system components were designed and fabricated.

Following the design and fabrication of the microprocessor hardware, the required software was devised. A simplified flowchart representative of the actual computer program is presented in Figure 13. The object of the main program in this flowchart is to group solar cells in accordance with input data supplied by the programmer. The actual grouping operation is performed by three subroutines within the main program. The first subroutine, shown in Figure 13A, measures and stores V_{oc}. The second subroutine shown in Figure 13B measures and stores I_{sc}. The third subroutine shown in Figure 13C, utilizes a numerical analysis technique to group solar cells on the basis of their peak power output.

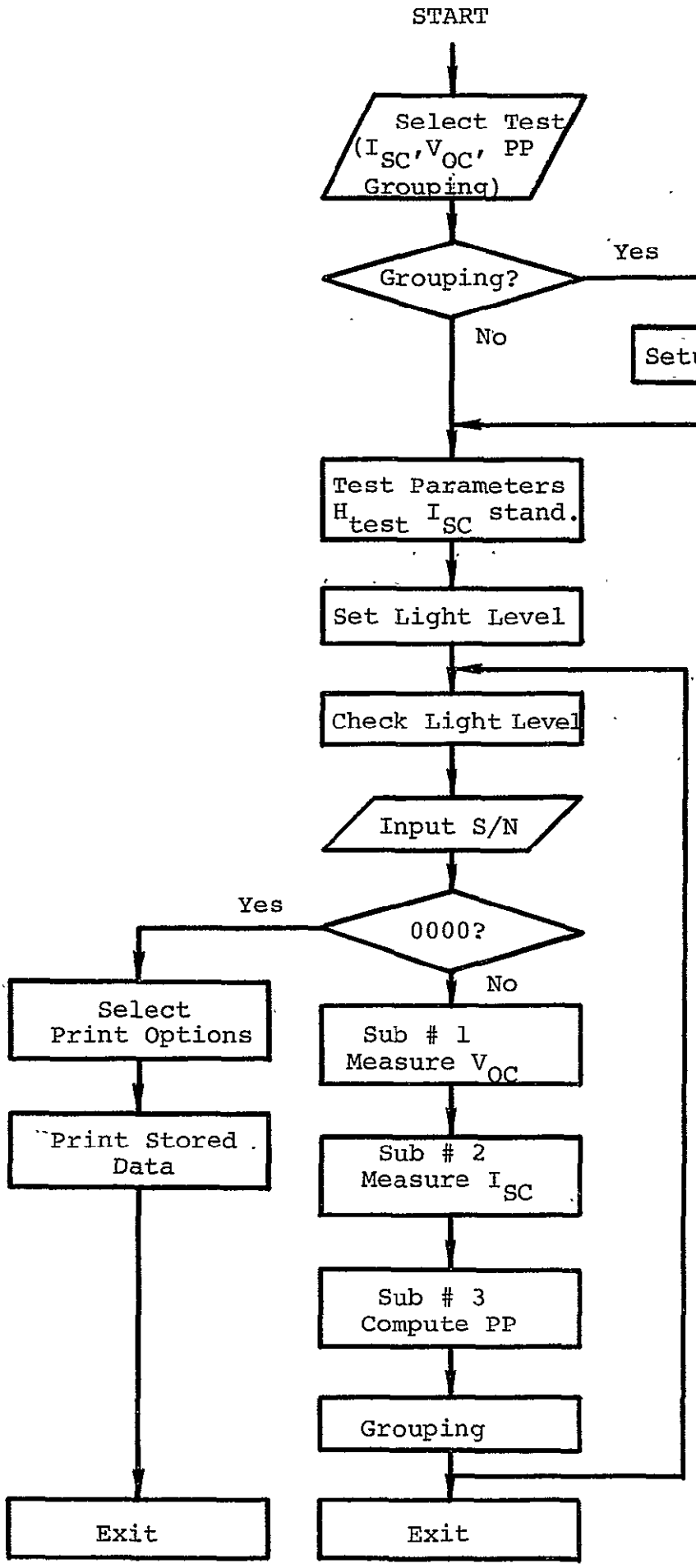


Figure 13. Flow chart of solar cell and modu test data acquisition and storage system. Solar cells are groupe in accordance with inpu data supplied by the programmer. Voc, Isc and peak power are determined respectivel by three subroutines. Data is stored and is available for print out.

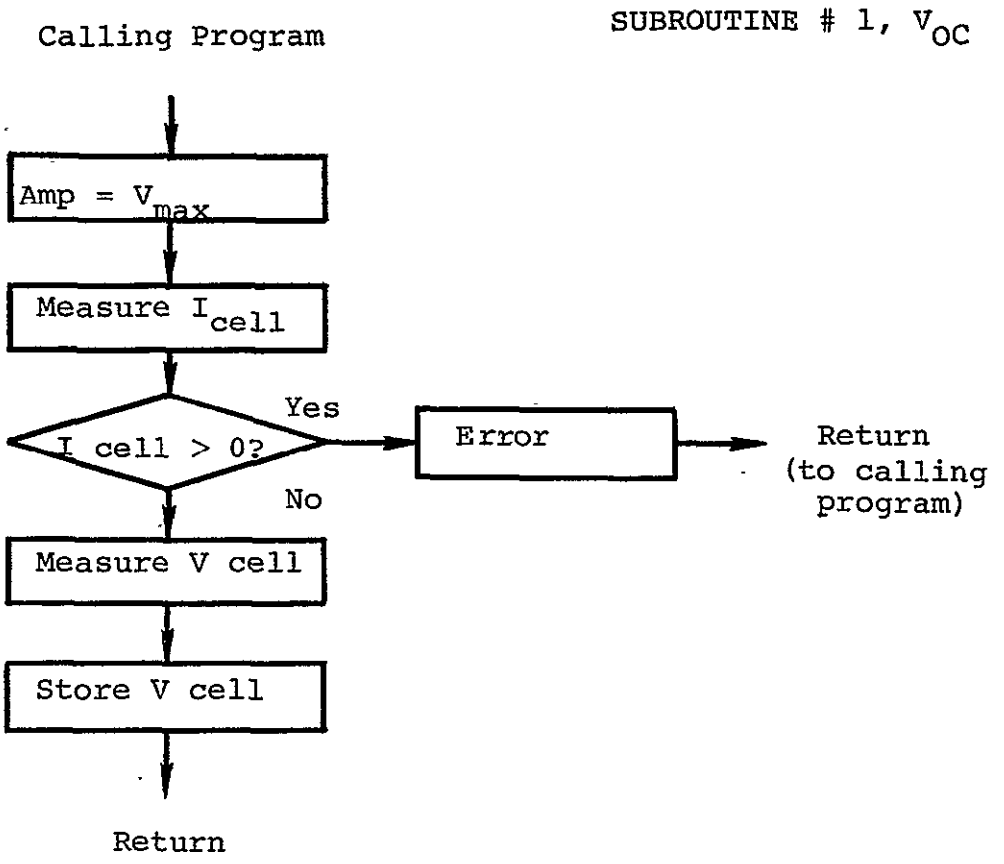


Figure 13A. Flow chart of subroutine number one for measuring open circuit voltage of solar cells or module.

Note: Amp V_{in} is set to a maximum. This effectively discounts the unit under test from the load so that V_{oc} may be measured. I_{cell} is checked first and if it is greater than zero then an error occurs because Voc is higher than what the equipment can measure.

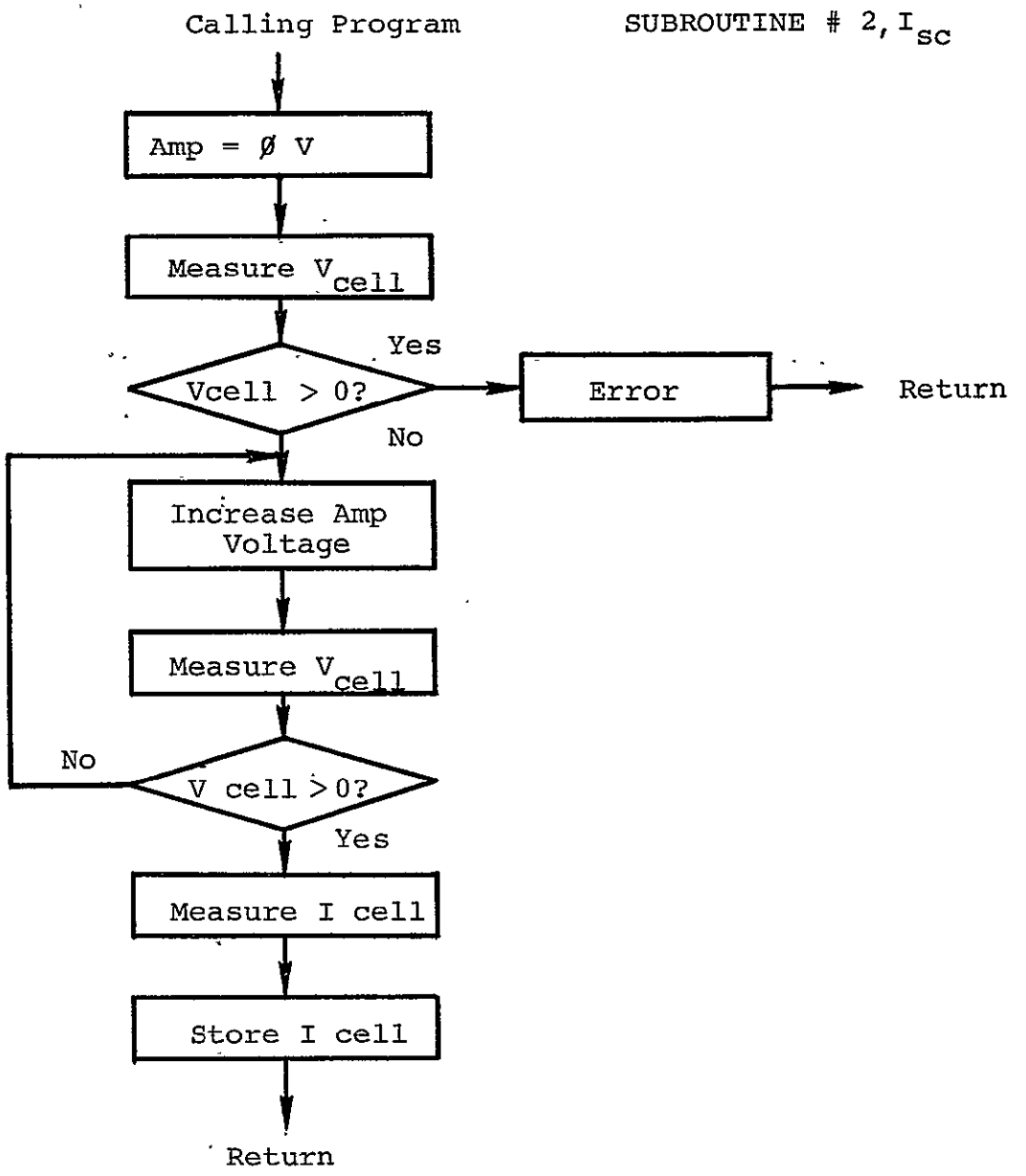


Figure 13 B. Flow chart of subroutine number two to measure short circuit current of solar cell or module.

Note: Amp Vin set to Ø V: If V cell is greater than zero then equipment is unable to measure Isc. Amp Vin is increased until Vcell is greater than zero. I cell is then measured and stored.

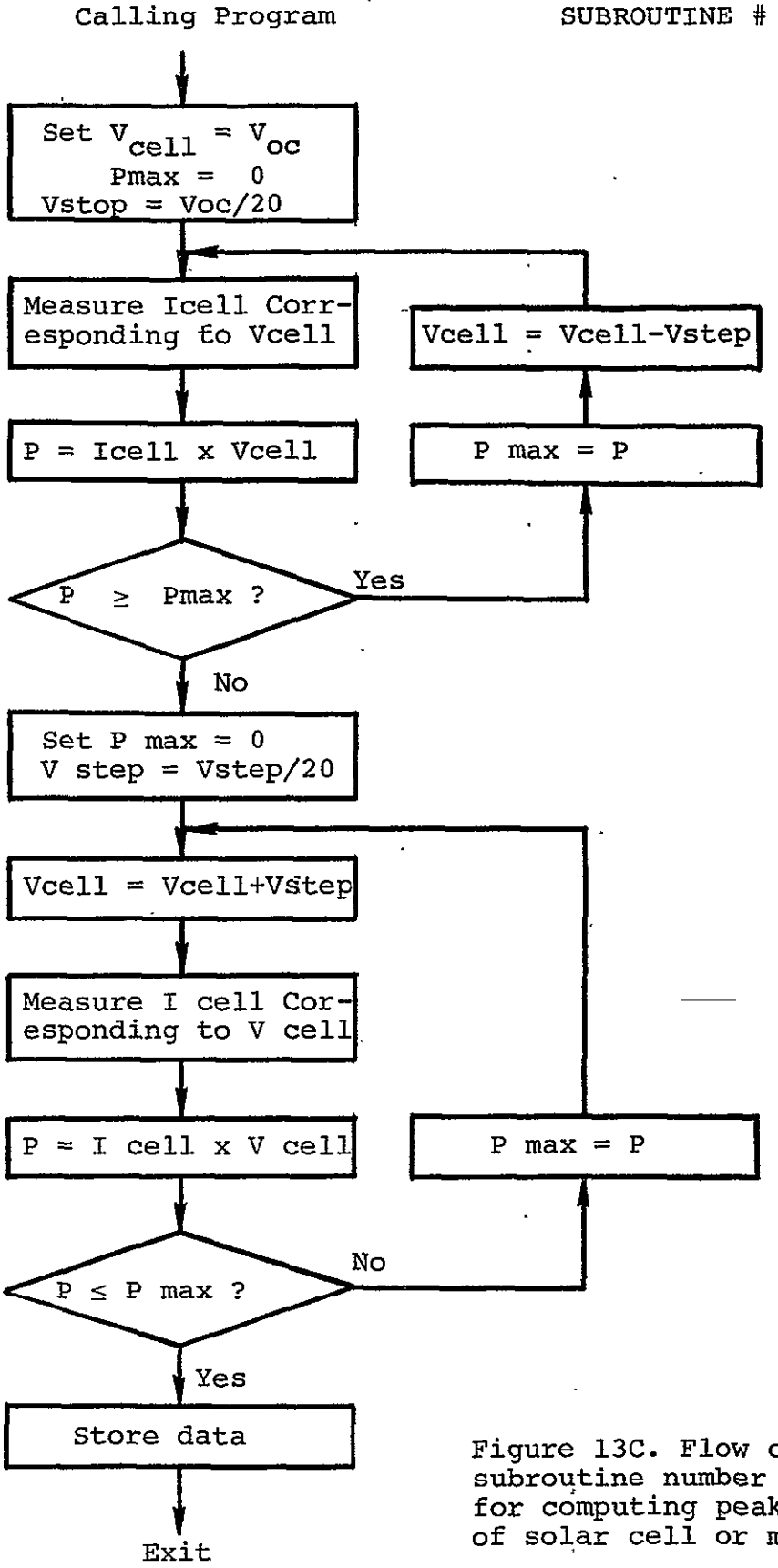


Figure 13C. Flow chart of subroutine number three for computing peak power of solar cell or module.

The criteria utilized in the grouping operation are as follows:

(1) Current at maximum power point

(2) Voltage at maximum power point

(3) Power at maximum power point

In practice, the majority of the solar cells which comprise a module is interconnected in series, so that each series connected solar cell will provide an identical current output. Since cell groups based upon current at maximum power are the most plausible grouping criterion in this case, the microprocessor was programmed to group the solar cells and modules accordingly.

The solar cell and module test and data storage system was tested to establish its data analysis and grouping performance capability. The verification of the grouping operation proceeded in four stages.

The first stage involved the grouping of solar cells with premeasured electrical performance characteristics. Ten solar cells from three separate groups of 2.15 inch diameter production solar cells were selected and mixed with two groups of rejected solar cells. A total number of fifteen solar cells was selected for test. The solar cells were identified

by a four digit serial number. The first digit indicates the premeasured electrical performance group (1 indicates the good solar cells and 5 indicates the rejected solar cells) and the fourth or last digit indicates the cell number used in a particular group. For example, 2003 indicates the second group, third solar cell. The solar cell data acquisition and storage system was programmed to group the solar cells based on 10 ma current increments from 460 ma to 530 ma at peak power. The current groups were chosen by the programmer and were part of the input data prior to the tests. Up to one hundred groups can be selected. The selected parameters to be measured were: short circuit current, I(sc), open circuit voltage, V(oc), peak power, and grouping. The tests were performed. The data were stored. The results were printed out and are shown in Table 9. A one-to-one correspondence exists between the two grouping methods which is indicative of the success of the computerized grouping operation.

The second stage checked the system capability to detect a wide range of solar cell current variations. The results of this performance verification test are presented in Table 10 which was generated by shadowing a solar cell to varying degrees. As is apparent from the table, the computerized system is able to detect a wide range in solar cell current variations.

Table 9. Solar cell data acquisition and storage system printout. The solar cells are grouped according to selected current increments at peak power and at a light intensity of 100 mW/cm^2, Xenon.

TEST LIGHT LEVEL (MW/CM^) 100.0
ABSOLUTE LIGHT LEVEL (MW/CM^) 111.5

SELECTED PARAMETERS TO BE MEASURED: I(SC) V(OC) PEAK POWER GROUPING

GROUP	MIN I(P) MA	MAX I(P) MA
00	0000	0460
01	0460	0470
02	0470	0480
03	0480	0490
04	0490	0500
05	0500	0510
06	0510	0520
07	0520	0530
08	0530	9999

S#	V(OC) MV	I(SC) MA	P(P) MW	V(P) MV	I(P) MA	GRP
4002	0532	0568	0180	0427	0422	00
3004	0537	0573	0222	0427	0522	07
3003	0537	0585	0221	0439	0505	05
5002	0537	0576	0201	0446	0451	00
5001	0527	0583	0200	0446	0449	00
2001	0537	0571	0232	0446	0522	07
5003	0515	0549	0128	0400	0322	00
3002	0539	0576	0227	0446	0510	05
2004	0541	0571	0233	0446	0524	07
1001	0544	0573	0239	0458	0522	07
2003	0537	0583	0235	0446	0527	07
3001	0559	0551	0236	0466	0507	05
5004	0505	0524	0097	0332	0295	00
3005	0544	0576	0221	0454	0488	03
1002	0534	0581	0238	0451	0529	07
4002	0532	0568	0180	0427	0422	00
0000						

C-2

Table 10. Solar cell data acquisition and storage system printout. The system capability to detect a wide range of solar cell current variations is demonstrated by shadowing a solar cell to varying degrees.

TEST LIGHT LEVEL (MW/CM^) 100.0
ABSOLUTE LIGHT LEVEL (MW/CM^) 104.4

SELECTED PARAMETERS TO BE MEASURED: I(SC) V(OC) PEAK POWER GROUPING

GROUP	MIN I(P) MA	MAX I(P) MA
00	0000	0100
01	0100	0200
02	0200	0300
03	0300	0400
04	0400	0500
05	0500	9999

S#	V(OC) MV	I(SC) MA	P(P) MW	V(P) MV	I(P) MA	GRP
9999	0524	0375	0095	0295	0324	03
9999	0527	0378	0095	0295	0324	03
9999	0524	0375	0095	0295	0324	03
9999	0524	0378	0095	0295	0324	03
9999	0524	0375	0095	0307	0312	03
1111	0522	0302	0082	0295	0278	02
1111	0522	0302	0082	0295	0278	02
1111	0522	0302	0082	0295	0278	02
1111	0522	0302	0082	0295	0278	02
2222	0500	0136	0042	0358	0119	01
2222	0500	0136	0042	0358	0119	01
2222	0502	0136	0042	0358	0119	01
2222	0502	0136	0042	0358	0119	01
3333	0507	0166	0052	0358	0146	01
3333	0507	0163	0050	0334	0151	01
3333	0507	0163	0050	0334	0151	01
4444	0520	0246	0072	0327	0222	02
4444	0520	0246	0072	0327	0222	02
4444	0520	0246	0072	0327	0222	02
5555	0529	0393	0098	0300	0329	03
5555	0529	0393	0098	0314	0314	03
5555	0529	0392	0098	0300	0329	03
9999	0529	0375	0096	0295	0327	03
9999	0529	0375	0096	0295	0327	03
9999	0529	0375	0096	0307	0314	03
0000						

The third stage involved the grouping of modules with premeasured electrical performance characteristics. Three solar cell modules from two different groups were selected. The results of this performance verification test are presented in Table 11, where it can be seen that the data acquisition and storage system grouped the modules into two categories which agreed with the premeasured electrical performance tests.

The fourth stage proceeded analogously to the second stage, however, in this case the system capability to detect a wide range of solar cell module current variations was investigated. The results of this performance verification test are presented in Table 12 which was generated by shadowing one module to varying degrees. As is apparent from the table, the computerized system is able to detect a wide range of solar cell module current variations.

The grouping operation has thus been shown to be highly successful in all respects. The first conclusion which may be drawn from the experimental data is the existence of a one-to-one correspondence between the currently utilized manual grouping method and the computerized grouping method. It can also be concluded that the computerized solar cell and module test and data storage system is capable of easily detecting a wide range of solar cell and module

Table 11. Solar cell module data acquisition and storage system printout. The modules are grouped according to selected current increments at peak power and at a light intensity of 100 mW/cm^2, Xenon.

TEST LIGHT LEVEL (MW/CM²) 100.0
ABSOLUTE LIGHT LEVEL (MW/CM²) 112.5

SELECTED PARAMETERS TO BE MEASURED: I(SC), V(OC) PEAK POWER GROUPING

GROUP	MIN I(P) MA	MAX I(P) MA
00	0000	2300
01	2300	2400
02	2400	2500
03	2500	5000
04	5000	9999

S#	V(OC) MV	I(SC) MA	P(P) MW	V(P) MV	I(P) MA	GRP
7405	4457	2651	7237	3137	2307	01
7386	3964	2756	6999	2902	2412	02
7407	3952	2682	7498	3100	2419	02
0000						

Table 12. Solar cell module data acquisition and storage system printout. The system capability to detect a wide range of module current variations is demonstrated by shadowing the module to varying degrees.

TEST LIGHT LEVEL (MW/CM²) 100.0
ABSOLUTE LIGHT LEVEL (MW/CM²) 102.0

SELECTED PARAMETERS TO BE MEASURED: I(SC) V(OC) PEAK POWER GROUPING

GROUP	MIN I(P) MA	MAX I(P) MA
00	0000	1500
01	1500	1750
02	1750	2000
03	2000	2250
04	2250	2500
05	2500	9999

S#	V(OC) MV	I(SC) MA	P(P) MW	V(P) MV	I(P) MA	GRP
1001	4497	2724	7426	3359	2211	03
1002	4497	2604	7414	3398	2182	03
1003	4492	2492	7314	3410	2145	03
1004	4494	2551	7395	3405	2172	03
1005	4492	2451	7427	3393	2189	03
1006	4489	2517	7419	3374	2199	03
1007	4497	2973	8955	3359	2666	05
1008	4492	2770	8467	3417	2478	04
1009	4487	2702	7885	3386	2329	04
1010	4450	1833	4398	3420	1286	00
0000						

current variations. An assessment of the far-reaching potential of the computerized solar cell and module test and data storage system has led to the expectation that it will immensely simplify the performance of statistical analysis and quality assurance in all areas of solar cell and module fabrication.

14. Module Construction Study

An indepth module construction study based on a unique solar cell central hole interconnection concept was performed in this task. The investigation was carried out in three distinct stages. The first stage dealt with the solar cell conceptual design, and involved grid pattern optimization and theoretical fractional power loss predictions for a hexagonal solar cell with central hole. The second stage dealt with the module conceptual design, and encompassed the area of solar cell interconnection by means of a flexible printed circuit sheet. The final stage of this investigation consisted of a module fabrication study, and required an analysis of solar cell dispensing techniques, tab pop-up, and the interconnection soldering operation. Each of the above mentioned areas will be discussed in detail, in the following sections.

a) Solar Cell Conceptual Design

A hexagonal solar cell with central hole was selected for usage in the proposed module. The most pronounced difference between the new solar cell design and the solar cell currently produced by Sensor

Technology is respectively, the new central hole current collection method as opposed to the present edge current collection method.

The new solar cell was fabricated from 3.54 inch (90 mm) diameter silicon wafers. Hexagonally shaped wafers with point to point diameters of 3.54 inches and central hole diameters of .150 inches were formed by means of an automated laserscribe. The solar cell gridline pattern was designed to minimize the combined effect of the shadowing and ohmic power loss components. The ohmic power loss encompasses both the diffusion layer ohmic loss and metal gridline ohmic loss.

The gridline pattern optimization was calculated according to the following specifications:

(1) The gridline width was fixed at 7 mils which is the technological limit imposed by the thick film printing equipment.

(2) Each gridline was separated by equal areas which results in an equal current flow into each gridline.

(3) The trunk-line was extended through the center of each triangular area which permits the cell to be cut through any diagonal thus preparing the cell for placement in the module.

(4) The approximate values of the resistances used in the various power loss calculations are as follows:

Diffusion layer resistance:	30 Ω/□
Gridline sheet resistance:	0.004 Ω/□
Trunkline sheet resistance:	0.001 Ω/□

(5) Current density was assumed to be 32.5 mA/cm^2 and the voltage at the maximum load was assumed to be 0.5 volts.

Upon utilizing the above assumptions, it was found that the optimum number of gridlines should be seven for the hexagonal solar cell with central hole. The optimized grid-line pattern is presented in Figures 14 and 15.

The calculated results for the fractional power loss of each element of the hexagonal solar cell with central hole are presented in Table 13. It is evident from the table that the largest contributing element to the total fractional power loss resides with the gridline shadowing power loss. Theoretical analysis shows that the fractional power loss can be improved by as much as two to three percent by reducing the width of the gridlines. This is due to the fact that the ohmic loss for our solar cell gridlines is very small. The solar cell gridlines, unfortunately, can

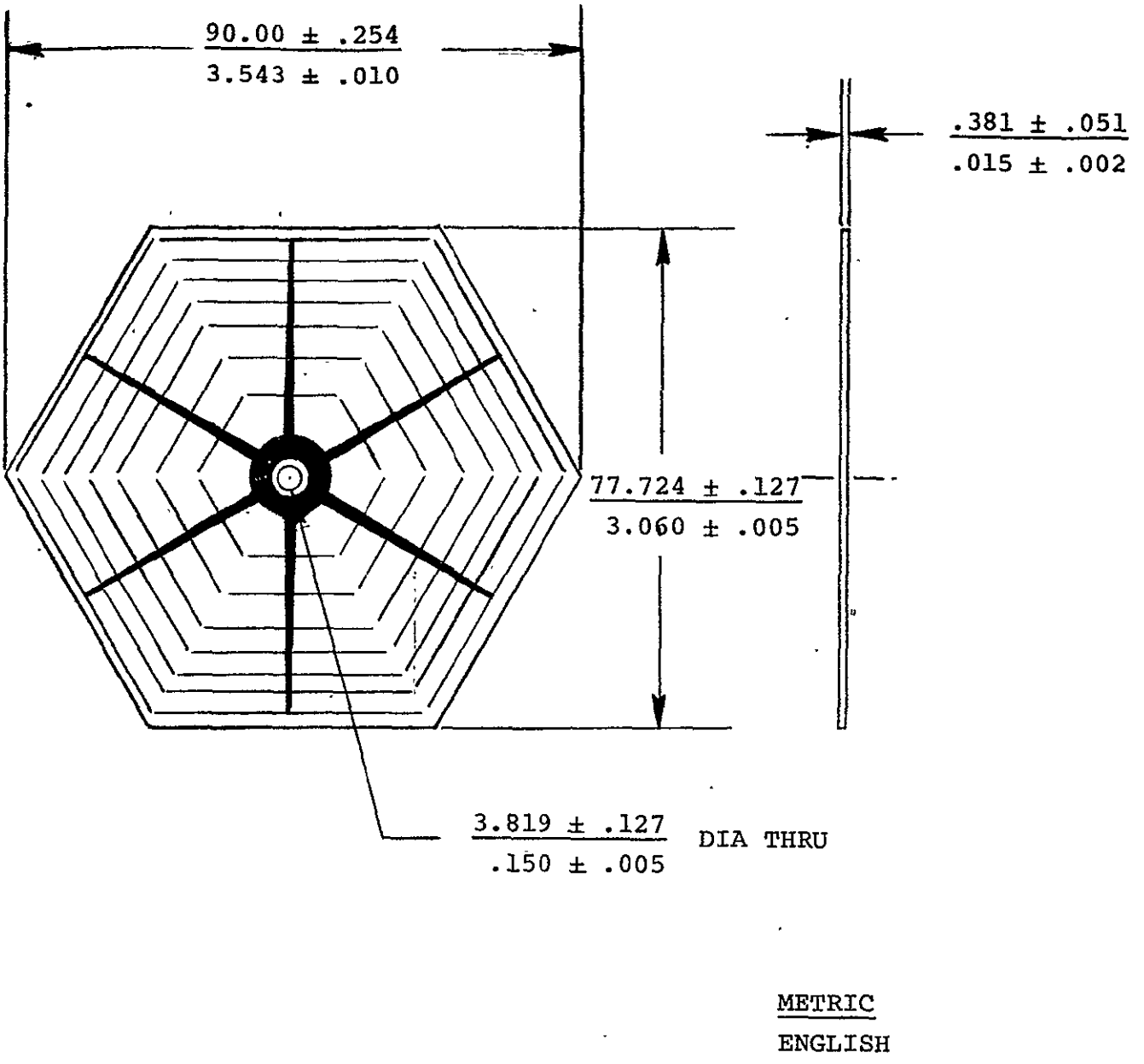


Figure 14. Hexagonal solar cell with central hole.

All Widths of Gridlines = 0.007

Trunk Width = 0.010 to 0.040

Number of Gridlines = 7

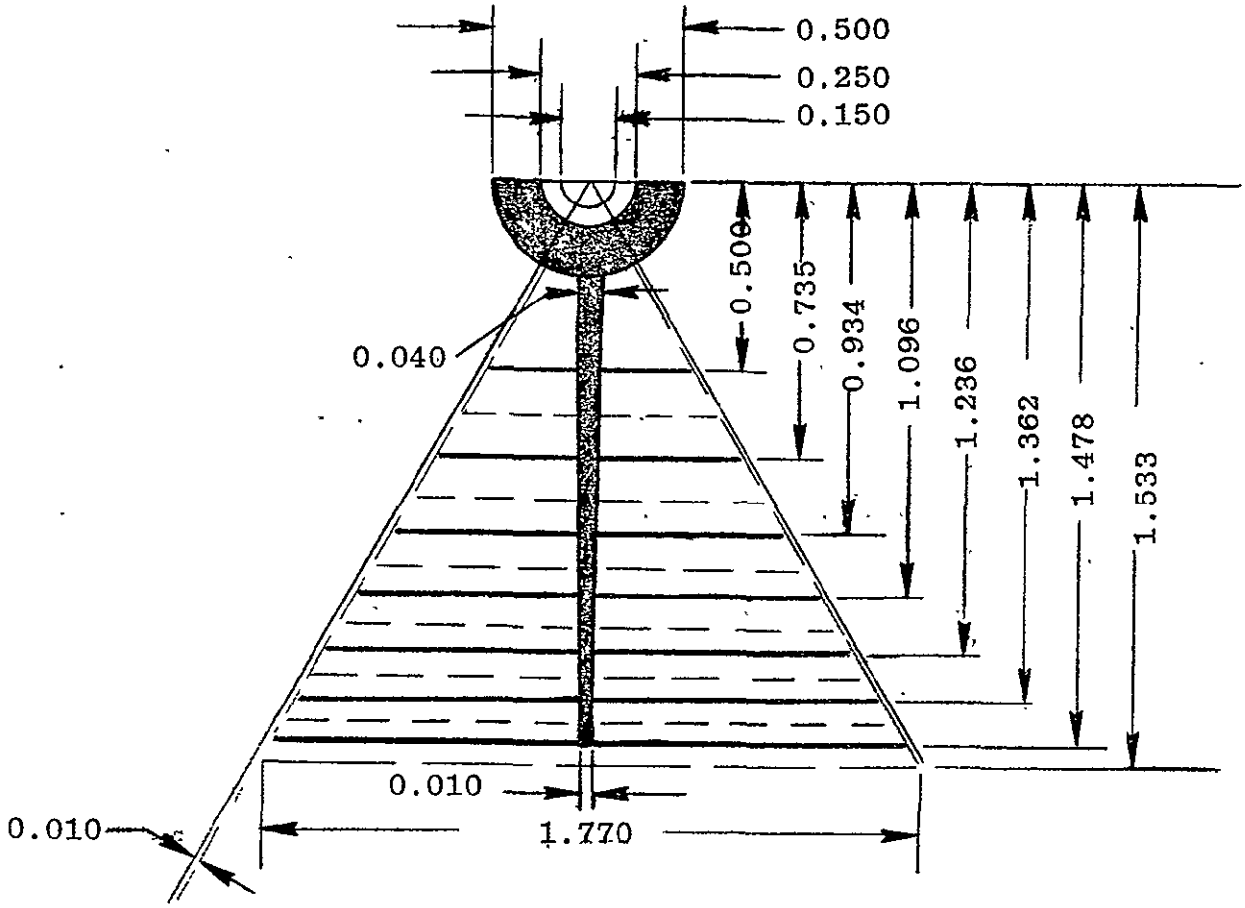


Figure 15. Hexagonal solar cell grid pattern with central hole.

Table 13. Fractional power loss of each element of the hexagonal solar cell with central hole.

Element	Shadowing Loss (%)	Ohmic Loss (%)
Diffusion layer	--	2.761
Gridline	4.374	0.402
Trunk line	2.364	2.205
Center "O" ring	1.810	1.610
Total	8.548	6.978
Total fractional power loss = 15.526%		

only be reduced to a certain width which is subject to the constraints imposed by the technological limits of the current thick film printing equipment.

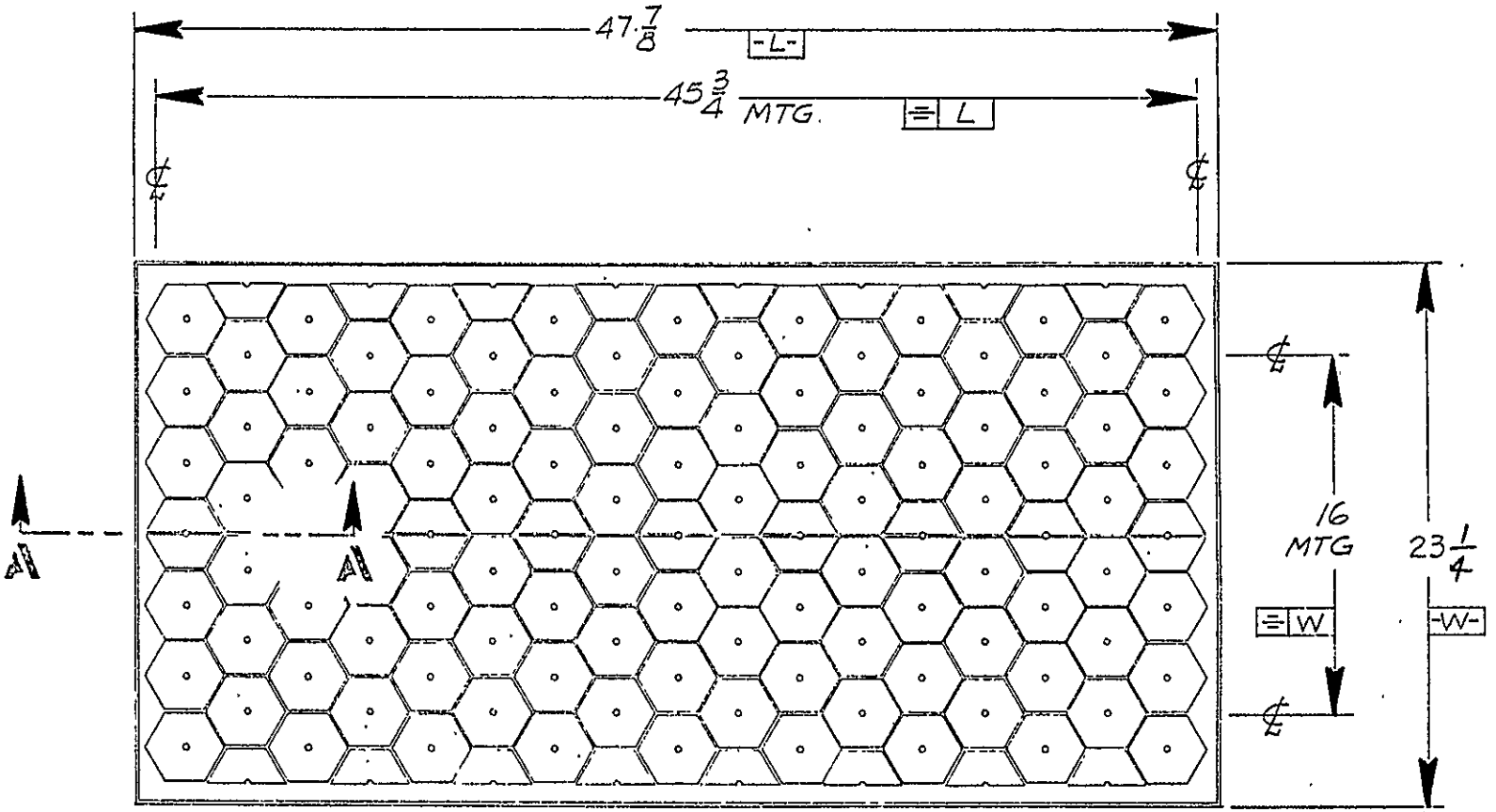
A second alternative is to decrease the number of gridlines on the solar cell. However, by decreasing the number of gridlines from, for example, seven to six, the total fractional power loss increased from 14.36% to 14.90%. This fractional power loss occured because the shadow reduction due to less gridlines was not sufficient enough to compensate for the increase in ohmic power loss. Calculations also show that the number of gridlines and the gridline patterns are relatively insensitive for an optimized amount of shadowing on a solar cell.

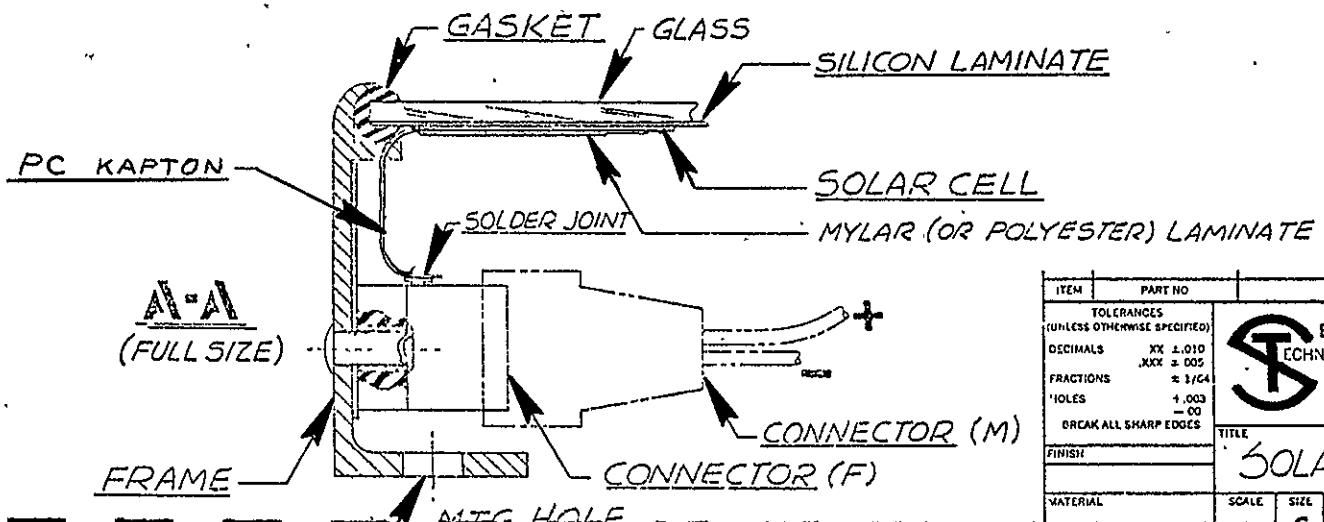
The final solar cell design feature considered in this study was the "O" ring contact line which exhibited a fairly large shadowing loss and a small ohmic power loss. This situation cannot be easily rectified since tab soldering requires a finite area.

b) Module Conceptual Design

The module conceptual design for 1986 consists of 119 hexagonal solar cells. The packing arrangement of 102 full solar cells and 34 half solar cells in the two by four foot module is exemplified in Figure 16, where the spacing between the cells is 0.05 inches,

DATE	LTR	REVISION	DR	CHK	APP





NOTES: UNLESS OTHERWISE SPECIFIED

ITEM	PART NO	DESCRIPTION	REQ

TOLERANCES (UNLESS OTHERWISE SPECIFIED)
DECIMALS XX ±.010, .XXX ± .005
FRACTIONS ± 1/64
HOLES +.003 −.00
BREAK ALL SHARP EDGES
FINISH
MATERIAL

SENSOR TECHNOLOGY, Inc
CHATSWORTH • CA. 91311

DR
CHK
APP
JOB NO JPL RFP ED-2-8571

TITLE
SOLAR CELL MODULE

SCALE | SIZE C | DWG NO FIG 16. | SHEET —OF— | REV

the solar cell area is 968.65 in^2, the solar cell nesting area is 1030.58 in^2 and the module area is 1113.09 in^2. The module packing efficiency was determined to be 87% and the solar cell nesting efficiency was found to be 94%. In order to minimize the potential electrical power loss due to solar cell failure a group of three full hexagonal solar cells and one half solar cell shall be connected in parallel and thirty-four groups shall be connected in series. The encapsulated solar cell efficiency shall be 14.5% with a peak power output of 0.76 watts. The expected module electrical performance at 100 mW/cm^2 and at 28°C shall be as follows: 90 watts at peak power, 17.14 volts at peak power, and 5.25 amps at peak power.

All solar cell interconnections in the module conceptual design shall be achieved by means of a flexible printed circuit sheet. The flexible printed circuit sheet conceptual design is shown in Figure 17. Two ounces of copper per square foot is a good guide for typical P.C.sheets. The copper would be about 3.0 mils thick. This thickness is variable and could be adjusted to specification. The sheet configuration could use either a single or double clad design. A

DATE	LTR	REVISION	DR	CHK	APP

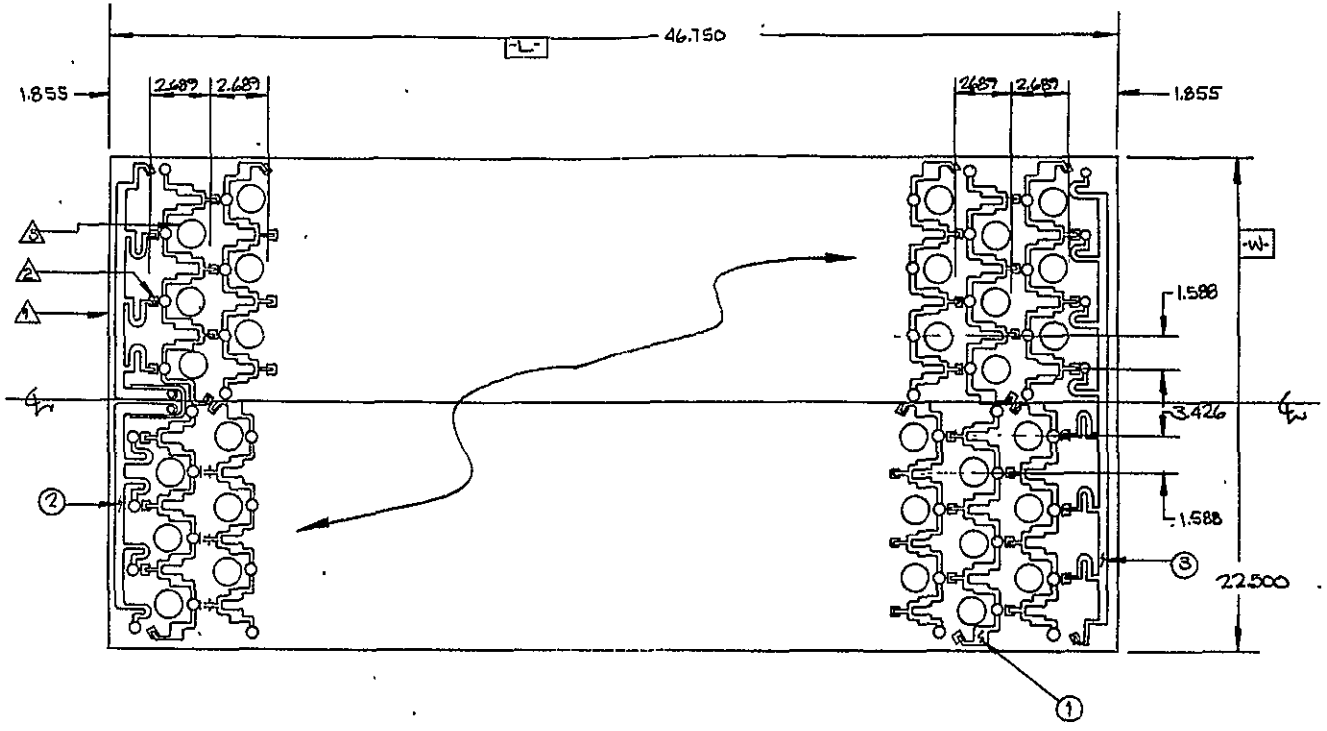


Figure 17. Cell string flex circuit for the 2' x 4' module.

ITEM	PART NO.	DESCRIPTION	REQ
3	JPL4-14-204	END BUS BAR	
2	JPL4-14-203	TERMINAL BUS BAR	
1	JPL4-14-202	INTER-CONNECTION	

TOLERANCES (UNLESS OTHERWISE SPECIFIED): DECIMALS .XX ±.010, .XXX ±.005; FRACTIONS ± 1/64; HOLES +.003 −.00; BREAK ALL SHARP EDGES

ENSOR TECHNOLOGY, Inc. CHATSWORTH • CA. 91311

DR P Lackey 3-13-97 | CHK Sung Rhim 3-15-97 | APP | USED ON

FINISH | MATERIAL

TITLE: JPL SOLAR MODULE (FLEX CIRCUIT SHEET)

SCALE — | SIZE C | DWG. NO JPL4-14-201 | SHEET 1 OF 1 | REV —

⚠3 2.125 DIA. CUT OUT.

⚠2 TAB CUT OUT.

⚠1 USE 3 MILES KAPTON (OR MYLAR) SHEET CLADDED BY 2 OZ. PER SQUARE FT OF COPPER.

NOTES, UNLESS OTHERWISE SPECIFIED

single clad design was found to substantially reduce the cost of the PC sheet and is the preferred configuration. The single clad flexible printed circuit sheet was designed to minimize thermal stress. The PC sheet will allow for connection from the bottom of one solar cell through the central hole, to the top of an adjacent solar cell as shown in Figure 18. The flexible PC sheet has tab cutouts which allow the tabs to be pushed up by a plunger to thread the solar cell. When the plunger is removed the tab makes contact with the center solder ring of the solar cell. Holes 2.125 inches in diameter are also cut out of the flexible printed circuit sheet which will allow for total lamination from the front of the module through the sides of the solar cells to the back of the module. Two types of PC sheet materials were studied. Either Kapton or mylar are potential candidate materials. One mil thick Kapton with two ounce copper was chosen for the flexible printed circuit sheet as will be discussed in the next section and Task 17.

An exploded view of the hexagonal solar cell module is shown in Figure 19. The sequence of encapsulation materials to be utilized for the conceptual module design is as follows: (a) glass (front or top surface), (b) polyvinyl butyral (PVB),

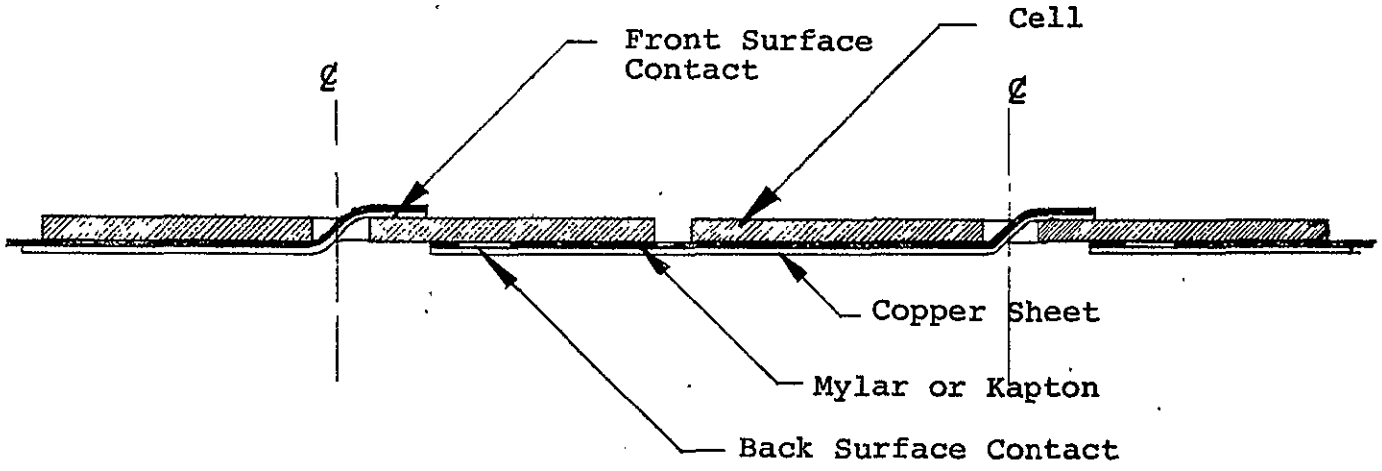


Figure 18. Inter-Connection Method Between Cells
(Copper Claded Kapton Sheet without Overlay)

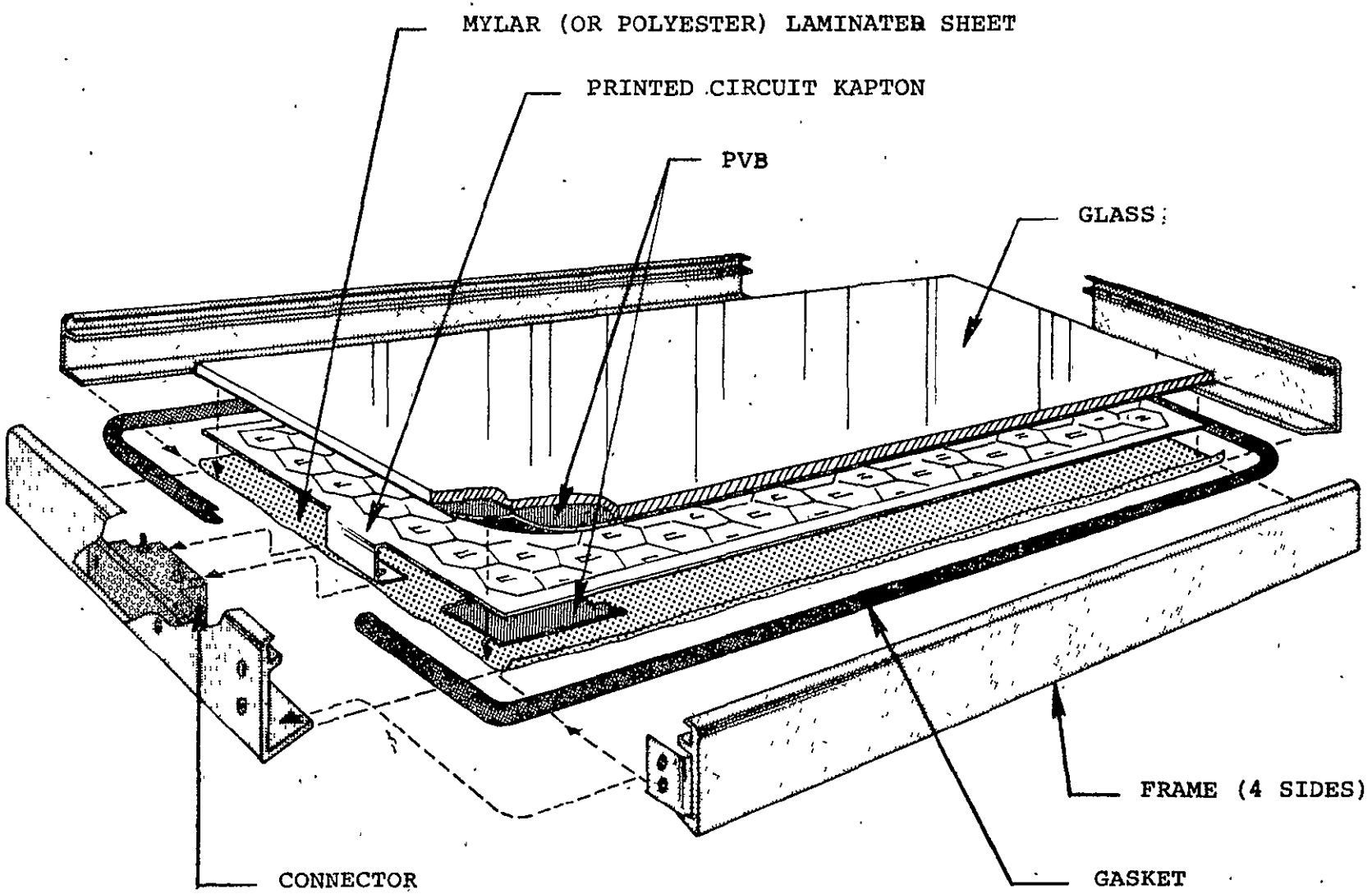


Figure19. Exploded view of hexagonal solar cell module.

(c) flexible printed circuit sheet with solar cells, (d) PVB, (e) mylar with moisture protective coating (back surface) (f) gasket and aluminum frame assembly.

The module encapsulation method will follow the standard SAFLEX lamination procedure as currently performed throughout the auto-glass industry. The only modification needed in order to apply this method to solar cell modules will be to utilize a vacuum bag procedure. The sequential steps incorporated within this encapsulation technique include: (1) washing dusted SAFLEX, (2) material lay-up, (3) degassing and vacuum bagging, (4) curing, (5) trimming and frame assembly.

c) Module Fabrication Study

An experimental investigation was performed in three areas of module fabrication. This work included a study of solar cell dispensing techniques, a tab "pop up" scheme to allow solar cells to be dropped into position on a flexible printed circuit sheet and a solar cell interconnection soldering operation on a flexible printed circuit sheet.

The first area studied was concerned with techniques for precise solar cell dispensing. This subject is discussed in detail in Task 11, where it was concluded that solar cell handling by means of robot arms is the most suitable solar cell handling technique.

The second area considered was a tab "pop-up" scheme for solar cell interconnections. In this interconnection method, a solar cell string configuration shall be interconnected by means of notched out interconnect tabs on a flexible printed circuit sheet. A basic experiment was conducted for the purpose of observing (1) the compliance characteristic of the notched-out tab when constrained to bend upright from a flat position, and (2) under simulated production conditions, the practicality of interconnecting individually dropped cells from an overhead dispenser by the tab "pop-up" method. A single "pop-up" plunger mechanism and cell dispenser were fabricated and manually tested. The plunger pin was modified to include a groove which guided the tab during the push up motion. This experiment demonstrated the viability of the tab "pop-up" interconnection technique.

The third area studied was the interconnection soldering operation. The utilization of a flexible printed circuit sheet requires simultaneous soldering of both the front and back contacts. Four potential soldering methods for performing the simultaneous soldering of the front and back contacts were identified. These four soldering methods are: (1) induction soldering, (2) I.R. soldering, (3) direct soldering, and (4) flameless gas soldering.

Induction soldering and I.R. soldering are both widely used procedures for producing simultaneous multiconnections. Unfortunately, however, neither method appears to be applicable to solar cells containing soldered gridlines, since reflow of solder from the gridlines will damage the metal contacts, which in turn will adversely affect the solar cell efficiency. Therefore, the investigation focused on the direct and flameless gas soldering methods.

A direct contact soldering test on a flexible printed circuit sheet was performed with the primary objective of evaluating three prospective materials for use as a base material in the flexible pc sheet, and then selecting from these, that material which displays the most admisable characteristics.

The three materials which were evaluated are as follows:

K1 = 1 mil Kapton with 2 oz. Cu.

K2 = 2 mil Kapton with 2 oz. Cu.

M3 = 3 mil Mylar with 2 oz. Cu.

A highly skilled operator performed the actual soldering task with the use of a controlled tip, hand-soldering iron at a temperature of 700^{o}F. The entire soldering sequence was precisely timed and the following results were subsequently obtained:

K1: time: 4 sec, no damage to Kapton - satisfactory

K2: time: 10 sec, no damage to Kapton - solder deposit melt

M3: time: 4 sec, Mylar melts - good soldering

Direct contact soldering was found to be completely ineffectual with regard to melting solder on material type K2. On the other hand, the soldering characteristics of material type K1 were found to be adequate. Due to its low melting point the mylar material had melted prior to the solder. Back surface contact soldering produced poor results for each material. Consequently a more accurate and intense heat source was required for accomplishing contact soldering.

The alternative method of flameless inert gas soldering was investigated in order to determine its applicability for use in conjunction with a specified base material for the flexible pc sheet. The flameless heating unit studied offers extremely precise temperature control for production soldering, brazing, bonding, curing or melting at temperatures up to 1600^{o}F. The heater consists of a tungsten filament inside a quartz tube over which air or inert gasses such as argon or nitrogen are passed. The coil design provides extremely efficient energy transfer which permits non-contact heating of parts in open or confined areas. Controls

permit regulation of gas flow, pressure, and electrical input into the heater thus allowing pin-point repeatable heat control.

The following experiments were performed with this equipment:

(1) Front surface contact soldering.

(2) Back surface contact soldering.

(3) Soldering cell to a 2 oz. copper Kapton sheet.

All experimental results proved to be extremely satisfactory and this method is therefore recommended for use in the solar cell interconnection soldering operation.

15. Spray-on Dopant Junction Formation

The spray-on dopant process is a low-cost, innovative junction formation technique which appears to have a high potential for achieving the 1986 LSA program goals. Several features of the spray-on dopant equipment contribute to the favorable prospects of the spray-on dopant junction formation technique. Among these characteristics are the high wafer throughput rate and the reasonably short processing time obtainable from the prototype spray-on dopant equipment. An important feature of the spray-on dopant equipment is its high adaptability to large

scale production. An equally important feature of the prototype equipment is its capability of performing a wide range of parametric variations which lead to process optimization. The following sections present a detailed description of the prototype spray-on dopant equipment, as well as documentation of the process study.

a) Spray-on Dopant Equipment

The spray-on dopant equipment utilized by Sensor Technology is the Model 100 SC precision spray-on coating and drying system which was designed and constructed by Advanced Concepts Equipment, a Division of Huestis Machine Corporation, Bristol, Rhode Island. This system was specifically designed for the purpose of spraying thin film dopants onto silicon wafers. An illustration of this system can be found in Figure 20. The system is capable of processing approximately one sq. ft. per minute, allowing 65% utilization of the conveyor area. In order to provide a more economical system which maintains all the essential controls of the sophisticated spray-on equipment, the support frame was reconstructed as a bench type model with open access. This system has the capability of providing a high degree of uniformity between successive coating batches due to a manually selected flush system which cleans the internal passages, filter, and nozzle orifice of the spray gun after the coating cycle. Good

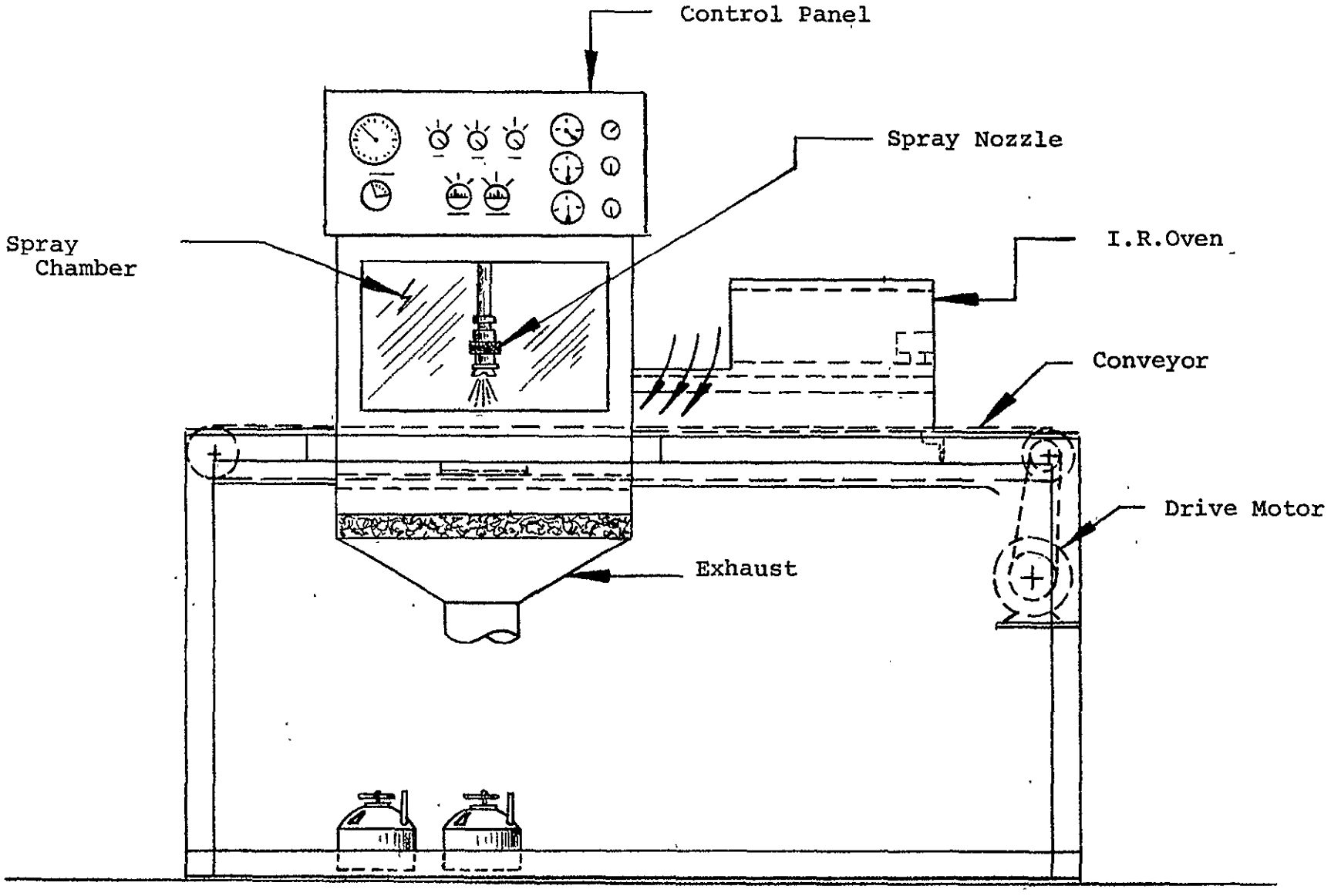


Figure 20. Sketch of spray on dopant system model.

thickness and leveling control can be attained as a result of the many overlapping passes of the spray gun. Important parameters such as conveyor speed, coating material flow rate, air or nitrogen flow rate (atomization) and I.R. emitter temperature are fully adjustable. All functions are controlled by conveniently located switches and regulators.

The coating and drying system consists of six components, each of which performs a specific function. The loading station is 12" long and accessible from three sides. The conveyor system will transport manually loaded pallets containing six wafers each, through the spraying operation, drying tunnel and finally onto the unloading station. It is driven by an explosion-proof motor and adjustable speed reducer which will provide conveyor speeds of .3 to 3 feet per minute. The spray chamber houses the air atomization spray gun which can dispense both the coating material and the cleaning solvent as the result of a special valving arrangement which has the additional advantage of facilitating selective control of the spray/flush sequence. The spray chamber has a rectangular cross-sectional area of 24" by 27" and a height of 16". The conveyor entry and exit openings extend 2" in height. An exhaust

plenum located in the lower portion of the spray chamber serves to maintain the cleanliness of the chamber through the use of overspray pans and an exhaust filter. The air dry station located between the spray chamber and the IR/convection drying tunnel, is fabricated from type 304 stainless steel. The special environment maintained in the "air dry" station hinders the formation of "pin holes" on the substrates during the subsequent elevated temperature drying cycle by evaporating the more volatile solvents from the coating. The drying tunnel is constructed of stainless steel and utilizes both convection and IR radiation to cure the thin-film coating. The infra-red radiation output of the heater panel is independently regulated by a solid state temperature controller which provides a maximum variation of $\pm$ 2% at a maximum temperature of 800^{o}F. The heater panel is covered with fiberglass insulation to minimize thermal radiation leakage to the outside enclosure. Unlike many conventional IR heat sources, this panel heater has been specifically designed for explosion-proof operation in an environment of concentrated organic solvent vapors such as that encountered in the drying tunnel. To minimize the concentration of solvent vapors within the oven tunnel, an air flow of approximately 50 linear feet per minute is recommended. The spray booth exhaust is used to

facilitate this requirement. The unloading station, like the loading station, is 12" long and accessible from three sides.

b) Mechanical Parameter Optimization

Upon delivery and installation of the spray-on dopant equipment at Sensor Technology tests were devised which set out to optimize the following key mechanical parameters:

(1) Conveyor speed, V_C

(2) Nozzle speed, V_n

(3) Dopant pot pressure, P_d

(4) Atomization pressure, P_a

(5) Baking temperature, T_o

(6) Nozzle diameter, D_n

The uniformity of the dopant spray is strongly dependent upon V_C, V_n, P_a and D_n. The pot pressure P_d, controls the dopant consumption rate, and the I.R. oven temperature, T_o depends on the conveyor speed, and the thickness of the dopant layer on the wafer surface utilized. Each of these parameters is also dependent upon the type of dopant material utilized in the dopant spray. The two types of dopant materials which were utilized in the experimental studies are as follows:

(1) Emulsitone N250, water based phosphosilica film

Viscosity: 22 centipoise

Concentration: 1×10^{18}, 1×10^{19}, and 5×10^{19} atoms /cm^3

(2) Emulsitone borosilica film, water based

Viscosity: 32 centipoise

Concentration: 1×10^{19} and 1×10^{20} atoms/cm^2

By utilizing the above mentioned dopant solutions on texturized wafers, tests succeeded in optimizing all mechanical parameters. It was found that:

(1) The optimum nozzle speed, V_n, was 50 strokes per minute at a maximum conveyor speed, V_c, of 2 feet per minute.

(2) The optimum atomization pressure P_a, for a dopant flow rate of 7cc/min., was 18 psi. For a dopant flow rate of 10cc/min., the optimized atomization pressure, P_a, was 25 psi.

(3) The optimum baking temperature, T_o, for all test conditions was 375°F.

(4) The optimum nozzle diameter, D_n, for both dopants was 10 mil.

(5) The optimized dopant pot pressures, P_d, for three different phosphosilica and boron dopant flow rates and film thicknesses are shown in Table 14.

c) Dopant Flow Rate Versus Solar Cell Electrical Performance

The mechanical parameter optimization study prompted a further investigation which was designed to assess the relationship between the phosphosilica dopant flow rate and the solar cell electrical performance. Three batches of solar cells were used in the experimental study. All spray-on dopant process parameters were fixed as shown in Table 15 with the one exception of the dopant flow rate, in order to evaluate the effect of dopant flow rate variations on solar cell electrical performance. (The atomization pressure was increased from 18 psi to 25 psi in Batch 3 in order to prevent the "dripping" effect and thus optimize the atomization pressure.)

The electrical performance test results were evaluated for the round solar cells; the fill factors and efficiencies were found to be very poor. A dopant overlap was suspected. Hexagonal solar cells were cut by laserscribe from the round solar cells and a much improved electrical performance was observed as shown

Phosphosilica Dopant:

Dopant Flow Rate	5cc/min.	7cc/min.	10cc/min
Pot Pressure	65" H_2O	95"H_2O	145" H_2O
Thickness	4 μ	8 μ	15 μ

Boron Dopant:

Dopant Flow Rate	5cc/min.	7cc/min.	10cc/min.
Pot Pressure	48" H_2O	73" H_2O	110" H_2O
Thickness	4 μ	8 μ	15 μ

Table 14. Experimental data relating the optimized dopant pot pressure, P_d, with three different phosphosilica and boron dopant flow rates and film thicknesses.

FRONT SURFACE COATING-PHOSPHORSILICA DOPANT

	BATCH 1	BATCH 2	BATCH 3
Conveyor Speed	2ft/min.	2ft/min.	2ft/min.
Oven Temperature	375°F	375°F	375°F
Dopant Flow Rate	5cc/min.	7cc/min.	10cc/min.
Drain Spray Nozzle	10 mils	10 mils	10 mils
Atomization Pressure	18 psi	18 psi	25 psi
Drying Time	½ hour	½ hour	½ hour

BACK SURFACE COATING - BOROSILICA DOPANT

	BATCH 1	BATCH 2	BATCH 3
Conveyor Speed	2ft/min.	2ft/min.	2ft/min.
Oven Temperature	375°F	375°F	375°F
Dopant Flow Rate	7cc/min.	7cc/min.	7cc/min.
Drain Spray Nozzle	10 mils	10 mils	10 mils
Atomization Pressure	18 psi	18 psi	18 psi
Drying Time	½ hour	½ hour	½ hour

Table 15. Spray-on dopant process parameters utilized in three solar cell batches. The dopant flow rate was varied in the front surface coating while all other parameters in both the front surface coating and back surface coating were held constant in the three batches.

in Table 16. The fill factors and efficiencies for all three batches were significantly increased after the round solar cells were cut into hexagons. Therefore, it can be concluded that dopant overlap can be eliminated by use of the laserscribe to trim off the solar cell edges.

The laser trimming operation is thus seen to be very effective, and it or some other edge clean up technique is an essential procedure for improving the photovoltaic energy conversion efficiencies of solar cells processed with the spray-on dopant technique.

A relationship between the dopant flow rate and the hexagonal solar cell efficiencies can be established on the basis of the experimental data obtained from the three batches. As shown in Figure 21, a plot was made of the mean value of the hexagonal solar cell efficiencies versus the dopant flow rate. The maximum and minimum efficiencies of each of the three batches are included in the figure. The mean value in the efficiency appears to increase as the dopant flow rate goes up. The increase in efficiency, however, is less than the spread of the data; therefore, a firm conclusion cannot be made at this time, and further work in this area is recommended. The data shown in Figure 21 also indicate that the spread in the efficiency data tends to decrease as the dopant flow rate increases, but again no definite conclusion can be made at this time, and further work in this area is recommended.

Table 16. Electrical performance of round and hexagonal solar cells for three spray-on dopant flow rates. Data recorded at 28°C and at 100 mW/cm^2 under tungsten light.

Cell No.	Isc (a)		Voc (v)		Ipp (a)		Vpp (v)		Ppp (w)		FF		η (%)	
	Round	Hex	Round	Hex	Round	Hex	Round	Hex	Round	Hex	Round	Hex	Round	Hex
BATCH 1 (Dopant Flow Rate is 5cc per minute)														
1.	1.76	1.47	.535	.565	1.44	1.31	.390	.420	.562	.550	.597	.662	8.83	10.82
2.	1.78	1.45	.540	.565	1.50	1.13	.375	.440	.562	.497	.585	.607	8.83	9.78
3.	1.78	1.52	.535	.565	1.50	1.34	.330	.430	.495	.581	.520	.677	7.78	11.44
4.	1.82	1.47	.545	.570	1.58	1.28	.375	.425	.592	.544	.597	.662	9.31	10.71
5.	1.71	1.46	.545	.570	1.45	1.34	.375	.400	.544	.536	.584	.644	8.55	10.55
6.	1.68	1.42	.535	.560	1.32	1.12	.375	.425	.495	.476	.551	.599	7.78	9.37
Avg.	1.76	1.47	.539	.566	1.47	1.26	.370	.423	.542	.530	.572	.642	8.51	10.45
BATCH 2 (Dopant Flow Rate is 7 cc per minute)														
1.	1.78	1.49	.545	.570	1.50	1.39	.395	.425	.592	.591	.610	.696	9.31	11.63
2.	1.78	1.53	.545	.555	1.60	1.35	.360	.400	.576	.540	.594	.636	9.05	10.63
3.	1.81	1.48	.545	.570	1.60	1.27	.375	.400	.600	.508	.608	.602	9.43	10.00
Avg.	1.79	1.50	.545	.565	1.56	1.34	.377	.408	.590	.546	.604	.645	9.26	10.75
BATCH 3 (Dopant Flow Rate is 10 cc per minute)														
1.	1.75	1.44	.540	.570	1.49	1.35	.400	.420	.596	.567	.631	.691	9.37	11.16
2.	1.75	1.50	.540	.565	1.37	1.40	.400	.395	.548	.553	.580	.652	8.61	10.89
3.	1.79	1.48	.545	.570	1.59	1.34	.375	.430	.596	.576	.611	.683	9.37	11.34
4.	1.78	1.47	.535	.565	1.45	1.34	.390	.415	.566	.556	.594	.669	8.90	10.95
5.	1.74	1.47	.535	.565	1.35	1.35	.400	.400	.540	.540	.580	.650	8.49	10.63
Avg.	1.762	1.472	.539	.567	1.45	1.356	.393	.412	.569	.558	.600	.669	8.95	11.00

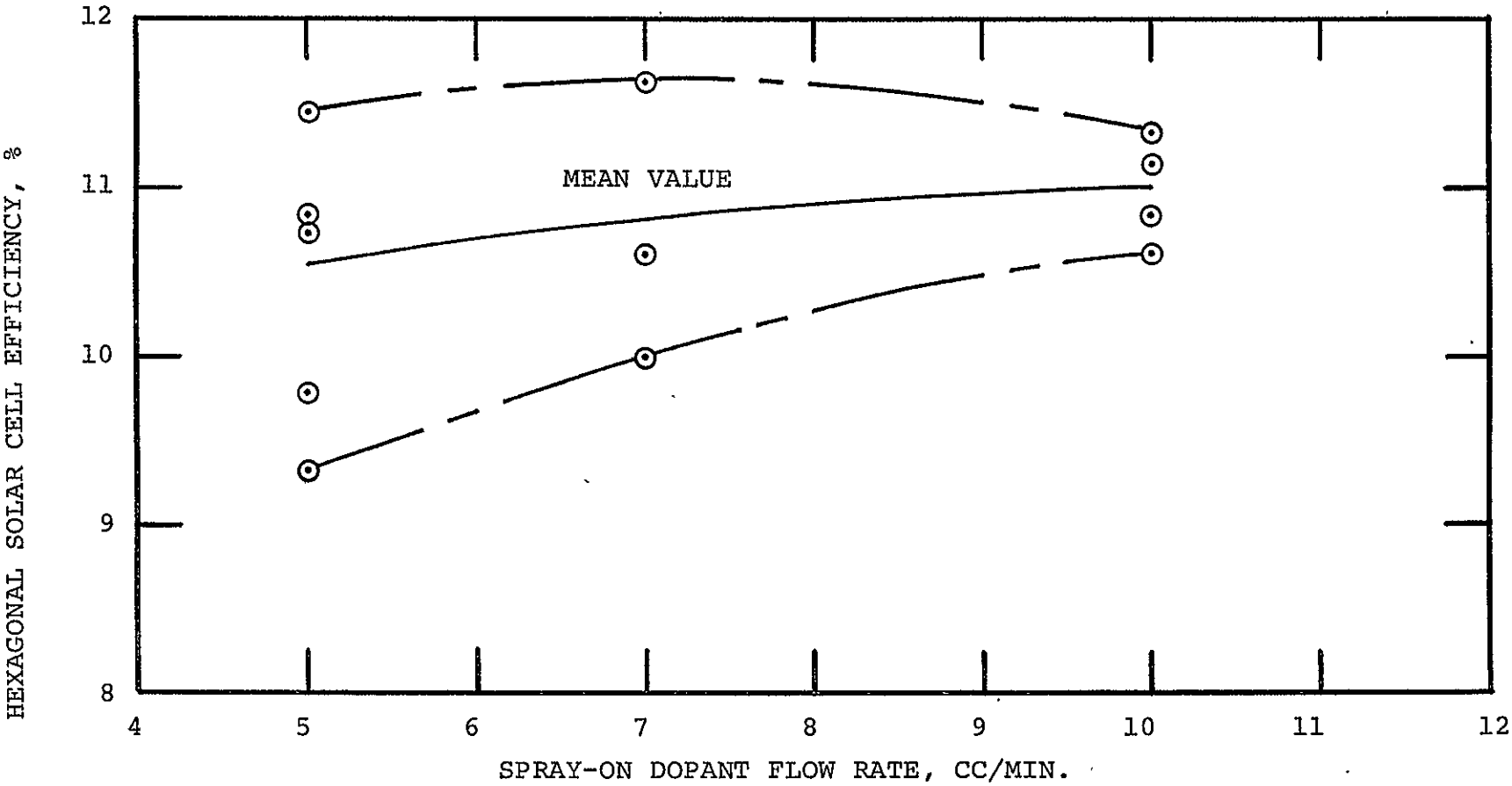


Figure 21. Spray-on dopant flow rate versus hexagonal solar cell efficiency.

d) Excess Dopant Removal

The excess dopant remaining on spray-on-doped cells following the drive-in process must be removed since the excess dopant will cover the cell surface in the form of a silica film, and have the undesirable effect of reducing the solar cell electrical performance. The silica film can be removed by a hydrofluoric acid etching process. The electrical performances of solar cells with and without excess dopant removal are shown in Figure 22 and Table 17. The electrical performance improvement includes both the fill factor and the solar cell efficiency. It is apparent from the figure and the table that excess dopant removal will significantly enhance solar cell efficiency.

e) Summary of Results and Cost Analysis

The mechanical parameter optimization study was highly effective in defining specific mechanical parameter values which lead to low cost, high efficiency solar cells. Several unexpected developments which were a direct outgrowth of this study appear to warrant further investigation and study. One such development includes an experimental correlation between dopant flow rates and hexagonal solar cell efficiencies. An additional development consists of an apparent correspondence between small efficiency data spreads and large dopant

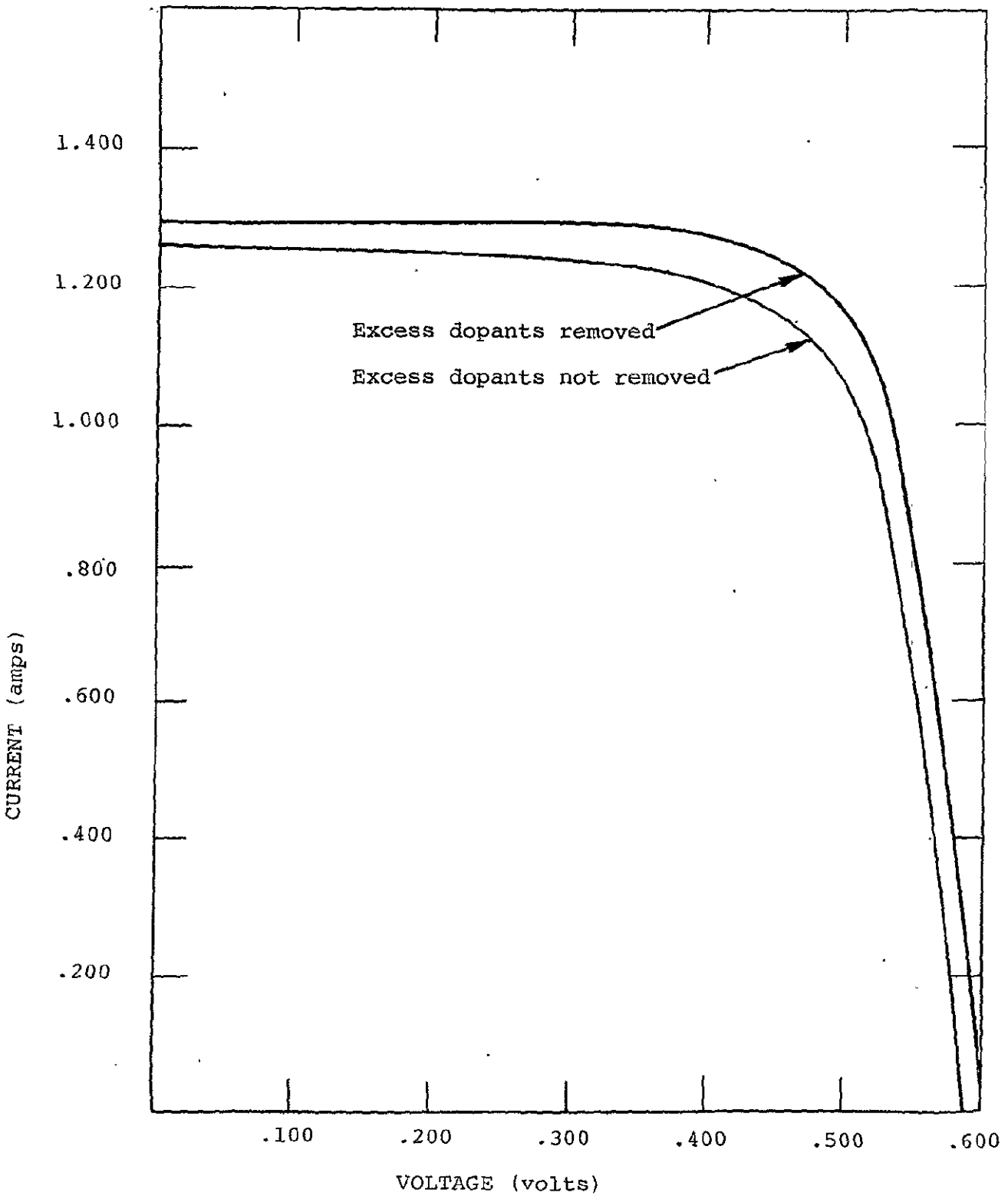


Figure 22. Effect on solar cell electrical performance when excess dopants are removed in the spray-on dopant process. Cells are texturized with no A.R. coating. Surface area is 45 cm^2. Cells are tested at 28°C under 100 mW/cm^2 tungsten light.

	EXCESS DOPANTS NOT REMOVED	EXCESS DOPANTS REMOVED
I_{sc}	1.25 amps	1.28 amps
V_{oc}	0.6 volts	0.61 volts
I_{pp}	0.10 amps	1.18 amps
V_{pp}	0.475 volts	0.480 volts
P_{max}	0.5225 watts	0.5664 watts
FF	0.697	0.725
η	11.611 %	12.59 %

Table 17. Electrical parameters of solar cells with and without excess dopant removal.

flow rates. As a further means of improving the efficiency of hexagonal spray-on-dopant solar cells, it is recommended that an excess dopant removal step should be incorporated in the overall spray-on-dopant process sequence.

A SAMICS cost analysis was performed on the spray-on-dopant process sequence. A detailed cost breakdown for the spray-on dopant process is shown in Table 18. The process sequence consists of three steps which include (1) spray-on N^+ and P^+ dopants, (2) dopant drive-in, and (3) excess dopant removal. The resulting process cost is 3.10 cents per peak watt in 1975 cents. This cost is in line with the 1986 LSA program goals. Consequently, the spray-on dopant process is highly recommended for usage in the 1986 LSA solar cell industry.

16. Conveyorized Dopant Diffusion

Conveyorized dopant diffusion was investigated as an alternative dopant deposition technique. The distinguishing feature of this deposition method resides in the utilization of a conveyorized low temperature doped oxide (LTO) system. The carrier gas for the LTO system is nitrogen and the reactive gases forming the N^+ source

Table 18. Process costs for a fully automated spray-on dopant junction formation process in 1975 cents per peak watt.

Equipment	0.550
Floor Space	0.174
Labor	0.567
Material	1.180
Utility	0.641
TOTAL	3.10

Spray-On Dopant Process Steps

1. Spray-on N^+ and P^+ Dopants.
2. Dopant Drive-In.
3. Excess Dopant Removal.

are silane, phosphine, and oxygen. At the conclusion of a suitable time period, the phosphine gas is eliminated so that a layer of silicon dioxide glass may form on the wafer surface. This "cap" oxide will serve to prevent the occurance of cross diffusion during the subsequent dopant drive-in step. Immediately following the N^+ dopant depositions, each wafer is automatically turned over by means of a conveyorized mechanism, thus readying them for p^+ deposition in a second LTO system.

Several companies were identified which possessed the capability of performing low temperature doped oxide depositions. Advanced Silicon Material Co. (ASM) was selected to perform the dopant tests and to design a fixture to simulate the conveyor. Upon carrying out the experimental test runs in their LTO sytem, the specially designed fixturing for the 3¼ inch wafers was found to actually improve the uniformity across the wafers to an extent which exceeded the expectations of ASM. A total of 25 cells had undergone processing in the LTO system, with a deposition time of 9 minutes at 425^{o}C and .196 torr. These processed cells were received by Sensor Technology and electrical performance tests were conducted for process

verification. Each test, however, yielded negative results which were attributed to surface damage incurred during processing at low pressure in a chemical reactor. Surface damage, which promotes low minority carrier lifetime, is thus responsible for the poor electrical performance of the experimental cells. While this dopant process was not thoroughly investigated, sufficient cause was found to render this process unsuitable for our applications.

17. Module Model Fabrication Study

A unique hexagonal solar cell central hole interconnection concept involving the use of a flexible printed circuit sheet with notched-out tabs, and a PVB lamination procedure for module encapsulation, was demonstrated with the fabrication of a module model. The novel solar cell interconnection concept was found to greatly simplify the cumbersome task of solar cell interconnection for cell string assembly. The demonstration of the PVB lamination procedure required a determination of important process parameters such as the time, pressure, and temperature cycles required for the optimal performance of the lamination procedure. An important facet of the demonstration of the PVB lamination procedure resided in verifying that hexagonal solar cells with central holes can withstand the lamination procedure without incurring excessive damage due to radial cracks. Since the viability of

the flexible printed circuit sheet with notched out tabs is described in detail in Task (14), the demonstration of the lamination procedure and module assembly process will receive major emphasis in the following sections.

a) Description of the Module Model

A module model consisting of hexagonal solar cells interconnected through their central holes by way of notched-out tabs on a flexible printed circuit sheet was fabricated through the use of a PVB lamination process. A picture of the hexagonal solar cell module is shown in Figure 23. The dimensions of the module are 12" x 15". All other aspects of the module model are identical to the large scale prototype module described in Task 14, with the exception of the number of hexagonal solar cells.

The flexible printed circuit sheet for the module model is shown in Figure 24. As can be seen from this Figure, 3½ cells are connected in parallel, and five such cell strings are connected in series so that the total number of cells is equivalent to 17.5 full hexagonal solar cells (15 full cells and 5 half cells). Two types of terminal tabs were utilized.

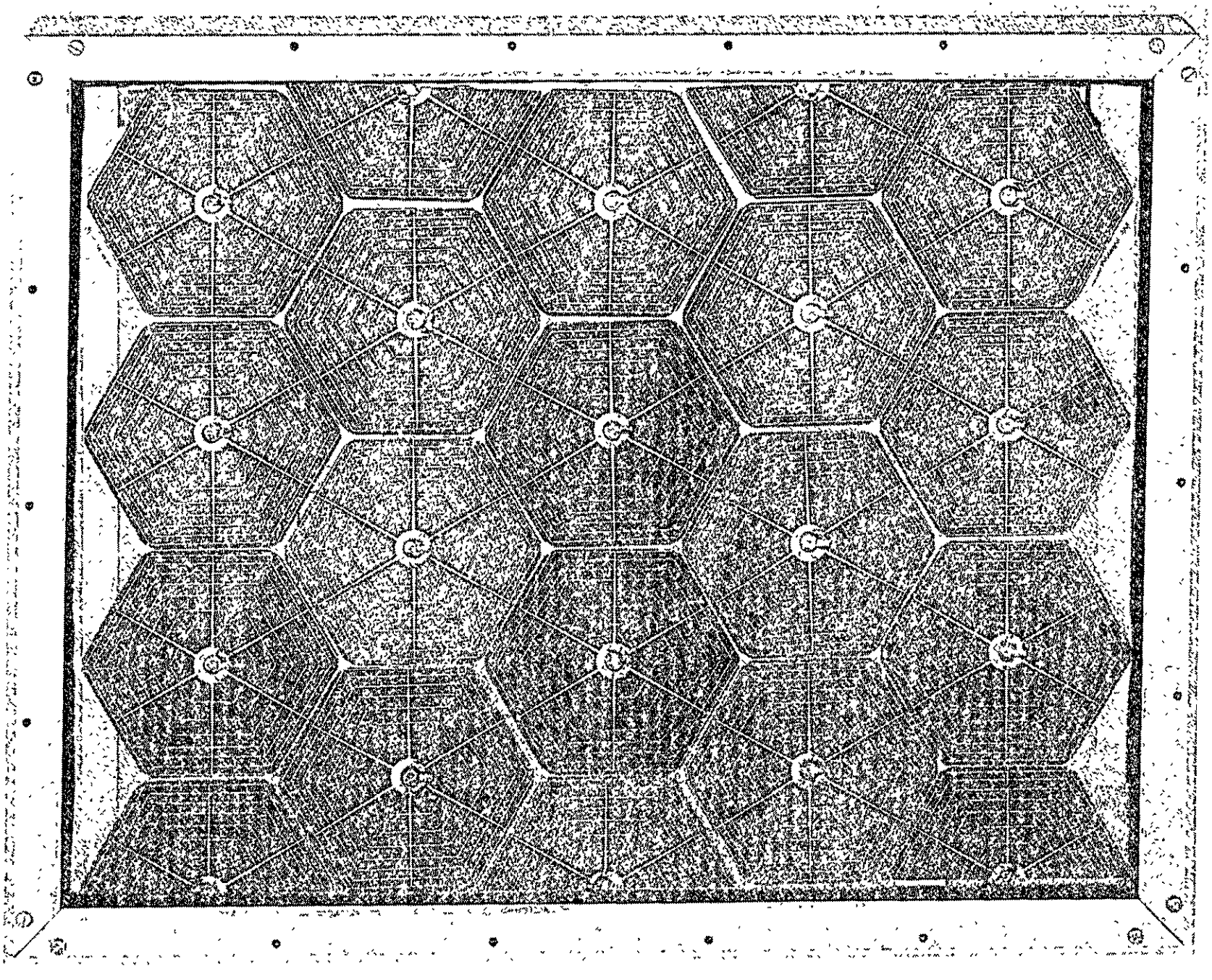


Figure 23. Picture of the hexagonal solar cell module with center hole interconnection scheme.

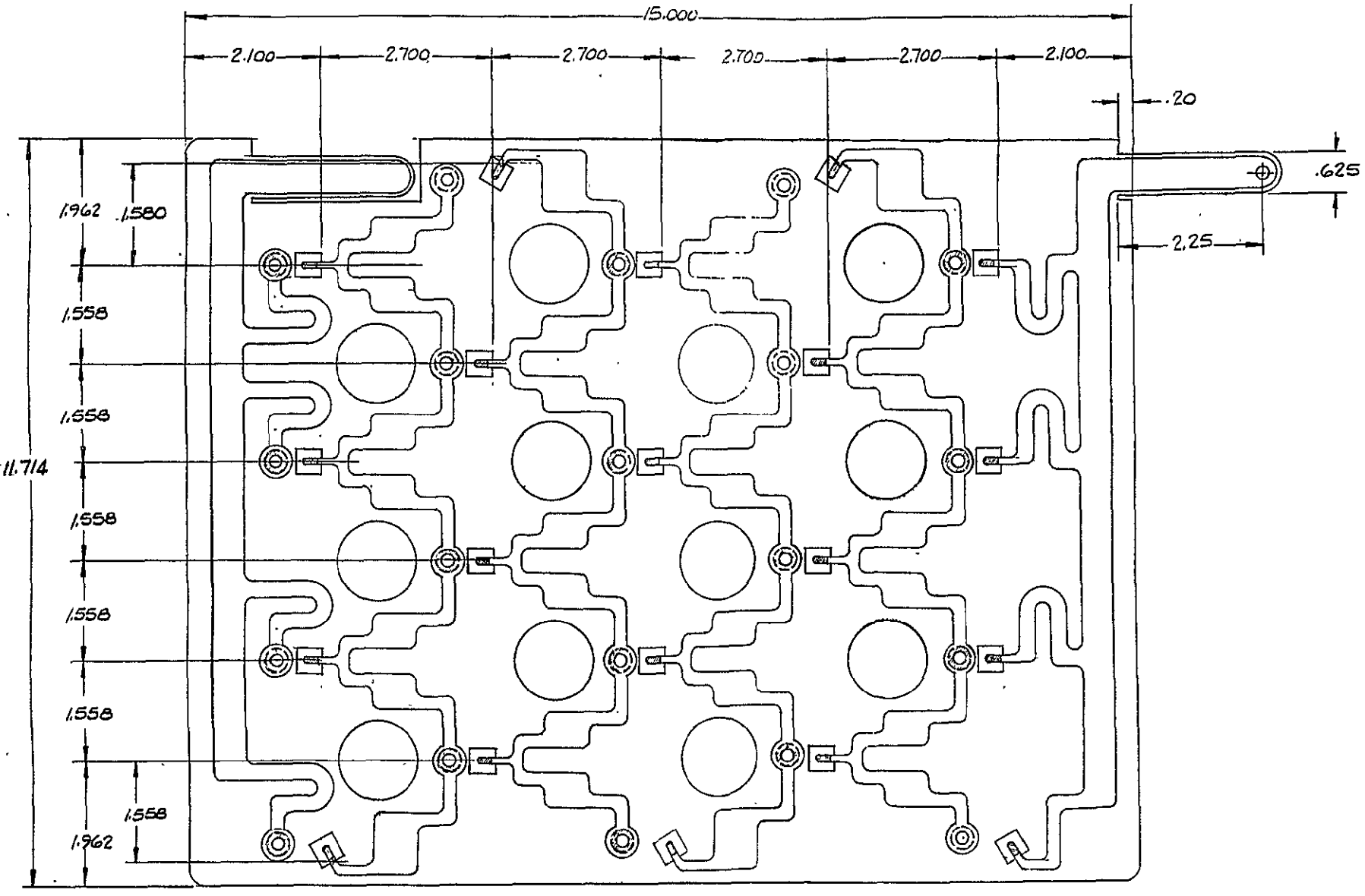


FIGURE 24. Cell string flex circuit model configuration

All encapsulation materials which were utilized for the module model are presented in Table 19. The sequence of encapsulant materials consists of glass, PVB, solar cells on a flexible printed circuit sheet, PVB and mylar. The edge seal is butyl-rubber sealant and the framing assembly is aluminum.

(b) Description of Fabrication Method

(1) Flexible Printed Circuit Sheet:

The flexible printed circuit sheet was manufactured by an outside flexible printed circuit sheet manufacturer. A two ounce per square foot sheet of copper was laminated onto a prepunched Kapton sheet. The copper was then etched in order to obtain the proper circuit pattern. Finally, the tab for central hole solar cell interconnection was cut out.

(2) Solar Cell Interconnection:

The cells with central holes were positioned and manually soldered by means of the flameless inert gas soldering method. The cells were then prepared for the lamination procedure.

(3) Encapsulation:

The standard PVB lamination procedure is currently practised throughout the autoglass industry. The only modification which was necessary in order to apply this method to photovoltaic modules was the use

Table 19. Final Encapsulant Materials for Module Element

Elements:	Selected Materials
Superstrate:	ASG SUNADEX (Rolled water white, 0.019 iron oxide), glass, tempered, $^1/_8$" thick.
Flexible Circuits:	0.001" Kapton with 2 oz/sq.ft. copper laminated.
Adhesive Material:	SAFLEX SR11 (Architectural type), 0.015 in. thick. Two layers of this type are needed at top and bottom of cell strings.
Substrate:	Mylar type "A", 0.005" thick
Edge Sealant:	Butyl-rubber sealant (TREMCO's proglaze) with TREMCO ARO-SHIM.
Frame:	Aluminum frame, anodized.

of a vacuum bag method. The design dependant parameters such as temperature, and pressure, were determined experimentally and will be discussed in a later section.

A brief description of each step incorporated within this encapsulation technique is presented below.

Washing Dusted Saflex

Dusted Saflex, which is utilized to prevent sticking, consists of a uniform layer of sodium bicarbonate applied to the sheet surface. Prior to lamination, the Saflex must be removed by a 110 to 120^{o}F water wash and rinse.

Lay-Up

All layers are put in lay-up form in order to facilitate encapsulation. The layered structure consists of glass/PVB/cell string assembly/PVB/mylar. Each sheet must be cleaned prior to lay-up, and the lay-up takes place in a temperature and moisture controlled room.

Degassing and Vacuum Bagging

All layers are placed into the vacuum chamber with heat sealable nylon at the top and bottom of the layer. The chamber is gradually heated up to 165 to265^{o}F

while it undergoes concurrent degassing with the vacuum pump. The chamber is then pressurized at approximately 15 to 50 psi, and the vacuum bag is sealed.

Autoclaving

The autoclaving operation is the final step in the laminating process. The vacuum bagged module layers are heated up to a temperature range of 250 to 300^{o}F. The entire assembly is then pressurized at 50 to 180 psi and held for 7 to 30 minutes. After this holding period, it is slowly cooled down to 160^{o}F, while under pressure. The pressure is then released.

The key parameters for this operation are temperature, holding time, and pressure. In particular, if the grid lines contain solder, the maximum temperature must be less than the melting point of solder in order to prevent solder reflow. In addition, the pressure must be as small as possible to prevent cell cracking due to pressure loads.

All parameters are dependent upon lamination size, thickness, and number of layers. Consequently these parameters will be determined experimentally.

(4) Framing Assembly:

The excess sheet material at the edges of the encapsulated modules was trimmed off. The aluminum frame was then mounted with the proper sealant.

c) Experimental Study

Four progressive tests were performed to determine the proper laminating conditions. A reference module with "parallel track" pattern hexagonal solar cells without a PC sheet was used to elicit a comparative analysis. The test conditions in all four cases are summarized in Table 20. A summary of the results of each test is presented in Table 21. The test results are elucidated in the following sections.

Test # 1

For the initial test, the highest possible temperature (356^{o}C) and the lowest possible pressure (50 psi) were chosen in conformance with the previously designated process parameter limitations. The test results indicate that many cracks developed within the central hole solder ring. In addition, there was evidence of solder reflow caused by the high temperature. Despite the fact that 90% of the cells were cracked,

Table 20. Summary of the test conditions for the module model fabrication

Test No.	Top PVB Thickness	Autoclave Temp.	Autoclave Pressure	Total Process Time
A-1	15 mils	356°F	50 psi	2 hours
A-2	30 mils	347°F	50 psi	2 hours
A-3	30 mils	270°F	50 spi	4 hours
A-4	30 mils	270°F	45 psi	4 hours
Ref. (B-2)	15 mils	347°F	50 psi	2 hours

Table 21. Summary of the electrical performance test results for the module model fabrication

Test No.	Voc *	Isc *	Description of Results
A-1	2.89 volt	4.16 amp	90% of cell has ring cracks. Solder reflow. Bubble at center hole.
A-2	2.87 volt	4.6 amp	50% of cell has ring cracks. Bubble at center hole. No solder reflow.
A-3	2.65 volt	4.15 amp	Three line cracks. No bubble. No solder reflow.
A-4	2.85 volt	4.29 amp	One line crack. No bubble. No solder reflow.
Ref. (B-2)	2.89 volt	4.24 amp	No cracks. No bubbles

*Test at 28°C, 100 mw/cm^2 insolation

there was no indication that this had a deleterious effect on the module electrical performance as evidenced by Table 21. The negligible effect of the cracked cells on the module performance can be explained on the basis that since the cracks occured within the center ring, they have no influence on current collection outside of the ring.

Test # 2

To eliminate the solder reflow problem observed in Test # 1, the temperture was reduced to 347^{o}F and also, a thicker PVB sheet (30 mil) was utilized to prevent interior center ring cracks induced by the thick solder layer at the center ring.

The results show that 50% of the cells still have interior center ring cracks. However, the solder reflow problem was eliminated. The module electrical performance was similar to test # 1. Bubbles were also trapped in the front surface.

Test # 3

This test was distinguished by lower temperature (270^{o}F) and longer heating cycles with the same pressure load. The longer heating cycle served to ensure uniform heating prior to pressurization. The results show an apparent improvement. No center ring cracks were

observed, however, three cells had line cracks. The electrical performance of this module was almost identical to the reference module.

Test # 4

This test was identical to test # 3 except that a slightly lower pressure was utilized. This time, only one line crack was observed. However, it is believed that this crack was introduced during lay-up from mishandling. The electrical performance of this module was found to be higher than the other tests.

Test # 5 - Reference Module

The "parallel track" pattern hexagonal solar cell module without central holes incurred no encapsulation problems based on past experience. The sequence of encapsulation materials was glass/PVB/cell string/PVB/mylar. Back solar cell interconnection was achieved by two ribbon wires. Three and one-half cells were interconnected in parallel and five such groups were connected in series. The encapsulated module was

bubble and crack free. This module type was used as a reference module for comparing the test module.

Discussion of Test Results

The module model which utilized the central hole interconnection method with a flexible printed circuit sheet was successfully encapsulated with PVB adhesive as the underlayer. The module model fabrication required the specification of several process parameters due to the thick solder layer at the center hole and the stress concentration at the center hole. In comparison with conventional (reference) module fabrication, it can be concluded that:

(1) The new module requires more processing time due to the longer heating cycle.
(2) The new module requires low temperature during fabrication.
(3) The new module displays good electrical characteristics if a thick layer of PVB is utilized.

An extensive experimental study could possibly reduce the processing time. Since the processing parameters were dependant upon the module size,

no further study will be performed with the small scale module. It was demonstrated that the new fabrication concept is feasible, and further study with a prototype scale module to optimize fabricaton parameters is recommended.

d) Module Model Fabrication Conclusion

The specification of several process parameters led to the successful performance of the lamination procedure for the module model. The central hole interconnection scheme was successfully demonstrated; no solar cell cracks were observed after the proper lamination procedure was evolved. It was found that this central hole interconnection method greatly simplifies solar cell string assembly for module fabrication.

SAMICS - PROCESS COST ANALYSIS

All Low-Cost Solar Array (LSA) projects require a thorough cost analysis to establish their potential for meeting certain specific price goals. Since process cost estimation methods differ from one company to the next, Solar Array Manufacturing Industry Costing Standards (SAMICS) are recommended. The SAMICS method allows one to make a relative comparison between potential prices attributable to competing processes and to obtain the best possible process price estimate.

All process steps under this program for Phase 2 of the Array Automated Assembly Task had a cost analysis performed. A simplified preliminary cost analysis was initially made for each process step in order to elicit a relative comparison between competing processes. The process which displayed the lowest overall cost was selected for use in a model automated production line. The more costly competing processes were rejected.

Large volume production and high throughput rate are essential for meeting the 1986 LSA goals; therefore, the automation potential of each of the selected processes was evaluated. If state-of the-art technology was available to produce automated versions

of the current process equipment, then the automated equipment was utilized in the model company. However, in those cases for which current technology was deemed inadequate to produce automated process equipment, existing unidentified versions of the equipment were utilized in the model company. Also, a number of necessary intermediate process steps in the total process were given minor emphasis in this program since they are standard processes presently in use at Sensor Technology Inc.

Several SAMICS procedures were updated during the course of this program. Consequently, all SAMICS results presented in this study are to the latest SAMICS revisions.

All hypothetical industries utilized in SAMICS are the 1986 standards as defined by the Interim Price Estimation Guidelines, IPEG, in reference (5). Input data preparation and process cost computations were performed in accordance with references (6), (8) and (9). All expense items were evaluated on the basis of the cost account catalog in reference (7).

1. Description of the Industry

The structure of the industry is assumed to be the 1986 standard industry as defined in reference (5). The model industry is composed of a sequence of companies, each of which is an independent financial entity. A total of five successive companies constitute the model industry. This study focussed on only two of these companies; the cell manufacturing company and the module manufacturing company. It was assumed that all remaining companies of the model industry operate under the current price goals defined in reference (5). The two companies under consideration in this study will hereby be designated as CELLCO and MODULCO, which manufacture photovoltaic cells and modules respectively.

The basic assumptions utilized in the standard industry are listed below:

(1) CELLCO and MODULCO are vertically integrated companies which share 40 percent of their corresponding markets. CELLCO will purchase wafers from WAFERCO at the price of 22 cents per peak watt in 1975 cents as set forth in reference (5). MODULCO will purchase 100% of its solar cells from CELLCO.

(2) A double burden was not charged for silicon wafers or cells since they were assumed to be vertically integrated as defined in reference (9).

(3) CELLCO and MODULCO require 4.7 shifts per day, 24 hours per day, 7 days per week, 345 operating days. All remaining modifications specified in reference (9) were utilized in this analysis.

(4) CELLCO and MODULCO maintain a production yield of 96.3% and 95.1% respectively.

(5) The module cost is based upon both its design and electrical performance. The detailed product description presented in reference (1) and (11) can be summarized as follows:

Module size: 2' x 4'

Number of Cells: 119 equivalent modified hexagonal cells (102 full cells and 34 half cells)

Cell Efficiency: 14.7% after encapsulation

Packing Ratio: 87%

Usable silicon per wafer: 81%

Cell size: 90mm point to point diameter modified hexagonal solar cell with 51.32 cm^2 area.

Module Output: 90 watts (0.76 watts/cell) at 100mW/cm^2 insolation.

In view of the above specifications, the anticipated annual production output for the two companies is as follows:

CELLCO: 278 million solar cells per year or 210.3 MW per year

MODULCO: 2.22 million modules per year or 200 MW per year

These output rates are used in the SAMICS analysis.

2. CELLCO Firm

a) Company Description

The CELLCO firm is a model company in the 1986 standard industry which produces solar cells from silicon wafers. The annual production quantity for this company is 278 million solar cells per year which is equivalent to 210 MW per year.

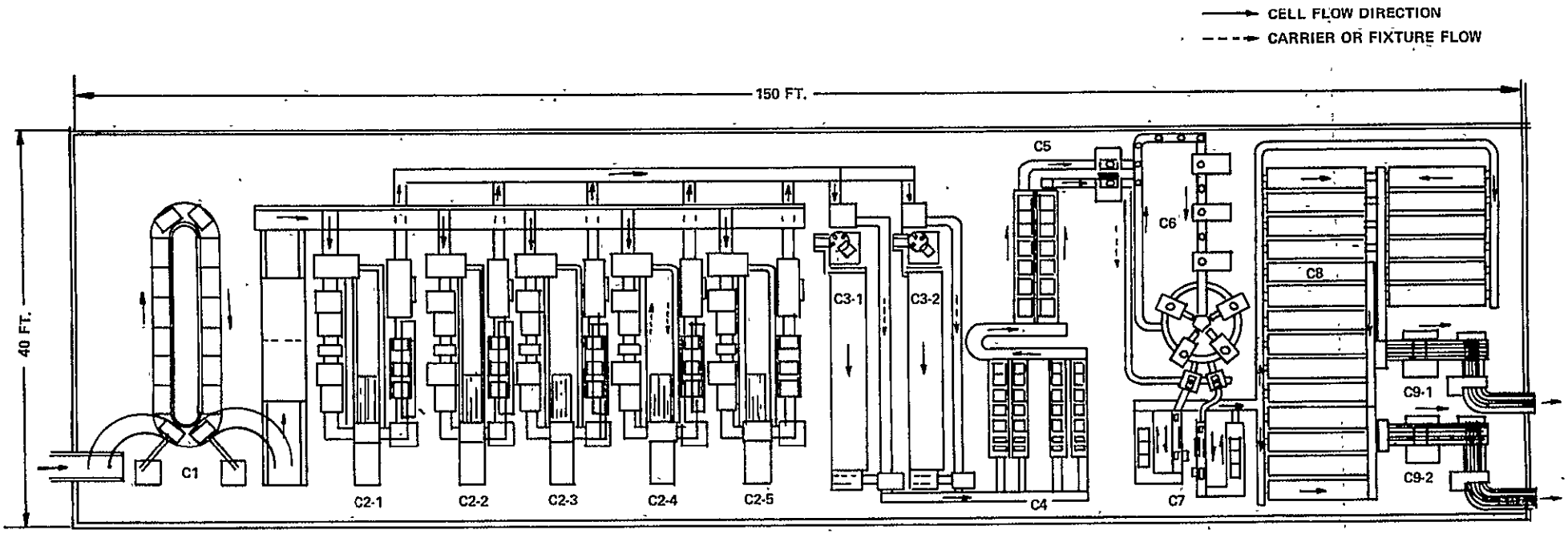
The solar cell production process sequence was selected for CELLCO on the basis of a SAMICS cost analysis performed on all process steps investigated in this array automated assembly program. A production line consisting of nine solar cell process steps was selected for CELLCO. A conceptual layout of the model plant is shown in Figure 25.

SENSOR TECHNOLOGY CELLCO PRODUCTION LINE

40 MEGAWATT PER YEAR CAPACITY

7200 WAFERS PER HOUR

CELLCO NEEDS SIX LINES FOR 200 MEGAWATT PER YEAR PLANT.



C1 : WAFER SURFACE PREPARATION (1 UNIT)

C2 : JUNCTION FORMATION (5 UNITS)

C3 : FRONT SURFACE PATTERN PRINTING (2 UNITS)

C4 : ELECTROLESS NICKEL PLATING (4 UNITS)

C5 : RESIST REMOVAL (2 UNITS)

C6 : LASERSCRIBING (1 UNIT)

C7 : SOLDER FLOW (2 UNITS)

C8 : PLASMA A-R COATING (20 UNITS)

C9 : CELL TESTING & GROUPING (2 UNITS)

The Sensor Technology CELLCO plant was designed to produce approximately 40 MW per year, or about 7200 wafers per hour. Six production lines will therefore be required to produce 200 MW per year, which is 40 percent of the total market.

A brief description of each of the nine selected process steps in the CELLCO model plant is given below:

(C-1) Wafer Surface Preparation (WFSURPR)

This process step consists of wafer surface cleaning, wafer surface texturizing, and final cleaning and drying.

(C-2) Junction Formation (JUNCF)

The junction formation process sequence includes: spray-on n^+ dopant onto the front surface with a subsequent IR bake, spray-on p^+ dopant onto the back surface with a subsequent IR bake, dopant drive-in, and excess dopant removal.

(C-3) Front Surface Pattern Printing (FSPP)

An initial process step prior to metallization is thick film resist printing by means of a negative mask. Metallization pattern printing of the front surface is followed by a standard drying process.

(C-4) Electroless Nickel Plating (ELNIPL)

This is an active metallization process. Nickel is plated onto the front surface gridline pattern, in addition to the entire back surface. A cleaning step after plating is included in this process step.

(C-5) Resist Removal (RESREM)

This process step consists of a wet chemical resist removal procedure. A wafer cleaning and drying method is also incorporated in this process step.

(C-6) Laserscribing (HEXLS)

An automatic laserscribing system for large volume production was developed and utilized in this program. The laserscribe performs the scribing of hexagonal solar cells and also trepans center holes.

(C-7) Solder Flow (SDFLW)

The front surface grid pattern and back surface are solder coated in this process. The complete solder flow process consists of preheating, flux application, solder dipping and flux removal.

(C-8) Anti-Reflective Coating (ARCT)

The solar cell anti-reflective coating is applied by silicon nitride plasma deposition.

(C-9) Cell Testing and Grouping (CELTEST)

Solar cells are automatically tested, analyzed and grouped according to electrical performance.

b) Price Computation

The price of a solar cell was determined after all the data in Format A's were compiled. The cost computation proceeded in accordance with the procedures outlined in the process work sheets and company work sheets described in Reference 6. Additional expense item information, which was not included in the cost account catalog in Reference 7, was found in currently available market price literature.

The cost for each solar cell process step was manually calculated and is shown in Table 22. The cost for each step was further broken down into cost elements which include the cost for equipment, floor space, labor, material and by-products, and utilities in terms of 1975 cents per peak watt.

Table 22. CELLCO process cost summary in 1975 cents per peak watt.

* Highest Cost Element

Process Number	Process Referent	Equipment	Floor Space	Labor	Material & By Products	Utilities	TOTAL
C-1	WFSURPR	.200	.072	.440	.780	.190	1.682
C-2	JUNF	.550	.174	.570	1.200	.641	3.135
C-3	FSPP	.128	.110	.270	.424	.050	.982
C-4	ELNIPL	.084	.038	.430	3.810 *	.138	4.500 *
C-5	RESREM	.027	.017	.220	1.636	.109	2.009
C-6	HEXLS	.270	.030	.350	.004	.123	.777
C-7	SDFLW	.050	.021	.210	1.900	.213	2.394
C-8	ARCT	1.861*	.124	.940	.800	.274	3.999 *
C-9	CELLTEST	.100	.018	.185	0	.018	.321
TOTAL		3.270	.604	3.615	10.554	1.756	19.80

c) Discussion of Results

The total added value for CELLCO is 19.8 cents per peak watt in 1975 cents. This value is slightly higher than the IPEG price goal of 18.7 cents per peak watt. As shown in Table 22 the metallization (step C-4) and A.R.Coating (step C-8) claim a disproportionate share of the total cost for CELLCO. The major short coming of the current electroless nickel plating metallization process is its use of expensive materials. The major short coming of the silicon nitride plasma deposition A.R.coating process resides with the high equipment cost which is primarily due to low throughput rate. It is recommended that work be directed toward reducing costs in the metallization and A.R.coating process steps. Candidate procedures for these two processes respectively are spray-on metallization and spray-on A.R.coating.

3. MODULCO Firm

a) Company Description

The MODULCO firm is a model company in the 1986 standard industry which produces solar cell modules from solar cells. The annual production quantity for this company is 2.222 million modules per year which is equivalent to 200 MW per year.

The module assembly process sequence was selected for MODULCO on the basis of the work performed in Tasks (11), (14), and (17) in this annual report. A production line consisting of seven module assembly steps was selected for MODULCO. A conceptual layout of the model plant is shown in Figure 26. The Sensor Technology MODULCO plant was designed to produce approximately 40 MW per year, or about 60 modules per hour. Six production lines will therefore be required to produce 200 megawatts per year, or 40 percent of the market.

A brief description of each of the seven selected process steps in the MODULCO model plant is given below:

(M-1) Solar Cell Interconnection (INCON)

In this process, solar cells are interconnected by means of a flexible printed circuit sheet.

(M-2) Module Lay-up (MDLAYUP)

Interconnected cells are layed-up with other materials for lamination. The arrangement for lay-up is glass/PVB/interconnected solar cells/PVB/Mylar.

(M-3) Degassing Process (DEGAS)

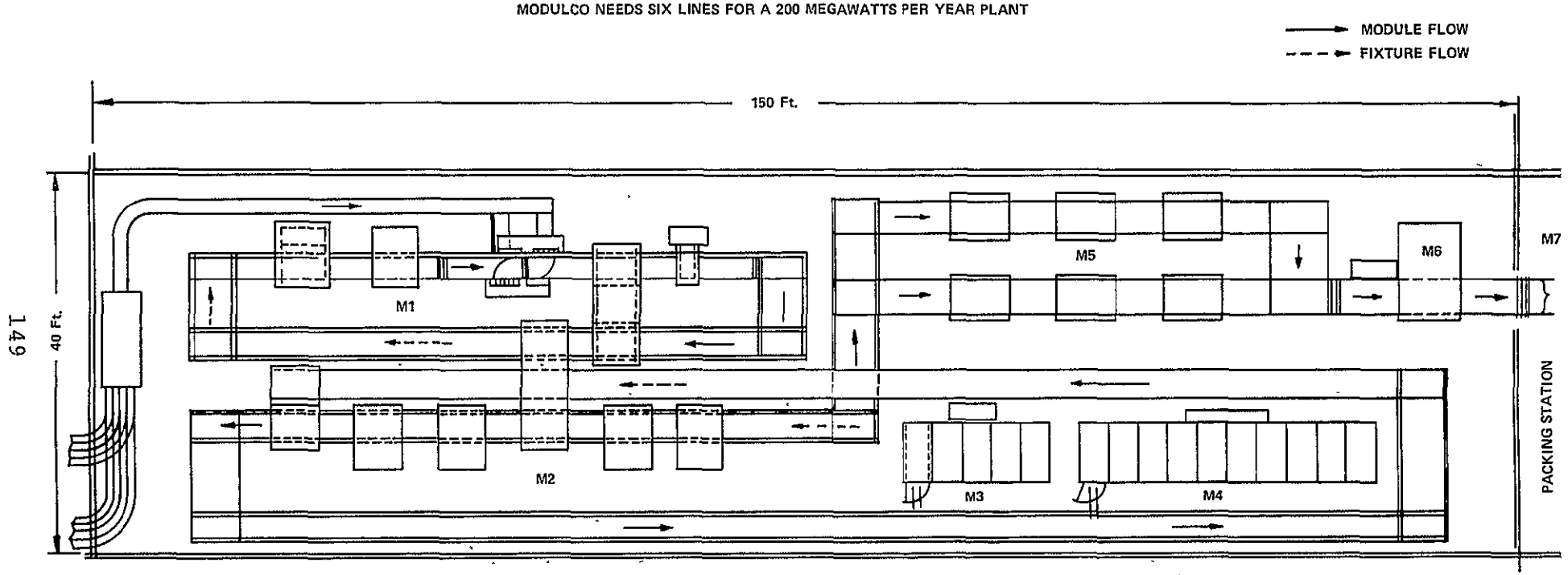
In this process step, module layers are heated to a predesignated temperature. Following the degassing procedure, module layers are placed into a special fixture which is subsequently

SENSOR TECHNOLOGY MODULCO PRODUCTION LINE

40 MEGAWATT PER YEAR CAPACITY

60 MODULES PER HOUR

MODULCO NEEDS SIX LINES FOR A 200 MEGAWATTS PER YEAR PLANT



M1 : INTERCONNECTION (1 UNIT)

M2 : LAY-UP STATION (1 UNIT)

M3 : DEGAS STATION (5 CHAMBERS)

M4 : AUTOCLAVE (10 CHAMBERS

M5 : FRAME ASSEMBLY STATIONS (2 LINES)

M6 : MODULE TEST STATION (1 UNIT)

M7 : PACKING AND STORAGE

transported by conveyor to the autoclave process.

(M-4) Autoclave Encapsulation (ENCAP)

The encapsulation process completes the module lamination by heating the module layers under low pressure in an autoclave

(M-5) Frame Assembly (FRMASEM)

The laminated module is framed in an aluminum frame with the use of a suitable sealant material. Terminals are then mounted onto the aluminum frame, for connection with the module terminal wires.

(M-6) Module Testing (MDLTEST)

The electrical performance of the framed modules is evaluated at this process step.

(M-7) Packing and Storage (PKGMDL)

Modules are prepared for shipment at this process step.

b) Price Computation

The price of a solar cell module was determined after all the data in Format A's were compiled. The cost computation proceeded in accordance with the procedures outlined in the process work sheets and

and company work sheets described in Reference 6. Additional expense item information, which was not included in the cost account catalog in Reference 7, was found in currently available market price literature.

The cost for each module process step was manually calculated and is shown in Table 23. The cost for each step was further broken down into cost elements which include the cost for equipment, floor space, labor, material and by-products, and utilities in terms of 1975 cents per peak watt.

c) Discussion of Results

The total added value for MODULCO including the encapsulation material is 116.8 cents per peak watt in 1975 cents. This value is nearly an order of magnitude (ten times) higher than the IPEG price goal of 15.3 cents per peak watt set forth in Reference (5). As shown in Table 23, the primary cause for the high module cost is due to the high module material cost, which accounts for 111.7 cents per peak watt, which is equivalent to 96 percent of the total cost for MODULCO.

Table 23. MODULCO process cost summary (Plan A). Module is based on present technology. Costs are in 1975 cents per peak watt.

Process No.	Process Referent	Equipment	Floor Space	Labor	Material & by products	Utilities	TOTAL
M-1	INTCON	0.118	0.370	0.240	85.35 *	1.766	87.84
M-2	MDLAYUP	0.081	0.113	0.235	18.31 *	0.004	18.743
M-3	DEGAS	0.089	0.038	0.313	0	0.067	.507
M-4	ENCAP	0.228	0.073	0.083	0	0.380	.764
M-5	FRMASEM	0.007	0.110	0.055	7.581 *	0.002	7.755
M-6	MDLTEST	0.074	0.016	0.189	0	0.003	.282
M-7	PKGMDL	0.010	0.017	0.348	0.536	0	.911
TOTAL		0.607	0.737	1.463	111.777 *	2.222	116.806

*Highest Cost Element

A detailed breakdown of the module material costs is presented in Table 24. The single highest material cost element is the flexible printed circuit sheet, which accounts for 85.35 cents per peak watt. The encapsulation material alone, which includes the glass, PVB, Mylar, aluminum frame, sealant, terminals, and packing material, accounts for 26.42 cents per peak watt. This value is very high compared to the IPEG price goal of 2.7 cents per peak watt set forth for module encapsulation material in Reference (5).

An interesting aspect, not to be overlooked, is the cost of the module assembly process alone, which is the difference between the total module cost (116.8 cents) and the sum of the flexible printed circuit sheet (85.35 cents) and the encapsulation material cost (26.42 cents). The module assembly process cost is only 5.03 cents per peak watt. This value is less than one-half the cost of 12.6 cents per peak watt for the MODULCO module assembly process as defined by the IPEG price goal in Reference (5).

Table 24. Detailed breakdown of MODULCO module material costs (Plan A) in 1975 cents per peak watt.

Flexible PC Sheet	85.35¢
Lamination of Glass/PVB/Cell/ PVB/Mylar	18.31¢
Aluminum Frame, Sealant, Terminals	7.58¢
Packing Material	.53¢
TOTAL COST (1975 cents)	111.77¢

It can be concluded from the above results that the flexible printed circuit sheet interconnection scheme reduces the module assembly cost considerably; it was found, however, to be unfeasible due to the high cost of the flexible printed circuit sheet. It can also be concluded that the encapsulation material used in this program is too expensive and will not meet the 1986 IPEG price goals.

The module selling price (Plan A) based on present technology and on the work performed in this array automated assembly program was found to be 158.6 cents per peak watt in 1975 cents. The price was obtained by summing the added values of each company as shown in Table 25. The wafer price for WAFERCO, 22 cents per peak watt, was obtained from the 1986 IPEG price goal in Reference 5. The CELLCO price, 19.8 cents per peak watt, and the MODULCO price, 116.8 cents per peak watt, were obtained from the above results.

The total module selling price of 158.6 cents per peak watt is more than three times the 1986 IPEG price goal, which is 50 cents per peak watt. The module encapsulation materials, which are discussed above, were found to be the major contributing factors to the high module selling price. Recommended

Table 25. MODULCO Module selling price (Plan A) in 1975 cents per peak watt

WAFERCO	22
CELLCO	19.8¢
MODULCO	116.8¢
MODULE SELLING PRICE	158.6¢ / watt

encapsulation material modifications based on updated technology will be discussed in the following section.

d) Recommended Direct Material Modifications

The recommended MODULCO direct material modifications are listed below:

(1) The flexible printed circuit sheet should be replaced with a stamped copper strip on Kapton to reduce the price from $5.00/ft. to $0.25/ft.

(2) Replacement of PVB sheet with EVA, to reduce the price from $10.34/ft to $0.086/ft.

(3) The aluminum frame should be modified by changing its height and thickness to reduce the price from $0.38/ft. to $0.19/ft. Each of the above mentioned modifications are possible with updated technology.

e) Discussion of Results

The cost for each process step in MODULCO was computed with the inclusion of the above recommended direct material modifications and is shown in Table 26.

Table 26. MODULCO process cost summary (Plan B).
Module based on potential technology.
Costs are in 1975 cents per peak watt.

Process Number	Process Referent	Equipment	Floor Space	Labor	Material by products	Utilities	TOTAL
M-1	INTCON	0.118	0.370	0.240	4.268	1.766	6.762
M-2	MDLAYUP	0.081	0.113	0.235	14.080	0.004	14.513
M-3	DEGAS	0.089	0.038	0.313	0	0.067	.507
M-4	ENCAP	0.228	0.073	0.083	0	0.380	.764
M-5	FRMASEM	0.007	0.110	0.055	4.230	0.002	4.404
M-6	MDLTEST	0.074	0.016	0.189	0	0.003	.282
M-7	PKGMDL	0.010	0.017	0.348	0.536	0	.911
TOTAL		0.607	0.737	1.463	23.114	2.222	28.143

The total added value of MODULCO is 28.14 cents per peak watt in 1975 cents. This revised value is still much too high when it is compared to the IPEG price goal of 15.3 cents per peak watt in 1975 cents.

A detailed breakdown of the revised module module material costs (Plan B) is presented in Table 27. It can be seen from the table that the module encapsulation materials alone account for 18.85 cents per peak watt which is well above the IPEG price goal of 2.7 cents per peak watt for module encapsulation materials. The net module price without considering the encapsulation materials is 9.29 cents per peak watt which is well below the IPEG price goal of 12.6 cents per peak watt.

The module selling price (Plan B) based on potential technology was found to be 69.94 cents per peak watt in 1975 cents. The price was obtained by summing the added values of each company as shown in Table 28. The wafer price for WAFERCO, 22 cents per peak watt, was obtained from the 1986 IPEG price goal in Reference (5). The CELLCO price, 19.8 cents per peak watt, and the MODULCO price, 28.14 cents per peak watt, were obtained from the above results.

Table 27. Detailed breakdown of MODULCO module material costs (Plan B) in 1975 cents per peak watt.

Stamped Copper Strip	4.268¢
Lamination of Glass/EVA/Cell EVA/Mylar	14.08 ¢
Aluminum Frame, Sealant, Terminals	4.23 ¢
Packing Material	0.536¢
Total Cost (1975 cents)	23.114¢ / watt

Table 28. MODULCO module selling price (Plan B) in 1975 cents per peak watt.

WAFERCO	22.00¢
CELLCO	19.80¢
MODULCO	28.14¢
MODULE SELLING PRICE	69.94¢

The total module selling price of 69.94 cents per peak watt exceeds the 1986 IPEG price goal of 50 cents per peak watt in 1975 cents.

The major contributing factor for this cost over-run was the module encapsulation material costs. Since the encapsulation material task did not play a feature role in this program, it received only a cursory analysis. Consequently, it is recommended that future work be directed toward the development of alternative, low-cost encapsulation materials.

CONCLUSIONS AND RECOMMENDATIONS

This program for Phase 2 of the Array Automated Assembly Task has led to a number of conclusions and recommendations which are listed below by task:

1. Cell Test Data Acquisition

The solar cell test data acquisition system was shown to be able to measure automatically the solar cell electrical performance parameters (i.e. I_{sc}, V_{oc}, I_v, I_{cell} and V_{cell}) and to be extremely conducive to module assembly. The successful completion of this task resulted in an extension of this concept to solar cell and module data acquisition and storage, Task 13.

2. Plasma Etching of Resist

Plasma etching of thick film resist was found to be unfeasible since the processing time to remove a five mil thick film resist was found to take approximately 40 hours.

3. Laser Trimming and Holing Operation

Solar cells can be scribed and/or holed by laser without causing mechanical defects (i.e. micro-cracks) nor any major degradation in solar cell electrical performance. The operational simplicity, high yield factor, and demonstrated technological capability of the laserscribe equipment was indicative of the success

of the laser trimming and holing operation. This technique is highly recommended, however, in order to comply with the 1986 LSA production goals, it is essential that the laser trimming and holing operation be fully automated.

4. Wafer Surface Preparation

The silicon wafer surface preparation task demonstrated a low-cost, high throughput texturizing process readily adaptable to automation. This recommended process will contribute significantly to reducing the cost and increasing the solar cell and module efficiency, which is in line with the 1986 LSA goals.

5. Laser Scanning Inspection

The ASM ASIS (laser scanning) system has potential for use in the inspection of mechanical defects in silicon solar cells in view of the process cost. However, this system will require development in order to detect all types of solar cell defects.

6. Wafer Printing

A general review of currently available thick film printing equipment provided the indication that state-of-the-art technology can adequately transform the throughput capability of current printing machines to the elevated rate of 7200 wafers per hour. A tunnel dryer system is recommended for this high throughput process.

7. Low Pressure Vapor Metal Deposition

No manufacturers could be found during the scheduled time phase of this program task to have successfully performed copper depositions. Consequently, any conclusive results pertaining to the viability of this process is not reported.

8. Silicon Nitride A.R.Coating

The LFE System 8000 silicon nitride plasma deposition system with the inclusion of minor equipment modifications was shown to be consistent with the 1986 LSA pricing goals for the overal solar cell cost. The performance verification test of the silicon nitride A.R.coating process provided the result that texturized,

A.R.coated solar cells display a 14.1% improvement in electrical performance over identical solar cells without an A.R. coating. Performance verification tests also indicated, that an inprocess (after junction formation but prior to metallization) silicon nitride plasma deposition A.R.coating improves solar cell efficiency. It is recommended that a detailed and thorough investigation of the application of inprocess A.R.coatings for solar cells be performed.

9. Wafer Plating

A new electroless nickel plating system was installed and demonstrated a low-cost, high throughput process readily adaptable to automation. The electroless nickel wafer plating system is, therefore, highly recommended for the 1986 LSA solar cell industry.

10. Solder Coating and Flux Removal

A multiple wafer dipping method was investigated and operational parameters defined. The optimum temperature range providing solder coating uniformity using the multiple wafer dipping method was 500 to 550^{o}F. A flux removal method consisting of a three stage D.I. water cascade rinse

system with ultrasonic agitator in the first tank is highly recommended.

11. Cell Handling for Module Construction

A precision solar cell positioning system consisting of robot arms with multiple pick-up heads was deemed suitable for the 1986 array automated assembly system.

12. Laser Trimming and Holing Automation

A fully automated serial flow laser trimming and holing system was identified. It was shown to be a low-cost system which maintains a large volume throughput with high output yields. It is a highly recommended solar cell trimming and/or holing process.

13. Cell and Module Test and Data Storage

The solar cell and module test and data storage system was shown to be highly successful in all respects. The system was able to measure automatically the solar cell or module (also strings

of solar cells) electrical performance parameters (i.e. I(sc), V(oc), P(p), V(p), I(p), store the data and group the modules or solar cells according to selected current increments at peak power. Another conclusion which may be drawn from the experimental data is the existance of a one-to-one correspondence between the current utilized manual grouping method and the computerized grouping method. It can also be concluded that the computerized solar cell and module test and data storage system is capable of easily detecting a wide rage of solar cell and module current variations. An assessment of the far-reaching potential of the computerized solar cell and module test and data storage system has led to the expectation that it could immensely simplify the performance of statistical analysis and quality assurance in all areas of solar cell and module fabrication.

14. Module Construction Study

The hexagonal solar cell center hole interconnection concept involving the use of a flexible printed circuit sheet with notched out tabs was found to greatly simplify the cumbersome task of solar cell interconnection for solar cell string assembly. The

solar cell conceptual design calculations showed that the number of gridlines and the types of gridline patterns are relatively insensitive for an optimized amount of shadowing. This is due to the relatively low gridline ohmic loss. The flameless inert gas soldering method is recommended for use in the solar cell string assembly operation.

15. Spray-on Dopant Junction Formation

The spray-on dopant junction formation process offers excellent prospects for meeting the 1986 LSA goals. It is highly recommended. The semi-automated prototype equipment constructed in this program demonstrated very high wafer throughput and reasonably short processing time. Spray-on doped solar cells with efficiencies equal to standard diffused production cells, between 11% and 12% efficiencies, were produced. A sequential spray-on of the n front surface followed by a p^+ back surface can easily be performed, but a light dopant overlap occurs. The laser trimming operation or some other solar cell edge clean up technique is an essential procedure for improving the photovoltaic energy conversion efficiency of solar cells processed with

the spray-on dopant technique.

The mechanical parameter optimization study was highly effective in defining specific mechanical parameter values which lead to low cost, high efficiency solar cells. Several unexpected developments which were a direct outgrowth of this study appear to warrant further investigation and study. One such development includes an experimental correlation between dopant flow rates and hexagonal solar cell efficiencies. An additional development consists of an apparent correspondence between small efficiency data spreads and large dopant flow rates. As a further means of improving the efficiency of hexagonal spray-on dopant solar cells, it is recommended that an excess dopant removal step should be incorporated in the overall spray-on dopant process sequence.

16. Conveyorized Dopant Diffusion

Conveyorized dopant diffusion was investigated as an alternative dopant deposition technique. The performance verification test for this process yielded negative results. While this dopant process was not thoroughly investigated, sufficient cause was found to render this process unsuitable for our applications.

17. Module Model Fabrication Study

A unique hexagonal solar cell central hole interconnection concept involving the use of a flexible printed circuit sheet with notched-out tabs, and a PVB lamination procedure for module encapsulation, was demonstrated with the fabrication of a module model. This novel solar cell interconnection concept was found to greatly simplify the cumbersome task of solar cell interconnection for cell string assembly. The new module model requires more processing time and lower processing temperature than the more conventional (reference) module process (without a flexible printed circuit sheet). Further study with a prototype scale module to determine optimum fabrication parameters is recommended.

SAMICS Process Cost Conclusion

It can be concluded from a detailed SAMICS process cost analysis that the solar cell process costs and the module assembly costs (excluding the encapsulation material costs) are in line with the 1986 LSA cost goals.

A significant reduction in the solar cell process costs can be made by reducing the metallization and anti-reflective coating costs. Candidate procedures for these two processes respectively are spray-on metallization and spray-on anti-reflective coating.

The total module selling price of 69.94 cents per peak watt exceeds the 1986 LSA price goal of 50 cents per peak watt in 1975 cents. The major contributing factor for the cost over-run was the module encapsulation materials costs. Since the encapsulation material task did not play a featured role in this program, it received only a cursory analysis. Consequently, it is recommended that future work be directed toward the development of alternative, low-cost encapsulation materials.

LIST OF REFERENCES

1. G. T. Jones, DOE/JPL - 954565-77/1; 40 KW of Solar Cell Modules; Final Report: JPL Contract 954565; LSSA Project; Large Scale Production Task; December 1977; Sensor Technology, Inc.

2. G.T. Jones and S. Chitre, ERDA/JPL - 954605-78/5; Development of Low-Cost, High Energy-Per-Unit-Area Solar Cell Modules; Final Report; JPL Contract 954605; LSSA Project; Automated Array Assembly Task; April 1978; Sensor Technology, Inc.

3. Low-Cost Silicon Solar Array Project; Robert G. Forney; Project Manager; Jet Propulsion Laboratory; California Institute of Technology; Proceedings of the Second ERDA Semi-Annual Solar Photovoltaic Review Meeting; January 20-22, 1976 at Lake Buena Vista, Florida; Conf. 76031.

4. S. R. Chitre, The Conference Record of the Thirteenth IEEE Photovoltaic Specialists Conference - 1978, IEEE Press, p. 152 (1978).

5. R. G. Chamberlain and R. W. Aster, JPL-5101-33; "Interim Price Estimation Guidelines, A Precursor Adjunct to SAMIS III;" Jet Propulsion Laboratory, Pasadena, California; September 10, 1977.

6. R. G. Chamberlain; JPL-5101-15; "SAMICS (Solar Array Manufacturing Industry Costing Standards) Workbook"; Jet Propulsion Laboratory, Pasadena, California, September 1977.

7. SAMICS Support Study, Final Report, Volume I; "Cost Account Catalog;" ERDA/JPL-954800-77/2.1; Theodore Barry & Associates, Management Consultants; Los Angeles, New York, Atlanta, Chicago, September 1977.

8. R. G. Chamberlain; JPL-5101-44; "SAMICS Input Data Preparation (Solar Array Manufacturing Industry Costing Standards)"; Jet Propulsion Laboratory, Pasadena, California; September 30, 1977.

9. R. G. Chamberlain; JPL-5101-59; "SAMICS Usage Update No. 1;" Jet Propulsion Laboratroy, Pasadena, California, February 1, 1978.

10. S. S. Rhee, G. T. Jones, and K. L. Allison, DOE/JPL-954865-79/5; Phase 2 Array Automated Assembly Task; Annual Report; JPL Contract 954865; LSA Project, Automated Array Assembly Task, January 1979 by Sensor Technology, Inc.

11. S.S.Rhee, K.L.Allison, and G.T.Jones DOE/JPL-954865-79/5; Phase 2 of the Array Automated Assembly Task; SAMICS Annual Report; JPL Contract 954865, LSA Project, Automated Assembly Task, January 1979 by Sensor Technology, Inc. (unpublished).