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ELECTRICAL EVALUATION OF RCA MWS5001D RANDOM ACCESS MEMORY

JUNE 1979

AEROSPACE GROUPS
HUGHES
HUGHES AIRCRAFT COMPANY
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Volume 1

FINAL REPORT

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TEST ABSTRACT

Electrical characterization and qualification tests were performed on the RCA MWS5001D, 1024 by 1-bit, CMOS, random access memory. Characterization tests were performed on five devices. The tests included functional tests, AC and DC parametric tests, AC-parametric worst-case pattern selection test, determination of worst-case transition for setup and hold times, and a series of schmoo plots. The qualification tests were performed on 32 devices and included a 2000 hour burn-in with electrical tests performed at 0 hours and after 168 hours, 1000 hours, and 2000 hours of burn-in. The tests performed included functional tests and AC and DC parametric tests.

All of the tests in the characterization phase, with the exception of the worst-case transition test, were performed at ambient temperatures of 25°C, -55°C and 125°C. The worst-case transition test was performed at 25°C. The preburn-in electrical tests were performed at 25°C, -55°C, and 125°C. All burn-in endpoint tests were performed at 25°C, -40°C, -55°C, 85°C, and 125°C.

All tests were performed on a Tektronix S-3260 automated test system. Temperatures were controlled by a Temptronic TP450A thermal airstream unit.

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*Each appendix is a separate volume.

ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

This report documents the results of characterization and qualification tests performed on the RCA MWS5001D, 1024 by 1-bit, CMOS, random access memory. Test results are contained in the appendices of this report and include raw data, statistical analysis of the qualification data, and calculated deltas for all AC and DC qualification tests from the initial data to each of the end points.

The characterization tests included functional tests, AC parametric pattern selection tests, AC and DC parametric tests, worst-case transition determination for setup and hold times, and schmoo plots. The functional tests were performed on a pass/fail basis to verify that it was possible to write into and read from all memory array locations, and to assure uniqueness of all memory array locations. AC parametric pattern selection tests were performed to determine which memory test patterns would best determine worst-case performance for the individual AC parameters. The patterns selected were used in all subsequent AC parametric tests. The worst-case transition test determined whether return-to-zero or return-to-one timing produced worst-case results for the setup and hold time tests. AC parametric tests were performed to determine minimum operating values for individual AC parameters. The AC parametric tests were performed functionally, using standard memory test patterns. The DC parametric tests were all static measurements made by forcing specific conditions on the device and measuring a voltage or current. The schmoo plot tests were performed to determine if any interaction of device parameters existed.

Device qualification included the performance of environmental tests and a 2000-hour burn-in at JPL, with electrical test performed at Hughes Aircraft before burn-in and after 168, 1000, and 2000 hours of burn-in. The electrical tests performed as part of the qualification included functional and AC and DC parametric tests.

All of the tests were performed on a Tektronix S-3260 automated test system. The characterization tests were performed at ambient temperatures of 25°C, -55°C, and 125°C. The worst-case transition test was performed at ambient temperatures of 25°C, -55°C, and 125°C. All end-point data was taken at 25°C, -40°C, -55°C, 85°C, and 125°C.

2.0 DEVICE DESCRIPTION

The RCA MWS5001D is a 1024 by 1-bit, CMOS, random access memory, packaged in a 16-lead, ceramic, dual-in-line package. Brief descriptions of device operation and the functions of its external connections are given in paragraphs 2.1 and 2.2. See Figures 2-1 and 2-2 for terminal assignments and logic diagram.

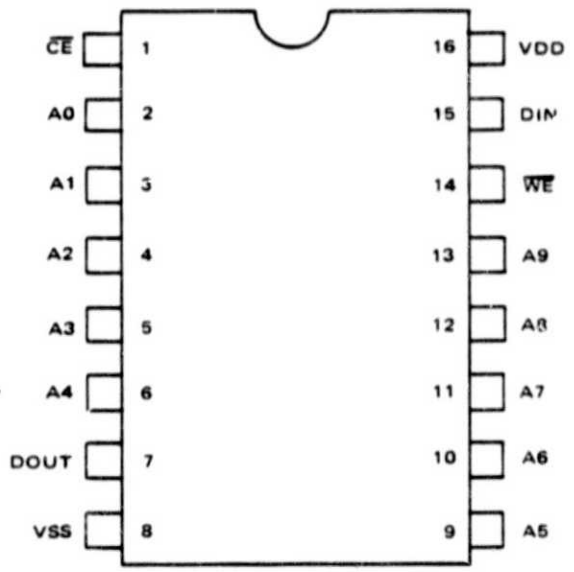

Figure 2-1. RCA MWS5001D terminal assignments.

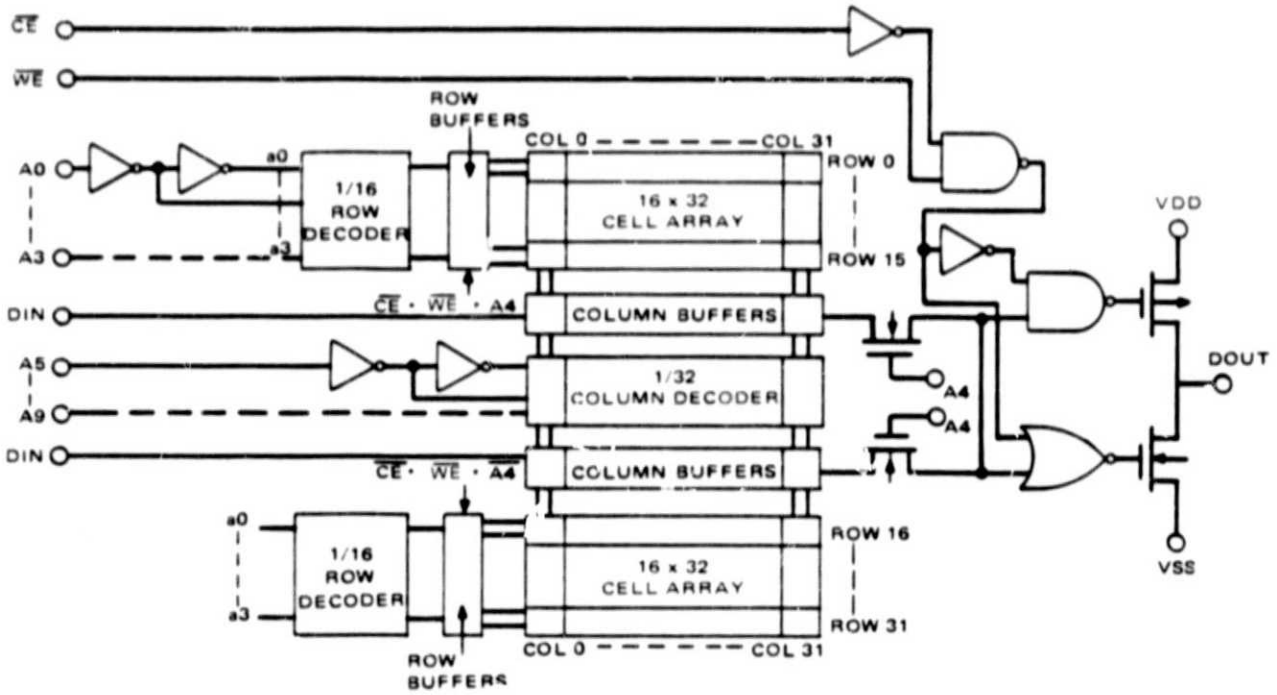

Figure 2-2. RCA MWS5001D logic diagram.

2.1 PIN DESCRIPTIONS

2.1.1 Cnip Enable ($\overline{CE}$) Input

The $\overline{CE}$ input is used to enable or disable the memory. When a logic "0" is applied to the $\overline{CE}$ input, the memory is enabled for a read or write operation. When a logic "1" is applied, the memory is disabled and the output is in a high-impedance state.

2.1.2 Write Enable ($\overline{WE}$) Input

The $\overline{WE}$ input controls write/read mode selection. When the $\overline{WE}$ input is high (logic "1"), the memory is in the read mode. When $\overline{WE}$ is low (logic "0"), the memory is in the write mode and the output is in a high-impedance state.

2.1.3 Data-In (DIN) Input

Data to be written into the memory array is entered through the DIN input. Positive logic is used (i.e., a low written into the memory is recognized as a low at the output when read from the memory).

2.1.4 Address (A0 through A9) Inputs

The address inputs are used to select one of 1024 possible memory array locations. Data may either be written into or read from the selected location in the memory, provided the memory has been enabled with $\overline{CE}$. $\overline{WE}$ must be in the proper logic state to select the desired mode of operation.

2.1.5 Data-Out (DOUT) Output

During a read operation, the data being read from the memory array is sampled at the DOUT output. The data output is in a high-impedance state if either $\overline{CE}$ is high (logic "1") and/or $\overline{WE}$ is low (logic "0").

2.2 DEVICE OPERATION

2.2.1 Write Mode

To write data into the memory array, $\overline{CE}$ must be in a logic "0" state. The desired address data must be present on the address inputs for time interval TAS (address setup time) before the $\overline{WE}$ high-to-low transition. The address data must remain at the selected address for time interval TAH (address hold time) after the $\overline{WE}$ low-to-high transition. The desired data must be present on the data input for the time interval TDS (data setup time) before the $\overline{WE}$ low-to high transition. The data must remain in the desired state for time interval TDH (data hold time) after the $\overline{WE}$ low-to-high transition. The $\overline{WE}$ input must be forced low (logic "0") for time interval TWP (write pulse width). See Figure 2-3 for timing diagram.

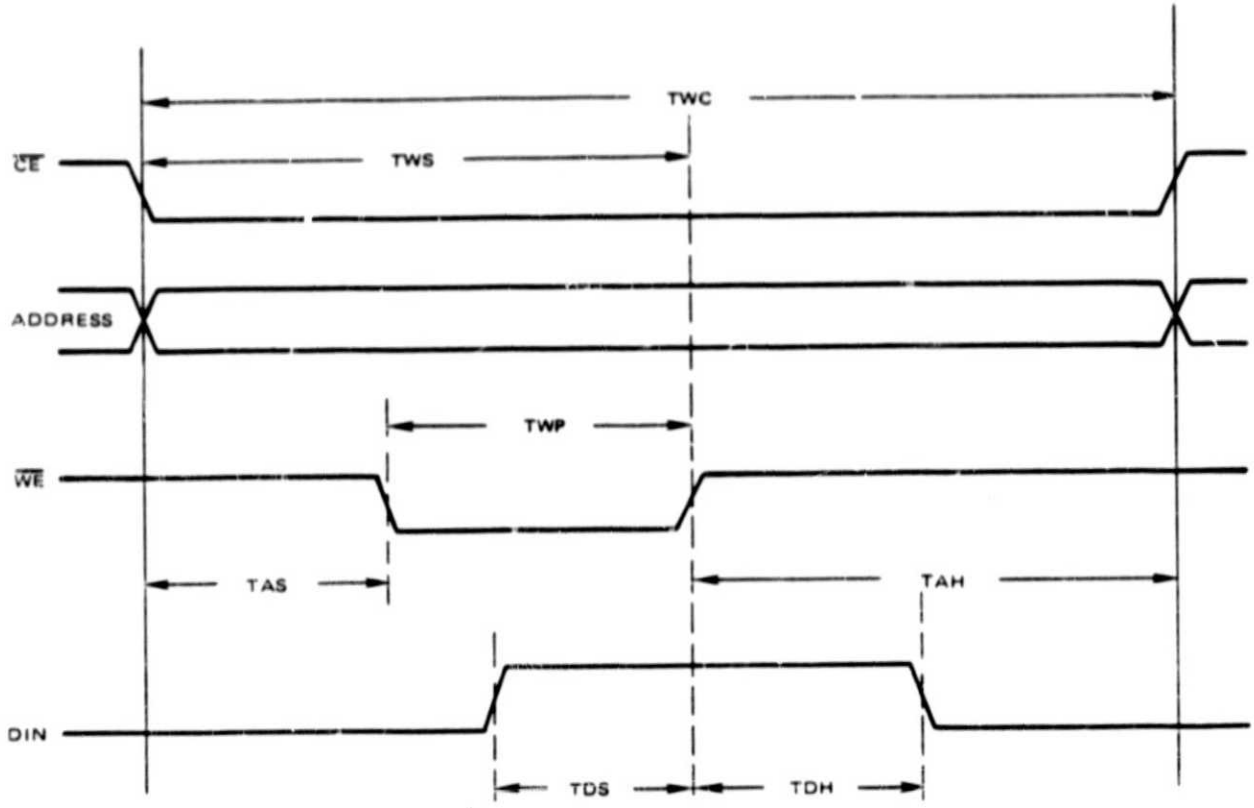

Figure 2-3. Write cycle timing diagram.

2.2.2 Read Mode

To read data from the memory array, $\overline{CE}$ must be in a logic "0" state and $\overline{WE}$ must be in a logic "1" state. The desired address data must be entered on the address inputs. Valid data will be available at the DOUT after time interval TAA (address access time). See Figure 2-4 for timing diagram.

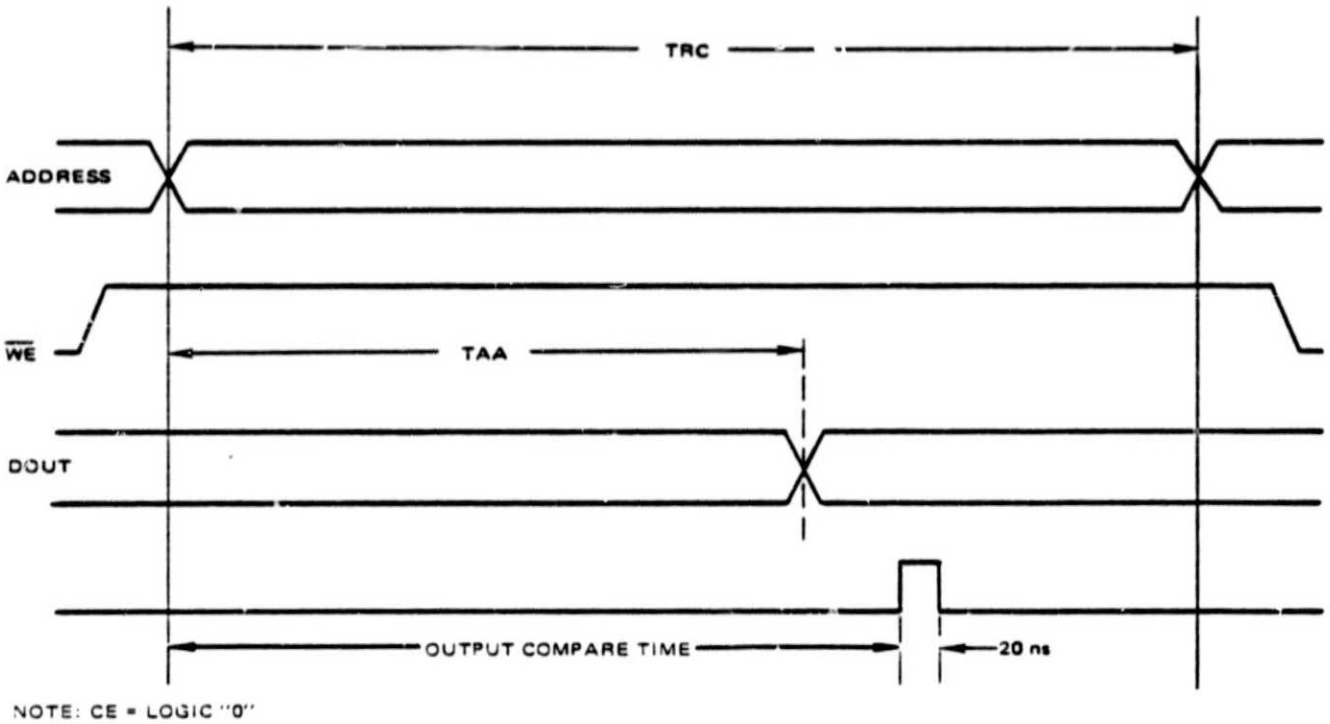

Figure 2-4. Read cycle timing diagram.

3.0 DESCRIPTION OF CHARACTERIZATION TESTS

3.1 PATTERN SELECTION

Pattern selection for the AC parametric tests was based on the results of AC parametric tests performed using a number of different memory test patterns. The patterns used were galpat, skip, walk, checkerboard, scan, and two diagonal patterns. Refer to Section 6.0 for detailed pattern descriptions and flow charts.

The patterns selected were those which produced the worst case data for a given AC parameter. If two or more patterns produced similar results, the pattern which was most time-efficient was selected. The patterns selected are listed in Table 3-1. Test results of the pattern selection are in Appendix A.

TABLE 3-1. AC-PARAMETRIC TEST PATTERNS

Parameter	Pattern
TAA	Skip
TDS	Checkerboard
TDH	Checkerboard
TWP	Diagonal
TAS	Checkerboard
TAH	Checkerboard
TWS	Diagonal
TRC	Diagonal*
TWC	Diagonal*

*The read and write portions of the diagonal pattern were divided into two separate patterns.

3.2 WORST-CASE TRANSITION FOR TAS, TAH, TDS, AND TDH

TAS (address setup time), TAH (address hold time), TDS (data setup time), and TDH (data hold time) were tested with return-to-zero (RZ) timing and return-to-one (RZI)* timing to determine the worst-case condition. The tests were performed on two devices (serial numbers 1 and 2). Based on the data obtained from this test, RZ timing was used on the address inputs for measuring TAS and TAH and on DIN (data-in) for measuring TDS and TDH. Refer to Table 3-2 for test results.

TABLE 3-2. WORST-CASE TRANSITION DATA

Parameter	Timing	Serial No. 1			Serial No. 2		
		VDD= 4.5V	VDD= 5.0V	VDD= 5.5V	VDD= 4.5V	VDD= 5.0V	VDD= 5.5V
TDS (ns)	RZ	16	14	12	12	12	14
	RZI	-8	-8	-10	-4	-6	-8
TDH (ns)	RZ	16	18	22	18	20	22
	RZI	2	2	2	0	2	2
TAS (ns)	RZ	14	16	16	10	12	12
	RZI	10	10	10	10	10	10
TAH (ns)	RZ	-6	-2	-2	-4	0	4
	RZI	-6	-2	0	0	2	4

*RZI = return-to-zero, invert (equivalent to return-to-one).

3.3 FUNCTIONAL TESTS

Three functional tests were performed. The first was a "dead or alive" test with conditions set well within the specified operating limits for the device. The second was a noise immunity test with input levels set to more critical values. The third functional test tested the device at more severe timing conditions. All functional tests were performed at a 5V supply voltage. The pattern used was galpat. Refer to Table 3-3 for test conditions and see Figure 3-1 for the timing diagram.

TABLE 3-3. FUNCTIONAL TEST CONDITIONS

Test Number	Test Conditions							
	VIH (V)	VIL (V)	Logic "0" Threshold (V)	Logic "1" Threshold (V)	Cycle Time	TWP (ns)	TDS (ns)	Output Compare Time (ns)
1	3.5	0	1	3	1 μs	200	400	800
2	3.0	0.8	1	3	1 μs	200	400	800
3	3.0	0.8	1	3	270ns	70	160	250

Note: $\overline{CE}$ = logic "0".

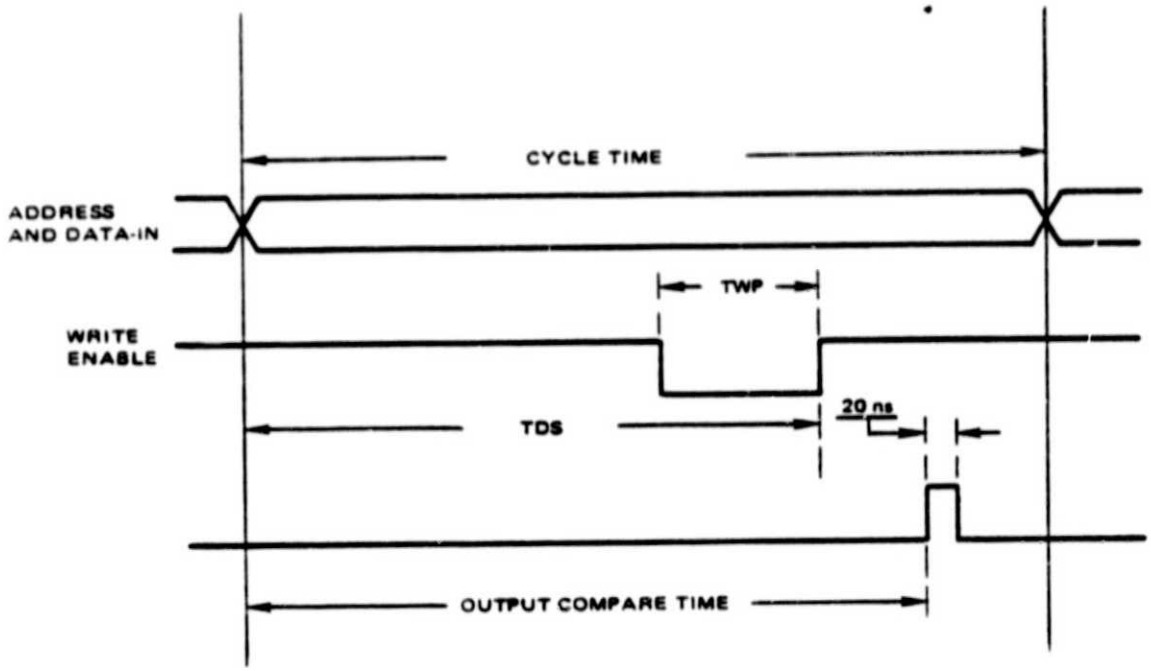

Figure 3-1. Functional timing diagram.

3.4 AC PARAMETRIC TESTS

All AC parameters were tested functionally using standard memory test patterns. The parameter of interest was set to a starting value, and a functional test was performed to determine whether the memory could function at the programmed value. If the memory failed, the parameter was incremented by 2 or 5ns, depending upon the parameter. This process was repeated until the memory passed the functional test or until the range of values for the parameter was exceeded. The value of the parameter was recorded at the time of successful completion of the functional test. If the range of values for the parameter was exceeded without the memory passing the functional test, a 1K default reading was recorded.

All parameters were measured at three supply voltages (4.5V, 5.0V, and 5.5V). The input logic levels were 3.5V for a logic "1" and 0V for a logic "0". The output compare levels were 3V-or-greater recognized as a logic "1" and 1V-or-less recognized as a logic "0". Timing conditions for the individual AC parametric tests are listed in Table 3-4. Test patterns used are listed in Table 3-1. A checkerboard pattern was used for TEN (output enable time). The output load was 50pF, including system and fixture capacitance, during these tests.

TABLE 3-4. AC-PARAMETER TIMING CONDITIONS

Parameter	Timing Conditions*								
	TDS (ns)	TDH (ns)	TWP (ns)	TAS (ns)	TAH (ns)	TWS (ns)	TAA (ns)	TEN (ns)	Compare Time
TDS	Varied from 0ns to 100ns in 2-ns incr	200	250	200	600	**	N/A	**	800ns
TDH	200	Varied from 0ns to 100ns in 2-ns incr	200	200	600	**	N/A	**	800ns
TWP	400	600	Varied from 20ns to 100ns in 2-ns incr	200	600	**	N/A	**	800ns
TAS	400	600	200	Varied from -20ns to 150ns in 2-ns incr	500	**	N/A	**	800ns
TAH	600	400	200	400	Varied from -20ns to 60ns in 2-ns incr	**	N/A	**	500ns
TWS	400	600	200	200	600	Varied from 0ns to 200ns in 2-ns incr	N/A	N/A	800ns
TAA	400	600	200	200	600	**	Varied from 50ns to 350ns in 5-ns incr	**	Same as TAA
TEN	900	100	200	700	100	N/A	N/A	Varied from 0ns to 200ns in 2-ns incr	800ns

Notes: *Cycle time = 1 μs.

**$\overline{CE}$ = logic "0".

3.4.1 Address Access Time (TAA) Test

The TAA test determined the maximum time required to access a memory array location from any other location in the memory. The measurement is made from the time the address data becomes stable until the output data becomes valid.

3.4.2 Data Setup Time (TDS) Test

The TDS test determined the minimum time before the WE low-to-high transition that stable data had to be present at the data input to assure proper write operation.

3.4.3 Data Hold Time (TDH) Test

The TDH test determined the minimum time after the $\overline{WE}$ low-to-high transition that stable data had to remain on the data inputs to assure proper write operation.

3.4.4 Write Pulse Width (TWP) Test

The TWP test determined the minimum time that the $\overline{WE}$ input had to remain low to assure a successful write operation.

3.4.5 Address Setup Time (TAS) Test

The TAS test determined the minimum time before the $\overline{WE}$ high-to-low transition that the address inputs had to be stable to assure that the desired memory location was being accessed.

3.4.6 Address Hold Time (TAH) Test

The TAH test determined the minimum time after the $\overline{WE}$ low-to-high transition that the address inputs had to remain stable to assure that the desired memory location was being accessed.

3.4.7 Chip Enable to Write Time (TWS) Test

The TWS test determined the minimum time required from the $\overline{CE}$ high-to-low transition to the $\overline{WE}$ low-to-high transition to assure a successful write operation.

3.4.8 Read Cycle Time (TRC) Test

The TRC test determined the minimum cycle time at which the memory could perform a successful read operation. A modified diagonal pattern was used to perform this test. In the modified pattern, the memory write and memory read portions of the diagonal pattern were divided into separate patterns to allow for unique timing conditions for the write and read cycles. Two separate patterns were used to prevent write cycle timing limitations from affecting the TRC measurement. Refer to Table 3-5 for timing conditions.

TABLE 3-5. TRC TIMING CONDITIONS

Parameter	Read Cycle	Write Cycle
Cycle time	Varied in 5-μs increments from 100ns to 500ns	1μs
TDS	N/A	400ns
TDH	N/A	600ns
TAS	N/A	200ns
TAH	N/A	600ns
TWP	N/A	200ns
Compare time	(cycle time) minus 20ns	N/A

3.4.9 Write Cycle Time (TWC) Test

The TWC test determined the minimum cycle time at which data could successfully be written into the memory array. As in the read cycle time test, a modified diagonal pattern was used. Two separate patterns were used to assure that read cycle timing limitations would not affect the TWC measurement.

To perform the TWC test, the memory was written with a background of zeros. The write timing conditions were well within the operating range of the memory to assure a successful write operation. Next, an attempt

was made to write a diagonal of ones into the memory using more severe timing conditions. The memory was then read to verify a successful write operation. If the write operation was unsuccessful, TWP was incremented by 5ns and the process was repeated. (Refer to Table 3-6 for timing conditions.) The value of TWC at the time of successful completion of a functional test was recorded. If the range of values for TWC was exhausted before completion of a successful functional test, a 1K default value was recorded.

TABLE 3-6. TWC TIMING CONDITIONS

Parameter	Read Cycle	Write Cycle (Loose Limits)	Write Cycle* (Tight Limits)
Cycle Time	1 μs	1 μs	***
TDS	N/A	400ns	TAS+TWP+10ns
TDH	N/A	600ns	Cycle-(TAS+TWP+10ns)
TAS	N/A	200ns	TAS+5ns
TAH	N/A	600ns	Cycle-(TAS+TWP+10ns)
TWP	N/A	200ns	TWP+5ns
Compare Time	800ns	N/A	N/A

Notes: * TAS and TWP refer to values previously measured for these parameters

*** Cycle time was varied in 5-ns increments from (TAS+TWP+10ns) or 80ns, whichever was greater, to 500ns.

3.4.10 Chip Enable Time (TEN) Test

The TEN test determined the propagation delay time from the $\overline{CE}$ high-to-low transition until the output became enabled (switched from a high-impedance state to a known state).

3.5 PLOTS

3.5.1 AC Parameters Versus Supply Voltage

Each of the following AC parameters was plotted as a function of VDD (supply voltage):

Address access time	(TAA)
Data setup time	(TDS)
Data hold time	(TDH)
Write pulse width	(TWP)
Address setup time	(TAS)
Address hold time	(TAH)
Chip enable to write time	(TWS)
Read cycle time	(TRC)
Output enable time	(TEN)

These plots show the minimum value of nine AC parameters as a function of VDD. VDD was varied from 4.5V to 5.5V in 100-mV increments. An AC parametric measurement was made for each setting of VDD.

The AC parameters were tested functionally using standard memory test patterns. The parameter of interest was set to a starting value, and a functional test was performed to determine whether the memory could function at the programmed value. If the memory failed, the parameter was incremented by 2 or 10 ns, depending upon the prameter. This process was repeated until the memory passed the test or until the range of values for the parameter was exceeded. Upon successful completion of a functional test, an asterisk was printed on the plot indicating the value of the AC parameter for the specific value of VDD.

For these tests, input logic levels were 3.5V for a logic "1" and 0V for a logic "0". The output compare levels were 3V-or-greater recognized as a logic "1" and 1V-or-less recognized as a logic "0". Refer to Table 3-7 for the timing conditions and test patterns used. An output load of 50pF was present during these tests.

TABLE 3-7. TEST CONDITIONS FOR AC-PARAMETERS-VERSUS-SUPPLY-VOLTAGE PLOTS

Test Conditions		AC Parameters			
		Address Access Time (TAA)	Write Pulse Width (TWP)	Data Setup Time (TDS)	Data Hold Time (TDH)
Timing Conditions	Address Inputs	Stable for Complete Cycle	Stable for Complete Cycle	Stable for Complete Cycle	Stable for Complete Cycle
	Data Inputs	Stable for Complete Cycle	Stable for Complete Cycle	Varied in 2-ns increments from 0ns to 40ns (TDH = 500ns)	Varied in 2-ns increments from 0ns to 40ns (TDS = 400ns)
	Write Enable Pulse Width (Write cycle)	200ns, starting from t0 + 200ns	Varied in 5-ns increments from 20ns to 150ns, starting from t0 + 200ns	200ns, starting from t0 + 200ns	200ns, starting from t0 + 200ns
	Chip enable input	Held at logic "0" for Complete Cycle	Held at logic "0" for Complete Cycle	Held at logic "0" for Complete Cycle	Held at logic "0" for Complete Cycle
	Compare Time	Varied in 10-ns increments from 50ns to 500ns	800ns	800ns	800ns
	Cycle Time	1 μs	1 μs	1 μs	1 μs
Test Pattern Used		Skip	Diagnonal	Checkerboard	Checkerboard

Note: *t0 indicates start of cycle

(Table 3-7, continued)

Test Conditions		AC Parameters				
		Address Setup Time (TAS)	Address Hold Time (TAH)	Chip Enable to Write Time (TWS)	Read Cycle Time (TRC)	Chip Enable Time (TEN)
Timing Conditions	Address inputs	Varied in 5-ns increments from 0ns to 100ns	Varied in 2-ns increments from 0ns to 60ns	Stable for complete cycle	Stable for complete cycle	Stable for complete cycle
	Data input	Stable for complete cycle	Stable for complete cycle	Stable for complete cycle	Stable for complete cycle	Stable for complete cycle
	Write enable pulse width (write cycle)	200ns, starting from t0 + 200ns	200ns, starting from t0 + 400ns	200ns, starting from t0 + 200ns	Held at logic "1" for complete cycle	200ns, starting from t0 + 700ns
	Chip enable input	Held at logic "0" for complete cycle	Held at logic "0" for complete cycle	Varied in 2-ns increments from 10ns to 90ns	Held at logic "0" for complete cycle	500ns low-going pulse, starting from t0 + 500ns
	Compare time	800ns	500ns	800ns	Cycle time -20ns	Varied in 2-ns increments from 0ns to 100ns
	Cycle time	1 μs	1 μs	1 μs	Varied in 2-ns increments from 80ns to 500ns	1 μs
Test Pattern Used		Checkerboard	Checkerboard	Diagonal	Diagonal** (read only)	Checkerboard

Note: *t0 indicates start of cycle
**A diagonal pattern was written into the memory array before TRC was measured.

3.5.2 AC Parameters Versus Temperature

Each of the following parameters was plotted as a function of temperature:

Address access time	(TAA)
Write pulse width	(TWP)
Data setup time	(TDS)
Data hold time	(TDH)
Address setup time	(TAS)
Address hold time	(TAH)
Chip enable to write time	(TWS)
Read cycle time	(TRC)
Output enable time	(TEN)

These plots show the minimum value of nine AC parameters as a function of temperature. Temperature was varied from -55°C to 125°C in 20°C increments. An AC parametric measurement was made for each temperature. The AC parameters were tested functionally using memory test patterns. The parameter of interest was set to a starting value, and a functional test was performed to determine whether the memory could function at the programmed value. If the memory failed, the parameter was incremented by 2 or 5ns, depending upon the parameter. This process was repeated until the memory passed the test or until the range of values for the parameter was exceeded. Upon successful completion of the functional test, an asterisk was printed on the plot indicating the value of the AC parameter for that specific temperature.

For these tests, input logic levels were 3.5V for a logic "1" and 0V for a logic "0". The output threshold levels were 3V-or-greater recognized as a logic "1" and 1V-or-less recognized as a logic "0". Timing conditions and patterns used for these tests are listed in Table 3-8. An output load of 50pF was present during these tests.

TABLE 3-8. TEST CONDITIONS FOR AC-PARAMETER-VERSUS-TEMPERATURE PLOTS

Test Conditions		AC Parameters			
		Address Access Time (TAA)	Write Pulse Width (TWP)	Data Setup Time (TDS)	Data Hold Time (TDH)
Timing Conditions	Address Inputs	Stable for complete cycle	Stable for complete cycle	Stable for complete cycle	Stable for complete cycle
	Data Input	Stable for complete cycle	Stable for complete cycle	Varied in 2-ns increments from -20ns to 60ns (TDH = 200ns)	Varied in 2-ns increments from 0ns to 40ns (TDS = 100ns)
	Write enable pulse width (write cycle)	200ns, starting from t0 + 200ns	Varied in 2-ns increments from 20ns to 100ns, starting from t0 + 200ns	200ns, starting from t0 + 200ns	200ns, starting from t0 + 200ns
	Chip enable input	Held at logic "0" for complete cycle	Held at logic "0" for complete cycle	Held at logic "0" for complete cycle	Held at logic "0" for complete cycle
	Compare time	Varied in 5-ns increments from 50ns to 200ns	800ns	800ns	800ns
	Cycle time	1 μs	1 μs	1 μs	1 μs
Test Pattern Used		Skip	Diagonal	Checkerboard	Checkerboard

Note: t0 indicates start of cycle

(Table 3-8, continued)

Test Conditions		AC Parameters				
		Address Setup Time (TAS)	Address Hold Time (TAH)	Chip Enable to Write Time (TWS)	Read Cycle Time (TRC)	Chip Enable Time (TEN)
Timing Conditions	Address inputs	Varied in 2-ns increments from 0ns to 60ns (TAH = 500ns)	Varied in 2-ns increments from -20ns to 40ns (TAS = 600ns)	Stable for complete cycle	Stable for complete cycle	Stable for complete cycle
	Data input	Stable for complete cycle	Stable for complete cycle	Stable for complete cycle	Stable for complete cycle	Stable for complete cycle
	Write enable pulse width (write cycle)	200ns, starting from t0 + 200ns	200ns, starting from t0 + 400ns	200ns, starting from t0 + 200ns	Held at 3.5V for complete cycle	200ns, starting from t0 + 200ns
	Chip enable input	Held at logic "0" for complete cycle	Held at logic "0" for complete cycle	Varied in 2-ns increments from 20ns to 100ns	Held at logic "0" for complete cycle	Varied in 2-ns increments from 0ns to 100ns
	Compare time	800ns	500ns	800ns	Cycle time -20ns	800ns
	Cycle time	1 μs	1 μs	1 μs	Varied in 2-ns increments from 100ns to 200ns	1 μs
Test Pattern Used		Checkerboard	Checkerboard	Diagonal	Diagonal** (read only)	Checkerboard

Note: *t0 indicates start of cycle
**A diagonal pattern was written into the memory array before TRC was measured.

3.5.3 Supply Current Versus Cycle Time

This test plotted supply current as a function of cycle time. The cycle time was varied from 100ns to 1μs in 100-ns increments. Supply current was measured and plotted for each setting of cycle time. The current was measured while the device was being exercised. The address and DIN (data-in) inputs were forced to alternate logic states every cycle. The WE (write enable) input was forced to a logic "0" for a 50-ns interval during each cycle.

3.5.4 Schmoo Plots

Schmoo plots determine whether interdependence exists between two device parameters. They also provide information about the operating range of the device. Plots were performed on the following parameters:

TWP versus TAS
TWP versus TAH
TWP versus TDS
TWP versus TDH

Although the following is a description of TWP versus TDS, it is typical of the way in which all the schmoo plot tests were performed. TWP versus TDS was performed with DIN (data-in) on RZ (return-to-zero) timing. Both TWP and TDS were set to a starting value below their operating range. Refer to Table 3-9 for test conditions. TDS was incremented through a range of values until it reached a predetermined stop value. After each increment, a functional test was performed. If the functional test was passed, an asterisk was printed on the plot indicating that for those values of TWP and TDS the memory functioned properly. When the stop value for TDS was reached, TWP was incremented and TDS was reset to its starting value. The process described above was repeated until TWP reached its predetermined stop value plus one increment. At this point the test was terminated.

For the schmoo plot tests, the supply voltage was set to 5.0V. Input logic levels were 3.5V for a logic "1" and 0V for a logic "0". The output threshold levels were 3V-or-greater recognized as a logic "1" and 1V-or-less recognized as a logic "0". An output load of 50 pF was present during these tests.

TABLE 3-9. SCHMOO PLOT TEST CONDITIONS

Parameter	Test Conditions						
	TAS	TAH	TDS	TDH	TWP	Compare Strobe (Measured from Start of Cycle)	Pattern
TWP versus TAS	Varied from 0ns to 40ns in 2-ns incr	>780ns	>30ns	>880ns	Varied from 30ns to 80ns in 5-ns incr	800ns	Skip
TWP versus TAH	>780ns	Varied from 0ns to 40ns in 2-ns incr	>860ns	>100ns	Varied from 30ns to 80ns in 5-ns incr	800ns	Skip
TWP versus TDS	>320ns	400ns	Varied from 0ns to 40ns in 2-ns incr	500ns	Varied from 30ns to 80ns in 5-ns incr	800ns	Checkerboard
TWP versus TDH	>320ns	400ns	400ns	Varied from 0ns to 40ns in 2-ns incr	Varied from 30ns to 80ns in 5-ns incr	800ns	Checkerboard

Notes: Cycle Time = 1μs.
$\overline{CE}$ = logic "0".

3.6 DC PARAMETRIC TESTS

The following tests were performed in accordance with the test conditions in Tables 3-10 and 3-11.

VOL(output voltage low)

VOH(output voltage high

IOL(output leakage current)

IIL(input low current)

IIH(input high current)

ICC1B0(supply current)

ICC1B1(supply current)

ICC2B0(supply current)

ICC2B1(supply current)

The test conditions for the VOH test are listed under VOH1 in Table 3-11. VOH2 does not apply to the characterization phase of this program. Input currents were measured on all inputs, however only the average current was recorded.

TABLE 3-10. IIL AND IIH TEST CONDITIONS

Parameter	Symbol	VDD	Input Under Test	All Other Inputs
Input low current	IIL	5.5V	0V	0V
Input high current	IIH	5.5V	5.5V	5.5V

TABLE 3-11. DC-PARAMETRIC TEST CONDITIONS

Test	Symbol	Pin Tested	Current/Voltage Load	Test Conditions
Output voltage low	VOL	Data out	2mA	Logic "0" written into memory location 0, VDD = 4.5V, address inputs = 0V, data in = 0V, $\overline{CE}$ = 0V, $\overline{WE}$ = 3.5V
Output voltage high	VOH1	Data out	-1mA	Logic "1" written into memory location 0, VDD = 4.5V, address inputs = 0V, data in = 3.5V, $\overline{CE}$ = 0V, $\overline{WE}$ = 3.5V
Output voltage high	VOH2	Data out	-1mA	Logic "1" written into memory location 0, VDD = 5.0V, address inputs = 0V, data in = 3.5V, $\overline{CE}$ = 0V, $\overline{WE}$ = 3.5V
Output leakage current	IOL	Data out	5.5V	Logic "1" written into memory location 0, VDD = 5.5V, address inputs = 3.5V, data in = 3.5V, $\overline{CE}$ = 3.5V, $\overline{WE}$ = 3.5V
Supply current	IDD1B0	VDD	5.5V	Logic "0" written into all memory locations, all inputs at 0V
Supply current	IDD1B1	VDD	5.5V	Logic "1" written into all memory locations, all inputs at 0V
Supply current	IDD2B0	VDD	5.5V	Logic "0" written into all memory locations, all inputs at 5.5V
Supply current	IDD2B1	VDD	5.5V	Logic "1" written into all memory locations, all inputs at 5.5V

4.0 DESCRIPTION OF QUALIFICATION TESTS

Thirty-two devices were subjected to qualification tests with two additional devices (serial numbers 4 and 5) serving as controls. Serial numbers 6 through 35 were subjected to environmental and burn-in tests at JPL with electrical measurements performed at Hughes Aircraft at 0 hours and after 168, 1000 and 2000 hours of burn-in. The initial tests were performed at ambient temperatures of 25°C, -55°C and 125°C. The post-168-hour, 1000-hour, and 2000-hour tests were performed at ambient temperatures of 25°C, -40°C, -55°C, 85°C, and 125°C.

The test results are contained in the appendices of this report. The data includes the raw data (functional and AC and DC parametric data), statistical data, and calculated deltas.

4.1 FUNCTIONAL TESTS

The functional tests were performed as outlined in Paragraph 3.3.

4.2 AC PARAMETRIC TESTS

The AC parametric tests were performed as outlined in Paragraph 3.4.

4.3 DC PARAMETRIC TESTS

The following tests were performed in accordance with the test conditions specified in Tables 3-10 and 3-11.

VOL (output voltage low)
VOH1 (output voltage high)
VOH2 (output voltage high)
IOL (output leakage current)

IIL (input low current)

IIH (input high current)

IDD1B0 (supply current)

IDD1B1 (supply current)

IDD2B0 (supply current)

IDD2B1 (supply current)

Input currents were measured on all inputs, however only worst-case and average data was recorded.

5.0 DATA SUMMARY

5.1 DATA SHEET FORMAT

Test data which exceeded the specified limits were flagged with one of the following symbols: "<*" or "*". (TWC) write cycle time data preceeded by the symbol "<" indicates that TWC is actually less than the recorded value. The minimum measurable time (starting value) for TWC is either 80ns (test system minimum cycle time) or the sum of the previously recorded data for TAS and TWP plus 10ns, whichever is greater.

5.2 CHARACTERIZATION DATA SUMMARY (APPENDIX A)

5.2.1 AC and DC Parametric Data

The AC parametric test results were within specified limits with the exception of test results for serial number 3. TAA (address access time) for serial number 3 was considerably longer than the data for the other 4 characterization devices and exceeded the measurement range of 350 ns at -20°C and -55°C. The worst case TAA for the other devices was in the range of 160ns to 180ns. The slow TAA caused the TAH (address hold time) and TEN (output enable time) tests to fail because the output data was not stable in time for the output compare strobe. The output compare strobe placement was somewhat closer to the address transitions in these tests than in the other AC parametric tests.

Data obtained during characterization program preparation revealed that current measurements were not always repeatable. To some extent, test system noise of approximately ±4na contributed to this problem particularly when measuring currents below approximately 10na. However some

lack of repeatability also occurred at higher currents. This problem was investigated, but the cause was not determined. Because of time limitations further investigation was discontinued.

DC parametric tests revealed no problems with the output voltage tests, however several of the current readings were higher than the specified limits. The worst-case currents (125°C data) for the 5 characterization devices is listed in Table 5-1.

TABLE 5-1. WORST CASE CURRENT DATA

Parameter	Device Serial Numbers					Units
	1	2	3	4	5	
IOL	10.7	3.51	.67	21.6*	4.56	μA
IIL	-100	-165	-94.8	-240	-300*	nA
IIH	105	145	107	263	339*	nA
IDD1B0	96.4	311	115	727*	240	μA
IDD1B1	113	493	197	1130*	274	μA
IDD2B0	105	312	116	716*	421	μA
IDD2B1	90.9	408	158	838*	372	μA

Notes: *Worst case, results
Temperature = 125°C

5.2.2 AC Parameters Versus Voltage and Temperature

The AC parametric plots revealed that worst case performance for most of the AC parameters was at 125°C and VDD = 4.5V. Refer to Table 5-2 for exceptions.

TABLE 5-2. WORST CASE SUPPLY VOLTAGE AND TEMPERATURE FOR AC PARAMETRIC PLOTS

Parameter	Worst Case	
	Temperature	VDD (Supply Voltage)
TAS	-55°C	4.5V
TAH	Indepedent of temperature	5.5V
TDS	125°C	4.5V (minor change over the VDD range)
TDH	125°C (minor change over the temperature range)	5.5V

5.2.3 Schmoo Plots

Schmoo plots were performed on TAS (address setup time), TAH (address hold time), TDS (data setup time) and TDH (data hold time) versus TWP (write pulse width). TDS versus TWP was the only plot to show some interaction. The interaction between parameters was worst at -55°C and VDD = 4.5V. Data for TAS and TAH was not recorded.

5.3 QUALIFICATION DATA SUMMARY

Three devices failed during environmental testing at JPL and were not returned for further electrical end-point measurements. Serial numbers 24 and 29 were not returned after the pre burn-in electrical measurements, and serial number 32 was not returned after the 168 hour burn-in end-point measurements. Refer to Appendix B for the qualification data, Appendix C for the statistical data and Appendix D for the calculated deltas.

5.3.1 Functional Failures

Refer to Table 5-3 for a summary of functional failures. The functional data taken after the 168 hour burn-in is not consistent with the post 1000 and 2000 hour burn-in data. A number of the failures which

TABLE 5-3. FUNCTIONAL FAILURE SUMMARY

		Serial Number	7			9			16			18			19			22			23			31			32		
		Functional** Test Number	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3
End Points	Initial	25°C																									*	*	
		-40°C																											
		-55°C																									*	*	
		85°C																											
		125°C	*	*					*	*					*	*											*	*	
	168 Hr	25°C		*						*						*											*	*	
		-40°C																									*	*	
		-55°C								*																	*	*	
		85°C		*					*	*						*											*	*	
		125°C	*	*			*		*	*					*	*			*			*			*		*	*	
	1000 Hr	25°C								*																			
		-40°C																											
		-55°C																											
		85°C								*						*													
		125°C		*					*	*					*	*													
	2000 Hr	25°C								*			*			*													
		-40°C																											
		-55°C																											
		85°C		*					*	*			*			*													
		125°C	*	*			*		*	*		*	*		*	*													

Notes: *Failed functional test.

**Refer to Paragraph 3.3 and Table 3 for definitions.

occurred at post 168 hours did not repeat at post 1000 or 2000 hours. The inconsistency appears to be a result of test samples operating near their performance limits and test system resolution.

5.3.2 AC Parametric Data

Out of the 10 AC parametric tests performed TAA (address access time) and TAS (address setup time) most frequently exceeded the specified limits. Nine devices failed TAA at one or more of the end point tests. Fifteen devices failed TAS.

Other scattered failures occurred for TWC and TWS. The majority of the failures were at -40°C and -55°C and at VDD = 4.5V. The calculated deltas revealed no noticeable drift over the 2000 hours burn-in.

The post-168-hour data for TAS and TWS is erratic at lower temperatures and VDD = 4.5V. This data is not consistent with the initial data or the post 1000-hour and 2000-hour data. The problem appears to be test-system related.

5.3.3 DC Parametric Data

The DC parametric test revealed no problems with the output voltage tests however the IOL (output leakage current) and IIH (input high current) tests exceeded the specified limits for the majority of the devices at 85°C and/or 125°C. The supply current measurements exceeded the specified limits on three devices. The calculated deltas revealed no noticeable drift over the 2000 hour burn-in.

6.0 PATTERN DESCRIPTIONS

6.1 GALPAT (Figure 6-1)

Write a background of zeros into all memory addresses. Write a one into the first reference cell. Read the first background cell. Read the reference cell. Read the next background cell. Read the reference cell. Read the next background cell, continuing this sequence until all background cells have been checked. Write the reference cell to zero and write a one into the next reference cell. Repeat the process until all cells have been used as reference cell. Repeat the entire sequence using a background of ones.

6.2 CHECKERBOARD (Figure 6-2)

Write alternate one and zero into all memory locations while incrementing the address count from memory location zero to memory location 1024. Read alternate one and zero in all memory locations. Write alternate zero and one into all memory locations. Read alternate zero and one in all memory locations.

6.3 DIAGONAL (WRITE ONLY) (Figure 6-3)

Write zeroes into all memory locations. Write ones into all memory locations where the row and column address are equal.

6.4 DIAGONAL ROW/COLUMN PING-PONG READ (READ ONLY)(Figure 6-4)

Read the first cell in the diagonal, which becomes the reference cell for the row/column read. Read all the cells in the same row as the reference cell as follows: Read the reference cell. Read the first background cell in

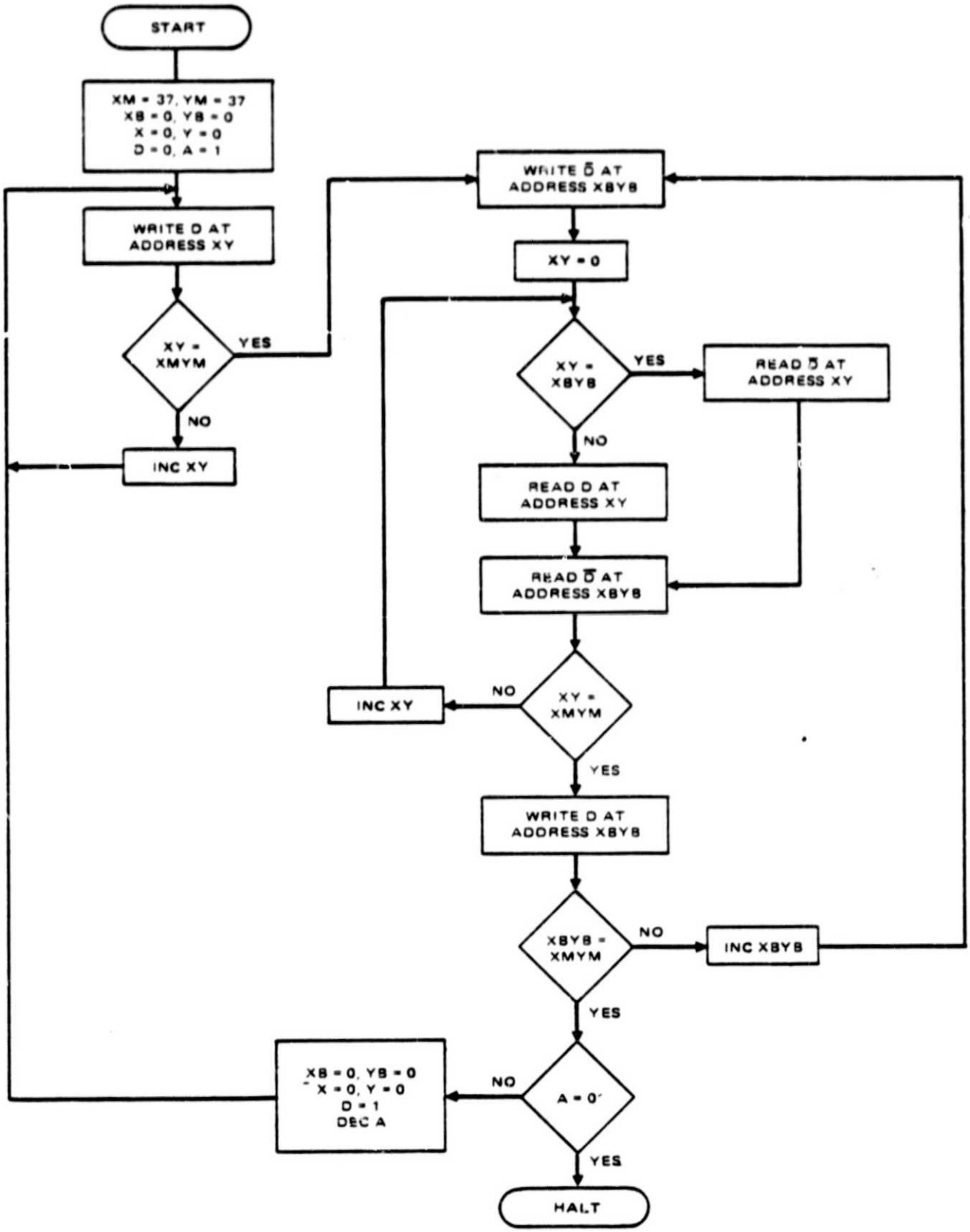

Figure 6-1. Galpat flow chart.

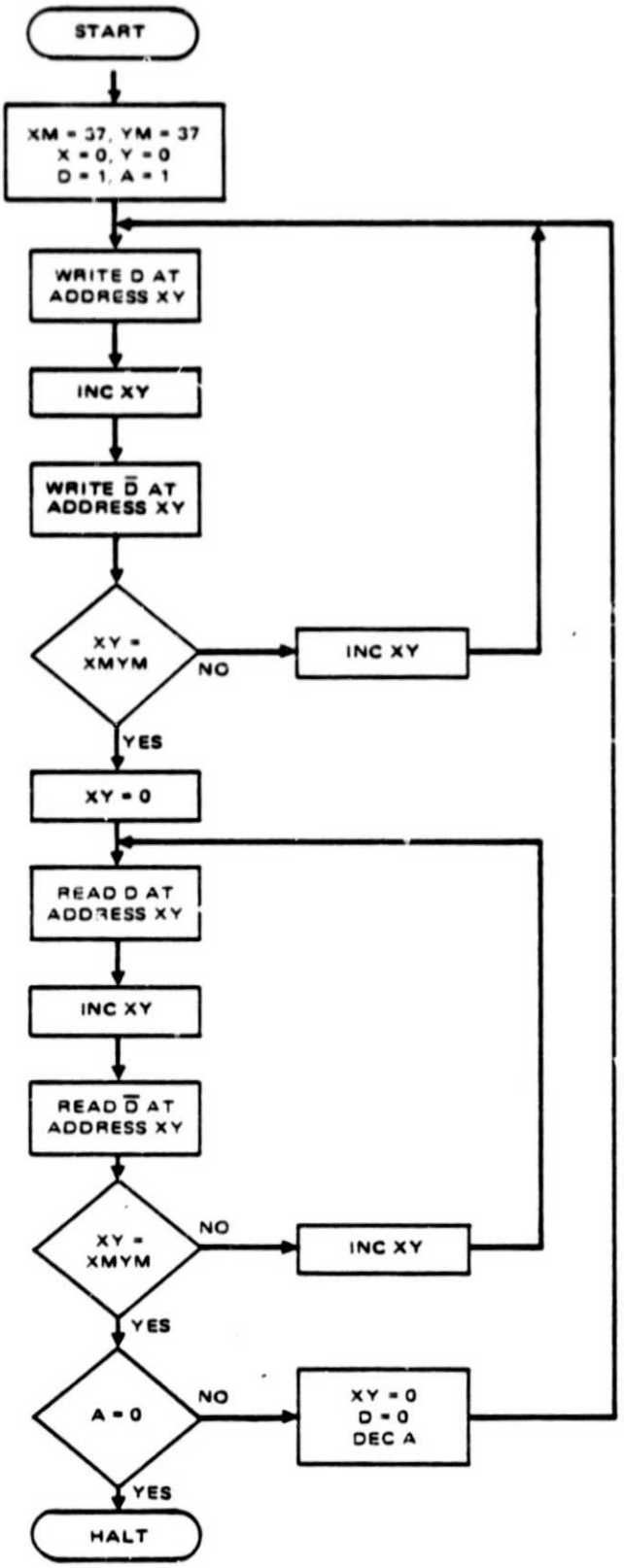

Figure 6-2. Checkerboard flow chart.

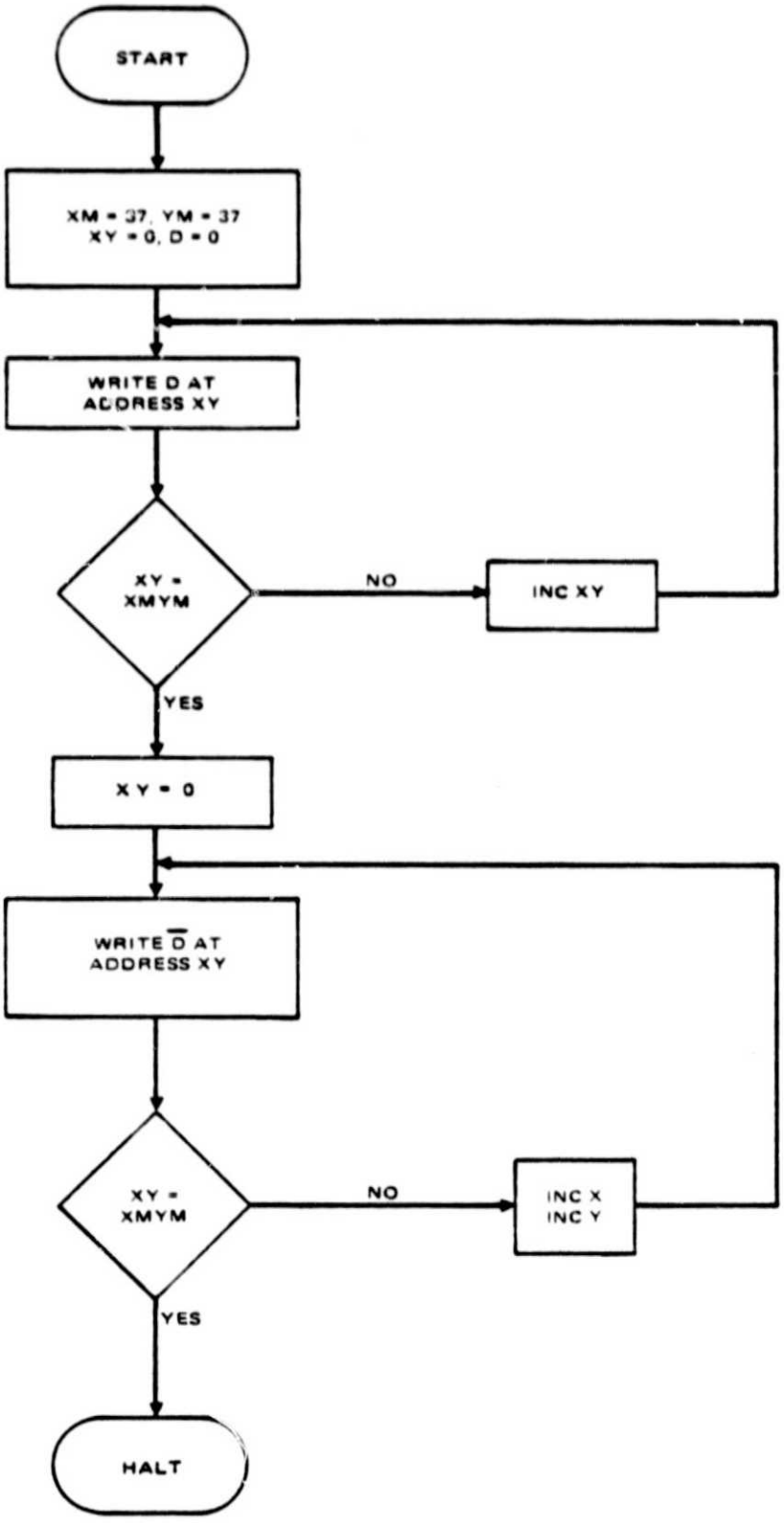

Figure 6-3. Diagonal (write only) flow chart.

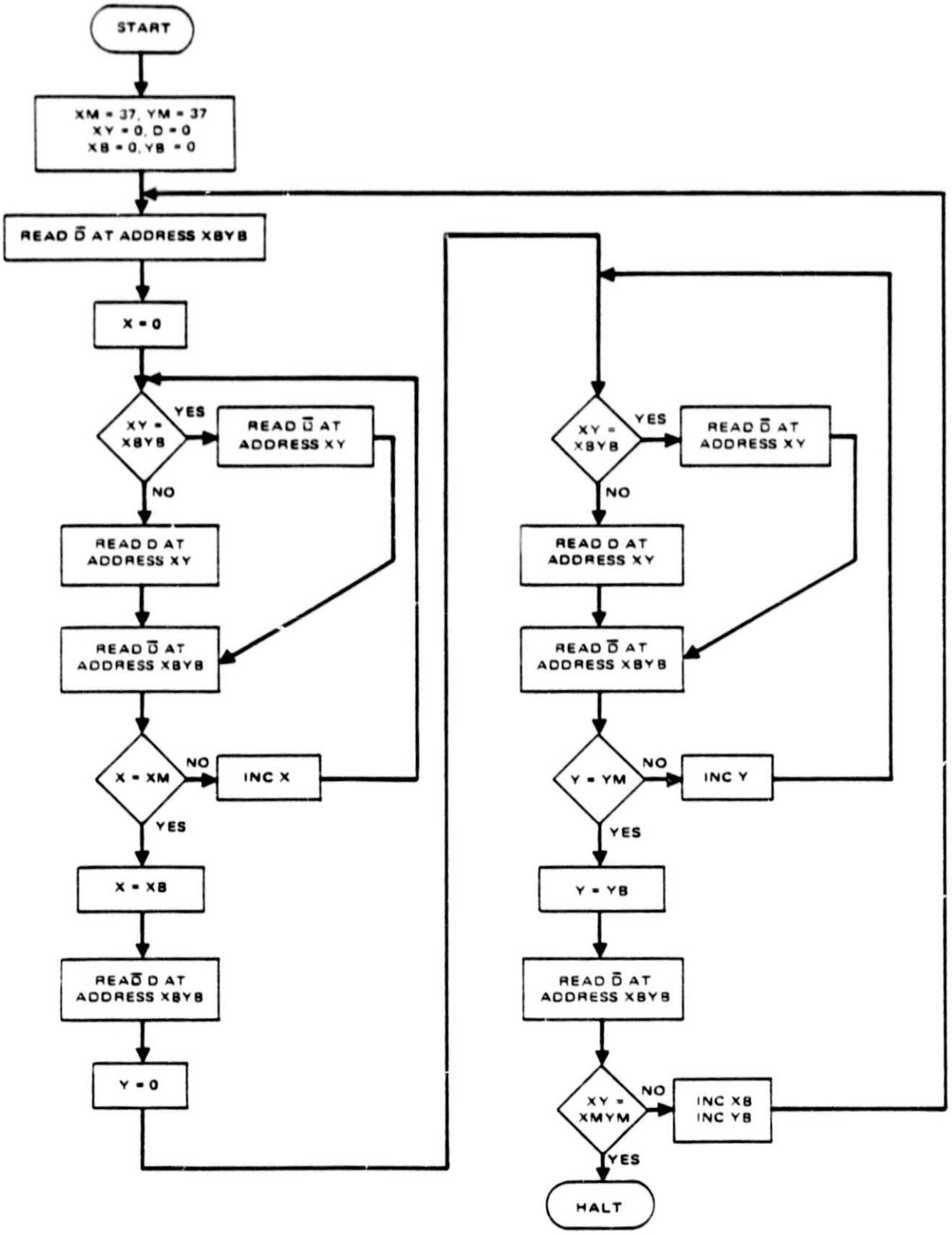

Figure 6-4. Diagonal row/column ping-pong read (read only) flow chart.

the row. Read the reference cell. Read the next background cell in the row. Continue this procedure until all the cells in the row have been read. Repeat the above procedure for all the cells that share the same column as the reference cell. Upon completion of reading the column, select the next cell in the diagonal as the reference cell and repeat the entire procedure. The above procedure is repeated until every cell in the diagonal has been selected for the reference cell once.

6.5 SKIP (ROW/COL GALPAT) (Figure 6-5)

Write a background of zeros. Write one into the first reference cell. Only background cells which share the same row or the same column as the reference cell are read. Read the first background cell in the row. Read the reference cell. Read the next background cell in the row, and continue this sequence until all the background cells in the row have been checked. Now repeat this process with all the cells that share the same column as the reference cell. Write the reference cell back to zero and write a one into the next reference cell. Repeat the process until all cells have been used as the reference cell. Repeat the entire sequence using a background of ones.

6.6 SCAN (Figure 6-6)

Write a zero in all memory locations. Read a zero in all memory locations. Write a one in all memory locations. Read a one in all memory locations.

6.7 WALK (Figure 6-7)

Write a background of zeros into all memory locations. Address zero becomes the reference cell. Write a one into the reference cell. Starting with the lowest address location, increment through all address locations read and compare with expected data. Read and compare the reference cell with the expected data. Write background data into the reference cell. Select the next higher memory location as reference cell. Write a one into the reference cell. Again read and compare all memory locations with expected data. Repeat this process until all memory cells

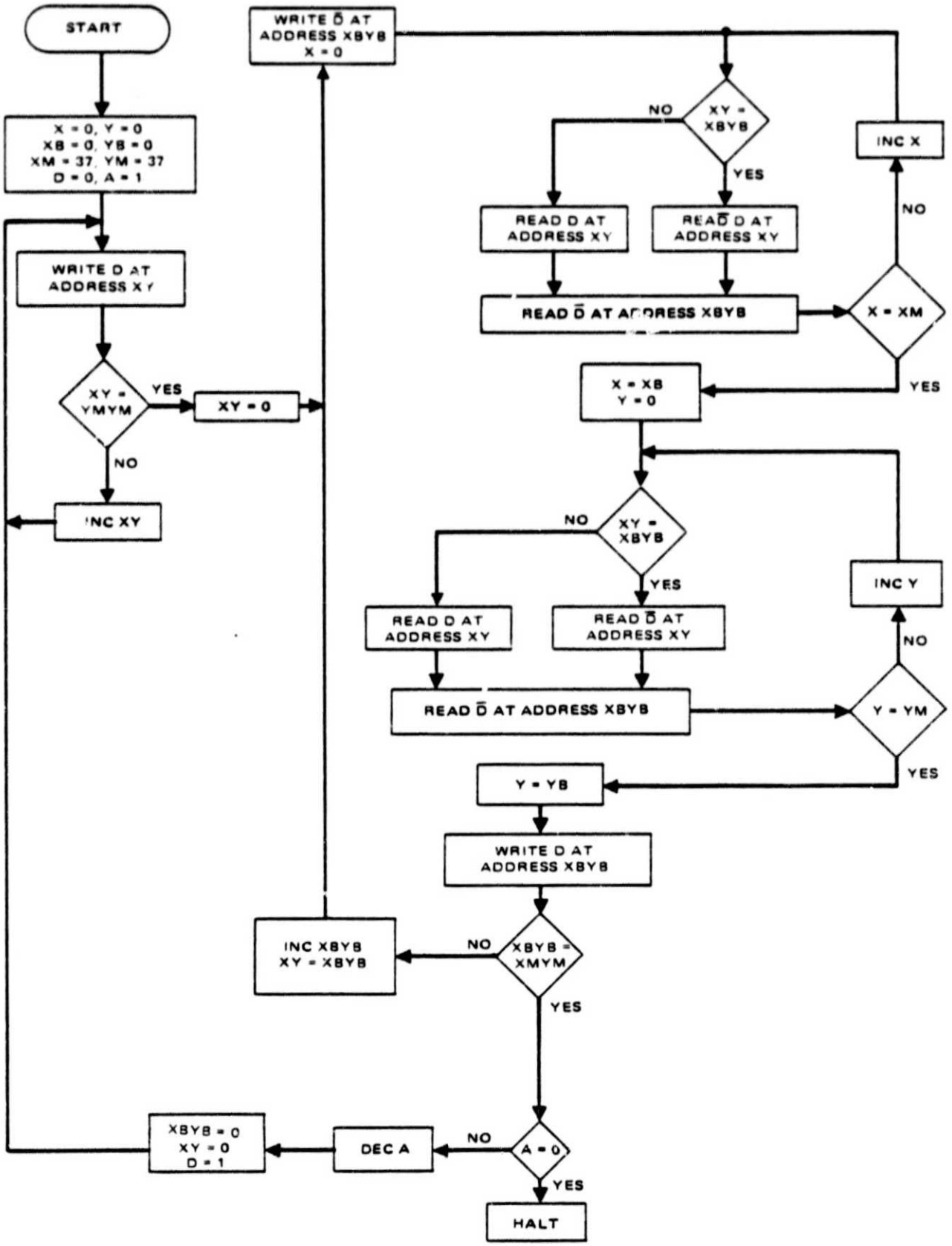

Figure 6-5. Skip (row/col galpat) flow chart.

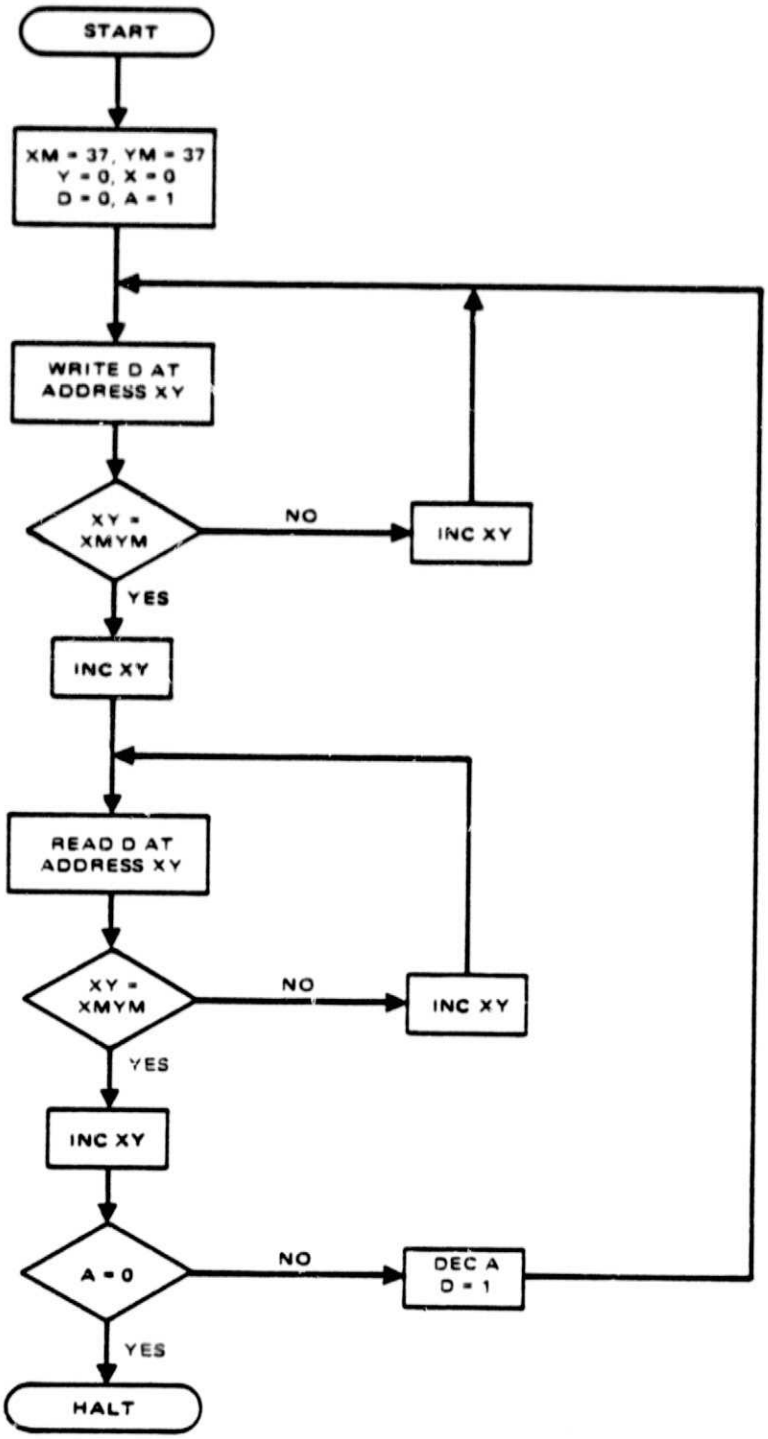

Figure 6-6. Scan flow chart.

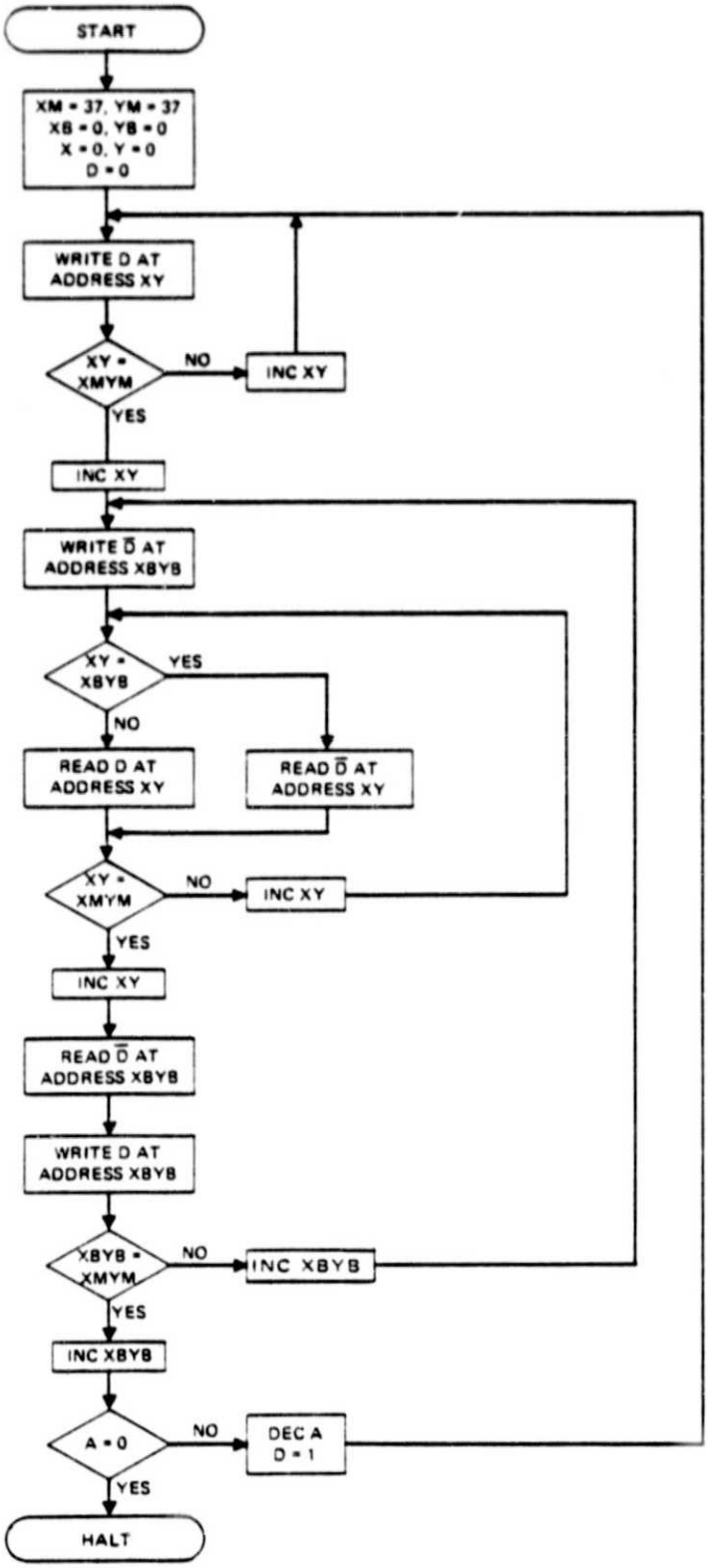

Figure 6-7. Walk flow chart.

have served as reference cell. Then repeat the whole process with a background of ones and the reference cells equal to zero.

6.8 DIAGONAL SCAN READ (Figure 6-8)

Write a background of zeros. Write a diagonal by writing ones into all memory addresses where X and Y addresses are equal. Read and compare all memory locations with expected data. Repeat the above process with a background of ones and a diagonal of zeros.

6.9 DIAGONAL ROW/COLUMN PING-PONG READ (Figure 6-9)

Write a background of zeros. Write a diagonal of ones by writing a one into all memory locations where row address equals column address. Read the first cell in the diagonal, which becomes the reference cell for the row/column read. Read all the cells in the same row as the reference cell as follows: Read the reference cell. Read the first background cell in the row. Read the reference cell. Read the next background cell in the row. Continue this procedure until all the cells in the row have been read. Repeat the procedure for all the cells that share the same column as the reference cell. Upon completion of reading the column, select the next cell in the diagonal as the referecne cell and repeat the entire procedure. The procedure is repeated until every cell in the diagonal has been selected for the reference cell once. Then repeat the entire procedure again, writing a background of ones and a diagonal of zeros.

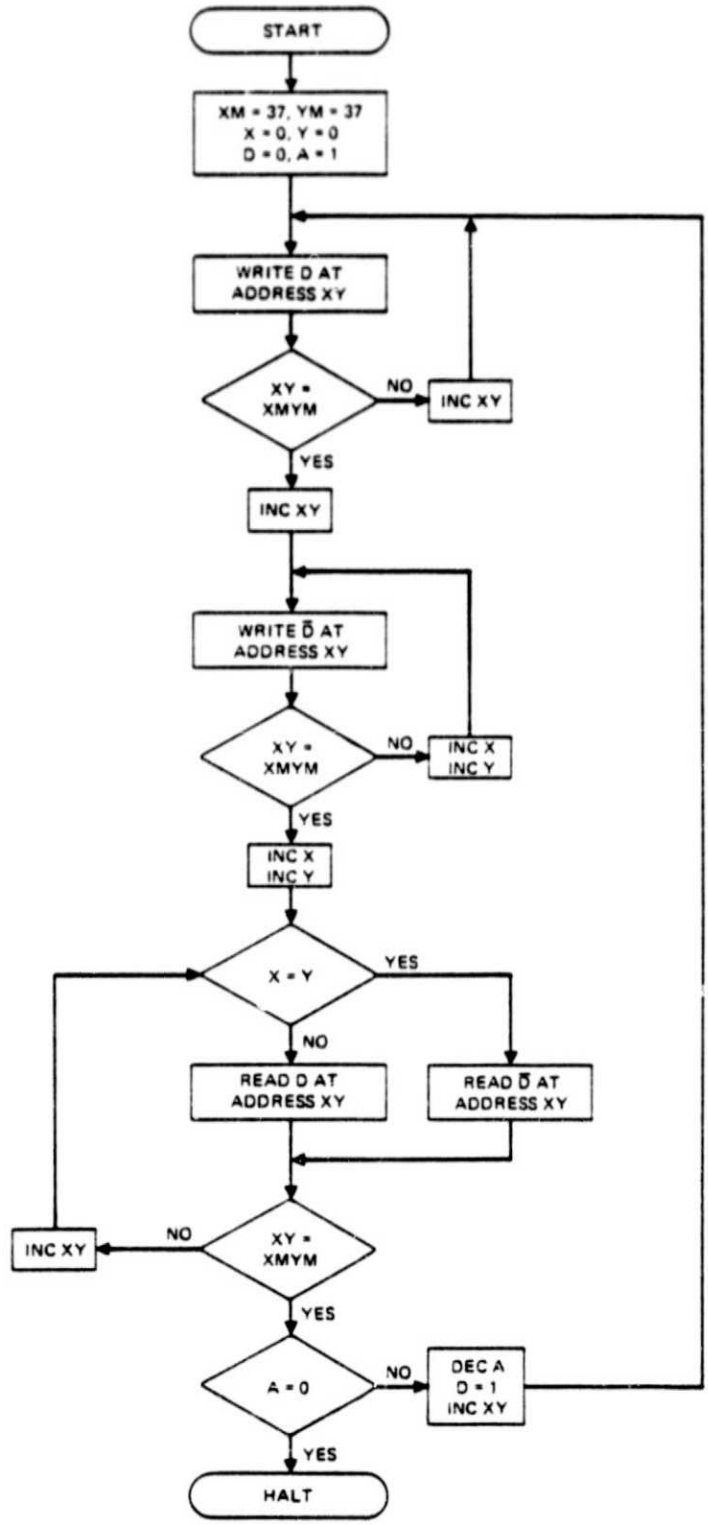

Figure 6-8. Diagonal scan read flow chart.

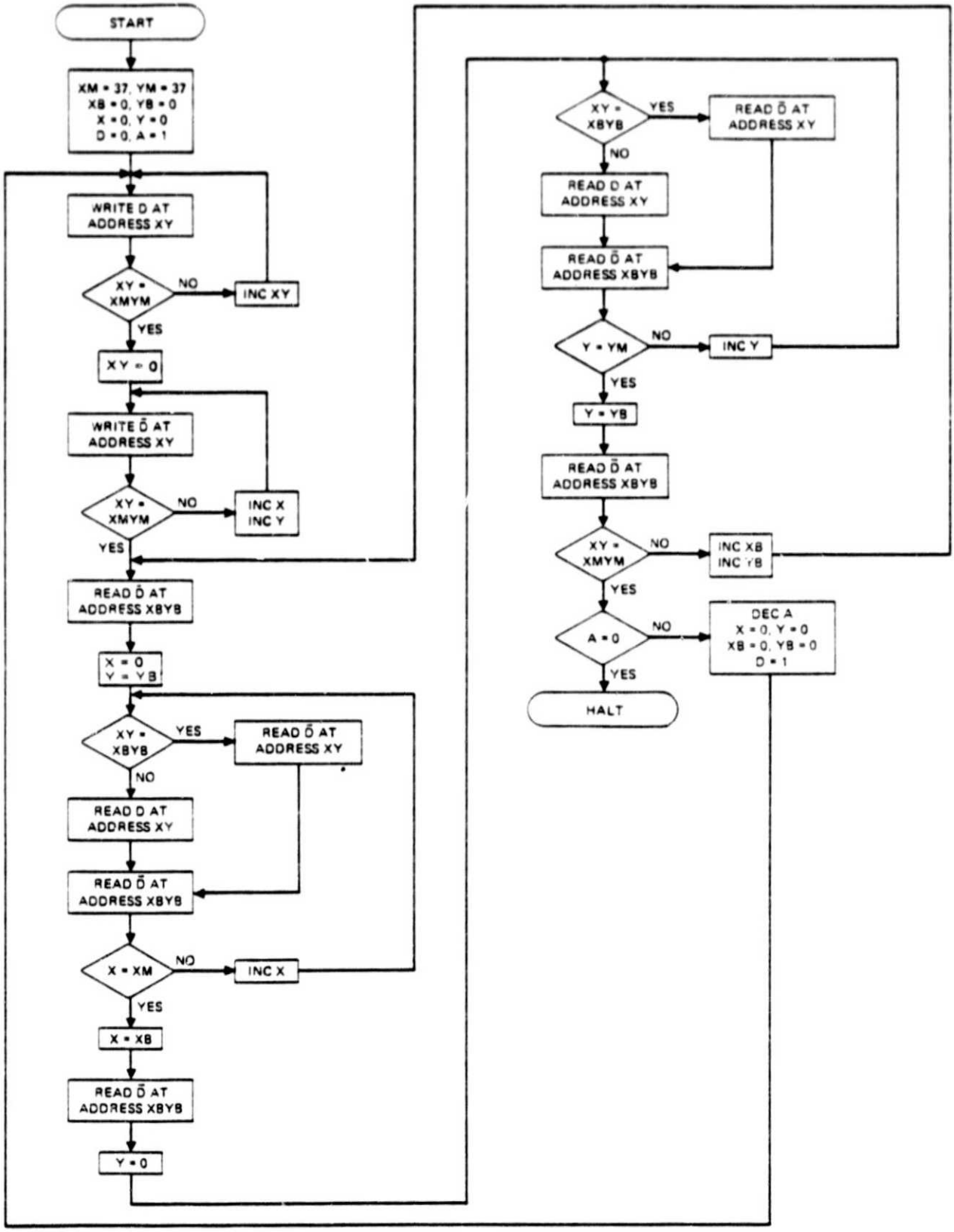

Figure 6-9. Diagonal row/column ping-pong read flow chart.