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AEROSPACE GROUPS

HUGHES

HUGHES AIRCRAFT COMPANY
CULVER CITY, CALIFORNIA



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ELECTRICAL CHARACTERIZATION OF THE RCA CDP1822SD RANDOM ACCESS MEMORY

Volume 2
FINAL REPORT
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(Appendix B and C)
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APPENDIX B

RAW DATA

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN:

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	315.N	255.N	95.0N
DATA SETUP TIME	(TDS)	38.0N	30.0N	10.0N
DATA HOLD TIME	(TDH)	10.0N	10.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	18.0N	14.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	144.N	118.N	56.0N
ADDRESS HOLD TIME	(TAH)	-28.0N	-22.0N	-6.00N
WRITE PULSE WIDTH	(TWP)	100.N	86.0N	44.0N
CS1 SETUP TIME	(TCSS1)	224.N	186.N	84.0N
CS2 SETUP TIME	(TCSS2)	218.N	182.N	82.0N
CS1 HOLD TIME	(TCSH1)	62.0N	54.0N	28.0N
CS2 HOLD TIME	(TCSH2)	66.0N	56.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	290.N	242.N	106.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	286.N	238.N	104.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	66.0N	58.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	166.N	132.N	38.0N
OUTPUT HOLD FROM CS2	(TDOH2)	160.N	128.N	38.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	120.N	38.0N
OUTPUT HOLD FROM MWR	(TPDH)	142.N	116.N	40.0N
READ CYCLE TIME	(TRC)	320.N	264.N	120.N
WRITE CYCLE TIME	(TWC)	312.N	272.N	136.N

	IIL	IIH	VIC1	VIC2
A0	-2.60NA	2.40NA	3.50 V	-3.51 V
A1	-2.60NA	2.70NA	3.52 V	-3.52 V
A2	-2.40NA	2.30NA	3.54 V	-3.57 V
A3	-2.70NA	2.70NA	3.53 V	-3.57 V
A4	-2.50NA	2.60NA	3.54 V	-3.57 V
A5	-2.40NA	3.00NA	3.45 V	-3.52 V
A6	-2.30NA	2.90NA	3.49 V	-3.50 V
A7	-2.60NA	2.50NA	3.47 V	-3.53 V
CS1	-2.60NA	2.60NA	3.51 V	-3.53 V
CS2	-2.70NA	2.60NA	3.56 V	-3.56 V
MWR	-2.80NA	2.50NA	3.49 V	-3.50 V
MRD	-2.40NA	2.40NA	3.51 V	-3.51 V
DI0	-2.30NA	2.30NA	3.61 V	-3.57 V
DI1	-2.40NA	2.40NA	3.61 V	-3.55 V
DI2	-2.70NA	2.80NA	3.60 V	-3.55 V
DI3	-2.50NA	2.40NA	3.59 V	-3.54 V

	DO0	DO1	DO2	DO3
VOL1	120.MV	120.MV	130.MV	125.MV
VOL2	120.MV	130.MV	145.MV	140.MV
VOH1	4.82 V	4.82 V	4.82 V	4.82 V
VOH2	9.76 V	9.76 V	9.75 V	9.76 V
IDN1	6.30MA	6.10MA	5.75MA	5.85MA
IDN2	15.7MA	14.8MA	13.2MA	13.6MA
IDP1	-2.13MA	-2.13MA	-2.10MA	-2.13MA
IDP2	-5.01MA	-5.03MA	-4.89MA	-5.05MA
IOZ1	21.6NA	22.8NA	20.3NA	22.3NA
IOZ2	24.6NA	19.2NA	23.8NA	19.0NA
IOZ3	19.0NA	23.4NA	20.2NA	21.8NA
IOZ4	17.9NA	24.8NA	18.6NA	24.5NA
IOZ5	25.0NA	18.1NA	25.8NA	17.6NA
IOZ6	25.2NA	18.2NA	25.7NA	17.4NA
IOZ7	24.9NA	18.3NA	25.9NA	17.3NA
IOZ8	25.1NA	17.8NA	25.6NA	17.4NA

ILDP	-10.0UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-5.00UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	335.N	260.N	90.0N
DATA SETUP TIME	(TDS)	44.0N	32.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	30.0N	20.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	146.N	118.N	50.0N
ADDRESS HOLD TIME	(TAH)	-26.0N	-20.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	112.N	92.0N	40.0N
CS1 SETUP TIME	(TCSS1)	228.N	186.N	78.0N
CS2 SETUP TIME	(TCSS2)	222.N	182.N	76.0N
CS1 HOLD TIME	(TCSH1)	58.0N	48.0N	20.0N
CS2 HOLD TIME	(TCSH2)	58.0N	50.0N	24.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	298.N	238.N	98.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	294.N	236.N	96.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	62.0N	52.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	156.N	124.N	54.0N
OUTPUT HOLD FROM CS2	(TDOH2)	154.N	120.N	54.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	56.0N
OUTPUT HOLD FROM MWR	(TPDH)	138.N	114.N	58.0N
READ CYCLE TIME	(TRC)	312.N	248.N	128.N
WRITE CYCLE TIME	(TWC)	320.N	256.N	128.N

	IIL	IIH	VIC1	VIC2
A0	-200.PA	200.PA	3.51 V	-3.51 V
A1	-300.PA	300.PA	3.53 V	-3.52 V
A2	-300.PA	200.PA	3.54 V	-3.56 V
A3	-300.PA	300.PA	3.53 V	-3.57 V
A4	-200.PA	300.PA	3.54 V	-3.57 V
A5	-300.PA	400.PA	3.46 V	-3.52 V
A6	-200.PA	400.PA	3.50 V	-3.50 V
A7	-300.PA	200.PA	3.48 V	-3.53 V
CS1	-300.PA	300.PA	3.51 V	-3.53 V
CS2	-400.PA	300.PA	3.56 V	-3.55 V
MWR	-400.PA	300.PA	3.50 V	-3.50 V
MRD	-200.PA	300.PA	3.51 V	-3.51 V
DI0	-200.PA	200.PA	3.61 V	-3.57 V
DI1	-200.PA	300.PA	3.61 V	-3.55 V
DI2	-300.PA	300.PA	3.60 V	-3.54 V
DI3	-300.PA	200.PA	3.59 V	-3.53 V

	DO0	DO1	DO2	DO3
VOL1	105.MV	105.MV	115.MV	110.MV
VOL2	105.MV	110.MV	125.MV	120.MV
VOH1	4.85 V	4.84 V	4.84 V	4.84 V
VOH2	9.80 V	9.79 V	9.79 V	9.80 V
IDN1	7.00MA	6.85MA	6.45MA	6.55MA
IDN2	17.8MA	17.0MA	15.2MA	15.7MA
IDP1	-2.55MA	-2.53MA	-2.48MA	-2.55MA
IDP2	-5.97MA	-5.96MA	-5.82MA	-6.04MA
IOZ1	1.60NA	6.80NA	700.PA	7.00NA
IOZ2	4.20NA	3.50NA	3.60NA	4.20NA
IOZ3	3.60NA	3.50NA	4.60NA	2.30NA
IOZ4	900.PA	7.20NA	1.10NA	5.80NA
IOZ5	7.30NA	900.PA	6.20NA	1.40NA
IOZ6	7.40NA	1.00NA	6.60NA	1.40NA
IOZ7	7.60NA	1.00NA	6.40NA	1.40NA
IOZ8	7.40NA	900.PA	6.60NA	1.30NA
ILDP	-5.00UA			
IL1	-5.00UA			
IL2	-5.00UA			
IL3	-5.00UA			
IL4	-5.00UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	330.N	250.N	85.0N
DATA SETUP TIME	(TDS)	58.0N	40.0N	10.0N
DATA HOLD TIME	(TDH)	8.00N	8.00N	8.00N
ADDRESS SETUP TIME	(TAS1)	34.0N	18.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	144.N	114.N	46.0N
ADDRESS HOLD TIME	(TAH)	-26.0N	-20.0N	-8.00N
WRITE PULSE WIDTH	(TWP)	104.N	94.0N	38.0N
CS1 SETUP TIME	(TCSS1)	232.N	174.N	76.0N
CS2 SETUP TIME	(TCSS2)	232.N	182.N	70.0N
CS1 HOLD TIME	(TCSH1)	74.0N	60.0N	24.0N
CS2 HOLD TIME	(TCSH2)	78.0N	62.0N	24.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	298.N	232.N	90.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	296.N	230.N	90.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	58.0N	50.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	152.N	116.N	32.0N
OUTPUT HOLD FROM CS2	(TDOH2)	148.N	114.N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	34.0N
OUTPUT HOLD FROM MWR	(TPDH)	138.N	112.N	30.0N
READ CYCLE TIME	(TRC)	288.N	232.N	120.N
WRITE CYCLE TIME	(TWC)	344.N	272.N	136.N

	IIL	IIH	VIC1	VIC2
A0	0.00 A	100.PA	3.54 V	-3.54 V
A1	-100.PA	100.PA	3.56 V	-3.55 V
A2	0.00 A	100.PA	3.57 V	-3.59 V
A3	-100.PA	100.PA	3.56 V	-3.60 V
A4	-100.PA	100.PA	3.57 V	-3.61 V
A5	-100.PA	100.PA	3.49 V	-3.55 V
A6	-100.PA	100.PA	3.53 V	-3.53 V
A7	-100.PA	100.PA	3.50 V	-3.56 V
CS1	-100.PA	100.PA	3.54 V	-3.54 V
CS2	-100.PA	100.PA	3.60 V	-3.59 V
MWR	-100.PA	100.PA	3.53 V	-3.54 V
MRD	0.00 A	100.PA	3.55 V	-3.54 V
DI0	0.00 A	0.00 A	3.63 V	-3.60 V
DI1	-100.PA	100.PA	3.63 V	-3.58 V
DI2	-100.PA	100.PA	3.63 V	-3.57 V
DI3	-100.PA	100.PA	3.62 V	-3.56 V

	D00	D01	D02	D03
VOL1	100.MV	100.MV	105.MV	105.MV
VOL2	95.0MV	100.MV	110.MV	110.MV
VOH1	4.87 V	4.87 V	4.87 V	4.87 V
VOH2	9.82 V	9.82 V	9.82 V	9.82 V
IDN1	7.60MA	7.45MA	7.05MA	7.15MA
IDN2	19.7MA	18.8MA	17.0MA	17.4MA
IDP1	-2.93MA	-2.92MA	-2.91MA	-2.94MA
IDP2	-6.89MA	-6.96MA	-6.80MA	-6.99MA
IOZ1	-1.00NA	5.70NA	-1.60NA	7.40NA
IOZ2	1.10NA	3.00NA	-600.PA	5.70NA
IOZ3	3.30NA	-700.PA	3.50NA	1.20NA
IOZ4	-100.PA	3.00NA	200.PA	4.60NA
IOZ5	3.10NA	600.PA	2.10NA	4.10NA
IOZ6	3.30NA	700.PA	1.60NA	4.10NA
IOZ7	2.80NA	800.PA	1.80NA	4.50NA
IOZ8	2.90NA	1.10NA	1.30NA	4.70NA

ILDP	-1.20UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-5.00UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	300.N	250.N	110.N
DATA SETUP TIME	(TDS)	40.0N	32.0N	10.0N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	10.0N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	144.N	126.N	64.0N
ADDRESS HOLD TIME	(TAH)	-26.0N	-22.0N	-8.00N
WRITE PULSE WIDTH	(TWP)	110.N	96.0N	50.0N
CS1 SETUP TIME	(TCSS1)	232.N	198.N	94.0N
CS2 SETUP TIME	(TCSS2)	226.N	194.N	92.0N
CS1 HOLD TIME	(TCSH1)	70.0N	62.0N	34.0N
CS2 HOLD TIME	(TCSH2)	76.0N	66.0N	34.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	292.N	252.N	122.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	288.N	248.N	118.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	70.0N	62.0N	34.0N
OUTPUT HOLD FROM CS1	(TDOH1)	170.N	136.N	44.0N
OUTPUT HOLD FROM CS2	(TDOH2)	164.N	134.N	46.0N
OUTPUT HOLD FROM MRD	(TDOH3)	144.N	122.N	40.0N
OUTPUT HOLD FROM MWR	(TPOH)	144.N	120.N	42.0N
READ CYCLE TIME	(TRC)	328.N	272.N	128.N
WRITE CYCLE TIME	(TWC)	280.N	256.N	164.N

	IIL	IIH	VIC1	VIC2
A0	-42.9NA	42.8NA	3.53 V	-3.54 V
A1	-42.7NA	43.0NA	3.55 V	-3.55 V
A2	-42.0NA	41.8NA	3.58 V	-3.61 V
A3	-43.3NA	43.4NA	3.56 V	-3.61 V
A4	-40.9NA	41.8NA	3.57 V	-3.61 V
A5	-42.4NA	44.2NA	3.48 V	-3.54 V
A6	-41.1NA	43.4NA	3.52 V	-3.52 V
A7	-42.9NA	42.0NA	3.51 V	-3.56 V
CS1	-42.1NA	41.8NA	3.54 V	-3.57 V
CS2	-41.5NA	43.4NA	3.59 V	-3.59 V
MWR	-42.5NA	41.3NA	3.51 V	-3.53 V
MRD	-41.2NA	41.0NA	3.54 V	-3.54 V
DI0	-40.5NA	41.4NA	3.63 V	-3.61 V
DI1	-40.7NA	41.6NA	3.64 V	-3.58 V
DI2	-40.9NA	42.1NA	3.63 V	-3.59 V
DI3	-41.0NA	41.5NA	3.62 V	-3.57 V

	D00	D01	D02	D03
VOL1	135.MV	140.MV	150.MV	150.MV
VOL2	145.MV	155.MV	170.MV	165.MV
VOH1	4.78 V	4.78 V	4.78 V	4.78 V
VOH2	9.70 V	9.70 V	9.69 V	9.71 V
IDN1	5.45MA	5.30MA	4.95MA	5.05MA
IDN2	13.3MA	12.5MA	11.2MA	11.5MA
IDP1	-1.80MA	-1.80MA	-1.78MA	-1.81MA
IDP2	-4.22MA	-4.26MA	-4.13MA	-4.27MA
IOZ1	164.NA	177.NA	162.NA	168.NA
IOZ2	161.NA	171.NA	168.NA	162.NA
IOZ3	158.NA	173.NA	164.NA	163.NA
IOZ4	162.NA	166.NA	171.NA	161.NA
IOZ5	161.NA	172.NA	170.NA	164.NA
IOZ6	174.NA	163.NA	167.NA	170.NA
IOZ7	161.NA	176.NA	161.NA	169.NA
IOZ8	164.NA	165.NA	173.NA	164.NA
ILDP	5.00UA			
IL1	-25.0UA			
IL2	-30.0UA			
IL3	-25.0UA			
IL4	-20.0UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	310.N	265.N	120.N
DATA SETUP TIME	(TDS)	38.0N	32.0N	12.0N
DATA HOLD TIME	(TDH)	14.0N	14.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	6.00N	6.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	152.N	136.N	72.0N
ADDRESS HOLD TIME	(TAH)	-28.0N	-24.0N	-10.0N
WRITE PULSE WIDTH	(TWP)	114.N	100.N	54.0N
CS1 SETUP TIME	(TCSS1)	236.N	204.N	102.N
CS2 SETUP TIME	(TCSS2)	230.N	198.N	100.N
CS1 HOLD TIME	(TCSH1)	74.0N	64.0N	36.0N
CS2 HOLD TIME	(TCSH2)	78.0N	68.0N	36.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	310.N	268.N	134.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	304.N	264.N	130.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	74.0N	66.0N	36.0N
OUTPUT HOLD FROM CS1	(TDOH1)	170.N	140.N	50.0N
OUTPUT HOLD FROM CS2	(TDOH2)	166.N	136.N	50.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	122.N	44.0N
OUTPUT HOLD FROM MWR	(TPDH)	146.N	122.N	46.0N
READ CYCLE TIME	(TRC)	328.N	280.N	144.N
WRITE CYCLE TIME	(TWC)	296.N	264.N	152.N

	IIL	IIH	VIC1	VIC2
A0	-252.NA	248.NA	3.59 V	-3.60 V
A1	-251.NA	248.NA	3.62 V	-3.61 V
A2	-246.NA	242.NA	3.63 V	-3.66 V
A3	-248.NA	246.NA	3.63 V	-3.66 V
A4	-240.NA	238.NA	3.63 V	-3.66 V
A5	-248.NA	246.NA	3.53 V	-3.60 V
A6	-244.NA	245.NA	3.58 V	-3.58 V
A7	-250.NA	244.NA	3.56 V	-3.63 V
CS1	-245.NA	236.NA	3.60 V	-3.63 V
CS2	-238.NA	245.NA	3.64 V	-3.65 V
MWR	-242.NA	237.NA	3.56 V	-3.59 V
MRD	-239.NA	234.NA	3.59 V	-3.60 V
DI0	-238.NA	239.NA	3.69 V	-3.66 V
DI1	-236.NA	241.NA	3.70 V	-3.63 V
DI2	-234.NA	237.NA	3.69 V	-3.69 V
DI3	-236.NA	236.NA	3.68 V	-3.63 V

	D00	D01	D02	D03
VOL1	150.MV	155.MV	170.MV	165.MV
VOL2	160.MV	170.MV	195.MV	185.MV
VOH1	4.76 V	4.76 V	4.75 V	4.76 V
VOH2	9.67 V	9.67 V	9.65 V	9.67 V
IDN1	4.90MA	4.80MA	4.45MA	4.55MA
IDN2	11.8MA	11.2MA	9.95MA	10.3MA
IDP1	-1.64MA	-1.62MA	-1.61MA	-1.65MA
IDP2	-3.80MA	-3.80MA	-3.70MA	-3.86MA
IOZ1	538.NA	553.NA	548.NA	530.NA
IOZ2	530.NA	552.NA	537.NA	535.NA
IOZ3	531.NA	546.NA	539.NA	531.NA
IOZ4	526.NA	552.NA	533.NA	536.NA
IOZ5	535.NA	553.NA	544.NA	543.NA
IOZ6	521.NA	560.NA	536.NA	530.NA
IOZ7	526.NA	545.NA	543.NA	528.NA
IOZ8	526.NA	552.NA	534.NA	537.NA
ILDP	50.0UA			
IL1	-125.UA			
IL2	-150.UA			
IL3	-110.UA			
IL4	-95.0UA			

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN: 2

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	205.N	175.N	80.0N
DATA SETUP TIME	(TDS)	22.0N	18.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	12.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	100.N	88.0N	44.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-12.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	68.0N	60.0N	36.0N
CS1 SETUP TIME	(TCSS1)	150.N	130.N	68.0N
CS2 SETUP TIME	(TCSS2)	146.N	126.N	64.0N
CS1 HOLD TIME	(TCSH1)	42.0N	38.0N	24.0N
CS2 HOLD TIME	(TCSH2)	44.0N	38.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	198.N	172.N	90.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	194.N	168.N	86.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	44.0N	40.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	126.N	98.0N	22.0N
OUTPUT HOLD FROM CS2	(TDOH2)	126.N	96.0N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	130.N	108.N	32.0N
OUTPUT HOLD FROM MWR	(TPDH)	124.N	104.N	32.0N
READ CYCLE TIME	(TRC)	216.N	192.N	96.0N
WRITE CYCLE TIME	(TWC)	200.N	176.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-1.40NA	1.60NA	2.80 V	-2.81 V
A1	-1.50NA	1.30NA	2.88 V	-2.87 V
A2	-1.80NA	1.20NA	2.89 V	-2.93 V
A3	-1.30NA	2.30NA	2.89 V	-2.92 V
A4	-1.40NA	1.30NA	2.88 V	-2.91 V
A5	-1.50NA	1.70NA	2.81 V	-2.86 V
A6	-2.00NA	1.40NA	2.82 V	-2.88 V
A7	-1.40NA	1.40NA	2.85 V	-2.88 V
CS1	-1.40NA	1.20NA	2.84 V	-2.83 V
CS2	-2.00NA	1.30NA	2.85 V	-2.89 V
MWR	-1.40NA	1.40NA	2.83 V	-2.85 V
MRD	-1.30NA	1.70NA	2.84 V	-2.84 V
DI0	-1.60NA	1.60NA	2.91 V	-2.87 V
DI1	-1.60NA	1.40NA	2.91 V	-2.85 V
DI2	-1.80NA	1.60NA	2.93 V	-2.87 V
DI3	-1.60NA	1.40NA	2.91 V	-2.85 V

	D00	D01	D02	D03
VOL1	90.0MV	95.0MV	100.MV	100.MV
VOL2	100.MV	105.MV	125.MV	120.MV
VOH1	4.86 V	4.86 V	4.86 V	4.86 V
VOH2	9.79 V	9.79 V	9.78 V	9.80 V
IDN1	8.20MA	7.85MA	7.25MA	7.45MA
IDN2	19.1MA	17.5MA	15.2MA	15.9MA
IDP1	-2.71MA	-2.73MA	-2.66MA	-2.74MA
IDP2	-5.89MA	-5.92MA	-5.67MA	-6.02MA
IOZ1	26.2NA	26.9NA	30.3NA	25.5NA
IOZ2	22.6NA	30.1NA	27.1NA	28.6NA
IOZ3	27.9NA	25.3NA	31.2NA	25.5NA
IOZ4	28.3NA	23.9NA	32.8NA	23.3NA
IOZ5	22.4NA	31.5NA	26.7NA	31.4NA
IOZ6	22.6NA	31.8NA	26.8NA	31.0NA
IOZ7	22.4NA	31.8NA	26.5NA	30.2NA
IOZ8	22.3NA	31.5NA	26.4NA	30.5NA

ILDP	-1.20UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-5.00UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	205.N	170.N	70.0N
DATA SETUP TIME	(TDS)	22.0N	18.0N	6.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	98.0N	80.0N	38.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	70.0N	54.0N	34.0N
CS1 SETUP TIME	(TCSS1)	144.N	122.N	60.0N
CS2 SETUP TIME	(TCSS2)	142.N	120.N	60.0N
CS1 HOLD TIME	(TCSH1)	38.0N	34.0N	22.0N
CS2 HOLD TIME	(TCSH2)	40.0N	34.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	192.N	160.N	84.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	190.N	158.N	82.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	40.0N	36.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	122.N	92.0N	22.0N
OUTPUT HOLD FROM CS2	(TDOH2)	120.N	90.0N	22.0N
OUTPUT HOLD FROM MRD	(TDOH3)	126.N	108.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	122.N	102.N	30.0N
READ CYCLE TIME	(TRC)	200.N	176.N	100.N
WRITE CYCLE TIME	(TWC)	224.N	176.N	96..N

	IIL	IIH	VIC1	VIC2
A0	-200.PA	200.PA	2.89 V	-2.89 V
A1	-200.PA	200.PA	2.95 V	-2.95 V
A2	-300.PA	200.PA	2.97 V	-3.00 V
A3	-200.PA	500.PA	2.97 V	-3.00 V
A4	-200.PA	200.PA	2.95 V	-2.98 V
A5	-200.PA	400.PA	2.89 V	-2.93 V
A6	-400.PA	200.PA	2.90 V	-2.95 V
A7	-200.PA	200.PA	2.93 V	-2.95 V
CS1	-100.PA	200.PA	2.93 V	-2.91 V
CS2	-400.PA	200.PA	2.93 V	-2.96 V
MWR	-200.PA	200.PA	2.91 V	-2.93 V
MRD	-100.PA	400.PA	2.93 V	-2.92 V
DI0	-200.PA	300.PA	2.99 V	-2.94 V
DI1	-300.PA	300.PA	2.99 V	-2.93 V
DI2	-400.PA	300.PA	3.01 V	-2.95 V
DI3	-300.PA	200.PA	2.98 V	-2.93 V

	D00	D01	D02	D03
VOL1	75.0MV	80.0MV	90.0MV	85.0MV
VOL2	85.0MV	95.0MV	105.MV	100.MV
VOH1	4.88 V	4.88 V	4.88 V	4.88 V
VOH2	9.82 V	9.82 V	9.82 V	9.83 V
IDN1	9.40MA	9.05MA	8.35MA	8.55MA
IDN2	22.1MA	20.4MA	17.8MA	18.6MA
IDP1	-3.23MA	-3.26MA	-3.18MA	-3.29MA
IDP2	-6.96MA	-7.01MA	-6.76MA	-7.11MA
IOZ1	2.30NA	5.60NA	1.40NA	6.40NA
IOZ2	5.40NA	2.40NA	4.50NA	3.20NA
IOZ3	2.00NA	4.70NA	3.00NA	3.50NA
IOZ4	200.PA	7.50NA	300.PA	7.20NA
IOZ5	7.50NA	300.PA	6.90NA	1.20NA
IOZ6	7.30NA	600.PA	7.10NA	1.10NA
IOZ7	7.50NA	300.PA	6.90NA	1.00NA
IOZ8	7.30NA	500.PA	7.00NA	1.10NA

ILDP	-5.00UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-5.00UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	195.N	160.N	65.0N
DATA SETUP TIME	(TDS)	26.0N	20.0N	6.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	14.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	94.0N	76.0N	34.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	70.0N	62.0N	32.0N
CS1 SETUP TIME	(TCSS1)	140.N	118.N	56.0N
CS2 SETUP TIME	(TCSS2)	136.N	114.N	54.0N
CS1 HOLD TIME	(TCSH1)	46.0N	34.0N	22.0N
CS2 HOLD TIME	(TCSH2)	48.0N	38.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	188.N	152.N	80.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	186.N	152.N	78.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	38.0N	32.0N	20.0N
OUTPUT HOLD FROM CS1	(TDOH1)	116.N	86.0N	20.0N
OUTPUT HOLD FROM CS2	(TDOH2)	114.N	86.0N	20.0N
OUTPUT HOLD FROM MRD	(TDOH3)	126.N	106.N	20.0N
OUTPUT HOLD FROM MWR	(TPDH)	122.N	102.N	30.0N
READ CYCLE TIME	(TRC)	200.N	176.N	96.0N
WRITE CYCLE TIME	(TWC)	208.N	168.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	0.00 A	100.PA	2.96 V	2.97 V
A1	-100.PA	100.PA	3.02 V	3.02 V
A2	-100.PA	0.00 A	3.04 V	3.08 V
A3	-100.PA	100.PA	3.04 V	3.07 V
A4	0.00 A	0.00 A	3.03 V	3.05 V
A5	-100.PA	200.PA	2.96 V	3.01 V
A6	-100.PA	100.PA	2.97 V	3.02 V
A7	-100.PA	100.PA	3.00 V	3.02 V
CS1	0.00 A	0.00 A	3.00 V	2.98 V
CS2	-100.PA	0.00 A	3.00 V	3.02 V
MWR	0.00 A	100.PA	2.98 V	3.00 V
MRD	0.00 A	200.PA	3.00 V	2.99 V
DI0	-100.PA	100.PA	3.06 V	3.01 V
DI1	-100.PA	100.PA	3.06 V	3.00 V
DI2	-100.PA	100.PA	3.08 V	3.02 V
DI3	0.00 A	100.PA	3.06 V	3.00 V

	DO0	DO1	DO2	DO3
VOL1	70.0MV	75.0MV	80.0MV	75.0MV
VOL2	75.0MV	80.0MV	95.0MV	90.0MV
VOH1	4.89 V	4.90 V	4.90 V	4.90 V
VOH2	9.85 V	9.85 V	9.84 V	9.85 V
IDN1	10.4MA	10.0MA	9.35MA	9.55MA
IDN2	24.7MA	22.9MA	20.2MA	20.9MA
IDP1	-3.69MA	-3.78MA	-3.71MA	-3.81MA
IDP2	-7.92MA	-8.11MA	-7.82MA	-8.16MA
IOZ1	-200.PA	4.60NA	-1.60NA	4.90NA
IOZ2	2.80NA	1.10NA	1.20NA	1.90NA
IOZ3	1.30NA	1.30NA	1.80NA	700.PA
IOZ4	-1.40NA	5.00NA	-1.40NA	4.40NA
IOZ5	5.20NA	-1.20NA	4.10NA	-400.PA
IOZ6	5.50NA	-1.20NA	4.00NA	-600.PA
IOZ7	5.40NA	-1.20NA	4.40NA	-700.PA
IOZ8	5.70NA	-1.30NA	4.20NA	-800.PA

ILDP	-200.NA
IL1	-5.00UA
IL2	-5.00UA
IL3	-5.00UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	210.N	185.N	85.0N
DATA SETUP TIME	(TDS)	24.0N	18.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	106.N	96.0N	50.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	78.0N	70.0N	40.0N
CS1 SETUP TIME	(TCSS1)	156.N	136.N	74.0N
CS2 SETUP TIME	(TCSS2)	152.N	134.N	70.0N
CS1 HOLD TIME	(TCSH1)	54.0N	48.0N	30.0N
CS2 HOLD TIME	(TCSH2)	54.0N	48.0N	30.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	210.N	186.N	96.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	206.N	184.N	94.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	44.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	132.N	102.N	26.0N
OUTPUT HOLD FROM CS2	(TDOH2)	130.N	100.N	26.0N
OUTPUT HOLD FROM MRD	(TDOH3)	130.N	110.N	34.0N
OUTPUT HOLD FROM MWR	(TPOH)	126.N	106.N	46.0N
READ CYCLE TIME	(TRC)	232.N	208.N	120.N
WRITE CYCLE TIME	(TWC)	216.N	192.N	120.N

	IIL	IIH	VIC1	VIC2
A0	-21.6NA	21.7NA	2.76 V	-2.77 V
A1	-21.6NA	20.6NA	2.84 V	-2.84 V
A2	-23.5NA	20.8NA	2.86 V	-2.89 V
A3	-21.2NA	24.5NA	2.86 V	-2.89 V
A4	-21.1NA	20.3NA	2.85 V	-2.87 V
A5	-21.4NA	21.7NA	2.77 V	-2.82 V
A6	-23.8NA	21.4NA	2.78 V	-2.84 V
A7	-21.6NA	21.0NA	2.82 V	-2.84 V
CS1	-21.8NA	19.8NA	2.80 V	-2.79 V
CS2	-22.6NA	20.8NA	2.81 V	-2.85 V
MWR	-20.6NA	20.8NA	2.79 V	-2.81 V
MRD	-20.5NA	21.8NA	2.80 V	-2.80 V
DI0	-20.8NA	21.9NA	2.88 V	-2.83 V
DI1	-21.6NA	20.8NA	2.88 V	-2.81 V
DI2	-21.8NA	21.5NA	2.90 V	-2.84 V
DI3	-21.1NA	20.9NA	2.88 V	-2.81 V

	DQ0	DQ1	DQ2	DQ3
VOL1	105.MV	110.MV	120.MV	120.MV
VOL2	120.MV	130.MV	150.MV	145.MV
VOH1	4.82 V	4.82 V	4.82 V	4.83 V
VOH2	9.74 V	9.75 V	9.74 V	9.76 V
IDN1	6.90MA	6.60MA	6.10MA	6.30MA
IDN2	15.9MA	14.6MA	12.7MA	13.3MA
IDP1	-2.27MA	-2.27MA	-2.21MA	-2.31MA
IDP2	-4.94MA	-4.97MA	-4.75MA	-5.07MA
IOZ1	321.NA	340.NA	364.NA	314.NA
IOZ2	324.NA	335.NA	364.NA	319.NA
IOZ3	319.NA	336.NA	367.NA	319.NA
IOZ4	326.NA	335.NA	361.NA	324.NA
IOZ5	325.NA	341.NA	375.NA	334.NA
IOZ6	329.NA	351.NA	364.NA	336.NA
IOZ7	320.NA	349.NA	366.NA	323.NA
IOZ8	331.NA	339.NA	367.NA	328.NA

ILDP	-5.00UA
IL1	-20.0UA
IL2	-20.0UA
IL3	-20.0UA
IL4	-15.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	220.N	195.N	95.0N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	14.0N	14.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	6.00N	6.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	116.N	104.N	58.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-16.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	84.0N	74.0N	44.0N
CS1 SETUP TIME	(TCSS1)	166.N	148.N	80.0N
CS2 SETUP TIME	(TCSS2)	164.N	144.N	78.0N
CS1 HOLD TIME	(TCSH1)	56.0N	50.0N	32.0N
CS2 HOLD TIME	(TCSH2)	58.0N	52.0N	30.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	226.N	202.N	106.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	224.N	200.N	106.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	54.0N	48.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	142.N	112.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	140.N	110.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	116.N	34.0N
OUTPUT HOLD FROM MWR	(TPDH)	134.N	112.N	36.0N
READ CYCLE TIME	(TRC)	248.N	216.N	129.N
WRITE CYCLE TIME	(TWC)	232.N	208.N	124.N

	IIL	IIH	VIC1	VIC2
A0	-131.NA	126.NA	2.74 V	-2.75 V
A1	-129.NA	124.NA	2.82 V	-2.81 V
A2	-131.NA	123.NA	2.84 V	-2.88 V
A3	-127.NA	130.NA	2.84 V	-2.88 V
A4	-127.NA	120.NA	2.83 V	-2.86 V
A5	-128.NA	123.NA	2.75 V	-2.80 V
A6	-134.NA	124.NA	2.77 V	-2.82 V
A7	-128.NA	122.NA	2.80 V	-2.83 V
CS1	-133.NA	117.NA	2.78 V	-2.78 V
CS2	-128.NA	120.NA	2.79 V	-2.84 V
MWR	-123.NA	119.NA	2.77 V	-2.79 V
MRD	-125.NA	122.NA	2.78 V	-2.79 V
DI0	-124.NA	124.NA	2.86 V	-2.81 V
DI1	-123.NA	120.NA	2.86 V	-2.79 V
DI2	-124.NA	122.NA	2.89 V	-2.82 V
DI3	-122.NA	121.NA	2.86 V	-2.79 V

	D00	D01	D02	D03
VOL1	120.MV	125.MV	140.MV	135.MV
VOL2	135.MV	150.MV	170.MV	160.MV
VOH1	4.80 V	4.80 V	4.80 V	4.81 V
VOH2	9.72 V	9.72 V	9.71 V	9.72 V
IDN1	6.10MA	5.85MA	5.40MA	5.55MA
IDN2	14.0MA	13.0MA	11.3MA	11.8MA
IDP1	-2.01MA	-2.05MA	-2.00MA	-2.06MA
IDP2	-4.40MA	-4.47MA	-4.28MA	-4.50MA
IOZ1	1.52UA	1.57UA	1.66UA	1.47UA
IOZ2	1.50UA	1.58UA	1.65UA	1.48UA
IOZ3	1.50UA	1.57UA	1.66UA	1.48UA
IOZ4	1.50UA	1.58UA	1.65UA	1.48UA
IOZ5	1.52UA	1.60UA	1.71UA	1.54UA
IOZ6	1.54UA	1.60UA	1.69UA	1.50UA
IOZ7	1.53UA	1.59UA	1.68UA	1.50UA
IOZ8	1.51UA	1.59UA	1.67UA	1.50UA
ILDP	40.0UA			
IL1	-80.0UA			
IL2	-95.0UA			
IL3	-85.0UA			
IL4	-75.0UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	400.N	290.N	95.0N
DATA SETUP TIME	(TDS)	18.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	16.0N	14.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	142.N	110.N	46.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	68.0N	60.0N	36.0N
CS1 SETUP TIME	(TCSS1)	250.N	140.N	68.0N
CS2 SETUP TIME	(TCSS2)	246.N	136.N	66.0N
CS1 HOLD TIME	(TCSH1)	40.0N	36.0N	24.0N
CS2 HOLD TIME	(TCSH2)	44.0N	38.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	366.N	286.N	104.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	364.N	282.N	102.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	56.0N	50.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	156.N	124.N	38.0N
OUTPUT HOLD FROM CS2	(TDOH2)	152.N	120.N	36.0N
OUTPUT HOLD FROM MRD	(TDOH3)	144.N	122.N	32.0N
OUTPUT HOLD FROM MWR	(TPDH)	144.N	116.N	32.0N
READ CYCLE TIME	(TRC)	384.N	288.N	120.N
WRITE CYCLE TIME	(TWC)	200.N	184.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-2.90NA	2.90NA	3.18 V	-3.16 V
A1	-3.10NA	3.00NA	3.19 V	-3.20 V
A2	-2.80NA	3.00NA	3.21 V	-3.24 V
A3	-2.70NA	2.50NA	3.20 V	-3.23 V
A4	-3.30NA	3.00NA	3.24 V	-3.28 V
A5	-2.60NA	2.90NA	3.14 V	-3.18 V
A6	-2.40NA	2.60NA	3.12 V	-3.17 V
A7	-2.30NA	2.60NA	3.14 V	-3.18 V
CS1	-2.80NA	2.60NA	3.23 V	-3.24 V
CS2	-2.90NA	3.10NA	3.25 V	-3.23 V
MWR	-2.90NA	2.60NA	3.19 V	-3.21 V
MRD	-2.70NA	2.80NA	3.22 V	-3.24 V
DI0	-2.20NA	2.80NA	3.25 V	-3.21 V
DI1	-2.40NA	2.60NA	3.25 V	-3.18 V
DI2	-2.60NA	2.50NA	3.30 V	-3.23 V
DI3	-2.50NA	3.20NA	3.25 V	-3.20 V

	D00	D01	D02	D03
VOL1	115.MV	120.MV	130.MV	125.MV
VOL2	110.MV	120.MV	140.MV	135.MV
VOH1	4.86 V	4.86 V	4.84 V	4.86 V
VOH2	9.79 V	9.78 V	9.77 V	9.79 V
IDN1	6.35MA	6.15MA	5.65MA	5.80MA
IDN2	16.8MA	15.5MA	13.5MA	14.1MA
IDP1	-2.67MA	-2.63MA	-2.58MA	-2.66MA
IDP2	-5.85MA	-5.78MA	-5.61MA	-5.91MA
IOZ1	19.4NA	15.6NA	19.7NA	15.9NA
IOZ2	18.9NA	14.3NA	21.3NA	13.6NA
IOZ3	12.7NA	20.7NA	14.1NA	20.7NA
IOZ4	14.9NA	18.3NA	15.1NA	18.8NA
IOZ5	17.4NA	14.8NA	19.4NA	14.1NA
IOZ6	17.4NA	14.8NA	19.8NA	13.9NA
IOZ7	17.6NA	14.4NA	19.9NA	13.8NA
IOZ8	17.4NA	14.6NA	20.0NA	13.8NA

ILDP	-10.0UA
IL1	-35.0UA
IL2	-65.0UA
IL3	-10.0UA
IL4	-40.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	490.N	325.N	90.0N
DATA SETUP TIME	(TDS)	20.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	14.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	150.N	114.N	40.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	72.0N	64.0N	34.0N
CS1 SETUP TIME	(TCSS1)	360.N	166.N	64.0N
CS2 SETUP TIME	(TCSS2)	358.N	164.N	62.0N
CS1 HOLD TIME	(TCSH1)	38.0N	32.0N	22.0N
CS2 HOLD TIME	(TCSH2)	40.0N	34.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	434.N	308.N	98.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	432.N	306.N	96.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	52.0N	46.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	150.N	118.N	36.0N
OUTPUT HOLD FROM CS2	(TDOH2)	146.N	114.N	36.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	120.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	142.N	114.N	36.0N
READ CYCLE TIME	(TRC)	400.N	288.N	112.N
WRITE CYCLE TIME	(TWC)	256.N	176.N	104.N

	IIL	IIH	VIC1	VIC2
A0	-400.PA	500.PA	3.23 V	-3.21 V
A1	-400.PA	400.PA	3.24 V	-3.26 V
A2	-400.PA	500.PA	3.26 V	-3.29 V
A3	-400.PA	300.PA	3.25 V	-3.28 V
A4	-700.PA	500.PA	3.29 V	-3.32 V
A5	-400.PA	500.PA	3.20 V	-3.23 V
A6	-300.PA	500.PA	3.17 V	-3.23 V
A7	-300.PA	400.PA	3.19 V	-3.23 V
CS1	-400.PA	400.PA	3.29 V	-3.28 V
CS2	-500.PA	500.PA	3.30 V	-3.27 V
MWR	-500.PA	400.PA	3.25 V	-3.26 V
MRD	-300.PA	500.PA	3.28 V	-3.29 V
DI0	-300.PA	500.PA	3.30 V	-3.26 V
DI1	-400.PA	400.PA	3.30 V	-3.22 V
DI2	-400.PA	400.PA	3.35 V	-3.28 V
DI3	-400.PA	500.PA	3.30 V	-3.25 V

	DO0	DO1	DO2	DO3
VOL1	105.MV	105.MV	115.MV	115.MV
VOL2	95.0MV	105.MV	125.MV	115.MV
VOH1	4.88 V	4.88 V	4.88 V	4.88 V
VOH2	9.82 V	9.82 V	9.81 V	9.82 V
IDN1	7.00MA	6.80MA	6.25MA	6.45MA
IDN2	19.2MA	17.7MA	15.4MA	16.1MA
IDP1	-3.12MA	-3.09MA	-3.01MA	-3.11MA
IDP2	-6.88MA	-6.82MA	-6.55MA	-6.95MA
IOZ1	5.00NA	3.50NA	5.50NA	2.40NA
IOZ2	1.60NA	6.50NA	2.20NA	5.70NA
IOZ3	6.60NA	2.20NA	5.70NA	3.00NA
IOZ4	7.20NA	900.PA	7.90NA	700.PA
IOZ5	800.PA	8.00NA	800.PA	7.60NA
IOZ6	700.PA	7.80NA	900.PA	7.70NA
IOZ7	900.PA	8.00NA	900.PA	7.40NA
IOZ8	800.PA	7.80NA	1.00NA	7.40NA

ILDP	15.0UA
IL1	-35.0UA
IL2	-60.0UA
IL3	-5.00UA
IL4	-35.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
FAILED GALPAT (TIGHT LIMITS) VCC=5V ADD = 207 DIAG = 10 PIN: 004

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	585.N	355.N	85.0N
DATA SETUP TIME	(TDS)	26.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	60.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	162.N	112.N	36.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	76.0N	66.0N	32.0N
CS1 SETUP TIME	(TCSS1)	422.N	180.N	60.0N
CS2 SETUP TIME	(TCSS2)	422.N	176.N	58.0N
CS1 HOLD TIME	(TCSH1)	40.0N	34.0N	22.0N
CS2 HOLD TIME	(TCSH2)	48.0N	36.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	1.00K	318.N	94.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	1.00K	318.N	92.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	42.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	142.N	112.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	138.N	110.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	1.00K	114.N	30.0N
READ CYCLE TIME	(TRC)	448.N	320.N	124.N
WRITE CYCLE TIME	(TWC)	192.N	176.N	98.0N

	IIL	IIH	VIC1	VIC2
A0	-100.PA	100.PA	3.30 V	-3.28 V
A1	-100.PA	100.PA	3.31 V	-3.32 V
A2	-100.PA	100.PA	3.32 V	-3.35 V
A3	-100.PA	100.PA	3.31 V	-3.35 V
A4	-200.PA	100.PA	3.35 V	-3.36 V
A5	-100.PA	100.PA	3.26 V	-3.30 V
A6	-100.PA	100.PA	3.23 V	-3.29 V
A7	-100.PA	100.PA	3.25 V	-3.29 V
CS1	-100.PA	100.PA	3.36 V	-3.35 V
CS2	-100.PA	100.PA	3.37 V	-3.32 V
MWR	-100.PA	100.PA	3.31 V	-3.32 V
MRD	-100.PA	100.PA	3.35 V	-3.36 V
DI0	-100.PA	100.PA	3.37 V	-3.32 V
DI1	-100.PA	100.PA	3.36 V	-3.28 V
DI2	-100.PA	100.PA	3.41 V	-3.34 V
DI3	-100.PA	100.PA	3.37 V	-3.30 V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

	DO0	DO1	DO2	DO3
VOL1	100.MV	100.MV	105.MV	105.MV
VOL2	90.0MV	95.0MV	110.MV	105.MV
VOH1	4.89 V	4.89 V	4.88 V	4.89 V
VOH2	9.85 V	9.84 V	9.84 V	9.85 V
IDN1	7.60MA	7.35MA	6.80MA	7.00MA
IDN2	21.1MA	19.7MA	17.3MA	17.9MA
IDP1	-3.56MA	-3.55MA	-3.47MA	-3.60MA
IDP2	-7.88MA	-7.85MA	-7.62MA	-8.00MA
IOZ1	3.10NA	1.80NA	1.80NA	2.80NA
IOZ2	5.90NA	-1.20NA	5.30NA	-600.PA
IOZ3	-1.00NA	5.50NA	-1.10NA	4.60NA
IOZ4	-300.PA	4.20NA	-1.40NA	4.80NA
IOZ5	4.60NA	-1.30NA	4.60NA	-1.30NA
IOZ6	4.40NA	-1.00NA	4.70NA	-1.40NA
IOZ7	4.40NA	-1.20NA	4.50NA	-1.20NA
IOZ8	4.10NA	-800.PA	4.50NA	-1.30NA

ILDP	-3.20UA
IL1	-30.0UA
IL2	-60.0UA
IL3	-5.00UA
IL4	-30.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	345.N	270.N	100.N
DATA SETUP TIME	(TDS)	18.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	16.0N	16.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	6.00N	6.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	134.N	106.N	50.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-14.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	78.0N	70.0N	40.0N
CS1 SETUP TIME	(TCSS1)	166.N	144.N	76.0N
CS2 SETUP TIME	(TCSS2)	162.N	142.N	72.0N
CS1 HOLD TIME	(TCSH1)	46.0N	42.0N	28.0N
CS2 HOLD TIME	(TCSH2)	50.0N	46.0N	26.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	340.N	276.N	114.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	338.N	272.N	112.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	58.0N	50.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	158.N	126.N	40.0N
OUTPUT HOLD FROM CS2	(TDOH2)	154.N	122.N	42.0N
OUTPUT HOLD FROM MRD	(TDOH3)	144.N	122.N	36.0N
OUTPUT HOLD FROM MWR	(TPDH)	142.N	116.N	36.0N
READ CYCLE TIME	(TRC)	368.N	288.N	120.N
WRITE CYCLE TIME	(TWC)	224.N	200.N	128.N

	IIL	IIH	VIC1	VIC2
A0	-35.3NA	35.6NA	3.16 V	-3.14 V
A1	-34.4NA	35.7NA	3.17 V	-3.19 V
A2	-34.7NA	35.5NA	3.20 V	-3.24 V
A3	-34.5NA	34.4NA	3.19 V	-3.22 V
A4	-35.4NA	35.5NA	3.24 V	-3.27 V
A5	-33.7NA	35.4NA	3.13 V	-3.16 V
A6	-33.2NA	33.5NA	3.10 V	-3.15 V
A7	-33.5NA	33.8NA	3.13 V	-3.16 V
CS1	-35.6NA	33.9NA	3.22 V	-3.22 V
CS2	-34.3NA	36.1NA	3.24 V	-3.23 V
MWR	-34.6NA	34.2NA	3.18 V	-3.20 V
MRD	-35.1NA	35.2NA	3.21 V	-3.23 V
DI0	-31.7NA	34.0NA	3.24 V	-3.19 V
DI1	-32.5NA	34.1NA	3.23 V	-3.16 V
DI2	-32.3NA	33.1NA	3.29 V	-3.22 V
DI3	-32.9NA	35.7NA	3.24 V	-3.19 V

	D00	D01	D02	D03
VOL1	130.MV	135.MV	150.MV	145.MV
VOL2	130.MV	145.MV	165.MV	160.MV
VOH1	4.82 V	4.82 V	4.82 V	4.82 V
VOH2	9.75 V	9.75 V	9.73 V	9.75 V
IDN1	5.60MA	5.40MA	4.95MA	5.10MA
IDN2	14.4MA	13.2MA	11.5MA	12.0MA
IDP1	-2.27MA	-2.24MA	-2.20MA	-2.27MA
IDP2	-4.94MA	-4.93MA	-4.74MA	-4.99MA
IOZ1	8.50NA	19.1NA	5.90NA	6.00NA
IOZ2	-2.20NA	11.9NA	-1.20NA	3.50NA
IOZ3	-4.30NA	-2.00NA	2.40NA	-6.60NA
IOZ4	-4.60NA	3.60NA	-700.PA	-5.20NA
IOZ5	-9.70NA	1.40NA	-4.80NA	-4.80NA
IOZ6	-6.60NA	3.20NA	-3.10NA	-3.80NA
IOZ7	-9.50NA	900.PA	-4.60NA	-4.80NA
IOZ8	-6.20NA	1.70NA	-4.80NA	-4.40NA
ILDP	20.0UA			
IL1	-60.0UA			
IL2	-105.UA			
IL3	-40.0UA			
IL4	-65.0UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	340.N	275.N	110.N
DATA SETUP TIME	(TDS)	18.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	18.0N	18.0N	16.0N
ADDRESS SETUP TIME	(TAS1)	2.00N	2.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	136.N	112.N	58.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-12.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	82.0N	72.0N	44.0N
CS1 SETUP TIME	(TCSS1)	174.N	152.N	82.0N
CS2 SETUP TIME	(TCSS2)	170.N	150.N	78.0N
CS1 HOLD TIME	(TCSH1)	48.0N	44.0N	30.0N
CS2 HOLD TIME	(TCSH2)	52.0N	46.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	354.N	290.N	120.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	352.N	286.N	118.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	60.0N	54.0N	32.0N
OUTPUT HOLD FROM CS1	(TDOH1)	158.N	128.N	42.0N
OUTPUT HOLD FROM CS2	(TDOH2)	154.N	124.N	44.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	122.N	36.0N
OUTPUT HOLD FROM MWR	(TPDH)	144.N	118.N	38.0N
READ CYCLE TIME	(TRC)	360.N	288.N	128.N
WRITE CYCLE TIME	(TWC)	232.N	208.N	136.N

	IIL	IIH	VIC1	VIC2
A0	-194.NA	195.NA	3.17 V	-3.15 V
A1	-192.NA	192.NA	3.18 V	-3.20 V
A2	-194.NA	195.NA	3.21 V	-3.25 V
A3	-192.NA	192.NA	3.20 V	-3.23 V
A4	-192.NA	191.NA	3.25 V	-3.29 V
A5	-189.NA	192.NA	3.13 V	-3.17 V
A6	-189.NA	189.NA	3.10 V	-3.16 V
A7	-191.NA	189.NA	3.13 V	-3.17 V
CS1	-199.NA	188.NA	3.23 V	-3.24 V
CS2	-190.NA	196.NA	3.25 V	-3.25 V
MWR	-193.NA	189.NA	3.19 V	-3.21 V
MRD	-194.NA	189.NA	3.22 V	-3.25 V
DI0	-180.NA	187.NA	3.25 V	-3.20 V
DI1	-183.NA	189.NA	3.24 V	-3.17 V
DI2	-182.NA	184.NA	3.30 V	-3.23 V
DI3	-184.NA	190.NA	3.25 V	-3.20 V

	D00	D01	D02	D03
VOL1	145.MV	150.MV	165.MV	160.MV
VOL2	145.MV	160.MV	190.MV	180.MV
VOH1	4.80 V	4.80 V	4.80 V	4.81 V
VOH2	9.72 V	9.72 V	9.70 V	9.72 V
IDN1	5.05MA	4.90MA	4.50MA	4.65MA
IDN2	12.9MA	11.8MA	10.2MA	10.7MA
IDP1	-2.05MA	-2.04MA	-1.99MA	-2.05MA
IDP2	-4.47MA	-4.43MA	-4.25MA	-4.51MA
IOZ1	-456.NA	-429.NA	-439.NA	-451.NA
IOZ2	-483.NA	-442.NA	-460.NA	-452.NA
IOZ3	-496.NA	-455.NA	-462.NA	-466.NA
IOZ4	-499.NA	-452.NA	-471.NA	-465.NA
IOZ5	-500.NA	-455.NA	-466.NA	-471.NA
IOZ6	-512.NA	-450.NA	-472.NA	-473.NA
IOZ7	-510.NA	-460.NA	-461.NA	-482.NA
IOZ8	-505.NA	-461.NA	-473.NA	-472.NA

ILDP	65.0UA
IL1	-190.UA
IL2	-275.UA
IL3	-145.UA
IL4	-160.UA

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN: 4

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	270.N	220.N	90.0N
DATA SETUP TIME	(TDS)	18.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	12.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	128.N	106.N	48.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	66.0N	58.0N	36.0N
CS1 SETUP TIME	(TCSS1)	164.N	142.N	70.0N
CS2 SETUP TIME	(TCSS2)	160.N	138.N	68.0N
CS1 HOLD TIME	(TCSH1)	34.0N	30.0N	22.0N
CS2 HOLD TIME	(TCSH2)	38.0N	34.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	260.N	216.N	94.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	258.N	214.N	92.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	54.0N	48.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	158.N	126.N	38.0N
OUTPUT HOLD FROM CS2	(TDOH2)	154.N	122.N	38.0N
OUTPUT HOLD FROM MRD	(TDOH3)	146.N	122.N	34.0N
OUTPUT HOLD FROM MWR	(TPDH)	142.N	116.N	32.0N
READ CYCLE TIME	(TRC)	272.N	232.N	120.N
WRITE CYCLE TIME	(TWC)	304.N	216.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-2.40NA	2.60NA	2.99 V	-2.96 V
A1	-2.30NA	1.90NA	3.04 V	-3.02 V
A2	-2.40NA	3.10NA	3.05 V	-3.08 V
A3	-2.30NA	3.50NA	3.03 V	-3.06 V
A4	-3.10NA	3.00NA	3.07 V	-3.10 V
A5	-2.50NA	2.20NA	3.00 V	-3.02 V
A6	-2.30NA	2.50NA	3.00 V	-3.02 V
A7	-2.30NA	2.10NA	3.01 V	-3.03 V
CS1	-2.50NA	2.20NA	3.03 V	-3.04 V
CS2	-2.70NA	2.50NA	3.05 V	-3.10 V
MWR	-2.70NA	2.50NA	3.00 V	-3.02 V
MRD	-2.90NA	3.00NA	3.02 V	-3.04 V
DI0	-2.30NA	2.10NA	3.09 V	-3.04 V
DI1	-2.80NA	2.30NA	3.08 V	-3.01 V
DI2	-2.60NA	2.60NA	3.10 V	-3.06 V
DI3	-2.60NA	2.50NA	3.11 V	-3.06 V

	D00	D01	D02	D03
VOL1	115.MV	120.MV	130.MV	125.MV
VOL2	115.MV	120.MV	140.MV	135.MV
VOH1	4.85 V	4.85 V	4.85 V	4.85 V
VOH2	9.79 V	9.80 V	9.78 V	9.80 V
IDN1	6.35MA	6.20MA	5.75MA	5.80MA
IDN2	16.5MA	15.5MA	13.7MA	14.1MA
IDP1	-2.63MA	-2.63MA	-2.55MA	-2.60MA
IDP2	-5.93MA	-5.93MA	-5.69MA	-5.92MA
IOZ1	18.5NA	11.4NA	16.5NA	10.8NA
IOZ2	15.0NA	13.6NA	13.7NA	12.3NA
IOZ3	13.3NA	15.4NA	10.6NA	16.2NA
IOZ4	16.9NA	12.2NA	13.9NA	12.9NA
IOZ5	12.6NA	15.2NA	11.3NA	14.4NA
IOZ6	12.9NA	14.7NA	12.1NA	14.1NA
IOZ7	12.9NA	15.0NA	12.0NA	13.5NA
IOZ8	13.3NA	14.5NA	11.6NA	13.9NA

ILDP	-10.0UA
IL1	-35.0UA
IL2	-25.0UA
IL3	-115.UA
IL4	-35.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	280.N	220.N	80.0N
DATA SETUP TIME	(TDS)	22.0N	18.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	128.N	102.N	42.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	64.0N	56.0N	34.0N
CS1 SETUP TIME	(TCSS1)	160.N	136.N	66.0N
CS2 SETUP TIME	(TCSS2)	156.N	134.N	64.0N
CS1 HOLD TIME	(TCSH1)	32.0N	30.0N	20.0N
CS2 HOLD TIME	(TCSH2)	38.0N	32.0N	18.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	266.N	214.N	88.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	264.N	212.N	86.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	44.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	150.N	116.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	146.N	114.N	36.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	120.N	32.0N
OUTPUT HOLD FROM MWR	(TPDH)	138.N	114.N	32.0N
READ CYCLE TIME	(TRC)	256.N	192.N	112.N
WRITE CYCLE TIME	(TWC)	248.N	200.N	104.N

	IIL	IIH	VIC1	VIC2
A0	-400.PA	400.PA	3.11 V	-3.08 V
A1	-400.PA	300.PA	3.16 V	-3.13 V
A2	-400.PA	700.PA	3.17 V	-3.18 V
A3	-400.PA	800.PA	3.15 V	-3.17 V
A4	-700.PA	600.PA	3.19 V	-3.21 V
A5	-400.PA	400.PA	3.12 V	-3.14 V
A6	-400.PA	400.PA	3.13 V	-3.13 V
A7	-400.PA	500.PA	3.13 V	-3.15 V
CS1	-400.PA	400.PA	3.16 V	-3.16 V
CS2	-500.PA	400.PA	3.17 V	-3.20 V
MWR	-600.PA	500.PA	3.13 V	-3.14 V
MRD	-600.PA	700.PA	3.15 V	-3.15 V
DI0	-400.PA	300.PA	3.20 V	-3.15 V
DI1	-500.PA	400.PA	3.20 V	-3.13 V
DI2	-600.PA	500.PA	3.21 V	-3.17 V
DI3	-500.PA	400.PA	3.23 V	-3.16 V

	D00	D01	D02	D03
VOL1	105.MV	105.MV	115.MV	115.MV
VOL2	100.MV	105.MV	120.MV	115.MV
VOH1	4.88 V	4.88 V	4.88 V	4.88 V
VOH2	9.82 V	9.83 V	9.82 V	9.82 V
IDN1	7.00MA	6.85MA	6.40MA	6.45MA
IDN2	18.7MA	17.7MA	15.8MA	16.2MA
IDP1	-3.10MA	-3.08MA	-3.04MA	-3.08MA
IDP2	-6.94MA	-6.98MA	-6.75MA	-7.00MA
IOZ1	3.80NA	5.10NA	3.50NA	3.70NA
IOZ2	1.40NA	8.00NA	600.PA	7.10NA
IOZ3	8.60NA	900.PA	6.70NA	1.30NA
IOZ4	6.50NA	1.20NA	6.10NA	800.PA
IOZ5	1.80NA	6.70NA	300.PA	7.40NA
IOZ6	2.10NA	7.00NA	-100.PA	7.20NA
IOZ7	1.80NA	6.70NA	400.PA	7.40NA
IOZ8	1.90NA	6.70NA	200.PA	7.20NA

ILDP	-20.0UA
IL1	-30.0UA
IL2	-15.0UA
IL3	-100.UA
IL4	-30.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	280.N	210.N	75.0N
DATA SETUP TIME	(TDS)	28.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	12.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	126.N	100.N	40.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	66.0N	56.0N	32.0N
CS1 SETUP TIME	(TCSS1)	158.N	134.N	62.0N
CS2 SETUP TIME	(TCSS2)	160.N	130.N	60.0N
CS1 HOLD TIME	(TCSH1)	40.0N	32.0N	20.0N
CS2 HOLD TIME	(TCSH2)	42.0N	38.0N	18.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	282.N	216.N	84.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	282.N	214.N	82.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	48.0N	42.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	146.N	110.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	142.N	108.N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	118.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	138.N	112.N	30.0N
READ CYCLE TIME	(TRC)	248.N	208.N	112.N
WRITE CYCLE TIME	(TWC)	256.N	192.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-100.PA	100.PA	3.22 V	-3.19 V
A1	-100.PA	100.PA	3.27 V	-3.25 V
A2	-100.PA	200.PA	3.28 V	-3.29 V
A3	-100.PA	200.PA	3.27 V	-3.28 V
A4	-100.PA	200.PA	3.30 V	-3.32 V
A5	-100.PA	100.PA	3.24 V	-3.25 V
A6	-100.PA	100.PA	3.23 V	-3.24 V
A7	-100.PA	200.PA	3.24 V	-3.26 V
CS1	-100.PA	100.PA	3.28 V	-3.27 V
CS2	-100.PA	100.PA	3.29 V	-3.31 V
MWR	-100.PA	200.PA	3.25 V	-3.25 V
MRD	-100.PA	200.PA	3.27 V	-3.26 V
DI0	-100.PA	100.PA	3.32 V	-3.26 V
DI1	-100.PA	100.PA	3.31 V	-3.23 V
DI2	-100.PA	100.PA	3.32 V	-3.28 V
DI3	-100.PA	100.PA	3.35 V	-3.27 V

	D00	D01	D02	D03
VOL1	100.MV	100.MV	105.MV	105.MV
VOL2	90.0MV	95.0MV	110.MV	105.MV
VOH1	4.89 V	4.89 V	4.89 V	4.89 V
VOH2	9.85 V	9.85 V	9.84 V	9.85 V
IDN1	7.55MA	7.40MA	6.90MA	7.00MA
IDN2	20.5MA	19.5MA	17.5MA	17.9MA
IDP1	-3.55MA	-3.56MA	-3.49MA	-3.57MA
IDP2	-7.99MA	-8.04MA	-7.84MA	-8.09MA
IOZ1	5.20NA	300.PA	3.50NA	1.10NA
IOZ2	5.80NA	-1.40NA	5.50NA	-1.40NA
IOZ3	-800.PA	5.60NA	-1.80NA	5.70NA
IOZ4	2.00NA	2.80NA	-100.PA	3.50NA
IOZ5	3.40NA	300.PA	3.40NA	-100.PA
IOZ6	3.00NA	800.PA	3.30NA	-300.PA
IOZ7	3.20NA	500.PA	3.20NA	100.PA
IOZ8	3.00NA	900.PA	3.20NA	-200.PA
ILDP	-20.0UA			
IL1	-30.0UA			
IL2	-15.0UA			
IL3	-80.0UA			
IL4	-25.0UA			

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	260.N	220.N	95.0N
DATA SETUP TIME	(TDS)	20.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	16.0N	14.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	6.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	128.N	106.N	54.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	78.0N	68.0N	40.0N
CS1 SETUP TIME	(TCSS1)	168.N	148.N	76.0N
CS2 SETUP TIME	(TCSS2)	166.N	144.N	74.0N
CS1 HOLD TIME	(TCSH1)	44.0N	40.0N	26.0N
CS2 HOLD TIME	(TCSH2)	48.0N	42.0N	26.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	256.N	218.N	106.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	252.N	216.N	104.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	58.0N	50.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	162.N	130.N	42.0N
OUTPUT HOLD FROM CS2	(TDOH2)	156.N	126.N	42.0N
OUTPUT HOLD FROM MRD	(TDOH3)	146.N	124.N	36.0N
OUTPUT HOLD FROM MWR	(TPDH)	142.N	118.N	38.0N
READ CYCLE TIME	(TRC)	280.N	240.N	128.N
WRITE CYCLE TIME	(TWC)	232.N	200.N	128.N

	IIL	IIH	VIC1	VIC2
A0	-29.0NA	30.1NA	2.93 V	-2.91 V
A1	-29.7NA	27.7NA	2.98 V	-2.97 V
A2	-29.4NA	31.3NA	2.99 V	-3.02 V
A3	-28.9NA	33.7NA	2.97 V	-3.01 V
A4	-31.8NA	31.3NA	3.01 V	-3.05 V
A5	-29.7NA	28.7NA	2.94 V	-2.97 V
A6	-29.1NA	29.2NA	2.94 V	-2.96 V
A7	-29.0NA	28.3NA	2.95 V	-2.98 V
CS1	-30.7NA	28.4NA	2.97 V	-2.99 V
CS2	-31.0NA	30.9NA	3.00 V	-3.05 V
MWR	-29.1NA	29.9NA	2.95 V	-2.97 V
MRD	-32.0NA	31.4NA	2.97 V	-2.98 V
DI0	-28.0NA	28.8NA	3.03 V	-2.98 V
DI1	-30.5NA	28.8NA	3.02 V	-2.96 V
DI2	-28.5NA	30.6NA	3.04 V	-3.01 V
DI3	-28.5NA	28.8NA	3.05 V	-3.00 V

	DQ0	DQ1	DQ2	DQ3
VOL1	130.MV	140.MV	150.MV	145.MV
VOL2	135.MV	145.MV	165.MV	160.MV
VOH1	4.82 V	4.82 V	4.82 V	4.82 V
VOH2	9.74 V	9.75 V	9.74 V	9.75 V
IDN1	5.55MA	5.40MA	5.00MA	5.05MA
IDN2	14.0MA	13.2MA	11.7MA	12.1MA
IDP1	-2.23MA	-2.21MA	-2.14MA	-2.19MA
IDP2	-4.99MA	-4.99MA	-4.76MA	-5.01MA
IOZ1	-16.3NA	-14.7NA	-30.5NA	-23.8NA
IOZ2	-31.4NA	-19.0NA	-39.5NA	-25.2NA
IOZ3	-34.0NA	-33.0NA	-37.8NA	-36.9NA
IOZ4	-34.4NA	-30.7NA	-39.5NA	-35.6NA
IOZ5	-39.6NA	-29.1NA	-45.0NA	-34.6NA
IOZ6	-37.2NA	-29.3NA	-43.4NA	-32.7NA
IOZ7	-39.9NA	-30.9NA	-44.5NA	-35.0NA
IOZ8	-37.7NA	-31.3NA	-41.9NA	-33.6NA

ILDP	20.0UA
IL1	-65.0UA
IL2	-60.0UA
IL3	-145.UA
IL4	-55.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	270.N	230.N	105.N
DATA SETUP TIME	(TDS)	20.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	16.0N	16.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	4.00N	4.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	132.N	112.N	60.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	82.0N	72.0N	44.0N
CS1 SETUP TIME	(TCSS1)	176.N	156.N	84.0N
CS2 SETUP TIME	(TCSS2)	172.N	152.N	82.0N
CS1 HOLD TIME	(TCSH1)	46.0N	42.0N	28.0N
CS2 HOLD TIME	(TCSH2)	50.0N	46.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	268.N	232.N	114.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	264.N	230.N	114.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	60.0N	54.0N	32.0N
OUTPUT HOLD FROM CS1	(TDOH1)	162.N	132.N	44.0N
OUTPUT HOLD FROM CS2	(TDOH2)	158.N	128.N	44.0N
OUTPUT HOLD FROM MRD	(TDOH3)	146.N	124.N	38.0N
OUTPUT HOLD FROM MWR	(TPDH)	144.N	120.N	40.0N
READ CYCLE TIME	(TRC)	288.N	248.N	128.N
WRITE CYCLE TIME	(TWC)	240.N	216.N	136.N

	IIL	ITH	VIC1	VIC2
A0	-166.NA	161.NA	2.90 V	-2.88 V
A1	-167.NA	159.NA	2.95 V	-2.94 V
A2	-165.NA	165.NA	2.96 V	-3.00 V
A3	-164.NA	167.NA	2.95 V	-2.99 V
A4	-171.NA	166.NA	2.99 V	-3.02 V
A5	-168.NA	160.NA	2.91 V	-2.94 V
A6	-164.NA	159.NA	2.91 V	-2.93 V
A7	-164.NA	159.NA	2.93 V	-2.95 V
CS1	-172.NA	159.NA	2.94 V	-2.96 V
CS2	-168.NA	165.NA	2.97 V	-3.03 V
MWR	-163.NA	159.NA	2.91 V	-2.94 V
MRD	-171.NA	166.NA	2.93 V	-2.95 V
DI0	-160.NA	161.NA	3.00 V	-2.95 V
DI1	-166.NA	159.NA	3.00 V	-2.93 V
DI2	-159.NA	164.NA	3.01 V	-2.98 V
DI3	-159.NA	161.NA	3.03 V	-2.98 V

	DO0	DO1	DO2	DO3
VOL1	145.MV	150.MV	165.MV	165.MV
VOL2	150.MV	165.MV	185.MV	180.MV
VOH1	4.80 V	4.80 V	4.80 V	4.80 V
VOH2	9.72 V	9.72 V	9.71 V	9.72 V
IDN1	5.00MA	4.85MA	4.50MA	4.55MA
IDN2	12.5MA	11.8MA	10.4MA	10.7MA
IDP1	-2.00MA	-2.00MA	-1.94MA	-1.99MA
IDP2	-4.46MA	-4.50MA	-4.30MA	-4.47MA
IOZ1	-622.NA	-568.NA	-608.NA	-578.NA
IOZ2	-655.NA	-592.NA	-620.NA	-592.NA
IOZ3	-673.NA	-600.NA	-634.NA	-598.NA
IOZ4	-670.NA	-607.NA	-631.NA	-606.NA
IOZ5	-672.NA	-603.NA	-633.NA	-607.NA
IOZ6	-672.NA	-619.NA	-626.NA	-604.NA
IOZ7	-673.NA	-613.NA	-631.NA	-593.NA
IOZ8	-677.NA	-606.NA	-633.NA	-605.NA
ILDP	80.0UA			
IL1	-195.UA			
IL2	-235.UA			
IL3	-260.UA			
IL4	-150.UA			

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN: 5

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	265.N	215.N	85.0N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	12.0N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	128.N	102.N	48.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	72.0N	62.0N	36.0N
CS1 SETUP TIME	(TCSS1)	168.N	142.N	68.0N
CS2 SETUP TIME	(TCSS2)	166.N	140.N	66.0N
CS1 HOLD TIME	(TCSH1)	40.0N	36.0N	22.0N
CS2 HOLD TIME	(TCSH2)	44.0N	38.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	252.N	208.N	90.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	248.N	206.N	88.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	54.0N	46.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	152.N	120.N	36.0N
OUTPUT HOLD FROM CS2	(TDOH2)	148.N	118.N	36.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	118.N	30.0N
OUTPUT HOLD FROM MWR	(TPOH)	138.N	114.N	32.0N
READ CYCLE TIME	(TRC)	272.N	224.N	120.N
WRITE CYCLE TIME	(TWC)	400.N	208.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-2.20NA	1.90NA	3.12 V	-3.12 V
A1	-1.80NA	2.10NA	3.16 V	-3.18 V
A2	-2.30NA	2.00NA	3.20 V	-3.20 V
A3	-1.70NA	1.80NA	3.18 V	-3.20 V
A4	-1.60NA	1.80NA	3.19 V	-3.23 V
A5	-1.70NA	2.20NA	3.09 V	-3.14 V
A6	-2.00NA	2.10NA	3.10 V	-3.13 V
A7	-1.50NA	2.00NA	3.10 V	-3.12 V
CS1	-2.10NA	1.80NA	3.17 V	-3.15 V
CS2	-1.90NA	2.20NA	3.16 V	-3.17 V
MWR	-1.80NA	1.40NA	3.15 V	-3.18 V
MRD	-1.80NA	2.00NA	3.16 V	-3.17 V
DI0	-2.00NA	1.90NA	3.19 V	-3.14 V
DI1	-2.00NA	2.30NA	3.17 V	-3.12 V
DI2	-2.00NA	2.00NA	3.20 V	-3.16 V
DI3	-1.90NA	2.20NA	3.18 V	-3.14 V

	D00	D01	D02	D03
VOL1	110.MV	115.MV	125.MV	120.MV
VOL2	110.MV	120.MV	135.MV	130.MV
VOH1	4.85 V	4.85 V	4.85 V	4.85 V
VOH2	9.80 V	9.80 V	9.78 V	9.80 V
IDN1	6.80MA	6.45MA	6.00MA	6.05MA
IDN2	17.3MA	15.9MA	13.9MA	14.3MA
IDP1	-2.64MA	-2.63MA	-2.55MA	-2.61MA
IDP2	-6.01MA	-5.96MA	-5.68MA	-5.96MA
IOZ1	25.3NA	19.6NA	25.9NA	18.5NA
IOZ2	21.5NA	21.6NA	23.6NA	20.1NA
IOZ3	20.0NA	24.2NA	20.0NA	23.8NA
IOZ4	23.4NA	21.0NA	23.4NA	20.6NA
IOZ5	19.5NA	24.3NA	21.4NA	21.9NA
IOZ6	19.6NA	23.9NA	21.3NA	22.1NA
IOZ7	19.5NA	24.4NA	21.0NA	21.7NA
IOZ8	19.6NA	23.4NA	21.1NA	22.0NA

ILDP	-800.NA
IL1	-20.0UA
IL2	-15.0UA
IL3	-10.0UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	280.N	215.N	75.0N
DATA SETUP TIME	(TDS)	28.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	128.N	100.N	42.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	68.0N	68.0N	32.0N
CS1 SETUP TIME	(TCSS1)	166.N	138.N	62.0N
CS2 SETUP TIME	(TCSS2)	164.N	136.N	60.0N
CS1 HOLD TIME	(TCSH1)	40.0N	34.0N	22.0N
CS2 HOLD TIME	(TCSH2)	44.0N	36.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	258.N	206.N	82.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	256.N	204.N	82.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	42.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	146.N	114.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	142.N	110.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	30.0N
OUTPUT HOLD FROM MWR	(TDOH)	136.N	112.N	30.0N
READ CYCLE TIME	(TRC)	272.N	216.N	112.N
WRITE CYCLE TIME	(TWC)	264.N	192.N	104.N

	IIL	IIH	VIC1	VIC2
A0	-300.PA	300.PA	3.15 V	-3.15 V
A1	-300.PA	400.PA	3.20 V	-3.21 V
A2	-300.PA	300.PA	3.23 V	-3.23 V
A3	-300.PA	200.PA	3.21 V	-3.23 V
A4	-200.PA	300.PA	3.22 V	-3.25 V
A5	-300.PA	400.PA	3.13 V	-3.18 V
A6	-400.PA	300.PA	3.14 V	-3.17 V
A7	-200.PA	300.PA	3.14 V	-3.15 V
CS1	-400.PA	300.PA	3.21 V	-3.19 V
CS2	-300.PA	400.PA	3.20 V	-3.21 V
MWR	-300.PA	200.PA	3.18 V	-3.21 V
MRD	-300.PA	400.PA	3.20 V	-3.20 V
DI0	-300.PA	300.PA	3.23 V	-3.18 V
DI1	-200.PA	300.PA	3.22 V	-3.16 V
DI2	-300.PA	300.PA	3.24 V	-3.20 V
DI3	-300.PA	400.PA	3.22 V	-3.18 V

	D00	D01	D02	D03
VOL1	95.0MV	100.MV	110.MV	110.MV
VOL2	95.0MV	105.MV	120.MV	115.MV
VOH1	4.88 V	4.88 V	4.88 V	4.88 V
VOH2	9.83 V	9.83 V	9.82 V	9.82 V
IDN1	7.50MA	7.20MA	6.70MA	6.75MA
IDN2	19.6MA	18.2MA	16.0MA	16.5MA
IDP1	-3.12MA	-3.09MA	-3.03MA	-3.10MA
IDP2	-7.07MA	-7.03MA	-6.76MA	-7.07MA
IOZ1	6.10NA	1.80NA	6.50NA	800.PA
IOZ2	2.20NA	5.00NA	2.90NA	3.70NA
IOZ3	5.20NA	2.80NA	3.70NA	3.50NA
IOZ4	7.60NA	100.PA	7.40NA	600.PA
IOZ5	500.PA	7.50NA	600.PA	6.80NA
IOZ6	500.PA	7.80NA	500.PA	6.60NA
IOZ7	500.PA	7.50NA	600.PA	6.90NA
IOZ8	600.PA	7.70NA	500.PA	6.80NA

ILDP	-5.00UA
IL1	-20.0UA
IL2	-15.0UA
IL3	-5.00UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	280.N	210.N	70.0N
DATA SETUP TIME	(TDS)	36.0N	26.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	8.00N
ADDRESS SETUP TIME	(TAS1)	16.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	126.N	98.0N	38.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	88.0N	72.0N	30.0N
CS1 SETUP TIME	(TCSS1)	166.N	134.N	58.0N
CS2 SETUP TIME	(TCSS2)	168.N	134.N	56.0N
CS1 HOLD TIME	(TCSH1)	52.0N	36.0N	20.0N
CS2 HOLD TIME	(TCSH2)	54.0N	42.0N	18.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	266.N	202.N	80.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	264.N	200.N	80.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	48.0N	40.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	142.N	108.N	32.0N
OUTPUT HOLD FROM CS2	(TDOH2)	138.N	104.N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	28.0N
OUTPUT HOLD FROM MWR	(TDOH)	136.N	112.N	28.0N
READ CYCLE TIME	(TRC)	248.N	208.N	104.N
WRITE CYCLE TIME	(TWC)	248.N	192.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-100.PA	100.PA	3.22 V	-3.21 V
A1	-100.PA	100.PA	3.26 V	-3.27 V
A2	-100.PA	100.PA	3.29 V	-3.28 V
A3	-100.PA	100.PA	3.28 V	-3.29 V
A4	0.00 A	100.PA	3.28 V	-3.31 V
A5	0.00 A	100.PA	3.19 V	-3.24 V
A6	-100.PA	100.PA	3.20 V	-3.23 V
A7	0.00 A	100.PA	3.20 V	-3.21 V
CS1	-100.PA	100.PA	3.28 V	-3.25 V
CS2	-100.PA	100.PA	3.27 V	-3.27 V
MWR	-100.PA	100.PA	3.25 V	-3.27 V
MRD	-100.PA	100.PA	3.27 V	-3.26 V
DI0	-100.PA	100.PA	3.29 V	-3.24 V
DI1	-100.PA	100.PA	3.28 V	-3.22 V
DI2	-100.PA	100.PA	3.31 V	-3.26 V
DI3	-100.PA	100.PA	3.29 V	-3.24 V

	D00	D01	D02	D03
VOL1	90.0MV	95.0MV	100.MV	100.MV
VOL2	85.0MV	95.0MV	105.MV	105.MV
VOH1	4.89 V	4.89 V	4.88 V	4.89 V
VOH2	9.85 V	9.85 V	9.84 V	9.85 V
IDN1	8.15MA	7.85MA	7.25MA	7.30MA
IDN2	21.6MA	20.2MA	17.8MA	18.3MA
IDP1	-3.57MA	-3.59MA	-3.48MA	-3.60MA
IDP2	-8.11MA	-8.13MA	-7.80MA	-8.17MA
IOZ1	-100.PA	4.10NA	-900.PA	4.60NA
IOZ2	3.50NA	400.PA	2.40NA	1.30NA
IOZ3	600.PA	2.70NA	1.10NA	1.40NA
IOZ4	-1.40NA	5.60NA	-1.80NA	5.30NA
IOZ5	6.00NA	-1.70NA	5.20NA	-1.30NA
IOZ6	5.70NA	-1.70NA	5.60NA	-1.50NA
IOZ7	5.90NA	-1.80NA	5.40NA	-1.50NA
IOZ8	5.50NA	-1.70NA	5.50NA	-1.60NA

ILDP	-5.00UA
IL1	-15.0UA
IL2	-15.0UA
IL3	-5.00UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	260.N	215.N	90.0N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	6.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	126.N	106.N	54.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	82.0N	70.0N	40.0N
CS1 SETUP TIME	(TCSS1)	174.N	148.N	74.0N
CS2 SETUP TIME	(TCSS2)	172.N	146.N	70.0N
CS1 HOLD TIME	(TCSH1)	52.0N	46.0N	26.0N
CS2 HOLD TIME	(TCSH2)	56.0N	48.0N	26.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	250.N	214.N	102.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	248.N	212.N	98.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	56.0N	50.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	156.N	124.N	40.0N
OUTPUT HOLD FROM CS2	(TDOH2)	150.N	120.N	40.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	120.N	34.0N
OUTPUT HOLD FROM MWR	(TPDH)	140.N	114.N	34.0N
READ CYCLE TIME	(TRC)	280.N	240.N	120.N
WRITE CYCLE TIME	(TWC)	240.N	208.N	120.N

	IIL	IIH	VIC1	VIC2
A0	-27.4NA	26.7NA	3.13 V	-3.12 V
A1	-26.2NA	27.1NA	3.17 V	-3.19 V
A2	-27.9NA	25.7NA	3.21 V	-3.21 V
A3	-26.2NA	26.3NA	3.19 V	-3.22 V
A4	-25.6NA	26.6NA	3.21 V	-3.24 V
A5	-26.1NA	26.7NA	3.09 V	-3.14 V
A6	-26.7NA	26.7NA	3.11 V	-3.14 V
A7	-25.4NA	26.1NA	3.11 V	-3.12 V
CS1	-27.9NA	26.4NA	3.18 V	-3.16 V
CS2	-25.5NA	27.1NA	3.17 V	-3.19 V
MWR	-26.1NA	25.3NA	3.15 V	-3.19 V
MRD	-26.1NA	26.6NA	3.17 V	-3.18 V
DI0	-25.2NA	25.4NA	3.19 V	-3.14 V
DI1	-24.8NA	26.9NA	3.18 V	-3.13 V
DI2	-24.5NA	26.4NA	3.21 V	-3.17 V
DI3	-24.9NA	26.6NA	3.19 V	-3.15 V

	D00	D01	D02	D03
VOL1	125.MV	130.MV	140.MV	140.MV
VOL2	125.MV	140.MV	160.MV	155.MV
VOH1	4.82 V	4.82 V	4.82 V	4.82 V
VOH2	9.76 V	9.76 V	9.74 V	9.76 V
IDN1	5.95MA	5.65MA	5.20MA	5.25MA
IDN2	14.9MA	13.6MA	11.9MA	12.2MA
IDP1	-2.23MA	-2.23MA	-2.15MA	-2.21MA
IDP2	-5.03MA	-5.03MA	-4.80MA	-5.01MA
IOZ1	232.NA	253.NA	231.NA	235.NA
IOZ2	225.NA	251.NA	233.NA	229.NA
IOZ3	227.NA	254.NA	233.NA	232.NA
IOZ4	225.NA	249.NA	237.NA	228.NA
IOZ5	225.NA	253.NA	239.NA	233.NA
IOZ6	235.NA	243.NA	243.NA	232.NA
IOZ7	233.NA	252.NA	233.NA	241.NA
IOZ8	226.NA	250.NA	241.NA	229.NA

ILDP	-5.00UA
IL1	-35.0UA
IL2	-40.0UA
IL3	-25.0UA
IL4	-20.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	265.N	225.N	100.N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	14.0N	14.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	4.00N	4.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	130.N	112.N	60.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-16.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	86.0N	76.0N	42.0N
CS1 SETUP TIME	(TCSS1)	182.N	158.N	80.0N
CS2 SETUP TIME	(TCSS2)	178.N	154.N	78.0N
CS1 HOLD TIME	(TCSH1)	54.0N	48.0N	28.0N
CS2 HOLD TIME	(TCSH2)	58.0N	50.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	266.N	230.N	112.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	264.N	226.N	110.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	60.0N	54.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	158.N	128.N	42.0N
OUTPUT HOLD FROM CS2	(TDOH2)	154.N	124.N	44.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	120.N	36.0N
OUTPUT HOLD FROM MWR	(TPOH)	142.N	118.N	38.0N
READ CYCLE TIME	(TRC)	288.N	248.N	128.N
WRITE CYCLE TIME	(TWC)	240.N	216.N	136.N

	IIL	IIH	VIC1	VIC2
A0	-163.NA	157.NA	3.16 V	-3.16 V
A1	-162.NA	159.NA	3.22 V	-3.24 V
A2	-167.NA	157.NA	3.26 V	-3.26 V
A3	-161.NA	156.NA	3.23 V	-3.27 V
A4	-161.NA	157.NA	3.26 V	-3.30 V
A5	-161.NA	158.NA	3.13 V	-3.19 V
A6	-161.NA	157.NA	3.14 V	-3.18 V
A7	-158.NA	155.NA	3.14 V	-3.16 V
CS1	-168.NA	156.NA	3.22 V	-3.20 V
CS2	-160.NA	162.NA	3.21 V	-3.24 V
MWR	-161.NA	155.NA	3.20 V	-3.24 V
MRD	-160.NA	158.NA	3.22 V	-3.23 V
DI0	-153.NA	155.NA	3.24 V	-3.18 V
DI1	-154.NA	157.NA	3.22 V	-3.16 V
DI2	-150.NA	153.NA	3.25 V	-3.21 V
DI3	-150.NA	155.NA	3.23 V	-3.19 V

	D00	D01	D02	D03
VOL1	140.MV	145.MV	160.MV	160.MV
VOL2	145.MV	160.MV	180.MV	175.MV
VOH1	4.80 V	4.80 V	4.80 V	4.80 V
VOH2	9.72 V	9.72 V	9.71 V	9.72 V
IDN1	5.35MA	5.05MA	4.70MA	4.75MA
IDN2	13.2MA	12.1MA	10.6MA	10.9MA
IDP1	-2.00MA	-2.01MA	-1.94MA	-1.99MA
IDP2	-4.52MA	-4.52MA	-4.30MA	-4.49MA
IOZ1	1.09UA	1.13UA	1.10UA	1.05UA
IOZ2	1.07UA	1.13UA	1.08UA	1.06UA
IOZ3	1.08UA	1.12UA	1.09UA	1.05UA
IOZ4	1.07UA	1.13UA	1.09UA	1.05UA
IOZ5	1.08UA	1.14UA	1.11UA	1.07UA
IOZ6	1.09UA	1.14UA	1.11UA	1.06UA
IOZ7	1.09UA	1.13UA	1.10UA	1.06UA
IOZ8	1.08UA	1.14UA	1.09UA	1.07UA
ILDP	40.0UA			
IL1	-110.UA			
IL2	-120.UA			
IL3	-100.UA			
IL4	-80.0UA			

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN: 6

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	325.N	255.N	85.0N
DATA SETUP TIME	(TDS)	30.0N	24.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	10.0N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	142.N	114.N	48.0N
ADDRESS HOLD TIME	(TAH)	-26.0N	-20.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	78.0N	68.0N	36.0N
CS1 SETUP TIME	(TCSS1)	188.N	154.N	68.0N
CS2 SETUP TIME	(TCSS2)	182.N	150.N	66.0N
CS1 HOLD TIME	(TCSH1)	50.0N	42.0N	24.0N
CS2 HOLD TIME	(TCSH2)	54.0N	46.0N	24.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	294.N	236.N	94.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	290.N	232.N	94.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	60.0N	52.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	162.N	130.N	40.0N
OUTPUT HOLD FROM CS2	(TDOH2)	158.N	126.N	42.0N
OUTPUT HOLD FROM MRD	(TDOH3)	144.N	120.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	142.N	118.N	32.0N
READ CYCLE TIME	(TRC)	328.N	264.N	120.N
WRITE CYCLE TIME	(TWC)	272.N	272.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-37.5NA	2.20NA	3.39 V	-3.38 V
A1	-2.20NA	2.80NA	3.41 V	-3.41 V
A2	-2.30NA	2.20NA	3.44 V	-3.45 V
A3	-2.50NA	2.60NA	3.45 V	-3.47 V
A4	-10.8NA	2.40NA	3.46 V	-3.47 V
A5	-2.30NA	2.40NA	3.35 V	-3.39 V
A6	-2.30NA	2.30NA	3.37 V	-3.41 V
A7	-2.70NA	2.60NA	3.39 V	-3.40 V
CS1	-2.40NA	2.50NA	3.42 V	-3.44 V
CS2	-2.40NA	3.10NA	3.41 V	-3.44 V
MWR	-2.60NA	2.60NA	3.38 V	-3.38 V
MRD	-2.40NA	2.30NA	3.38 V	-3.39 V
DI0	-2.30NA	2.40NA	3.52 V	-3.46 V
DI1	-2.40NA	2.40NA	3.51 V	-3.44 V
DI2	-2.40NA	2.10NA	3.48 V	-3.44 V
DI3	-2.40NA	2.30NA	3.46 V	-3.42 V

	DO0	DO1	DO2	DO3
VOL1	125.MV	130.MV	140.MV	140.MV
VOL2	120.MV	130.MV	150.MV	145.MV
VOH1	4.83 V	4.83 V	4.82 V	4.82 V
VOH2	9.77 V	9.77 V	9.76 V	9.77 V
IDN1	5.75MA	5.55MA	5.25MA	5.20MA
IDN2	15.7MA	14.5MA	13.0MA	13.0MA
IDP1	-2.28MA	-2.27MA	-2.23MA	-2.25MA
IDP2	-5.41MA	-5.45MA	-5.24MA	-5.41MA
IOZ1	44.8NA	54.3NA	51.6NA	74.1NA
IOZ2	44.1NA	53.9NA	49.8NA	75.4NA
IOZ3	49.7NA	47.7NA	56.9NA	66.1NA
IOZ4	46.2NA	50.3NA	53.9NA	82.7NA
IOZ5	46.0NA	51.7NA	53.2NA	85.9NA
IOZ6	46.6NA	52.2NA	52.3NA	72.8NA
IOZ7	46.0NA	52.2NA	51.6NA	73.3NA
IOZ8	45.9NA	51.9NA	51.0NA	72.4NA

ILOP	-10.0UA
IL1	-60.0UA
IL2	-115.UA
IL3	-40.0UA
IL4	-95.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	385.N	270.N	80.0N
DATA SETUP TIME	(TDS)	36.0N	26.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	18.0N	14.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	162.N	116.N	44.0N
ADDRESS HOLD TIME	(TAH)	-26.0N	-20.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	94.0N	66.0N	36.0N
CS1 SETUP TIME	(TCSS1)	208.N	154.N	64.0N
CS2 SETUP TIME	(TCSS2)	206.N	150.N	62.0N
CS1 HOLD TIME	(TCSH1)	44.0N	38.0N	22.0N
CS2 HOLD TIME	(TCSH2)	50.0N	42.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	326.N	242.N	88.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	322.N	242.N	86.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	58.0N	50.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	158.N	124.N	38.0N
OUTPUT HOLD FROM CS2	(TDOH2)	154.N	120.N	38.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	118.N	30.0N
OUTPUT HOLD FROM MWR	(TPOH)	142.N	116.N	30.0N
READ CYCLE TIME	(TRC)	320.N	248.N	104.N
WRITE CYCLE TIME	(TWC)	288.N	304.N	104.N

	IIL	IIH	VIC1	VIC2
A0	-13.4NA	300.PA	3.43 V	-3.42 V
A1	-200.PA	500.PA	3.46 V	-3.45 V
A2	-300.PA	300.PA	3.49 V	-3.49 V
A3	-300.PA	300.PA	3.50 V	-3.51 V
A4	-2.20NA	300.PA	3.50 V	-3.51 V
A5	-300.PA	300.PA	3.40 V	-3.44 V
A6	-300.PA	300.PA	3.42 V	-3.45 V
A7	-500.PA	400.PA	3.43 V	-3.45 V
CS1	-400.PA	400.PA	3.47 V	-3.48 V
CS2	-300.PA	600.PA	3.47 V	-3.48 V
MWR	-300.PA	400.PA	3.43 V	-3.43 V
MRD	-300.PA	300.PA	3.43 V	-3.43 V
DI0	-300.PA	300.PA	3.57 V	-3.50 V
DI1	-300.PA	300.PA	3.56 V	-3.48 V
DI2	-300.PA	300.PA	3.53 V	-3.48 V
DI3	-400.PA	300.PA	3.53 V	-3.47 V

	D00	D01	D02	D03
VOL1	120.MV	120.MV	130.MV	130.MV
VOL2	105.MV	115.MV	130.MV	130.MV
VOH1	4.86 V	4.85 V	4.85 V	4.86 V
VOH2	9.80 V	9.81 V	9.80 V	9.81 V
IDN1	6.20MA	6.00MA	5.70MA	5.65MA
IDN2	17.6MA	16.3MA	14.6MA	14.8MA
IDP1	-2.68MA	-2.67MA	-2.61MA	-2.63MA
IDP2	-6.40MA	-6.42MA	-6.15MA	-6.40MA
IOZ1	7.00NA	7.80NA	8.90NA	13.8NA
IOZ2	4.00NA	11.0NA	5.40NA	20.5NA
IOZ3	10.7NA	4.80NA	11.3NA	17.9NA
IOZ4	9.60NA	4.70NA	11.6NA	15.0NA
IOZ5	4.10NA	11.1NA	5.10NA	22.0NA
IOZ6	3.90NA	10.9NA	5.30NA	24.2NA
IOZ7	4.00NA	11.3NA	5.10NA	22.6NA
IOZ8	3.80NA	11.0NA	5.10NA	22.9NA

ILDP	-2.80UA
IL1	-50.0UA
IL2	-95.0UA
IL3	-30.0UA
IL4	-75.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	415.N	270.N	75.0N
DATA SETUP TIME	(TDS)	50.0N	34.0N	8.00N
DATA HOLD TIME	(TDH)	6.00N	6.00N	8.00N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	172.N	116.N	40.0N
ADDRESS HOLD TIME	(TAH)	-28.0N	-20.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	112.N	84.0N	36.0N
CS1 SETUP TIME	(TCSS1)	238.N	154.N	62.0N
CS2 SETUP TIME	(TCSS2)	236.N	156.N	60.0N
CS1 HOLD TIME	(TCSH1)	48.0N	52.0N	22.0N
CS2 HOLD TIME	(TCSH2)	74.0N	52.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	366.N	246.N	82.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	364.N	244.N	82.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	54.0N	46.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	154.N	118.N	38.0N
OUTPUT HOLD FROM CS2	(TDOH2)	148.N	116.N	36.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	140.N	114.N	30.0N
READ CYCLE TIME	(TRC)	336.N	240.N	104.N
WRITE CYCLE TIME	(TWC)	288.N	224.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-6.40NA	100.PA	3.51 V	-3.49 V
A1	-100.PA	200.PA	3.53 V	-3.52 V
A2	-100.PA	100.PA	3.56 V	-3.56 V
A3	-100.PA	100.PA	3.58 V	-3.59 V
A4	-600.PA	100.PA	3.58 V	-3.58 V
A5	-100.PA	100.PA	3.47 V	-3.51 V
A6	-100.PA	100.PA	3.49 V	-3.52 V
A7	-100.PA	100.PA	3.50 V	-3.52 V
CS1	-100.PA	100.PA	3.55 V	-3.56 V
CS2	-100.PA	200.PA	3.55 V	-3.55 V
MWR	-100.PA	100.PA	3.51 V	-3.51 V
MRD	-100.PA	100.PA	3.51 V	-3.51 V
DI0	-100.PA	100.PA	3.64 V	-3.57 V
DI1	-100.PA	100.PA	3.63 V	-3.55 V
DI2	-100.PA	100.PA	3.60 V	-3.56 V
DI3	-100.PA	100.PA	3.61 V	-3.54 V

	D00	D01	D02	D03
VOL1	115.MV	115.MV	125.MV	125.MV
VOL2	100.MV	105.MV	120.MV	115.MV
VOH1	4.88 V	4.88 V	4.88 V	4.88 V
VOH2	9.84 V	9.84 V	9.83 V	9.84 V
IDN1	6.60MA	6.35MA	6.05MA	5.95MA
IDN2	19.2MA	17.8MA	16.1MA	16.1MA
IDP1	-3.03MA	-3.05MA	-3.00MA	-3.00MA
IDP2	-7.30MA	-7.43MA	-7.14MA	-7.32MA
IOZ1	-100.PA	5.60NA	-600.PA	11.9NA
IOZ2	3.10NA	2.30NA	1.90NA	9.20NA
IOZ3	2.60NA	1.30NA	3.60NA	6.70NA
IOZ4	-400.PA	5.00NA	300.PA	10.4NA
IOZ5	4.80NA	300.PA	4.10NA	7.80NA
IOZ6	4.90NA	500.PA	3.60NA	7.10NA
IOZ7	4.30NA	600.PA	3.70NA	4.70NA
IOZ8	4.40NA	900.PA	3.10NA	7.30NA

ILDP	-2.40UA
IL1	-45.0UA
IL2	-90.0UA
IL3	-25.0UA
IL4	-70.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	295.N	240.N	95.0N
DATA SETUP TIME	(TDS)	32.0N	24.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	6.00N	6.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	136.N	112.N	54.0N
ADDRESS HOLD TIME	(TAH)	-24.0N	-18.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	92.0N	78.0N	42.0N
CS1 SETUP TIME	(TCSS1)	192.N	160.N	74.0N
CS2 SETUP TIME	(TCSS2)	188.N	158.N	72.0N
CS1 HOLD TIME	(TCSH1)	60.0N	52.0N	30.0N
CS2 HOLD TIME	(TCSH2)	62.0N	54.0N	30.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	278.N	232.N	104.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	274.N	230.N	102.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	62.0N	54.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	162.N	130.N	42.0N
OUTPUT HOLD FROM CS2	(TDOH2)	158.N	126.N	42.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	120.N	34.0N
OUTPUT HOLD FROM MWR	(TPDH)	142.N	118.N	34.0N
READ CYCLE TIME	(TRC)	320.N	264.N	120.N
WRITE CYCLE TIME	(TWC)	248.N	216.N	128.N

	IIL	IIH	VIC1	VIC2
A0	-147.NA	30.8NA	3.39 V	-3.38 V
A1	-31.3NA	31.9NA	3.41 V	-3.41 V
A2	-30.8NA	30.3NA	3.44 V	-3.45 V
A3	-31.3NA	32.2NA	3.46 V	-3.48 V
A4	-62.0NA	30.1NA	3.46 V	-3.48 V
A5	-31.5NA	31.3NA	3.35 V	-3.39 V
A6	-31.5NA	31.2NA	3.38 V	-3.41 V
A7	-32.1NA	31.6NA	3.39 V	-3.41 V
CS1	-29.9NA	30.4NA	3.42 V	-3.44 V
CS2	-30.7NA	33.2NA	3.41 V	-3.44 V
MWR	-30.8NA	30.5NA	3.38 V	-3.38 V
MRD	-30.5NA	30.1NA	3.38 V	-3.39 V
DI0	-30.7NA	31.0NA	3.53 V	-3.47 V
DI1	-30.5NA	30.9NA	3.51 V	-3.44 V
DI2	-29.8NA	29.8NA	3.48 V	-3.44 V
DI3	-30.0NA	29.8NA	3.48 V	-3.43 V

	DO0	DO1	DO2	DO3
VOL1	140.MV	150.MV	160.MV	160.MV
VOL2	140.MV	150.MV	175.MV	170.MV
VOH1	4.80 V	4.80 V	4.80 V	4.80 V
VOH2	9.73 V	9.73 V	9.72 V	9.72 V
IDN1	5.20MA	4.95MA	4.70MA	4.65MA
IDN2	13.6MA	12.5MA	11.1MA	11.3MA
IDP1	-1.96MA	-1.93MA	-1.91MA	-1.92MA
IDP2	-4.58MA	-4.59MA	-4.43MA	-4.58MA
IOZ1	373.NA	394.NA	414.NA	416.NA
IOZ2	376.NA	389.NA	405.NA	434.NA
IOZ3	370.NA	388.NA	408.NA	425.NA
IOZ4	372.NA	390.NA	402.NA	448.NA
IOZ5	376.NA	393.NA	411.NA	432.NA
IOZ6	366.NA	404.NA	405.NA	449.NA
IOZ7	369.NA	390.NA	413.NA	431.NA
IOZ8	371.NA	398.NA	403.NA	436.NA

ILOP	-5.00UA
IL1	-90.0UA
IL2	-150.UA
IL3	-70.0UA
IL4	-125.UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	285.N	240.N	105.N
DATA SETUP TIME	(TDS)	30.0N	24.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	2.00N	2.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	136.N	120.N	62.0N
ADDRESS HOLD TIME	(TAH)	-22.0N	-18.0N	-6.00N
WRITE PULSE WIDTH	(TWP)	94.0N	82.0N	44.0N
CS1 SETUP TIME	(TCSS1)	190.N	164.N	80.0N
CS2 SETUP TIME	(TCSS2)	186.N	160.N	78.0N
CS1 HOLD TIME	(TCSH1)	64.0N	54.0N	30.0N
CS2 HOLD TIME	(TCSH2)	66.0N	56.0N	30.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	284.N	244.N	118.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	280.N	240.N	114.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	62.0N	54.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	160.N	130.N	46.0N
OUTPUT HOLD FROM CS2	(TDOH2)	156.N	126.N	46.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	120.N	36.0N
OUTPUT HOLD FROM MWR	(TPDH)	144.N	118.N	36.0N
READ CYCLE TIME	(TRC)	320.N	264.N	128.N
WRITE CYCLE TIME	(TWC)	232.N	216.N	128.N

	IIL	IIH	VIC1	VTC2
A0	-403.NA	174.NA	3.42 V	-3.41 V
A1	-177.NA	173.NA	3.44 V	-3.44 V
A2	-176.NA	172.NA	3.48 V	-3.49 V
A3	-178.NA	175.NA	3.49 V	-3.52 V
A4	-250.NA	165.NA	3.49 V	-3.52 V
A5	-178.NA	174.NA	3.38 V	-3.42 V
A6	-179.NA	175.NA	3.40 V	-3.44 V
A7	-179.NA	172.NA	3.43 V	-3.44 V
CS1	-170.NA	167.NA	3.45 V	-3.47 V
CS2	-171.NA	176.NA	3.44 V	-3.48 V
MWR	-173.NA	164.NA	3.40 V	-3.41 V
MRD	-170.NA	164.NA	3.40 V	-3.42 V
DI0	-171.NA	174.NA	3.56 V	-3.50 V
DI1	-172.NA	172.NA	3.55 V	-3.48 V
DI2	-169.NA	164.NA	3.52 V	-3.48 V
DI3	-168.NA	166.NA	3.52 V	-3.46 V

	D00	D01	D02	D03
VOL1	155.MV	165.MV	175.MV	175.MV
VOL2	155.MV	170.MV	195.MV	190.MV
VOH1	4.78 V	4.78 V	4.77 V	4.77 V
VOH2	9.69 V	9.69 V	9.68 V	9.69 V
IDN1	4.75MA	4.55MA	4.30MA	4.25MA
IDN2	12.2MA	11.3MA	10.0MA	10.1MA
IDP1	-1.78MA	-1.77MA	-1.73MA	-1.75MA
IDP2	-4.13MA	-4.13MA	-3.99MA	-4.13MA
IOZ1	1.33UA	1.40UA	1.44UA	1.42UA
IOZ2	1.29UA	1.40UA	1.42UA	1.42UA
IOZ3	1.30UA	1.39UA	1.43UA	1.40UA
IOZ4	1.29UA	1.39UA	1.42UA	1.40UA
IOZ5	1.31UA	1.40UA	1.45UA	1.44UA
IOZ6	1.31UA	1.40UA	1.44UA	1.44UA
IOZ7	1.30UA	1.39UA	1.43UA	1.43UA
IOZ8	1.29UA	1.40UA	1.42UA	1.44UA
ILDP	50.0UA			
IL1	-185.UA			
IL2	-265.UA			
IL3	-165.UA			
IL4	-205.UA			

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN: 7

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	285.N	230.N	95.0N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	14.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	134.N	108.N	52.0N
ADDRESS HOLD TIME	(TAH)	-20.0N	-16.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	76.0N	62.0N	38.0N
CS1 SETUP TIME	(TCSS1)	178.N	152.N	76.0N
CS2 SETUP TIME	(TCSS2)	174.N	150.N	74.0N
CS1 HOLD TIME	(TCSH1)	38.0N	32.0N	22.0N
CS2 HOLD TIME	(TCSH2)	40.0N	36.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	266.N	224.N	100.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	264.N	220.N	98.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	56.0N	50.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	152.N	120.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	148.N	116.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	118.N	36.0N
OUTPUT HOLD FROM MWR	(TPDH)	138.N	114.N	36.0N
READ CYCLE TIME	(TRC)	288.N	240.N	128.N
WRITE CYCLE TIME	(TWC)	240.N	208.N	120.N

	IIL	IIH	VIC1	VIC2
A0	-1.30NA	1.50NA	2.93 V	-2.91 V
A1	-1.50NA	1.80NA	2.98 V	-3.00 V
A2	-1.40NA	1.40NA	2.99 V	-3.01 V
A3	-1.70NA	1.40NA	2.97 V	-3.02 V
A4	-1.30NA	1.40NA	3.01 V	-3.02 V
A5	-1.80NA	1.80NA	2.92 V	-2.94 V
A6	-1.70NA	1.40NA	2.94 V	-2.96 V
A7	-1.40NA	1.70NA	2.94 V	-2.94 V
CS1	-1.50NA	1.40NA	2.93 V	-2.95 V
CS2	-1.80NA	1.30NA	2.96 V	-2.99 V
MWR	-1.70NA	1.50NA	2.93 V	-2.98 V
MRD	-1.50NA	1.90NA	2.93 V	-2.94 V
DI0	-2.20NA	1.40NA	3.03 V	-2.98 V
DI1	-1.70NA	1.40NA	3.02 V	-2.96 V
DI2	-1.60NA	1.50NA	3.01 V	-2.97 V
DI3	-1.70NA	1.30NA	3.00 V	-2.97 V

	DO0	DO1	DO2	DO3
VOL1	115.MV	120.MV	125.MV	125.MV
VOL2	115.MV	130.MV	145.MV	135.MV
VOH1	4.84 V	4.84 V	4.84 V	4.84 V
VOH2	9.77 V	9.77 V	9.76 V	9.77 V
IDN1	6.35MA	6.10MA	5.85MA	5.95MA
IDN2	16.0MA	14.9MA	13.4MA	13.9MA
IDP1	-2.40MA	-2.42MA	-2.37MA	-2.44MA
IDP2	-5.33MA	-5.39MA	-5.24MA	-5.47MA
IOZ1	34.6NA	27.8NA	34.5NA	30.5NA
IOZ2	34.2NA	26.2NA	36.2NA	28.3NA
IOZ3	27.8NA	32.8NA	29.2NA	35.9NA
IOZ4	30.2NA	30.3NA	30.8NA	33.3NA
IOZ5	32.0NA	27.7NA	34.8NA	30.3NA
IOZ6	32.3NA	28.2NA	35.2NA	29.9NA
IOZ7	32.0NA	27.6NA	34.8NA	30.0NA
IOZ8	31.7NA	27.9NA	34.3NA	29.5NA
ILDP	1.00UA			
IL1	-20.0UA			
IL2	-20.0UA			
IL3	-5.00UA			
IL4	-5.00UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	290.N	225.N	85.0N
DATA SETUP TIME	(TDS)	26.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	14.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	128.N	104.N	46.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	76.0N	64.0N	34.0N
CS1 SETUP TIME	(TCSS1)	168.N	142.N	70.0N
CS2 SETUP TIME	(TCSS2)	166.N	142.N	68.0N
CS1 HOLD TIME	(TCSH1)	36.0N	32.0N	22.0N
CS2 HOLD TIME	(TCSH2)	40.0N	34.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	264.N	216.N	90.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	262.N	212.N	90.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	44.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	146.N	112.N	30.0N
OUTPUT HOLD FROM CS2	(TDOH2)	140.N	108.N	30.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	34.0N
OUTPUT HOLD FROM MWR	(TPDH)	134.N	110.N	32.0N
READ CYCLE TIME	(TRC)	272.N	224.N	120.N
WRITE CYCLE TIME	(TWC)	248.N	192.N	104.N

	IIL	IIH	VIC1	VIC2
A0	-200.PA	200.PA	3.01 V	-2.99 V
A1	-300.PA	300.PA	3.06 V	-3.09 V
A2	-200.PA	200.PA	3.07 V	-3.09 V
A3	-300.PA	200.PA	3.05 V	-3.10 V
A4	-200.PA	200.PA	3.09 V	-3.10 V
A5	-300.PA	300.PA	3.00 V	-3.03 V
A6	-300.PA	200.PA	3.02 V	-3.04 V
A7	-300.PA	300.PA	3.02 V	-3.02 V
CS1	-200.PA	300.PA	3.02 V	-3.03 V
CS2	-300.PA	200.PA	3.05 V	-3.07 V
MWR	-300.PA	200.PA	3.02 V	-3.06 V
MRD	-300.PA	400.PA	3.01 V	-3.02 V
DI0	-500.PA	200.PA	3.11 V	-3.05 V
DI1	-300.PA	200.PA	3.11 V	-3.04 V
DI2	-300.PA	200.PA	3.11 V	-3.05 V
DI3	-300.PA	300.PA	3.08 V	-3.05 V

	DO0	DO1	DO2	DO3
VOL1	105.MV	105.MV	110.MV	110.MV
VOL2	100.MV	110.MV	125.MV	115.MV
VOH1	4.86 V	4.87 V	4.86 V	4.86 V
VOH2	9.80 V	9.81 V	9.80 V	9.81 V
IDN1	7.15MA	6.85MA	6.60MA	6.75MA
IDN2	18.4MA	17.0MA	15.5MA	16.0MA
IDP1	=2.85MA	=2.88MA	=2.85MA	=2.91MA
IDP2	=6.31MA	=6.41MA	=6.21MA	=6.48MA
IOZ1	7.60NA	1.20NA	7.70NA	700.PA
IOZ2	4.20NA	3.80NA	4.90NA	2.70NA
IOZ3	4.50NA	4.50NA	3.00NA	5.20NA
IOZ4	8.20NA	1.20NA	6.60NA	1.90NA
IOZ5	2.00NA	6.00NA	2.40NA	5.50NA
IOZ6	2.10NA	6.40NA	2.40NA	5.20NA
IOZ7	2.00NA	6.10NA	2.30NA	5.50NA
IOZ8	1.80NA	6.60NA	2.40NA	5.20NA

ILDP	=200.NA
IL1	=20.0UA
IL2	=20.0UA
IL3	=5.00UA
IL4	=5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	280.N	215.N	80.0N
DATA SETUP TIME	(TDS)	30.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	14.0N	10.0N	4.0 N
ADDRESS SETUP TIME	(TAS2)	130.N	100.N	42.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	84.0N	70.0N	32.0N
CS1 SETUP TIME	(TCSS1)	168.N	134.N	64.0N
CS2 SETUP TIME	(TCSS2)	168.N	134.N	62.0N
CS1 HOLD TIME	(TCSH1)	48.0N	38.0N	20.0N
CS2 HOLD TIME	(TCSH2)	50.0N	38.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	272.N	210.N	88.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	268.N	210.N	88.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	48.0N	42.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	138.N	106.N	26.0N
OUTPUT HOLD FROM CS2	(TDOH2)	134.N	102.N	26.0N
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	114.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	134.N	110.N	32.0N
READ CYCLE TIME	(TRC)	248.N	208.N	112.N
WRITE CYCLE TIME	(TWC)	224.N	200.N	96.0N

	IIL	IIH	VIC1	VTC2
A0	0.00 A	100.PA	3.10 V	-3.08 V
A1	-100.PA	100.PA	3.15 V	-3.16 V
A2	0.00 A	100.PA	3.15 V	-3.17 V
A3	-100.PA	100.PA	3.14 V	-3.18 V
A4	0.00 A	100.PA	3.17 V	-3.17 V
A5	-100.PA	100.PA	3.09 V	-3.12 V
A6	-100.PA	100.PA	3.11 V	-3.13 V
A7	-100.PA	100.PA	3.11 V	-3.11 V
CS1	-100.PA	100.PA	3.11 V	-3.12 V
CS2	-100.PA	100.PA	3.13 V	-3.14 V
MWR	-100.PA	100.PA	3.11 V	-3.14 V
MRD	-100.PA	100.PA	3.11 V	-3.1[illegible] V
DI0	-100.PA	100.PA	3.19 V	-3.14 V
DI1	0.00 A	100.PA	3.19 V	-3.13 V
DI2	-100.PA	100.PA	3.18 V	-3.13 V
DI3	0.00 A	100.PA	3.16 V	-3.13 V

	DO0	DO1	DO2	DO3
VOL1	95.0MV	100.MV	100.MV	100.MV
VOL2	90.0MV	100.MV	110.MV	105.MV
VOH1	4.88 V	4.88 V	4.88 V	4.89 V
VOH2	9.84 V	9.84 V	9.84 V	9.84 V
IDN1	7.85MA	7.50MA	7.25MA	7.35MA
IDN2	20.5MA	19.0MA	17.4MA	17.9MA
IDP1	-3.25MA	-3.37MA	-3.30MA	-3.35MA
IDP2	-7.23MA	-7.44MA	-7.19MA	-7.49MA
IOZ1	4.60NA	200.PA	2.40NA	800.PA
IOZ2	5.50NA	-1.90NA	5.20NA	-1.80NA
IOZ3	-1.50NA	5.10NA	-1.80NA	5.30NA
IOZ4	300.PA	3.10NA	-900.PA	3.80NA
IOZ5	3.70NA	-1.10NA	4.10NA	-1.80NA
IOZ6	3.80NA	-1.20NA	3.90NA	-1.60NA
IOZ7	3.70NA	-900.PA	4.00NA	-1.80NA
IOZ8	3.70NA	-1.20NA	3.80NA	-1.70NA
ILDP	-15.0UA			
IL1	-15.0UA			
IL2	-15.0UA			
IL3	-5.00UA			
IL4	-5.00UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	280.N	235.N	100.N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	14.0N	14.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	134.N	114.N	58.0N
ADDRESS HOLD TIME	(TAH)	-20.0N	-16.0N	-6.00N
WRITE PULSE WIDTH	(TWP)	84.0N	74.0N	42.0N
CS1 SETUP TIME	(TCSS1)	186.N	162.N	84.0N
CS2 SETUP TIME	(TCSS2)	182.N	158.N	82.0N
CS1 HOLD TIME	(TCSH1)	50.0N	46.0N	28.0N
CS2 HOLD TIME	(TCSH2)	54.0N	48.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	272.N	232.N	112.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	268.N	230.N	110.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	60.0N	54.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	158.N	126.N	40.0N
OUTPUT HOLD FROM CS2	(TDOH2)	154.N	122.N	40.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	120.N	38.0N
OUTPUT HOLD FROM MWR	(TPDH)	140.N	116.N	40.0N
READ CYCLE TIME	(TRC)	304.N	256.N	136.N
WRITE CYCLE TIME	(TWC)	248.N	224.N	136.N

	IIL	IIH	VIC1	VIC2
A0	-17.8NA	18.8NA	2.89 V	-2.88 V
A1	-18.4NA	19.8NA	2.95 V	-2.97 V
A2	-17.8NA	18.8NA	2.96 V	-2.98 V
A3	-19.0NA	18.4NA	2.94 V	-2.99 V
A4	-17.6NA	18.1NA	2.98 V	-2.99 V
A5	-18.8NA	19.3NA	2.89 V	-2.91 V
A6	-18.8NA	18.2NA	2.91 V	-2.93 V
A7	-18.4NA	18.8NA	2.91 V	-2.91 V
CS1	-18.9NA	17.9NA	2.91 V	-2.91 V
CS2	-19.0NA	18.4NA	2.93 V	-2.97 V
MWR	-18.5NA	17.9NA	2.90 V	-2.95 V
MRD	-18.1NA	19.5NA	2.90 V	-2.91 V
DI0	-19.7NA	18.1NA	3.00 V	-2.94 V
DI1	-18.1NA	17.7NA	2.98 V	-2.93 V
DI2	-17.6NA	18.4NA	2.98 V	-2.94 V
DI3	-17.6NA	16.8NA	2.96 V	-2.94 V

	DO0	DO1	DO2	DO3
VOL1	135.MV	140.MV	150.MV	145.MV
VOL2	140.MV	150.MV	170.MV	160.MV
VOH1	4.80 V	4.81 V	4.80 V	4.80 V
VOH2	9.72 V	9.72 V	9.72 V	9.73 V
IDN1	5.50MA	5.25MA	5.05MA	5.15MA
IDN2	13.6MA	12.6MA	11.4MA	11.8MA
IDP1	-2.02MA	-2.05MA	-2.00MA	-2.06MA
IDP2	-4.50MA	-4.55MA	-4.41MA	-4.62MA
IOZ1	313.NA	300.NA	321.NA	335.NA
IOZ2	301.NA	304.NA	321.NA	330.NA
IOZ3	305.NA	302.NA	320.NA	333.NA
IOZ4	299.NA	299.NA	323.NA	326.NA
IOZ5	303.NA	307.NA	328.NA	339.NA
IOZ6	312.NA	297.NA	339.NA	328.NA
IOZ7	313.NA	300.NA	325.NA	340.NA
IOZ8	303.NA	305.NA	327.NA	328.NA
ILDP	15.0UA			
IL1	-35.0UA			
IL2	-35.0UA			
IL3	-20.0UA			
IL4	-15.0UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	290.N	245.N	110.N
DATA SETUP TIME	(TDS)	24.0N	22.0N	10.0N
DATA HOLD TIME	(TDH)	16.0N	16.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	4.00N	4.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	136.N	122.N	66.0N
ADDRESS HOLD TIME	(TAH)	-20.0N	-18.0N	-6.00N
WRITE PULSE WIDTH	(TWP)	92.0N	82.0N	46.0N
CS1 SETUP TIME	(TCSS1)	198.N	172.N	92.0N
CS2 SETUP TIME	(TCSS2)	194.N	170.N	88.0N
CS1 HOLD TIME	(TCSH1)	54.0N	48.0N	30.0N
CS2 HOLD TIME	(TCSH2)	60.0N	52.0N	30.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	288.N	248.N	126.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	284.N	246.N	122.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	64.0N	58.0N	34.0N
OUTPUT HOLD FROM CS1	(TDOH1)	160.N	130.N	44.0N
OUTPUT HOLD FROM CS2	(TDOH2)	156.N	126.N	42.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	120.N	38.0N
OUTPUT HOLD FROM MWR	(TPDH)	142.N	118.N	40.0N
READ CYCLE TIME	(TRC)	312.N	272.N	144.N
WRITE CYCLE TIME	(TWC)	256.N	232.N	144.N

	IIL	IIH	VIC1	VIC2
A0	-107.NA	109.NA	2.88 V	-2.86 V
A1	-107.NA	109.NA	2.94 V	-2.95 V
A2	-107.NA	107.NA	2.95 V	-2.97 V
A3	-108.NA	107.NA	2.93 V	-2.98 V
A4	-104.NA	101.NA	2.97 V	-2.98 V
A5	-108.NA	107.NA	2.87 V	-2.89 V
A6	-106.NA	103.NA	2.89 V	-2.91 V
A7	-106.NA	103.NA	2.89 V	-2.89 V
CS1	-109.NA	103.NA	2.89 V	-2.90 V
CS2	-104.NA	103.NA	2.92 V	-2.96 V
MWR	-108.NA	103.NA	2.89 V	-2.94 V
MRD	-104.NA	105.NA	2.88 V	-2.90 V
DI0	-105.NA	102.NA	2.98 V	-2.93 V
DI1	-104.NA	101.NA	2.97 V	-2.92 V
DI2	-99.5NA	101.NA	2.97 V	-2.93 V
DI3	-101.NA	98.3NA	2.95 V	-2.93 V

	D00	D01	D02	D03
VOL1	150.MV	160.MV	165.MV	160.MV
VOL2	155.MV	170.MV	190.MV	180.MV
VOH1	4.78 V	4.78 V	4.78 V	4.78 V
VOH2	9.69 V	9.69 V	9.68 V	9.69 V
IDN1	4.90MA	4.70MA	4.50MA	4.65MA
IDN2	12.2MA	11.2MA	10.1MA	10.5MA
IDP1	-1.81MA	-1.84MA	-1.80MA	-1.86MA
IDP2	-4.04MA	-4.08MA	-3.96MA	-4.15MA
IOZ1	1.31UA	1.25UA	1.38UA	1.38UA
IOZ2	1.28UA	1.26UA	1.36UA	1.39UA
IOZ3	1.30UA	1.25UA	1.38UA	1.38UA
IOZ4	1.28UA	1.25UA	1.36UA	1.39UA
IOZ5	1.30UA	1.26UA	1.40UA	1.41UA
IOZ6	1.31UA	1.26UA	1.39UA	1.40UA
IOZ7	1.30UA	1.26UA	1.38UA	1.40UA
IOZ8	1.29UA	1.26UA	1.37UA	1.40UA
ILDP	20.0UA			
IL1	-90.0UA			
IL2	-105.UA			
IL3	-80.0UA			
IL4	-65.0UA			

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN: A

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	285.N	205.N	75.0N
DATA SETUP TIME	(TDS)	24.0N	18.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	14.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	130.N	106.N	48.0N
ADDRESS HOLD TIME	(TAH)	-22.0N	-18.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	74.0N	66.0N	36.0N
CS1 SETUP TIME	(TCSS1)	170.N	144.N	68.0N
CS2 SETUP TIME	(TCSS2)	166.N	142.N	66.0N
CS1 HOLD TIME	(TCSH1)	38.0N	34.0N	22.0N
CS2 HOLD TIME	(TCSH2)	42.0N	36.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	266.N	218.N	94.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	264.N	216.N	90.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	54.0N	48.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	154.N	122.N	38.0N
OUTPUT HOLD FROM CS2	(TDOH2)	150.N	120.N	38.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	120.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	142.N	116.N	32.0N
READ CYCLE TIME	(TRC)	280.N	232.N	120.N
WRITE CYCLE TIME	(TWC)	256.N	192.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-1.90NA	1.70NA	2.99 V	-2.98 V
A1	-1.60NA	1.70NA	3.01 V	-3.03 V
A2	-1.60NA	1.80NA	3.05 V	-3.09 V
A3	-1.70NA	1.50NA	3.04 V	-3.07 V
A4	-1.80NA	1.90NA	3.04 V	-3.08 V
A5	-1.80NA	1.90NA	2.99 V	-3.03 V
A6	-1.50NA	2.80NA	3.01 V	-3.05 V
A7	-2.00NA	2.40NA	3.01 V	-3.03 V
CS1	-1.90NA	1.90NA	3.04 V	-3.04 V
CS2	-1.80NA	1.80NA	3.06 V	-3.09 V
MWR	-1.60NA	1.70NA	2.98 V	-2.99 V
MRD	-2.10NA	2.20NA	3.00 V	-3.01 V
DI0	-2.10NA	2.40NA	3.13 V	-3.08 V
DI1	-2.10NA	1.90NA	3.12 V	-3.06 V
DI2	-3.00NA	2.20NA	3.12 V	-3.09 V
DI3	-1.90NA	2.10NA	3.11 V	-3.07 V

	DO0	DO1	DO2	DO3
VOL1	120.MV	125.MV	130.MV	125.MV
VOL2	115.MV	130.MV	145.MV	140.MV
VOH1	4.84 V	4.84 V	4.84 V	4.84 V
VOH2	9.78 V	9.78 V	9.77 V	9.78 V
IDN1	6.15MA	5.95MA	5.60MA	5.80MA
IDN2	16.1MA	14.8MA	13.0MA	13.6MA
IDP1	-2.47MA	-2.45MA	-2.43MA	-2.50MA
IDP2	-5.59MA	-5.57MA	-5.43MA	-5.72MA
IOZ1	32.0NA	15.7NA	58.5NA	16.9NA
IOZ2	28.2NA	16.8NA	57.0NA	16.5NA
IOZ3	24.6NA	20.7NA	52.5NA	22.3NA
IOZ4	27.6NA	17.6NA	53.8NA	20.0NA
IOZ5	26.2NA	17.8NA	54.1NA	18.6NA
IOZ6	26.8NA	18.0NA	55.5NA	18.0NA
IOZ7	27.3NA	17.5NA	55.3NA	18.1NA
IOZ8	26.5NA	18.0NA	58.6NA	17.7NA

ILDP	-5.00UA
IL1	-15.0UA
IL2	-15.0UA
IL3	-65.0UA
IL4	-50.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	295.N	220.N	80.0N
DATA SETUP TIME	(TDS)	28.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	18.0N	14.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	130.N	104.N	42.0N
ADDRESS HOLD TIME	(TAH)	-22.0N	-18.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	78.0N	60.0N	32.0N
CS1 SETUP TIME	(TCSS1)	170.N	142.N	62.0N
CS2 SETUP TIME	(TCSS2)	166.N	138.N	62.0N
CS1 HOLD TIME	(TCSH1)	44.0N	36.0N	22.0N
CS2 HOLD TIME	(TCSH2)	46.0N	38.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	276.N	216.N	86.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	274.N	214.N	82.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	44.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	148.N	114.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	144.N	112.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	30.0N
OUTPUT HOLD FROM MWR	(TPOH)	138.N	114.N	30.0N
READ CYCLE TIME	(TRC)	264.N	216.N	112.N
WRITE CYCLE TIME	(TWC)	272.N	208.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-300.PA	300.PA	3.10 V	-3.09 V
A1	-300.PA	300.PA	3.12 V	-3.13 V
A2	-300.PA	300.PA	3.15 V	-3.18 V
A3	-400.PA	300.PA	3.14 V	-3.17 V
A4	-400.PA	300.PA	3.14 V	-3.18 V
A5	-300.PA	300.PA	3.10 V	-3.13 V
A6	-300.PA	500.PA	3.11 V	-3.15 V
A7	-400.PA	500.PA	3.12 V	-3.13 V
CS1	-400.PA	400.PA	3.14 V	-3.14 V
CS2	-400.PA	300.PA	3.16 V	-3.18 V
MWR	-300.PA	300.PA	3.09 V	-3.11 V
MRD	-400.PA	500.PA	3.11 V	-3.11 V
DI0	-400.PA	600.PA	3.23 V	-3.17 V
DI1	-500.PA	400.PA	3.21 V	-3.16 V
DI2	-700.PA	400.PA	3.21 V	-3.17 V
DI3	-300.PA	300.PA	3.20 V	-3.16 V

	DO0	DO1	DO2	DO3
VOL1	110.MV	110.MV	115.MV	115.MV
VOL2	105.MV	115.MV	125.MV	120.MV
VOH1	4.87 V	4.87 V	4.86 V	4.87 V
VOH2	9.82 V	9.81 V	9.80 V	9.82 V
IDN1	6.75MA	6.55MA	6.25MA	6.40MA
IDN2	18.3MA	16.8MA	15.0MA	15.5MA
IDP1	-2.89MA	-2.88MA	-2.85MA	-2.94MA
IDP2	-6.58MA	-6.57MA	-6.40MA	-6.73MA
IOZ1	9.90NA	2.40NA	25.1NA	3.20NA
IOZ2	10.7NA	500.PA	33.2NA	500.PA
IOZ3	4.00NA	7.70NA	26.9NA	7.40NA
IOZ4	6.10NA	5.50NA	27.0NA	6.00NA
IOZ5	9.20NA	1.10NA	32.2NA	800.PA
IOZ6	9.10NA	1.30NA	31.0NA	500.PA
IOZ7	9.40NA	1.00NA	33.4NA	600.PA
IOZ8	9.30NA	1.10NA	30.7NA	500.PA

ILDP	-15.0UA
IL1	-15.0UA
IL2	-10.0UA
IL3	-50.0UA
IL4	-40.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	295.N	215.N	70.0N
DATA SETUP TIME	(TDS)	34.0N	24.0N	8.00N
DATA HOLD TIME	(TDH)	6.00N	6.00N	8.00N
ADDRESS SETUP TIME	(TAS1)	14.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	130.N	102.N	38.0N
ADDRESS HOLD TIME	(TAH)	-24.0N	-18.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	88.0N	72.0N	32.0N
CS1 SETUP TIME	(TCSS1)	172.N	138.N	60.0N
CS2 SETUP TIME	(TCSS2)	158.N	134.N	52.0N
CS1 HOLD TIME	(TCSH1)	54.0N	42.0N	28.0N
CS2 HOLD TIME	(TCSH2)	58.0N	44.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	300.N	214.N	80.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	298.N	212.N	80.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	42.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	142.N	110.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	140.N	108.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	138.N	112.N	28.0N
READ CYCLE TIME	(TRC)	264.N	208.N	104.N
WRITE CYCLE TIME	(TWC)	232.N	192.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-100.PA	100.PA	3.20 V	-3.19 V
A1	-100.PA	100.PA	3.22 V	-3.24 V
A2	-100.PA	100.PA	3.25 V	-3.29 V
A3	-100.PA	100.PA	3.25 V	-3.27 V
A4	-100.PA	100.PA	3.24 V	-3.28 V
A5	-500.PA	100.PA	3.20 V	-3.23 V
A6	-100.PA	200.PA	3.21 V	-3.25 V
A7	-100.PA	100.PA	3.21 V	-3.24 V
CS1	-100.PA	100.PA	3.25 V	-3.25 V
CS2	-100.PA	100.PA	3.26 V	-3.28 V
MWR	-100.PA	100.PA	3.20 V	-3.21 V
MRD	-200.PA	100.PA	3.21 V	-3.21 V
DI0	-100.PA	100.PA	3.34 V	-3.28 V
DI1	-100.PA	100.PA	3.31 V	-3.26 V
DI2	-200.PA	100.PA	3.31 V	-3.27 V
DI3	-100.PA	100.PA	3.30 V	-3.25 V

	D00	D01	D02	D03
VOL1	[illegible]MV	105.MV	110.MV	105.MV
VOL2	9[illegible]	100.MV	115.MV	110.MV
VOH1	4.88 V	4.88 V	4.88 V	4.88 V
VOH2	9.84 V	9.84 V	9.84 V	9.84 V
IDN1	7.30MA	7.10MA	6.75MA	6.90MA
IDN2	20.0MA	18.6MA	16.6MA	17.3MA
IDP1	-3.32MA	-3.33MA	-3.27MA	-3.40MA
IDP2	-7.54MA	-7.58MA	-7.35MA	-7.76MA
IOZ1	800.PA	5.20NA	16.6NA	5.40NA
IOZ2	3.30NA	2.00NA	20.2NA	2.90NA
IOZ3	3.60NA	1.10NA	24.6NA	-300.PA
IOZ4	-100.PA	4.90NA	18.0NA	3.40NA
IOZ5	6.10NA	-300.PA	20.9NA	200.PA
IOZ6	6.00NA	-400.PA	18.7NA	200.PA
IOZ7	6.20NA	-400.PA	18.5NA	-100.PA
IOZ8	6.20NA	-600.PA	18.9NA	-100.PA
ILDP	-5.00UA			
IL1	-10.0UA			
IL2	-10.0UA			
IL3	-45.0UA			
IL4	-35.0UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	270.N	225.N	95.0N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	130.N	106.N	54.0N
ADDRESS HOLD TIME	(TAH)	-20.0N	-18.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	84.0N	72.0N	40.0N
CS1 SETUP TIME	(TCSS1)	178.N	150.N	74.0N
CS2 SETUP TIME	(TCSS2)	172.N	148.N	72.0N
CS1 HOLD TIME	(TCSH1)	52.0N	46.0N	26.0N
CS2 HOLD TIME	(TCSH2)	54.0N	48.0N	26.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	258.N	220.N	104.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	256.N	218.N	102.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	58.0N	50.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	158.N	126.N	42.0N
OUTPUT HOLD FROM CS2	(TDOH2)	154.N	124.N	42.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	120.N	34.0N
OUTPUT HOLD FROM MWR	(TPDH)	142.N	116.N	34.0N
READ CYCLE TIME	(TRC)	288.N	248.N	120.N
WRITE CYCLE TIME	(TWC)	232.N	200.N	120.N

	IIL	IIH	VIC1	VIC2
A0	-20.2NA	20.8NA	2.93 V	-2.92 V
A1	-19.3NA	20.5NA	2.95 V	-2.97 V
A2	-19.6NA	20.6NA	2.99 V	-3.02 V
A3	-19.9NA	19.5NA	2.97 V	-3.00 V
A4	-20.0NA	20.9NA	2.97 V	-3.01 V
A5	-21.3NA	21.0NA	2.93 V	-2.96 V
A6	-19.3NA	24.5NA	2.95 V	-2.99 V
A7	-21.4NA	22.8NA	2.95 V	-2.97 V
CS1	-20.9NA	21.9NA	2.98 V	-2.98 V
CS2	-19.5NA	21.5NA	3.00 V	-3.03 V
MWR	-18.7NA	19.8NA	2.91 V	-2.93 V
MRD	-21.8NA	22.2NA	2.94 V	-2.94 V
DI0	-20.4NA	24.7NA	3.08 V	-3.02 V
DI1	-21.0NA	22.4NA	3.05 V	-3.00 V
DI2	-21.9NA	23.1NA	3.05 V	-3.02 V
DI3	-20.2NA	22.0NA	3.04 V	-3.01 V

	DO0	DO1	DO2	DO3
VOL1	135.MV	140.MV	150.MV	145.MV
VOL2	140.MV	150.MV	170.MV	165.MV
VOH1	4.81 V	4.80 V	4.80 V	4.82 V
VOH2	9.73 V	9.73 V	9.72 V	9.74 V
IDN1	5.40MA	5.20MA	4.90MA	5.05MA
IDN2	13.8MA	12.6MA	11.2MA	11.6MA
IDP1	-2.10MA	-2.08MA	-2.04MA	-2.12MA
IDP2	-4.74MA	-4.72MA	-4.53MA	-4.85MA
IOZ1	158.NA	148.NA	230.NA	157.NA
IOZ2	161.NA	142.NA	231.NA	160.NA
IOZ3	154.NA	141.NA	233.NA	158.NA
IOZ4	157.NA	145.NA	227.NA	166.NA
IOZ5	161.NA	145.NA	223.NA	164.NA
IOZ6	151.NA	157.NA	221.NA	165.NA
IOZ7	151.NA	144.NA	228.NA	156.NA
IOZ8	155.NA	146.NA	221.NA	167.NA

ILDP	6.80UA
IL1	-35.0UA
IL2	-40.0UA
IL3	-85.0UA
IL4	-70.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	270.N	230.N	100.N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	14.0N	12.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	4.00N	6.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	132.N	112.N	60.0N
ADDRESS HOLD TIME	(TAH)	-20.0N	-18.0N	-6.00N
WRITE PULSE WIDTH	(TWP)	88.0N	78.0N	44.0N
CS1 SETUP TIME	(TCSS1)	182.N	158.N	82.0N
CS2 SETUP TIME	(TCSS2)	178.N	154.N	78.0N
CS1 HOLD TIME	(TCSH1)	54.0N	48.0N	30.0N
CS2 HOLD TIME	(TCSH2)	58.0N	50.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	270.N	234.N	114.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	266.N	230.N	112.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	60.0N	54.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	158.N	128.N	44.0N
OUTPUT HOLD FROM CS2	(TDOH2)	156.N	124.N	44.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	122.N	36.0N
OUTPUT HOLD FROM MWR	(TPDH)	144.N	118.N	38.0N
READ CYCLE TIME	(TRC)	296.N	256.N	128.N
WRITE CYCLE TIME	(TWC)	232.N	208.N	136.N

	IIL	IIH	VIC1	VIC2
A0	-117.NA	118.NA	2.89 V	-2.89 V
A1	-116.NA	120.NA	2.92 V	-2.94 V
A2	-117.NA	119.NA	2.96 V	-3.00 V
A3	-115.NA	115.NA	2.94 V	-2.97 V
A4	-115.NA	118.NA	2.94 V	-2.98 V
A5	-120.NA	119.NA	2.90 V	-2.93 V
A6	-113.NA	124.NA	2.92 V	-2.96 V
A7	-115.NA	119.NA	2.93 V	-2.94 V
CS1	-118.NA	121.NA	2.95 V	-2.94 V
CS2	-114.NA	121.NA	2.97 V	-3.00 V
MWR	-113.NA	114.NA	2.88 V	-2.89 V
MRD	-119.NA	120.NA	2.90 V	-2.91 V
DI0	-116.NA	126.NA	3.05 V	-2.99 V
DI1	-118.NA	119.NA	3.02 V	-2.97 V
DI2	-116.NA	118.NA	3.02 V	-3.00 V
DI3	-113.NA	117.NA	3.01 V	-2.98 V

	DO0	DO1	DO2	DO3
VOL1	150.MV	155.MV	170.MV	165.MV
VOL2	155.MV	170.MV	195.MV	185.MV
VOH1	4.79 V	4.79 V	4.78 V	4.79 V
VOH2	9.70 V	9.70 V	9.69 V	9.71 V
IDN1	4.85MA	4.70MA	4.40MA	4.55MA
IDN2	12.3MA	11.3MA	9.95MA	10.4MA
IDP1	-1.88MA	-1.88MA	-1.85MA	-1.92MA
IDP2	-4.24MA	-4.23MA	-4.09MA	-4.33MA
IOZ1	484.NA	550.NA	646.NA	601.NA
IOZ2	467.NA	539.NA	650.NA	590.NA
IOZ3	464.NA	539.NA	645.NA	589.NA
IOZ4	465.NA	531.NA	654.NA	582.NA
IOZ5	469.NA	542.NA	658.NA	600.NA
IOZ6	477.NA	531.NA	659.NA	596.NA
IOZ7	469.NA	540.NA	645.NA	599.NA
IOZ8	460.NA	535.NA	662.NA	588.NA

ILDP	40.0UA
IL1	-95.0UA
IL2	-115.UA
IL3	-150.UA
IL4	-125.UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	230.N	195.N	85.0N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	12.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	112.N	94.0N	46.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	66.0N	60.0N	36.0N
CS1 SETUP TIME	(TCSS1)	158.N	136.N	68.0N
CS2 SETUP TIME	(TCSS2)	154.N	132.N	64.0N
CS1 HOLD TIME	(TCSH1)	40.0N	36.0N	22.0N
CS2 HOLD TIME	(TCSH2)	42.0N	36.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	226.N	192.N	90.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	224.N	188.N	90.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	44.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	146.N	114.N	32.0N
OUTPUT HOLD FROM CS2	(TDOH2)	142.N	112.N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	116.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	136.N	112.N	32.0N
READ CYCLE TIME	(TRC)	248.N	208.N	120.N
WRITE CYCLE TIME	(TWC)	280.N	184.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-2.60NA	1.60NA	2.81 V	-2.82 V
A1	-1.50NA	1.20NA	2.85 V	-2.87 V
A2	-1.70NA	1.50NA	2.88 V	-2.91 V
A3	-1.80NA	1.60NA	2.87 V	-2.89 V
A4	-1.90NA	1.50NA	2.89 V	-2.93 V
A5	-1.70NA	1.20NA	2.84 V	-2.87 V
A6	-1.50NA	1.50NA	2.84 V	-2.87 V
A7	-1.80NA	1.40NA	2.86 V	-2.88 V
CS1	-1.40NA	1.40NA	2.89 V	-2.89 V
CS2	-1.50NA	1.90NA	2.93 V	-2.93 V
MWR	-1.80NA	8.10NA	2.84 V	-2.86 V
MRD	-1.60NA	1.40NA	2.87 V	-2.86 V
DI0	-1.50NA	1.30NA	2.97 V	-2.93 V
DI1	-1.50NA	1.30NA	2.94 V	-2.89 V
DI2	-2.10NA	1.70NA	2.97 V	-2.91 V
DI3	-2.20NA	1.50NA	2.94 V	-2.89 V

	DO0	DO1	DO2	DO3
VOL1	100.MV	105.MV	110.MV	110.MV
VOL2	105.MV	115.MV	130.MV	130.MV
VOH1	4.86 V	4.86 V	4.85 V	4.86 V
VOH2	9.79 V	9.79 V	9.78 V	9.80 V
IDN1	7.40MA	7.05MA	6.60MA	6.70MA
IDN2	17.9MA	16.3MA	14.4MA	14.9MA
IDP1	-2.67MA	-2.66MA	-2.61MA	-2.68MA
IDP2	-5.88MA	-5.91MA	-5.72MA	-5.97MA
IOZ1	18.2NA	25.4NA	19.9NA	26.6NA
IOZ2	19.9NA	23.1NA	20.7NA	24.7NA
IOZ3	22.4NA	19.9NA	25.1NA	19.0NA
IOZ4	19.4NA	22.6NA	22.2NA	22.2NA
IOZ5	22.2NA	21.5NA	22.7NA	23.3NA
IOZ6	21.8NA	21.7NA	23.0NA	23.3NA
IOZ7	22.0NA	21.9NA	22.5NA	23.4NA
IOZ8	21.3NA	21.6NA	22.6NA	23.5NA

ILDP	-5.00UA
IL1	-20.0UA
IL2	-5.00UA
IL3	-20.0UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	240.N	195.N	75.0N
DATA SETUP TIME	(TDS)	26.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	110.N	90.0N	42.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	72.0N	58.0N	32.0N
CS1 SETUP TIME	(TCSS1)	154.N	130.N	62.0N
CS2 SETUP TIME	(TCSS2)	150.N	126.N	60.0N
CS1 HOLD TIME	(TCSH1)	38.0N	32.0N	22.0N
CS2 HOLD TIME	(TCSH2)	38.0N	32.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	226.N	186.N	86.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	224.N	184.N	82.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	46.0N	40.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	138.N	106.N	30.0N
OUTPUT HOLD FROM CS2	(TDOH2)	136.N	106.N	30.0N
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	116.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	110.N	30.0N
READ CYCLE TIME	(TRC)	232.N	200.N	112.N
WRITE CYCLE TIME	(TWC)	200.N	176.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-500.PA	200.PA	2.91 V	-2.93 V
A1	-200.PA	200.PA	2.95 V	-2.96 V
A2	-400.PA	200.PA	2.98 V	-3.00 V
A3	-300.PA	200.PA	2.97 V	-2.99 V
A4	-300.PA	200.PA	2.99 V	-3.02 V
A5	-300.PA	200.PA	2.94 V	-2.96 V
A6	-200.PA	200.PA	2.94 V	-2.97 V
A7	-300.PA	200.PA	2.96 V	-2.97 V
CS1	-200.PA	200.PA	2.98 V	-2.98 V
CS2	-200.PA	300.PA	3.02 V	-3.02 V
MWR	-300.PA	1.70NA	2.94 V	-2.95 V
MRD	-200.PA	200.PA	2.97 V	-2.95 V
DI0	-200.PA	200.PA	3.07 V	-3.03 V
DI1	-200.PA	200.PA	3.04 V	-2.99 V
DI2	-400.PA	300.PA	3.07 V	-3.00 V
DI3	-400.PA	200.PA	3.04 V	-2.98 V

	D00	D01	D02	D03
VOL1	85.0MV	95.0MV	100.MV	95.0MV
VOL2	90.0MV	100.MV	115.MV	110.MV
VOH1	4.88 V	4.88 V	4.88 V	4.88 V
VOH2	9.82 V	9.83 V	9.82 V	9.82 V
IDN1	8.35MA	7.90MA	7.45MA	7.55MA
IDN2	20.5MA	18.7MA	16.7MA	17.1MA
IDP1	-3.16MA	-3.14MA	-3.14MA	-3.17MA
IDP2	-6.91MA	-6.97MA	-6.79MA	-7.04MA
IOZ1	3.20NA	4.30NA	4.00NA	2.80NA
IOZ2	600.PA	7.40NA	900.PA	6.30NA
IOZ3	7.70NA	300.PA	6.50NA	1.30NA
IOZ4	6.10NA	400.PA	6.80NA	200.PA
IOZ5	500.PA	6.70NA	500.PA	7.40NA
IOZ6	800.PA	6.90NA	300.PA	7.10NA
IOZ7	400.PA	6.80NA	500.PA	7.30NA
IOZ8	500.PA	7.00NA	200.PA	7.20NA

ILDP	-5.00UA
IL1	-15.0UA
IL2	-5.00UA
IL3	-15.0UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	240.N	185.N	70.0N
DATA SETUP TIME	(TDS)	32.0N	24.0N	8.00N
DATA HOLD TIME	(TDH)	6.00N	6.00N	8.00N
ADDRESS SETUP TIME	(TAS1)	14.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	110.N	88.0N	38.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	64.0N	62.0N	32.0N
CS1 SETUP TIME	(TCSS1)	152.N	126.N	58.0N
CS2 SETUP TIME	(TCSS2)	150.N	122.N	56.0N
CS1 HOLD TIME	(TCSH1)	46.0N	38.0N	22.0N
CS2 HOLD TIME	(TCSH2)	42.0N	36.0N	18.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	230.N	182.N	82.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	228.N	182.N	80.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	44.0N	38.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	132.N	100.N	22.0N
OUTPUT HOLD FROM CS2	(TDOH2)	132.N	100.N	28.0N
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	114.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	108.N	28.0N
READ CYCLE TIME	(TRC)	216.N	184.N	104.N
WRITE CYCLE TIME	(TWC)	248.N	176.N	96.0N

	IIL	IIH	VTC1	VTC2
A0	-100.PA	100.PA	3.01 V	-3.02 V
A1	0.00 A	100.PA	3.05 V	-3.06 V
A2	-100.PA	0.00 A	3.08 V	-3.10 V
A3	0.00 A	100.PA	3.08 V	-3.09 V
A4	-100.PA	0.00 A	3.09 V	-3.12 V
A5	0.00 A	100.PA	3.03 V	-3.06 V
A6	-100.PA	100.PA	3.04 V	-3.06 V
A7	-100.PA	100.PA	3.05 V	-3.06 V
CS1	-100.PA	100.PA	3.08 V	-3.08 V
CS2	-100.PA	100.PA	3.12 V	-3.12 V
MWR	-100.PA	400.PA	3.04 V	-3.05 V
MRD	-100.PA	100.PA	3.06 V	-3.05 V
DI0	0.00 A	0.00 A	3.16 V	-3.12 V
DI1	0.00 A	0.00 A	3.14 V	-3.08 V
DI2	-100.PA	100.PA	3.16 V	-3.10 V
DI3	-100.PA	100.PA	3.13 V	-3.08 V

	D00	D01	D02	D03
VOL1	80.0MV	85.0MV	90.0MV	90.0MV
VOL2	85.0MV	90.0MV	100.MV	100.MV
VOH1	4.89 V	4.89 V	4.89 V	4.89 V
VOH2	9.85 V	9.85 V	9.84 V	9.85 V
IDN1	9.10MA	8.65MA	8.15MA	8.25MA
IDN2	22.6MA	20.8MA	18.7MA	19.1MA
IDP1	-3.60MA	-3.64MA	-3.63MA	-3.67MA
IDP2	-7.92MA	-8.09MA	-7.86MA	-8.11MA
IOZ1	-800.PA	5.80NA	-1.10NA	4.50NA
IOZ2	-100.PA	3.90NA	-1.20NA	4.20NA
IOZ3	4.00NA	-1.20NA	4.20NA	-1.70NA
IOZ4	400.PA	2.30NA	900.PA	1.60NA
IOZ5	2.50NA	1.10NA	1.60NA	2.00NA
IOZ6	2.80NA	1.20NA	1.30NA	1.90NA
IOZ7	2.40NA	1.20NA	1.50NA	2.10NA
IOZ8	2.80NA	1.20NA	1.20NA	1.90NA
ILDP	-5.00UA			
IL1	-15.0UA			
IL2	-5.00UA			
IL3	-15.0UA			
IL4	-5.00UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	230.N	195.N	90.0N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	114.N	100.N	52.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	78.0N	70.0N	40.0N
CS1 SETUP TIME	(TCSS1)	164.N	140.N	74.0N
CS2 SETUP TIME	(TCSS2)	160.N	136.N	70.0N
CS1 HOLD TIME	(TCSH1)	48.0N	44.0N	28.0N
CS2 HOLD TIME	(TCSH2)	50.0N	46.0N	26.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	228.N	200.N	102.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	224.N	198.N	100.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	52.0N	48.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	148.N	118.N	36.0N
OUTPUT HOLD FROM CS2	(TDOH2)	146.N	116.N	36.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	34.0N
OUTPUT HOLD FROM MWR	(TPDH)	136.N	114.N	32.0N
READ CYCLE TIME	(TRC)	256.N	216.N	128.N
WRITE CYCLE TIME	(TWC)	216.N	192.N	120.N

	IIL	IIH	VIC1	VIC2
A0	-24.8NA	22.5NA	2.77 V	-2.77 V
A1	-22.1NA	21.0NA	2.80 V	-2.82 V
A2	-21.9NA	22.4NA	2.84 V	-2.87 V
A3	-22.0NA	22.5NA	2.83 V	-2.85 V
A4	-23.1NA	22.0NA	2.85 V	-2.89 V
A5	-22.7NA	21.2NA	2.78 V	-2.82 V
A6	-22.5NA	22.3NA	2.79 V	-2.83 V
A7	-22.6NA	21.8NA	2.81 V	-2.83 V
CS1	-22.1NA	21.7NA	2.85 V	-2.85 V
CS2	-21.9NA	24.0NA	2.89 V	-2.89 V
MWR	-22.0NA	39.6NA	2.79 V	-2.81 V
MRD	-22.1NA	21.7NA	2.83 V	-2.81 V
DI0	-21.4NA	21.6NA	2.93 V	-2.89 V
DI1	-21.6NA	21.4NA	2.91 V	-2.86 V
DI2	-22.5NA	22.1NA	2.93 V	-2.88 V
DI3	-23.2NA	22.0NA	2.91 V	-2.86 V

	D00	D01	D02	D03
VOL1	115.MV	120.MV	130.MV	130.MV
VOL2	125.MV	140.MV	155.MV	150.MV
VOH1	4.82 V	4.82 V	4.82 V	4.82 V
VOH2	9.75 V	9.75 V	9.74 V	9.75 V
IDN1	6.40MA	6.05MA	5.70MA	5.75MA
IDN2	15.3MA	13.8MA	12.2MA	12.6MA
IDP1	-2.23MA	-2.23MA	-2.21MA	-2.25MA
IDP2	-4.93MA	-4.95MA	-4.81MA	-5.02MA
IOZ1	206.NA	208.NA	219.NA	201.NA
IOZ2	208.NA	205.NA	216.NA	207.NA
IOZ3	203.NA	204.NA	219.NA	203.NA
IOZ4	209.NA	203.NA	213.NA	209.NA
IOZ5	207.NA	204.NA	222.NA	211.NA
IOZ6	206.NA	216.NA	209.NA	214.NA
IOZ7	199.NA	212.NA	217.NA	203.NA
IOZ8	210.NA	206.NA	217.NA	211.NA

ILDP	5.80UA
IL1	-40.0UA
IL2	-20.0UA
IL3	-40.0UA
IL4	-15.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	235.N	205.N	100.N
DATA SETUP TIME	(TDS)	24.0N	20.0N	10.0N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	6.00N	6.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	120.N	108.N	60.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-16.0N	-6.00N
WRITE PULSE WIDTH	(TWP)	82.0N	74.0N	44.0N
CS1 SETUP TIME	(TCSS1)	170.N	150.N	80.0N
CS2 SETUP TIME	(TCSS2)	164.N	144.N	78.0N
CS1 HOLD TIME	(TCSH1)	50.0N	46.0N	30.0N
CS2 HOLD TIME	(TCSH2)	54.0N	48.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	242.N	214.N	114.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	238.N	210.N	112.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	56.0N	50.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	152.N	120.N	38.0N
OUTPUT HOLD FROM CS2	(TDOH2)	148.N	118.N	38.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	36.0N
OUTPUT HOLD FROM MWR	(TPDH)	138.N	116.N	36.0N
READ CYCLE TIME	(TRC)	256.N	232.N	128.N
WRITE CYCLE TIME	(TWC)	224.N	200.N	128.N

	IIL	IIH	VIC1	VIC2
A0	-136.NA	132.NA	2.74 V	-2.75 V
A1	-132.NA	126.NA	2.77 V	-2.79 V
A2	-130.NA	133.NA	2.81 V	-2.85 V
A3	-130.NA	130.NA	2.80 V	-2.83 V
A4	-132.NA	127.NA	2.83 V	-2.86 V
A5	-135.NA	128.NA	2.76 V	-2.79 V
A6	-135.NA	130.NA	2.77 V	-2.80 V
A7	-133.NA	128.NA	2.79 V	-2.81 V
CS1	-135.NA	127.NA	2.82 V	-2.83 V
CS2	-131.NA	135.NA	2.87 V	-2.88 V
MWR	-131.NA	152.NA	2.76 V	-2.79 V
MRD	-130.NA	128.NA	2.80 V	-2.79 V
DI0	-128.NA	131.NA	2.91 V	-2.88 V
DI1	-130.NA	128.NA	2.89 V	-2.84 V
DI2	-131.NA	127.NA	2.91 V	-2.86 V
DI3	-131.NA	129.NA	2.89 V	-2.83 V

	DO0	DO1	DO2	DO3
VOL1	130.MV	135.MV	145.MV	145.MV
VOL2	140.MV	155.MV	175.MV	170.MV
VOH1	4.80 V	4.80 V	4.80 V	4.80 V
VOH2	9.72 V	9.72 V	9.71 V	9.72 V
IDN1	5.75MA	5.45MA	5.10MA	5.15MA
IDN2	13.6MA	12.4MA	11.0MA	11.3MA
IDP1	-2.00MA	-2.03MA	-1.99MA	-2.02MA
IDP2	-4.42MA	-4.47MA	-4.32MA	-4.49MA
IOZ1	850.NA	874.NA	853.NA	835.NA
IOZ2	831.NA	865.NA	853.NA	826.NA
IOZ3	827.NA	863.NA	849.NA	827.NA
IOZ4	826.NA	857.NA	853.NA	820.NA
IOZ5	833.NA	872.NA	867.NA	844.NA
IOZ6	847.NA	860.NA	867.NA	836.NA
IOZ7	835.NA	870.NA	854.NA	841.NA
IOZ8	830.NA	861.NA	861.NA	824.NA

ILDP	30.0UA
IL1	-115.UA
IL2	-120.UA
IL3	-110.UA
IL4	-75.0UA

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN: 10

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	200.N	170.N	75.0N
DATA SETUP TIME	(TDS)	24.0N	18.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	98.0N	86.0N	42.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	70.0N	60.0N	36.0N
CS1 SETUP TIME	(TCSS1)	150.N	130.N	66.0N
CS2 SETUP TIME	(TCSS2)	146.N	126.N	62.0N
CS1 HOLD TIME	(TCSH1)	44.0N	38.0N	24.0N
CS2 HOLD TIME	(TCSH2)	46.0N	40.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	194.N	168.N	86.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	190.N	166.N	82.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	44.0N	40.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	132.N	102.N	26.0N
OUTPUT HOLD FROM CS2	(TDOH2)	130.N	102.N	26.0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	114.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	130.N	108.N	30.0N
READ CYCLE TIME	(TRC)	216.N	184.N	112.N
WRITE CYCLE TIME	(TWC)	200.N	176.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-1.90NA	1.70NA	2.95 V	-2.94 V
A1	-2.30NA	2.20NA	3.00 V	-3.00 V
A2	-1.60NA	2.00NA	2.96 V	-3.00 V
A3	-2.00NA	1.90NA	2.97 V	-3.00 V
A4	-1.80NA	2.00NA	2.99 V	-3.04 V
A5	-1.80NA	1.50NA	2.95 V	-2.98 V
A6	-2.00NA	1.80NA	2.97 V	-3.02 V
A7	-1.50NA	2.10NA	2.97 V	-3.00 V
CS1	-1.80NA	1.60NA	2.96 V	-2.98 V
CS2	-2.20NA	1.60NA	3.00 V	-3.03 V
MWR	-1.80NA	1.70NA	2.93 V	-2.96 V
MRD	-2.20NA	2.10NA	2.96 V	-2.98 V
DI0	-1.70NA	1.70NA	3.09 V	-3.01 V
DI1	-1.80NA	1.70NA	3.05 V	-2.99 V
DI2	-2.00NA	2.00NA	3.05 V	-3.01 V
DI3	-1.90NA	1.70NA	3.03 V	-3.02 V

	DO0	DO1	DO2	DO3
VOL1	85.0MV	90.0MV	95.0MV	95.0MV
VOL2	95.0MV	105.MV	120.MV	120.MV
VOH1	4.86 V	4.86 V	4.86 V	4.86 V
VOH2	9.80 V	9.80 V	9.79 V	9.80 V
IDN1	8.65MA	8.15MA	7.55MA	7.55MA
IDN2	19.7MA	17.9MA	15.8MA	16.0MA
IDP1	-2.78MA	-2.79MA	-2.73MA	-2.86MA
IDP2	-6.07MA	-6.11MA	-5.91MA	-6.27MA
IOZ1	18.7NA	21.9NA	16.0NA	21.7NA
IOZ2	21.3NA	18.8NA	18.9NA	18.4NA
IOZ3	19.2NA	19.9NA	18.5NA	17.8NA
IOZ4	16.9NA	23.3NA	15.5NA	21.3NA
IOZ5	24.0NA	16.5NA	21.2NA	17.2NA
IOZ6	24.0NA	17.2NA	21.1NA	16.9NA
IOZ7	23.7NA	16.7NA	20.5NA	16.9NA
IOZ8	23.1NA	17.0NA	20.6NA	16.9NA

ILDP	-5.00UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-5.00UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	200.N	165.N	70.0N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	18.0N	14.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	96.0N	80.0N	38.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	72.0N	62.0N	34.0N
CS1 SETUP TIME	(TCSS1)	148.N	126.N	62.0N
CS2 SETUP TIME	(TCSS2)	146.N	122.N	58.0N
CS1 HOLD TIME	(TCSH1)	42.0N	36.0N	22.0N
CS2 HOLD TIME	(TCSH2)	44.0N	36.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	188.N	160.N	80.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	186.N	158.N	78.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	40.0N	36.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	126.N	98.0N	24.0N
OUTPUT HOLD FROM CS2	(TDOH2)	124.N	96.0N	24.0N
OUTPUT HOLD FROM MRD	(TDOH3)	132.N	112.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	128.N	106.N	28.0N
READ CYCLE TIME	(TRC)	208.N	176.N	104.N
WRITE CYCLE TIME	(TWC)	224.N	184.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-200.PA	300.PA	3.00 V	-2.99 V
A1	-400.PA	400.PA	3.04 V	-3.04 V
A2	-200.PA	300.PA	3.01 V	-3.04 V
A3	-300.PA	300.PA	3.02 V	-3.04 V
A4	-300.PA	300.PA	3.04 V	-3.09 V
A5	-300.PA	200.PA	3.00 V	-3.02 V
A6	-300.PA	300.PA	3.01 V	-3.06 V
A7	-200.PA	400.PA	3.01 V	-3.04 V
CS1	-300.PA	300.PA	3.01 V	-3.03 V
CS2	-400.PA	200.PA	3.04 V	-3.08 V
MWR	-300.PA	200.PA	2.98 V	-3.00 V
MRD	-300.PA	400.PA	3.01 V	-3.02 V
DI0	-200.PA	400.PA	3.13 V	-3.05 V
DI1	-200.PA	300.PA	3.10 V	-3.03 V
DI2	-400.PA	400.PA	3.10 V	-3.05 V
DI3	-300.PA	300.PA	3.08 V	-3.06 V

	D00	D01	D02	D03
VOL1	75.0MV	80.0MV	85.0MV	85.0MV
VOL2	80.0MV	90.0MV	105.MV	105.MV
VOH1	4.88 V	4.88 V	4.88 V	4.88 V
VOH2	9.83 V	9.84 V	9.82 V	9.84 V
IDN1	9.75MA	9.20MA	8.60MA	8.55MA
IDN2	22.6MA	20.6MA	18.1MA	18.4MA
IDP1	=3.27MA	=3.27MA	=3.26MA	=3.36MA
IDP2	=7.10MA	=7.16MA	=6.98MA	=7.36MA
IOZ1	6.90NA	1.10NA	6.40NA	=100.PA
IOZ2	3.20NA	4.30NA	3.00NA	2.60NA
IOZ3	4.70NA	3.50NA	2.20NA	4.20NA
IOZ4	8.10NA	600.PA	5.80NA	1.00NA
IOZ5	1.50NA	5.90NA	1.10NA	4.90NA
IOZ6	1.60NA	6.10NA	1.20NA	4.50NA
IOZ7	1.70NA	5.70NA	1.20NA	4.60NA
IOZ8	1.90NA	5.80NA	1.50NA	4.10NA

ILDP	=10.0UA
IL1	=5.00UA
IL2	=5.00UA
IL3	=5.00UA
IL4	=5.00UA

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

C-2

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	195.N	160.N	65.0N
DATA SETUP TIME	(TDS)	30.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	6.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	94.0N	74.0N	34.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	76.0N	64.0N	32.0N
CS1 SETUP TIME	(TCSS1)	144.N	120.N	56.0N
CS2 SETUP TIME	(TCSS2)	142.N	118.N	54.0N
CS1 HOLD TIME	(TCSH1)	48.0N	40.0N	22.0N
CS2 HOLD TIME	(TCSH2)	40.0N	40.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	184.N	152.N	80.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	182.N	148.N	78.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	38.0N	34.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	120.N	90.0N	22.0N
OUTPUT HOLD FROM CS2	(TDOH2)	118.N	90.0N	22.0N
OUTPUT HOLD FROM MRD	(TDOH3)	132.N	110.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	126.N	106.N	28.0N
READ CYCLE TIME	(TRC)	200.N	168.N	104.N
WRITE CYCLE TIME	(TWC)	232.N	176.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-100.PA	100.PA	3.06 V	-3.04 V
A1	-100.PA	100.PA	3.10 V	-3.10 V
A2	0.00 A	100.PA	3.06 V	-3.10 V
A3	-100.PA	100.PA	3.08 V	-3.10 V
A4	-100.PA	100.PA	3.10 V	-3.14 V
A5	-100.PA	100.PA	3.05 V	-3.08 V
A6	-100.PA	100.PA	3.07 V	-3.12 V
A7	0.00 A	100.PA	3.07 V	-3.11 V
CS1	-100.PA	100.PA	3.08 V	-3.09 V
CS2	-100.PA	0.00 A	3.11 V	-3.13 V
MWR	-100.PA	100.PA	3.04 V	-3.07 V
MRD	-100.PA	100.PA	3.08 V	-3.08 V
DI0	0.00 A	100.PA	3.18 V	-3.11 V
DI1	0.00 A	100.PA	3.15 V	-3.10 V
DI2	-100.PA	0.00 A	3.15 V	-3.11 V
DI3	0.00 A	100.PA	3.14 V	-3.13 V

	D00	D01	D02	D03
VOL1	70.0MV	70.0MV	75.0MV	75.0MV
VOL2	75.0MV	80.0MV	90.0MV	90.0MV
VOH1	4.90 V	4.90 V	4.90 V	4.90 V
VOH2	9.85 V	9.86 V	9.85 V	9.86 V
IDN1	10.8MA	10.3MA	9.65MA	9.60MA
IDN2	25.4MA	23.3MA	20.7MA	20.9MA
IDP1	-3.80MA	-3.85MA	-3.84MA	-3.95MA
IDP2	-8.26MA	-8.38MA	-8.15MA	-8.58MA
IOZ1	3.80NA	-100.PA	3.90NA	-1.40NA
IOZ2	-100.PA	3.40NA	300.PA	1.80NA
IOZ3	3.60NA	400.PA	1.70NA	1.20NA
IOZ4	5.70NA	-1.90NA	5.20NA	-1.70NA
IOZ5	-1.60NA	5.40NA	-1.70NA	4.70NA
IOZ6	-1.50NA	5.60NA	-1.80NA	4.50NA
IOZ7	-1.50NA	5.40NA	-1.80NA	4.90NA
IOZ8	-1.40NA	5.50NA	-1.80NA	4.70NA

ILDP	-20.0UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-5.00UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	200.N	175.N	85.0N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	10.0N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	106.N	94.0N	48.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	78.0N	70.0N	40.0N
CS1 SETUP TIME	(TCSS1)	154.N	136.N	72.0N
CS2 SETUP TIME	(TCSS2)	150.N	134.N	70.0N
CS1 HOLD TIME	(TCSH1)	54.0N	46.0N	30.0N
CS2 HOLD TIME	(TCSH2)	54.0N	48.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	202.N	180.N	96.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	200.N	178.N	94.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	48.0N	44.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	138.N	108.N	28.0N
OUTPUT HOLD FROM CS2	(TDOH2)	134.N	106.N	30.0N
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	116.N	32.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	110.N	32.0N
READ CYCLE TIME	(TRC)	224.N	200.N	120.N
WRITE CYCLE TIME	(TWC)	208.N	184.N	120.N

	IIL	IIH	VIC1	VICP
A0	-27.1NA	27.5NA	2.94 V	-2.93 V
A1	-29.2NA	28.6NA	2.98 V	-2.99 V
A2	-27.4NA	28.1NA	2.95 V	-2.99 V
A3	-28.6NA	27.8NA	2.96 V	-2.99 V
A4	-27.0NA	27.8NA	2.98 V	-3.03 V
A5	-28.0NA	26.4NA	2.94 V	-2.97 V
A6	-29.1NA	28.4NA	2.96 V	-3.00 V
A7	-27.2NA	29.4NA	2.96 V	-2.99 V
CS1	-28.3NA	26.3NA	2.95 V	-2.97 V
CS2	-28.2NA	26.8NA	2.98 V	-3.02 V
MWR	-26.5NA	26.1NA	2.91 V	-2.94 V
MRD	-28.1NA	27.5NA	2.94 V	-2.96 V
DI0	-27.1NA	28.1NA	3.08 V	-2.99 V
DI1	-26.9NA	27.4NA	3.04 V	-2.98 V
DI2	-27.0NA	27.6NA	3.04 V	-2.99 V
DI3	-27.4NA	27.1NA	3.02 V	-3.01 V

	D00	D01	D02	D03
VOL1	100.MV	105.MV	115.MV	115.MV
VOL2	115.MV	125.MV	145.MV	140.MV
VOH1	4.83 V	4.84 V	4.82 V	4.84 V
VOH2	9.76 V	9.76 V	9.75 V	9.76 V
IDN1	7.30MA	6.90MA	6.40MA	6.40MA
IDN2	16.6MA	15.1MA	13.2MA	13.5MA
IDP1	-2.32MA	-2.33MA	-2.29MA	-2.39MA
IDP2	-5.10MA	-5.12MA	-4.99MA	-5.27MA
IOZ1	203.NA	195.NA	185.NA	185.NA
IOZ2	195.NA	200.NA	182.NA	180.NA
IOZ3	199.NA	196.NA	182.NA	183.NA
IOZ4	193.NA	200.NA	185.NA	178.NA
IOZ5	199.NA	201.NA	188.NA	189.NA
IOZ6	199.NA	196.NA	195.NA	174.NA
IOZ7	207.NA	191.NA	191.NA	185.NA
IOZ8	195.NA	202.NA	187.NA	181.NA

ILDP	-5.00UA
IL1	-20.0UA
IL2	-25.0UA
IL3	-20.0UA
IL4	-20.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	215.N	190.N	95.0N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	114.N	104.N	56.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-16.0N	-6.00N
WRITE PULSE WIDTH	(TWP)	82.0N	72.0N	44.0N
CS1 SETUP TIME	(TCSS1)	164.N	144.N	80.0N
CS2 SETUP TIME	(TCSS2)	158.N	142.N	78.0N
CS1 HOLD TIME	(TCSH1)	54.0N	48.0N	30.0N
CS2 HOLD TIME	(TCSH2)	56.0N	50.0N	30.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	218.N	194.N	106.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	214.N	192.N	104.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	52.0N	48.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	140.N	110.N	32.0N
OUTPUT HOLD FROM CS2	(TDOH2)	138.N	108.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	118.N	36.0N
OUTPUT HOLD FROM MWR	(TPDH)	134.N	112.N	36.0N
READ CYCLE TIME	(TRC)	232.N	208.N	128.N
WRITE CYCLE TIME	(TWC)	224.N	192.N	128.N

	IIL	IIH	VIC1	VIC2
A0	-164.NA	159.NA	2.95 V	-2.94 V
A1	-169.NA	160.NA	2.99 V	-3.00 V
A2	-165.NA	160.NA	2.96 V	-3.00 V
A3	-164.NA	158.NA	2.97 V	-3.00 V
A4	-158.NA	154.NA	3.00 V	-3.04 V
A5	-167.NA	157.NA	2.95 V	-2.98 V
A6	-170.NA	163.NA	2.97 V	-3.02 V
A7	-165.NA	164.NA	2.97 V	-3.00 V
CS1	-166.NA	151.NA	2.95 V	-2.98 V
CS2	-162.NA	156.NA	2.99 V	-3.04 V
MWR	-157.NA	149.NA	2.91 V	-2.95 V
MRD	-161.NA	153.NA	2.95 V	-2.97 V
DI0	-160.NA	161.NA	3.10 V	-3.01 V
DI1	-160.NA	159.NA	3.06 V	-2.99 V
DI2	-158.NA	154.NA	3.05 V	-3.00 V
DI3	-157.NA	156.NA	3.03 V	-3.02 V

	DO0	DO1	DO2	DO3
VOL1	115.MV	120.MV	130.MV	130.MV
VOL2	130.MV	145.MV	165.MV	160.MV
VOH1	4.80 V	4.81 V	4.81 V	4.82 V
VOH2	9.72 V	9.72 V	9.72 V	9.73 V
IDN1	6.50MA	6.15MA	5.70MA	5.70MA
IDN2	14.8MA	13.3MA	11.7MA	11.9MA
IDP1	-2.07MA	-2.11MA	-2.07MA	-2.13MA
IDP2	-4.56MA	-4.61MA	-4.45MA	-4.72MA
IOZ1	849.NA	813.NA	790.NA	732.NA
IOZ2	834.NA	816.NA	787.NA	725.NA
IOZ3	835.NA	806.NA	784.NA	728.NA
IOZ4	828.NA	812.NA	787.NA	722.NA
IOZ5	842.NA	824.NA	805.NA	745.NA
IOZ6	838.NA	814.NA	806.NA	724.NA
IOZ7	847.NA	809.NA	799.NA	733.NA
IOZ8	833.NA	817.NA	793.NA	725.NA

ILDP	40.0UA
IL1	-95.0UA
IL2	-115.UA
IL3	-90.0UA
IL4	-75.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	230.N	190.N	75.0N
DATA SETUP TIME	(TDS)	18.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	112.N	92.0N	40.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	62.0N	52.0N	32.0N
CS1 SETUP TIME	(TCSS1)	136.N	118.N	58.0N
CS2 SETUP TIME	(TCSS2)	132.N	116.N	56.0N
CS1 HOLD TIME	(TCSH1)	38.0N	34.0N	22.0N
CS2 HOLD TIME	(TCSH2)	40.0N	34.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	226.N	188.N	84.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	224.N	186.N	82.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	46.0N	40.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	140.N	110.N	30.0N
OUTPUT HOLD FROM CS2	(TDOH2)	138.N	108.N	30.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	134.N	110.N	28.0N
READ CYCLE TIME	(TRC)	240.N	200.N	104.N
WRITE CYCLE TIME	(TWC)	176.N	160.N	96.0N

	IIL	IIH	VIC1	VTC2
A0	-2.90NA	2.80NA	3.20 V	-3.19 V
A1	-3.60NA	3.10NA	3.25 V	-3.26 V
A2	-3.20NA	2.60NA	3.25 V	-3.27 V
A3	-2.40NA	2.60NA	3.25 V	-3.28 V
A4	-2.70NA	2.70NA	3.27 V	-3.29 V
A5	-2.60NA	2.80NA	3.17 V	-3.22 V
A6	-3.40NA	2.40NA	3.17 V	-3.21 V
A7	-2.60NA	2.50NA	3.17 V	-3.20 V
CS1	-2.50NA	2.70NA	3.20 V	-3.18 V
CS2	-2.60NA	2.70NA	3.22 V	-3.24 V
MWR	-2.70NA	2.60NA	3.17 V	-3.16 V
MRD	-3.00NA	2.70NA	3.21 V	-3.20 V
DI0	-2.50NA	3.10NA	3.28 V	-3.23 V
DI1	-2.50NA	2.50NA	3.26 V	-3.21 V
DI2	-2.50NA	2.50NA	3.25 V	-3.21 V
DI3	-2.30NA	2.30NA	3.25 V	-3.20 V

	D00	D01	D02	D03
VOL1	90.0MV	95.0MV	100.MV	100.MV
VOL2	95.0MV	105.MV	115.MV	115.MV
VOH1	4.87 V	4.87 V	4.86 V	4.87 V
VOH2	9.81 V	9.81 V	9.80 V	9.81 V
IDN1	7.90MA	7.50MA	7.10MA	7.10MA
IDN2	19.8MA	18.0MA	16.1MA	16.4MA
IDP1	-2.94MA	-2.96MA	-2.89MA	-2.99MA
IDP2	-6.47MA	-6.51MA	-6.23MA	-6.61MA
IOZ1	17.7NA	11.6NA	17.9NA	10.6NA
IOZ2	14.0NA	14.2NA	14.4NA	13.5NA
IOZ3	15.8NA	13.2NA	14.6NA	14.0NA
IOZ4	19.0NA	10.5NA	18.3NA	10.8NA
IOZ5	12.1NA	16.9NA	12.4NA	15.3NA
IOZ6	12.4NA	16.6NA	12.4NA	15.5NA
IOZ7	12.1NA	16.6NA	12.3NA	15.1NA
IOZ8	12.0NA	16.1NA	12.6NA	15.0NA
ILDP	-15.0UA			
IL1	-5.00UA			
IL2	-10.0UA			
IL3	-10.0UA			
IL4	-5.00UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	250.N	185.N	65.0N
DATA SETUP TIME	(TDS)	20.0N	16.0N	6.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	12.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	114.N	92.0N	34.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	64.0N	56.0N	30.0N
CS1 SETUP TIME	(TCSS1)	134.N	116.N	54.0N
CS2 SETUP TIME	(TCSS2)	130.N	112.N	54.0N
CS1 HOLD TIME	(TCSH1)	32.0N	30.0N	20.0N
CS2 HOLD TIME	(TCSH2)	34.0N	30.0N	18.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	240.N	190.N	80.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	238.N	188.N	78.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	42.0N	38.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	134.N	102.N	30.0N
OUTPUT HOLD FROM CS2	(TDOH2)	132.N	102.N	30.0N
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	114.N	26.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	108.N	28.0N
READ CYCLE TIME	(TRC)	224.N	192.N	104.N
WRITE CYCLE TIME	(TWC)	176.N	160.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-400.PA	300.PA	3.25 V	-3.24 V
A1	-500.PA	500.PA	3.30 V	-3.30 V
A2	-500.PA	300.PA	3.30 V	-3.32 V
A3	-300.PA	300.PA	3.30 V	-3.32 V
A4	-300.PA	300.PA	3.32 V	-3.34 V
A5	-300.PA	300.PA	3.23 V	-3.27 V
A6	-500.PA	300.PA	3.22 V	-3.26 V
A7	-300.PA	300.PA	3.22 V	-3.25 V
CS1	-300.PA	400.PA	3.25 V	-3.23 V
CS2	-300.PA	300.PA	3.28 V	-3.28 V
MWR	-300.PA	200.PA	3.22 V	-3.21 V
MRD	-300.PA	400.PA	3.26 V	-3.25 V
DI0	-200.PA	400.PA	3.33 V	-3.27 V
DI1	-300.PA	300.PA	3.31 V	-3.25 V
DI2	-300.PA	300.PA	3.30 V	-3.26 V
DI3	-200.PA	300.PA	3.30 V	-3.25 V

	D00	D01	D02	D03
VOL1	80.0MV	85.0MV	90.0MV	90.0MV
VOL2	80.0MV	90.0MV	100.MV	100.MV
VOH1	4.88 V	4.89 V	4.89 V	4.89 V
VOH2	9.84 V	9.84 V	9.84 V	9.84 V
IDN1	8.80MA	8.35MA	8.00MA	7.95MA
IDN2	22.6MA	20.6MA	18.6MA	18.8MA
IDP1	-3.44MA	-3.50MA	-3.41MA	-3.51MA
IDP2	-7.57MA	-7.66MA	-7.38MA	-7.75MA
IOZ1	7.60NA	1.80NA	5.60NA	2.40NA
IOZ2	7.60NA	-400.PA	7.70NA	200.PA
IOZ3	800.PA	7.20NA	600.PA	7.50NA
IOZ4	3.10NA	4.60NA	2.40NA	5.60NA
IOZ5	5.60NA	1.70NA	6.40NA	600.PA
IOZ6	5.80NA	1.30NA	6.40NA	700.PA
IOZ7	5.70NA	1.50NA	6.40NA	500.PA
IOZ8	5.90NA	1.00NA	6.50NA	600.PA

ILDP	-5.00UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-5.00UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	245.N	180.N	65.0N
DATA SETUP TIME	(TDS)	24.0N	18.0N	6.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	12.0N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	114.N	88.0N	32.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	66.0N	56.0N	28.0N
CS1 SETUP TIME	(TCSS1)	134.N	110.N	52.0N
CS2 SETUP TIME	(TCSS2)	130.N	110.N	50.0N
CS1 HOLD TIME	(TCSH1)	38.0N	32.0N	20.0N
CS2 HOLD TIME	(TCSH2)	38.0N	32.0N	18.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	240.N	182.N	76.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	238.N	180.N	74.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	40.0N	34.0N	20.0N
OUTPUT HOLD FROM CS1	(TDOH1)	130.N	98.0N	28.0N
OUTPUT HOLD FROM CS2	(TDOH2)	128.N	96.0N	30.0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	112.N	26.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	108.N	26.0N
READ CYCLE TIME	(TRC)	208.N	176.N	96.0N
WRITE CYCLE TIME	(TWC)	184.N	160.N	88.0N

	IIL	IIH	VIC1	VIC2
A0	-100.PA	100.PA	3.30 V	-3.29 V
A1	-100.PA	100.PA	3.36 V	-3.36 V
A2	-100.PA	100.PA	3.36 V	-3.37 V
A3	0.00 A	100.PA	3.36 V	-3.37 V
A4	-100.PA	100.PA	3.37 V	-3.38 V
A5	-100.PA	100.PA	3.28 V	-3.32 V
A6	-100.PA	100.PA	3.27 V	-3.31 V
A7	-100.PA	100.PA	3.28 V	-3.30 V
CS1	-100.PA	100.PA	3.30 V	-3.29 V
CS2	-100.PA	100.PA	3.33 V	-3.34 V
MWR	-100.PA	0.00 A	3.27 V	-3.27 V
MRD	-100.PA	100.PA	3.31 V	-3.30 V
DI0	0.00 A	100.PA	3.38 V	-3.32 V
DI1	-100.PA	100.PA	3.36 V	-3.30 V
DI2	-100.PA	100.PA	3.36 V	-3.31 V
DI3	0.00 A	100.PA	3.36 V	-3.29 V

	D00	D01	D02	D03
VOL1	80.0MV	85.0MV	85.0MV	85.0MV
VOL2	75.0MV	80.0MV	90.0MV	90.0MV
VOH1	4.90 V	4.90 V	4.90 V	4.90 V
VOH2	9.86 V	9.86 V	9.85 V	9.86 V
IDN1	9.55MA	9.15MA	8.75MA	8.70MA
IDN2	24.8MA	23.0MA	20.8MA	21.1MA
IDP1	-4.00MA	-4.00MA	-3.96MA	-4.09MA
IDP2	-8.73MA	-8.82MA	-8.53MA	-8.97MA
IOZ1	4.60NA	-700.PA	4.80NA	-1.60NA
IOZ2	600.PA	2.70NA	1.30NA	1.10NA
IOZ3	3.10NA	1.00NA	1.50NA	1.80NA
IOZ4	5.90NA	-1.70NA	5.40NA	-1.30NA
IOZ5	-1.30NA	5.10NA	-1.10NA	4.40NA
IOZ6	-1.20NA	5.50NA	-1.20NA	4.40NA
IOZ7	-1.30NA	5.30NA	-1.30NA	4.80NA
IOZ8	-1.30NA	5.50NA	-1.30NA	4.70NA

ILDP	-15.0UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-5.00UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	215.N	185.N	80.0N
DATA SETUP TIME	(TDS)	190.N	16.0N	8.00N
DATA HOLD TIME	(TDH)	18.0N	16.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	6.00N	6.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	108.N	92.0N	44.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	66.0N	60.0N	36.0N
CS1 SETUP TIME	(TCSS1)	140.N	122.N	64.0N
CS2 SETUP TIME	(TCSS2)	138.N	120.N	62.0N
CS1 HOLD TIME	(TCSH1)	42.0N	38.0N	24.0N
CS2 HOLD TIME	(TCSH2)	46.0N	40.0N	24.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	218.N	188.N	90.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	216.N	186.N	90.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	46.0N	42.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	142.N	112.N	32.0N
OUTPUT HOLD FROM CS2	(TDOH2)	138.N	108.N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	134.N	110.N	30.0N
READ CYCLE TIME	(TRC)	240.N	208.N	112.N
WRITE CYCLE TIME	(TWC)	192.N	176.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-40.3NA	41.3NA	3.19 V	-3.18 V
A1	-42.2NA	40.5NA	3.24 V	-3.25 V
A2	-41.6NA	40.2NA	3.24 V	-3.27 V
A3	-38.7NA	39.5NA	3.25 V	-3.27 V
A4	-39.4NA	39.0NA	3.26 V	-3.28 V
A5	-39.9NA	40.6NA	3.16 V	-3.21 V
A6	-42.3NA	39.2NA	3.16 V	-3.20 V
A7	-40.7NA	40.2NA	3.16 V	-3.18 V
CS1	-38.7NA	38.3NA	3.18 V	-3.17 V
CS2	-38.8NA	40.4NA	3.21 V	-3.23 V
MWR	-38.8NA	38.5NA	3.15 V	-3.15 V
MRD	-39.6NA	38.5NA	3.19 V	-3.19 V
DI0	-38.7NA	41.6NA	3.27 V	-3.22 V
DI1	-39.0NA	39.3NA	3.24 V	-3.19 V
DI2	-37.7NA	39.3NA	3.24 V	-3.20 V
DI3	-37.1NA	38.1NA	3.24 V	-3.19 V

	D00	D01	D02	D03
VOL1	105.MV	110.MV	120.MV	120.MV
VOL2	110.MV	125.MV	140.MV	135.MV
VOH1	4.84 V	4.84 V	4.84 V	4.84 V
VOH2	9.77 V	9.77 V	9.76 V	9.78 V
IDN1	6.85MA	6.50MA	6.15MA	6.15MA
IDN2	16.9MA	15.3MA	13.7MA	13.9MA
IDP1	-2.48MA	-2.50MA	-2.44MA	-2.54MA
IDP2	-5.45MA	-5.49MA	-5.31MA	-5.58MA
IOZ1	-34.1NA	-46.8NA	-45.7NA	-48.2NA
IOZ2	-37.1NA	-54.0NA	-44.1NA	-53.6NA
IOZ3	-49.6NA	-50.6NA	-55.7NA	-50.1NA
IOZ4	-45.4NA	-52.6NA	-53.9NA	-51.0NA
IOZ5	-43.9NA	-56.5NA	-50.8NA	-58.7NA
IOZ6	-45.6NA	-57.4NA	-52.0NA	-56.7NA
IOZ7	-47.4NA	-58.5NA	-52.8NA	-56.5NA
IOZ8	-46.0NA	-55.6NA	-51.8NA	-57.0NA

ILDP	-10.0UA
IL1	-40.0UA
IL2	-55.0UA
IL3	-35.0UA
IL4	-30.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	225.N	195.N	90.0N
DATA SETUP TIME	(TDS)	28.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	20.0N	18.0N	16.0N
ADDRESS SETUP TIME	(TAS1)	4.00N	4.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	122.N	104.N	52.0N
ADDRESS HOLD TIME	(TAH)	-12.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	68.0N	62.0N	38.0N
CS1 SETUP TIME	(TCSS1)	148.N	130.N	70.0N
CS2 SETUP TIME	(TCSS2)	144.N	126.N	68.0N
CS1 HOLD TIME	(TCSH1)	42.0N	38.0N	24.0N
CS2 HOLD TIME	(TCSH2)	46.0N	40.0N	24.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	232.N	202.N	98.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	230.N	200.N	98.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	44.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	142.N	114.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	140.N	110.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	32.0N
OUTPUT HOLD FROM MWR	(TPDH)	136.N	112.N	32.0N
READ CYCLE TIME	(TRC)	248.N	216.N	120.N
WRITE CYCLE TIME	(TWC)	208.N	184.N	120.N

	IIL	IIH	VIC1	VTC2
A0	-234.NA	233.NA	3.20 V	-3.19 V
A1	-236.NA	231.NA	3.26 V	-3.26 V
A2	-232.NA	229.NA	3.25 V	-3.28 V
A3	-227.NA	225.NA	3.25 V	-3.29 V
A4	-226.NA	221.NA	3.27 V	-3.29 V
A5	-232.NA	231.NA	3.17 V	-3.22 V
A6	-237.NA	227.NA	3.17 V	-3.21 V
A7	-235.NA	232.NA	3.17 V	-3.19 V
CS1	-229.NA	219.NA	3.19 V	-3.17 V
CS2	-224.NA	228.NA	3.22 V	-3.23 V
MWR	-222.NA	217.NA	3.15 V	-3.16 V
MRD	-224.NA	220.NA	3.20 V	-3.19 V
DI0	-227.NA	233.NA	3.28 V	-3.23 V
DI1	-226.NA	226.NA	3.25 V	-3.20 V
DI2	-218.NA	225.NA	3.24 V	-3.20 V
DI3	-218.NA	220.NA	3.24 V	-3.19 V

	D00	D01	D02	D03
VOL1	115.MV	125.MV	135.MV	135.MV
VOL2	125.MV	140.MV	160.MV	155.MV
VOH1	4.82 V	4.82 V	4.82 V	4.82 V
VOH2	9.74 V	9.74 V	9.73 V	9.74 V
IDN1	6.20MA	5.85MA	5.55MA	5.55MA
IDN2	15.1MA	13.6MA	12.2MA	12.4MA
IDP1	-2.24MA	-2.26MA	-2.21MA	-2.29MA
IDP2	-4.88MA	-4.95MA	-4.75MA	-4.99MA
IOZ1	-751.NA	-761.NA	-752.NA	-738.NA
IOZ2	-758.NA	-775.NA	-751.NA	-744.NA
IOZ3	-771.NA	-779.NA	-762.NA	-750.NA
IOZ4	-764.NA	-784.NA	-760.NA	-749.NA
IOZ5	-762.NA	-775.NA	-762.NA	-760.NA
IOZ6	-770.NA	-797.NA	-775.NA	-748.NA
IOZ7	-779.NA	-782.NA	-778.NA	-746.NA
IOZ8	-774.NA	-788.NA	-768.NA	-757.NA

ILOP	80.0UA
IL1	-200.UA
IL2	-260.UA
IL3	-155.UA
IL4	-130.UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	215.N	185.N	75.0N
DATA SETUP TIME	(TDS)	22.0N	18.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	10.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	14.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	106.N	90.0N	42.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	64.0N	56.0N	34.0N
CS1 SETUP TIME	(TCSS1)	150.N	130.N	62.0N
CS2 SETUP TIME	(TCSS2)	180.N	154.N	74.0N
CS1 HOLD TIME	(TCSH1)	38.0N	32.0N	22.0N
CS2 HOLD TIME	(TCSH2)	0.00	0.00	0.00
OUTPUT ACTIVE FROM CS1	(TDOA1)	208.N	176.N	84.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	238.N	200.N	94.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	46.0N	40.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	136.N	108.N	30.0N
OUTPUT HOLD FROM CS2	(TDOH2)	194.N	164.N	58.0N
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	114.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	110.N	30.0N
READ CYCLE TIME	(TRC)	224.N	200.N	112.N
WRITE CYCLE TIME	(TWC)	248.N	176.N	104.N

	IIL	IIH	VIC1	VIC2
A0	-2.00NA	1.50NA	2.91 V	-2.89 V
A1	-1.90NA	2.00NA	2.91 V	-2.92 V
A2	-2.30NA	2.20NA	2.94 V	-2.95 V
A3	-1.30NA	1.40NA	2.95 V	-2.96 V
A4	-1.50NA	2.00NA	2.97 V	-2.96 V
A5	-1.90NA	1.60NA	2.86 V	-2.91 V
A6	-1.40NA	1.60NA	2.86 V	-2.91 V
A7	-2.30NA	1.70NA	2.86 V	-2.89 V
CS1	-1.40NA	1.80NA	2.91 V	-2.91 V
CS2	-2.50NA	1.40NA	4.96 V	-4.95 V
MWR	-2.90NA	1.50NA	2.89 V	-2.89 V
MRD	-1.50NA	1.60NA	2.89 V	-2.88 V
DI0	-2.00NA	1.60NA	2.97 V	-2.91 V
DI1	-2.30NA	1.90NA	2.94 V	-2.91 V
DI2	-1.70NA	1.60NA	2.96 V	-2.92 V
DI3	-2.10NA	1.60NA	2.94 V	-2.89 V

	D00	D01	D02	D03
VOL1	90.0MV	95.0MV	105.MV	105.MV
VOL2	95.0MV	110.MV	130.MV	120.MV
VOH1	4.86 V	4.86 V	4.86 V	4.86 V
VOH2	9.80 V	9.80 V	9.79 V	9.80 V
IDN1	7.95MA	7.55MA	6.85MA	7.10MA
IDN2	19.3MA	17.4MA	14.9MA	15.7MA
IDP1	-2.83MA	-2.83MA	-2.79MA	-2.86MA
IDP2	-6.22MA	-6.22MA	-6.02MA	-6.34MA
IOZ1	25.6NA	21.2NA	24.7NA	19.2NA
IOZ2	22.1NA	22.9NA	22.3NA	19.8NA
IOZ3	20.0NA	25.8NA	18.0NA	24.9NA
IOZ4	23.3NA	22.1NA	21.1NA	21.5NA
IOZ5	20.0NA	24.8NA	20.0NA	23.1NA
IOZ6	19.9NA	25.5NA	20.0NA	22.5NA
IOZ7	20.1NA	25.0NA	20.0NA	22.3NA
IOZ8	19.7NA	25.3NA	20.2NA	22.4NA
ILDP	1.00UA			
IL1	-5.00UA			
IL2	-10.0UA			
IL3	-5.00UA			
IL4	-5.00UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	220.N	180.N	70.0N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	104.N	86.0N	38.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-10.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	70.0N	50.0N	32.0N
$\overline{CS_1}$ SETUP TIME	(TCSS1)	148.N	124.N	60.0N
$\overline{CS2}$ SETUP TIME	(TCSS2)	180.N	152.N	70.0N
$\overline{CS_1}$ HOLD TIME	(TCSH1)	38.0N	32.0N	22.0N
$\overline{CS2}$ HOLD TIME	(TCSH2)	0.00	0.00	0.00
OUTPUT ACTIVE FROM $\overline{CS_1}$	(TDOA1)	210.N	170.N	80.0N
OUTPUT ACTIVE FROM $\overline{CS2}$	(TDOA2)	232.N	192.N	86.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	42.0N	36.0N	22.0N
OUTPUT HOLD FROM $\overline{CS_1}$	(TDOH1)	130.N	100.N	28.0N
OUTPUT HOLD FROM $\overline{CS2}$	(TDOH2)	178.N	146.N	44.0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	112.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	128.N	108.N	28.0N
READ CYCLE TIME	(TRC)	216.N	184.N	104.N
WRITE CYCLE TIME	(TWC)	248.N	184.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-400.PA	300.PA	3.00 V	-2.98 V
A1	-300.PA	500.PA	3.00 V	-3.01 V
A2	-400.PA	500.PA	3.03 V	-3.04 V
A3	-300.PA	300.PA	3.04 V	-3.04 V
A4	-300.PA	400.PA	3.06 V	-3.04 V
A5	-400.PA	300.PA	2.95 V	-3.00 V
A6	-300.PA	300.PA	2.95 V	-3.00 V
A7	-400.PA	300.PA	2.95 V	-2.97 V
$\overline{CS1}$	-200.PA	400.PA	3.00 V	-3.00 V
$\overline{CS2}$	-700.PA	300.PA	4.96 V	-4.95 V
MWR	+600.PA	300.PA	2.98 V	-2.99 V
MRD	-400.PA	400.PA	2.99 V	-2.97 V
DI0	-400.PA	300.PA	3.06 V	-3.00 V
DI1	-500.PA	400.PA	3.04 V	-3.00 V
DI2	-300.PA	300.PA	3.05 V	-3.01 V
DI3	-400.PA	400.PA	3.03 V	-2.98 V

	D00	D01	D02	D03
VOL1	80.0MV	85.0MV	95.0MV	95.0MV
VOL2	85.0MV	95.0MV	110.MV	105.MV
VOH1	4.88 V	4.88 V	4.88 V	4.89 V
VOH2	9.84 V	9.84 V	9.83 V	9.84 V
IDN1	8.85MA	8.40MA	7.70MA	7.95MA
IDN2	22.0MA	19.8MA	17.1MA	17.9MA
IDP1	-3.30MA	-3.35MA	-3.28MA	-3.35MA
IDP2	-7.27MA	-7.37MA	-7.06MA	-7.41MA
IOZ1	4.20NA	6.00NA	2.30NA	6.20NA
IOZ2	7.40NA	2.60NA	5.60NA	2.80NA
IOZ3	1.90NA	6.60NA	2.20NA	5.70NA
IOZ4	800.PA	8.10NA	300.PA	8.30NA
IOZ5	7.60NA	1.50NA	7.80NA	1.40NA
IOZ6	7.90NA	1.40NA	7.50NA	1.20NA
IOZ7	7.70NA	1.40NA	7.70NA	1.30NA
IOZ8	7.90NA	1.40NA	7.40NA	1.40NA
ILDP	-20.0UA			
IL1	-5.00UA			
IL2	-5.00UA			
IL3	-5.00UA			
IL4	-5.00UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	220.N	175.N	65.0N
DATA SETUP TIME	(TDS)	30.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	12.0N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	104.N	84.0N	34.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	76.0N	62.0N	30.0N
CS1 SETUP TIME	(TCSS1)	142.N	120.N	54.0N
CS2 SETUP TIME	(TCSS2)	178.N	146.N	66.0N
CS1 HOLD TIME	(TCSH1)	46.0N	38.0N	22.0N
CS2 HOLD TIME	(TCSH2)	0.00	0.00	0.00
OUTPUT ACTIVE FROM CS1	(TDOA1)	210.N	168.N	80.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	238.N	192.N	86.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	38.0N	34.0N	20.0N
OUTPUT HOLD FROM CS1	(TDOH1)	126.N	96.0N	26.0N
OUTPUT HOLD FROM CS2	(TDOH2)	178.N	148.N	44.0N
OUTPUT HOLD FROM MRD	(TDOH3)	132.N	110.N	26.0N
OUTPUT HOLD FROM MWR	(TPDH)	130.N	106.N	26.0N
READ CYCLE TIME	(TRC)	216.N	176.N	104.N
WRITE CYCLE TIME	(TWC)	208.N	164.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-100.PA	100.PA	3.10 V	-3.08 V
A1	-100.PA	200.PA	3.11 V	-3.11 V
A2	-100.PA	100.PA	3.13 V	-3.13 V
A3	-100.PA	100.PA	3.13 V	-3.14 V
A4	-100.PA	100.PA	3.16 V	-3.14 V
A5	-100.PA	100.PA	3.04 V	-3.10 V
A6	-100.PA	100.PA	3.04 V	-3.11 V
A7	-300.PA	100.PA	3.05 V	-3.08 V
CS1	-100.PA	100.PA	3.11 V	-3.10 V
CS2	-200.PA	100.PA	4.97 V	-4.95 V
MWR	-100.PA	100.PA	3.08 V	-3.09 V
MRD	-100.PA	100.PA	3.10 V	-3.07 V
DI0	-100.PA	100.PA	3.16 V	-3.10 V
DI1	-100.PA	100.PA	3.13 V	-3.10 V
DI2	-100.PA	100.PA	3.15 V	-3.11 V
DI3	-100.PA	100.PA	3.13 V	-3.08 V

	DO0	DO1	DO2	DO3
VOL1	75.0MV	80.0MV	85.0MV	85.0MV
VOL2	75.0MV	85.0MV	100.MV	95.0MV
VOH1	4.90 V	4.90 V	4.89 V	4.90 V
VOH2	9.85 V	9.85 V	9.85 V	9.86 V
IDN1	9.60MA	9.15MA	8.40MA	8.70MA
IDN2	24.3MA	22.1MA	19.2MA	20.1MA
IDP1	-3.80MA	-3.86MA	-3.78MA	-3.90MA
IDP2	-8.36MA	-8.48MA	-8.15MA	-8.58MA
IOZ1	1.80NA	3.20NA	400.PA	3.80NA
IOZ2	4.90NA	-200.PA	3.80NA	300.PA
IOZ3	-400.PA	4.40NA	-200.PA	2.90NA
IOZ4	-1.20NA	5.50NA	-2.00NA	5.50NA
IOZ5	5.50NA	-1.50NA	5.20NA	-1.50NA
IOZ6	5.30NA	-1.30NA	5.40NA	-1.70NA
IOZ7	5.50NA	-1.50NA	5.20NA	-1.60NA
IOZ8	5.20NA	-1.30NA	5.30NA	-1.70NA
ILDP	-2.20UA			
IL1	-5.00UA			
IL2	-5.00UA			
IL3	-5.00UA			
IL4	-5.00UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	215.N	185.N	85.0N
DATA SETUP TIME	(TDS)	24.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	100.N	96.0N	48.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	76.0N	66.0N	38.0N
CS1 SETUP TIME	(TCSS1)	154.N	134.N	70.0N
CS2 SETUP TIME	(TCSS2)	150.N	132.N	68.0N
CS1 HOLD TIME	(TCSH1)	48.0N	42.0N	28.0N
CS2 HOLD TIME	(TCSH2)	50.0N	46.0N	26.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	212.N	186.N	94.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	210.N	184.N	92.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	48.0N	42.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	140.N	110.N	32.0N
OUTPUT HOLD FROM CS2	(TDOH2)	138.N	108.N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	116.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	110.N	30.0N
READ CYCLE TIME	(TRC)	232.N	208.N	120.N
WRITE CYCLE TIME	(TWC)	216.N	192.N	120.N

	IIL	IIH	VIC1	VIC2
A0	-21.2NA	19.3NA	2.86 V	-2.84 V
A1	-21.2NA	21.0NA	2.86 V	-2.87 V
A2	-22.4NA	21.8NA	2.89 V	-2.90 V
A3	-19.3NA	19.1NA	2.90 V	-2.91 V
A4	-19.6NA	20.5NA	2.91 V	-2.91 V
A5	-21.3NA	20.0NA	2.79 V	-2.86 V
A6	-19.5NA	19.9NA	2.80 V	-2.86 V
A7	-22.1NA	20.3NA	2.80 V	-2.83 V
CS1	-20.1NA	20.2NA	2.86 V	-2.85 V
CS2	-21.4NA	19.6NA	2.89 V	-2.89 V
MWR	-20.6NA	19.2NA	2.83 V	-2.84 V
MRD	-19.1NA	19.1NA	2.84 V	-2.82 V
DI0	-19.9NA	19.7NA	2.91 V	-2.86 V
DI1	-20.9NA	20.5NA	2.89 V	-2.86 V
DI2	-19.3NA	19.6NA	2.91 V	-2.86 V
DI3	-20.0NA	19.7NA	2.89 V	-2.84 V

	DO0	DO1	DO2	DO3
VOL1	105.MV	115.MV	125.MV	120.MV
VOL2	115.MV	130.MV	155.MV	145.MV
VOH1	4.84 V	4.84 V	4.83 V	4.84 V
VOH2	9.76 V	9.76 V	9.75 V	9.77 V
IDN1	6.90MA	6.50MA	5.90MA	6.15MA
IDN2	16.4MA	14.8MA	12.5MA	13.3MA
IDP1	-2.39MA	-2.38MA	-2.34MA	-2.41MA
IDP2	-5.27MA	-5.25MA	-5.08MA	-5.37MA
IOZ1	196.NA	193.NA	174.NA	189.NA
IOZ2	187.NA	196.NA	169.NA	187.NA
IOZ3	189.NA	192.NA	171.NA	191.NA
IOZ4	183.NA	199.NA	169.NA	186.NA
IOZ5	189.NA	199.NA	172.NA	193.NA
IOZ6	184.NA	197.NA	177.NA	178.NA
IOZ7	194.NA	188.NA	179.NA	185.NA
IOZ8	186.NA	200.NA	170.NA	188.NA

ILDP	-5.00UA
IL1	-20.0UA
IL2	-25.0UA
IL3	-25.0UA
IL4	-20.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	220.N	195.N	95.0N
DATA SETUP TIME	(TDS)	22.0N	18.0N	8.00N
DATA HOLD TIME	(TDH)	14.0N	14.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	6.00N	6.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	114.N	104.N	56.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-12.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	78.0N	70.0N	42.0N
CS1 SETUP TIME	(TCSS1)	160.N	142.N	76.0N
CS2 SETUP TIME	(TCSS2)	156.N	138.N	74.0N
CS1 HOLD TIME	(TCSH1)	50.0N	46.0N	28.0N
CS2 HOLD TIME	(TCSH2)	54.0N	46.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	224.N	198.N	104.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	220.N	196.N	102.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	46.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	142.N	112.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	138.N	110.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	116.N	32.0N
OUTPUT HOLD FROM MWR	(TPDH)	134.N	112.N	32.0N
READ CYCLE TIME	(TRC)	248.N	216.N	128.N
WRITE CYCLE TIME	(TWC)	224.N	200.N	128.N

	IIL	IIH	VIC1	VIC2
A0	-119.NA	112.NA	2.84 V	-2.81 V
A1	-118.NA	113.NA	2.83 V	-2.84 V
A2	-121.NA	115.NA	2.88 V	-2.88 V
A3	-114.NA	111.NA	2.88 V	-2.88 V
A4	-113.NA	111.NA	2.89 V	-2.88 V
A5	-118.NA	111.NA	2.77 V	-2.84 V
A6	-115.NA	112.NA	2.77 V	-2.83 V
A7	-121.NA	112.NA	2.77 V	-2.79 V
CS1	-117.NA	108.NA	2.83 V	-2.82 V
CS2	-114.NA	109.NA	2.87 V	-2.87 V
MWR	-115.NA	108.NA	2.79 V	-2.80 V
MRD	-109.NA	106.NA	2.80 V	-2.79 V
DI0	-113.NA	109.NA	2.89 V	-2.83 V
DI1	-113.NA	113.NA	2.86 V	-2.84 V
DI2	-110.NA	109.NA	2.88 V	-2.84 V
DI3	-110.NA	108.NA	2.86 V	-2.81 V

	D00	D01	D02	D03
VOL1	120.MV	125.MV	140.MV	135.MV
VOL2	130.MV	145.MV	170.MV	165.MV
VOH1	4.82 V	4.82 V	4.82 V	4.82 V
VOH2	9.73 V	9.73 V	9.72 V	9.73 V
IDN1	6.25MA	5.85MA	5.35MA	5.55MA
IDN2	14.7MA	13.2MA	11.3MA	11.8MA
IDP1	-2.15MA	-2.15MA	-2.12MA	-2.19MA
IDP2	-4.71MA	-4.75MA	-4.54MA	-4.81MA
IOZ1	730.NA	730.NA	667.NA	675.NA
IOZ2	721.NA	717.NA	668.NA	678.NA
IOZ3	708.NA	717.NA	661.NA	673.NA
IOZ4	716.NA	711.NA	662.NA	676.NA
IOZ5	722.NA	724.NA	679.NA	693.NA
IOZ6	723.NA	730.NA	658.NA	692.NA
IOZ7	710.NA	725.NA	662.NA	678.NA
IOZ8	717.NA	716.NA	664.NA	684.NA

ILOP	-5.00UA
IL1	-85.0UA
IL2	-110.UA
IL3	-85.0UA
IL4	-75.0UA

RCA COP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN: 13

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	245.N	205.N	80.0N
DATA SETUP TIME	(TDS)	20.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	12.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	114.N	94.0N	44.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	64.0N	56.0N	34.0N
CS1 SETUP TIME	(TCSS1)	148.N	128.N	62.0N
CS2 SETUP TIME	(TCSS2)	144.N	126.N	62.0N
CS1 HOLD TIME	(TCSH1)	38.0N	34.0N	22.0N
CS2 HOLD TIME	(TCSH2)	42.0N	38.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	232.N	196.N	88.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	230.N	192.N	86.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	44.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	148.N	118.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	146.N	114.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	136.N	112.N	30.0N
READ CYCLE TIME	(TRC)	256.N	216.N	112.N
WRITE CYCLE TIME	(TWC)	232.N	216.N	112.N

	IIL	IIH	VIC1	VTC2
A0	-2.80NA	3.20NA	2.90 V	-2.90 V
A1	-3.10NA	2.70NA	2.94 V	-2.93 V
A2	-3.00NA	2.40NA	3.02 V	-3.01 V
A3	-2.70NA	3.00NA	2.99 V	-2.99 V
A4	-6.00NA	2.40NA	3.04 V	-3.06 V
A5	-3.10NA	2.80NA	2.90 V	-2.93 V
A6	-2.40NA	2.70NA	2.93 V	-2.97 V
A7	-2.40NA	2.40NA	2.93 V	-2.96 V
CS1	-2.50NA	2.70NA	3.00 V	-2.99 V
CS2	-2.70NA	2.50NA	3.04 V	-3.03 V
MWR	-2.10NA	2.70NA	2.99 V	-2.98 V
MRD	-2.60NA	2.50NA	2.99 V	-3.00 V
DI0	-2.60NA	3.00NA	3.05 V	-2.99 V
DI1	-3.30NA	3.00NA	3.03 V	-2.99 V
DI2	-3.40NA	4.40NA	3.11 V	-3.06 V
DI3	-3.20NA	2.50NA	3.08 V	-3.04 V

	DO0	DO1	DO2	DO3
VOL1	110.MV	110.MV	125.MV	120.MV
VOL2	110.MV	120.MV	140.MV	135.MV
VOH1	4.85 V	4.85 V	4.84 V	4.84 V
VOH2	9.79 V	9.79 V	9.77 V	9.78 V
IDN1	6.70MA	6.55MA	5.95MA	6.00MA
IDN2	17.0MA	16.0MA	13.8MA	14.2MA
IDP1	-2.56MA	-2.57MA	-2.49MA	-2.53MA
IDP2	-5.78MA	-5.81MA	-5.61MA	-5.77MA
IOZ1	14.5NA	9.30NA	13.5NA	11.3NA
IOZ2	15.2NA	7.40NA	15.6NA	8.40NA
IOZ3	8.00NA	14.5NA	8.40NA	15.3NA
IOZ4	10.4NA	12.3NA	9.20NA	13.9NA
IOZ5	13.5NA	8.10NA	14.1NA	8.60NA
IOZ6	13.1NA	8.30NA	14.5NA	8.40NA
IOZ7	13.2NA	8.00NA	14.5NA	8.50NA
IOZ8	13.1NA	8.30NA	14.3NA	8.50NA

ILDP	-5.00UA
IL1	-10.0UA
IL2	-10.0UA
IL3	-175.UA
IL4	-175.UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	250.N	200.N	75.0N
DATA SETUP TIME	(TDS)	24.0N	18.0N	6.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	114.N	92.0N	40.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	70.0N	62.0N	32.0N
CS1 SETUP TIME	(TCSS1)	146.N	124.N	60.0N
CS2 SETUP TIME	(TCSS2)	142.N	120.N	58.0N
CS1 HOLD TIME	(TCSH1)	36.0N	30.0N	22.0N
CS2 HOLD TIME	(TCSH2)	38.0N	32.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	238.N	192.N	82.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	234.N	190.N	80.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	48.0N	42.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	142.N	110.N	32.0N
OUTPUT HOLD FROM CS2	(TDOH2)	138.N	108.N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	134.N	110.N	30.0N
READ CYCLE TIME	(TRC)	232.N	200.N	96.0N
WRITE CYCLE TIME	(TWC)	232.N	184.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-400.PA	800.PA	3.00 V	-3.00 V
A1	-600.PA	400.PA	3.04 V	-3.03 V
A2	-500.PA	400.PA	3.13 V	-3.10 V
A3	-500.PA	700.PA	3.09 V	-3.09 V
A4	-1.20NA	400.PA	3.13 V	-3.15 V
A5	-500.PA	500.PA	3.00 V	-3.04 V
A6	-400.PA	500.PA	3.03 V	-3.07 V
A7	-300.PA	400.PA	3.03 V	-3.06 V
CS1	-400.PA	500.PA	3.11 V	-3.09 V
CS2	-500.PA	400.PA	3.14 V	-3.12 V
MWR	-300.PA	400.PA	3.09 V	-3.08 V
MRD	-400.PA	500.PA	3.10 V	-3.10 V
DI0	-400.PA	400.PA	3.15 V	-3.09 V
DI1	-800.PA	600.PA	3.14 V	-3.09 V
DI2	-700.PA	900.PA	3.20 V	-3.15 V
DI3	-800.PA	500.PA	3.17 V	-3.13 V

	D00	D01	D02	D03
VOL1	100.MV	100.MV	110.MV	110.MV
VOL2	95.0MV	105.MV	120.MV	115.MV
VOH1	4.88 V	4.80 V	4.87 V	4.87 V
VOH2	9.82 V	9.82 V	9.81 V	9.81 V
IDN1	7.40MA	7.25MA	6.60MA	6.70MA
IDN2	19.3MA	18.2MA	15.8MA	16.2MA
IDP1	=3.01MA	=3.03MA	=2.96MA	=2.98MA
IDP2	=6.78MA	=6.86MA	=6.59MA	=6.78MA
IOZ1	2.00NA	5.40NA	2.50NA	4.50NA
IOZ2	500.PA	7.00NA	300.PA	7.60NA
IOZ3	7.50NA	=300.PA	7.60NA	600.PA
IOZ4	4.80NA	1.40NA	5.40NA	1.50NA
IOZ5	1.80NA	5.10NA	1.30NA	6.90NA
IOZ6	2.10NA	5.30NA	900.PA	6.40NA
IOZ7	1.70NA	5.20NA	1.10NA	6.60NA
IOZ8	1.90NA	5.30NA	900.PA	6.30NA

ILDP	=5.00UA
IL1	=5.00UA
IL2	=5.00UA
IL3	=200.UA
IL4	=200.UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	250.N	190.N	70.0N
DATA SETUP TIME	(TDS)	30.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	112.N	90.0N	36.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	68.0N	62.0N	30.0N
CS1 SETUP TIME	(TCSS1)	150.N	122.N	56.0N
CS2 SETUP TIME	(TCSS2)	148.N	120.N	54.0N
CS1 HOLD TIME	(TCSH1)	42.0N	34.0N	20.0N
CS2 HOLD TIME	(TCSH2)	46.0N	36.0N	18.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	246.N	192.N	80.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	242.N	190.N	78.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	44.0N	38.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	138.N	106.N	32.0N
OUTPUT HOLD FROM CS2	(TDOH2)	134.N	104.N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	114.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	110.N	28.0N
READ CYCLE TIME	(TRC)	224.N	200.N	104.N
WRITE CYCLE TIME	(TWC)	224.N	176.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-100.PA	300.PA	3.12 V	-3.11 V
A1	-100.PA	100.PA	3.15 V	-3.14 V
A2	-100.PA	100.PA	3.22 V	-3.20 V
A3	-100.PA	200.PA	3.19 V	-3.18 V
A4	-400.PA	100.PA	3.23 V	-3.24 V
A5	-100.PA	100.PA	3.12 V	-3.15 V
A6	-100.PA	100.PA	3.14 V	-3.18 V
A7	-100.PA	100.PA	3.13 V	-3.17 V
CS1	-100.PA	100.PA	3.21 V	-3.19 V
CS2	-100.PA	100.PA	3.24 V	-3.22 V
MWR	-100.PA	100.PA	3.18 V	-3.17 V
MRD	-100.PA	200.PA	3.19 V	-3.19 V
DI0	-100.PA	100.PA	3.26 V	-3.19 V
DI1	-200.PA	200.PA	3.25 V	-3.19 V
DI2	-200.PA	200.PA	3.30 V	-3.25 V
DI3	-300.PA	100.PA	3.28 V	-3.23 V

	D00	D01	D02	D03
VOL1	95.0MV	95.0MV	105.MV	105.MV
VOL2	90.0MV	95.0MV	110.MV	105.MV
VOH1	4.89 V	4.89 V	4.88 V	4.88 V
VOH2	9.84 V	9.84 V	9.84 V	9.84 V
IDN1	7.95MA	7.85MA	7.15MA	7.20MA
IDN2	21.2MA	20.1MA	17.5MA	17.9MA
IDP1	-3.44MA	-3.49MA	-3.40MA	-3.43MA
IDP2	-7.78MA	-7.87MA	-7.61MA	-7.82MA
IOZ1	3.50NA	1.20NA	2.20NA	2.40NA
IOZ2	5.90NA	-1.50NA	5.70NA	-1.00NA
IOZ3	-1.20NA	5.60NA	-1.20NA	4.60NA
IOZ4	-100.PA	4.10NA	-1.10NA	4.70NA
IOZ5	4.50NA	-1.50NA	4.80NA	-1.40NA
IOZ6	4.30NA	-1.20NA	4.80NA	-1.50NA
IOZ7	4.40NA	-1.40NA	4.60NA	-1.50NA
IOZ8	4.20NA	-1.20NA	4.70NA	-1.50NA

ILDP	-5.00UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-230.UA
IL4	-230.UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	235.N	200.N	90.0N
DATA SETUP TIME	(TDS)	20.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	14.0N	14.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	110.N	96.0N	50.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	74.0N	66.0N	38.0N
CS1 SETUP TIME	(TCSS1)	156.N	134.N	70.0N
CS2 SETUP TIME	(TCSS2)	150.N	130.N	68.0N
CS1 HOLD TIME	(TCSH1)	44.0N	40.0N	26.0N
CS2 HOLD TIME	(TCSH2)	48.0N	42.0N	26.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	230.N	198.N	98.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	224.N	194.N	96.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	52.0N	46.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	150.N	120.N	38.0N
OUTPUT HOLD FROM CS2	(TDOH2)	146.N	118.N	38.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	32.0N
OUTPUT HOLD FROM MWR	(TPDH)	134.N	112.N	32.0N
READ CYCLE TIME	(TRC)	256.N	224.N	120.N
WRITE CYCLE TIME	(TWC)	224.N	200.N	120.N

	IIL	IIH	VIC1	VIC2
A0	-34.6NA	35.4NA	2.85 V	-2.85 V
A1	-34.8NA	34.2NA	2.89 V	-2.88 V
A2	-37.0NA	33.7NA	2.97 V	-2.96 V
A3	-34.1NA	36.6NA	2.94 V	-2.94 V
A4	-42.8NA	33.9NA	2.99 V	-3.02 V
A5	-36.2NA	34.4NA	2.85 V	-2.88 V
A6	-34.2NA	34.8NA	2.88 V	-2.91 V
A7	-34.4NA	33.7NA	2.88 V	-2.91 V
CS1	-34.5NA	35.2NA	2.95 V	-2.94 V
CS2	-34.7NA	35.6NA	2.99 V	-2.99 V
MWR	-32.3NA	35.4NA	2.94 V	-2.94 V
MRD	-35.3NA	34.7NA	2.94 V	-2.95 V
DI0	-33.2NA	34.8NA	3.00 V	-2.94 V
DI1	-35.1NA	36.5NA	2.98 V	-2.93 V
DI2	-34.2NA	40.0NA	3.06 V	-3.02 V
DI3	-34.2NA	34.2NA	3.03 V	-2.99 V

	D00	D01	D02	D03
VOL1	125.MV	130.MV	145.MV	140.MV
VOL2	130.MV	140.MV	165.MV	160.MV
VOH1	4.82 V	4.82 V	4.82 V	4.82 V
VOH2	9.74 V	9.75 V	9.73 V	9.74 V
IDN1	5.85MA	5.70MA	5.15MA	5.25MA
IDN2	14.6MA	13.6MA	11.7MA	12.1MA
IDP1	-2.16MA	-2.18MA	-2.11MA	-2.13MA
IDP2	-4.93MA	-4.95MA	-4.71MA	-4.92MA
IOZ1	-32.7NA	-39.4NA	-33.1NA	-35.2NA
IOZ2	-41.6NA	-39.9NA	-39.6NA	-34.1NA
IOZ3	-40.8NA	-47.8NA	-38.2NA	-41.2NA
IOZ4	-39.3NA	-48.4NA	-38.1NA	-42.7NA
IOZ5	-46.9NA	-43.3NA	-46.1NA	-36.4NA
IOZ6	-47.4NA	-44.2NA	-44.9NA	-36.2NA
IOZ7	-48.6NA	-44.5NA	-47.2NA	-37.9NA
IOZ8	-47.3NA	-45.1NA	-44.3NA	-38.1NA

ILDP	8.20UA
IL1	-40.0UA
IL2	-50.0UA
IL3	-170.UA
IL4	-165.UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	245.N	215.N	95.0N
DATA SETUP TIME	(TDS)	20.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	14.0N	14.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	4.00N	4.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	118.N	104.N	56.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-12.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	76.0N	68.0N	42.0N
CS1 SETUP TIME	(TCSS1)	158.N	138.N	74.0N
CS2 SETUP TIME	(TCSS2)	154.N	136.N	72.0N
CS1 HOLD TIME	(TCSH1)	46.0N	42.0N	28.0N
CS2 HOLD TIME	(TCSH2)	50.0N	44.0N	26.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	248.N	216.N	106.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	244.N	214.N	106.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	54.0N	50.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	150.N	120.N	40.0N
OUTPUT HOLD FROM CS2	(TDOH2)	146.N	116.N	40.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	36.0N
OUTPUT HOLD FROM MWR	(TPDH)	136.N	114.N	36.0N
READ CYCLE TIME	(TRC)	256.N	232.N	120.N
WRITE CYCLE TIME	(TWC)	216.N	200.N	128.N

	IIL	IIH	VIC1	VIC2
A0	-202.NA	198.NA	2.81 V	-2.81 V
A1	-199.NA	193.NA	2.86 V	-2.85 V
A2	-209.NA	195.NA	2.95 V	-2.94 V
A3	-203.NA	201.NA	2.91 V	-2.92 V
A4	-215.NA	194.NA	2.97 V	-3.00 V
A5	-200.NA	195.NA	2.81 V	-2.85 V
A6	-201.NA	197.NA	2.84 V	-2.89 V
A7	-201.NA	193.NA	2.84 V	-2.88 V
CS1	-204.NA	197.NA	2.92 V	-2.93 V
CS2	-201.NA	203.NA	2.96 V	-2.97 V
MWR	-198.NA	197.NA	2.92 V	-2.91 V
MRD	-204.NA	196.NA	2.91 V	-2.93 V
DI0	-192.NA	198.NA	2.97 V	-2.91 V
DI1	-196.NA	201.NA	2.95 V	-2.91 V
DI2	-196.NA	206.NA	3.04 V	-3.00 V
DI3	-195.NA	197.NA	3.00 V	-2.97 V

	D00	D01	D02	D03
VOL1	140.MV	145.MV	160.MV	160.MV
VOL2	145.MV	155.MV	185.MV	175.MV
VOH1	4.80 V	4.80 V	4.80 V	4.80 V
VOH2	9.72 V	9.72 V	9.70 V	9.72 V
IDN1	5.30MA	5.15MA	4.70MA	4.75MA
IDN2	13.0MA	12.2MA	10.5MA	10.8MA
IDP1	-1.94MA	-1.99MA	-1.91MA	-1.93MA
IDP2	-4.40MA	-4.47MA	-4.26MA	-4.39MA
IOZ1	-613.NA	-613.NA	-594.NA	-553.NA
IOZ2	-637.NA	-616.NA	-602.NA	-566.NA
IOZ3	-644.NA	-627.NA	-610.NA	-567.NA
IOZ4	-650.NA	-625.NA	-609.NA	-572.NA
IOZ5	-643.NA	-625.NA	-611.NA	-575.NA
IOZ6	-656.NA	-645.NA	-607.NA	-584.NA
IOZ7	-644.NA	-643.NA	-606.NA	-575.NA
IOZ8	-654.NA	-633.NA	-615.NA	-579.NA

ILDP	90.0UA
IL1	-180.UA
IL2	-240.UA
IL3	-270.UA
IL4	-250.UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	185.N	160.N	75.0N
DATA SETUP TIME	(TDS)	18.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	14.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	96.0N	84.0N	42.0N
ADDRESS HOLD TIME	(TAH)	-12.0N	-10.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	54.0N	50.0N	32.0N
CS1 SETUP TIME	(TCSS1)	128.N	112.N	60.0N
CS2 SETUP TIME	(TCSS2)	126.N	110.N	58.0N
CS1 HOLD TIME	(TCSH1)	32.0N	30.0N	22.0N
CS2 HOLD TIME	(TCSH2)	34.0N	30.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	178.N	156.N	82.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	176.N	154.N	80.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	40.0N	36.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	124.N	94.0N	22.0N
OUTPUT HOLD FROM CS2	(TDOH2)	122.N	94.0N	22.0N
OUTPUT HOLD FROM MRD	(TDOH3)	130.N	110.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	126.N	104.N	28.0N
READ CYCLE TIME	(TRC)	200.N	176.N	104.N
WRITE CYCLE TIME	(TWC)	176.N	160.N	104.N

	IIL	IIH	VIC1	VIC2
A0	-1.20NA	1.10NA	2.61 V	-2.59 V
A1	-1.60NA	800.PA	2.63 V	-2.65 V
A2	-1.00NA	1.00NA	2.64 V	-2.68 V
A3	-1.50NA	1.20NA	2.63 V	-2.67 V
A4	-1.10NA	3.40NA	2.63 V	-2.64 V
A5	-1.20NA	1.20NA	2.58 V	-2.63 V
A6	-1.10NA	1.30NA	2.61 V	-2.64 V
A7	-900.PA	1.10NA	2.60 V	-2.64 V
CS1	-1.10NA	1.10NA	2.62 V	-2.63 V
CS2	-1.00NA	1.30NA	2.64 V	-2.64 V
MWR	-1.20NA	900.PA	2.59 V	-2.61 V
MRD	-1.10NA	1.10NA	2.60 V	-2.62 V
DI0	-1.20NA	1.10NA	2.69 V	-2.65 V
DI1	-1.00NA	1.30NA	2.67 V	-2.63 V
DI2	-1.30NA	1.00NA	2.70 V	-2.66 V
DI3	-1.30NA	1.00NA	2.67 V	-2.64 V

	D00	D01	D02	D03
VOL1	85.0MV	90.0MV	95.0MV	95.0MV
VOL2	95.0MV	105.MV	120.MV	115.MV
VOH1	4.87 V	4.87 V	4.86 V	4.86 V
VOH2	9.80 V	9.80 V	9.80 V	9.80 V
IDN1	8.70MA	8.30MA	7.65MA	7.85MA
IDN2	20.1MA	18.3MA	15.8MA	16.5MA
IDP1	-3.00MA	-2.94MA	-2.89MA	-2.97MA
IDP2	-6.30MA	-6.26MA	-6.03MA	-6.33MA
IOZ1	36.0NA	35.8NA	42.3NA	35.6NA
IOZ2	32.3NA	37.7NA	38.8NA	37.9NA
IOZ3	33.0NA	37.9NA	37.7NA	40.1NA
IOZ4	36.1NA	34.2NA	40.6NA	37.0NA
IOZ5	30.9NA	40.0NA	38.5NA	42.5NA
IOZ6	31.8NA	41.2NA	38.5NA	41.2NA
IOZ7	31.7NA	40.4NA	38.1NA	41.5NA
IOZ8	31.1NA	40.3NA	37.8NA	40.5NA

ILDP	-5.00UA
IL1	-15.0UA
IL2	-25.0UA
IL3	-50.0UA
IL4	-50.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR.

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	185.N	155.N	65.0N
DATA SETUP TIME	(TDS)	20.0N	16.0N	6.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	14.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	88.0N	74.0N	36.0N
ADDRESS HOLD TIME	(TAH)	-10.0N	-10.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	56.0N	50.0N	30.0N
CS1 SETUP TIME	(TCSS1)	122.N	104.N	54.0N
CS2 SETUP TIME	(TCSS2)	120.N	102.N	52.0N
CS1 HOLD TIME	(TCSH1)	30.0N	28.0N	20.0N
CS2 HOLD TIME	(TCSH2)	32.0N	30.0N	18.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	168.N	144.N	80.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	166.N	142.N	78.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	36.0N	32.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	116.N	88.0N	20.0N
OUTPUT HOLD FROM CS2	(TDOH2)	116.N	86.0N	20.0N
OUTPUT HOLD FROM MRD	(TDOH3)	128.N	108.N	26.0N
OUTPUT HOLD FROM MWR	(TPDH)	124.N	104.N	24.0N
READ CYCLE TIME	(TRC)	192.N	168.N	104.N
WRITE CYCLE TIME	(TWC)	176.N	144.N	88.0N

	IIL	IIH	VIC1	VIC2
A0	-200.PA	200.PA	2.75 V	-2.73 V
A1	-300.PA	100.PA	2.77 V	-2.79 V
A2	-200.PA	100.PA	2.78 V	-2.81 V
A3	-300.PA	300.PA	2.76 V	-2.81 V
A4	-200.PA	1.40NA	2.77 V	-2.78 V
A5	-200.PA	200.PA	2.71 V	-2.76 V
A6	-200.PA	300.PA	2.74 V	-2.77 V
A7	-200.PA	200.PA	2.73 V	-2.78 V
CS1	-200.PA	200.PA	2.75 V	-2.76 V
CS2	-200.PA	200.PA	2.78 V	-2.77 V
MWR	-200.PA	100.PA	2.73 V	-2.75 V
MRD	-200.PA	200.PA	2.74 V	-2.75 V
DI0	-200.PA	200.PA	2.83 V	-2.78 V
DI1	-200.PA	300.PA	2.81 V	-2.76 V
DI2	-200.PA	200.PA	2.84 V	-2.79 V
DI3	-200.PA	200.PA	2.80 V	-2.77 V

	D00	D01	D02	D03
VOL1	75.0MV	75.0MV	85.0MV	80.0MV
VOL2	80.0MV	90.0MV	100.MV	95.0MV
VOH1	4.89 V	4.89 V	4.89 V	4.89 V
VOH2	9.84 V	9.84 V	9.83 V	9.84 V
IDN1	10.0MA	9.65MA	8.85MA	9.10MA
IDN2	23.4MA	21.4MA	18.6MA	19.3MA
IDP1	-3.56MA	-3.53MA	-3.44MA	-3.55MA
IDP2	-7.43MA	-7.39MA	-7.15MA	-7.49MA
IOZ1	7.70NA	1.90NA	6.80NA	2.50NA
IOZ2	6.50NA	1.10NA	7.50NA	800.PA
IOZ3	1.10NA	7.40NA	600.PA	7.80NA
IOZ4	4.10NA	4.50NA	3.10NA	5.30NA
IOZ5	4.50NA	2.60NA	5.60NA	2.50NA
IOZ6	4.50NA	3.20NA	5.80NA	2.20NA
IOZ7	4.80NA	2.70NA	5.60NA	2.30NA
IOZ8	4.60NA	3.10NA	5.80NA	2.00NA

ILDP	-5.00UA
IL1	-10.0UA
IL2	-20.0UA
IL3	-40.0UA
IL4	-35.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	175.N	140.N	60.0N
DATA SETUP TIME	(TDS)	22.0N	16.0N	6.00N
DATA HOLD TIME	(TDH)	6.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	10.0N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	84.0N	70.0N	32.0N
ADDRESS HOLD TIME	(TAH)	-12.0N	-10.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	50.0N	44.0N	28.0N
CS1 SETUP TIME	(TCSS1)	114.N	98.0N	90.0N
CS2 SETUP TIME	(TCSS2)	114.N	96.0N	48.0N
CS1 HOLD TIME	(TCSH1)	34.0N	28.0N	20.0N
CS2 HOLD TIME	(TCSH2)	34.0N	28.0N	18.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	166.N	136.N	76.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	162.N	134.N	74.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	32.0N	30.0N	20.0N
OUTPUT HOLD FROM CS1	(TDOH1)	110.N	82.0N	20.0N
OUTPUT HOLD FROM CS2	(TDOH2)	110.N	82.0N	20.0N
OUTPUT HOLD FROM MRD	(TDOH3)	126.N	108.N	24.0N
OUTPUT HOLD FROM MWR	(TPDH)	124.N	102.N	24.0N
READ CYCLE TIME	(TRC)	184.N	144.N	96.0N
WRITE CYCLE TIME	(TWC)	168.N	136.N	88.0N

	IIL	IIH	VIC1	VIC2
A0	0.00 A	0.00 A	2.85 V	-2.84 V
A1	0.00 A	0.00 A	2.88 V	-2.89 V
A2	-100.PA	0.00 A	2.88 V	-2.91 V
A3	-100.PA	100.PA	2.87 V	-2.91 V
A4	0.00 A	300.PA	2.88 V	-2.88 V
A5	0.00 A	100.PA	2.83 V	-2.87 V
A6	0.00 A	100.PA	2.85 V	-2.88 V
A7	0.00 A	100.PA	2.84 V	-2.88 V
CS1	0.00 A	100.PA	2.87 V	-2.87 V
CS2	0.00 A	100.PA	2.89 V	-2.88 V
MWR	0.00 A	0.00 A	2.84 V	-2.86 V
MRD	0.00 A	100.PA	2.85 V	-2.85 V
DI0	0.00 A	0.00 A	2.93 V	-2.89 V
DI1	0.00 A	100.PA	2.92 V	-2.86 V
DI2	0.00 A	0.00 A	2.94 V	-2.89 V
DI3	0.00 A	0.00 A	2.91 V	-2.88 V

	DO0	DO1	DO2	DO3
VOL1	65.0MV	65.0MV	75.0MV	70.0MV
VOL2	70.0MV	75.0MV	90.0MV	85.0MV
VOH1	4.90 V	4.91 V	4.90 V	4.91 V
VOH2	9.86 V	9.86 V	9.85 V	9.86 V
IDN1	11.3MA	10.8MA	10.0MA	10.2MA
IDN2	26.5MA	24.3MA	21.3MA	22.0MA
IDP1	-4.11MA	-4.13MA	-4.06MA	-4.17MA
IDP2	-8.56MA	-8.70MA	-8.34MA	-8.73MA
IOZ1	-1.00NA	5.90NA	-1.50NA	5.10NA
IOZ2	400.PA	3.50NA	-1.10NA	4.00NA
IOZ3	3.60NA	-1.00NA	3.90NA	-1.30NA
IOZ4	-100.PA	2.70NA	500.PA	2.00NA
IOZ5	2.80NA	800.PA	1.70NA	1.80NA
IOZ6	2.90NA	1.00NA	1.20NA	1.80NA
IOZ7	2.40NA	1.10NA	1.50NA	2.00NA
IOZ8	2.80NA	1.20NA	1.20NA	1.90NA

ILDP	-5.00UA
IL1	-10.0UA
IL2	-20.0UA
IL3	-30.0UA
IL4	-35.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	190.N	170.N	80.0N
DATA SETUP TIME	(TDS)	18.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	10.0N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	102.N	92.0N	48.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-10.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	64.0N	58.0N	36.0N
CS1 SETUP TIME	(TCSS1)	134.N	118.N	64.0N
CS2 SETUP TIME	(TCSS2)	132.N	116.N	62.0N
CS1 HOLD TIME	(TCSH1)	40.0N	38.0N	26.0N
CS2 HOLD TIME	(TCSH2)	42.0N	38.0N	24.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	192.N	170.N	90.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	190.N	168.N	90.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	44.0N	40.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	128.N	98.0N	24.0N
OUTPUT HOLD FROM CS2	(TDOH2)	126.N	96.0N	24.0N
OUTPUT HOLD FROM MRD	(TDOH3)	132.N	112.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	128.N	106.N	30.0N
READ CYCLE TIME	(TRC)	216.N	192.N	120.N
WRITE CYCLE TIME	(TWC)	184.N	176.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-13.4NA	12.9NA	2.53 V	-2.51 V
A1	-14.2NA	12.5NA	2.56 V	-2.58 V
A2	-13.5NA	13.3NA	2.58 V	-2.61 V
A3	-14.7NA	14.2NA	2.55 V	-2.61 V
A4	-13.3NA	18.6NA	2.56 V	-2.58 V
A5	-14.1NA	13.4NA	2.50 V	-2.55 V
A6	-13.2NA	13.3NA	2.53 V	-2.57 V
A7	-13.1NA	13.7NA	2.52 V	-2.57 V
CS1	-14.6NA	13.4NA	2.54 V	-2.55 V
CS2	-13.0NA	14.7NA	2.57 V	-2.58 V
MWR	-13.3NA	12.5NA	2.51 V	-2.54 V
MRD	-13.0NA	13.0NA	2.52 V	-2.54 V
DI0	-12.9NA	13.9NA	2.62 V	-2.59 V
DI1	-13.0NA	13.9NA	2.60 V	-2.55 V
DI2	-13.0NA	13.1NA	2.63 V	-2.59 V
DI3	-13.1NA	12.5NA	2.60 V	-2.58 V

	D00	D01	D02	D03
VOL1	100.MV	105.MV	115.MV	110.MV
VOL2	110.MV	125.MV	145.MV	135.MV
VOH1	4.84 V	4.84 V	4.84 V	4.84 V
VOH2	9.76 V	9.76 V	9.76 V	9.77 V
IDN1	7.30MA	7.00MA	6.40MA	6.60MA
IDN2	16.9MA	15.4MA	13.3MA	13.9MA
IDP1	-2.52MA	-2.48MA	-2.39MA	-2.50MA
IDP2	-5.31MA	-5.29MA	-5.06MA	-5.36MA
IOZ1	411.NA	463.NA	471.NA	458.NA
IOZ2	408.NA	458.NA	477.NA	456.NA
IOZ3	404.NA	460.NA	473.NA	458.NA
IOZ4	410.NA	454.NA	482.NA	460.NA
IOZ5	417.NA	472.NA	502.NA	486.NA
IOZ6	435.NA	476.NA	494.NA	485.NA
IOZ7	418.NA	481.NA	485.NA	476.NA
IOZ8	420.NA	465.NA	494.NA	473.NA

ILDP	-5.00UA
IL1	-30.0UA
IL2	-45.0UA
IL3	-75.0UA
IL4	-75.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	205.N	180.N	90.0N
DATA SETUP TIME	(TDS)	20.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	110.N	100.N	56.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-12.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	70.0N	62.0N	38.0N
CS1 SETUP TIME	(TCSS1)	144.N	126.N	70.0N
CS2 SETUP TIME	(TCSS2)	140.N	126.N	68.0N
CS1 HOLD TIME	(TCSH1)	46.0N	40.0N	28.0N
CS2 HOLD TIME	(TCSH2)	46.0N	42.0N	26.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	208.N	184.N	102.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	204.N	182.N	98.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	48.0N	42.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	132.N	102.N	28.0N
OUTPUT HOLD FROM CS2	(TDOH2)	130.N	100.N	28.0N
OUTPUT HOLD FROM MRD	(TDOH3)	132.N	114.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	130.N	108.N	32.0N
READ CYCLE TIME	(TRC)	224.N	200.N	120.N
WRITE CYCLE TIME	(TWC)	200.N	176.N	120.N

	IIL	IIH	VIC1	VIC2
A0	-82.6NA	79.4NA	2.47 V	-2.46 V
A1	-83.0NA	77.1NA	2.50 V	-2.52 V
A2	-81.9NA	77.5NA	2.52 V	-2.56 V
A3	-85.3NA	83.9NA	2.50 V	-2.55 V
A4	-83.5NA	91.9NA	2.50 V	-2.51 V
A5	-84.9NA	77.7NA	2.44 V	-2.49 V
A6	-82.0NA	75.5NA	2.47 V	-2.51 V
A7	-82.7NA	79.8NA	2.46 V	-2.51 V
CS1	-92.0NA	81.5NA	2.48 V	-2.49 V
CS2	-81.0NA	82.9NA	2.51 V	-2.52 V
MWR	-81.7NA	73.7NA	2.45 V	-2.48 V
MRD	-80.9NA	76.8NA	2.46 V	-2.48 V
DI0	-78.2NA	79.5NA	2.57 V	-2.52 V
DI1	-78.3NA	77.3NA	2.54 V	-2.50 V
DI2	-77.8NA	74.9NA	2.57 V	-2.53 V
DI3	-78.9NA	74.3NA	2.54 V	-2.52 V

	D00	D01	D02	D03
VOL1	115.MV	120.MV	130.MV	130.MV
VOL2	125.MV	140.MV	165.MV	155.MV
VOH1	4.82 V	4.82 V	4.82 V	4.82 V
VOH2	9.73 V	9.73 V	9.72 V	9.74 V
IDN1	6.45MA	6.15MA	5.65MA	5.80MA
IDN2	14.9MA	13.6MA	11.7MA	12.2MA
IDP1	-2.23MA	-2.23MA	-2.16MA	-2.22MA
IDP2	-4.74MA	-4.74MA	-4.53MA	-4.77MA
IOZ1	1.94UA	2.13UA	2.20UA	2.12UA
IOZ2	1.91UA	2.14UA	2.19UA	2.13UA
IOZ3	1.92UA	2.13UA	2.21UA	2.13UA
IOZ4	1.90UA	2.14UA	2.20UA	2.14UA
IOZ5	1.97UA	2.20UA	2.31UA	2.25UA
IOZ6	1.99UA	2.21UA	2.28UA	2.19UA
IOZ7	1.96UA	2.19UA	2.26UA	2.19UA
IOZ8	1.95UA	2.19UA	2.25UA	2.19UA

ILDP	40.0UA
IL1	-90.0UA
IL2	-120.UA
IL3	-150.UA
IL4	-135.UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	195.N	160.N	70.0N
DATA SETUP TIME	(TDS)	20.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	18.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	96.0N	82.0N	40.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-10.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	62.0N	54.0N	34.0N
CS1 SETUP TIME	(TCSS1)	432.N	354.N	72.0N
CS2 SETUP TIME	(TCSS2)	210.N	164.N	60.0N
CS1 HOLD TIME	(TCSH1)	40.0N	36.0N	24.0N
CS2 HOLD TIME	(TCSH2)	40.0N	36.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	176.N	152.N	82.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	172.N	150.N	82.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	38.0N	34.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	122.N	92.0N	20.0N
OUTPUT HOLD FROM CS2	(TDOH2)	120.N	92.0N	22.0N
OUTPUT HOLD FROM MRD	(TDOH3)	130.N	110.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	126.N	106.N	28.0N
READ CYCLE TIME	(TRC)	200.N	176.N	112.N
WRITE CYCLE TIME	(TWC)	184.N	176.N	104.N

	IIL	IIH	VIC1	VIC2
A0	-2.00NA	1.50NA	2.77 V	-2.78 V
A1	-1.80NA	1.80NA	2.80 V	-2.83 V
A2	-1.80NA	1.60NA	2.82 V	-2.86 V
A3	-2.00NA	2.10NA	2.85 V	-2.87 V
A4	-2.20NA	1.70NA	2.82 V	-2.84 V
A5	-1.90NA	1.90NA	2.73 V	-2.83 V
A6	-1.70NA	2.20NA	2.73 V	-2.76 V
A7	-1.50NA	2.20NA	2.75 V	-2.77 V
CS1	-1.60NA	1.90NA	2.76 V	-2.77 V
CS2	-2.00NA	1.80NA	4.96 V	-4.95 V
MWR	-1.70NA	1.60NA	2.78 V	-2.80 V
MRD	-1.70NA	1.60NA	2.77 V	-2.78 V
DI0	-1.80NA	1.70NA	2.84 V	-2.80 V
DI1	-1.70NA	1.80NA	2.83 V	-2.79 V
DI2	-1.90NA	1.60NA	2.81 V	-2.80 V
DI3	-1.90NA	1.80NA	2.82 V	-2.77 V

	D00	D01	D02	D03
VOL1	75.0MV	80.0MV	85.0MV	85.0MV
VOL2	85.0MV	95.0MV	110.MV	105.MV
VOH1	4.88 V	4.88 V	4.88 V	4.88 V
VOH2	9.81 V	9.82 V	9.91 V	9.82 V
IDN1	9.65MA	9.35MA	8.55MA	8.70MA
IDN2	21.7MA	20.1MA	17.3MA	18.0MA
IDP1	-3.11MA	-3.18MA	-3.05MA	-3.21MA
IDP2	-6.65MA	-6.82MA	-6.48MA	-6.91MA
IOZ1	51.7NA	63.9NA	53.7NA	62.2NA
IOZ2	53.7NA	60.9NA	55.6NA	60.1NA
IOZ3	54.7NA	58.3NA	59.0NA	56.0NA
IOZ4	51.4NA	62.0NA	55.2NA	59.6NA
IOZ5	56.9NA	58.7NA	59.8NA	60.1NA
IOZ6	57.4NA	58.9NA	59.7NA	58.5NA
IOZ7	57.7NA	58.4NA	59.4NA	58.3NA
IOZ8	56.4NA	58.2NA	59.4NA	57.9NA

ILDP	-5.00UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-5.00UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	185.N	150.N	65.0N
DATA SETUP TIME	(TDS)	20.0N	16.0N	6.00N
DATA HOLD TIME	(TDH)	6.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	90.0N	74.0N	36.0N
ADDRESS HOLD TIME	(TAH)	-12.0N	-10.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	62.0N	54.0N	32.0N
CS1 SETUP TIME	(TCSS1)	134.N	114.N	58.0N
CS2 SETUP TIME	(TCSS2)	132.N	112.N	54.0N
CS1 HOLD TIME	(TCSH1)	38.0N	34.0N	22.0N
CS2 HOLD TIME	(TCSH2)	38.0N	34.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	170.N	146.N	80.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	168.N	142.N	78.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	34.0N	32.0N	20.0N
OUTPUT HOLD FROM CS1	(TDOH1)	116.N	86.0N	20.0N
OUTPUT HOLD FROM CS2	(TDOH2)	114.N	86.0N	20.0N
OUTPUT HOLD FROM MRD	(TDOH3)	130.N	108.N	26.0N
OUTPUT HOLD FROM MWR	(TPDH)	124.N	104.N	28.0N
READ CYCLE TIME	(TRC)	192.N	168.N	104.N
WRITE CYCLE TIME	(TWC)	176.N	168.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-400.PA	200.PA	2.84 V	-2.85 V
A1	-300.PA	300.PA	2.88 V	-2.89 V
A2	-300.PA	200.PA	2.89 V	-2.92 V
A3	-400.PA	300.PA	2.91 V	-2.93 V
A4	-600.PA	200.PA	2.89 V	-2.89 V
A5	-400.PA	300.PA	2.80 V	-2.89 V
A6	-200.PA	400.PA	2.80 V	-2.83 V
A7	-200.PA	400.PA	2.83 V	-2.84 V
CS1	-200.PA	300.PA	2.84 V	-2.84 V
CS2	-300.PA	300.PA	2.86 V	-2.89 V
MWR	-300.PA	200.PA	2.85 V	-2.87 V
MRD	-300.PA	300.PA	2.85 V	-2.85 V
DI0	-300.PA	200.PA	2.91 V	-2.87 V
DI1	-300.PA	300.PA	2.89 V	-2.86 V
DI2	-300.PA	200.PA	2.89 V	-2.86 V
DI3	-300.PA	300.PA	2.89 V	-2.84 V

	D00	D01	D02	D03
VOL1	65.0MV	70.0MV	75.0MV	75.0MV
VOL2	75.0MV	80.0MV	95.0MV	90.0MV
VOH1	4.89 V	4.90 V	4.89 V	4.90 V
VOH2	9.84 V	9.85 V	9.84 V	9.85 V
IDN1	11.1MA	10.7MA	9.85MA	10.0MA
IDN2	25.2MA	23.3MA	20.2MA	20.9MA
IDP1	-3.68MA	-3.76MA	-3.69MA	-3.81MA
IDP2	-7.83MA	-8.04MA	-7.69MA	-8.15MA
IOZ1	7.40NA	7.00NA	7.80NA	5.20NA
IOZ2	4.10NA	10.3NA	4.40NA	8.40NA
IOZ3	9.80NA	5.30NA	8.10NA	5.50NA
IOZ4	9.90NA	3.90NA	10.0NA	3.70NA
IOZ5	3.30NA	10.9NA	3.50NA	11.3NA
IOZ6	3.60NA	11.2NA	3.20NA	10.8NA
IOZ7	3.30NA	11.1NA	3.40NA	11.1NA
IOZ8	3.50NA	11.2NA	3.10NA	10.7NA

ILDP	-15.0UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-5.00UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	175.N	145.N	60.0N
DATA SETUP TIME	(TDS)	24.0N	18.0N	6.00N
DATA HOLD TIME	(TDH)	6.00N	6.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	14.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	86.0N	70.0N	32.0N
ADDRESS HOLD TIME	(TAH)	-12.0N	-10.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	54.0N	56.0N	30.0N
CS1 SETUP TIME	(TCSS1)	128.N	108.N	54.0N
CS2 SETUP TIME	(TCSS2)	126.N	106.N	52.0N
CS1 HOLD TIME	(TCSH1)	42.0N	34.0N	22.0N
CS2 HOLD TIME	(TCSH2)	42.0N	34.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	166.N	136.N	76.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	162.N	134.N	74.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	32.0N	30.0N	20.0N
OUTPUT HOLD FROM CS1	(TDOH1)	110.N	82.0N	18.0N
OUTPUT HOLD FROM CS2	(TDOH2)	108.N	82.0N	20.0N
OUTPUT HOLD FROM MRD	(TDOH3)	128.N	108.N	26.0N
OUTPUT HOLD FROM MWR	(TPDH)	124.N	104.N	26.0N
READ CYCLE TIME	(TRC)	184.N	144.N	96.0N
WRITE CYCLE TIME	(TWC)	168.N	168.N	88.0N

	IIL	IIH	VIC1	VIC2
A0	-100.PA	100.PA	2.91 V	-2.91 V
A1	-100.PA	100.PA	2.94 V	-2.95 V
A2	-100.PA	100.PA	2.95 V	-2.98 V
A3	-100.PA	100.PA	2.97 V	-2.99 V
A4	-200.PA	100.PA	2.95 V	-2.95 V
A5	-100.PA	100.PA	2.88 V	-2.95 V
A6	0.00 A	100.PA	2.87 V	-2.90 V
A7	-100.PA	100.PA	2.89 V	-2.91 V
CS1	-100.PA	100.PA	2.90 V	-2.91 V
CS2	-100.PA	100.PA	2.93 V	-2.95 V
MWR	-100.PA	0.00 A	2.91 V	-2.93 V
MRD	-100.PA	100.PA	2.91 V	-2.91 V
DI0	-100.PA	100.PA	2.98 V	-2.93 V
DI1	0.00 A	100.PA	2.96 V	-2.93 V
DI2	-100.PA	100.PA	2.95 V	-2.93 V
DI3	-100.PA	100.PA	2.95 V	-2.91 V

	D00	D01	D02	D03
VOL1	60.0MV	60.0MV	65.0MV	65.0MV
VOL2	65.0MV	70.0MV	85.0MV	80.0MV
VOH1	4.91 V	4.91 V	4.91 V	4.91 V
VOH2	9.87 V	9.87 V	9.86 V	9.88 V
IDN1	12.3MA	12.0MA	11.0MA	11.2MA
IDN2	28.3MA	26.3MA	22.8MA	23.7MA
IDP1	-4.23MA	-4.39MA	-4.29MA	-4.44MA
IDP2	-8.97MA	-9.24MA	-8.92MA	-9.40MA
IOZ1	6.60NA	-800.PA	6.10NA	-800.PA
IOZ2	3.70NA	600.PA	4.10NA	-600.PA
IOZ3	900.PA	4.30NA	-700.PA	4.50NA
IOZ4	4.50NA	600.PA	2.70NA	1.20NA
IOZ5	10.2UA	10.2UA	10.2UA	10.2UA
IOZ6	-700.PA	5.80NA	-1.50NA	5.80NA
IOZ7	-800.PA	5.40NA	-1.40NA	5.90NA
IOZ8	-500.PA	5.30NA	-1.50NA	5.50NA
ILOP	-10.0UA			
IL1	-5.00UA			
IL2	-5.00UA			
IL3	-5.00UA			
IL4	-5.00UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	185.N	160.N	80.0N
DATA SETUP TIME	(TDS)	20.0N	18.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	10.0N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	98.0N	88.0N	46.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	70.0N	62.0N	38.0N
CS1 SETUP TIME	(TCSS1)	140.N	124.N	68.0N
CS2 SETUP TIME	(TCSS2)	138.N	122.N	66.0N
CS1 HOLD TIME	(TCSH1)	48.0N	44.0N	30.0N
CS2 HOLD TIME	(TCSH2)	50.0N	46.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	184.N	164.N	90.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	180.N	160.N	88.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	42.0N	38.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	124.N	94.0N	1.00K
OUTPUT HOLD FROM CS2	(TDOH2)	124.N	94.0N	22.0N
OUTPUT HOLD FROM MRD	(TDOH3)	132.N	112.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	128.N	106.N	30.0N
READ CYCLE TIME	(TRC)	208.N	184.N	120.N
WRITE CYCLE TIME	(TWC)	192.N	176.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-22.1NA	20.8NA	2.73 V	-2.74 V
A1	-22.3NA	22.5NA	2.77 V	-2.79 V
A2	-22.5NA	22.0NA	2.79 V	-2.83 V
A3	-23.1NA	23.4NA	2.81 V	-2.84 V
A4	-22.8NA	21.9NA	2.79 V	-2.80 V
A5	-22.7NA	22.7NA	2.69 V	-2.78 V
A6	-21.9NA	22.3NA	2.69 V	-2.72 V
A7	-20.7NA	22.9NA	2.72 V	-2.73 V
CS1	-22.4NA	21.8NA	2.73 V	-2.74 V
CS2	-21.1NA	22.6NA	2.75 V	-2.80 V
MWR	-21.3NA	21.8NA	2.74 V	-2.77 V
MRD	-21.5NA	20.3NA	2.74 V	-2.74 V
DI0	-20.9NA	21.0NA	2.80 V	-2.76 V
DI1	-20.5NA	21.7NA	2.79 V	-2.76 V
DI2	-21.0NA	20.2NA	2.78 V	-2.76 V
DI3	-21.6NA	21.3NA	2.78 V	-2.74 V

	D00	D01	D02	D03
VOL1	90.0MV	95.0MV	105.MV	100.MV
VOL2	105.MV	110.MV	130.MV	125.MV
VOH1	4.85 V	4.86 V	4.85 V	4.86 V
VOH2	9.78 V	9.78 V	9.77 V	9.78 V
IDN1	8.20MA	7.90MA	7.20MA	7.35MA
IDN2	18.3MA	16.9MA	14.5MA	15.1MA
IDP1	-2.60MA	-2.65MA	-2.59MA	-2.69MA
IDP2	-5.58MA	-5.73MA	-5.47MA	-5.82MA
IOZ1	606.NA	649.NA	644.NA	634.NA
IOZ2	609.NA	642.NA	640.NA	638.NA
IOZ3	606.NA	646.NA	644.NA	636.NA
IOZ4	608.NA	647.NA	639.NA	644.NA
IOZ5	616.NA	655.NA	662.NA	665.NA
IOZ6	616.NA	670.NA	649.NA	655.NA
IOZ7	609.NA	658.NA	654.NA	645.NA
IOZ8	618.NA	657.NA	649.NA	653.NA
ILDP	20.0UA			
IL1	-25.0UA			
IL2	-30.0UA			
IL3	-30.0UA			
IL4	-25.0UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	195.N	175.N	90.0N
DATA SETUP TIME	(TDS)	22.0N	18.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	104.N	96.0N	50.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	74.0N	68.0N	42.0N
CS1 SETUP TIME	(TCSS1)	148.N	132.N	74.0N
CS2 SETUP TIME	(TCSS2)	144.N	128.N	70.0N
CS1 HOLD TIME	(TCSH1)	52.0N	46.0N	30.0N
CS2 HOLD TIME	(TCSH2)	54.0N	48.0N	30.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	198.N	178.N	100.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	194.N	174.N	96.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	46.0N	42.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	128.N	98.0N	24.0N
OUTPUT HOLD FROM CS2	(TDOH2)	128.N	98.0N	24.0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	114.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	130.N	108.N	32.0N
READ CYCLE TIME	(TRC)	216.N	192.N	120.N
WRITE CYCLE TIME	(TWC)	200.N	184.N	128.N

	IIL	IIH	VIC1	VIC2
A0	-127.NA	118.NA	2.72 V	-2.72 V
A1	-127.NA	121.NA	2.76 V	-2.78 V
A2	-129.NA	123.NA	2.77 V	-2.81 V
A3	-128.NA	124.NA	2.80 V	-2.83 V
A4	-125.NA	118.NA	2.78 V	-2.79 V
A5	-126.NA	121.NA	2.67 V	-2.77 V
A6	-125.NA	119.NA	2.67 V	-2.70 V
A7	-120.NA	118.NA	2.70 V	-2.71 V
CS1	-129.NA	118.NA	2.71 V	-2.72 V
CS2	-122.NA	122.NA	2.73 V	-2.78 V
MWR	-122.NA	118.NA	2.73 V	-2.76 V
MRD	-122.NA	114.NA	2.72 V	-2.73 V
DI0	-118.NA	117.NA	2.79 V	-2.74 V
DI1	-118.NA	117.NA	2.77 V	-2.74 V
DI2	-116.NA	110.NA	2.76 V	-2.74 V
DI3	-116.NA	113.NA	2.77 V	-2.72 V

	D00	D01	D02	D03
VOL1	100.MV	105.MV	115.MV	115.MV
VOL2	115.MV	125.MV	150.MV	145.MV
VOH1	4.82 V	4.84 V	4.83 V	4.84 V
VOH2	9.75 V	9.76 V	9.74 V	9.76 V
IDN1	7.25MA	7.00MA	6.40MA	6.50MA
IDN2	16.2MA	14.9MA	12.8MA	13.4MA
IDP1	-2.31MA	-2.39MA	-2.31MA	-2.40MA
IDP2	-5.03MA	-5.16MA	-4.89MA	-5.22MA
IOZ1	2.61UA	2.76UA	2.73UA	2.71UA
IOZ2	2.59UA	2.77UA	2.72UA	2.71UA
IOZ3	2.60UA	2.75UA	2.73UA	2.71UA
IOZ4	2.59UA	2.76UA	2.72UA	2.72UA
IOZ5	2.64UA	2.80UA	2.81UA	2.81UA
IOZ6	2.66UA	2.82UA	2.78UA	2.76UA
IOZ7	2.63UA	2.80UA	2.77UA	2.76UA
IOZ8	2.62UA	2.80UA	2.76UA	2.76UA
ILDP	40.0UA			
IL1	-105.UA			
IL2	-115.UA			
IL3	-125.UA			
IL4	-100.UA			

RCA COP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN: 16

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	295.N	240.N	95.0N
DATA SETUP TIME	(TDS)	36.0N	28.0N	10.0N
DATA HOLD TIME	(TDH)	10.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	18.0N	14.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	138.N	112.N	52.0N
ADDRESS HOLD TIME	(TAH)	-26.0N	-20.0N	-6.00N
WRITE PULSE WIDTH	(TWP)	96.0N	80.0N	42.0N
CS1 SETUP TIME	(TCSS1)	218.N	178.N	80.0N
CS2 SETUP TIME	(TCSS2)	254.N	214.N	100.N
CS1 HOLD TIME	(TCSH1)	62.0N	54.0N	38.0N
CS2 HOLD TIME	(TCSH2)	0.00	0.00	0.00
OUTPUT ACTIVE FROM CS1	(TDOA1)	278.N	232.N	104.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	314.N	266.N	122.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	62.0N	54.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	166.N	132.N	40.0N
OUTPUT HOLD FROM CS2	(TDOH2)	232.N	204.N	92.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	122.N	34.0N
OUTPUT HOLD FROM MWR	(TPDH)	142.N	118.N	36.0N
READ CYCLE TIME	(TRC)	312.N	256.N	128.N
WRITE CYCLE TIME	(TWC)	304.N	280.N	120.N

	IIL	IIH	VIC1	VIC2
A0	-3.00NA	2.60NA	3.40 V	-3.40 V
A1	-2.80NA	3.00NA	3.44 V	-3.44 V
A2	-2.60NA	2.80NA	3.48 V	-3.49 V
A3	-2.80NA	2.70NA	3.47 V	-3.48 V
A4	-2.70NA	2.70NA	3.44 V	-3.47 V
A5	-3.00NA	2.60NA	3.37 V	-3.41 V
A6	-2.70NA	2.30NA	3.43 V	-3.34 V
A7	-2.90NA	2.70NA	3.41 V	-3.43 V
CS1	-2.50NA	2.90NA	3.47 V	-3.45 V
CS2	-2.80NA	4.50NA	4.96 V	-4.95 V
MWR	-2.60NA	2.60NA	3.41 V	-3.43 V
MRD	-2.50NA	2.50NA	3.42 V	-3.42 V
DI0	-2.80NA	2.60NA	3.54 V	-3.48 V
DI1	-3.00NA	2.40NA	3.53 V	-3.48 V
DI2	-2.70NA	2.80NA	3.49 V	-3.46 V
DI3	-3.30NA	2.40NA	3.45 V	-3.44 V

	DO0	DO1	DO2	DO3
VOL1	115.MV	115.MV	125.MV	120.MV
VOL2	115.MV	125.MV	140.MV	135.MV
VOH1	4.82 V	4.82 V	4.82 V	4.82 V
VOH2	9.76 V	9.76 V	9.76 V	9.77 V
IDN1	6.50MA	6.35MA	6.00MA	6.10MA
IDN2	16.2MA	15.2MA	13.8MA	14.1MA
IDP1	-2.21MA	-2.23MA	-2.18MA	-2.24MA
IDP2	-5.22MA	-5.27MA	-5.13MA	-5.33MA
IOZ1	21.7NA	28.9NA	20.5NA	26.9NA
IOZ2	23.9NA	26.1NA	22.5NA	24.3NA
IOZ3	25.1NA	23.8NA	25.2NA	20.3NA
IOZ4	22.0NA	27.4NA	21.6NA	23.7NA
IOZ5	26.5NA	23.5NA	24.4NA	22.5NA
IOZ6	26.2NA	23.7NA	24.7NA	22.5NA
IOZ7	26.6NA	23.6NA	24.1NA	22.5NA
IOZ8	26.0NA	23.7NA	24.5NA	22.5NA

ILDP	-2.00UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-5.00UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	320.N	245.N	85.0N
DATA SETUP TIME	(TDS)	42.0N	32.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	32.0N	20.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	146.N	114.N	48.0N
ADDRESS HOLD TIME	(TAH)	-26.0N	-20.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	106.N	84.0N	38.0N
CS1 SETUP TIME	(TCSS1)	218.N	172.N	74.0N
CS2 SETUP TIME	(TCSS2)	266.N	222.N	102.N
CS1 HOLD TIME	(TCSH1)	54.0N	46.0N	26.0N
CS2 HOLD TIME	(TCSH2)	0.00	0.00	0.00
OUTPUT ACTIVE FROM CS1	(TDOA1)	284.N	228.N	96.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	340.N	274.N	114.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	58.0N	50.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	158.N	124.N	38.0N
OUTPUT HOLD FROM CS2	(TDOH2)	248.N	212.N	104.N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	120.N	34.0N
OUTPUT HOLD FROM MWR	(TPDH)	138.N	116.N	32.0N
READ CYCLE TIME	(TRC)	296.N	240.N	120.N
WRITE CYCLE TIME	(TWC)	304.N	248.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-400.PA	300.PA	3.42 V	-3.41 V
A1	-300.PA	300.PA	3.46 V	-3.45 V
A2	-300.PA	300.PA	3.49 V	-3.50 V
A3	-300.PA	300.PA	3.48 V	-3.49 V
A4	-300.PA	500.PA	3.46 V	-3.48 V
A5	-300.PA	300.PA	3.38 V	-3.43 V
A6	-300.PA	200.PA	3.44 V	-3.38 V
A7	-500.PA	300.PA	3.42 V	-3.44 V
CS1	-300.PA	300.PA	3.48 V	-3.45 V
CS2	-400.PA	1.00NA	4.96 V	-4.95 V
MWR	-300.PA	300.PA	3.42 V	-3.44 V
MRD	-300.PA	300.PA	3.44 V	-3.43 V
DI0	-300.PA	300.PA	3.55 V	-3.48 V
DI1	-500.PA	200.PA	3.54 V	-3.48 V
DI2	-300.PA	400.PA	3.50 V	-3.46 V
DI3	-400.PA	200.PA	3.46 V	-3.44 V

	D00	D01	D02	D03
VOL1	100.MV	105.MV	110.MV	105.MV
VOL2	100.MV	110.MV	120.MV	115.MV
VOH1	4.85 V	4.86 V	4.85 V	4.85 V
VOH2	9.80 V	9.80 V	9.80 V	9.80 V
IDN1	7.20MA	7.05MA	6.75MA	6.80MA
IDN2	18.4MA	17.4MA	15.8MA	16.3MA
IDP1	-2.61MA	-2.63MA	-2.61MA	-2.64MA
IDP2	-6.19MA	-6.25MA	-6.13MA	-6.31MA
IOZ1	7.10NA	3.20NA	5.80NA	3.20NA
IOZ2	7.70NA	1.30NA	8.10NA	700.PA
IOZ3	1.20NA	8.60NA	800.PA	7.70NA
IOZ4	3.50NA	6.10NA	2.00NA	6.10NA
IOZ5	6.30NA	2.30NA	6.60NA	1.20NA
IOZ6	6.20NA	2.80NA	6.70NA	1.10NA
IOZ7	6.30NA	2.20NA	6.60NA	1.10NA
IOZ8	6.20NA	2.30NA	6.80NA	900.PA
ILDP	-5.00UA			
IL1	-5.00UA			
IL2	-5.00UA			
IL3	-5.00UA			
IL4	-5.00UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	325.N	240.N	80.0N
DATA SETUP TIME	(TDS)	56.0N	38.0N	8.00N
DATA HOLD TIME	(TDH)	6.00N	6.00N	8.00N
ADDRESS SETUP TIME	(TAS1)	36.0N	18.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	142.N	108.N	42.0N
ADDRESS HOLD TIME	(TAH)	-26.0N	-20.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	120.N	76.0N	38.0N
CS1 SETUP TIME	(TCSS1)	220.N	164.N	70.0N
CS2 SETUP TIME	(TCSS2)	284.N	232.N	102.N
CS1 HOLD TIME	(TCSH1)	54.0N	52.0N	24.0N
CS2 HOLD TIME	(TCSH2)	0.00	0.00	0.00
OUTPUT ACTIVE FROM CS1	(TDOA1)	288.N	222.N	88.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	342.N	270.N	112.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	54.0N	46.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	152.N	118.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	262.N	224.N	112.N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	138.N	114.N	32.0N
READ CYCLE TIME	(TRC)	280.N	224.N	120.N
WRITE CYCLE TIME	(TWC)	320.N	280.N	104.N

	IIL	IIH	VIC1	VIC2
A0	-100.PA	100.PA	3.46 V	-3.45 V
A1	-100.PA	100.PA	3.50 V	-3.49 V
A2	0.00 A	100.PA	3.53 V	-3.54 V
A3	-100.PA	100.PA	3.52 V	-3.52 V
A4	-100.PA	100.PA	3.50 V	-3.51 V
A5	-100.PA	100.PA	3.42 V	-3.47 V
A6	-100.PA	100.PA	3.47 V	-3.43 V
A7	-100.PA	100.PA	3.46 V	-3.48 V
CS1	-100.PA	100.PA	3.52 V	-3.49 V
CS2	-100.PA	400.PA	4.97 V	-4.95 V
MWR	-100.PA	100.PA	3.46 V	-3.48 V
MRD	-100.PA	100.PA	3.48 V	-3.47 V
DI0	-100.PA	100.PA	3.58 V	-3.51 V
DI1	-100.PA	100.PA	3.57 V	-3.51 V
DI2	0.00 A	100.PA	3.54 V	-3.49 V
DI3	-100.PA	100.PA	3.50 V	-3.48 V

	D00	D01	D02	D03
VOL1	95.0MV	95.0MV	100.MV	100.MV
VOL2	95.0MV	100.MV	105.MV	105.MV
VOH1	4.87 V	4.88 V	4.87 V	4.88 V
VOH2	9.84 V	9.84 V	9.82 V	9.84 V
IDN1	7.80MA	7.65MA	7.35MA	7.45MA
IDN2	20.3MA	19.3MA	17.7MA	18.1MA
IDP1	-3.01MA	-3.05MA	-3.03MA	-3.06MA
IDP2	-7.15MA	-7.25MA	-7.13MA	-7.32MA
IOZ1	6.20NA	-500.PA	4.90NA	-400.PA
IOZ2	4.40NA	-800.PA	4.90NA	-1.70NA
IOZ3	-600.PA	5.00NA	-1.60NA	4.90NA
IOZ4	2.80NA	1.80NA	1.20NA	2.20NA
IOZ5	2.00NA	1.30NA	2.50NA	300.PA
IOZ6	1.90NA	1.60NA	2.60NA	-100.PA
IOZ7	2.00NA	1.20NA	2.50NA	200.PA
IOZ8	1.90NA	1.40NA	2.60NA	-100.PA

ILDP	-10.0UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-5.00UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	280.N	235.N	105.N
DATA SETUP TIME	(TDS)	38.0N	30.0N	10.0N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	10.0N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	140.N	120.N	60.0N
ADDRESS HOLD TIME	(TAH)	-26.0N	-20.0N	-6.00N
WRITE PULSE WIDTH	(TWP)	104.N	92.0N	48.0N
CS1 SETUP TIME	(TCSS1)	1.00K	184.N	88.0N
CS2 SETUP TIME	(TCSS2)	214.N	180.N	86.0N
CS1 HOLD TIME	(TCSH1)	68.0N	60.0N	34.0N
CS2 HOLD TIME	(TCSH2)	70.0N	62.0N	32.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	1.00K	236.N	118.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	268.N	232.N	114.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	66.0N	58.0N	32.0N
OUTPUT HOLD FROM CS1	(TDOH1)	168.N	136.N	46.0N
OUTPUT HOLD FROM CS2	(TDOH2)	164.N	132.N	46.0N
OUTPUT HOLD FROM MRD	(TDOH3)	144.N	122.N	36.0N
OUTPUT HOLD FROM MWR	(TPDH)	142.N	120.N	38.0N
READ CYCLE TIME	(TRC)	304.N	256.N	128.N
WRITE CYCLE TIME	(TWC)	272.N	240.N	136.N

	IIL	IIH	VIC1	VIC2
A0	-45.3NA	44.8NA	3.42 V	-3.42 V
A1	-44.9NA	45.8NA	3.46 V	-3.46 V
A2	-43.2NA	44.4NA	3.50 V	-3.52 V
A3	-43.8NA	44.3NA	3.49 V	-3.51 V
A4	-43.2NA	43.0NA	3.46 V	-3.49 V
A5	-45.5NA	43.8NA	3.39 V	-3.43 V
A6	-44.4NA	38.4NA	3.45 V	-3.33 V
A7	-43.9NA	44.5NA	3.43 V	-3.44 V
CS1	-43.5NA	44.6NA	3.50 V	-3.47 V
CS2	-43.9NA	48.5NA	4.28 V	-4.30 V
MWR	-42.2NA	42.2NA	3.43 V	-3.45 V
MRD	-43.1NA	42.9NA	3.44 V	-3.44 V
DI0	-43.2NA	43.5NA	3.57 V	-3.50 V
DI1	-44.7NA	42.7NA	3.56 V	-3.50 V
DI2	-41.9NA	42.8NA	3.52 V	-3.48 V
DI3	-43.5NA	42.9NA	3.46 V	-3.45 V

	DO0	DO1	DO2	DO3
VOL1	130.MV	135.MV	145.MV	140.MV
VOL2	140.MV	145.MV	165.MV	160.MV
VOH1	4.78 V	4.79 V	4.78 V	4.79 V
VOH2	9.72 V	9.72 V	9.71 V	9.72 V
IDN1	5.65MA	5.50MA	5.20MA	5.30MA
IDN2	13.8MA	12.9MA	11.7MA	12.0MA
IDP1	-1.86MA	-1.88MA	-1.86MA	-1.87MA
IDP2	-4.39MA	-4.43MA	-4.30MA	-4.47MA
IOZ1	195.NA	188.NA	184.NA	188.NA
IOZ2	187.NA	194.NA	180.NA	185.NA
IOZ3	189.NA	189.NA	180.NA	188.NA
IOZ4	183.NA	196.NA	181.NA	182.NA
IOZ5	187.NA	195.NA	182.NA	188.NA
IOZ6	185.NA	189.NA	192.NA	176.NA
IOZ7	194.NA	186.NA	187.NA	187.NA
IOZ8	183.NA	197.NA	183.NA	183.NA

ILDP	-5.00UA
IL1	-30.0UA
IL2	-35.0UA
IL3	-25.0UA
IL4	-20.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	285.N	245.N	115.N
DATA SETUP TIME	(TDS)	36.0N	30.0N	10.0N
DATA HOLD TIME	(TDH)	12.0N	12.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	6.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	146.N	130.N	68.0N
ADDRESS HOLD TIME	(TAH)	-26.0N	-22.0N	-8.00N
WRITE PULSE WIDTH	(TWP)	108.N	94.0N	52.0N
CS1 SETUP TIME	(TCSS1)	218.N	190.N	96.0N
CS2 SETUP TIME	(TCSS2)	214.N	184.N	92.0N
CS1 HOLD TIME	(TCSH1)	68.0N	60.0N	34.0N
CS2 HOLD TIME	(TCSH2)	72.0N	62.0N	34.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	288.N	252.N	130.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	282.N	246.N	128.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	70.0N	62.0N	34.0N
OUTPUT HOLD FROM CS1	(TDOH1)	170.N	138.N	50.0N
OUTPUT HOLD FROM CS2	(TDOH2)	166.N	136.N	50.0N
OUTPUT HOLD FROM MRD	(TDOH3)	144.N	122.N	38.0N
OUTPUT HOLD FROM MWR	(TPDH)	146.N	122.N	40.0N
READ CYCLE TIME	(TRC)	304.N	264.N	136.N
WRITE CYCLE TIME	(TWC)	272.N	240.N	144.N

	IIL	IIH	VIC1	VIC2
A0	-263.NA	258.NA	3.47 V	-3.47 V
A1	-264.NA	261.NA	3.51 V	-3.51 V
A2	-256.NA	257.NA	3.56 V	-3.57 V
A3	-254.NA	253.NA	3.54 V	-3.56 V
A4	-252.NA	250.NA	3.51 V	-3.54 V
A5	-265.NA	256.NA	3.44 V	-3.48 V
A6	-261.NA	220.NA	3.50 V	-3.36 V
A7	-259.NA	257.NA	3.48 V	-3.50 V
CS1	-258.NA	253.NA	3.55 V	-3.52 V
CS2	-255.NA	262.NA	3.56 V	-3.59 V
MWR	-247.NA	244.NA	3.48 V	-3.51 V
MRD	-254.NA	250.NA	3.49 V	-3.50 V
DI0	-252.NA	254.NA	3.63 V	-3.56 V
DI1	-254.NA	250.NA	3.62 V	-3.55 V
DI2	-245.NA	249.NA	3.57 V	-3.53 V
DI3	-248.NA	248.NA	3.52 V	-3.51 V

	D00	D01	D02	D03
VOL1	145.MV	150.MV	160.MV	155.MV
VOL2	155.MV	165.MV	185.MV	180.MV
VOH1	4.76 V	4.76 V	4.76 V	4.76 V
VOH2	9.68 V	9.68 V	9.67 V	9.68 V
IDN1	5.10MA	4.95MA	4.70MA	4.75MA
IDN2	12.3MA	11.5MA	10.4MA	10.7MA
IDP1	-1.69MA	-1.70MA	-1.66MA	-1.71MA
IDP2	-3.94MA	-3.96MA	-3.84MA	-4.02MA
IOZ1	640.NA	652.NA	654.NA	633.NA
IOZ2	637.NA	643.NA	652.NA	633.NA
IOZ3	630.NA	642.NA	652.NA	630.NA
IOZ4	638.NA	639.NA	649.NA	635.NA
IOZ5	641.NA	647.NA	663.NA	642.NA
IOZ6	636.NA	651.NA	644.NA	644.NA
IOZ7	626.NA	650.NA	649.NA	629.NA
IOZ8	638.NA	641.NA	650.NA	635.NA
ILOP	65.0UA			
IL1	-135.UA			
IL2	-160.UA			
IL3	-120.UA			
IL4	-105.UA			

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN: 17

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	240.N	205.N	85.0N
DATA SETUP TIME	(TDS)	26.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	14.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	114.N	98.0N	48.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-16.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	86.0N	74.0N	40.0N
CS1 SETUP TIME	(TCSS1)	182.N	154.N	76.0N
CS2 SETUP TIME	(TCSS2)	176.N	150.N	74.0N
CS1 HOLD TIME	(TCSH1)	56.0N	50.0N	28.0N
CS2 HOLD TIME	(TCSH2)	60.0N	52.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	232.N	198.N	96.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	228.N	194.N	92.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	54.0N	46.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	148.N	118.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	166.N	118.N	36.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	34.0N
OUTPUT HOLD FROM MWR	(TPDH)	134.N	114.N	32.0N
READ CYCLE TIME	(TRC)	256.N	216.N	120.N
WRITE CYCLE TIME	(TWC)	256.N	216.N	120.N

	IIL	IIH	VIC1	VIC2
A0	-2.80NA	2.70NA	3.19 V	-3.18 V
A1	-2.70NA	2.70NA	3.23 V	-3.23 V
A2	-2.60NA	2.60NA	3.28 V	-3.28 V
A3	-2.60NA	2.80NA	3.27 V	-3.27 V
A4	-2.70NA	2.60NA	3.33 V	-3.35 V
A5	-2.50NA	2.60NA	3.18 V	-3.23 V
A6	-3.00NA	2.40NA	3.18 V	-3.20 V
A7	-2.80NA	2.50NA	3.19 V	-3.19 V
CS1	-2.70NA	2.50NA	3.27 V	-3.28 V
CS2	-2.70NA	2.60NA	3.30 V	-3.30 V
MWR	-2.50NA	2.50NA	3.27 V	-3.27 V
MRD	-2.60NA	2.50NA	3.27 V	-3.28 V
DI0	-2.80NA	2.60NA	3.34 V	-3.24 V
DI1	-2.50NA	2.60NA	3.28 V	-3.23 V
DI2	-2.70NA	2.60NA	3.32 V	-3.27 V
DI3	-2.90NA	2.60NA	3.30 V	-3.25 V

	DO0	DO1	DO2	DO3
VOL1	100.MV	105.MV	115.MV	115.MV
VOL2	105.MV	120.MV	135.MV	135.MV
VOH1	4.84 V	4.84 V	4.84 V	4.84 V
VOH2	9.78 V	9.78 V	9.77 V	9.78 V
IDN1	7.45MA	7.00MA	6.55MA	6.50MA
IDN2	17.5MA	15.9MA	14.1MA	14.2MA
IDP1	-2.49MA	-2.49MA	-2.44MA	-2.43MA
IDP2	-5.61MA	-5.58MA	-5.41MA	-5.53MA
IOZ1	33.3NA	24.7NA	30.7NA	24.4NA
IOZ2	31.2NA	24.4NA	31.0NA	23.4NA
IOZ3	25.5NA	30.6NA	24.7NA	30.4NA
IOZ4	28.3NA	27.7NA	26.9NA	28.2NA
IOZ5	29.2NA	26.4NA	30.0NA	24.8NA
IOZ6	29.9NA	26.1NA	29.9NA	24.8NA
IOZ7	29.9NA	25.9NA	30.0NA	24.1NA
IOZ8	30.0NA	25.3NA	30.0NA	24.2NA

ILDP	-5.00UA
IL1	-10.0UA
IL2	-20.0UA
IL3	-55.0UA
IL4	-50.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	245.N	200.N	80.0N
DATA SETUP TIME	(TDS)	28.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	22.0N	16.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	116.N	92.0N	42.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	78.0N	68.0N	38.0N
CS1 SETUP TIME	(TCSS1)	174.N	146.N	70.0N
CS2 SETUP TIME	(TCSS2)	172.N	144.N	68.0N
CS1 HOLD TIME	(TCSH1)	46.0N	40.0N	24.0N
CS2 HOLD TIME	(TCSH2)	46.0N	38.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	226.N	188.N	88.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	224.N	186.N	86.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	48.0N	42.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	140.N	110.N	32.0N
OUTPUT HOLD FROM CS2	(TDOH2)	142.N	110.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	110.N	30.0N
READ CYCLE TIME	(TRC)	240.N	208.N	120.N
WRITE CYCLE TIME	(TWC)	256.N	224.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-300.PA	300.PA	3.20 V	-3.19 V
A1	-300.PA	300.PA	3.24 V	-3.24 V
A2	-300.PA	300.PA	3.28 V	-3.29 V
A3	-300.PA	300.PA	3.28 V	-3.28 V
A4	-300.PA	300.PA	3.34 V	-3.35 V
A5	-300.PA	300.PA	3.19 V	-3.24 V
A6	-400.PA	300.PA	3.19 V	-3.21 V
A7	-300.PA	300.PA	3.21 V	-3.20 V
CS1	-300.PA	300.PA	3.28 V	-3.28 V
CS2	-300.PA	300.PA	3.97 V	-3.96 V
MWR	-300.PA	200.PA	3.28 V	-3.28 V
MRD	-300.PA	300.PA	3.28 V	-3.29 V
DI0	-300.PA	300.PA	3.31 V	-3.25 V
DI1	-200.PA	300.PA	3.29 V	-3.24 V
DI2	-300.PA	300.PA	3.33 V	-3.27 V
DI3	-400.PA	400.PA	3.31 V	-3.26 V

	D00	D01	D02	D03
VOL1	85.0MV	90.0MV	100.MV	100.MV
VOL2	95.0MV	105.MV	115.MV	115.MV
VOH1	4.87 V	4.87 V	4.87 V	4.87 V
VOH2	9.81 V	9.81 V	9.81 V	9.81 V
IDN1	8.50MA	8.00MA	7.50MA	7.40MA
IDN2	20.2MA	18.4MA	16.4MA	16.5MA
IDP1	-2.97MA	-2.94MA	-2.92MA	-2.92MA
IDP2	-6.64MA	-6.64MA	-6.44MA	-6.57MA
IOZ1	2.10NA	7.70NA	1.90NA	6.00NA
IOZ2	1.90NA	7.10NA	700.PA	7.40NA
IOZ3	7.60NA	700.PA	7.70NA	700.PA
IOZ4	5.00NA	2.80NA	5.40NA	1.90NA
IOZ5	3.10NA	5.80NA	1.80NA	6.80NA
IOZ6	2.90NA	6.30NA	1.20NA	6.90NA
IOZ7	2.00NA	6.60NA	1.00NA	7.40NA
IOZ8	2.00NA	7.10NA	800.PA	7.50NA

ILDP	-5.00UA
IL1	-5.00UA
IL2	-15.0UA
IL3	-55.0UA
IL4	-50.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	240.N	190.N	70.0N
DATA SETUP TIME	(TDS)	34.0N	24.0N	8.00N
DATA HOLD TIME	(TDH)	6.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	22.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	112.N	88.0N	38.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	80.0N	66.0N	36.0N
CS1 SETUP TIME	(TCSS1)	166.N	138.N	64.0N
CS2 SETUP TIME	(TCSS2)	166.N	138.N	62.0N
CS1 HOLD TIME	(TCSH1)	48.0N	38.0N	22.0N
CS2 HOLD TIME	(TCSH2)	46.0N	38.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	220.N	178.N	84.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	216.N	176.N	82.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	44.0N	38.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	134.N	104.N	28.0N
OUTPUT HOLD FROM CS2	(TDOH2)	134.N	104.N	30.0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	112.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	108.N	30.0N
READ CYCLE TIME	(TRC)	224.N	192.N	112.N
WRITE CYCLE TIME	(TWC)	264.N	192.N	104.N

	IIL	IIH	VIC1	VIC2
A0	0.00 A	100.PA	3.23 V	-3.22 V
A1	-100.PA	0.00 A	3.27 V	-3.27 V
A2	-100.PA	100.PA	3.31 V	-3.31 V
A3	-100.PA	100.PA	3.31 V	-3.30 V
A4	-100.PA	100.PA	3.37 V	-3.37 V
A5	-100.PA	100.PA	3.23 V	-3.27 V
A6	-100.PA	100.PA	3.22 V	-3.25 V
A7	-100.PA	100.PA	3.24 V	-3.24 V
CS1	0.00 A	100.PA	3.31 V	-3.31 V
CS2	0.00 A	100.PA	3.91 V	-3.91 V
MWR	-100.PA	100.PA	3.31 V	-3.30 V
MRD	-100.PA	100.PA	3.31 V	-3.32 V
DI0	-100.PA	100.PA	3.35 V	-3.28 V
DI1	0.00 A	100.PA	3.31 V	-3.27 V
DI2	0.00 A	100.PA	3.36 V	-3.30 V
DI3	-100.PA	100.PA	3.34 V	-3.28 V

	D00	D01	D02	D03
VOL1	80.0MV	85.0MV	90.0MV	90.0MV
VOL2	85.0MV	90.0MV	105.MV	100.MV
VOH1	4.88 V	4.89 V	4.88 V	4.89 V
VOH2	9.84 V	9.84 V	9.84 V	9.84 V
IDN1	9.35MA	8.85MA	8.30MA	8.20MA
IDN2	22.4MA	20.6MA	18.4MA	18.4MA
IDP1	-3.44MA	-3.46MA	-3.40MA	-3.39MA
IDP2	-7.68MA	-7.70MA	-7.47MA	-7.61MA
IOZ1	3.20NA	2.00NA	1.10NA	2.50NA
IOZ2	6.10NA	-1.30NA	4.80NA	-900.PA
IOZ3	-1.10NA	5.10NA	-1.10NA	4.40NA
IOZ4	-500.PA	3.90NA	-1.20NA	4.70NA
IOZ5	4.50NA	-1.30NA	5.00NA	-2.00NA
IOZ6	4.60NA	-1.50NA	4.60NA	-1.70NA
IOZ7	4.20NA	-1.10NA	4.60NA	-1.80NA
IOZ8	4.30NA	-1.20NA	4.40NA	-1.60NA

ILDP	-5.00UA
IL1	-5.00UA
IL2	-15.0UA
IL3	-55.0UA
IL4	-55.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	240.N	210.N	95.0N
DATA SETUP TIME	(TDS)	28.0N	24.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	122.N	108.N	56.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-16.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	100.N	86.0N	48.0N
CS1 SETUP TIME	(TCSS1)	192.N	166.N	86.0N
CS2 SETUP TIME	(TCSS2)	188.N	162.N	82.0N
CS1 HOLD TIME	(TCSH1)	66.0N	58.0N	34.0N
CS2 HOLD TIME	(TCSH2)	70.0N	60.0N	32.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	242.N	212.N	110.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	236.N	208.N	106.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	58.0N	52.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	154.N	124.N	38.0N
OUTPUT HOLD FROM CS2	(TDOH2)	152.N	122.N	40.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	36.0N
OUTPUT HOLD FROM MWR	(TPDH)	138.N	116.N	36.0N
READ CYCLE TIME	(TRC)	272.N	232.N	128.N
WRITE CYCLE TIME	(TWC)	256.N	224.N	136.N

	IIL	IIH	VIC1	VIC2
A0	-42.1NA	41.1NA	3.20 V	-3.19 V
A1	-42.0NA	41.3NA	3.24 V	-3.25 V
A2	-41.6NA	40.6NA	3.30 V	-3.30 V
A3	-41.0NA	41.5NA	3.29 V	-3.29 V
A4	-41.1NA	40.0NA	3.36 V	-3.37 V
A5	-41.4NA	41.0NA	3.20 V	-3.24 V
A6	-42.7NA	39.5NA	3.19 V	-3.22 V
A7	-42.1NA	41.0NA	3.21 V	-3.21 V
CS1	-41.0NA	39.9NA	3.29 V	-3.29 V
CS2	-41.2NA	42.1NA	3.31 V	-3.33 V
MWR	-40.0NA	39.4NA	3.29 V	-3.28 V
MRD	-41.1NA	39.5NA	3.29 V	-3.30 V
DI0	-40.6NA	40.7NA	3.32 V	-3.26 V
DI1	-39.9NA	41.1NA	3.29 V	-3.25 V
DI2	-41.6NA	40.8NA	3.34 V	-3.28 V
DI3	-40.7NA	40.6NA	3.32 V	-3.27 V

	D00	D01	D02	D03
VOL1	115.MV	125.MV	135.MV	135.MV
VOL2	130.MV	140.MV	160.MV	160.MV
VOH1	4.82 V	4.81 V	4.80 V	4.80 V
VOH2	9.73 V	9.73 V	9.72 V	9.73 V
IDN1	6.35MA	6.00MA	5.55MA	5.55MA
IDN2	14.8MA	13.5MA	11.9MA	12.1MA
IDP1	-2.10MA	-2.08MA	-2.03MA	-2.06MA
IDP2	-4.70MA	-4.68MA	-4.53MA	-4.65MA
IOZ1	271.NA	273.NA	262.NA	250.NA
IOZ2	268.NA	266.NA	266.NA	244.NA
IOZ3	266.NA	268.NA	263.NA	246.NA
IOZ4	270.NA	262.NA	269.NA	244.NA
IOZ5	269.NA	268.NA	271.NA	250.NA
IOZ6	283.NA	264.NA	267.NA	255.NA
IOZ7	271.NA	274.NA	260.NA	254.NA
IOZ8	273.NA	264.NA	273.NA	246.NA

ILDP	1.80UA
IL1	-35.0UA
IL2	-50.0UA
IL3	-75.0UA
IL4	-70.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	255.N	225.N	110.N
DATA SETUP TIME	(TDS)	28.0N	24.0N	10.0N
DATA HOLD TIME	(TDH)	14.0N	14.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	6.00N	4.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	132.N	118.N	64.0N
ADDRESS HOLD TIME	(TAH)	-20.0N	-18.0N	-6.00N
WRITE PULSE WIDTH	(TWP)	104.N	92.0N	52.0N
CS1 SETUP TIME	(TCSS1)	206.N	180.N	94.0N
CS2 SETUP TIME	(TCSS2)	202.N	174.N	90.0N
CS1 HOLD TIME	(TCSH1)	68.0N	62.0N	34.0N
CS2 HOLD TIME	(TCSH2)	72.0N	62.0N	34.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	258.N	230.N	122.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	254.N	224.N	118.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	62.0N	56.0N	34.0N
OUTPUT HOLD FROM CS1	(TDOH1)	160.N	128.N	44.0N
OUTPUT HOLD FROM CS2	(TDOH2)	156.N	126.N	44.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	122.N	38.0N
OUTPUT HOLD FROM MWR	(TPDH)	142.N	118.N	40.0N
READ CYCLE TIME	(TRC)	280.N	248.N	128.N
WRITE CYCLE TIME	(TWC)	264.N	240.N	144.N

	IIL	IIH	VIC1	VICP
A0	-243.NA	234.NA	3.24 V	-3.23 V
A1	-244.NA	236.NA	3.29 V	-3.29 V
A2	-239.NA	232.NA	3.35 V	-3.35 V
A3	-236.NA	233.NA	3.33 V	-3.34 V
A4	-237.NA	227.NA	3.40 V	-3.41 V
A5	-241.NA	234.NA	3.23 V	-3.29 V
A6	-242.NA	227.NA	3.23 V	-3.26 V
A7	-241.NA	233.NA	3.25 V	-3.25 V
CS1	-238.NA	226.NA	3.34 V	-3.34 V
CS2	-236.NA	234.NA	3.37 V	-3.38 V
MWR	-231.NA	223.NA	3.34 V	-3.34 V
MRD	-233.NA	225.NA	3.34 V	-3.35 V
DI0	-232.NA	231.NA	3.37 V	-3.30 V
DI1	-229.NA	231.NA	3.34 V	-3.29 V
DI2	-234.NA	232.NA	3.38 V	-3.33 V
DI3	-232.NA	228.NA	3.37 V	-3.31 V

	D00	D01	D02	D03
VOL1	130.MV	140.MV	155.MV	150.MV
VOL2	145.MV	160.MV	180.MV	180.MV
VOH1	4.79 V	4.78 V	4.78 V	4.78 V
VOH2	9.70 V	9.69 V	9.69 V	9.69 V
IDN1	5.65MA	5.35MA	4.95MA	4.95MA
IDN2	13.1MA	11.9MA	10.6MA	10.7MA
IDP1	-1.88MA	-1.86MA	-1.82MA	-1.84MA
IDP2	-4.20MA	-4.18MA	-4.03MA	-4.16MA
IOZ1	1.09UA	1.06UA	1.03UA	995.NA
IOZ2	1.09UA	1.05UA	1.04UA	990.NA
IOZ3	1.08UA	1.06UA	1.03UA	984.NA
IOZ4	1.07UA	1.06UA	1.03UA	992.NA
IOZ5	1.10UA	1.06UA	1.07UA	995.NA
IOZ6	1.09UA	1.06UA	1.04UA	989.NA
IOZ7	1.08UA	1.05UA	1.04UA	988.NA
IOZ8	1.08UA	1.06UA	1.04UA	987.NA

ILDP	70.0UA
IL1	-130.UA
IL2	-160.UA
IL3	-170.UA
IL4	-150.UA

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN: 1A

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
FAILED GALPAT (TIGHT LIMITS) VCC=5V ADD = 56 DIAG = 9 PIN: 010

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	450.N	330.N	105.N
DATA SETUP TIME	(TDS)	20.0N	10.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	242.N	184.N	54.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	70.0N	60.0N	36.0N
CS1 SETUP TIME	(TCSS1)	372.N	1.00K	418.N
CS2 SETUP TIME	(TCSS2)	294.N	142.N	68.0N
CS1 HOLD TIME	(TCSH1)	38.0N	32.0N	24.0N
CS2 HOLD TIME	(TCSH2)	40.0N	34.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	414.N	318.N	114.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	410.N	314.N	112.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	54.0N	48.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	154.N	122.N	36.0N
OUTPUT HOLD FROM CS2	(TDOH2)	150.N	118.N	36.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	120.N	34.0N
OUTPUT HOLD FROM MWR	(TPOH)	140.N	114.N	32.0N
READ CYCLE TIME	(TRC)	392.N	312.N	120.N
WRITE CYCLE TIME	(TWC)	208.N	184.N	112.N

	IIL	IIH	VIC1	VTC2
A0	-2.20NA	2.20NA	2.94 V	-2.93 V
A1	-1.80NA	2.10NA	2.97 V	-3.00 V
A2	-2.00NA	2.30NA	3.01 V	-3.01 V
A3	-1.90NA	2.40NA	3.01 V	-3.03 V
A4	-1.80NA	2.00NA	3.01 V	-3.02 V
A5	-2.10NA	2.00NA	2.93 V	-2.98 V
A6	-2.00NA	2.30NA	2.90 V	-2.96 V
A7	-2.50NA	2.60NA	2.94 V	-2.97 V
CS1	-2.00NA	2.70NA	2.99 V	-2.98 V
CS2	-2.30NA	2.40NA	3.02 V	-3.04 V
MWR	-2.00NA	2.10NA	2.93 V	-2.96 V
MRD	-2.10NA	2.60NA	2.95 V	-2.95 V
DI0	-2.50NA	2.50NA	3.09 V	-3.04 V
DI1	-2.40NA	2.80NA	3.07 V	-3.02 V
DI2	-2.60NA	2.90NA	3.07 V	-3.03 V
DI3	-2.70NA	2.60NA	3.05 V	-3.03 V

	DO0	DO1	DO2	DO3
VOL1	115.MV	115.MV	125.MV	125.MV
VOL2	110.MV	120.MV	35.MV	130.MV
VOH1	4.86 V	4.85 V	4.85 V	4.86 V
VOH2	9.79 V	9.78 V	9.78 V	9.79 V
IDN1	6.35MA	6.15MA	5.85MA	5.90MA
IDN2	16.8MA	15.7MA	14.1MA	14.5MA
IDP1	-2.64MA	-2.62MA	-2.59MA	-2.64MA
IDP2	-5.82MA	-5.82MA	-5.68MA	-5.88MA
IOZ1	28.5NA	27.0NA	26.0NA	34.5NA
IOZ2	30.2NA	23.6NA	27.7NA	31.8NA
IOZ3	31.2NA	21.4NA	30.3NA	27.5NA
IOZ4	28.3NA	24.7NA	27.4NA	30.5NA
IOZ5	31.8NA	21.9NA	29.0NA	30.3NA
IOZ6	31.5NA	22.3NA	28.7NA	30.7NA
IOZ7	31.1NA	22.3NA	28.2NA	30.7NA
IOZ8	30.4NA	22.8NA	27.9NA	30.8NA

ILDP	2.00UA
IL1	-200.UA
IL2	-200.UA
IL3	-20.0UA
IL4	-15.0UA

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: -20 C SN: 1A

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
FAILED G PAT (TIGHT LIMITS) VCC=5V ADD = 8 DIAG = 9 PIN: 010

FAILED DATA 'ENTION TEST ADD = 97 DIAG = 17 PIN: 010

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	535.N	370.N	100.N
DATA SETUP TIME	(TDS)	22.0N	18.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	42.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	278.N	194.N	50.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	68.0N	58.0N	36.0N
CS1 SETUP TIME	(TCSS1)	402.N	206.N	66.0N
CS2 SETUP TIME	(TCSS2)	366.N	200.N	62.0N
CS1 HOLD TIME	(TCSH1)	38.0N	34.0N	22.0N
CS2 HOLD TIME	(TCSH2)	40.0N	34.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	1.00K	342.N	110.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	1.00K	338.N	106.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	44.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	146.N	114.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	144.N	112.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	116.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	1.00K	114.N	32.0N
READ CYCLE TIME	(TRC)	400.N	312.N	112.N
WRITE CYCLE TIME	(TWC)	208.N	176.N	104.N

	IIL	IIH	VIC1	VIC2
A0	-400.PA	300.PA	3.05 V	-3.03 V
A1	-300.PA	300.PA	3.08 V	-3.10 V
A2	-400.PA	400.PA	3.12 V	-3.11 V
A3	-300.PA	400.PA	3.12 V	-3.13 V
A4	-300.PA	200.PA	3.12 V	-3.12 V
A5	-400.PA	300.PA	3.03 V	-3.08 V
A6	-300.PA	300.PA	3.00 V	-3.07 V
A7	-500.PA	400.PA	3.04 V	-3.07 V
CS1	-300.PA	400.PA	3.10 V	-3.09 V
CS2	-400.PA	400.PA	3.12 V	-3.13 V
MWR	-300.PA	300.PA	3.03 V	-3.06 V
MRD	-300.PA	500.PA	3.06 V	-3.05 V
DI0	-400.PA	400.PA	3.18 V	-3.13 V
DI1	-400.PA	400.PA	3.17 V	-3.12 V
DI2	-500.PA	500.PA	3.16 V	-3.13 V
DI3	-400.PA	400.PA	3.15 V	-3.13 V

	D00	D01	D02	D03
VOL1	105.MV	105.MV	110.MV	110.MV
VOL2	95.0MV	105.MV	115.MV	115.MV
VOH1	4.88 V	4.88 V	4.88 V	4.88 V
VOH2	9.82 V	9.82 V	9.82 V	9.82 V
IDN1	7.10MA	6.90MA	6.55MA	6.65MA
IDN2	19.3MA	18.1MA	16.3MA	16.7MA
IDP1	-3.09MA	-3.08MA	-3.06MA	-3.10MA
IDP2	-6.86MA	-6.86MA	-6.77MA	-6.94MA
IOZ1	7.80NA	3.30NA	5.90NA	4.70NA
IOZ2	9.20NA	1.30NA	8.70NA	1.90NA
IOZ3	2.20NA	8.30NA	1.50NA	8.20NA
IOZ4	4.00NA	6.40NA	1.80NA	7.50NA
IOZ5	7.80NA	1.50NA	7.60NA	1.80NA
IOZ6	7.80NA	1.50NA	7.90NA	1.30NA
IOZ7	8.00NA	1.20NA	7.70NA	1.70NA
IOZ8	8.10NA	1.40NA	8.00NA	1.60NA

ILDP	-5.00UA
IL1	-205.UA
IL2	-200.UA
IL3	-10.0UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
FAILED GALPAT (TIGHT LIMITS) VCC=5V ADD = 6 DIAG = 9 PIN: 010

FAILED DATA RETENTION TEST ADD = 97 DIAG = 17 PIN: 010

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	1.00K	400.N	95.0N
DATA SETUP TIME	(TDS)	26.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	112.N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	1.00K	214.N	48.0N
ADDRESS HOLD TIME	(TAH)	1.00K	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	68.0N	60.0N	32.0N
CS1 SETUP TIME	(TCSS1)	484.N	230.N	62.0N
CS2 SETUP TIME	(TCSS2)	480.N	228.N	60.0N
CS1 HOLD TIME	(TCSH1)	1.00K	34.0N	22.0N
CS2 HOLD TIME	(TCSH2)	1.00K	36.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	1.00K	364.N	104.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	1.00K	362.N	102.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	48.0N	40.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	1.00K	110.N	32.0N
OUTPUT HOLD FROM CS2	(TDOH2)	1.00K	108.N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	1.00K	116.N	30.0N
OUTPUT HOLD FROM MWR	(TPOH)	1.00K	112.N	30.0N
READ CYCLE TIME	(TRC)	432.N	328.N	104.N
WRITE CYCLE TIME	(TWC)	224.N	176.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-100.PA	100.PA	3.14 V	-3.13 V
A1	-100.PA	100.PA	3.17 V	-3.19 V
A2	-100.PA	100.PA	3.21 V	-3.20 V
A3	-100.PA	100.PA	3.21 V	-3.22 V
A4	-100.PA	100.PA	3.20 V	-3.21 V
A5	-100.PA	100.PA	3.12 V	-3.17 V
A6	-100.PA	100.PA	3.10 V	-3.16 V
A7	-100.PA	100.PA	3.13 V	-3.16 V
CS1	-100.PA	100.PA	3.19 V	-3.17 V
CS2	-100.PA	100.PA	3.21 V	-3.22 V
MWR	-100.PA	100.PA	3.13 V	-3.16 V
MRD	-100.PA	100.PA	3.16 V	-3.14 V
DI0	-100.PA	100.PA	3.28 V	-3.22 V
DI1	-100.PA	100.PA	3.26 V	-3.20 V
DI2	-100.PA	100.PA	3.25 V	-3.21 V
DI3	-100.PA	100.PA	3.24 V	-3.21 V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

	D00	D01	D02	D03
VOL1	95.0MV	95.0MV	100.MV	100.MV
VOL2	85.0MV	95.0MV	105.MV	100.MV
VOH1	4.89 V	4.89 V	4.89 V	4.89 V
VOH2	9.84 V	9.84 V	9.84 V	9.85 V
IDN1	7.75MA	7.50MA	7.15MA	7.20MA
IDN2	21.3MA	20.0MA	18.2MA	18.6MA
IDP1	-3.51MA	-3.53MA	-3.53MA	-3.56MA
IDP2	-7.87MA	-7.91MA	-7.74MA	-8.01MA
IOZ1	3.60NA	800.PA	3.50NA	-100.PA
IOZ2	-300.PA	4.50NA	-400.PA	3.90NA
IOZ3	5.20NA	-400.PA	4.00NA	300.PA
IOZ4	5.20NA	-1.30NA	5.20NA	-1.60NA
IOZ5	-800.PA	5.20NA	-1.60NA	5.50NA
IOZ6	-800.PA	5.00NA	-1.50NA	5.60NA
IOZ7	-500.PA	5.00NA	-1.60NA	5.30NA
IOZ8	-500.PA	4.80NA	-1.40NA	5.30NA

ILDP	1.20UA
IL1	-215.UA
IL2	-210.UA
IL3	-5.00UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
FAILED GALPAT (TIGHT LIMITS) VCC=5V ADD = 24 DIAG = 121 PTN: 010

FAILED DATA RETENTION TEST ADD = 97 DIAG = 17 PIN: 010

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	405.N	310.N	145.N
DATA SETUP TIME	(TDS)	20.0N	18.0N	8.00N
DATA HOLD TIME	(TDH)	14.0N	14.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	4.00N	4.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	226.N	178.N	58.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-10.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	78.0N	70.0N	42.0N
CS1 SETUP TIME	(TCSS1)	230.N	146.N	78.0N
CS2 SETUP TIME	(TCSS2)	226.N	142.N	76.0N
CS1 HOLD TIME	(TCSH1)	48.0N	44.0N	28.0N
CS2 HOLD TIME	(TCSH2)	52.0N	46.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	384.N	306.N	154.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	380.N	304.N	152.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	58.0N	50.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	156.N	124.N	38.0N
OUTPUT HOLD FROM CS2	(TDOH2)	154.N	122.N	38.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	122.N	36.0N
OUTPUT HOLD FROM MWR	(TPDH)	142.N	116.N	1.00K
READ CYCLE TIME	(TRC)	400.N	320.N	168.N
WRITE CYCLE TIME	(TWC)	216.N	200.N	128.N

	IIL	IIH	VIC1	VIC2
A0	-26.1NA	27.2NA	2.89 V	-2.87 V
A1	-24.3NA	26.0NA	2.91 V	-2.93 V
A2	-25.5NA	27.8NA	2.95 V	-2.95 V
A3	-24.7NA	26.9NA	2.95 V	-2.98 V
A4	-24.5NA	25.9NA	2.95 V	-2.96 V
A5	-25.7NA	26.6NA	2.87 V	-2.91 V
A6	-25.0NA	27.2NA	2.84 V	-2.91 V
A7	-26.8NA	28.9NA	2.88 V	-2.91 V
CS1	-26.0NA	28.4NA	2.93 V	-2.93 V
CS2	-26.1NA	28.0NA	2.95 V	-2.97 V
MWR	-25.0NA	26.8NA	2.86 V	-2.91 V
MRD	-26.4NA	28.1NA	2.89 V	-2.89 V
DI0	-27.4NA	28.7NA	3.03 V	-2.98 V
DI1	-27.5NA	29.8NA	3.01 V	-2.96 V
DI2	-27.5NA	29.1NA	3.01 V	-2.97 V
DI3	-27.5NA	28.0NA	3.00 V	-2.97 V

	D00	D01	D02	D03
VOL1	130.MV	135.MV	145.MV	145.MV
VOL2	130.MV	140.MV	160.MV	155.MV
VOH1	4.82 V	4.82 V	4.82 V	4.82 V
VOH2	9.74 V	9.75 V	9.74 V	9.74 V
IDN1	5.55MA	5.35MA	5.10MA	5.15MA
IDN2	14.3MA	13.3MA	11.9MA	12.3MA
IDP1	-2.23MA	-2.21MA	-2.21MA	-2.23MA
IDP2	-4.92MA	-4.91MA	-4.82MA	-4.97MA
IOZ1	223.NA	128.NA	206.NA	209.NA
IOZ2	218.NA	122.NA	198.NA	211.NA
IOZ3	210.NA	117.NA	198.NA	205.NA
IOZ4	210.NA	121.NA	190.NA	212.NA
IOZ5	211.NA	119.NA	196.NA	211.NA
IOZ6	205.NA	131.NA	190.NA	211.NA
IOZ7	203.NA	119.NA	201.NA	203.NA
IOZ8	208.NA	119.NA	193.NA	215.NA

ILDP	15.0UA
IL1	-220.UA
IL2	-230.UA
IL3	-55.0UA
IL4	-45.0UA

FAILED GALPAT (WIDE LIMITS) VCC=10V ADD = 82 DIAG = 64 PIN: 010
FAILED GALPAT (TIGHT LIMITS) VCC=10V ADD = 83 DIAG = 64 PIN: 010
FAILED GALPAT (TIGHT LIMITS) VCC=5V ADD = 8 DIAG = 121 PIN: 010

FAILED DATA RETENTION TEST ADD = 97 DIAG = 17 PIN: 010

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	420.N	325.N	1.00K
DATA SETUP TIME	(TDS)	20.0N	18.0N	1.00K
DATA HOLD TIME	(TDH)	16.0N	16.0N	1.00K
ADDRESS SETUP TIME	(TAS1)	2.00N	2.00N	1.00K
ADDRESS SETUP TIME	(TAS2)	234.N	182.N	64.0N
ADDRESS HOLD TIME	(TAH)	-12.0N	-10.0N	1.00K
WRITE PULSE WIDTH	(TWP)	84.0N	76.0N	1.00K
CS1 SETUP TIME	(TCSS1)	246.N	158.N	1.00K
CS2 SETUP TIME	(TCSS2)	244.N	154.N	1.00K
CS1 HOLD TIME	(TCSH1)	50.0N	46.0N	1.00K
CS2 HOLD TIME	(TCSH2)	54.0N	48.0N	1.00K
OUTPUT ACTIVE FROM CS1	(TDOA1)	408.N	328.N	1.00K
OUTPUT ACTIVE FROM CS2	(TDOA2)	406.N	324.N	1.00K
OUTPUT ACTIVE FROM MRD	(TDOA3)	62.0N	54.0N	1.00K
OUTPUT HOLD FROM CS1	(TDOH1)	162.N	130.N	1.00K
OUTPUT HOLD FROM CS2	(TDOH2)	156.N	126.N	1.00K
OUTPUT HOLD FROM MRD	(TDOH3)	144.N	122.N	1.00K
OUTPUT HOLD FROM MWR	(TPOH)	144.N	120.N	1.00K
READ CYCLE TIME	(TRC)	432.N	336.N	1.00K
WRITE CYCLE TIME	(TWC)	216.N	216.N	1.00K

	IIL	IIH	VIC1	VIC2
A0	-148.NA	146.NA	2.84 V	-2.83 V
A1	-143.NA	142.NA	2.87 V	-2.89 V
A2	-147.NA	148.NA	2.91 V	-2.92 V
A3	-145.NA	145.NA	2.91 V	-2.94 V
A4	-141.NA	140.NA	2.91 V	-2.93 V
A5	-146.NA	142.NA	2.83 V	-2.88 V
A6	-147.NA	142.NA	2.79 V	-2.87 V
A7	-148.NA	143.NA	2.84 V	-2.87 V
CS1	-151.NA	144.NA	2.89 V	-2.89 V
CS2	-145.NA	146.NA	2.92 V	-2.94 V
MWR	-141.NA	143.NA	2.81 V	-2.87 V
MRD	-144.NA	145.NA	2.84 V	-2.86 V
DI0	-142.NA	142.NA	2.99 V	-2.94 V
DI1	-143.NA	143.NA	2.97 V	-2.93 V
DI2	-142.NA	139.NA	2.97 V	-2.94 V
DI3	-141.NA	139.NA	2.96 V	-2.93 V

	D00	D01	D02	D03
VOL1	145.MV	155.MV	160.MV	160.MV
VOL2	150.MV	160.MV	180.MV	175.MV
VOH1	4.80 V	4.80 V	4.80 V	4.80 V
VOH2	9.72 V	9.72 V	9.70 V	9.72 V
IDN1	5.00MA	4.85MA	4.55MA	4.65MA
IDN2	12.7MA	11.9MA	10.6MA	11.0MA
IDP1	-2.02MA	-2.00MA	-1.99MA	-2.02MA
IDP2	-4.43MA	-4.40MA	-4.33MA	-4.47MA
IOZ1	680.NA	294.NA	594.NA	667.NA
IOZ2	647.NA	281.NA	578.NA	673.NA
IOZ3	641.NA	270.NA	580.NA	667.NA
IOZ4	631.NA	272.NA	572.NA	667.NA
IOZ5	644.NA	279.NA	595.NA	679.NA
IOZ6	636.NA	287.NA	585.NA	675.NA
IOZ7	632.NA	275.NA	598.NA	671.NA
IOZ8	636.NA	275.NA	583.NA	675.NA

ILDP	75.0UA
IL1	-330.UA
IL2	-370.UA
IL3	-180.UA
IL4	-145.UA

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN: 19

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
FAILED GALPAT (TIGHT LIMITS) VCC=5V ADD = 200 DIAG = 57 PIN: 010

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	410.N	315.N	105.N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	14.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	234.N	182.N	58.0N
ADDRESS HOLD TIME	(TAH)	-20.0N	-16.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	76.0N	64.0N	38.0N
CS1 SETUP TIME	(TCSS1)	252.N	154.N	76.0N
CS2 SETUP TIME	(TCSS2)	248.N	150.N	72.0N
CS1 HOLD TIME	(TCSH1)	36.0N	32.0N	22.0N
CS2 HOLD TIME	(TCSH2)	40.0N	36.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	386.N	304.N	112.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	384.N	302.N	110.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	56.0N	50.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	160.N	126.N	38.0N
OUTPUT HOLD FROM CS2	(TDOH2)	156.N	124.N	38.0N
OUTPUT HOLD FROM MRD	(TDOH3)	144.N	122.N	34.0N
OUTPUT HOLD FROM MWR	(TPDH)	142.N	116.N	34.0N
READ CYCLE TIME	(TRC)	360.N	288.N	128.N
WRITE CYCLE TIME	(TWC)	248.N	256.N	120.N

	IIL	IIH	VIC1	VIC2
A0	-1.70NA	1.80NA	3.13 V	-3.11 V
A1	-1.40NA	1.80NA	3.14 V	-3.14 V
A2	-1.50NA	1.40NA	3.16 V	-3.18 V
A3	-1.80NA	2.00NA	3.14 V	-3.17 V
A4	-1.40NA	1.90NA	3.16 V	-3.15 V
A5	-1.80NA	1.70NA	3.12 V	-3.11 V
A6	-1.90NA	1.70NA	3.12 V	-3.11 V
A7	-1.80NA	1.30NA	3.13 V	-3.14 V
CS1	-2.20NA	1.70NA	3.13 V	-3.12 V
CS2	-2.10NA	1.70NA	3.16 V	-3.15 V
MWR	-2.30NA	1.70NA	3.12 V	-3.13 V
MRD	-1.50NA	1.60NA	3.13 V	-3.12 V
DI0	-1.90NA	1.80NA	3.17 V	-3.16 V
DI1	-2.00NA	1.50NA	3.16 V	-3.09 V
DI2	-2.00NA	2.00NA	3.16 V	-3.15 V
DI3	-1.80NA	1.90NA	3.15 V	-3.12 V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

	D00	D01	D02	D03
VOL1	125.MV	125.MV	135.MV	130.MV
VOL2	120.MV	130.MV	145.MV	140.MV
VOH1	4.84 V	4.84 V	4.84 V	4.84 V
VOH2	9.77 V	9.78 V	9.77 V	9.78 V
IDN1	6.00MA	5.90MA	5.60MA	5.65MA
IDN2	15.4MA	14.6MA	13.2MA	13.6MA
IDP1	-2.40MA	-2.41MA	-2.39MA	-2.42MA
IDP2	-5.45MA	-5.52MA	-5.39MA	-5.58MA
IOZ1	20.8NA	16.4NA	22.3NA	15.6NA
IOZ2	16.7NA	18.9NA	18.7NA	18.3NA
IOZ3	18.9NA	17.7NA	18.6NA	19.1NA
IOZ4	22.0NA	14.9NA	22.4NA	16.3NA
IOZ5	15.2NA	21.0NA	17.3NA	21.5NA
IOZ6	15.4NA	21.6NA	17.0NA	20.7NA
IOZ7	15.6NA	21.0NA	16.9NA	20.8NA
IOZ8	15.1NA	21.1NA	17.1NA	20.3NA

ILDP	-5.00UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-35.0UA
IL4	-20.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
FAILED GALPAT (TIGHT LIMITS) VCC=5V ADD = 8 DIAG = 57 PIN: 010

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	455.N	335.N	95.0N
DATA SETUP TIME	(TDS)	28.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	18.0N	14.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	250.N	182.N	56.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-16.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	78.0N	70.0N	36.0N
CS1 SETUP TIME	(TCSS1)	294.N	164.N	70.0N
CS2 SETUP TIME	(TCSS2)	290.N	148.N	68.0N
CS1 HOLD TIME	(TCSH1)	36.0N	32.0N	22.0N
CS2 HOLD TIME	(TCSH2)	40.0N	34.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	414.N	312.N	104.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	412.N	312.N	102.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	52.0N	46.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	152.N	118.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	148.N	116.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	118.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	140.N	114.N	32.0N
READ CYCLE TIME	(TRC)	352.N	272.N	120.N
WRITE CYCLE TIME	(TWC)	272.N	200.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-200.PA	300.PA	3.22 V	-3.20 V
A1	-300.PA	300.PA	3.24 V	-3.24 V
A2	-300.PA	300.PA	3.25 V	-3.28 V
A3	-400.PA	400.PA	3.24 V	-3.26 V
A4	-300.PA	300.PA	3.26 V	-3.25 V
A5	-400.PA	300.PA	3.21 V	-3.20 V
A6	-500.PA	400.PA	3.21 V	-3.20 V
A7	-400.PA	200.PA	3.22 V	-3.23 V
CS1	-500.PA	300.PA	3.22 V	-3.21 V
CS2	-500.PA	300.PA	3.26 V	-3.24 V
MWR	-500.PA	300.PA	3.22 V	-3.22 V
MRD	-300.PA	300.PA	3.22 V	-3.21 V
DI0	-400.PA	300.PA	3.27 V	-3.25 V
DI1	-600.PA	300.PA	3.26 V	-3.18 V
DI2	-400.PA	700.PA	3.26 V	-3.24 V
DI3	-400.PA	400.PA	3.25 V	-3.21 V

	D00	D01	D02	D03
VOL1	110.MV	115.MV	120.MV	115.MV
VOL2	105.MV	115.MV	125.MV	120.MV
VOH1	4.86 V	4.86 V	4.86 V	4.86 V
VOH2	9.81 V	9.81 V	9.80 V	9.81 V
IDN1	6.65MA	6.50MA	6.20MA	6.25MA
IDN2	17.5MA	16.7MA	15.2MA	15.5MA
IDP1	-2.83MA	-2.85MA	-2.84MA	-2.86MA
IDP2	-6.41MA	-6.52MA	-6.37MA	-6.58MA
IOZ1	4.30NA	3.50NA	4.30NA	2.30NA
IOZ2	1.00NA	7.00NA	700.PA	5.90NA
IOZ3	7.80NA	500.PA	6.10NA	1.20NA
IOZ4	6.30NA	400.PA	6.30NA	300.PA
IOZ5	1.00NA	6.40NA	200.PA	7.20NA
IOZ6	1.40NA	6.20NA	-100.PA	6.70NA
IOZ7	1.30NA	5.80NA	600.PA	6.70NA
IOZ8	1.90NA	5.60NA	500.PA	6.40NA

ILDP	-5.00UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-25.0UA
IL4	-15.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
FAILED GALPAT (TIGHT LIMITS) VCC=5V ADD = 8 DIAG = 57 PIN: 010

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	505.N	350.N	90.0N
DATA SETUP TIME	(TDS)	32.0N	26.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	284.N	196.N	52.0N
ADDRESS HOLD TIME	(TAH)	-20.0N	-16.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	84.0N	70.0N	34.0N
CS1 SETUP TIME	(TCSS1)	334.N	176.N	66.0N
CS2 SETUP TIME	(TCSS2)	334.N	176.N	62.0N
CS1 HOLD TIME	(TCSH1)	44.0N	38.0N	22.0N
CS2 HOLD TIME	(TCSH2)	46.0N	38.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	1.00K	328.N	100.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	1.00K	326.N	98.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	42.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	146.N	112.N	32.0N
OUTPUT HOLD FROM CS2	(TDOH2)	142.N	110.N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	140.N	114.N	30.0N
READ CYCLE TIME	(TRC)	360.N	272.N	112.N
WRITE CYCLE TIME	(TWC)	248.N	192.N	104.N

	IIL	IIH	VIC1	VICP
A0	-100.PA	100.PA	3.32 V	-3.29 V
A1	-100.PA	100.PA	3.34 V	-3.34 V
A2	-100.PA	100.PA	3.35 V	-3.38 V
A3	-100.PA	100.PA	3.34 V	-3.36 V
A4	-100.PA	100.PA	3.36 V	-3.35 V
A5	-100.PA	100.PA	3.31 V	-3.29 V
A6	-100.PA	100.PA	3.30 V	-3.30 V
A7	-100.PA	100.PA	3.31 V	-3.34 V
CS1	-100.PA	100.PA	3.32 V	-3.30 V
CS2	-100.PA	100.PA	3.36 V	-3.34 V
MWR	-100.PA	100.PA	3.32 V	-3.32 V
MRD	-100.PA	100.PA	3.34 V	-3.30 V
DI0	-100.PA	100.PA	3.38 V	-3.35 V
DI1	-200.PA	100.PA	3.36 V	-3.28 V
DI2	-100.PA	300.PA	3.36 V	-3.34 V
DI3	-100.PA	100.PA	3.36 V	-3.30 V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

	D00	D01	D02	D03
VOL1	105.MV	105.MV	110.MV	110.MV
VOL2	100.MV	100.MV	115.MV	110.MV
VOH1	4.88 V	4.88 V	4.88 V	4.88 V
VOH2	9.83 V	9.84 V	9.84 V	9.84 V
IDN1	7.15MA	7.05MA	6.70MA	6.75MA
IDN2	19.3MA	18.3MA	16.8MA	17.2MA
IDP1	-3.21MA	-3.29MA	-3.26MA	-3.29MA
IDP2	-7.38MA	-7.52MA	-7.31MA	-7.54MA
IOZ1	4.40NA	-500.PA	4.00NA	-900.PA
IOZ2	-100.PA	3.20NA	-100.PA	2.90NA
IOZ3	4.00NA	-100.PA	3.00NA	800.PA
IOZ4	5.30NA	-1.90NA	5.40NA	-1.80NA
IOZ5	-1.30NA	5.40NA	-2.00NA	5.50NA
IOZ6	-1.30NA	5.00NA	-1.90NA	5.60NA
IOZ7	-1.10NA	5.00NA	-2.00NA	5.30NA
IOZ8	-1.10NA	4.60NA	-1.80NA	5.30NA

ILDP	-5.00UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-25.0UA
IL4	-15.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	375.N	300.N	115.N
DATA SETUP TIME	(TDS)	24.0N	22.0N	10.0N
DATA HOLD TIME	(TDH)	14.0N	14.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	6.00N
ADDRESS SETUP TIME	(TAS2)	218.N	176.N	64.0N
ADDRESS HOLD TIME	(TAH)	-20.0N	-16.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	86.0N	76.0N	44.0N
CS1 SETUP TIME	(TCSS1)	200.N	162.N	82.0N
CS2 SETUP TIME	(TCSS2)	196.N	158.N	80.0N
CS1 HOLD TIME	(TCSH1)	50.0N	46.0N	28.0N
CS2 HOLD TIME	(TCSH2)	54.0N	48.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	362.N	298.N	122.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	360.N	296.N	120.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	60.0N	54.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	164.N	132.N	44.0N
OUTPUT HOLD FROM CS2	(TDOH2)	160.N	130.N	44.0N
OUTPUT HOLD FROM MRD	(TDOH3)	146.N	122.N	36.0N
OUTPUT HOLD FROM MWR	(TPDH)	144.N	118.N	38.0N
READ CYCLE TIME	(TRC)	360.N	296.N	128.N
WRITE CYCLE TIME	(TWC)	256.N	232.N	136.N

	IIL	IIH	VIC1	VIC2
A0	-19.7NA	20.7NA	3.06 V	-3.03 V
A1	-18.6NA	20.2NA	3.08 V	-3.08 V
A2	-18.8NA	18.8NA	3.09 V	-3.12 V
A3	-19.8NA	20.8NA	3.08 V	-3.11 V
A4	-18.4NA	20.1NA	3.10 V	-3.09 V
A5	-20.4NA	20.6NA	3.04 V	-3.04 V
A6	-21.0NA	20.5NA	3.04 V	-3.04 V
A7	-20.5NA	18.5NA	3.05 V	-3.08 V
CS1	-21.7NA	20.3NA	3.05 V	-3.04 V
CS2	-20.9NA	20.2NA	3.09 V	-3.10 V
MWR	-21.6NA	19.5NA	3.04 V	-3.06 V
MRD	-19.2NA	19.1NA	3.05 V	-3.05 V
DI0	-19.4NA	20.6NA	3.11 V	-3.09 V
DI1	-20.4NA	19.3NA	3.09 V	-3.02 V
DI2	-20.4NA	20.2NA	3.10 V	-3.09 V
DI3	-19.4NA	20.3NA	3.09 V	-3.05 V

	D00	D01	D02	D03
VOL1	145.MV	145.MV	155.MV	150.MV
VOL2	145.MV	155.MV	170.MV	165.MV
VOH1	4.80 V	4.80 V	4.80 V	4.81 V
VOH2	9.72 V	9.73 V	9.72 V	9.73 V
IDN1	5.25MA	5.10MA	4.85MA	4.90MA
IDN2	13.2MA	12.4MA	11.3MA	11.6MA
IDP1	-2.00MA	-2.05MA	-2.00MA	-2.03MA
IDP2	-4.57MA	-4.64MA	-4.51MA	-4.68MA
IOZ1	167.NA	160.NA	172.NA	174.NA
IOZ2	157.NA	161.NA	170.NA	167.NA
IOZ3	161.NA	156.NA	169.NA	171.NA
IOZ4	152.NA	160.NA	172.NA	167.NA
IOZ5	160.NA	163.NA	173.NA	174.NA
IOZ6	161.NA	156.NA	184.NA	164.NA
IOZ7	167.NA	153.NA	178.NA	175.NA
IOZ8	158.NA	163.NA	174.NA	170.NA

ILDP	4.20UA
IL1	-20.0UA
IL2	-25.0UA
IL3	-45.0UA
IL4	-35.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	365.N	300.N	125.N
DATA SETUP TIME	(TDS)	24.0N	22.0N	10.0N
DATA HOLD TIME	(TDH)	16.0N	16.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	6.00N	6.00N	6.00N
ADDRESS SETUP TIME	(TAS2)	214.N	174.N	72.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-16.0N	-6.00N
WRITE PULSE WIDTH	(TWP)	92.0N	82.0N	46.0N
CS1 SETUP TIME	(TCSS1)	200.N	174.N	92.0N
CS2 SETUP TIME	(TCSS2)	192.N	168.N	88.0N
CS1 HOLD TIME	(TCSH1)	54.0N	48.0N	30.0N
CS2 HOLD TIME	(TCSH2)	58.0N	52.0N	30.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	368.N	306.N	130.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	364.N	304.N	128.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	64.0N	56.0N	34.0N
OUTPUT HOLD FROM CS1	(TDOH1)	166.N	136.N	48.0N
OUTPUT HOLD FROM CS2	(TDOH2)	162.N	132.N	50.0N
OUTPUT HOLD FROM MRD	(TDOH3)	144.N	124.N	38.0N
OUTPUT HOLD FROM MWR	(TPDH)	146.N	120.N	38.0N
READ CYCLE TIME	(TRC)	360.N	304.N	136.N
WRITE CYCLE TIME	(TWC)	264.N	240.N	144.N

	IIL	IIH	VIC1	VIC2
A0	-113.NA	111.NA	3.02 V	-2.99 V
A1	-109.NA	109.NA	3.03 V	-3.03 V
A2	-108.NA	105.NA	3.05 V	-3.09 V
A3	-111.NA	108.NA	3.04 V	-3.06 V
A4	-108.NA	106.NA	3.06 V	-3.05 V
A5	-114.NA	110.NA	3.00 V	-3.00 V
A6	-115.NA	109.NA	3.00 V	-3.00 V
A7	-113.NA	105.NA	3.01 V	-3.04 V
CS1	-118.NA	109.NA	3.01 V	-3.00 V
CS2	-114.NA	111.NA	3.05 V	-3.06 V
MWR	-113.NA	106.NA	3.00 V	-3.02 V
MRD	-108.NA	105.NA	3.01 V	-3.01 V
DI0	-109.NA	109.NA	3.06 V	-3.05 V
DI1	-110.NA	108.NA	3.05 V	-2.98 V
DI2	-109.NA	109.NA	3.05 V	-3.05 V
DI3	-106.NA	106.NA	3.04 V	-3.01 V

	DO0	DO1	DO2	DO3
VOL1	160.MV	160.MV	170.MV	170.MV
VOL2	160.MV	170.MV	190.MV	185.MV
VOH1	4.78 V	4.78 V	4.78 V	4.78 V
VOH2	9.69 V	9.70 V	9.68 V	9.70 V
IDN1	4.70MA	4.60MA	4.35MA	4.45MA
IDN2	11.7MA	11.2MA	10.0MA	10.4MA
IDP1	-1.82MA	-1.83MA	-1.81MA	-1.85MA
IDP2	-4.11MA	-4.15MA	-4.05MA	-4.22MA
IOZ1	623.NA	561.NA	687.NA	625.NA
IOZ2	610.NA	555.NA	674.NA	629.NA
IOZ3	605.NA	549.NA	675.NA	623.NA
IOZ4	602.NA	552.NA	666.NA	628.NA
IOZ5	616.NA	566.NA	693.NA	647.NA
IOZ6	606.NA	578.NA	684.NA	635.NA
IOZ7	606.NA	561.NA	692.NA	628.NA
IOZ8	611.NA	565.NA	683.NA	641.NA

ILDP	20.0UA
IL1	-85.0UA
IL2	-105.UA
IL3	-115.UA
IL4	-85.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	230.N	190.N	75.0N
DATA SETUP TIME	(TDS)	16.0N	14.0N	6.00N
DATA HOLD TIME	(TDH)	12.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	118.N	96.0N	40.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	56.0N	48.0N	30.0N
CS1 SETUP TIME	(TCSS1)	128.N	112.N	58.0N
CS2 SETUP TIME	(TCSS2)	126.N	108.N	56.0N
CS1 HOLD TIME	(TCSH1)	32.0N	30.0N	20.0N
CS2 HOLD TIME	(TCSH2)	34.0N	30.0N	18.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	230.N	190.N	86.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	228.N	188.N	84.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	46.0N	40.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	140.N	108.N	30.0N
OUTPUT HOLD FROM CS2	(TDOH2)	136.N	108.N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	114.N	28.0N
OUTPUT HOLD FROM MWR	(TPOH)	134.N	110.N	30.0N
READ CYCLE TIME	(TRC)	232.N	200.N	96.0N
WRITE CYCLE TIME	(TWC)	168.N	144.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-1.90NA	1.60NA	3.13 V	-3.10 V
A1	-1.90NA	1.90NA	3.15 V	-3.19 V
A2	-1.80NA	1.90NA	3.18 V	-3.19 V
A3	-1.90NA	2.00NA	3.17 V	-3.19 V
A4	-1.90NA	2.10NA	3.19 V	-3.22 V
A5	-1.70NA	1.80NA	3.11 V	-3.17 V
A6	-1.80NA	1.70NA	3.10 V	-3.16 V
A7	-2.00NA	2.20NA	3.11 V	-3.14 V
CS1	-1.90NA	1.60NA	3.19 V	-3.19 V
CS2	-1.90NA	1.80NA	3.24 V	-3.26 V
MWR	-2.50NA	1.90NA	3.11 V	-3.13 V
MRD	-1.80NA	1.90NA	3.16 V	-3.17 V
DI0	-2.20NA	1.80NA	3.26 V	-3.19 V
DI1	-1.80NA	1.90NA	3.22 V	-3.18 V
DI2	-1.60NA	2.00NA	3.28 V	-3.23 V
DI3	-1.70NA	2.00NA	3.24 V	-3.23 V

	D00	D01	D02	D03
VOL1	100.MV	105.MV	115.MV	115.MV
VOL2	115.MV	125.MV	140.MV	140.MV
VOH1	4.85 V	4.85 V	4.84 V	4.84 V
VOH2	9.76 V	9.76 V	9.76 V	9.75 V
IDN1	7.30MA	6.95MA	6.45MA	6.50MA
IDN2	16.6MA	15.4MA	13.6MA	13.8MA
IDP1	-2.61MA	-2.63MA	-2.53MA	-2.55MA
IDP2	-5.19MA	-5.25MA	-5.05MA	-5.00MA
IOZ1	10.0NA	14.4NA	7.40NA	15.9NA
IOZ2	12.2NA	11.3NA	9.60NA	13.1NA
IOZ3	12.4NA	10.4NA	11.6NA	10.0NA
IOZ4	9.70NA	13.3NA	8.20NA	13.2NA
IOZ5	14.8NA	8.50NA	11.3NA	10.9NA
IOZ6	14.6NA	8.90NA	11.6NA	10.7NA
IOZ7	14.6NA	8.60NA	11.3NA	10.7NA
IOZ8	14.4NA	8.80NA	11.6NA	10.6NA

ILDP	-10.0UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-25.0UA
IL4	-20.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	245.N	185.N	70.0N
DATA SETUP TIME	(TDS)	18.0N	14.0N	6.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	12.0N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	128.N	96.0N	36.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	60.0N	46.0N	28.0N
CS1 SETUP TIME	(TCSS1)	126.N	108.N	54.0N
CS2 SETUP TIME	(TCSS2)	122.N	106.N	52.0N
CS1 HOLD TIME	(TCSH1)	28.0N	24.0N	18.0N
CS2 HOLD TIME	(TCSH2)	30.0N	26.0N	16.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	242.N	192.N	80.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	240.N	190.N	78.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	42.0N	36.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	132.N	102.N	30.0N
OUTPUT HOLD FROM CS2	(TDOH2)	130.N	100.N	30.0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	112.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	108.N	28.0N
READ CYCLE TIME	(TRC)	216.N	184.N	88.0N
WRITE CYCLE TIME	(TWC)	176.N	144.N	88.0N

	IIL	IIH	VIC1	VIC2
A0	-200.PA	200.PA	3.20 V	-3.16 V
A1	-200.PA	200.PA	3.23 V	-3.26 V
A2	-200.PA	300.PA	3.24 V	-3.25 V
A3	-200.PA	300.PA	3.24 V	-3.25 V
A4	-300.PA	300.PA	3.26 V	-3.28 V
A5	-300.PA	200.PA	3.17 V	-3.23 V
A6	-200.PA	200.PA	3.16 V	-3.22 V
A7	-200.PA	400.PA	3.17 V	-3.20 V
CS1	-300.PA	200.PA	3.26 V	-3.25 V
CS2	-300.PA	200.PA	3.30 V	-3.32 V
MWR	-500.PA	300.PA	3.18 V	-3.20 V
MRD	-200.PA	300.PA	3.23 V	-3.23 V
DI0	-300.PA	200.PA	3.33 V	-3.25 V
DI1	-200.PA	300.PA	3.29 V	-3.24 V
DI2	-200.PA	300.PA	3.35 V	-3.29 V
DI3	-200.PA	400.PA	3.31 V	-3.29 V

	DO0	DO1	DO2	DO3
VOL1	90.0MV	95.0MV	105.MV	100.MV
VOL2	105.MV	110.MV	125.MV	125.MV
VOH1	4.87 V	4.87 V	4.87 V	4.86 V
VOH2	9.79 V	9.80 V	9.78 V	9.77 V
IDN1	8.00MA	7.60MA	7.15MA	7.15MA
IDN2	18.2MA	16.9MA	15.0MA	15.3MA
IDP1	-2.97MA	-2.99MA	-2.94MA	-2.88MA
IDP2	-5.83MA	-5.91MA	-5.72MA	-5.59MA
IOZ1	3.00NA	4.00NA	2.90NA	2.70NA
IOZ2	300.PA	7.10NA	-400.PA	6.30NA
IOZ3	7.40NA	-100.PA	6.20NA	400.PA
IOZ4	5.30NA	300.PA	5.20NA	200.PA
IOZ5	800.PA	5.70NA	-400.PA	6.50NA
IOZ6	1.10NA	5.80NA	-400.PA	6.20NA
IOZ7	1.00NA	5.40NA	-300.PA	6.40NA
IOZ8	1.30NA	5.50NA	-400.PA	6.20NA

ILDP	-5.00UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-20.0UA
IL4	-25.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	245.N	180.N	65.0N
DATA SETUP TIME	(TDS)	20.0N	16.0N	6.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	8.00N
ADDRESS SETUP TIME	(TAS1)	10.0N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	130.N	96.0N	32.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-10.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	52.0N	46.0N	26.0N
CS1 SETUP TIME	(TCSS1)	122.N	104.N	50.0N
CS2 SETUP TIME	(TCSS2)	120.N	102.N	48.0N
CS1 HOLD TIME	(TCSH1)	32.0N	24.0N	18.0N
CS2 HOLD TIME	(TCSH2)	32.0N	26.0N	14.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	258.N	192.N	76.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	254.N	184.N	74.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	38.0N	34.0N	20.0N
OUTPUT HOLD FROM CS1	(TDOH1)	128.N	98.0N	30.0N
OUTPUT HOLD FROM CS2	(TDOH2)	126.N	96.0N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	112.N	26.0N
OUTPUT HOLD FROM MWR	(TPDH)	130.N	108.N	28.0N
READ CYCLE TIME	(TRC)	208.N	176.N	96.0N
WRITE CYCLE TIME	(TWC)	152.N	144.N	80.0N

	IIL	IIH	VIC1	VIC2
A0	-100.PA	0.00 A	3.26 V	-3.22 V
A1	-100.PA	100.PA	3.28 V	-3.32 V
A2	0.00 A	100.PA	3.30 V	-3.31 V
A3	-100.PA	100.PA	3.29 V	-3.31 V
A4	-100.PA	100.PA	3.31 V	-3.34 V
A5	-100.PA	100.PA	3.22 V	-3.29 V
A6	0.00 A	100.PA	3.22 V	-3.28 V
A7	-100.PA	100.PA	3.23 V	-3.26 V
CS1	-100.PA	100.PA	3.32 V	-3.31 V
CS2	-100.PA	100.PA	3.36 V	-3.38 V
MWR	-100.PA	100.PA	3.23 V	-3.25 V
MRD	-100.PA	100.PA	3.29 V	-3.29 V
DI0	-100.PA	0.00 A	3.38 V	-3.31 V
DI1	0.00 A	100.PA	3.35 V	-3.29 V
DI2	0.00 A	100.PA	3.40 V	-3.35 V
DI3	0.00 A	100.PA	3.37 V	-3.35 V

	D00	D01	D02	D03
VOL1	85.0MV	90.0MV	95.0MV	95.0MV
VOL2	95.0MV	105.MV	115.MV	115.MV
VOH1	4.88 V	4.88 V	4.88 V	4.88 V
VOH2	9.80 V	9.81 V	9.80 V	9.80 V
IDN1	8.65MA	8.30MA	7.75MA	7.75MA
IDN2	19.5MA	18.3MA	16.3MA	16.5MA
IDP1	-3.35MA	-3.39MA	-3.32MA	-3.21MA
IDP2	-6.51MA	-6.58MA	-6.34MA	-6.08MA
IOZ1	3.60NA	-100.PA	3.30NA	-700.PA
IOZ2	-400.PA	3.50NA	-400.PA	3.00NA
IOZ3	4.10NA	-400.PA	2.90NA	500.PA
IOZ4	5.00NA	-1.90NA	5.10NA	-1.90NA
IOZ5	-1.50NA	5.20NA	-2.20NA	5.30NA
IOZ6	-1.60NA	5.00NA	-2.00NA	5.40NA
IOZ7	-1.50NA	5.10NA	-2.20NA	5.20NA
IOZ8	-1.60NA	4.90NA	-2.00NA	5.40NA

ILDP	-10.0UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-15.0UA
IL4	-20.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	215.N	185.N	80.0N
DATA SETUP TIME	(TDS)	16.0N	14.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	6.00N	6.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	112.N	92.0N	44.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	62.0N	54.0N	34.0N
CS1 SETUP TIME	(TCSS1)	132.N	116.N	62.0N
CS2 SETUP TIME	(TCSS2)	130.N	114.N	60.0N
CS1 HOLD TIME	(TCSH1)	38.0N	32.0N	22.0N
CS2 HOLD TIME	(TCSH2)	38.0N	34.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	222.N	190.N	94.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	218.N	188.N	92.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	46.0N	42.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	140.N	110.N	32.0N
OUTPUT HOLD FROM CS2	(TDOH2)	138.N	108.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	134.N	110.N	30.0N
READ CYCLE TIME	(TRC)	240.N	208.N	104.N
WRITE CYCLE TIME	(TWC)	176.N	160.N	104.N

	IIL	IIH	VIC1	VIC2
A0	-27.6NA	26.6NA	3.11 V	-3.07 V
A1	-27.0NA	28.1NA	3.13 V	-3.16 V
A2	-28.7NA	28.1NA	3.15 V	-3.17 V
A3	-28.0NA	28.2NA	3.14 V	-3.16 V
A4	-27.7NA	28.4NA	3.16 V	-3.19 V
A5	-26.8NA	26.3NA	3.08 V	-3.14 V
A6	-27.8NA	27.3NA	3.07 V	-3.13 V
A7	-28.0NA	29.4NA	3.08 V	-3.11 V
CS1	-29.2NA	27.2NA	3.17 V	-3.16 V
CS2	-28.2NA	29.5NA	3.21 V	-3.24 V
MWR	-29.4NA	27.7NA	3.08 V	-3.11 V
MRD	-28.0NA	28.5NA	3.14 V	-3.14 V
DI0	-28.5NA	27.6NA	3.24 V	-3.17 V
DI1	-26.8NA	27.9NA	3.20 V	-3.15 V
DI2	-27.1NA	29.1NA	3.25 V	-3.20 V
DI3	-27.0NA	28.8NA	3.22 V	-3.20 V

	D00	D01	D02	D03
VOL1	115.MV	120.MV	130.MV	130.MV
VOL2	130.MV	140.MV	160.MV	160.MV
VOH1	4.82 V	4.82 V	4.82 V	4.82 V
VOH2	9.72 V	9.73 V	9.72 V	9.72 V
IDN1	6.45MA	6.10MA	5.70MA	5.75MA
IDN2	14.7MA	13.5MA	11.9MA	12.2MA
IDP1	-2.24MA	-2.26MA	-2.21MA	-2.21MA
IDP2	-4.53MA	-4.61MA	-4.42MA	-4.42MA
IOZ1	4.30NA	-15.0NA	-25.9NA	-6.70NA
IOZ2	1.10NA	-20.4NA	-27.1NA	-9.60NA
IOZ3	-1.40NA	-27.7NA	-25.3NA	-16.7NA
IOZ4	-2.30NA	-24.2NA	-27.8NA	-13.6NA
IOZ5	-100.PA	-27.6NA	-27.0NA	-17.2NA
IOZ6	1.00NA	-28.4NA	-27.6NA	-16.7NA
IOZ7	-1.70NA	-28.8NA	-26.8NA	-16.8NA
IOZ8	1.00NA	-29.1NA	-26.6NA	-16.7NA
ILDP	7.40UA			
IL1	-35.0UA			
IL2	-40.0UA			
IL3	-50.0UA			
IL4	-45.0UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	225.N	195.N	90.0N
DATA SETUP TIME	(TDS)	16.0N	14.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	4.00N	4.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	114.N	96.0N	50.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	64.0N	58.0N	36.0N
CS1 SETUP TIME	(TCSS1)	140.N	124.N	68.0N
CS2 SETUP TIME	(TCSS2)	136.N	122.N	66.0N
CS1 HOLD TIME	(TCSH1)	38.0N	34.0N	22.0N
CS2 HOLD TIME	(TCSH2)	40.0N	36.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	234.N	202.N	102.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	232.N	200.N	100.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	44.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	142.N	112.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	138.N	110.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	32.0N
OUTPUT HOLD FROM MWR	(TPDH)	134.N	112.N	32.0N
READ CYCLE TIME	(TRC)	248.N	216.N	120.N
WRITE CYCLE TIME	(TWC)	184.N	176.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-165.NA	157.NA	3.09 V	-3.05 V
A1	-163.NA	163.NA	3.12 V	-3.15 V
A2	-168.NA	163.NA	3.14 V	-3.15 V
A3	-166.NA	160.NA	3.13 V	-3.15 V
A4	-165.NA	163.NA	3.15 V	-3.18 V
A5	-162.NA	156.NA	3.06 V	-3.13 V
A6	-166.NA	160.NA	3.05 V	-3.12 V
A7	-165.NA	167.NA	3.06 V	-3.10 V
CS1	-175.NA	162.NA	3.15 V	-3.14 V
CS2	-171.NA	171.NA	3.20 V	-3.23 V
MWR	-168.NA	161.NA	3.06 V	-3.10 V
MRD	-166.NA	166.NA	3.12 V	-3.13 V
DI0	-166.NA	161.NA	3.23 V	-3.15 V
DI1	-162.NA	159.NA	3.18 V	-3.14 V
DI2	-163.NA	168.NA	3.24 V	-3.19 V
DI3	-163.NA	166.NA	3.21 V	-3.19 V

	D00	D01	D02	D03
VOL1	125.MV	135.MV	145.MV	145.MV
VOL2	140.MV	155.MV	175.MV	175.MV
VOH1	4.81 V	4.80 V	4.80 V	4.80 V
VOH2	9.69 V	9.69 V	9.69 V	9.69 V
IDN1	5.85MA	5.55MA	5.15MA	5.20MA
IDN2	13.5MA	12.4MA	10.8MA	11.2MA
IDP1	-2.05MA	-2.07MA	-2.00MA	-2.04MA
IDP2	-4.16MA	-4.20MA	-4.03MA	-4.10MA
IOZ1	-366.NA	-493.NA	-496.NA	-438.NA
IOZ2	-378.NA	-506.NA	-499.NA	-445.NA
IOZ3	-388.NA	-506.NA	-506.NA	-445.NA
IOZ4	-381.NA	-515.NA	-503.NA	-453.NA
IOZ5	-380.NA	-507.NA	-506.NA	-457.NA
IOZ6	-380.NA	-523.NA	-505.NA	-452.NA
IOZ7	-385.NA	-517.NA	-518.NA	-445.NA
IOZ8	-388.NA	-514.NA	-509.NA	-454.NA

ILDP	80.0UA
IL1	-150.UA
IL2	-195.UA
IL3	-140.UA
IL4	-120.UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	285.N	235.N	95.0N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	14.0N	14.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	18.0N	14.0N	6.00N
ADDRESS SETUP TIME	(TAS2)	136.N	116.N	58.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-16.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	78.0N	68.0N	36.0N
CS1 SETUP TIME	(TCSS1)	188.N	160.N	78.0N
CS2 SETUP TIME	(TCSS2)	182.N	158.N	78.0N
CS1 HOLD TIME	(TCSH1)	36.0N	32.0N	22.0N
CS2 HOLD TIME	(TCSH2)	40.0N	36.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	262.N	224.N	106.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	258.N	222.N	104.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	58.0N	52.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	160.N	128.N	40.0N
OUTPUT HOLD FROM CS2	(TDOH2)	156.N	124.N	40.0N
OUTPUT HOLD FROM MRD	(TDOH3)	144.N	122.N	36.0N
OUTPUT HOLD FROM MWR	(TPDH)	142.N	118.N	38.0N
READ CYCLE TIME	(TRC)	288.N	248.N	128.N
WRITE CYCLE TIME	(TWC)	264.N	232.N	128.N

	IIL	IIH	VIC1	VIC2
A0	-1.80NA	1.70NA	3.17 V	-3.14 V
A1	-1.50NA	1.60NA	3.18 V	-3.21 V
A2	-1.50NA	1.50NA	3.20 V	-3.21 V
A3	-2.80NA	1.70NA	3.19 V	-3.21 V
A4	-1.50NA	1.70NA	3.22 V	-3.19 V
A5	-1.50NA	1.90NA	3.13 V	-3.16 V
A6	-1.50NA	2.50NA	3.11 V	-3.17 V
A7	-1.40NA	2.00NA	3.13 V	-3.15 V
CS1	-1.50NA	1.50NA	3.16 V	-3.17 V
CS2	-1.90NA	1.80NA	3.18 V	-3.17 V
MWR	-1.70NA	1.40NA	3.13 V	-3.16 V
MRD	-1.50NA	1.60NA	3.14 V	-3.13 V
DI0	-2.20NA	2.10NA	3.23 V	-3.22 V
DI1	-2.40NA	2.50NA	3.23 V	-3.16 V
DI2	-1.80NA	2.20NA	3.22 V	-3.17 V
DI3	-1.90NA	2.00NA	3.20 V	-3.16 V

	D00	D01	D02	D03
VOL1	120.MV	125.MV	130.MV	130.MV
VOL2	125.MV	135.MV	150.MV	145.MV
VOH1	4.83 V	4.84 V	4.82 V	4.83 V
VOH2	9.76 V	9.76 V	9.74 V	9.76 V
IDN1	6.15MA	6.00MA	5.65MA	5.65MA
IDN2	15.4MA	14.3MA	12.8MA	13.1MA
IDP1	-2.30MA	-2.30MA	-2.24MA	-2.32MA
IDP2	-5.13MA	-5.16MA	-4.97MA	-5.24MA
IOZ1	35.8NA	28.7NA	34.7NA	28.5NA
IOZ2	32.7NA	30.1NA	32.6NA	29.3NA
IOZ3	30.0NA	33.4NA	27.9NA	34.1NA
IOZ4	33.5NA	29.7NA	31.0NA	31.3NA
IOZ5	30.1NA	32.6NA	29.8NA	32.9NA
IOZ6	30.5NA	33.1NA	29.7NA	32.5NA
IOZ7	30.1NA	32.7NA	29.8NA	32.9NA
IOZ8	30.1NA	32.8NA	29.6NA	32.4NA

ILDP	-20.0UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-35.0UA
IL4	-30.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	285.N	230.N	90.0N
DATA SETUP TIME	(TDS)	28.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	20.0N	16.0N	6.00N
ADDRESS SETUP TIME	(TAS2)	130.N	104.N	50.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	70.0N	70.0N	36.0N
CS1 SETUP TIME	(TCSS1)	180.N	150.N	72.0N
CS2 SETUP TIME	(TCSS2)	174.N	150.N	70.0N
CS1 HOLD TIME	(TCSH1)	36.0N	32.0N	22.0N
CS2 HOLD TIME	(TCSH2)	38.0N	34.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	262.N	216.N	98.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	258.N	214.N	96.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	54.0N	46.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	152.N	118.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	148.N	116.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	120.N	34.0N
OUTPUT HOLD FROM MWR	(TPDH)	140.N	116.N	34.0N
READ CYCLE TIME	(TRC)	272.N	224.N	120.N
WRITE CYCLE TIME	(TWC)	280.N	208.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-300.PA	300.PA	3.25 V	-3.22 V
A1	-200.PA	300.PA	3.25 V	-3.28 V
A2	-200.PA	200.PA	3.27 V	-3.28 V
A3	-700.PA	200.PA	3.26 V	-3.28 V
A4	-300.PA	300.PA	3.29 V	-3.26 V
A5	-400.PA	300.PA	3.21 V	-3.23 V
A6	-300.PA	500.PA	3.19 V	-3.25 V
A7	-200.PA	400.PA	3.21 V	-3.22 V
CS1	-300.PA	300.PA	3.24 V	-3.25 V
CS2	-400.PA	300.PA	3.26 V	-3.23 V
MWR	-400.PA	300.PA	3.21 V	-3.23 V
MRD	-300.PA	400.PA	3.22 V	-3.21 V
DI0	-400.PA	300.PA	3.30 V	-3.29 V
DI1	-500.PA	400.PA	3.31 V	-3.24 V
DI2	-300.PA	400.PA	3.30 V	-3.25 V
DI3	-300.PA	400.PA	3.28 V	-3.23 V

	D00	D01	D02	D03
VOL1	105.MV	110.MV	115.MV	115.MV
VOL2	110.MV	115.MV	130.MV	125.MV
VOH1	4.86 V	4.86 V	4.86 V	4.86 V
VOH2	9.80 V	9.80 V	9.79 V	9.80 V
IDN1	6.90MA	6.70MA	6.35MA	6.35MA
IDN2	17.5MA	16.4MA	14.8MA	15.0MA
IDP1	-2.69MA	-2.73MA	-2.65MA	-2.74MA
IDP2	-5.97MA	-6.11MA	-5.83MA	-6.13MA
IOZ1	2.10NA	8.50NA	1.30NA	8.80NA
IOZ2	4.20NA	5.60NA	2.70NA	6.80NA
IOZ3	5.90NA	2.60NA	6.30NA	2.60NA
IOZ4	2.40NA	6.10NA	2.90NA	5.90NA
IOZ5	6.30NA	3.20NA	5.30NA	4.60NA
IOZ6	6.50NA	3.00NA	5.00NA	4.60NA
IOZ7	6.20NA	3.30NA	5.10NA	4.60NA
IOZ8	6.40NA	3.00NA	4.60NA	4.60NA
ILDP	-10.0UA			
IL1	-5.00UA			
IL2	-5.00UA			
IL3	-25.0UA			
IL4	-25.0UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	280.N	220.N	85.0N
DATA SETUP TIME	(TDS)	32.0N	24.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	10.0N	14.0N	6.00N
ADDRESS SETUP TIME	(TAS2)	126.N	102.N	48.0N
ADDRESS HOLD TIME	(TAH)	-20.0N	-16.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	70.0N	60.0N	34.0N
CS1 SETUP TIME	(TCSS1)	174.N	146.N	68.0N
CS2 SETUP TIME	(TCSS2)	174.N	142.N	66.0N
CS1 HOLD TIME	(TCSH1)	42.0N	36.0N	22.0N
CS2 HOLD TIME	(TCSH2)	46.0N	38.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	260.N	210.N	90.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	258.N	208.N	88.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	44.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	144.N	112.N	32.0N
OUTPUT HOLD FROM CS2	(TDOH2)	140.N	108.N	30.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	118.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	138.N	114.N	32.0N
READ CYCLE TIME	(TRC)	248.N	216.N	120.N
WRITE CYCLE TIME	(TWC)	248.N	256.N	104.N

	IIL	IIH	VIC1	VIC2
A0	0.00 A	100.PA	3.34 V	-3.29 V
A1	0.00 A	100.PA	3.34 V	-3.36 V
A2	0.00 A	100.PA	3.39 V	-3.35 V
A3	-200.PA	100.PA	3.34 V	-3.36 V
A4	-100.PA	100.PA	3.37 V	-3.34 V
A5	-100.PA	100.PA	3.29 V	-3.31 V
A6	-100.PA	100.PA	3.27 V	-3.32 V
A7	-100.PA	100.PA	3.29 V	-3.30 V
CS1	-100.PA	100.PA	3.32 V	-3.32 V
CS2	-100.PA	100.PA	3.35 V	-3.31 V
MWR	-100.PA	100.PA	3.30 V	-3.32 V
MRD	-100.PA	100.PA	3.30 V	-3.29 V
DI0	-100.PA	100.PA	3.38 V	-3.37 V
DI1	-200.PA	100.PA	3.39 V	-3.31 V
DI2	-100.PA	100.PA	3.38 V	-3.32 V
DI3	-100.PA	100.PA	3.36 V	-3.30 V

	DO0	DO1	DO2	DO3
VOL1	100.MV	100.MV	105.MV	105.MV
VOL2	95.0MV	105.MV	115.MV	115.MV
VOH1	4.88 V	4.88 V	4.88 V	4.88 V
VOH2	9.82 V	9.82 V	9.81 V	9.83 V
IDN1	7.45MA	7.30MA	6.90MA	6.90MA
IDN2	19.3MA	18.2MA	16.4MA	16.6MA
IDP1	-3.09MA	-3.13MA	-3.08MA	-3.18MA
IDP2	-6.85MA	-6.96MA	-6.74MA	-7.06MA
IOZ1	6.00NA	-1.30NA	5.80NA	-1.40NA
IOZ2	2.80NA	600.PA	3.40NA	-500.PA
IOZ3	1.10NA	3.20NA	-600.PA	3.90NA
IOZ4	4.60NA	-200.PA	3.00NA	700.PA
IOZ5	400.PA	2.70NA	800.PA	2.20NA
IOZ6	400.PA	3.00NA	900.PA	1.80NA
IOZ7	500.PA	2.50NA	900.PA	2.00NA
IOZ8	600.PA	2.80NA	1.10NA	1.60NA

ILDP	-10.0UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-5.00UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	280.N	240.N	105.N
DATA SETUP TIME	(TDS)	26.0N	22.0N	10.0N
DATA HOLD TIME	(TDH)	16.0N	14.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	10.0N	10.0N	6.00N
ADDRESS SETUP TIME	(TAS2)	140.N	122.N	64.0N
ADDRESS HOLD TIME	(TAH)	-20.0N	-16.0N	-6.00N
WRITE PULSE WIDTH	(TWP)	86.0N	78.0N	44.0N
CS1 SETUP TIME	(TCSS1)	196.N	168.N	86.0N
CS2 SETUP TIME	(TCSS2)	190.N	166.N	86.0N
CS1 HOLD TIME	(TCSH1)	52.0N	46.0N	28.0N
CS2 HOLD TIME	(TCSH2)	56.0N	50.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	270.N	236.N	120.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	266.N	232.N	116.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	64.0N	56.0N	32.0N
OUTPUT HOLD FROM CS1	(TDOH1)	166.N	134.N	46.0N
OUTPUT HOLD FROM CS2	(TDOH2)	162.N	130.N	46.0N
OUTPUT HOLD FROM MRD	(TDOH3)	146.N	124.N	38.0N
OUTPUT HOLD FROM MWR	(TPOH)	144.N	120.N	40.0N
READ CYCLE TIME	(TRC)	304.N	264.N	128.N
WRITE CYCLE TIME	(TWC)	264.N	232.N	136.N

	IIL	IIH	VIC1	VIC2
A0	-19.2NA	18.5NA	3.15 V	-3.12 V
A1	-18.8NA	18.4NA	3.15 V	-3.19 V
A2	-18.0NA	18.2NA	3.18 V	-3.19 V
A3	-22.0NA	18.4NA	3.17 V	-3.19 V
A4	-18.4NA	18.5NA	3.20 V	-3.17 V
A5	-18.9NA	18.5NA	3.11 V	-3.13 V
A6	-18.4NA	21.0NA	3.09 V	-3.15 V
A7	-18.1NA	19.4NA	3.11 V	-3.13 V
CS1	-19.3NA	18.4NA	3.13 V	-3.15 V
CS2	-19.2NA	20.2NA	3.16 V	-3.19 V
MWR	-17.7NA	17.5NA	3.11 V	-3.13 V
MRD	-18.6NA	18.6NA	3.12 V	-3.11 V
DI0	-19.1NA	20.4NA	3.20 V	-3.19 V
DI1	-20.6NA	19.2NA	3.21 V	-3.14 V
DI2	-18.1NA	19.7NA	3.20 V	-3.15 V
DI3	-18.8NA	19.5NA	3.17 V	-3.13 V

	DO0	DO1	DO2	DO3
VOL1	140.MV	145.MV	150.MV	155.MV
VOL2	145.MV	155.MV	175.MV	175.MV
VOH1	4.80 V	4.80 V	4.79 V	4.80 V
VOH2	9.71 V	9.72 V	9.70 V	9.72 V
IDN1	5.35MA	5.20MA	4.90MA	4.90MA
IDN2	13.2MA	12.2MA	11.0MA	11.2MA
IDP1	-1.91MA	-1.96MA	-1.80MA	-1.94MA
IDP2	-4.31MA	-4.37MA	-4.17MA	-4.40MA
IOZ1	337.NA	323.NA	301.NA	328.NA
IOZ2	327.NA	330.NA	299.NA	321.NA
IOZ3	330.NA	324.NA	300.NA	326.NA
IOZ4	323.NA	330.NA	302.NA	320.NA
IOZ5	327.NA	332.NA	304.NA	331.NA
IOZ6	331.NA	327.NA	315.NA	320.NA
IOZ7	337.NA	323.NA	307.NA	329.NA
IOZ8	327.NA	332.NA	306.NA	325.NA

ILDP	-5.00UA
IL1	-20.0UA
IL2	-25.0UA
IL3	-50.0UA
IL4	-45.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	285.N	245.N	120.N
DATA SETUP TIME	(TDS)	26.0N	22.0N	10.0N
DATA HOLD TIME	(TDH)	18.0N	16.0N	16.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	6.00N
ADDRESS SETUP TIME	(TAS2)	146.N	130.N	72.0N
ADDRESS HOLD TIME	(TAH)	-20.0N	-18.0N	-8.00N
WRITE PULSE WIDTH	(TWP)	94.0N	84.0N	48.0N
CS1 SETUP TIME	(TCSS1)	206.N	182.N	94.0N
CS2 SETUP TIME	(TCSS2)	202.N	176.N	92.0N
CS1 HOLD TIME	(TCSH1)	56.0N	50.0N	30.0N
CS2 HOLD TIME	(TCSH2)	62.0N	54.0N	30.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	286.N	250.N	130.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	280.N	246.N	128.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	68.0N	60.0N	36.0N
OUTPUT HOLD FROM CS1	(TDOH1)	170.N	138.N	50.0N
OUTPUT HOLD FROM CS2	(TDOH2)	164.N	134.N	50.0N
OUTPUT HOLD FROM MRD	(TDOH3)	146.N	124.N	38.0N
OUTPUT HOLD FROM MWR	(TPDH)	148.N	124.N	40.0N
READ CYCLE TIME	(TRC)	312.N	272.N	136.N
WRITE CYCLE TIME	(TWC)	280.N	240.N	152.N

	IIL	IIH	VIC1	VIC2
A0	-105.NA	102.NA	3.14 V	-3.11 V
A1	-105.NA	99.5NA	3.14 V	-3.19 V
A2	-103.NA	99.7NA	3.18 V	-3.19 V
A3	-112.NA	102.NA	3.16 V	-3.19 V
A4	-104.NA	101.NA	3.20 V	-3.17 V
A5	-106.NA	101.NA	3.09 V	-3.13 V
A6	-105.NA	106.NA	3.08 V	-3.14 V
A7	-104.NA	104.NA	3.10 V	-3.12 V
CS1	-110.NA	102.NA	3.13 V	-3.14 V
CS2	-109.NA	107.NA	3.15 V	-3.15 V
MWR	-104.NA	99.4NA	3.10 V	-3.13 V
MRD	-105.NA	103.NA	3.10 V	-3.10 V
DI0	-105.NA	106.NA	3.20 V	-3.19 V
DI1	-111.NA	105.NA	3.20 V	-3.13 V
DI2	-103.NA	105.NA	3.19 V	-3.14 V
DI3	-105.NA	105.NA	3.17 V	-3.13 V

	D00	D01	D02	D03
VOL1	155.MV	160.MV	170.MV	170.MV
VOL2	165.MV	175.MV	200.MV	195.MV
VOH1	4.77 V	4.77 V	4.76 V	4.78 V
VOH2	9.68 V	9.68 V	9.66 V	9.68 V
IDN1	4.80MA	4.70MA	4.40MA	4.40MA
IDN2	11.7MA	10.9MA	9.75MA	9.95MA
IDP1	-1.73MA	-1.75MA	-1.68MA	-1.77MA
IDP2	-3.88MA	-3.91MA	-3.73MA	-3.96MA
IOZ1	1.43UA	1.38UA	1.31UA	1.37UA
IOZ2	1.42UA	1.38UA	1.31UA	1.38UA
IOZ3	1.42UA	1.37UA	1.32UA	1.37UA
IOZ4	1.42UA	1.37UA	1.31UA	1.38UA
IOZ5	1.43UA	1.39UA	1.34UA	1.41UA
IOZ6	1.44UA	1.39UA	1.34UA	1.39UA
IOZ7	1.44UA	1.39UA	1.33UA	1.39UA
IOZ8	1.42UA	1.39UA	1.32UA	1.40UA
ILDP	15.0UA			
IL1	-80.0UA			
IL2	-90.0UA			
IL3	-120.UA			
IL4	-105.UA			

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN: 22

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	225.N	195.N	85.0N
DATA SETUP TIME	(TDS)	26.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	14.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	112.N	98.0N	48.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	76.0N	68.0N	38.0N
CS1 SETUP TIME	(TCSS1)	170.N	146.N	72.0N
CS2 SETUP TIME	(TCSS2)	166.N	142.N	70.0N
CS1 HOLD TIME	(TCSH1)	50.0N	46.0N	26.0N
CS2 HOLD TIME	(TCSH2)	54.0N	46.0N	26.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	216.N	188.N	94.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	214.N	184.N	90.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	44.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	142.N	112.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	140.N	110.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	32.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	112.N	32.0N
READ CYCLE TIME	(TRC)	240.N	208.N	120.N
WRITE CYCLE TIME	(TWC)	224.N	200.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-3.70NA	3.50NA	3.30 V	-3.30 V
A1	-3.70NA	3.80NA	3.32 V	-3.35 V
A2	-3.40NA	3.20NA	3.34 V	-3.36 V
A3	-3.60NA	3.00NA	3.30 V	-3.34 V
A4	-3.00NA	2.60NA	3.29 V	-3.30 V
A5	-4.30NA	4.10NA	3.35 V	-3.38 V
A6	-4.90NA	5.00NA	3.37 V	-3.40 V
A7	-5.70NA	4.90NA	3.41 V	-3.45 V
CS1	-3.50NA	3.30NA	3.30 V	-3.30 V
CS2	-3.50NA	3.50NA	3.34 V	-3.38 V
MWR	-3.10NA	2.90NA	3.22 V	-3.24 V
MRD	-3.30NA	3.10NA	3.27 V	-3.28 V
DI0	-5.20NA	5.30NA	3.53 V	-3.49 V
DI1	-5.30NA	5.10NA	3.49 V	-3.44 V
DI2	-4.30NA	4.10NA	3.46 V	-3.40 V
DI3	-4.10NA	3.90NA	3.45 V	-3.40 V

	D00	D01	D02	D03
VOL1	100.MV	105.MV	110.MV	110.MV
VOL2	110.MV	125.MV	140.MV	135.MV
VOH1	4.84 V	4.84 V	4.84 V	4.84 V
VOH2	9.77 V	9.77 V	9.76 V	9.77 V
IDN1	7.45MA	7.05MA	6.65MA	6.65MA
IDN2	17.2MA	15.4MA	13.8MA	14.0MA
IDP1	-2.43MA	-2.47MA	-2.43MA	-2.46MA
IDP2	-5.43MA	-5.47MA	-5.30MA	-5.49MA
IOZ1	138.NA	120.NA	107.NA	101.NA
IOZ2	131.NA	126.NA	102.NA	101.NA
IOZ3	135.NA	123.NA	103.NA	104.NA
IOZ4	127.NA	130.NA	103.NA	100.NA
IOZ5	135.NA	125.NA	106.NA	108.NA
IOZ6	128.NA	128.NA	110.NA	97.6NA
IOZ7	134.NA	119.NA	115.NA	98.4NA
IOZ8	135.NA	124.NA	105.NA	106.NA

ILDP	-5.00UA
IL1	-5.00UA
IL2	-10.0UA
IL3	-10.0UA
IL4	-10.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	230.N	190.N	75.0N
DATA SETUP TIME	(TDS)	26.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	20.0N	14.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	108.N	90.0N	42.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-12.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	72.0N	60.0N	34.0N
CS1 SETUP TIME	(TCSS1)	166.N	140.N	66.0N
CS2 SETUP TIME	(TCSS2)	162.N	136.N	64.0N
CS1 HOLD TIME	(TCSH1)	40.0N	36.0N	22.0N
CS2 HOLD TIME	(TCSH2)	42.0N	38.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	210.N	178.N	84.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	208.N	176.N	82.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	44.0N	40.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	136.N	106.N	30.0N
OUTPUT HOLD FROM CS2	(TDOH2)	134.N	106.N	30.0N
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	114.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	108.N	30.0N
READ CYCLE TIME	(TRC)	240.N	200.N	112.N
WRITE CYCLE TIME	(TWC)	264.N	184.N	104.N

	IIL	IIH	VIC1	VIC2
A0	-400.PA	300.PA	3.26 V	-3.26 V
A1	-300.PA	400.PA	3.28 V	-3.30 V
A2	-300.PA	300.PA	3.30 V	-3.31 V
A3	-400.PA	300.PA	3.27 V	-3.30 V
A4	-300.PA	300.PA	3.27 V	-3.28 V
A5	-400.PA	400.PA	3.29 V	-3.32 V
A6	-500.PA	500.PA	3.30 V	-3.34 V
A7	-500.PA	400.PA	3.34 V	-3.38 V
CS1	-400.PA	400.PA	3.27 V	-3.27 V
CS2	-400.PA	400.PA	3.30 V	-3.34 V
MWR	-400.PA	300.PA	3.21 V	-3.23 V
MRD	-400.PA	400.PA	3.25 V	-3.26 V
DI0	-400.PA	400.PA	3.45 V	-3.41 V
DI1	-500.PA	400.PA	3.42 V	-3.37 V
DI2	-400.PA	400.PA	3.40 V	-3.34 V
DI3	-400.PA	300.PA	3.38 V	-3.34 V

	D00	D01	D02	D03
VOL1	85.0MV	90.0MV	95.0MV	95.0MV
VOL2	95.0MV	105.MV	120.MV	115.MV
VOH1	4.87 V	4.87 V	4.86 V	4.87 V
VOH2	9.81 V	9.81 V	9.80 V	9.81 V
IDN1	8.40MA	8.00MA	7.55MA	7.60MA
IDN2	19.6MA	17.8MA	16.0MA	16.1MA
IDP1	-2.89MA	-2.93MA	-2.88MA	-2.95MA
IDP2	-6.41MA	-6.45MA	-6.30MA	-6.52MA
IOZ1	13.6NA	13.2NA	10.2NA	11.4NA
IOZ2	16.5NA	9.90NA	13.4NA	8.10NA
IOZ3	11.0NA	14.5NA	9.40NA	10.6NA
IOZ4	10.1NA	15.9NA	7.40NA	13.4NA
IOZ5	17.3NA	8.90NA	15.1NA	7.10NA
IOZ6	17.4NA	9.30NA	15.2NA	6.90NA
IOZ7	17.5NA	9.20NA	14.6NA	7.10NA
IOZ8	17.2NA	9.20NA	14.5NA	7.20NA
ILDP	3.40UA			
IL1	-5.00UA			
IL2	-5.00UA			
IL3	-5.00UA			
IL4	-5.00UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	225.N	180.N	70.0N
DATA SETUP TIME	(TDS)	32.0N	24.0N	8.00N
DATA HOLD TIME	(TDH)	6.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	18.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	102.N	84.0N	38.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	78.0N	64.0N	32.0N
CS1 SETUP TIME	(TCSS1)	160.N	130.N	62.0N
CS2 SETUP TIME	(TCSS2)	154.N	128.N	60.0N
CS1 HOLD TIME	(TCSH1)	44.0N	38.0N	22.0N
CS2 HOLD TIME	(TCSH2)	46.0N	38.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	202.N	168.N	84.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	200.N	164.N	82.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	42.0N	36.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	130.N	100.N	28.0N
OUTPUT HOLD FROM CS2	(TDOH2)	128.N	100.N	28.0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	112.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	130.N	108.N	30.0N
READ CYCLE TIME	(TRC)	224.N	192.N	104.N
WRITE CYCLE TIME	(TWC)	240.N	184.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-100.PA	100.PA	3.27 V	-3.26 V
A1	-100.PA	100.PA	3.29 V	-3.31 V
A2	-100.PA	100.PA	3.31 V	-3.32 V
A3	-100.PA	100.PA	3.28 V	-3.31 V
A4	-100.PA	100.PA	3.29 V	-3.29 V
A5	-100.PA	100.PA	3.29 V	-3.32 V
A6	-100.PA	100.PA	3.30 V	-3.34 V
A7	-100.PA	100.PA	3.34 V	-3.37 V
CS1	-100.PA	100.PA	3.28 V	-3.28 V
CS2	-100.PA	100.PA	3.31 V	-3.35 V
MWR	-100.PA	100.PA	3.24 V	-3.25 V
MRD	-100.PA	100.PA	3.26 V	-3.27 V
DI0	-100.PA	100.PA	3.44 V	-3.40 V
DI1	-100.PA	100.PA	3.41 V	-3.36 V
DI2	0.00 A	100.PA	3.39 V	-3.33 V
DI3	-100.PA	100.PA	3.38 V	-3.32 V

	DO0	DO1	DOP	DO3
VOL1	80.0MV	85.0MV	85.0MV	85.0MV
VOL2	85.0MV	95.0MV	105.MV	105.MV
VOH1	4.88 V	4.89 V	4.88 V	4.88 V
VOH2	9.84 V	9.84 V	9.83 V	9.84 V
IDN1	9.25MA	8.85MA	8.40MA	8.40MA
IDN2	21.8MA	19.9MA	18.0MA	18.2MA
IDP1	-3.36MA	-3.40MA	-3.38MA	-3.44MA
IDP2	-7.39MA	-7.44MA	-7.31MA	-7.54MA
IOZ1	6.80NA	100.PA	5.10NA	400.PA
IOZ2	5.60NA	-600.PA	5.70NA	-1.30NA
IOZ3	-100.PA	5.70NA	-1.20NA	5.70NA
IOZ4	3.00NA	2.80NA	1.10NA	3.30NA
IOZ5	3.70NA	900.PA	3.80NA	-100.PA
IOZ6	3.60NA	1.30NA	4.00NA	-400.PA
IOZ7	3.80NA	800.PA	4.00NA	-200.PA
IOZ8	3.70NA	1.10NA	4.10NA	-500.PA
ILDP	-200.NA			
IL1	-5.00UA			
IL2	-5.00UA			
IL3	-5.00UA			
IL4	-5.00UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	225.N	200.N	95.0N
DATA SETUP TIME	(TDS)	28.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	120.N	106.N	56.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-16.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	86.0N	78.0N	44.0N
CS1 SETUP TIME	(TCSS1)	180.N	156.N	80.0N
CS2 SETUP TIME	(TCSS2)	174.N	152.N	78.0N
CS1 HOLD TIME	(TCSH1)	58.0N	50.0N	30.0N
CS2 HOLD TIME	(TCSH2)	60.0N	54.0N	30.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	228.N	200.N	106.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	224.N	198.N	104.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	54.0N	50.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	148.N	118.N	38.0N
OUTPUT HOLD FROM CS2	(TDOH2)	146.N	116.N	38.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	34.0N
OUTPUT HOLD FROM MWR	(TPDH)	136.N	114.N	36.0N
READ CYCLE TIME	(TRC)	248.N	224.N	128.N
WRITE CYCLE TIME	(TWC)	232.N	208.N	128.N

	IIL	IIH	VIC1	VIC2
A0	-58.7NA	58.9NA	3.36 V	-3.36 V
A1	-57.5NA	57.2NA	3.38 V	-3.40 V
A2	-52.5NA	51.0NA	3.38 V	-3.41 V
A3	-51.1NA	48.7NA	3.35 V	-3.38 V
A4	-44.8NA	42.5NA	3.32 V	-3.34 V
A5	-70.4NA	68.3NA	3.41 V	-3.44 V
A6	-77.0NA	74.5NA	3.44 V	-3.47 V
A7	-90.2NA	84.6NA	3.49 V	-3.53 V
CS1	-53.1NA	50.9NA	3.35 V	-3.35 V
CS2	-55.0NA	55.7NA	3.39 V	-3.44 V
MWR	-45.2NA	44.5NA	3.26 V	-3.28 V
MRD	-49.7NA	48.2NA	3.31 V	-3.33 V
DI0	-84.5NA	89.0NA	3.62 V	-3.59 V
DI1	-86.0NA	84.4NA	3.58 V	-3.52 V
DI2	-70.5NA	71.8NA	3.54 V	-3.48 V
DI3	-69.1NA	69.6NA	3.52 V	-3.47 V

	D00	D01	D02	D03
VOL1	115.MV	125.MV	135.MV	130.MV
VOL2	130.MV	145.MV	165.MV	165.MV
VOH1	4.81 V	4.81 V	4.80 V	4.81 V
VOH2	9.72 V	9.72 V	9.72 V	9.73 V
IDN1	6.35MA	6.00MA	5.65MA	5.65MA
IDN2	14.6MA	13.1MA	11.7MA	11.8MA
IDP1	-2.05MA	-2.07MA	-2.02MA	-2.09MA
IDP2	-4.57MA	-4.59MA	-4.44MA	-4.63MA
IOZ1	1.45UA	1.37UA	1.21UA	1.10UA
IOZ2	1.46UA	1.36UA	1.22UA	1.09UA
IOZ3	1.45UA	1.38UA	1.21UA	1.11UA
IOZ4	1.46UA	1.37UA	1.22UA	1.10UA
IOZ5	1.47UA	1.41UA	1.24UA	1.15UA
IOZ6	1.48UA	1.41UA	1.23UA	1.12UA
IOZ7	1.47UA	1.40UA	1.23UA	1.12UA
IOZ8	1.48UA	1.39UA	1.23UA	1.11UA

ILDP	13.2UA
IL1	-45.0UA
IL2	-50.0UA
IL3	-50.0UA
IL4	-45.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	245.N	215.N	105.N
DATA SETUP TIME	(TDS)	28.0N	24.0N	10.0N
DATA HOLD TIME	(TDH)	14.0N	14.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	6.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	134.N	118.N	64.0N
ADDRESS HOLD TIME	(TAH)	-20.0N	-18.0N	-6.00N
WRITE PULSE WIDTH	(TWP)	94.0N	84.0N	46.0N
CS1 SETUP TIME	(TCSS1)	190.N	166.N	88.0N
CS2 SETUP TIME	(TCSS2)	188.N	164.N	86.0N
CS1 HOLD TIME	(TCSH1)	60.0N	54.0N	32.0N
CS2 HOLD TIME	(TCSH2)	62.0N	56.0N	30.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	256.N	226.N	122.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	254.N	224.N	122.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	60.0N	54.0N	32.0N
OUTPUT HOLD FROM CS1	(TDOH1)	154.N	124.N	44.0N
OUTPUT HOLD FROM CS2	(TDOH2)	150.N	122.N	44.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	120.N	36.0N
OUTPUT HOLD FROM MWR	(TPDH)	138.N	116.N	38.0N
READ CYCLE TIME	(TRC)	264.N	240.N	128.N
WRITE CYCLE TIME	(TWC)	248.N	224.N	136.N

	IIL	IIH	VIC1	VIC2
A0	-349.NA	346.NA	3.46 V	-3.46 V
A1	-338.NA	329.NA	3.47 V	-3.50 V
A2	-313.NA	299.NA	3.48 V	-3.50 V
A3	-300.NA	284.NA	3.43 V	-3.47 V
A4	-263.NA	248.NA	3.40 V	-3.41 V
A5	-412.NA	399.NA	3.52 V	-3.56 V
A6	-457.NA	438.NA	3.57 V	-3.60 V
A7	-520.NA	498.NA	3.63 V	-3.66 V
CS1	-314.NA	295.NA	3.44 V	-3.44 V
CS2	-325.NA	326.NA	3.48 V	-3.54 V
MWR	-268.NA	252.NA	3.33 V	-3.35 V
MRD	-292.NA	279.NA	3.40 V	-3.41 V
DI0	-504.NA	521.NA	3.76 V	-3.72 V
DI1	-496.NA	499.NA	3.71 V	-3.65 V
DI2	-417.NA	420.NA	3.66 V	-3.61 V
DI3	-412.NA	412.NA	3.65 V	-3.60 V

	DO0	DO1	DO2	DO3
VOL1	130.MV	140.MV	150.MV	150.MV
VOL2	145.MV	165.MV	185.MV	185.MV
VOH1	4.78 V	4.78 V	4.78 V	4.78 V
VOH2	9.69 V	9.69 V	9.68 V	9.69 V
IDN1	5.65MA	5.35MA	5.00MA	5.05MA
IDN2	13.0MA	11.6MA	10.3MA	10.5MA
IDP1	-1.83MA	-1.84MA	-1.83MA	-1.87MA
IDP2	-4.09MA	-4.09MA	-3.99MA	-4.14MA
IOZ1	6.32UA	5.97UA	5.30UA	4.85UA
IOZ2	6.31UA	5.98UA	5.30UA	4.87UA
IOZ3	6.33UA	5.97UA	5.32UA	4.86UA
IOZ4	6.32UA	5.99UA	5.31UA	4.88UA
IOZ5	6.40UA	6.05UA	5.43UA	4.99UA
IOZ6	6.43UA	6.06UA	5.38UA	4.91UA
IOZ7	6.39UA	6.04UA	5.36UA	4.91UA
IOZ8	6.37UA	6.04UA	5.35UA	4.91UA
ILDP	80.0UA			
IL1	-220.UA			
IL2	-240.UA			
IL3	-240.UA			
IL4	-205.UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	335.N	265.N	95.0N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	10.0N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	180.N	142.N	64.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	70.0N	60.0N	36.0N
CS1 SETUP TIME	(TCSS1)	170.N	136.N	66.0N
CS2 SETUP TIME	(TCSS2)	166.N	134.N	64.0N
CS1 HOLD TIME	(TCSH1)	40.0N	34.0N	22.0N
CS2 HOLD TIME	(TCSH2)	42.0N	38.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	314.N	256.N	104.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	312.N	254.N	102.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	52.0N	44.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	148.N	116.N	36.0N
OUTPUT HOLD FROM CS2	(TDOH2)	146.N	114.N	36.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	30.0N
OUTPUT HOLD FROM MWR	(TDOH)	136.N	112.N	32.0N
READ CYCLE TIME	(TRC)	312.N	256.N	112.N
WRITE CYCLE TIME	(TWC)	272.N	208.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-2.00NA	1.90NA	3.02 V	-3.04 V
A1	-1.90NA	1.80NA	3.05 V	-3.09 V
A2	-1.90NA	1.80NA	3.08 V	-3.11 V
A3	-1.90NA	1.60NA	3.10 V	-3.12 V
A4	-1.70NA	1.80NA	3.10 V	-3.14 V
A5	-1.90NA	2.50NA	3.06 V	-3.06 V
A6	-2.10NA	2.00NA	3.05 V	-3.08 V
A7	-2.50NA	2.10NA	3.08 V	-3.10 V
CS1	-1.60NA	2.10NA	3.12 V	-3.11 V
CS2	-2.20NA	1.90NA	3.13 V	-3.15 V
MWR	-2.00NA	1.70NA	3.07 V	-3.05 V
MRD	-2.30NA	1.90NA	3.08 V	-3.10 V
DI0	-2.30NA	2.20NA	3.19 V	-3.13 V
DI1	-2.00NA	2.10NA	3.18 V	-3.13 V
DI2	-2.00NA	2.90NA	3.18 V	-3.17 V
DI3	-2.30NA	1.90NA	3.18 V	-3.13 V

	D00	D01	D02	D03
VOL1	105.MV	110.MV	120.MV	115.MV
VOL2	110.MV	115.MV	135.MV	130.MV
VOH1	4.85 V	4.84 V	4.84 V	4.84 V
VOH2	9.78 V	9.78 V	9.77 V	9.78 V
IDN1	7.10MA	6.75MA	6.25MA	6.35MA
IDN2	17.5MA	16.0MA	14.0MA	14.5MA
IDP1	-2.54MA	-2.48MA	-2.45MA	-2.48MA
IDP2	-5.73MA	-5.66MA	-5.47MA	-5.67MA
IOZ1	29.3NA	23.9NA	29.2NA	20.8NA
IOZ2	25.8NA	26.2NA	25.6NA	23.6NA
IOZ3	28.6NA	23.9NA	26.3NA	23.9NA
IOZ4	31.1NA	21.5NA	29.8NA	21.0NA
IOZ5	24.2NA	28.0NA	24.1NA	26.5NA
IOZ6	24.9NA	28.2NA	23.9NA	25.6NA
IOZ7	24.8NA	27.8NA	24.2NA	25.6NA
IOZ8	24.7NA	27.6NA	24.6NA	25.2NA

ILDP	2.20UA
IL1	-15.0UA
IL2	-20.0UA
IL3	-10.0UA
IL4	-20.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	395.N	285.N	90.0N
DATA SETUP TIME	(TDS)	28.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	194.N	150.N	62.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	70.0N	58.0N	32.0N
CS1 SETUP TIME	(TCSS1)	222.N	132.N	60.0N
CS2 SETUP TIME	(TCSS2)	220.N	130.N	60.0N
CS1 HOLD TIME	(TCSH1)	34.0N	30.0N	22.0N
CS2 HOLD TIME	(TCSH2)	40.0N	32.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	336.N	262.N	98.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	334.N	260.N	98.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	42.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	142.N	112.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	140.N	108.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	136.N	112.N	30.0N
READ CYCLE TIME	(TRC)	312.N	248.N	104.N
WRITE CYCLE TIME	(TWC)	256.N	200.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-300.PA	300.PA	3.10 V	-3.11 V
A1	-300.PA	300.PA	3.12 V	-3.15 V
A2	-300.PA	200.PA	3.14 V	-3.16 V
A3	-300.PA	300.PA	3.16 V	-3.17 V
A4	-200.PA	200.PA	3.16 V	-3.20 V
A5	-300.PA	600.PA	3.13 V	-3.13 V
A6	-400.PA	300.PA	3.12 V	-3.14 V
A7	-400.PA	500.PA	3.13 V	-3.15 V
CS1	-200.PA	500.PA	3.19 V	-3.17 V
CS2	-500.PA	400.PA	3.20 V	-3.21 V
MWR	-300.PA	300.PA	3.14 V	-3.13 V
MRD	-400.PA	400.PA	3.14 V	-3.16 V
DI0	-400.PA	300.PA	3.25 V	-3.19 V
DI1	-300.PA	400.PA	3.24 V	-3.18 V
DI2	-300.PA	600.PA	3.24 V	-3.22 V
DI3	-300.PA	300.PA	3.24 V	-3.18 V

	D00	D01	D02	D03
VOL1	95.0MV	95.0MV	105.MV	105.MV
VOL2	95.0MV	105.MV	120.MV	115.MV
VOH1	4.87 V	4.87 V	4.86 V	4.87 V
VOH2	9.82 V	9.82 V	9.81 V	9.82 V
IDN1	7.85MA	7.45MA	6.95MA	7.05MA
IDN2	19.8MA	18.3MA	16.0MA	16.5MA
IDP1	-2.96MA	-2.95MA	-2.88MA	-2.90MA
IDP2	-6.72MA	-6.69MA	-6.45MA	-6.66MA
IOZ1	9.30NA	2.00NA	6.70NA	2.30NA
IOZ2	8.90NA	600.PA	8.20NA	400.PA
IOZ3	2.30NA	7.60NA	1.20NA	7.80NA
IOZ4	4.70NA	5.10NA	3.10NA	5.70NA
IOZ5	6.80NA	2.40NA	6.80NA	1.00NA
IOZ6	7.10NA	2.00NA	6.80NA	1.20NA
IOZ7	7.10NA	2.60NA	7.00NA	1.00NA
IOZ8	7.10NA	1.80NA	6.80NA	1.10NA

ILDP	-1.40UA
IL1	-15.0UA
IL2	-20.0UA
IL3	-5.00UA
IL4	-15.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	425.N	300.N	85.0N
DATA SETUP TIME	(TDS)	34.0N	24.0N	8.00N
DATA HOLD TIME	(TDH)	6.00N	6.00N	8.00N
ADDRESS SETUP TIME	(TAS1)	16.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	206.N	154.N	60.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	76.0N	66.0N	32.0N
CS1 SETUP TIME	(TCSS1)	242.N	128.N	56.0N
CS2 SETUP TIME	(TCSS2)	242.N	126.N	56.0N
CS1 HOLD TIME	(TCSH1)	42.0N	36.0N	20.0N
CS2 HOLD TIME	(TCSH2)	48.0N	38.0N	18.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	364.N	266.N	96.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	360.N	264.N	94.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	46.0N	40.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	138.N	106.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	136.N	104.N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	114.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	134.N	110.N	30.0N
READ CYCLE TIME	(TRC)	328.N	248.N	104.N
WRITE CYCLE TIME	(TWC)	256.N	176.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-100.PA	100.PA	3.17 V	-3.18 V
A1	-100.PA	100.PA	3.19 V	-3.23 V
A2	-100.PA	100.PA	3.21 V	-3.24 V
A3	-100.PA	100.PA	3.23 V	-3.25 V
A4	-100.PA	100.PA	3.23 V	-3.27 V
A5	-100.PA	300.PA	3.20 V	-3.20 V
A6	-100.PA	100.PA	3.19 V	-3.21 V
A7	-100.PA	200.PA	3.21 V	-3.23 V
CS1	-100.PA	100.PA	3.26 V	-3.24 V
CS2	-100.PA	100.PA	3.27 V	-3.28 V
MWR	-100.PA	100.PA	3.22 V	-3.20 V
MRD	-100.PA	100.PA	3.22 V	-3.23 V
DI0	-100.PA	100.PA	3.32 V	-3.26 V
DI1	-100.PA	100.PA	3.31 V	-3.25 V
DI2	-100.PA	100.PA	3.31 V	-3.29 V
DI3	-100.PA	100.PA	3.32 V	-3.25 V

	D00	D01	D02	D03
VOL1	85.0MV	90.0MV	100.MV	95.0MV
VOL2	85.0MV	95.0MV	105.MV	105.MV
VOH1	4.89 V	4.88 V	4.88 V	4.88 V
VOH2	9.84 V	9.84 V	9.84 V	9.84 V
IDN1	8.45MA	8.10MA	7.55MA	7.65MA
IDN2	21.8MA	20.2MA	17.9MA	18.4MA
IDP1	-3.41MA	-3.38MA	-3.30MA	-3.38MA
IDP2	-7.70MA	-7.68MA	-7.41MA	-7.69MA
IOZ1	-700.PA	5.70NA	-1.00NA	4.90NA
IOZ2	-200.PA	3.80NA	-1.00NA	4.60NA
IOZ3	4.40NA	-1.20NA	4.90NA	-1.90NA
IOZ4	1.10NA	2.20NA	1.80NA	700.PA
IOZ5	2.50NA	1.90NA	700.PA	2.70NA
IOZ6	1.90NA	2.00NA	800.PA	3.00NA
IOZ7	2.10NA	2.20NA	400.PA	3.00NA
IOZ8	1.60NA	2.40NA	500.PA	3.30NA

ILDP	-15.0UA
IL1	-10.0UA
IL2	-15.0UA
IL3	-5.00UA
IL4	-10.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	310.N	255.N	105.N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	10.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	6.00N	6.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	172.N	138.N	68.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	80.0N	70.0N	40.0N
CS1 SETUP TIME	(TCSS1)	166.N	142.N	70.0N
CS2 SETUP TIME	(TCSS2)	164.N	140.N	70.0N
CS1 HOLD TIME	(TCSH1)	50.0N	44.0N	26.0N
CS2 HOLD TIME	(TCSH2)	54.0N	46.0N	26.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	300.N	254.N	114.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	296.N	250.N	114.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	54.0N	48.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	150.N	120.N	40.0N
OUTPUT HOLD FROM CS2	(TDOH2)	148.N	118.N	40.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	34.0N
OUTPUT HOLD FROM MWR	(TPDH)	138.N	114.N	34.0N
READ CYCLE TIME	(TRC)	312.N	264.N	120.N
WRITE CYCLE TIME	(TWC)	224.N	200.N	120.N

	IIL	IIH	VIC1	VIC2
A0	-25.0NA	23.9NA	3.00 V	-3.02 V
A1	-24.4NA	23.0NA	3.03 V	-3.06 V
A2	-24.6NA	23.5NA	3.06 V	-3.09 V
A3	-24.0NA	22.6NA	3.08 V	-3.10 V
A4	-23.7NA	24.1NA	3.08 V	-3.12 V
A5	-25.4NA	25.1NA	3.05 V	-3.04 V
A6	-25.0NA	24.6NA	3.03 V	-3.06 V
A7	-27.6NA	25.3NA	3.05 V	-3.08 V
CS1	-23.9NA	24.1NA	3.11 V	-3.09 V
CS2	-25.4NA	24.9NA	3.12 V	-3.14 V
MWR	-23.6NA	23.6NA	3.04 V	-3.03 V
MRD	-25.1NA	23.4NA	3.05 V	-3.08 V
DI0	-25.3NA	26.4NA	3.17 V	-3.12 V
DI1	-24.8NA	24.8NA	3.17 V	-3.12 V
DI2	-24.3NA	27.0NA	3.17 V	-3.15 V
DI3	-24.8NA	24.2NA	3.17 V	-3.11 V

	D00	D01	D02	D03
VOL1	120.MV	125.MV	140.MV	135.MV
VOL2	125.MV	140.MV	160.MV	155.MV
VOH1	4.82 V	4.82 V	4.81 V	4.81 V
VOH2	9.74 V	9.74 V	9.72 V	9.74 V
IDN1	6.20MA	5.85MA	5.40MA	5.50MA
IDN2	15.1MA	13.7MA	11.9MA	12.4MA
IDP1	-2.15MA	-2.11MA	-2.06MA	-2.10MA
IDP2	-4.86MA	-4.77MA	-4.63MA	-4.79MA
IOZ1	232.NA	223.NA	219.NA	224.NA
IOZ2	222.NA	228.NA	219.NA	218.NA
IOZ3	225.NA	225.NA	218.NA	220.NA
IOZ4	219.NA	224.NA	221.NA	214.NA
IOZ5	221.NA	228.NA	222.NA	222.NA
IOZ6	229.NA	219.NA	233.NA	215.NA
IOZ7	231.NA	224.NA	219.NA	227.NA
IOZ8	222.NA	225.NA	225.NA	215.NA
ILDP	3.20UA			
IL1	-35.0UA			
IL2	-45.0UA			
IL3	-25.0UA			
IL4	-35.0UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	305.N	255.N	110.N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	4.00N	4.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	170.N	148.N	72.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	84.0N	76.0N	44.0N
CS1 SETUP TIME	(TCSS1)	170.N	150.N	78.0N
CS2 SETUP TIME	(TCSS2)	166.N	146.N	76.0N
CS1 HOLD TIME	(TCSH1)	52.0N	46.0N	28.0N
CS2 HOLD TIME	(TCSH2)	54.0N	48.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	306.N	262.N	126.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	304.N	258.N	122.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	58.0N	52.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	152.N	122.N	42.0N
OUTPUT HOLD FROM CS2	(TDOH2)	148.N	120.N	42.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	34.0N
OUTPUT HOLD FROM MWR	(TPDH)	140.N	116.N	38.0N
READ CYCLE TIME	(TRC)	312.N	264.N	128.N
WRITE CYCLE TIME	(TWC)	224.N	208.N	128.N

	IIL	IIH	VIC1	VIC2
A0	-144.NA	138.NA	3.00 V	-3.02 V
A1	-144.NA	137.NA	3.03 V	-3.07 V
A2	-144.NA	137.NA	3.07 V	-3.10 V
A3	-140.NA	135.NA	3.09 V	-3.11 V
A4	-140.NA	138.NA	3.08 V	-3.13 V
A5	-145.NA	139.NA	3.05 V	-3.04 V
A6	-147.NA	143.NA	3.04 V	-3.06 V
A7	-152.NA	143.NA	3.06 V	-3.09 V
CS1	-143.NA	137.NA	3.11 V	-3.09 V
CS2	-146.NA	141.NA	3.13 V	-3.14 V
MWR	-139.NA	135.NA	3.04 V	-3.03 V
MRD	-142.NA	135.NA	3.05 V	-3.08 V
DI0	-145.NA	146.NA	3.19 V	-3.13 V
DI1	-143.NA	143.NA	3.18 V	-3.13 V
DI2	-142.NA	143.NA	3.17 V	-3.16 V
DI3	-140.NA	140.NA	3.17 V	-3.12 V

	DO0	DO1	DO2	DO3
VOL1	130.MV	140.MV	155.MV	150.MV
VOL2	140.MV	155.MV	180.MV	175.MV
VOH1	4.80 V	4.80 V	4.78 V	4.79 V
VOH2	9.72 V	9.70 V	9.69 V	9.71 V
IDN1	5.60MA	5.30MA	4.85MA	4.95MA
IDN2	13.5MA	12.2MA	10.6MA	11.1MA
IDP1	-1.94MA	-1.91MA	-1.87MA	-1.91MA
IDP2	-4.36MA	-4.30MA	-4.15MA	-4.31MA
IOZ1	895.NA	890.NA	885.NA	884.NA
IOZ2	877.NA	883.NA	883.NA	875.NA
IOZ3	875.NA	884.NA	878.NA	879.NA
IOZ4	872.NA	875.NA	883.NA	873.NA
IOZ5	880.NA	888.NA	895.NA	890.NA
IOZ6	889.NA	878.NA	892.NA	884.NA
IOZ7	883.NA	883.NA	881.NA	886.NA
IOZ8	879.NA	877.NA	891.NA	875.NA
ILDP	40.0UA			
IL1	-105.UA			
IL2	-135.UA			
IL3	-95.0UA			
IL4	-95.0UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	230.N	195.N	80.0N
DATA SETUP TIME	(TDS)	18.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	14.0N	14.0N	16.0N
ADDRESS SETUP TIME	(TAS1)	10.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	114.N	96.0N	44.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	62.0N	56.0N	34.0N
CS1 SETUP TIME	(TCSS1)	150.N	130.N	66.0N
CS2 SETUP TIME	(TCSS2)	148.N	128.N	64.0N
CS1 HOLD TIME	(TCSH1)	34.0N	30.0N	22.0N
CS2 HOLD TIME	(TCSH2)	38.0N	32.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	224.N	190.N	88.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	224.N	188.N	88.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	48.0N	42.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	142.N	112.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	138.N	108.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	134.N	110.N	32.0N
READ CYCLE TIME	(TRC)	256.N	208.N	112.N
WRITE CYCLE TIME	(TWC)	208.N	176.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-1.10NA	900.PA	2.86 V	-2.83 V
A1	-1.40NA	1.30NA	2.87 V	-2.89 V
A2	-1.00NA	1.40NA	2.86 V	-2.89 V
A3	-1.30NA	1.50NA	2.83 V	-2.88 V
A4	-1.00NA	1.70NA	2.88 V	-2.91 V
A5	-1.20NA	1.00NA	2.81 V	-2.85 V
A6	-1.50NA	1.30NA	2.80 V	-2.83 V
A7	-1.20NA	1.30NA	2.80 V	-2.85 V
CS1	-1.00NA	1.30NA	2.83 V	-2.84 V
CS2	-1.30NA	1.10NA	2.86 V	-2.86 V
MWR	-1.40NA	900.PA	2.81 V	-2.81 V
MRD	-1.60NA	1.00NA	2.84 V	-2.83 V
DI0	-1.60NA	1.00NA	2.89 V	-2.84 V
DI1	-1.10NA	1.00NA	2.88 V	-2.83 V
DI2	-1.50NA	1.10NA	2.89 V	-2.83 V
DI3	-1.20NA	1.50NA	2.89 V	-2.85 V

	DO0	DO1	DO2	DO3
VOL1	105.MV	115.MV	120.MV	120.MV
VOL2	110.MV	125.MV	140.MV	140.MV
VOH1	4.86 V	4.86 V	4.85 V	4.85 V
VOH2	9.78 V	9.78 V	9.77 V	9.78 V
IDN1	6.90MA	6.55MA	6.20MA	6.20MA
IDN2	17.0MA	15.4MA	13.6MA	13.8MA
IDP1	-2.67MA	-2.64MA	-2.63MA	-2.64MA
IDP2	-5.72MA	-5.72MA	-5.55MA	-5.73MA
IOZ1	25.0NA	17.0NA	22.9NA	16.3NA
IOZ2	21.2NA	19.6NA	19.7NA	18.5NA
IOZ3	22.3NA	19.5NA	18.3NA	20.5NA
IOZ4	26.0NA	16.5NA	22.2NA	17.4NA
IOZ5	19.3NA	21.7NA	18.0NA	21.6NA
IOZ6	19.8NA	22.2NA	18.0NA	21.1NA
IOZ7	19.7NA	21.6NA	17.9NA	21.3NA
IOZ8	19.7NA	22.0NA	17.9NA	20.8NA

ILDP	-20.0UA
IL1	-30.0UA
IL2	-40.0UA
IL3	-75.0UA
IL4	-80.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	235.N	190.N	75.0N
DATA SETUP TIME	(TDS)	20.0N	16.0N	6.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	16.0N
ADDRESS SETUP TIME	(TAS1)	12.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	112.N	92.0N	40.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	60.0N	60.0N	32.0N
CS1 SETUP TIME	(TCSS1)	142.N	122.N	62.0N
CS2 SETUP TIME	(TCSS2)	140.N	120.N	60.0N
CS1 HOLD TIME	(TCSH1)	34.0N	30.0N	20.0N
CS2 HOLD TIME	(TCSH2)	36.0N	32.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	218.N	180.N	80.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	218.N	178.N	80.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	42.0N	38.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	134.N	104.N	32.0N
OUTPUT HOLD FROM CS2	(TDOH2)	132.N	102.N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	114.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	110.N	30.0N
READ CYCLE TIME	(TRC)	224.N	200.N	96.0N
WRITE CYCLE TIME	(TWC)	200.N	168.N	104.N

	IIL	IIH	VIC1	VIC2
A0	-200.PA	100.PA	3.00 V	-2.96 V
A1	-200.PA	200.PA	3.00 V	-3.02 V
A2	-200.PA	200.PA	2.99 V	-3.02 V
A3	-200.PA	200.PA	2.97 V	-2.99 V
A4	-200.PA	400.PA	3.01 V	-3.05 V
A5	-200.PA	100.PA	2.96 V	-2.98 V
A6	-300.PA	200.PA	2.94 V	-2.97 V
A7	-300.PA	200.PA	2.94 V	-2.98 V
CS1	-200.PA	300.PA	2.97 V	-2.98 V
CS2	-200.PA	200.PA	2.99 V	-2.98 V
MWR	-200.PA	100.PA	2.95 V	-2.95 V
MRD	-300.PA	200.PA	2.98 V	-2.96 V
DI0	-300.PA	200.PA	3.03 V	-2.97 V
DI1	-200.PA	200.PA	3.02 V	-2.96 V
DI2	-200.PA	200.PA	3.03 V	-2.96 V
DI3	-300.PA	200.PA	3.03 V	-2.97 V

	D00	D01	D02	D03
VOL1	95.0MV	100.MV	105.MV	105.MV
VOL2	95.0MV	105.MV	120.MV	120.MV
VOH1	4.88 V	4.88 V	4.88 V	4.88 V
VOH2	9.82 V	9.82 V	9.81 V	9.82 V
IDN1	7.85MA	7.45MA	7.05MA	7.05MA
IDN2	19.6MA	17.8MA	15.8MA	16.0MA
IDP1	-3.17MA	-3.17MA	-3.11MA	-3.13MA
IDP2	-6.80MA	-6.82MA	-6.55MA	-6.82MA
IOZ1	6.20NA	1.40NA	5.10NA	700.PA
IOZ2	2.40NA	4.40NA	1.70NA	3.70NA
IOZ3	5.70NA	1.80NA	3.50NA	2.90NA
IOZ4	8.10NA	-300.PA	7.00NA	-100.PA
IOZ5	1.20NA	7.10NA	-200.PA	6.00NA
IOZ6	1.20NA	6.80NA	-200.PA	6.30NA
IOZ7	1.20NA	7.00NA	-200.PA	6.10NA
IOZ8	1.20NA	6.80NA	-200.PA	6.20NA
ILDP	2.00UA			
IL1	-25.0UA			
IL2	-35.0UA			
IL3	-75.0UA			
IL4	-75.0UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	230.N	180.N	70.0N
DATA SETUP TIME	(TDS)	24.0N	18.0N	6.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	10.0N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	110.N	88.0N	36.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	72.0N	60.0N	30.0N
CS1 SETUP TIME	(TCSS1)	136.N	118.N	56.0N
CS2 SETUP TIME	(TCSS2)	136.N	116.N	54.0N
CS1 HOLD TIME	(TCSH1)	42.0N	30.0N	20.0N
CS2 HOLD TIME	(TCSH2)	46.0N	34.0N	18.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	226.N	176.N	80.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	224.N	174.N	78.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	40.0N	36.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	130.N	100.N	32.0N
OUTPUT HOLD FROM CS2	(TDOH2)	128.N	98.0N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	112.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	130.N	108.N	28.0N
READ CYCLE TIME	(TRC)	216.N	184.N	88.0N
WRITE CYCLE TIME	(TWC)	200.N	168.N	96.0N

	IIL	IIH	VIC1	VTC2
A0	0.00 A	0.00 A	3.12 V	-3.08 V
A1	-100.PA	100.PA	3.12 V	-3.14 V
A2	-100.PA	100.PA	3.12 V	-3.14 V
A3	0.00 A	100.PA	3.10 V	-3.12 V
A4	0.00 A	100.PA	3.13 V	-3.16 V
A5	0.00 A	100.PA	3.08 V	-3.10 V
A6	-100.PA	100.PA	3.06 V	-3.09 V
A7	-100.PA	100.PA	3.06 V	-3.10 V
CS1	-100.PA	100.PA	3.09 V	-3.10 V
CS2	-100.PA	100.PA	3.11 V	-3.10 V
MWR	-100.PA	0.00 A	3.08 V	-3.08 V
MRD	-100.PA	100.PA	3.10 V	-3.08 V
DI0	-100.PA	100.PA	3.14 V	-3.09 V
DI1	0.00 A	100.PA	3.14 V	-3.09 V
DI2	-100.PA	0.00 A	3.15 V	-3.08 V
DI3	-100.PA	100.PA	3.15 V	-3.09 V

	DO0	DO1	DO2	DO3
VOL1	85.0MV	90.0MV	95.0MV	95.0MV
VOL2	85.0MV	95.0MV	105.MV	105.MV
VOH1	4.89 V	4.89 V	4.89 V	4.89 V
VOH2	9.84 V	9.84 V	9.84 V	9.85 V
IDN1	8.65MA	8.25MA	7.80MA	7.80MA
IDN2	21.7MA	19.8MA	17.8MA	18.0MA
IDP1	-3.60MA	-3.65MA	-3.61MA	-3.63MA
IDP2	-7.76MA	-7.86MA	-7.59MA	-7.84MA
IOZ1	6.10NA	-1.80NA	5.30NA	-1.50NA
IOZ2	2.90NA	-300.PA	3.00NA	-700.PA
IOZ3	-100.PA	2.80NA	-800.PA	3.90NA
IOZ4	4.00NA	-500.PA	2.70NA	600.PA
IOZ5	200.PA	2.60NA	600.PA	1.40NA
IOZ6	400.PA	2.10NA	600.PA	1.60NA
IOZ7	400.PA	2.40NA	800.PA	1.20NA
IOZ8	600.PA	1.80NA	900.PA	1.40NA

ILDP	-200.NA
IL1	-25.0UA
IL2	-35.0UA
IL3	-75.0UA
IL4	-75.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	240.N	205.N	90.0N
DATA SETUP TIME	(TDS)	18.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	18.0N	16.0N	18.0N
ADDRESS SETUP TIME	(TAS1)	6.00N	6.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	120.N	98.0N	50.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-14.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	72.0N	64.0N	38.0N
CS1 SETUP TIME	(TCSS1)	158.N	140.N	72.0N
CS2 SETUP TIME	(TCSS2)	156.N	136.N	72.0N
CS1 HOLD TIME	(TCSH1)	44.0N	40.0N	26.0N
CS2 HOLD TIME	(TCSH2)	48.0N	42.0N	26.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	236.N	200.N	98.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	234.N	198.N	98.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	52.0N	46.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	148.N	116.N	38.0N
OUTPUT HOLD FROM CS2	(TDOH2)	144.N	114.N	38.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	34.0N
OUTPUT HOLD FROM MWR	(TPDH)	136.N	114.N	32.0N
READ CYCLE TIME	(TRC)	264.N	224.N	112.N
WRITE CYCLE TIME	(TWC)	208.N	184.N	128.N

	IIL	IIH	VIC1	VIC2
A0	-14.8NA	17.1NA	2.76 V	-2.73 V
A1	-16.3NA	18.0NA	2.77 V	-2.80 V
A2	-14.9NA	17.7NA	2.76 V	-2.80 V
A3	-15.9NA	18.2NA	2.73 V	-2.76 V
A4	-14.8NA	19.3NA	2.78 V	-2.83 V
A5	-15.3NA	18.7NA	2.72 V	-2.75 V
A6	-16.3NA	20.5NA	2.70 V	-2.73 V
A7	-16.0NA	21.7NA	2.70 V	-2.75 V
CS1	-16.0NA	22.2NA	2.73 V	-2.74 V
CS2	-19.3NA	22.7NA	2.75 V	-2.76 V
MWR	-17.8NA	17.6NA	2.72 V	-2.72 V
MRD	-20.4NA	19.4NA	2.74 V	-2.73 V
DI0	-19.9NA	27.4NA	2.79 V	-2.74 V
DI1	-18.8NA	27.2NA	2.78 V	-2.73 V
DI2	-22.0NA	27.1NA	2.80 V	-2.73 V
DI3	-21.0NA	28.2NA	2.79 V	-2.75 V

	DO0	DO1	DO2	DO3
VOL1	125.MV	135.MV	145.MV	140.MV
VOL2	135.MV	150.MV	170.MV	165.MV
VOH1	4.82 V	4.82 V	4.82 V	4.82 V
VOH2	9.74 V	9.74 V	9.73 V	9.74 V
IDN1	5.85MA	5.55MA	5.25MA	5.25MA
IDN2	14.2MA	12.8MA	11.3MA	11.6MA
IDP1	-2.23MA	-2.20MA	-2.18MA	-2.21MA
IDP2	-4.81MA	-4.80MA	-4.64MA	-4.81MA
IOZ1	235.NA	211.NA	235.NA	221.NA
IOZ2	233.NA	208.NA	226.NA	225.NA
IOZ3	230.NA	205.NA	228.NA	221.NA
IOZ4	225.NA	209.NA	220.NA	227.NA
IOZ5	230.NA	210.NA	228.NA	228.NA
IOZ6	220.NA	220.NA	224.NA	222.NA
IOZ7	225.NA	206.NA	233.NA	217.NA
IOZ8	225.NA	212.NA	222.NA	227.NA

ILDP	9.00UA
IL1	-45.0UA
IL2	-65.0UA
IL3	-100.UA
IL4	-100.UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	255.N	220.N	100.N
DATA SETUP TIME	(TDS)	20.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	20.0N	20.0N	20.0N
ADDRESS SETUP TIME	(TAS1)	4.00N	4.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	128.N	106.N	58.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	78.0N	70.0N	42.0N
CS1 SETUP TIME	(TCSS1)	172.N	150.N	80.0N
CS2 SETUP TIME	(TCSS2)	168.N	148.N	78.0N
CS1 HOLD TIME	(TCSH1)	46.0N	42.0N	28.0N
CS2 HOLD TIME	(TCSH2)	50.0N	46.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	258.N	220.N	110.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	256.N	218.N	106.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	56.0N	50.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	152.N	122.N	42.0N
OUTPUT HOLD FROM CS2	(TDOH2)	148.N	118.N	42.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	120.N	36.0N
OUTPUT HOLD FROM MWR	(TPDH)	140.N	116.N	38.0N
READ CYCLE TIME	(TRC)	288.N	240.N	128.N
WRITE CYCLE TIME	(TWC)	216.N	200.N	136.N

	IIL	IIH	VIC1	VIC2
A0	-88.4NA	90.6NA	2.68 V	-2.65 V
A1	-91.8NA	91.4NA	2.69 V	-2.73 V
A2	-90.0NA	92.1NA	2.69 V	-2.72 V
A3	-91.5NA	90.7NA	2.66 V	-2.69 V
A4	-91.2NA	94.9NA	2.71 V	-2.75 V
A5	-90.3NA	93.3NA	2.64 V	-2.67 V
A6	-91.9NA	94.5NA	2.63 V	-2.65 V
A7	-94.5NA	98.8NA	2.63 V	-2.67 V
CS1	-98.2NA	97.4NA	2.65 V	-2.67 V
CS2	-99.9NA	101.NA	2.67 V	-2.69 V
MWR	-95.8NA	90.5NA	2.64 V	-2.64 V
MRD	-101.NA	91.8NA	2.66 V	-2.66 V
DI0	-100.NA	104.NA	2.72 V	-2.66 V
DI1	-94.9NA	103.NA	2.71 V	-2.66 V
DI2	-102.NA	103.NA	2.72 V	-2.66 V
DI3	-100.NA	106.NA	2.72 V	-2.67 V

	D00	D01	D02	D03
VOL1	140.MV	150.MV	160.MV	160.MV
VOL2	150.MV	165.MV	190.MV	185.MV
VOH1	4.80 V	4.80 V	4.80 V	4.80 V
VOH2	9.71 V	9.71 V	9.70 V	9.70 V
IDN1	5.25MA	4.95MA	4.70MA	4.70MA
IDN2	12.7MA	11.4MA	10.1MA	10.3MA
IDP1	-2.00MA	-2.00MA	-1.96MA	-1.99MA
IDP2	-4.31MA	-4.33MA	-4.16MA	-4.30MA
IOZ1	949.NA	915.NA	973.NA	932.NA
IOZ2	936.NA	899.NA	974.NA	926.NA
IOZ3	927.NA	901.NA	967.NA	926.NA
IOZ4	925.NA	888.NA	967.NA	923.NA
IOZ5	936.NA	905.NA	989.NA	948.NA
IOZ6	946.NA	906.NA	974.NA	947.NA
IOZ7	932.NA	910.NA	972.NA	937.NA
IOZ8	934.NA	895.NA	975.NA	932.NA
ILDP	40.0UA			
IL1	-105.UA			
IL2	-145.UA			
IL3	-180.UA			
IL4	-165.UA			

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN: 25

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

FAILED DATA RETENTION TEST ADD = 51 DIAG = 34 PIN: 002

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	210.N	180.N	75.0N
DATA SETUP TIME	(TDS)	22.0N	18.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	10.0N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	102.N	88.0N	42.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-10.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	62.0N	54.0N	32.0N
CS1 SETUP TIME	(TCSS1)	146.N	126.N	62.0N
CS2 SETUP TIME	(TCSS2)	142.N	122.N	60.0N
CS1 HOLD TIME	(TCSH1)	40.0N	36.0N	24.0N
CS2 HOLD TIME	(TCSH2)	42.0N	38.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	202.N	174.N	82.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	200.N	170.N	82.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	46.0N	40.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	138.N	108.N	32.0N
OUTPUT HOLD FROM CS2	(TDOH2)	134.N	106.N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	114.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	130.N	110.N	30.0N
READ CYCLE TIME	(TRC)	224.N	200.N	96.0N
WRITE CYCLE TIME	(TWC)	224.N	176.N	104.N

	IIL	IIH	VIC1	VIC2
A0	-2.00NA	3.90NA	2.94 V	-2.93 V
A1	-2.60NA	2.20NA	2.97 V	-2.99 V
A2	-2.10NA	1.90NA	3.00 V	-3.02 V
A3	-1.90NA	2.00NA	2.99 V	-3.00 V
A4	-2.10NA	1.80NA	3.02 V	-3.02 V
A5	-2.30NA	2.00NA	2.91 V	-2.93 V
A6	-2.00NA	2.10NA	2.88 V	-2.91 V
A7	-2.20NA	2.10NA	2.89 V	-2.92 V
CS1	-2.20NA	1.80NA	2.94 V	-2.95 V
CS2	-2.70NA	2.20NA	2.97 V	-3.00 V
MWR	-2.60NA	2.20NA	2.94 V	-2.95 V
MRD	-1.90NA	2.40NA	2.94 V	-2.94 V
DI0	-2.50NA	1.90NA	2.97 V	-2.94 V
DI1	-1.80NA	2.90NA	2.96 V	-2.91 V
DI2	-2.20NA	2.10NA	2.98 V	-2.94 V
DI3	-2.50NA	1.80NA	2.96 V	-2.94 V

	D00	D01	D02	D03
VOL1	90.0MV	95.0MV	105.MV	105.MV
VOL2	95.0MV	110.MV	130.MV	125.MV
VOH1	4.86 V	4.86 V	4.86 V	4.86 V
VOH2	9.80 V	9.80 V	9.80 V	9.80 V
IDN1	8.15MA	7.60MA	6.90MA	7.05MA
IDN2	19.6MA	17.4MA	14.9MA	15.5MA
IDP1	-2.83MA	-2.81MA	-2.71MA	-2.83MA
IDP2	-6.26MA	-6.23MA	-5.94MA	-6.31MA
IOZ1	34.0NA	39.1NA	33.1NA	36.1NA
IOZ2	36.7NA	35.0NA	36.6NA	32.6NA
IOZ3	33.1NA	37.9NA	35.1NA	32.8NA
IOZ4	31.4NA	40.6NA	32.4NA	36.4NA
IOZ5	38.5NA	33.6NA	39.2NA	31.3NA
IOZ6	38.8NA	34.4NA	39.5NA	30.9NA
IOZ7	38.8NA	34.3NA	38.9NA	30.8NA
IOZ8	38.6NA	34.2NA	39.0NA	30.7NA

ILDP	-10.0UA
IL1	-160.UA
IL2	-180.UA
IL3	-25.0UA
IL4	-40.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

FAILED DATA RETENTION TEST ADD = 51 DIAG = 34 PIN: 002

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	220.N	180.N	70.0N
DATA SETUP TIME	(TDS)	24.0N	18.0N	6.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	104.N	84.0N	38.0N
ADDRESS HOLD TIME	(TAH)	-12.0N	-10.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	60.0N	52.0N	32.0N
CS1 SETUP TIME	(TCSS1)	144.N	120.N	58.0N
CS2 SETUP TIME	(TCSS2)	142.N	118.N	56.0N
CS1 HOLD TIME	(TCSH1)	36.0N	32.0N	22.0N
CS2 HOLD TIME	(TCSH2)	38.0N	32.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	206.N	168.N	80.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	204.N	166.N	78.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	42.0N	38.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	132.N	104.N	32.0N
OUTPUT HOLD FROM CS2	(TDOH2)	130.N	102.N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	112.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	128.N	108.N	28.0N
READ CYCLE TIME	(TRC)	216.N	192.N	88.0N
WRITE CYCLE TIME	(TWC)	208.N	168.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-300.PA	1.10NA	3.03 V	-3.02 V
A1	-600.PA	500.PA	3.06 V	-3.08 V
A2	-300.PA	400.PA	3.10 V	-3.11 V
A3	-300.PA	300.PA	3.09 V	-3.10 V
A4	-400.PA	200.PA	3.11 V	-3.11 V
A5	-400.PA	300.PA	3.01 V	-3.02 V
A6	-400.PA	400.PA	2.97 V	-3.01 V
A7	-500.PA	300.PA	2.99 V	-3.01 V
CS1	-400.PA	300.PA	3.04 V	-3.04 V
CS2	-500.PA	800.PA	3.06 V	-3.09 V
MWR	-500.PA	400.PA	3.04 V	-3.03 V
MRD	-300.PA	500.PA	3.03 V	-3.03 V
DI0	-500.PA	300.PA	3.07 V	-3.03 V
DI1	-300.PA	700.PA	3.06 V	-3.01 V
DI2	-500.PA	400.PA	3.08 V	-3.03 V
DI3	-500.PA	300.PA	3.05 V	-3.03 V

	D00	D01	D02	D03
VOL1	80.0MV	85.0MV	95.0MV	90.0MV
VOL2	85.0MV	95.0MV	110.MV	105.MV
VOH1	4.88 V	4.88 V	4.88 V	4.88 V
VOH2	9.84 V	9.84 V	9.83 V	9.84 V
IDN1	9.10MA	8.50MA	7.80MA	7.95MA
IDN2	22.3MA	19.9MA	17.2MA	17.8MA
IDP1	-3.30MA	-3.33MA	-3.22MA	-3.30MA
IDP2	-7.31MA	-7.35MA	-7.01MA	-7.39MA
IOZ1	7.10NA	4.80NA	5.30NA	4.90NA
IOZ2	9.00NA	2.10NA	9.00NA	1.70NA
IOZ3	1.70NA	9.20NA	2.00NA	8.10NA
IOZ4	3.00NA	7.50NA	2.50NA	7.40NA
IOZ5	7.40NA	2.60NA	8.20NA	1.40NA
IOZ6	7.60NA	2.50NA	8.20NA	1.40NA
IOZ7	7.50NA	2.50NA	8.30NA	1.20NA
IOZ8	7.60NA	2.20NA	8.20NA	1.40NA

ILDP	-2.80UA
IL1	-165.UA
IL2	-180.UA
IL3	-20.0UA
IL4	-35.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

FAILED DATA RETENTION TEST ADD = 51 DIAG = 34 PTN: 002

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	220.N	175.N	65.0N
DATA SETUP TIME	(TDS)	32.0N	22.0N	6.00N
DATA HOLD TIME	(TDH)	6.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	14.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	100.N	82.0N	34.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-10.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	76.0N	52.0N	30.0N
CS1 SETUP TIME	(TCSS1)	142.N	122.N	54.0N
CS2 SETUP TIME	(TCSS2)	144.N	116.N	54.0N
CS1 HOLD TIME	(TCSH1)	46.0N	34.0N	20.0N
CS2 HOLD TIME	(TCSH2)	46.0N	38.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	208.N	166.N	78.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	206.N	162.N	76.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	40.0N	34.0N	20.0N
OUTPUT HOLD FROM CS1	(TDOH1)	128.N	98.0N	30.0N
OUTPUT HOLD FROM CS2	(TDOH2)	126.N	96.0N	30.0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	112.N	26.0N
OUTPUT HOLD FROM MWR	(TPDH)	128.N	106.N	28.0N
READ CYCLE TIME	(TRC)	216.N	184.N	88.0N
WRITE CYCLE TIME	(TWC)	216.N	160.N	88.0N

	IIL	IIH	VIC1	VIC2
A0	-100.PA	400.PA	3.13 V	-3.11 V
A1	-200.PA	100.PA	3.15 V	-3.17 V
A2	-100.PA	100.PA	3.18 V	-3.20 V
A3	-100.PA	100.PA	3.18 V	-3.18 V
A4	-100.PA	100.PA	3.20 V	-3.19 V
A5	-100.PA	100.PA	3.11 V	-3.12 V
A6	-100.PA	100.PA	3.06 V	-3.11 V
A7	-100.PA	100.PA	3.09 V	-3.10 V
CS1	-100.PA	100.PA	3.13 V	-3.13 V
CS2	-100.PA	200.PA	3.15 V	-3.18 V
MWR	-100.PA	100.PA	3.13 V	-3.13 V
MRD	-100.PA	100.PA	3.13 V	-3.12 V
DI0	-100.PA	100.PA	3.16 V	-3.13 V
DI1	-100.PA	200.PA	3.15 V	-3.10 V
DI2	-200.PA	100.PA	3.17 V	-3.12 V
DI3	-100.PA	100.PA	3.15 V	-3.13 V

	D00	D01	D02	D03
VOL1	75.0MV	80.0MV	85.0MV	85.0MV
VOL2	75.0MV	85.0MV	100.MV	95.0MV
VOH1	4.90 V	4.90 V	4.90 V	4.90 V
VOH2	9.85 V	9.86 V	9.85 V	9.85 V
IDN1	9.95MA	9.35MA	8.55MA	8.70MA
IDN2	24.7MA	22.2MA	19.3MA	19.9MA
IDP1	-3.79MA	-3.80MA	-3.73MA	-3.83MA
IDP2	-8.35MA	-8.41MA	-8.06MA	-8.50MA
IOZ1	700.PA	3.60NA	1.00NA	2.00NA
IOZ2	-1.20NA	5.70NA	-1.70NA	5.50NA
IOZ3	5.70NA	-2.00NA	5.50NA	-1.60NA
IOZ4	2.70NA	300.PA	3.20NA	-400.PA
IOZ5	600.PA	3.30NA	-400.PA	4.00NA
IOZ6	1.00NA	3.30NA	-500.PA	3.70NA
IOZ7	900.PA	3.00NA	-100.PA	3.70NA
IOZ8	1.30NA	2.90NA	-200.PA	3.40NA

ILDP	-20.0UA
IL1	-175.UA
IL2	-190.UA
IL3	-15.0UA
IL4	-30.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

FAILED DATA RETENTION TEST ADD = 51 DIAG = 34 PIN: 002

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	205.N	180.N	80.0N
DATA SETUP TIME	(TDS)	22.0N	18.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	106.N	94.0N	48.0N
ADDRESS HOLD TIME	(TAH)	-12.0N	-10.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	72.0N	64.0N	38.0N
CS1 SETUP TIME	(TCSS1)	150.N	128.N	66.0N
CS2 SETUP TIME	(TCSS2)	146.N	126.N	64.0N
CS1 HOLD TIME	(TCSH1)	46.0N	42.0N	26.0N
CS2 HOLD TIME	(TCSH2)	50.0N	44.0N	26.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	206.N	180.N	90.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	202.N	178.N	90.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	48.0N	42.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	140.N	110.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	136.N	108.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	114.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	110.N	30.0N
READ CYCLE TIME	(TRC)	232.N	200.N	112.N
WRITE CYCLE TIME	(TWC)	200.N	176.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-22.0NA	28.9NA	2.91 V	-2.90 V
A1	-24.0NA	22.8NA	2.95 V	-2.97 V
A2	-22.6NA	22.3NA	2.97 V	-3.00 V
A3	-21.8NA	22.8NA	2.96 V	-2.98 V
A4	-23.0NA	21.7NA	2.99 V	-3.00 V
A5	-23.4NA	22.1NA	2.89 V	-2.91 V
A6	-21.6NA	22.3NA	2.86 V	-2.89 V
A7	-21.6NA	21.8NA	2.87 V	-2.89 V
CS1	-24.1NA	20.8NA	2.92 V	-2.93 V
CS2	-22.7NA	22.6NA	2.94 V	-2.98 V
MWR	-23.4NA	22.6NA	2.92 V	-2.93 V
MRD	-21.8NA	23.2NA	2.91 V	-2.92 V
DI0	-22.2NA	21.1NA	2.95 V	-2.91 V
DI1	-20.1NA	23.6NA	2.94 V	-2.89 V
DI2	-20.5NA	21.2NA	2.96 V	-2.91 V
DI3	-20.6NA	20.1NA	2.94 V	-2.92 V

	DO0	DO1	DO2	DO3
VOL1	105.MV	110.MV	125.MV	120.MV
VOL2	115.MV	130.MV	150.MV	145.MV
VOH1	4.84 V	4.84 V	4.84 V	4.84 V
VOH2	9.77 V	9.77 V	9.76 V	9.77 V
IDN1	7.10MA	6.60MA	6.00MA	6.15MA
IDN2	16.8MA	14.9MA	12.7MA	13.3MA
IDP1	-2.40MA	-2.37MA	-2.33MA	-2.41MA
IDP2	-5.31MA	-5.30MA	-5.06MA	-5.37MA
IOZ1	316.NA	305.NA	305.NA	280.NA
IOZ2	318.NA	303.NA	300.NA	287.NA
IOZ3	314.NA	302.NA	303.NA	283.NA
IOZ4	316.NA	304.NA	298.NA	292.NA
IOZ5	319.NA	306.NA	306.NA	297.NA
IOZ6	314.NA	321.NA	298.NA	292.NA
IOZ7	312.NA	309.NA	308.NA	284.NA
IOZ8	318.NA	308.NA	300.NA	294.NA

ILDP	3.00UA
IL1	-180.UA
IL2	-200.UA
IL3	-45.0UA
IL4	-55.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

FAILED DATA RETENTION TEST ADD = 51 DIAG = 34 PIN: 002

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	215.N	190.N	90.0N
DATA SETUP TIME	(TDS)	22.0N	18.0N	8.00N
DATA HOLD TIME	(TDH)	14.0N	14.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	6.00N	4.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	114.N	102.N	54.0N
ADDRESS HOLD TIME	(TAH)	-12.0N	-10.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	76.0N	68.0N	40.0N
CS1 SETUP TIME	(TCSS1)	152.N	134.N	70.0N
CS2 SETUP TIME	(TCSS2)	150.N	132.N	70.0N
CS1 HOLD TIME	(TCSH1)	48.0N	44.0N	28.0N
CS2 HOLD TIME	(TCSH2)	52.0N	46.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	216.N	192.N	102.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	214.N	188.N	98.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	44.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	140.N	112.N	36.0N
OUTPUT HOLD FROM CS2	(TDOH2)	138.N	108.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	116.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	110.N	32.0N
READ CYCLE TIME	(TRC)	232.N	208.N	112.N
WRITE CYCLE TIME	(TWC)	208.N	192.N	120.N

	IIL	IIH	VIC1	VIC2
A0	-131.NA	138.NA	2.89 V	-2.89 V
A1	-135.NA	130.NA	2.93 V	-2.95 V
A2	-131.NA	128.NA	2.96 V	-2.98 V
A3	-129.NA	127.NA	2.95 V	-2.97 V
A4	-130.NA	124.NA	2.98 V	-2.99 V
A5	-130.NA	122.NA	2.88 V	-2.89 V
A6	-126.NA	122.NA	2.84 V	-2.87 V
A7	-123.NA	122.NA	2.85 V	-2.88 V
CS1	-133.NA	118.NA	2.91 V	-2.92 V
CS2	-127.NA	124.NA	2.93 V	-2.96 V
MWR	-129.NA	123.NA	2.91 V	-2.91 V
MRD	-126.NA	123.NA	2.89 V	-2.91 V
DI0	-120.NA	119.NA	2.93 V	-2.89 V
DI1	-115.NA	119.NA	2.92 V	-2.88 V
DI2	-117.NA	116.NA	2.94 V	-2.90 V
DI3	-115.NA	114.NA	2.92 V	-2.91 V

	D00	D01	D02	D03
VOL1	115.MV	125.MV	140.MV	135.MV
VOL2	125.MV	145.MV	170.MV	160.MV
VOH1	4.82 V	4.82 V	4.81 V	4.82 V
VOH2	9.74 V	9.73 V	9.72 V	9.74 V
IDN1	6.35MA	5.95MA	5.40MA	5.55MA
IDN2	15.0MA	13.3MA	11.4MA	11.9MA
IDP1	-2.18MA	-2.16MA	-2.08MA	-2.19MA
IDP2	-4.79MA	-4.77MA	-4.53MA	-4.86MA
IOZ1	1.28UA	1.25UA	1.19UA	1.14UA
IOZ2	1.28UA	1.23UA	1.20UA	1.13UA
IOZ3	1.26UA	1.24UA	1.18UA	1.14UA
IOZ4	1.27UA	1.22UA	1.20UA	1.13UA
IOZ5	1.27UA	1.26UA	1.21UA	1.18UA
IOZ6	1.27UA	1.26UA	1.20UA	1.15UA
IOZ7	1.27UA	1.24UA	1.20UA	1.14UA
IOZ8	1.28UA	1.24UA	1.21UA	1.14UA

ILDP	20.0UA
IL1	-250.UA
IL2	-285.UA
IL3	-115.UA
IL4	-120.UA

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN: 26

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	245.N	205.N	85.0N
DATA SETUP TIME	(TDS)	20.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	12.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	116.N	96.0N	48.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	64.0N	60.0N	36.0N
CS1 SETUP TIME	(TCSS1)	154.N	134.N	68.0N
CS2 SETUP TIME	(TCSS2)	150.N	132.N	66.0N
CS1 HOLD TIME	(TCSH1)	36.0N	32.0N	22.0N
CS2 HOLD TIME	(TCSH2)	38.0N	34.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TCOA1)	236.N	200.N	92.0N
OUTPUT ACTIVE FROM CS2	(TCOA2)	234.N	198.N	90.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	52.0N	46.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	142.N	112.N	42.0N
OUTPUT HOLD FROM CS2	(TDOH2)	140.N	110.N	40.0N
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	116.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	110.N	28.0N
READ CYCLE TIME	(TRC)	256.N	216.N	120.N
WRITE CYCLE TIME	(TWC)	296.N	184.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-1.50NA	1.40NA	2.80 V	-2.80 V
A1	-2.00NA	1.30NA	2.84 V	-2.84 V
A2	-1.30NA	1.60NA	2.85 V	-2.89 V
A3	-1.40NA	1.20NA	2.86 V	-2.87 V
A4	-1.20NA	1.70NA	2.84 V	-2.86 V
A5	-1.40NA	1.30NA	2.79 V	-2.81 V
A6	-1.50NA	1.60NA	2.80 V	-2.82 V
A7	-1.50NA	1.30NA	2.81 V	-2.85 V
CS1	-1.40NA	1.80NA	2.84 V	-2.84 V
CS2	-1.60NA	1.60NA	2.86 V	-2.88 V
MWR	-2.00NA	1.50NA	2.81 V	-2.82 V
MRD	-1.80NA	1.70NA	2.82 V	-2.84 V
DI0	-1.50NA	1.40NA	2.89 V	-2.84 V
DI1	-1.30NA	1.70NA	2.89 V	-2.83 V
DI2	-2.00NA	1.50NA	2.89 V	-2.84 V
DI3	-1.70NA	2.00NA	2.87 V	-2.83 V

	D00	D01	D02	D03
VOL1	110.MV	115.MV	130.MV	125.MV
VOL2	120.MV	145.MV	170.MV	175.MV
VOH1	4.84 V	4.84 V	4.84 V	4.84 V
VOH2	9.70 V	9.69 V	9.68 V	9.69 V
IDN1	6.60MA	6.30MA	5.90MA	6.00MA
IDN2	16.3MA	14.6MA	12.6MA	12.9MA
IDP1	-2.49MA	-2.57MA	-2.49MA	-2.53MA
IDP2	-4.64MA	-4.68MA	-4.48MA	-4.66MA
IOZ1	12.8NA	10.6NA	8.50NA	11.6NA
IOZ2	15.6NA	6.80NA	12.0NA	8.20NA
IOZ3	9.00NA	11.5NA	7.70NA	11.6NA
IOZ4	8.50NA	12.4NA	6.30NA	13.9NA
IOZ5	15.0NA	6.10NA	13.4NA	6.80NA
IOZ6	15.3NA	5.70NA	13.4NA	6.90NA
IOZ7	15.0NA	5.90NA	13.5NA	6.90NA
IOZ8	15.3NA	5.60NA	13.2NA	6.70NA

ILDP	15.0UA
IL1	-9.05MA
IL2	-9.02MA
IL3	-10.2MA
IL4	-10.2MA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	245.N	200.N	75.0N
DATA SETUP TIME	(TDS)	22.0N	18.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	114.N	92.0N	42.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	70.0N	58.0N	32.0N
CS1 SETUP TIME	(TCSS1)	148.N	128.N	62.0N
CS2 SETUP TIME	(TCSS2)	148.N	126.N	60.0N
CS1 HOLD TIME	(TCSH1)	34.0N	30.0N	22.0N
CS2 HOLD TIME	(TCSH2)	38.0N	32.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	236.N	192.N	86.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	234.N	192.N	84.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	48.0N	42.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	136.N	106.N	38.0N
OUTPUT HOLD FROM CS2	(TDOH2)	134.N	104.N	38.0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	112.N	26.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	106.N	28.0N
READ CYCLE TIME	(TRC)	232.N	200.N	96.0N
WRITE CYCLE TIME	(TWC)	208.N	176.N	104.N

	IIL	IIH	VIC1	VIC2
A0	-200.PA	300.PA	2.95 V	-2.95 V
A1	-300.PA	200.PA	2.99 V	-2.99 V
A2	-200.PA	300.PA	3.00 V	-3.03 V
A3	-200.PA	200.PA	3.01 V	-3.01 V
A4	-200.PA	300.PA	2.99 V	-3.00 V
A5	-200.PA	200.PA	2.94 V	-2.97 V
A6	-300.PA	300.PA	2.95 V	-2.97 V
A7	-300.PA	200.PA	2.96 V	-3.00 V
CS1	-200.PA	300.PA	2.99 V	-2.98 V
CS2	-300.PA	300.PA	3.00 V	-3.02 V
MWR	-400.PA	200.PA	2.96 V	-2.97 V
MRD	-400.PA	400.PA	2.97 V	-2.98 V
DI0	-300.PA	200.PA	3.03 V	-2.98 V
DI1	-200.PA	300.PA	3.03 V	-2.97 V
DI2	-400.PA	200.PA	3.03 V	-2.97 V
DI3	-300.PA	400.PA	3.02 V	-2.97 V

	D00	D01	D02	D03
VOL1	100.MV	105.MV	110.MV	110.MV
VOL2	105.MV	125.MV	145.MV	150.MV
VOH1	4.87 V	4.87 V	4.86 V	4.87 V
VOH2	9.76 V	9.75 V	9.74 V	9.76 V
IDN1	7.45MA	7.20MA	6.65MA	6.80MA
IDN2	18.8MA	17.1MA	14.8MA	15.2MA
IDP1	-2.99MA	-3.04MA	-2.96MA	-3.04MA
IDP2	-5.76MA	-5.79MA	-5.58MA	-5.82MA
IOZ1	2.90NA	3.10NA	1.40NA	3.90NA
IOZ2	6.20NA	-400.PA	4.90NA	500.PA
IOZ3	200.PA	4.90NA	-100.PA	3.80NA
IOZ4	-100.PA	5.40NA	-1.50NA	5.70NA
IOZ5	6.10NA	-1.40NA	5.60NA	-1.10NA
IOZ6	6.00NA	-1.10NA	5.80NA	-1.20NA
IOZ7	6.00NA	-1.30NA	5.60NA	-1.20NA
IOZ8	5.60NA	-1.20NA	5.60NA	-1.40NA
ILDP	11.6UA			
IL1	-9.56MA			
IL2	-9.49MA			
IL3	-10.2MA			
IL4	-10.2MA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	240.N	190.N	70.0N
DATA SETUP TIME	(TDS)	26.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	12.0N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	112.N	90.0N	38.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	70.0N	62.0N	32.0N
CS1 SETUP TIME	(TCSS1)	146.N	126.N	58.0N
CS2 SETUP TIME	(TCSS2)	146.N	118.N	56.0N
CS1 HOLD TIME	(TCSH1)	38.0N	34.0N	22.0N
CS2 HOLD TIME	(TCSH2)	42.0N	36.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	242.N	190.N	82.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	240.N	188.N	82.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	44.0N	38.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	132.N	102.N	36.0N
OUTPUT HOLD FROM CS2	(TDOH2)	132.N	102.N	36.0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	112.N	26.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	108.N	26.0N
READ CYCLE TIME	(TRC)	224.N	192.N	104.N
WRITE CYCLE TIME	(TWC)	208.N	176.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	0.00 A	100.PA	3.09 V	-3.09 V
A1	-100.PA	100.PA	3.12 V	-3.12 V
A2	0.00 A	100.PA	3.13 V	-3.15 V
A3	-100.PA	0.00 A	3.14 V	-3.14 V
A4	0.00 A	100.PA	3.12 V	-3.13 V
A5	-100.PA	100.PA	3.08 V	-3.10 V
A6	-100.PA	100.PA	3.08 V	-3.10 V
A7	-100.PA	100.PA	3.09 V	-3.13 V
CS1	-100.PA	100.PA	3.13 V	-3.12 V
CS2	-100.PA	100.PA	3.13 V	-3.14 V
MWR	-100.PA	100.PA	3.10 V	-3.10 V
MRD	-200.PA	100.PA	3.11 V	-3.11 V
DI0	0.00 A	0.00 A	3.16 V	-3.11 V
DI1	-100.PA	100.PA	3.16 V	-3.11 V
DI2	-100.PA	0.00 A	3.16 V	-3.11 V
DI3	0.00 A	100.PA	3.14 V	-3.10 V

	D00	D01	D02	D03
VOL1	90.0MV	95.0MV	100.MV	100.MV
VOL2	95.0MV	110.MV	130.MV	135.MV
VOH1	4.88 V	4.89 V	4.88 V	4.88 V
VOH2	9.79 V	9.79 V	9.78 V	9.79 V
IDN1	8.20MA	7.90MA	7.35MA	7.50MA
IDN2	20.9MA	19.2MA	16.8MA	17.2MA
IDP1	-3.42MA	-3.49MA	-3.46MA	-3.52MA
IDP2	-6.76MA	-6.86MA	-6.64MA	-6.90MA
IOZ1	4.80NA	-1.50NA	4.70NA	-2.20NA
IOZ2	900.PA	1.70NA	1.30NA	400.PA
IOZ3	2.20NA	1.30NA	400.PA	2.00NA
IOZ4	5.70NA	-1.80NA	4.20NA	-1.40NA
IOZ5	-1.40NA	4.20NA	-1.50NA	3.70NA
IOZ6	-1.50NA	4.90NA	-1.90NA	4.10NA
IOZ7	-1.70NA	5.10NA	-2.00NA	4.90NA
IOZ8	-1.80NA	5.20NA	-2.30NA	5.00NA

ILOP	7.60UA
IL1	-10.2MA
IL2	-10.2MA
IL3	-10.2MA
IL4	-10.2MA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	245.N	210.N	90.0N
DATA SETUP TIME	(TDS)	20.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	14.0N	14.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	118.N	102.N	52.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	4.00N
WRITE PULSE WIDTH	(TWP)	74.0N	66.0N	38.0N
CS1 SETUP TIME	(TCSS1)	160.N	142.N	74.0N
CS2 SETUP TIME	(TCSS2)	158.N	140.N	72.0N
CS1 HOLD TIME	(TCSH1)	44.0N	40.0N	26.0N
CS2 HOLD TIME	(TCSH2)	48.0N	42.0N	26.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	240.N	208.N	104.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	238.N	206.N	102.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	58.0N	50.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	146.N	116.N	44.0N
OUTPUT HOLD FROM CS2	(TDOH2)	142.N	114.N	44.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	28.0N
OUTPUT HOLD FROM MWR	(TDOH)	134.N	112.N	30.0N
READ CYCLE TIME	(TRC)	264.N	232.N	112.N
WRITE CYCLE TIME	(TWC)	216.N	200.N	128.N

	IIL	IIH	VIC1	VIC2
A0	-18.4NA	19.8NA	2.71 V	-2.72 V
A1	-20.8NA	18.8NA	2.75 V	-2.75 V
A2	-18.4NA	19.7NA	2.76 V	-2.80 V
A3	-18.5NA	18.4NA	2.78 V	-2.78 V
A4	-18.7NA	20.7NA	2.76 V	-2.78 V
A5	-18.5NA	19.2NA	2.70 V	-2.73 V
A6	-19.0NA	20.7NA	2.71 V	-2.73 V
A7	-18.9NA	20.2NA	2.73 V	-2.76 V
CS1	-19.5NA	23.2NA	2.75 V	-2.76 V
CS2	-21.0NA	22.3NA	2.77 V	-2.81 V
MWR	-21.0NA	20.1NA	2.73 V	-2.74 V
MRD	-21.9NA	21.2NA	2.73 V	-2.76 V
DI0	-20.3NA	21.7NA	2.80 V	-2.75 V
DI1	-19.5NA	21.9NA	2.80 V	-2.75 V
DI2	-21.7NA	22.3NA	2.80 V	-2.75 V
DI3	-21.0NA	23.7NA	2.79 V	-2.75 V

	D00	D01	D02	D03
VOL1	130.MV	135.MV	150.MV	145.MV
VOL2	145.MV	170.MV	205.MV	205.MV
VOH1	4.81 V	4.82 V	4.80 V	4.81 V
VOH2	9.64 V	9.64 V	9.62 V	9.64 V
IDN1	5.65MA	5.45MA	5.05MA	5.15MA
IDN2	13.7MA	12.4MA	10.6MA	10.8MA
IDP1	-2.11MA	-2.14MA	-2.09MA	-2.14MA
IDP2	-3.78MA	-3.75MA	-3.63MA	-3.79MA
IOZ1	65.5NA	44.5NA	43.7NA	37.5NA
IOZ2	59.9NA	38.7NA	43.1NA	33.5NA
IOZ3	48.9NA	44.0NA	34.2NA	39.8NA
IOZ4	52.5NA	41.7NA	35.7NA	37.9NA
IOZ5	53.0NA	37.3NA	39.2NA	32.2NA
IOZ6	54.4NA	37.3NA	40.5NA	32.8NA
IOZ7	54.0NA	36.3NA	39.1NA	32.0NA
IOZ8	54.6NA	37.3NA	40.5NA	31.8NA

ILDP	20.0UA
IL1	-8.53MA
IL2	-8.50MA
IL3	-10.2MA
IL4	-10.2MA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	260.N	220.N	105.N
DATA SETUP TIME	(TDS)	18.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	16.0N	14.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	4.00N	4.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	124.N	110.N	60.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-16.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	78.0N	70.0N	42.0N
CS1 SETUP TIME	(TCSS1)	172.N	150.N	82.0N
CS2 SETUP TIME	(TCSS2)	170.N	150.N	78.0N
CS1 HOLD TIME	(TCSH1)	46.0N	42.0N	26.0N
CS2 HOLD TIME	(TCSH2)	50.0N	46.0N	26.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	256.N	224.N	114.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	254.N	222.N	112.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	62.0N	56.0N	34.0N
OUTPUT HOLD FROM CS1	(TDOH1)	146.N	118.N	46.0N
OUTPUT HOLD FROM CS2	(TDOH2)	144.N	116.N	46.0N
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	116.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	136.N	112.N	30.0N
READ CYCLE TIME	(TRC)	280.N	248.N	120.N
WRITE CYCLE TIME	(TWC)	224.N	200.N	136.N

	IIL	IIH	VIC1	VIC2
A0	-111.NA	104.NA	2.63 V	-2.64 V
A1	-118.NA	105.NA	2.67 V	-2.68 V
A2	-111.NA	106.NA	2.69 V	-2.73 V
A3	-111.NA	102.NA	2.70 V	-2.71 V
A4	-112.NA	109.NA	2.68 V	-2.71 V
A5	-110.NA	102.NA	2.63 V	-2.65 V
A6	-113.NA	107.NA	2.63 V	-2.66 V
A7	-109.NA	105.NA	2.65 V	-2.69 V
CS1	-116.NA	114.NA	2.68 V	-2.68 V
CS2	-120.NA	115.NA	2.70 V	-2.74 V
MWR	-114.NA	105.NA	2.65 V	-2.66 V
MRD	-121.NA	110.NA	2.66 V	-2.68 V
DI0	-108.NA	108.NA	2.73 V	-2.68 V
DI1	-105.NA	105.NA	2.73 V	-2.67 V
DI2	-111.NA	108.NA	2.73 V	-2.68 V
DI3	-108.NA	110.NA	2.71 V	-2.68 V

	D00	D01	D02	D03
VOL1	145.MV	155.MV	170.MV	165.MV
VOL2	165.MV	190.MV	230.MV	235.MV
VOH1	4.78 V	4.78 V	4.78 V	4.78 V
VOH2	9.57 V	9.57 V	9.56 V	9.57 V
IDN1	5.10MA	4.90MA	4.50MA	4.65MA
IDN2	12.2MA	10.9MA	9.35MA	9.50MA
IDP1	-1.87MA	-1.89MA	-1.83MA	-1.89MA
IDP2	-3.20MA	-3.15MA	-3.00MA	-3.19MA
IOZ1	73.3NA	20.1NA	-5.50NA	-20.9NA
IOZ2	51.4NA	11.8NA	-14.8NA	-24.4NA
IOZ3	50.2NA	-100.PA	-13.5NA	-35.8NA
IOZ4	44.6NA	-900.PA	-18.0NA	-36.9NA
IOZ5	47.3NA	6.70NA	-15.7NA	-26.2NA
IOZ6	44.6NA	1.60NA	-16.4NA	-31.2NA
IOZ7	42.7NA	1.80NA	-17.0NA	-28.3NA
IOZ8	40.4NA	-1.20NA	-18.8NA	-31.5NA
ILDP	80.0UA			
IL1	-8.79MA			
IL2	-8.79MA			
IL3	-10.2MA			
IL4	-10.2MA			

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN: 27

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	255.N	215.N	85.0N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	12.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	122.N	100.N	50.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-16.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	70.0N	62.0N	36.0N
CS1 SETUP TIME	(TCSS1)	166.N	142.N	70.0N
CS2 SETUP TIME	(TCSS2)	162.N	140.N	68.0N
CS1 HOLD TIME	(TCSH1)	38.0N	34.0N	22.0N
CS2 HOLD TIME	(TCSH2)	40.0N	36.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	244.N	204.N	92.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	240.N	200.N	90.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	54.0N	46.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	154.N	122.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	150.N	118.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	120.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	138.N	114.N	32.0N
READ CYCLE TIME	(TRC)	264.N	224.N	120.N
WRITE CYCLE TIME	(TWC)	272.N	200.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-1.60NA	2.10NA	2.96 V	-2.97 V
A1	-1.70NA	1.70NA	2.99 V	-3.01 V
A2	-1.50NA	1.60NA	2.96 V	-2.98 V
A3	-1.40NA	7.10NA	2.95 V	-2.97 V
A4	-1.90NA	1.50NA	2.97 V	-2.99 V
A5	-2.10NA	1.90NA	2.93 V	-2.95 V
A6	-1.80NA	2.00NA	2.91 V	-2.93 V
A7	-1.60NA	1.60NA	2.91 V	-2.93 V
CS1	-1.60NA	2.20NA	2.94 V	-2.94 V
CS2	-2.50NA	2.00NA	2.96 V	-2.97 V
MWR	-2.90NA	1.50NA	2.91 V	-2.93 V
MRD	-2.10NA	2.00NA	2.92 V	-2.95 V
DI0	-2.30NA	2.20NA	2.98 V	-2.95 V
DI1	-1.80NA	2.10NA	2.97 V	-2.91 V
DI2	-2.10NA	1.90NA	3.00 V	-2.94 V
DI3	-2.20NA	2.40NA	2.98 V	-2.93 V

	DO0	DO1	DO2	DO3
VOL1	110.MV	110.MV	120.MV	120.MV
VOL2	110.MV	120.MV	135.MV	130.MV
VOH1	4.84 V	4.84 V	4.84 V	4.85 V
VOH2	9.76 V	9.79 V	9.78 V	9.79 V
IDN1	6.75MA	6.55MA	6.10MA	6.25MA
IDN2	17.0MA	15.9MA	14.0MA	14.5MA
IDP1	-2.51MA	-2.55MA	-2.48MA	-2.51MA
IDP2	-5.72MA	-5.78MA	-5.56MA	-5.76MA
IOZ1	40.6NA	47.4NA	44.6NA	34.8NA
IOZ2	42.8NA	43.0NA	47.0NA	33.0NA
IOZ3	38.4NA	45.5NA	45.8NA	33.8NA
IOZ4	35.8NA	47.8NA	42.9NA	36.8NA
IOZ5	43.6NA	41.9NA	50.2NA	31.7NA
IOZ6	44.0NA	42.0NA	49.4NA	31.3NA
IOZ7	43.2NA	42.1NA	49.1NA	31.4NA
IOZ8	42.8NA	41.3NA	48.4NA	31.7NA

ILDP	-5.00UA
IL1	-25.0UA
IL2	-20.0UA
IL3	-10.0UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	265.N	210.N	80.0N
DATA SETUP TIME	(TDS)	28.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	120.N	96.0N	42.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	80.0N	68.0N	34.0N
CS1 SETUP TIME	(TCSS1)	164.N	138.N	62.0N
CS2 SETUP TIME	(TCSS2)	158.N	134.N	62.0N
CS1 HOLD TIME	(TCSH1)	38.0N	32.0N	22.0N
CS2 HOLD TIME	(TCSH2)	42.0N	34.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	244.N	198.N	84.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	242.N	186.N	82.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	42.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	146.N	114.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	144.N	112.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	116.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	136.N	112.N	30.0N
READ CYCLE TIME	(TRC)	248.N	208.N	96.0N
WRITE CYCLE TIME	(TWC)	248.N	192.N	104.N

	IIL	IIH	VIC1	VIC2
A0	-200.PA	300.PA	3.07 V	-3.06 V
A1	-300.PA	300.PA	3.09 V	-3.10 V
A2	-300.PA	300.PA	3.08 V	-3.09 V
A3	-300.PA	2.00NA	3.07 V	-3.08 V
A4	-500.PA	300.PA	3.09 V	-3.10 V
A5	-400.PA	500.PA	3.04 V	-3.06 V
A6	-400.PA	400.PA	3.03 V	-3.05 V
A7	-300.PA	200.PA	3.03 V	-3.04 V
CS1	-300.PA	500.PA	3.06 V	-3.06 V
CS2	-600.PA	300.PA	3.09 V	-3.08 V
MWR	-700.PA	200.PA	3.02 V	-3.04 V
MRD	-500.PA	500.PA	3.04 V	-3.06 V
DI0	-400.PA	300.PA	3.11 V	-3.06 V
DI1	-400.PA	400.PA	3.10 V	-3.02 V
DI2	-400.PA	200.PA	3.12 V	-3.05 V
DI3	-500.PA	400.PA	3.11 V	-3.04 V

	D00	D01	D02	D03
VOL1	100.MV	100.MV	105.MV	105.MV
VOL2	95.0MV	105.MV	115.MV	115.MV
VOH1	4.88 V	4.88 V	4.87 V	4.87 V
VOH2	9.82 V	9.82 V	9.81 V	9.82 V
IDN1	7.50MA	7.35MA	6.85MA	7.00MA
IDN2	19.5MA	18.3MA	16.1MA	16.8MA
IDP1	-2.99MA	-3.00MA	-2.94MA	-3.00MA
IDP2	-6.77MA	-6.79MA	-6.61MA	-6.84MA
IOZ1	7.20NA	6.20NA	7.40NA	4.90NA
IOZ2	9.60NA	3.50NA	10.7NA	1.90NA
IOZ3	2.60NA	10.2NA	4.30NA	6.70NA
IOZ4	3.10NA	9.50NA	3.60NA	7.90NA
IOZ5	8.70NA	3.00NA	10.6NA	1.20NA
IOZ6	8.80NA	3.30NA	10.8NA	1.20NA
IOZ7	9.00NA	3.00NA	10.7NA	1.30NA
IOZ8	8.90NA	3.10NA	10.8NA	1.20NA
ILDP	800.NA			
IL1	-20.0UA			
IL2	-15.0UA			
IL3	-5.00UA			
IL4	-5.00UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	260.N	205.N	70.0N
DATA SETUP TIME	(TDS)	34.0N	26.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	14.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	116.N	92.0N	40.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	88.0N	60.0N	32.0N
CS1 SETUP TIME	(TCSS1)	156.N	134.N	60.0N
CS2 SETUP TIME	(TCSS2)	164.N	130.N	58.0N
CS1 HOLD TIME	(TCSH1)	38.0N	40.0N	20.0N
CS2 HOLD TIME	(TCSH2)	52.0N	42.0N	18.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	248.N	194.N	80.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	246.N	192.N	80.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	46.0N	40.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	142.N	108.N	32.0N
OUTPUT HOLD FROM CS2	(TDOH2)	138.N	106.N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	136.N	110.N	30.0N
READ CYCLE TIME	(TRC)	232.N	200.N	104.N
WRITE CYCLE TIME	(TWC)	224.N	200.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	0.00 A	200.PA	3.16 V	-3.15 V
A1	-100.PA	100.PA	3.17 V	-3.19 V
A2	-100.PA	100.PA	3.17 V	-3.19 V
A3	-100.PA	400.PA	3.17 V	-3.18 V
A4	-200.PA	100.PA	3.19 V	-3.20 V
A5	-100.PA	200.PA	3.13 V	-3.14 V
A6	-100.PA	100.PA	3.13 V	-3.15 V
A7	-100.PA	100.PA	3.13 V	-3.15 V
CS1	-100.PA	100.PA	3.17 V	-3.16 V
CS2	-200.PA	100.PA	3.19 V	-3.18 V
MWR	-200.PA	100.PA	3.13 V	-3.15 V
MRD	-100.PA	100.PA	3.15 V	-3.17 V
DI0	-100.PA	100.PA	3.21 V	-3.16 V
DI1	0.00 A	100.PA	3.20 V	-3.13 V
DI2	-100.PA	100.PA	3.22 V	-3.15 V
DI3	-100.PA	100.PA	3.21 V	-3.14 V

	D00	D01	D02	D03
VOL1	90.0MV	90.0MV	100.MV	95.0MV
VOL2	85.0MV	95.0MV	105.MV	100.MV
VOH1	4.88 V	4.89 V	4.88 V	4.89 V
VOH2	9.84 V	9.84 V	9.84 V	9.84 V
IDN1	8.15MA	7.95MA	7.45MA	7.55MA
IDN2	21.4MA	20.2MA	18.0MA	18.6MA
IDP1	-3.37MA	-3.45MA	-3.40MA	-3.44MA
IDP2	-7.70MA	-7.88MA	-7.59MA	-7.84MA
IOZ1	-200.PA	5.80NA	-1.10NA	5.30NA
IOZ2	2.70NA	2.50NA	1.30NA	2.70NA
IOZ3	2.50NA	1.40NA	3.20NA	100.PA
IOZ4	-700.PA	5.10NA	-100.PA	3.70NA
IOZ5	4.80NA	-100.PA	4.20NA	200.PA
IOZ6	5.10NA	200.PA	3.70NA	400.PA
IOZ7	4.60NA	300.PA	3.80NA	600.PA
IOZ8	4.70NA	400.PA	3.40NA	600.PA

ILDP	-3.40UA
IL1	-20.0UA
IL2	-15.0UA
IL3	-5.00UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	255.N	215.N	90.0N
DATA SETUP TIME	(TDS)	26.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	122.N	106.N	54.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-16.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	80.0N	70.0N	40.0N
CS1 SETUP TIME	(TCSS1)	174.N	148.N	74.0N
CS2 SETUP TIME	(TCSS2)	172.N	148.N	74.0N
CS1 HOLD TIME	(TCSH1)	48.0N	44.0N	26.0N
CS2 HOLD TIME	(TCSH2)	54.0N	46.0N	26.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	244.N	212.N	102.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	242.N	210.N	102.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	56.0N	50.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	156.N	124.N	40.0N
OUTPUT HOLD FROM CS2	(TDOH2)	152.N	122.N	40.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	120.N	34.0N
OUTPUT HOLD FROM MWR	(TPDH)	140.N	116.N	36.0N
READ CYCLE TIME	(TRC)	272.N	232.N	120.N
WRITE CYCLE TIME	(TWC)	232.N	208.N	128.N

	IIL	IIH	VIC1	VIC2
A0	-18.1NA	20.3NA	2.93 V	-2.94 V
A1	-18.2NA	18.9NA	2.96 V	-2.99 V
A2	-15.1NA	15.8NA	2.92 V	-2.94 V
A3	-14.8NA	27.1NA	2.91 V	-2.93 V
A4	-16.8NA	15.4NA	2.93 V	-2.95 V
A5	-18.6NA	17.3NA	2.89 V	-2.91 V
A6	-17.5NA	17.5NA	2.88 V	-2.89 V
A7	-15.9NA	16.3NA	2.87 V	-2.89 V
CS1	-17.0NA	17.4NA	2.90 V	-2.90 V
CS2	-16.9NA	17.3NA	2.93 V	-2.93 V
MWR	-17.3NA	15.1NA	2.87 V	-2.89 V
MRD	-17.0NA	16.0NA	2.88 V	-2.91 V
DI0	-16.3NA	16.8NA	2.93 V	-2.91 V
DI1	-15.3NA	15.8NA	2.93 V	-2.86 V
DI2	-15.6NA	15.7NA	2.95 V	-2.90 V
DI3	-15.6NA	16.7NA	2.94 V	-2.89 V

	DO0	DO1	DO2	DO3
VOL1	125.MV	130.MV	140.MV	135.MV
VOL2	130.MV	140.MV	160.MV	150.MV
VOH1	4.82 V	4.82 V	4.82 V	4.82 V
VOH2	9.74 V	9.75 V	9.74 V	9.75 V
IDN1	5.95MA	5.75MA	5.35MA	5.45MA
IDN2	14.8MA	13.7MA	12.1MA	12.5MA
IDP1	-2.15MA	-2.18MA	-2.12MA	-2.15MA
IDP2	-4.88MA	-4.93MA	-4.74MA	-4.94MA
IOZ1	371.NA	386.NA	375.NA	309.NA
IOZ2	363.NA	391.NA	375.NA	303.NA
IOZ3	363.NA	387.NA	372.NA	306.NA
IOZ4	356.NA	390.NA	376.NA	299.NA
IOZ5	364.NA	395.NA	379.NA	311.NA
IOZ6	364.NA	388.NA	392.NA	299.NA
IOZ7	373.NA	386.NA	381.NA	308.NA
IOZ8	362.NA	393.NA	378.NA	302.NA

ILDP	4.80UA
IL1	-35.0UA
IL2	-35.0UA
IL3	-30.0UA
IL4	-20.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	255.N	220.N	100.N
DATA SETUP TIME	(TDS)	26.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	14.0N	14.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	4.00N	4.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	128.N	114.N	60.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-16.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	86.0N	76.0N	44.0N
CS1 SETUP TIME	(TCSS1)	180.N	156.N	82.0N
CS2 SETUP TIME	(TCSS2)	178.N	154.N	78.0N
CS1 HOLD TIME	(TCSH1)	54.0N	46.0N	28.0N
CS2 HOLD TIME	(TCSH2)	56.0N	50.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	256.N	224.N	112.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	254.N	222.N	110.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	60.0N	54.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	158.N	128.N	44.0N
OUTPUT HOLD FROM CS2	(TDOH2)	154.N	124.N	44.0N
OUTPUT HOLD FROM MRD	(TDOH3)	142.N	122.N	36.0N
OUTPUT HOLD FROM MWR	(TPOH)	142.N	116.N	38.0N
READ CYCLE TIME	(TRC)	280.N	240.N	120.N
WRITE CYCLE TIME	(TWC)	240.N	216.N	136.N

	IIL	IIH	VIC1	VIC2
A0	-103.NA	107.NA	2.91 V	-2.93 V
A1	-108.NA	110.NA	2.95 V	-2.98 V
A2	-89.2NA	87.8NA	2.89 V	-2.91 V
A3	-86.3NA	101.NA	2.88 V	-2.90 V
A4	-88.5NA	84.3NA	2.89 V	-2.93 V
A5	-102.NA	90.9NA	2.87 V	-2.89 V
A6	-94.8NA	91.0NA	2.84 V	-2.86 V
A7	-88.9NA	85.2NA	2.83 V	-2.85 V
CS1	-92.3NA	85.6NA	2.86 V	-2.87 V
CS2	-90.1NA	88.9NA	2.89 V	-2.90 V
MWR	-88.7NA	80.8NA	2.83 V	-2.85 V
MRD	-90.0NA	85.2NA	2.84 V	-2.88 V
DI0	-84.5NA	85.2NA	2.89 V	-2.87 V
DI1	-82.0NA	80.7NA	2.89 V	-2.82 V
DI2	-84.0NA	82.3NA	2.92 V	-2.86 V
DI3	-80.4NA	80.9NA	2.90 V	-2.85 V

	D00	D01	D02	D03
VOL1	140.MV	145.MV	155.MV	150.MV
VOL2	[illegible].MV	155.MV	180.MV	170.MV
VOH1	[illegible]	4.80 V	4.80 V	4.80 V
VOH2	9.72 V	9.72 V	9.70 V	9.72 V
IDN1	5.35MA	5.20MA	4.85MA	4.95MA
IDN2	13.2MA	12.2MA	10.8MA	11.2MA
IDP1	-1.96MA	-1.96MA	-1.91MA	-1.96MA
IDP2	-4.42MA	-4.43MA	-4.24MA	-4.47MA
IOZ1	1.51UA	1.58UA	1.53UA	1.25UA
IOZ2	1.51UA	1.57UA	1.53UA	1.25UA
IOZ3	1.50UA	1.57UA	1.53UA	1.26UA
IOZ4	1.49UA	1.57UA	1.53UA	1.25UA
IOZ5	1.51UA	1.59UA	1.56UA	1.28UA
IOZ6	1.52UA	1.60UA	1.55UA	1.27UA
IOZ7	1.50UA	1.59UA	1.54UA	1.28UA
IOZ8	1.51UA	1.58UA	1.55UA	1.27UA

ILDP	5.00UA
IL1	-85.0UA
IL2	-95.0UA
IL3	-85.0UA
IL4	-65.0UA

RCA COP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN: 28

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	245.N	205.N	80.0N
DATA SETUP TIME	(TDS)	26.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	120.N	98.0N	48.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	68.0N	60.0N	36.0N
CS1 SETUP TIME	(TCSS1)	164.N	136.N	64.0N
CS2 SETUP TIME	(TCSS2)	160.N	134.N	62.0N
CS1 HOLD TIME	(TCSH1)	42.0N	38.0N	24.0N
CS2 HOLD TIME	(TCSH2)	46.0N	38.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	230.N	194.N	88.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	226.N	192.N	88.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	44.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	146.N	116.N	32.0N
OUTPUT HOLD FROM CS2	(TDOH2)	144.N	112.N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	30.0N
OUTPUT HOLD FROM MWR	(TPOH)	134.N	112.N	30.0N
READ CYCLE TIME	(TRC)	264.N	216.N	104.N
WRITE CYCLE TIME	(TWC)	256.N	184.N	112.N

	IIL	IIH	VIC1	VICP
A0	-3.40NA	3.00NA	3.23 V	-3.23 V
A1	-3.50NA	2.90NA	3.31 V	-3.29 V
A2	-3.40NA	3.10NA	3.31 V	-3.37 V
A3	-3.20NA	3.40NA	3.29 V	-3.34 V
A4	-3.30NA	3.20NA	3.36 V	-3.39 V
A5	-2.80NA	2.90NA	3.23 V	-3.25 V
A6	-3.80NA	3.60NA	3.22 V	-3.24 V
A7	-3.40NA	3.20NA	3.21 V	-3.23 V
CS1	-3.10NA	3.50NA	3.27 V	-3.28 V
CS2	-3.70NA	3.50NA	3.31 V	-3.35 V
MWR	-3.20NA	3.10NA	3.28 V	-3.30 V
MRD	-3.30NA	3.40NA	3.26 V	-3.26 V
DI0	-5.00NA	3.00NA	3.31 V	-3.29 V
DI1	-3.40NA	3.10NA	3.30 V	-3.25 V
DI2	-3.10NA	3.40NA	3.34 V	-3.26 V
DI3	-2.90NA	3.20NA	3.35 V	-3.28 V

	D00	D01	D02	D03
VOL1	90.0MV	95.0MV	105.MV	100.MV
VOL2	100.MV	105.MV	120.MV	120.MV
VOH1	4.85 V	4.85 V	4.84 V	4.85 V
VOH2	9.79 V	9.80 V	9.78 V	9.80 V
IDN1	7.95MA	7.70MA	7.20MA	7.20MA
IDN2	19.3MA	17.8MA	15.7MA	16.0MA
IDP1	-2.58MA	-2.62MA	-2.50MA	-2.56MA
IDP2	-5.88MA	-5.99MA	-5.64MA	-5.96MA
IOZ1	46.1NA	56.8NA	53.1NA	46.7NA
IOZ2	42.7NA	60.2NA	49.5NA	50.0NA
IOZ3	48.7NA	54.2NA	54.6NA	45.3NA
IOZ4	48.1NA	53.5NA	55.3NA	43.9NA
IOZ5	42.2NA	60.9NA	48.6NA	52.1NA
IOZ6	42.2NA	60.9NA	48.8NA	51.8NA
IOZ7	42.4NA	61.0NA	48.3NA	51.6NA
IOZ8	41.9NA	60.7NA	48.7NA	51.5NA

ILDP	-5.00UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-20.0UA
IL4	-20.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	270.N	215.N	75.0N
DATA SETUP TIME	(TDS)	30.0N	24.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	8.00N
ADDRESS SETUP TIME	(TAS1)	22.0N	16.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	126.N	100.N	42.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	72.0N	64.0N	32.0N
CS1 SETUP TIME	(TCSS1)	160.N	134.N	62.0N
CS2 SETUP TIME	(TCSS2)	158.N	132.N	60.0N
CS1 HOLD TIME	(TCSH1)	36.0N	30.0N	22.0N
CS2 HOLD TIME	(TCSH2)	38.0N	32.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	242.N	196.N	82.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	238.N	194.N	80.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	48.0N	42.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	142.N	110.N	30.0N
OUTPUT HOLD FROM CS2	(TDOH2)	138.N	108.N	30.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	28.0N
OUTPUT HOLD FROM MWR	(TPOH)	134.N	110.N	30.0N
READ CYCLE TIME	(TRC)	256.N	208.N	96.0N
WRITE CYCLE TIME	(TWC)	264.N	184.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-400.PA	300.PA	3.26 V	-3.32 V
A1	-400.PA	300.PA	3.34 V	-3.31 V
A2	-400.PA	300.PA	3.34 V	-3.38 V
A3	-400.PA	400.PA	3.32 V	-3.36 V
A4	-300.PA	300.PA	3.38 V	-3.40 V
A5	-300.PA	300.PA	3.25 V	-3.27 V
A6	-500.PA	600.PA	3.25 V	-3.27 V
A7	-400.PA	300.PA	3.23 V	-3.25 V
CS1	-300.PA	400.PA	3.30 V	-3.30 V
CS2	-500.PA	400.PA	3.34 V	-3.37 V
MWR	-400.PA	300.PA	3.30 V	-3.33 V
MRD	-400.PA	300.PA	3.29 V	-3.28 V
DI0	-900.PA	300.PA	3.34 V	-3.31 V
DI1	-500.PA	300.PA	3.32 V	-3.27 V
DI2	-300.PA	400.PA	3.36 V	-3.28 V
DI3	-300.PA	300.PA	3.37 V	-3.30 V

	D00	D01	D02	D03
VOL1	85.0MV	85.0MV	90.0MV	90.0MV
VOL2	85.0MV	95.0MV	105.MV	105.MV
VOH1	4.87 V	4.88 V	4.87 V	4.88 V
VOH2	9.82 V	9.83 V	9.82 V	9.83 V
IDN1	8.80MA	8.55MA	8.05MA	8.00MA
IDN2	21.9MA	20.4MA	18.0MA	18.3MA
IDP1	-3.01MA	-3.10MA	-2.98MA	-3.01MA
IDP2	-6.91MA	-7.09MA	-6.72MA	-7.02MA
IOZ1	10.7NA	6.00NA	10.8NA	3.40NA
IOZ2	7.80NA	6.60NA	9.00NA	3.50NA
IOZ3	4.10NA	11.1NA	4.20NA	9.30NA
IOZ4	7.50NA	7.60NA	7.40NA	6.00NA
IOZ5	5.10NA	9.60NA	6.70NA	5.70NA
IOZ6	5.10NA	9.20NA	6.50NA	6.20NA
IOZ7	4.90NA	9.90NA	6.30NA	5.90NA
IOZ8	4.80NA	9.60NA	6.10NA	6.30NA

ILDP	-1.80UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-20.0UA
IL4	-15.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	275.N	210.N	70.0N
DATA SETUP TIME	(TDS)	40.0N	28.0N	8.00N
DATA HOLD TIME	(TDH)	6.00N	6.00N	8.00N
ADDRESS SETUP TIME	(TAS1)	24.0N	16.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	126.N	100.N	40.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	82.0N	66.0N	32.0N
CS1 SETUP TIME	(TCSS1)	164.N	134.N	58.0N
CS2 SETUP TIME	(TCSS2)	162.N	132.N	56.0N
CS1 HOLD TIME	(TCSH1)	42.0N	36.0N	20.0N
CS2 HOLD TIME	(TCSH2)	40.0N	38.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	244.N	192.N	82.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	244.N	190.N	80.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	46.0N	38.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	138.N	104.N	30.0N
OUTPUT HOLD FROM CS2	(TDOH2)	136.N	102.N	30.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	134.N	110.N	28.0N
READ CYCLE TIME	(TRC)	240.N	200.N	104.N
WRITE CYCLE TIME	(TWC)	256.N	208.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-100.PA	100.PA	3.31 V	-3.30 V
A1	-100.PA	100.PA	3.38 V	-3.36 V
A2	-100.PA	100.PA	3.38 V	-3.42 V
A3	-100.PA	100.PA	3.37 V	-3.40 V
A4	-100.PA	100.PA	3.42 V	-3.44 V
A5	-100.PA	100.PA	3.30 V	-3.32 V
A6	-100.PA	200.PA	3.30 V	-3.31 V
A7	-100.PA	100.PA	3.29 V	-3.30 V
CS1	-100.PA	100.PA	3.36 V	-3.36 V
CS2	-100.PA	100.PA	3.39 V	-3.40 V
MWR	-100.PA	100.PA	3.36 V	-3.38 V
MRD	-100.PA	100.PA	3.35 V	-3.33 V
DI0	-200.PA	100.PA	3.38 V	-3.36 V
DI1	-100.PA	100.PA	3.38 V	-3.31 V
DI2	-100.PA	100.PA	3.41 V	-3.33 V
DI3	0.00 A	100.PA	3.41 V	-3.35 V

	DO0	DO1	DO2	DO3
VOL1	80.0MV	80.0MV	85.0MV	85.0MV
VOL2	80.0MV	85.0MV	95.0MV	95.0MV
VOH1	4.88 V	4.89 V	4.89 V	4.89 V
VOH2	9.85 V	9.85 V	9.84 V	9.85 V
IDN1	9.45MA	9.20MA	8.70MA	8.65MA
IDN2	23.9MA	22.4MA	19.9MA	20.4MA
IDP1	-3.46MA	-3.57MA	-3.44MA	-3.46MA
IDP2	-7.93MA	-8.17MA	-7.75MA	-8.09MA
IOZ1	6.60NA	-300.PA	5.60NA	-900.PA
IOZ2	3.70NA	500.PA	4.00NA	-900.PA
IOZ3	-100.PA	4.50NA	-600.PA	4.40NA
IOZ4	4.00NA	900.PA	3.10NA	1.00NA
IOZ5	500.PA	3.80NA	1.20NA	1.80NA
IOZ6	400.PA	3.60NA	900.PA	2.20NA
IOZ7	300.PA	4.10NA	1.00NA	2.00NA
IOZ8	300.PA	3.70NA	800.PA	2.40NA

ILOP	10.0UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-15.0UA
IL4	-15.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	230.N	195.N	85.0N
DATA SETUP TIME	(TDS)	28.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	10.0N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	120.N	104.N	52.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	76.0N	68.0N	38.0N
CS1 SETUP TIME	(TCSS1)	164.N	140.N	70.0N
CS2 SETUP TIME	(TCSS2)	160.N	136.N	68.0N
CS1 HOLD TIME	(TCSH1)	46.0N	42.0N	26.0N
CS2 HOLD TIME	(TCSH2)	50.0N	44.0N	26.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	224.N	196.N	98.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	222.N	194.N	96.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	46.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	146.N	116.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	144.N	112.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	118.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	134.N	112.N	32.0N
READ CYCLE TIME	(TRC)	256.N	224.N	120.N
WRITE CYCLE TIME	(TWC)	216.N	192.N	120.N

	IIL	IIH	VIC1	VIC2
A0	-41.2NA	40.3NA	3.23 V	-3.24 V
A1	-40.9NA	40.3NA	3.32 V	-3.30 V
A2	-40.7NA	41.2NA	3.33 V	-3.38 V
A3	-41.8NA	42.0NA	3.31 V	-3.35 V
A4	-41.4NA	41.9NA	3.38 V	-3.40 V
A5	-38.8NA	39.8NA	3.24 V	-3.25 V
A6	-41.8NA	41.1NA	3.24 V	-3.25 V
A7	-41.5NA	40.6NA	3.22 V	-3.24 V
CS1	-41.9NA	42.6NA	3.28 V	-3.29 V
CS2	-43.0NA	44.3NA	3.32 V	-3.37 V
MWR	-41.0NA	42.1NA	3.29 V	-3.32 V
MRD	-42.0NA	43.1NA	3.27 V	-3.27 V
DI0	-44.7NA	40.7NA	3.33 V	-3.30 V
DI1	-40.2NA	40.5NA	3.31 V	-3.26 V
DI2	-39.6NA	41.9NA	3.35 V	-3.27 V
DI3	-39.5NA	40.5NA	3.36 V	-3.30 V

	D00	D01	D02	D03
VOL1	105.MV	105.MV	120.MV	115.MV
VOL2	115.MV	125.MV	145.MV	140.MV
VOH1	4.82 V	4.82 V	4.82 V	4.82 V
VOH2	9.76 V	9.76 V	9.74 V	9.76 V
IDN1	7.05MA	6.80MA	6.35MA	6.35MA
IDN2	16.7MA	15.4MA	13.5MA	13.8MA
IDP1	-2.18MA	-2.25MA	-2.14MA	-2.18MA
IDP2	-4.97MA	-5.12MA	-4.81MA	-5.03MA
IOZ1	372.NA	430.NA	419.NA	389.NA
IOZ2	365.NA	421.NA	424.NA	381.NA
IOZ3	364.NA	425.NA	419.NA	386.NA
IOZ4	366.NA	418.NA	427.NA	382.NA
IOZ5	367.NA	426.NA	431.NA	391.NA
IOZ6	380.NA	419.NA	430.NA	391.NA
IOZ7	370.NA	428.NA	420.NA	394.NA
IOZ8	368.NA	422.NA	431.NA	384.NA

ILDP	-5.00UA
IL1	-35.0UA
IL2	-40.0UA
IL3	-50.0UA
IL4	-45.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	230.N	205.N	95.0N
DATA SETUP TIME	(TDS)	28.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	124.N	112.N	58.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	78.0N	70.0N	42.0N
CS1 SETUP TIME	(TCSS1)	162.N	142.N	76.0N
CS2 SETUP TIME	(TCSS2)	158.N	140.N	74.0N
CS1 HOLD TIME	(TCSH1)	48.0N	44.0N	28.0N
CS2 HOLD TIME	(TCSH2)	52.0N	46.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	234.N	208.N	110.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	232.N	206.N	106.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	54.0N	48.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	146.N	116.N	36.0N
OUTPUT HOLD FROM CS2	(TDOH2)	144.N	114.N	36.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	118.N	34.0N
OUTPUT HOLD FROM MWR	(TDOH)	136.N	112.N	36.0N
READ CYCLE TIME	(TRC)	256.N	224.N	120.N
WRITE CYCLE TIME	(TWC)	216.N	192.N	128.N

	IIL	IIH	VIC1	VIC2
A0	-234.NA	229.NA	3.27 V	-3.28 V
A1	-233.NA	231.NA	3.36 V	-3.35 V
A2	-232.NA	231.NA	3.37 V	-3.42 V
A3	-237.NA	235.NA	3.35 V	-3.39 V
A4	-236.NA	237.NA	3.42 V	-3.45 V
A5	-228.NA	227.NA	3.27 V	-3.29 V
A6	-233.NA	231.NA	3.27 V	-3.28 V
A7	-234.NA	227.NA	3.25 V	-3.27 V
CS1	-243.NA	239.NA	3.32 V	-3.34 V
CS2	-241.NA	246.NA	3.36 V	-3.41 V
MWR	-236.NA	239.NA	3.33 V	-3.36 V
MRD	-241.NA	240.NA	3.31 V	-3.31 V
DI0	-234.NA	231.NA	3.37 V	-3.35 V
DI1	-227.NA	231.NA	3.35 V	-3.30 V
DI2	-229.NA	233.NA	3.39 V	-3.31 V
DI3	-228.NA	232.NA	3.40 V	-3.34 V

	D00	D01	D02	D03
VOL1	115.MV	120.MV	130.MV	130.MV
VOL2	125.MV	140.MV	160.MV	155.MV
VOH1	4.80 V	4.80 V	4.80 V	4.80 V
VOH2	9.72 V	9.72 V	9.71 V	9.72 V
IDN1	6.40MA	6.15MA	5.75MA	5.75MA
IDN2	15.0MA	13.8MA	12.1MA	12.4MA
IDP1	-1.99MA	-2.03MA	-1.94MA	-2.00MA
IDP2	-4.49MA	-4.57MA	-4.33MA	-4.56MA
IOZ1	1.41UA	1.55UA	1.61UA	1.47UA
IOZ2	1.40UA	1.55UA	1.61UA	1.47UA
IOZ3	1.39UA	1.54UA	1.61UA	1.46UA
IOZ4	1.39UA	1.53UA	1.61UA	1.47UA
IOZ5	1.40UA	1.56UA	1.63UA	1.50UA
IOZ6	1.41UA	1.55UA	1.63UA	1.48UA
IOZ7	1.41UA	1.54UA	1.62UA	1.47UA
IOZ8	1.40UA	1.54UA	1.61UA	1.48UA

ILDP	70.0UA
IL1	-160.UA
IL2	-195.UA
IL3	-165.UA
IL4	-140.UA

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN: 29

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	285.N	235.N	90.0N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	14.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	134.N	112.N	54.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	74.0N	62.0N	36.0N
CS1 SETUP TIME	(TCSS1)	180.N	152.N	74.0N
CS2 SETUP TIME	(TCSS2)	174.N	150.N	72.0N
CS1 HOLD TIME	(TCSH1)	36.0N	32.0N	22.0N
CS2 HOLD TIME	(TCSH2)	38.0N	34.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	270.N	224.N	102.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	266.N	222.N	98.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	56.0N	50.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	156.N	122.N	32.0N
OUTPUT HOLD FROM CS2	(TDOH2)	150.N	118.N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	116.N	34.0N
OUTPUT HOLD FROM MWR	(TPDH)	138.N	112.N	36.0N
READ CYCLE TIME	(TRC)	296.N	248.N	128.N
WRITE CYCLE TIME	(TWC)	264.N	232.N	120.N

	IIL	IIH	VIC1	VIC2
A0	-2.40NA	2.10NA	3.07 V	-3.05 V
A1	-2.10NA	1.90NA	3.08 V	-3.11 V
A2	-3.00NA	1.80NA	3.10 V	-3.12 V
A3	-2.00NA	2.20NA	3.07 V	-3.11 V
A4	-1.90NA	1.50NA	3.11 V	-3.13 V
A5	-2.30NA	2.00NA	3.04 V	-3.08 V
A6	-2.40NA	1.80NA	3.04 V	-3.08 V
A7	-2.20NA	2.00NA	3.04 V	-3.09 V
CS1	-1.90NA	1.90NA	3.09 V	-3.11 V
CS2	-1.90NA	2.00NA	3.13 V	-3.10 V
MWR	-2.10NA	2.20NA	3.06 V	-3.08 V
MRD	-1.80NA	2.70NA	3.08 V	-3.11 V
DI0	-2.50NA	2.60NA	3.15 V	-3.09 V
DI1	-2.10NA	2.10NA	3.13 V	-3.09 V
DI2	-2.60NA	1.90NA	3.14 V	-3.09 V
DI3	-270.NA	2.10NA	3.14 V	-3.09 V

	D00	D01	D02	D03
VOL1	120.MV	125.MV	135.MV	130.MV
VOL2	120.MV	125.MV	140.MV	140.MV
VOH1	4.84 V	4.84 V	4.84 V	4.84 V
VOH2	9.77 V	9.78 V	9.77 V	9.77 V
IDN1	6.05MA	5.90MA	5.60MA	5.60MA
IDN2	15.8MA	15.0MA	13.7MA	13.9MA
IDP1	-2.43MA	-2.41MA	-2.37MA	-2.41MA
IDP2	-5.53MA	-5.55MA	-5.36MA	-5.55MA
IOZ1	51.0NA	50.8NA	49.4NA	46.3NA
IOZ2	47.8NA	53.8NA	45.7NA	49.5NA
IOZ3	54.7NA	45.6NA	51.4NA	45.0NA
IOZ4	52.7NA	46.1NA	51.6NA	43.8NA
IOZ5	47.5NA	53.6NA	47.0NA	52.8NA
IOZ6	48.8NA	53.7NA	46.0NA	51.4NA
IOZ7	47.9NA	53.2NA	46.2NA	51.9NA
IOZ8	47.9NA	53.3NA	45.5NA	51.2NA

ILDP	-5.00UA
IL1	-20.0UA
IL2	-45.0UA
IL3	-30.0UA
IL4	-50.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	295.N	230.N	85.0N
DATA SETUP TIME	(TDS)	28.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	10.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	134.N	106.N	48.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	76.0N	68.0N	34.0N
CS1 SETUP TIME	(TCSS1)	172.N	144.N	68.0N
CS2 SETUP TIME	(TCSS2)	168.N	142.N	66.0N
CS1 HOLD TIME	(TCSH1)	38.0N	30.0N	22.0N
CS2 HOLD TIME	(TCSH2)	38.0N	34.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	266.N	216.N	94.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	266.N	214.N	90.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	52.0N	46.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	148.N	114.N	30.0N
OUTPUT HOLD FROM CS2	(TDOH2)	144.N	112.N	30.0N
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	116.N	32.0N
OUTPUT HOLD FROM MWR	(TPDH)	136.N	110.N	32.0N
READ CYCLE TIME	(TRC)	280.N	232.N	120.N
WRITE CYCLE TIME	(TWC)	240.N	208.N	112.N

	IIL	IIH	VIC1	VICP
A0	-500.PA	400.PA	3.15 V	-3.13 V
A1	-500.PA	300.PA	3.16 V	-3.18 V
A2	-900.PA	200.PA	3.17 V	-3.18 V
A3	-300.PA	500.PA	3.15 V	-3.18 V
A4	-400.PA	200.PA	3.18 V	-3.19 V
A5	-400.PA	400.PA	3.13 V	-3.14 V
A6	-500.PA	300.PA	3.13 V	-3.15 V
A7	-400.PA	300.PA	3.13 V	-3.16 V
CS1	-400.PA	400.PA	3.17 V	-3.17 V
CS2	-400.PA	400.PA	3.21 V	-3.16 V
MWR	-400.PA	400.PA	3.14 V	-3.15 V
MRD	-300.PA	700.PA	3.16 V	-3.17 V
DI0	-500.PA	500.PA	3.23 V	-3.16 V
DI1	-400.PA	300.PA	3.20 V	-3.16 V
DI2	-500.PA	400.PA	3.22 V	-3.16 V
DI3	-154.NA	400.PA	3.22 V	-3.15 V

	D00	D01	D02	D03
VOL1	110.MV	115.MV	120.MV	120.MV
VOL2	105.MV	110.MV	125.MV	120.MV
VOH1	4.86 V	4.86 V	4.86 V	4.86 V
VOH2	9.81 V	9.81 V	9.80 V	9.81 V
IDN1	6.65MA	6.45MA	6.20MA	6.20MA
IDN2	17.8MA	16.9MA	15.5MA	15.7MA
IDP1	-2.86MA	-2.84MA	-2.81MA	-2.84MA
IDP2	-6.53MA	-6.55MA	-6.37MA	-6.58MA
IOZ1	10.9NA	4.20NA	10.5NA	3.30NA
IOZ2	7.60NA	6.60NA	7.80NA	4.50NA
IOZ3	7.10NA	8.20NA	4.90NA	8.40NA
IOZ4	10.3NA	4.90NA	8.10NA	5.20NA
IOZ5	5.60NA	8.40NA	5.80NA	7.20NA
IOZ6	5.90NA	8.50NA	5.80NA	6.50NA
IOZ7	5.90NA	7.90NA	6.00NA	6.90NA
IOZ8	5.90NA	8.20NA	6.00NA	6.20NA

ILDP	-1.40UA
IL1	-15.0UA
IL2	-40.0UA
IL3	-25.0UA
IL4	-40.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	295.NS	220.NS	80.0NS
DATA SETUP TIME	(TDS)	34.0NS	24.0NS	8.00NS
DATA HOLD TIME	(TDH)	10.0NS	10.0NS	10.0NS
ADDRESS SETUP TIME	(TAS1)	12.0NS	8.00NS	4.00NS
ADDRESS SETUP TIME	(TAS2)	134.NS	104.NS	44.0NS
ADDRESS HOLD TIME	(TAH)	-18.0NS	-14.0NS	-4.00NS
WRITE PULSE WIDTH	(TWP)	84.0NS	70.0NS	32.0NS
CS1 SETUP TIME	(TCSS1)	170.NS	142.NS	64.0NS
CS2 SETUP TIME	(TCSS2)	170.NS	138.NS	62.0NS
CS1 HOLD TIME	(TCSH1)	44.0NS	32.0NS	20.0NS
CS2 HOLD TIME	(TCSH2)	48.0NS	38.0NS	20.0NS
OUTPUT ACTIVE FROM CS1	(TDOA1)	278.NS	214.NS	90.0NS
OUTPUT ACTIVE FROM CS2	(TDOA2)	276.NS	212.NS	88.0NS
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0NS	42.0NS	24.0NS
OUTPUT HOLD FROM CS1	(TDOH1)	142.NS	108.NS	26.0NS
OUTPUT HOLD FROM CS2	(TDOH2)	138.NS	104.NS	26.0NS
OUTPUT HOLD FROM MRD	(TDOH3)	136.NS	114.NS	30.0NS
OUTPUT HOLD FROM MWR	(TDOH)	134.NS	110.NS	32.0NS
READ CYCLE TIME	(TRC)	272.NS	216.NS	112.NS
WRITE CYCLE TIME	(TWC)	264.NS	208.NS	104.NS

	IIL	IIH	VIC1	VIC2
A0	-100.PA	100.PA	3.24 V	-3.21 V
A1	-100.PA	100.PA	3.24 V	-3.26 V
A2	-300.PA	100.PA	3.26 V	-3.27 V
A3	-100.PA	100.PA	3.24 V	-3.27 V
A4	-100.PA	100.PA	3.27 V	-3.28 V
A5	-100.PA	100.PA	3.21 V	-3.23 V
A6	-100.PA	100.PA	3.21 V	-3.24 V
A7	-100.PA	100.PA	3.21 V	-3.25 V
CS1	-100.PA	100.PA	3.26 V	-3.26 V
CS2	-100.PA	100.PA	3.30 V	-3.25 V
MWR	-100.PA	100.PA	3.24 V	-3.24 V
MRD	-100.PA	100.PA	3.25 V	-3.26 V
DI0	-100.PA	100.PA	3.32 V	-3.25 V
DI1	-100.PA	100.PA	3.29 V	-3.25 V
DI2	-100.PA	100.PA	3.31 V	-3.24 V
DI3	-96.1NA	100.PA	3.31 V	-3.24 V

	D00	D01	D02	D03
VOL1	105.MV	105.MV	110.MV	110.MV
VOL2	95.0MV	100.MV	110.MV	110.MV
VOH1	4.88 V	4.88 V	4.88 V	4.88 V
VOH2	9.84 V	9.84 V	9.84 V	9.84 V
IDN1	7.15MA	6.95MA	6.65MA	6.65MA
IDN2	19.6MA	18.7MA	17.2MA	17.4MA
IDP1	-3.27MA	-3.28MA	-3.25MA	-3.29MA
IDP2	-7.49MA	-7.57MA	-7.35MA	-7.60MA
IOZ1	3.10NA	2.00NA	3.20NA	500.PA
IOZ2	-300.PA	5.50NA	-500.PA	4.20NA
IOZ3	6.10NA	-500.PA	4.40NA	-100.PA
IOZ4	5.00NA	-900.PA	4.80NA	-1.20NA
IOZ5	-400.PA	4.90NA	-1.20NA	5.40NA
IOZ6	-100.PA	4.90NA	-1.20NA	5.00NA
IOZ7	-100.PA	4.50NA	-900.PA	5.00NA
IOZ8	500.PA	4.50NA	-1.10NA	4.80NA

ILDP	-15.0UA
IL1	-15.0UA
IL2	-35.0UA
IL3	-25.0UA
IL4	-40.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	280.N	235.N	100.N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	16.0N	14.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	136.N	118.N	62.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	86.0N	76.0N	42.0N
CS1 SETUP TIME	(TCSS1)	186.N	160.N	82.0N
CS2 SETUP TIME	(TCSS2)	182.N	158.N	78.0N
CS1 HOLD TIME	(TCSH1)	50.0N	44.0N	28.0N
CS2 HOLD TIME	(TCSH2)	54.0N	48.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	268.N	232.N	112.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	264.N	228.N	110.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	60.0N	52.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	160.N	126.N	36.0N
OUTPUT HOLD FROM CS2	(TDOH2)	154.N	124.N	36.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	38.0N
OUTPUT HOLD FROM MWR	(TPDH)	138.N	114.N	38.0N
READ CYCLE TIME	(TRC)	304.N	256.N	136.N
WRITE CYCLE TIME	(TWC)	256.N	224.N	136.N

	IIL	IIH	VIC1	VIC2
A0	-22.9NA	23.1NA	3.03 V	-3.01 V
A1	-23.2NA	22.1NA	3.04 V	-3.06 V
A2	-23.9NA	22.8NA	3.06 V	-3.08 V
A3	-23.0NA	22.4NA	3.03 V	-3.08 V
A4	-22.1NA	20.4NA	3.08 V	-3.10 V
A5	-24.1NA	22.3NA	3.00 V	-3.03 V
A6	-23.6NA	22.1NA	3.00 V	-3.04 V
A7	-24.2NA	21.6NA	3.00 V	-3.05 V
CS1	-21.8NA	21.2NA	3.05 V	-3.06 V
CS2	-21.8NA	22.3NA	3.10 V	-3.06 V
MWR	-22.0NA	22.5NA	3.02 V	-3.04 V
MRD	-22.3NA	24.8NA	3.04 V	-3.07 V
DI0	-24.1NA	24.6NA	3.11 V	-3.05 V
DI1	-22.6NA	22.1NA	3.09 V	-3.05 V
DI2	-23.4NA	21.6NA	3.10 V	-3.05 V
DI3	-509.NA	22.1NA	3.11 V	-3.04 V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

	D00	D01	D02	D03
VOL1	140.MV	145.MV	155.MV	150.MV
VOL2	140.MV	150.MV	165.MV	160.MV
VOH1	4.81 V	4.81 V	4.80 V	4.81 V
VOH2	9.73 V	9.74 V	9.72 V	9.73 V
IDN1	5.30MA	5.15MA	4.90MA	4.90MA
IDN2	13.6MA	12.8MA	11.7MA	11.8MA
IDP1	-2.06MA	-2.05MA	-2.01MA	-2.05MA
IDP2	-4.70MA	-4.73MA	-4.57MA	-4.73MA
IOZ1	505.NA	492.NA	492.NA	468.NA
IOZ2	506.NA	484.NA	493.NA	472.NA
IOZ3	499.NA	486.NA	496.NA	471.NA
IOZ4	505.NA	483.NA	490.NA	476.NA
IOZ5	508.NA	493.NA	509.NA	491.NA
IOZ6	510.NA	497.NA	489.NA	485.NA
IOZ7	501.NA	493.NA	496.NA	474.NA
IOZ8	513.NA	488.NA	493.NA	481.NA

ILDP	6.00UA
IL1	-40.0UA
IL2	-70.0UA
IL3	-55.0UA
IL4	-75.0UA

C-4

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	285.N	245.N	110.N
DATA SETUP TIME	(TDS)	26.0N	22.0N	10.0N
DATA HOLD TIME	(TDH)	18.0N	18.0N	16.0N
ADDRESS SETUP TIME	(TAS1)	4.00N	4.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	140.N	126.N	68.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-16.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	92.0N	82.0N	46.0N
CS1 SETUP TIME	(TCSS1)	198.N	172.N	88.0N
CS2 SETUP TIME	(TCSS2)	194.N	168.N	86.0N
CS1 HOLD TIME	(TCSH1)	54.0N	48.0N	30.0N
CS2 HOLD TIME	(TCSH2)	58.0N	52.0N	30.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	284.N	246.N	124.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	280.N	242.N	122.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	64.0N	56.0N	32.0N
OUTPUT HOLD FROM CS1	(TDOH1)	160.N	130.N	40.0N
OUTPUT HOLD FROM CS2	(TDOH2)	156.N	126.N	40.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	38.0N
OUTPUT HOLD FROM MWR	(TPDH)	140.N	116.N	38.0N
READ CYCLE TIME	(TRC)	312.N	264.N	144.N
WRITE CYCLE TIME	(TWC)	264.N	240.N	144.N

	IIL	IIH	VIC1	VIC2
A0	-125.NA	121.NA	3.02 V	-3.00 V
A1	-127.NA	123.NA	3.03 V	-3.05 V
A2	-125.NA	121.NA	3.05 V	-3.08 V
A3	-124.NA	118.NA	3.02 V	-3.07 V
A4	-120.NA	113.NA	3.06 V	-3.09 V
A5	-126.NA	120.NA	2.99 V	-3.02 V
A6	-127.NA	120.NA	2.99 V	-3.03 V
A7	-129.NA	118.NA	2.99 V	-3.04 V
CS1	-123.NA	114.NA	3.04 V	-3.05 V
CS2	-120.NA	122.NA	3.09 V	-3.05 V
MWR	-119.NA	116.NA	3.01 V	-3.03 V
MRD	-122.NA	121.NA	3.02 V	-3.06 V
DI0	-125.NA	124.NA	3.10 V	-3.04 V
DI1	-121.NA	120.NA	3.09 V	-3.04 V
DI2	-122.NA	117.NA	3.10 V	-3.04 V
DI3	-873.NA	116.NA	3.10 V	-3.04 V

	D00	D01	D02	D03
VOL1	155.MV	160.MV	170.MV	170.MV
VOL2	155.MV	165.MV	185.MV	180.MV
VOH1	4.78 V	4.78 V	4.78 V	4.78 V
VOH2	9.70 V	9.70 V	9.69 V	9.70 V
IDN1	4.80MA	4.65MA	4.45MA	4.45MA
IDN2	12.2MA	11.4MA	10.4MA	10.6MA
IDP1	-1.86MA	-1.86MA	-1.81MA	-1.84MA
IDP2	-4.24MA	-4.25MA	-4.09MA	-4.27MA
IOZ1	2.01UA	1.97UA	1.94UA	1.90UA
IOZ2	2.01UA	1.96UA	1.95UA	1.89UA
IOZ3	2.00UA	1.96UA	1.95UA	1.90UA
IOZ4	1.99UA	1.96UA	1.95UA	1.90UA
IOZ5	2.02UA	1.99UA	2.00UA	1.96UA
IOZ6	2.03UA	1.99UA	1.96UA	1.92UA
IOZ7	2.02UA	1.98UA	1.96UA	1.92UA
IOZ8	2.02UA	1.97UA	1.96UA	1.91UA

ILDP	25.0UA
IL1	-115.UA
IL2	-160.UA
IL3	-140.UA
IL4	-150.UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	235.N	200.N	85.0N
DATA SETUP TIME	(TDS)	22.0N	18.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	14.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	116.N	96.0N	48.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	70.0N	60.0N	36.0N
CS1 SETUP TIME	(TCSS1)	164.N	140.N	70.0N
CS2 SETUP TIME	(TCSS2)	286.N	284.N	70.0N
CS1 HOLD TIME	(TCSH1)	38.0N	34.0N	22.0N
CS2 HOLD TIME	(TCSH2)	32.0N	28.0N	16.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	230.N	194.N	90.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	232.N	196.N	94.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	44.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	142.N	110.N	28.0N
OUTPUT HOLD FROM CS2	(TDOH2)	144.N	114.N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	136.N	114.N	34.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	110.N	34.0N
READ CYCLE TIME	(TRC)	256.N	216.N	120.N
WRITE CYCLE TIME	(TWC)	224.N	192.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-1.70NA	1.90NA	2.96 V	-2.95 V
A1	-1.40NA	1.90NA	2.99 V	-3.00 V
A2	-2.10NA	1.40NA	3.01 V	-3.04 V
A3	-1.90NA	1.50NA	3.01 V	-3.06 V
A4	-1.60NA	1.50NA	3.05 V	-3.10 V
A5	-1.40NA	1.40NA	2.94 V	-2.98 V
A6	-2.00NA	1.40NA	2.95 V	-2.95 V
A7	-1.40NA	1.60NA	2.95 V	-2.97 V
CS1	-1.30NA	1.60NA	3.00 V	-3.02 V
CS2	-1.70NA	1.70NA	5.01 V	-4.98 V
MWR	-1.80NA	1.30NA	2.99 V	-3.01 V
MRD	-1.40NA	1.30NA	3.00 V	-3.03 V
DI0	-1.70NA	1.30NA	3.01 V	-2.97 V
DI1	-1.20NA	1.40NA	2.99 V	-2.96 V
DI2	-1.80NA	2.20NA	3.09 V	-3.02 V
DI3	-1.50NA	1.60NA	3.06 V	-3.00 V

	D00	D01	D02	D03
VOL1	95.0MV	100.MV	110.MV	105.MV
VOL2	105.MV	110.MV	125.MV	125.MV
VOH1	4.86 V	4.85 V	4.85 V	4.86 V
VOH2	9.78 V	9.78 V	9.78 V	9.79 V
IDN1	7.60MA	7.40MA	6.75MA	6.90MA
IDN2	16.3MA	17.2MA	15.1MA	15.5MA
IDP1	-2.65MA	-2.65MA	-2.57MA	-2.65MA
IDP2	-5.79MA	-5.83MA	-5.61MA	-5.85MA
IOZ1	10.9NA	16.0NA	11.4NA	15.2NA
IOZ2	10.3NA	16.6NA	10.1NA	16.7NA
IOZ3	16.2NA	9.90NA	17.0NA	9.50NA
IOZ4	13.5NA	12.1NA	14.7NA	10.8NA
IOZ5	12.0NA	14.8NA	11.3NA	15.6NA
IOZ6	11.6NA	14.8NA	11.3NA	15.7NA
IOZ7	11.7NA	15.1NA	10.7NA	15.6NA
IOZ8	11.3NA	14.7NA	11.1NA	15.9NA

ILDP	-20.0UA
IL1	-20.0UA
IL2	-20.0UA
IL3	-20.0UA
IL4	-15.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	235.N	190.N	75.0N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	110.N	92.0N	42.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	70.0N	58.0N	32.0N
CS1 SETUP TIME	(TCSS1)	154.N	130.N	62.0N
CS2 SETUP TIME	(TCSS2)	152.N	130.N	62.0N
CS1 HOLD TIME	(TCSH1)	36.0N	30.0N	20.0N
CS2 HOLD TIME	(TCSH2)	36.0N	30.0N	18.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	222.N	184.N	88.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	222.N	182.N	86.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	46.0N	40.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	132.N	102.N	24.0N
OUTPUT HOLD FROM CS2	(TDOH2)	132.N	102.N	26.0N
OUTPUT HOLD FROM MRD	(TDOH3)	132.N	112.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	128.N	106.N	32.0N
READ CYCLE TIME	(TRC)	232.N	200.N	112.N
WRITE CYCLE TIME	(TWC)	208.N	176.N	104.N

	IIL	IIH	VIC1	VIC2
A0	-300.PA	300.PA	3.02 V	-3.00 V
A1	-200.PA	300.PA	3.04 V	-3.05 V
A2	-400.PA	200.PA	3.06 V	-3.09 V
A3	-400.PA	200.PA	3.06 V	-3.11 V
A4	-200.PA	200.PA	3.11 V	-3.13 V
A5	-200.PA	200.PA	3.00 V	-3.03 V
A6	-300.PA	200.PA	3.01 V	-3.01 V
A7	-200.PA	300.PA	3.01 V	-3.02 V
CS1	-100.PA	400.PA	3.05 V	-3.08 V
CS2	-300.PA	300.PA	3.60 V	-3.60 V
MWR	-300.PA	200.PA	3.04 V	-3.06 V
MRD	-200.PA	200.PA	3.05 V	-3.08 V
DI0	-200.PA	200.PA	3.07 V	-3.02 V
DI1	-200.PA	300.PA	3.06 V	-3.01 V
DI2	-300.PA	500.PA	3.14 V	-3.08 V
DI3	-200.PA	300.PA	3.12 V	-3.05 V

	D00	D01	D02	D03
VOL1	85.0MV	85.0MV	95.0MV	90.0MV
VOL2	90.0MV	95.0MV	110.MV	105.MV
VOH1	4.88 V	4.88 V	4.88 V	4.88 V
VOH2	9.82 V	9.82 V	9.81 V	9.82 V
IDN1	8.70MA	8.50MA	7.80MA	7.90MA
IDN2	21.2MA	19.9MA	17.5MA	18.0MA
IDP1	-3.15MA	-3.15MA	-3.11MA	-3.16MA
IDP2	-6.88MA	-6.92MA	-6.74MA	-6.97MA
IOZ1	6.50NA	-600.PA	6.30NA	-800.PA
IOZ2	3.00NA	1.80NA	3.30NA	500.PA
IOZ3	2.40NA	3.30NA	800.PA	4.00NA
IOZ4	6.00NA	-100.PA	4.60NA	500.PA
IOZ5	300.PA	4.40NA	600.PA	3.80NA
IOZ6	300.PA	4.90NA	500.PA	3.60NA
IOZ7	300.PA	4.60NA	500.PA	3.90NA
IOZ8	100.PA	5.20NA	300.PA	3.60NA

ILDP	-2.80UA
IL1	-20.0UA
IL2	-15.0UA
IL3	-15.0UA
IL4	-10.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	225.N	180.N	70.0N
DATA SETUP TIME	(TDS)	28.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	6.00N	8.00N	8.00N
ADDRESS SETUP TIME	(TAS1)	14.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	106.N	88.0N	38.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	70.0N	58.0N	30.0N
CS1 SETUP TIME	(TCSS1)	146.N	126.N	58.0N
CS2 SETUP TIME	(TCSS2)	146.N	124.N	58.0N
CS1 HOLD TIME	(TCSH1)	36.0N	32.0N	20.0N
CS2 HOLD TIME	(TCSH2)	38.0N	34.0N	16.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	216.N	174.N	84.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	216.N	172.N	82.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	42.0N	36.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	126.N	94.0N	22.0N
OUTPUT HOLD FROM CS2	(TDOH2)	126.N	94.0N	24.0N
OUTPUT HOLD FROM MRD	(TDOH3)	132.N	110.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	128.N	104.N	30.0N
READ CYCLE TIME	(TRC)	216.N	184.N	104.N
WRITE CYCLE TIME	(TWC)	192.N	168.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-100.PA	100.PA	3.08 V	-3.07 V
A1	-100.PA	100.PA	3.11 V	-3.12 V
A2	-100.PA	0.00 A	3.01 V	-3.14 V
A3	-100.PA	100.PA	3.12 V	-3.16 V
A4	-100.PA	0.00 A	3.15 V	-3.19 V
A5	0.00 A	100.PA	3.06 V	-3.10 V
A6	-100.PA	100.PA	3.08 V	-3.08 V
A7	-100.PA	100.PA	3.08 V	-3.09 V
CS1	0.00 A	100.PA	3.12 V	-3.13 V
CS2	-100.PA	100.PA	3.69 V	-3.68 V
MWR	-100.PA	100.PA	3.10 V	-3.12 V
MRD	-100.PA	0.00 A	3.12 V	-3.13 V
DI0	-100.PA	0.00 A	3.13 V	-3.09 V
DI1	0.00 A	100.PA	3.12 V	-3.08 V
DI2	-100.PA	200.PA	3.20 V	-3.13 V
DI3	0.00 A	100.PA	3.17 V	-3.12 V

	D00	D01	D02	D03
VOL1	75.0MV	75.0MV	85.0MV	85.0MV
VOL2	80.0MV	85.0MV	95.0MV	95.0MV
VOH1	4.89 V	4.89 V	4.89 V	4.89 V
VOH2	9.85 V	9.84 V	9.84 V	9.85 V
IDN1	9.70MA	9.50MA	8.70MA	8.80MA
IDN2	23.7MA	22.4MA	19.8MA	20.3MA
IDP1	-3.66MA	-3.70MA	-3.61MA	-3.71MA
IDP2	-7.95MA	-8.05MA	-7.80MA	-8.10MA
IOZ1	-200.PA	3.80NA	-1.50NA	4.20NA
IOZ2	2.90NA	400.PA	1.60NA	1.20NA
IOZ3	700.PA	1.80NA	1.20NA	300.PA
IOZ4	-1.60NA	5.20NA	-1.80NA	4.10NA
IOZ5	5.50NA	-1.60NA	3.90NA	-1.20NA
IOZ6	5.20NA	-1.60NA	4.30NA	-1.20NA
IOZ7	5.50NA	-1.70NA	4.20NA	-1.30NA
IOZ8	5.30NA	-1.70NA	4.60NA	-1.40NA

ILDP	-1.20UA
IL1	-20.0UA
IL2	-15.0UA
IL3	-15.0UA
IL4	-10.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	240.N	210.N	95.0N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	120.N	104.N	54.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	82.0N	72.0N	42.0N
CS1 SETUP TIME	(TCSS1)	174.N	150.N	78.0N
CS2 SETUP TIME	(TCSS2)	170.N	148.N	76.0N
CS1 HOLD TIME	(TCSH1)	52.0N	46.0N	26.0N
CS2 HOLD TIME	(TCSH2)	54.0N	48.0N	26.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	240.N	208.N	104.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	236.N	206.N	102.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	56.0N	50.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	148.N	116.N	34.0N
OUTPUT HOLD FROM CS2	(TDOH2)	144.N	114.N	34.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	118.N	36.0N
OUTPUT HOLD FROM MWR	(TPOH)	134.N	112.N	36.0N
READ CYCLE TIME	(TRC)	264.N	232.N	128.N
WRITE CYCLE TIME	(TWC)	232.N	208.N	128.N

	IIL	IIH	VIC1	VIC2
A0	-21.6NA	22.5NA	2.94 V	-2.92 V
A1	-20.7NA	22.9NA	2.97 V	-2.98 V
A2	-22.7NA	21.3NA	2.98 V	-3.02 V
A3	-23.7NA	21.8NA	2.99 V	-3.04 V
A4	-22.2NA	22.3NA	3.04 V	-3.08 V
A5	-21.1NA	20.9NA	2.91 V	-2.94 V
A6	-21.1NA	20.4NA	2.93 V	-2.91 V
A7	-20.1NA	20.5NA	2.93 V	-2.93 V
CS1	-22.1NA	22.0NA	2.98 V	-3.00 V
CS2	-22.3NA	22.8NA	3.03 V	-3.04 V
MWR	-22.7NA	21.4NA	2.96 V	-2.99 V
MRD	-21.8NA	21.8NA	2.97 V	-3.01 V
DI0	-20.9NA	20.2NA	2.98 V	-2.94 V
DI1	-19.5NA	20.3NA	2.96 V	-2.93 V
DI2	-21.7NA	22.6NA	3.06 V	-3.00 V
DI3	-20.8NA	22.1NA	3.03 V	-2.98 V

	D00	D01	D02	D03
VOL1	115.MV	120.MV	130.MV	130.MV
VOL2	125.MV	130.MV	155.MV	150.MV
VOH1	4.82 V	4.82 V	4.82 V	4.82 V
VOH2	9.74 V	9.75 V	9.74 V	9.75 V
IDN1	6.40MA	6.20MA	5.70MA	5.80MA
IDN2	15.3MA	14.3MA	12.6MA	13.0MA
IDP1	-2.20MA	-2.21MA	-2.15MA	-2.19MA
IDP2	-4.88MA	-4.91MA	-4.71MA	-4.92MA
IOZ1	134.NA	130.NA	141.NA	132.NA
IOZ2	133.NA	131.NA	134.NA	138.NA
IOZ3	133.NA	128.NA	138.NA	135.NA
IOZ4	131.NA	133.NA	131.NA	140.NA
IOZ5	133.NA	131.NA	137.NA	141.NA
IOZ6	122.NA	140.NA	136.NA	134.NA
IOZ7	128.NA	131.NA	145.NA	131.NA
IOZ8	131.NA	136.NA	133.NA	141.NA

ILDP	-10.0UA
IL1	-35.0UA
IL2	-35.0UA
IL3	-35.0UA
IL4	-25.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	255.N	220.N	105.N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	14.0N	14.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	4.00N	4.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	128.N	114.N	62.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-16.0N	-6.00N
WRITE PULSE WIDTH	(TWP)	48.0N	78.0N	44.0N
CS1 SETUP TIME	(TCSS1)	184.N	162.N	86.0N
CS2 SETUP TIME	(TCSS2)	182.N	158.N	84.0N
CS1 HOLD TIME	(TCSH1)	54.0N	48.0N	30.0N
CS2 HOLD TIME	(TCSH2)	58.0N	50.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	258.N	226.N	114.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	254.N	224.N	114.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	60.0N	54.0N	32.0N
OUTPUT HOLD FROM CS1	(TDOH1)	154.N	122.N	38.0N
OUTPUT HOLD FROM CS2	(TDOH2)	150.N	120.N	38.0N
OUTPUT HOLD FROM MRD	(TDOH3)	140.N	118.N	38.0N
OUTPUT HOLD FROM MWR	(TPDH)	136.N	114.N	40.0N
READ CYCLE TIME	(TRC)	280.N	248.N	136.N
WRITE CYCLE TIME	(TWC)	248.N	224.N	136.N

	IIL	IIH	VIC1	VIC2
A0	-125.NA	123.NA	2.93 V	-2.91 V
A1	-124.NA	125.NA	2.96 V	-2.97 V
A2	-127.NA	124.NA	2.98 V	-3.02 V
A3	-132.NA	123.NA	2.99 V	-3.04 V
A4	-131.NA	128.NA	3.04 V	-3.08 V
A5	-121.NA	118.NA	2.90 V	-2.94 V
A6	-121.NA	115.NA	2.92 V	-2.91 V
A7	-118.NA	115.NA	2.91 V	-2.93 V
CS1	-133.NA	124.NA	2.97 V	-3.00 V
CS2	-130.NA	129.NA	3.01 V	-3.03 V
MWR	-130.NA	124.NA	2.96 V	-2.98 V
MRD	-130.NA	125.NA	2.97 V	-3.01 V
DI0	-117.NA	117.NA	2.97 V	-2.93 V
DI1	-115.NA	116.NA	2.96 V	-2.91 V
DI2	-124.NA	122.NA	3.06 V	-2.99 V
DI3	-120.NA	123.NA	3.03 V	-2.97 V

	D00	D01	D02	D03
VOL1	130.MV	135.MV	150.MV	145.MV
VOL2	140.MV	150.MV	170.MV	170.MV
VOH1	4.80 V	4.80 V	4.80 V	4.80 V
VOH2	9.72 V	9.72 V	9.70 V	9.71 V
IDN1	5.65MA	5.50MA	5.05MA	5.15MA
IDN2	13.6MA	12.6MA	11.2MA	11.4MA
IDP1	-1.97MA	-1.99MA	-1.93MA	-1.98MA
IDP2	-4.34MA	-4.41MA	-4.23MA	-4.39MA
IOZ1	534.NA	578.NA	579.NA	564.NA
IOZ2	531.NA	569.NA	584.NA	562.NA
IOZ3	527.NA	569.NA	579.NA	561.NA
IOZ4	532.NA	561.NA	583.NA	564.NA
IOZ5	531.NA	571.NA	593.NA	573.NA
IOZ6	542.NA	569.NA	579.NA	577.NA
IOZ7	528.NA	576.NA	579.NA	569.NA
IOZ8	535.NA	562.NA	587.NA	567.NA
ILDP	20.0UA			
IL1	-85.0UA			
IL2	-100.UA			
IL3	-85.0UA			
IL4	-70.0UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	265.N	220.N	95.0N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	10.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	18.0N	14.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	124.N	106.N	54.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-16.0N	-6.00N
WRITE PULSE WIDTH	(TWP)	76.0N	64.0N	38.0N
$\overline{CS}_1$ SETUP TIME	(TCSS1)	180.N	154.N	78.0N
CS2 SETUP TIME	(TCSS2)	174.N	150.N	76.0N
$\overline{CS}_1$ HOLD TIME	(TCSH1)	38.0N	34.0N	22.0N
CS2 HOLD TIME	(TCSH2)	40.0N	34.0N	22.0N
OUTPUT ACTIVE FROM $\overline{CS}_1$	(TDOA1)	248.N	214.N	102.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	246.N	212.N	98.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	56.0N	50.0N	28.0N
OUTPUT HOLD FROM $\overline{CS}_1$	(TDOH1)	150.N	118.N	32.0N
OUTPUT HOLD FROM CS2	(TDOH2)	146.N	116.N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	36.0N
OUTPUT HOLD FROM MWR	(TPDH)	134.N	112.N	38.0N
READ CYCLE TIME	(TRC)	272.N	232.N	128.N
WRITE CYCLE TIME	(TWC)	256.N	192.N	120.N

	IIL	IIH	VIC1	VIC2
A0	-1.70NA	1.30NA	3.00 V	-2.98 V
A1	-1.40NA	1.20NA	3.02 V	-3.04 V
A2	-1.70NA	1.50NA	3.03 V	-3.09 V
A3	-1.30NA	1.30NA	3.05 V	-3.05 V
A4	-1.30NA	1.30NA	3.05 V	-3.08 V
A5	-1.40NA	1.30NA	3.03 V	-3.05 V
A6	-1.60NA	1.60NA	2.99 V	-3.06 V
A7	-1.90NA	1.40NA	3.01 V	-3.04 V
CS1	-1.40NA	1.20NA	3.05 V	-3.02 V
CS2	-1.40NA	1.50NA	3.08 V	-3.07 V
MWR	-2.00NA	1.30NA	3.01 V	-3.01 V
MRD	-1.60NA	1.40NA	2.98 V	-3.02 V
DI0	-1.60NA	1.20NA	3.13 V	-3.07 V
DI1	-2.60NA	1.20NA	3.13 V	-3.06 V
DI2	-1.40NA	1.30NA	3.13 V	-3.04 V
DI3	-1.30NA	1.30NA	3.13 V	-3.07 V

	D00	D01	D02	D03
VOL1	110.MV	115.MV	125.MV	125.MV
VOL2	115.MV	125.MV	140.MV	140.MV
VOH1	4.84 V	4.83 V	4.83 V	4.84 V
VOH2	9.76 V	9.76 V	9.76 V	9.76 V
IDN1	6.65MA	6.40MA	6.05MA	6.05MA
IDN2	16.3MA	15.1MA	13.6MA	13.8MA
IDP1	-2.35MA	-2.35MA	-2.31MA	-2.33MA
IDP2	-5.23MA	-5.22MA	-5.06MA	-5.24MA
IOZ1	28.0NA	24.8NA	29.7NA	23.4NA
IOZ2	24.1NA	27.9NA	26.2NA	26.8NA
IOZ3	29.7NA	23.1NA	30.5NA	23.4NA
IOZ4	29.5NA	22.1NA	31.6NA	21.6NA
IOZ5	24.1NA	29.1NA	25.2NA	29.3NA
IOZ6	23.7NA	28.6NA	25.3NA	29.2NA
IOZ7	24.5NA	29.1NA	25.1NA	28.8NA
IOZ8	23.9NA	28.8NA	25.2NA	28.6NA

ILDP	-15.0UA
IL1	-30.0UA
IL2	-25.0UA
IL3	-30.0UA
IL4	-25.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	260.N	215.N	85.0N
DATA SETUP TIME	(TDS)	26.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	18.0N	14.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	120.N	98.0N	48.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	78.0N	60.0N	36.0N
CS1 SETUP TIME	(TCSS1)	170.N	146.N	70.0N
CS2 SETUP TIME	(TCSS2)	166.N	142.N	70.0N
CS1 HOLD TIME	(TCSH1)	36.0N	32.0N	22.0N
CS2 HOLD TIME	(TCSH2)	38.0N	34.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	244.N	202.N	94.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	240.N	200.N	90.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	52.0N	46.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	142.N	110.N	28.0N
OUTPUT HOLD FROM CS2	(TDOH2)	140.N	108.N	28.0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	114.N	32.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	110.N	34.0N
READ CYCLE TIME	(TRC)	256.N	216.N	120.N
WRITE CYCLE TIME	(TWC)	248.N	248.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-400.PA	200.PA	3.07 V	-3.04 V
A1	-200.PA	200.PA	3.09 V	-3.11 V
A2	-300.PA	200.PA	3.09 V	-3.14 V
A3	-200.PA	200.PA	3.11 V	-3.11 V
A4	-300.PA	200.PA	3.11 V	-3.13 V
A5	-200.PA	200.PA	3.09 V	-3.12 V
A6	-300.PA	300.PA	3.05 V	-3.13 V
A7	-400.PA	200.PA	3.08 V	-3.11 V
CS1	-200.PA	200.PA	3.12 V	-3.09 V
CS2	-200.PA	300.PA	3.14 V	-3.13 V
MWR	-300.PA	200.PA	3.08 V	-3.07 V
MRD	-400.PA	500.PA	3.05 V	-3.09 V
DI0	-300.PA	200.PA	3.19 V	-3.13 V
DI1	-600.PA	200.PA	3.18 V	-3.12 V
DI2	-200.PA	200.PA	3.19 V	-3.11 V
DI3	-200.PA	200.PA	3.18 V	-3.13 V

	D00	D01	D02	D03
VOL1	100.MV	105.MV	110.MV	110.MV
VOL2	100.MV	110.MV	120.MV	120.MV
VOH1	4.86 V	4.86 V	4.86 V	4.86 V
VOH2	9.80 V	9.80 V	9.80 V	9.80 V
IDN1	7.50MA	7.15MA	6.85MA	6.80MA
IDN2	18.7MA	17.3MA	15.7MA	15.9MA
IDP1	-2.79MA	-2.81MA	-2.77MA	-2.78MA
IDP2	-6.21MA	-6.29MA	-6.11MA	-6.23MA
IOZ1	2.50NA	6.80NA	1.40NA	6.80NA
IOZ2	5.20NA	3.50NA	3.70NA	4.10NA
IOZ3	4.00NA	3.30NA	4.80NA	2.40NA
IOZ4	1.20NA	6.90NA	1.80NA	5.80NA
IOZ5	7.20NA	1.40NA	6.50NA	2.00NA
IOZ6	7.50NA	1.40NA	6.10NA	2.10NA
IOZ7	6.90NA	1.50NA	6.30NA	2.10NA
IOZ8	7.30NA	1.60NA	6.00NA	2.10NA

ILDP	-5.00UA
IL1	-25.0UA
IL2	-20.0UA
IL3	-25.0UA
IL4	-20.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	255.N	205.N	80.0N
DATA SETUP TIME	(TDS)	32.0N	24.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	118.N	96.0N	42.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	82.0N	60.0N	36.0N
CS1 SETUP TIME	(TCSS1)	166.N	136.N	66.0N
CS2 SETUP TIME	(TCSS2)	162.N	138.N	64.0N
CS1 HOLD TIME	(TCSH1)	42.0N	34.0N	22.0N
CS2 HOLD TIME	(TCSH2)	44.0N	38.0N	20.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	246.N	198.N	88.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	242.N	196.N	86.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	48.0N	42.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	136.N	102.N	24.0N
OUTPUT HOLD FROM CS2	(TDOH2)	132.N	100.N	24.0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	112.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	108.N	32.0N
READ CYCLE TIME	(TRC)	232.N	200.N	120.N
WRITE CYCLE TIME	(TWC)	240.N	272.N	104.N

	IIL	IIH	VIC1	VIC2
A0	-100.PA	100.PA	3.14 V	-3.13 V
A1	-100.PA	0.00 A	3.17 V	-3.18 V
A2	-100.PA	100.PA	3.16 V	-3.21 V
A3	0.00 A	100.PA	3.18 V	-3.18 V
A4	-100.PA	100.PA	3.18 V	-3.20 V
A5	0.00 A	100.PA	3.16 V	-3.19 V
A6	-100.PA	100.PA	3.13 V	-3.20 V
A7	-100.PA	100.PA	3.15 V	-3.18 V
CS1	-100.PA	100.PA	3.20 V	-3.16 V
CS2	-100.PA	100.PA	3.21 V	-3.20 V
MWR	-100.PA	0.00 A	3.15 V	-3.15 V
MRD	-100.PA	200.PA	3.13 V	-3.16 V
DI0	-100.PA	0.00 A	3.27 V	-3.20 V
DI1	-200.PA	0.00 A	3.26 V	-3.19 V
DI2	-100.PA	100.PA	3.27 V	-3.18 V
DI3	0.00 A	100.PA	3.26 V	-3.20 V

	D00	D01	D02	D03
VOL1	90.0MV	95.0MV	100.MV	100.MV
VOL2	90.0MV	100.MV	110.MV	105.MV
VOH1	4.88 V	4.88 V	4.88 V	4.88 V
VOH2	9.83 V	9.83 V	9.83 V	9.84 V
ION1	8.15MA	7.80MA	7.45MA	7.40MA
ION2	20.7MA	19.2MA	17.5MA	17.7MA
IOP1	-3.18MA	-3.25MA	-3.21MA	-3.21MA
IOP2	-7.10MA	-7.19MA	-7.03MA	-7.18MA
IOZ1	4.80NA	400.PA	2.70NA	1.30NA
IOZ2	5.70NA	-1.70NA	5.40NA	-1.30NA
IOZ3	-1.30NA	5.30NA	-1.50NA	5.50NA
IOZ4	400.PA	3.40NA	-800.PA	4.40NA
IOZ5	4.20NA	-1.10NA	4.60NA	-1.50NA
IOZ6	4.40NA	-1.30NA	4.50NA	-1.50NA
IOZ7	4.30NA	-1.20NA	4.70NA	-1.60NA
IOZ8	4.50NA	-1.40NA	4.70NA	-1.50NA

ILOP	-10.0UA
IL1	-20.0UA
IL2	-20.0UA
IL3	-20.0UA
IL4	-15.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	265.N	225.N	105.N
DATA SETUP TIME	(TDS)	26.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	14.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	10.0N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	132.N	114.N	60.0N
ADDRESS HOLD TIME	(TAH)	-20.0N	-18.0N	-6.00N
WRITE PULSE WIDTH	(TWP)	86.0N	76.0N	44.0N
CS1 SETUP TIME	(TCSS1)	188.N	162.N	86.0N
CS2 SETUP TIME	(TCSS2)	184.N	158.N	84.0N
CS1 HOLD TIME	(TCSH1)	50.0N	46.0N	30.0N
CS2 HOLD TIME	(TCSH2)	54.0N	48.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	256.N	226.N	114.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	254.N	222.N	112.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	60.0N	54.0N	32.0N
OUTPUT HOLD FROM CS1	(TDOH1)	156.N	124.N	38.0N
OUTPUT HOLD FROM CS2	(TDOH2)	154.N	122.N	38.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	118.N	38.0N
OUTPUT HOLD FROM MWR	(TPDH)	136.N	114.N	40.0N
READ CYCLE TIME	(TRC)	280.N	248.N	136.N
WRITE CYCLE TIME	(TWC)	248.N	224.N	136.N

	IIL	IIH	VIC1	VIC2
A0	-19.3NA	18.5NA	2.97 V	-2.94 V
A1	-19.0NA	18.2NA	2.99 V	-3.00 V
A2	-18.9NA	19.3NA	3.00 V	-3.05 V
A3	-18.5NA	18.3NA	3.02 V	-3.02 V
A4	-17.9NA	18.1NA	3.02 V	-3.05 V
A5	-19.2NA	18.5NA	3.00 V	-3.02 V
A6	-19.1NA	18.7NA	2.96 V	-3.03 V
A7	-20.2NA	18.5NA	2.98 V	-3.01 V
CS1	-18.6NA	17.6NA	3.02 V	-2.99 V
CS2	-17.9NA	19.9NA	3.05 V	-3.05 V
MWR	-18.5NA	17.9NA	2.98 V	-2.98 V
MRD	-18.9NA	18.5NA	2.95 V	-2.99 V
DI0	-18.6NA	18.0NA	3.11 V	-3.04 V
DI1	-20.5NA	18.1NA	3.10 V	-3.03 V
DI2	-17.1NA	17.6NA	3.10 V	-3.01 V
DI3	-17.3NA	17.6NA	3.10 V	-3.04 V

	D00	D01	D02	D03
VOL1	130.MV	135.MV	145.MV	145.MV
VOL2	140.MV	150.MV	165.MV	165.MV
VOH1	4.80 V	4.80 V	4.80 V	4.80 V
VOH2	9.72 V	9.72 V	9.71 V	9.72 V
IDN1	5.75MA	5.50MA	5.20MA	5.20MA
IDN2	13.8MA	12.7MA	11.5MA	11.7MA
IDP1	-1.97MA	-1.99MA	-1.95MA	-1.96MA
IDP2	-4.41MA	-4.45MA	-4.31MA	-4.42MA
IOZ1	281.NA	290.NA	291.NA	279.NA
IOZ2	278.NA	284.NA	295.NA	272.NA
IOZ3	275.NA	285.NA	294.NA	276.NA
IOZ4	278.NA	279.NA	300.NA	273.NA
IOZ5	279.NA	287.NA	304.NA	281.NA
IOZ6	291.NA	281.NA	300.NA	285.NA
IOZ7	280.NA	292.NA	295.NA	283.NA
IOZ8	283.NA	279.NA	307.NA	277.NA

TLDP	1.80UA
IL1	-45.0UA
IL2	-40.0UA
IL3	-45.0UA
IL4	-40.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	270.N	235.N	115.N
DATA SETUP TIME	(TDS)	26.0N	22.0N	10.0N
DATA HOLD TIME	(TDH)	16.0N	16.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	6.00N	6.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	140.N	124.N	68.0N
ADDRESS HOLD TIME	(TAH)	-20.0N	-18.0N	-8.00N
WRITE PULSE WIDTH	(TWP)	94.0N	84.0N	48.0N
CS1 SETUP TIME	(TCSS1)	198.N	174.N	94.0N
CS2 SETUP TIME	(TCSS2)	194.N	170.N	90.0N
CS1 HOLD TIME	(TCSH1)	56.0N	50.0N	30.0N
CS2 HOLD TIME	(TCSH2)	58.0N	52.0N	30.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	270.N	238.N	126.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	266.N	234.N	122.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	66.0N	58.0N	34.0N
OUTPUT HOLD FROM CS1	(TDOH1)	158.N	128.N	42.0N
OUTPUT HOLD FROM CS2	(TDOH2)	156.N	126.N	42.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	118.N	40.0N
OUTPUT HOLD FROM MWR	(TPDH)	140.N	116.N	40.0N
READ CYCLE TIME	(TRC)	296.N	256.N	152.N
WRITE CYCLE TIME	(TWC)	264.N	240.N	144.N

	IIL	IIH	VIC1	VIC2
A0	-110.NA	107.NA	2.97 V	-2.94 V
A1	-110.NA	108.NA	2.99 V	-3.00 V
A2	-107.NA	108.NA	3.00 V	-3.06 V
A3	-106.NA	104.NA	3.02 V	-3.02 V
A4	-105.NA	104.NA	3.02 V	-3.06 V
A5	-110.NA	107.NA	3.00 V	-3.02 V
A6	-109.NA	104.NA	2.95 V	-3.03 V
A7	-112.NA	105.NA	2.98 V	-3.00 V
CS1	-109.NA	102.NA	3.02 V	-2.99 V
CS2	-104.NA	108.NA	3.05 V	-3.05 V
MWR	-104.NA	101.NA	2.98 V	-2.97 V
MRD	-105.NA	104.NA	2.95 V	-2.99 V
DI0	-106.NA	105.NA	3.11 V	-3.04 V
DI1	-108.NA	103.NA	3.10 V	-3.02 V
DI2	-99.8NA	99.5NA	3.10 V	-3.01 V
DI3	-99.9NA	101.NA	3.10 V	-3.04 V

	D00	D01	D02	D03
VOL1	145.MV	150.MV	160.MV	160.MV
VOL2	155.MV	170.MV	190.MV	185.MV
VOH1	4.78 V	4.78 V	4.77 V	4.78 V
VOH2	9.68 V	9.68 V	9.67 V	9.68 V
IDN1	5.15MA	4.90MA	4.65MA	4.70MA
IDN2	12.3MA	11.3MA	10.2MA	10.4MA
IDP1	-1.78MA	-1.78MA	-1.75MA	-1.78MA
IDP2	-3.97MA	-3.95MA	-3.88MA	-3.99MA
IOZ1	1.23UA	1.23UA	1.27UA	1.21UA
IOZ2	1.21UA	1.23UA	1.26UA	1.22UA
IOZ3	1.22UA	1.22UA	1.27UA	1.21UA
IOZ4	1.21UA	1.22UA	1.26UA	1.22UA
IOZ5	1.23UA	1.24UA	1.30UA	1.25UA
IOZ6	1.24UA	1.24UA	1.29UA	1.22UA
IOZ7	1.23UA	1.24UA	1.28UA	1.22UA
IOZ8	1.22UA	1.24UA	1.27UA	1.23UA

ILDP	40.0UA
IL1	-105.UA
IL2	-110.UA
IL3	-110.UA
IL4	-90.0UA

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN: 32

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

FAILED DATA RETENTION TEST ADD = 16 DIAG = 0 PIN: 0I7

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	265.N	215.N	85.0N
DATA SETUP TIME	(TDS)	18.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	124.N	100.N	44.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	64.0N	56.0N	32.0N
CS1 SETUP TIME	(TCSS1)	0.00	0.00	60.0N
CS2 SETUP TIME	(TCSS2)	0.00	0.00	56.0N
CS1 HOLD TIME	(TCSH1)	0.00	0.00	14.0N
CS2 HOLD TIME	(TCSH2)	0.00	0.00	14.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	0.00	0.00	82.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	0.00	0.00	80.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	52.0N	46.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	300.N	300.N	18.0N
OUTPUT HOLD FROM CS2	(TDOH2)	300.N	300.N	20.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	32.0N
OUTPUT HOLD FROM MWR	(TPDH)	136.N	110.N	32.0N
READ CYCLE TIME	(TRC)	280.N	224.N	120.N
WRITE CYCLE TIME	(TWC)	192.N	176.N	104.N

	IIL	IIH	VIC1	VIC2
A0	-12.0NA	3.60NA	3.10 V	-3.10 V
A1	-16.6NA	3.70NA	3.15 V	-3.14 V
A2	-8.20NA	2.80NA	3.15 V	-3.17 V
A3	-6.40NA	2.70NA	3.16 V	-3.15 V
A4	-9.30NA	2.70NA	3.18 V	-3.18 V
A5	-3.40NA	3.40NA	3.09 V	-3.15 V
A6	-3.00NA	3.40NA	3.11 V	-3.14 V
A7	-2.70NA	2.90NA	3.12 V	-3.14 V
CS1	-3.20NA	4.00NA	3.15 V	-3.15 V
CS2	-3.00NA	3.30NA	3.17 V	-3.17 V
MWR	-5.40NA	2.90NA	3.11 V	-3.11 V
MRD	-3.40NA	2.80NA	3.14 V	-3.13 V
DI0	-2.60NA	2.90NA	3.23 V	-3.19 V
DI1	-2.50NA	2.90NA	3.20 V	-3.17 V
DI2	-2.80NA	3.20NA	3.22 V	-3.19 V
DI3	-3.20NA	3.00NA	3.22 V	-3.16 V

	D00	D01	D02	D03
VOL1	105.MV	110.MV	120.MV	115.MV
VOL2	110.MV	120.MV	130.MV	130.MV
VOH1	4.86 V	4.85 V	4.85 V	4.86 V
VOH2	9.78 V	9.78 V	9.78 V	9.79 V
IDN1	6.80MA	6.50MA	6.15MA	6.25MA
IDN2	17.4MA	15.9MA	14.3MA	14.7MA
IDP1	-2.66MA	-2.64MA	-2.59MA	-2.67MA
IDP2	-5.81MA	-5.81MA	-5.62MA	-5.91MA
IOZ1	10.2UA	10.2UA	10.2UA	10.2UA
IOZ2	12.3NA	9.70NA	9.50NA	10.2NA
IOZ3	10.2UA	10.2UA	10.2UA	10.2UA
IOZ4	10.0NA	12.3NA	7.10NA	12.4NA
IOZ5	-10.2UA	-10.2UA	-10.2UA	-10.2UA
IOZ6	13.2NA	9.90NA	12.2NA	7.80NA
IOZ7	13.3NA	9.10NA	12.4NA	7.60NA
IOZ8	13.5NA	8.90NA	12.4NA	7.10NA

ILDP	190.UA
IL1	-10.0UA
IL2	-10.0UA
IL3	-10.0UA
IL4	-15.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

FAILED DATA RETENTION TEST ADD = 16 DIAG = 0 PIN: 017

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	285.N	210.N	75.0N
DATA SETUP TIME	(TDS)	20.0N	16.0N	6.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	10.0N
ADDRESS SETUP TIME	(TAS1)	12.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	126.N	100.N	40.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	66.0N	58.0N	30.0N
CS1 SETUP TIME	(TCSS1)	0.00	0.00	54.0N
CS2 SETUP TIME	(TCSS2)	0.00	0.00	52.0N
CS1 HOLD TIME	(TCSH1)	0.00	0.00	10.0N
CS2 HOLD TIME	(TCSH2)	0.00	0.00	10.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	0.00	0.00	74.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	0.00	0.00	72.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	42.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	300.N	300.N	14.0N
OUTPUT HOLD FROM CS2	(TDOH2)	300.N	300.N	14.0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	112.N	30.0N
OUTPUT HOLD FROM MWR	(TPOH)	134.N	160.N	30.0N
READ CYCLE TIME	(TRC)	256.N	208.N	112.N
WRITE CYCLE TIME	(TWC)	192.N	176.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-500.PA	300.PA	3.17 V	-3.18 V
A1	-800.PA	400.PA	3.22 V	-3.22 V
A2	-500.PA	300.PA	3.22 V	-3.24 V
A3	-500.PA	300.PA	3.24 V	-3.23 V
A4	-400.PA	400.PA	3.25 V	-3.26 V
A5	-300.PA	400.PA	3.16 V	-3.22 V
A6	-400.PA	400.PA	3.18 V	-3.22 V
A7	-300.PA	300.PA	3.19 V	-3.22 V
CS1	-400.PA	500.PA	3.22 V	-3.23 V
CS2	-300.PA	300.PA	3.24 V	-3.24 V
MWR	-800.PA	400.PA	3.18 V	-3.18 V
MRD	-400.PA	300.PA	3.22 V	-3.21 V
DI0	-300.PA	300.PA	3.30 V	-3.26 V
DI1	-300.PA	300.PA	3.28 V	-3.24 V
DI2	-300.PA	400.PA	3.29 V	-3.26 V
DI3	-400.PA	400.PA	3.29 V	-3.23 V

	D00	D01	D02	D03
VOL1	95.0MV	100.MV	105.MV	105.MV
VOL2	95.0MV	100.MV	115.MV	110.MV
VOH1	4.88 V	4.88 V	4.88 V	4.88 V
VOH2	9.82 V	9.82 V	9.82 V	9.83 V
IDN1	7.60MA	7.25MA	6.95MA	7.00MA
IDN2	19.9MA	18.3MA	16.5MA	17.0MA
IDP1	-3.11MA	-3.13MA	-3.08MA	-3.13MA
IDP2	-6.84MA	-6.88MA	-6.67MA	-6.95MA
IOZ1	11.5NA	3.10NA	9.40NA	3.50NA
IOZ2	7.30NA	500.PA	6.80NA	-100.PA
IOZ3	12.2NA	18.3NA	15.1NA	21.6NA
IOZ4	5.10NA	3.00NA	3.40NA	3.90NA
IOZ5	-10.2UA	-10.2UA	-10.2UA	-10.2UA
IOZ6	1.40NA	6.90NA	700.PA	6.40NA
IOZ7	1.50NA	7.20NA	600.PA	6.30NA
IOZ8	1.50NA	7.00NA	800.PA	6.30NA

ILDP	155.UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-10.0UA
IL4	-10.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

FAILED DATA RETENTION TEST ADD = 16 DIAG = 0 PIN: Ø17

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	285.N	200.N	70.0N
DATA SETUP TIME	(TDS)	24.0N	18.0N	6.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	12.0N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	130.N	98.0N	36.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	70.0N	54.0N	30.0N
CS1 SETUP TIME	(TCSS1)	0.00	0.00	52.0N
CS2 SETUP TIME	(TCSS2)	0.00	0.00	48.0N
CS1 HOLD TIME	(TCSH1)	0.00	0.00	12.0N
CS2 HOLD TIME	(TCSH2)	0.00	0.00	12.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	0.00	0.00	70.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	0.00	0.00	66.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	44.0N	38.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	300.N	300.N	12.0N
OUTPUT HOLD FROM CS2	(TDOH2)	300.N	300.N	12.0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	110.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	106.N	28.0N
READ CYCLE TIME	(TRC)	232.N	200.N	104.N
WRITE CYCLE TIME	(TWC)	184.N	176.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-100.PA	100.PA	3.24 V	-3.25 V
A1	-100.PA	100.PA	3.29 V	-3.29 V
A2	-100.PA	100.PA	3.29 V	-3.31 V
A3	-100.PA	100.PA	3.30 V	-3.29 V
A4	-100.PA	100.PA	3.32 V	-3.32 V
A5	-100.PA	100.PA	3.23 V	-3.29 V
A6	-100.PA	100.PA	3.25 V	-3.29 V
A7	-100.PA	100.PA	3.26 V	-3.29 V
CS1	-100.PA	100.PA	3.29 V	-3.29 V
CS2	-100.PA	100.PA	3.31 V	-3.30 V
MWR	-200.PA	100.PA	3.25 V	-3.24 V
MRD	-100.PA	100.PA	3.29 V	-3.28 V
DI0	-100.PA	100.PA	3.37 V	-3.33 V
DI1	-100.PA	100.PA	3.35 V	-3.31 V
DI2	-100.PA	100.PA	3.36 V	-3.33 V
DI3	-100.PA	100.PA	3.36 V	-3.29 V

	D00	D01	D02	D03
VOL1	90.0MV	95.0MV	95.0MV	95.0MV
VOL2	85.0MV	90.0MV	105.MV	100.MV
VOH1	4.89 V	4.89 V	4.89 V	4.89 V
VOH2	9.84 V	9.85 V	9.84 V	9.85 V
IDN1	8.30MA	7.95MA	7.60MA	7.65MA
IDN2	22.0MA	20.4MA	18.6MA	19.0MA
IDP1	-3.61MA	-3.62MA	-3.57MA	-3.65MA
IDP2	-7.97MA	-8.01MA	-7.75MA	-8.11MA
IOZ1	4.50NA	-100.PA	4.10NA	-800.PA
IOZ2	600.PA	3.20NA	400.PA	2.50NA
IOZ3	4.20NA	300.PA	2.90NA	1.20NA
IOZ4	6.00NA	-1.70NA	5.80NA	-1.60NA
IOZ5	-10.2UA	-10.2UA	-10.2UA	-10.2UA
IOZ6	2.20NA	1.70NA	1.00NA	2.70NA
IOZ7	2.60NA	1.90NA	800.PA	2.60NA
IOZ8	2.40NA	1.70NA	1.10NA	2.70NA
ILDP	160.UA			
IL1	-5.00UA			
IL2	-5.00UA			
IL3	-5.00UA			
IL4	-5.00UA			

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

FAILED DATA RETENTION TEST ADD = 16 DIAG = 0 PTN: 017

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	250.N	210.N	90.0N
DATA SETUP TIME	(TDS)	18.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	14.0N	14.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	6.00N	6.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	120.N	100.N	50.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	70.0N	62.0N	38.0N
CS1 SETUP TIME	(TCSS1)	0.00	0.00	62.0N
CS2 SETUP TIME	(TCSS2)	0.00	0.00	62.0N
CS1 HOLD TIME	(TCSH1)	0.00	0.00	14.0N
CS2 HOLD TIME	(TCSH2)	0.00	0.00	14.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	0.00	0.00	90.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	0.00	0.00	88.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	54.0N	48.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	300.N	300.N	24.0N
OUTPUT HOLD FROM CS2	(TDOH2)	300.N	300.N	22.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	34.0N
OUTPUT HOLD FROM MWR	(TDOH)	136.N	112.N	34.0N
READ CYCLE TIME	(TRC)	272.N	232.N	128.N
WRITE CYCLE TIME	(TWC)	208.N	184.N	120.N

	IIL	IIH	VIC1	VIC2
A0	-209.NA	51.5NA	3.05 V	-3.06 V
A1	-267.NA	50.9NA	3.12 V	-3.11 V
A2	-152.NA	41.1NA	3.12 V	-3.14 V
A3	-115.NA	36.5NA	3.13 V	-3.13 V
A4	-102.NA	35.0NA	3.15 V	-3.16 V
A5	-50.2NA	46.5NA	3.05 V	-3.12 V
A6	-41.1NA	42.8NA	3.08 V	-3.11 V
A7	-35.8NA	42.4NA	3.09 V	-3.12 V
CS1	-32.6NA	49.9NA	3.12 V	-3.12 V
CS2	-40.5NA	48.0NA	3.14 V	-3.14 V
MWR	-77.9NA	36.6NA	3.07 V	-3.07 V
MRD	-46.4NA	41.7NA	3.11 V	-3.10 V
DI0	-33.3NA	44.5NA	3.20 V	-3.16 V
DI1	-32.7NA	44.1NA	3.17 V	-3.14 V
DI2	-35.8NA	45.3NA	3.19 V	-3.16 V
DI3	-37.5NA	44.3NA	3.19 V	-3.13 V

	D00	D01	D02	D03
VOL1	125.MV	130.MV	135.MV	135.MV
VOL2	125.MV	140.MV	155.MV	150.MV
VOH1	4.82 V	4.82 V	4.82 V	4.82 V
VOH2	9.75 V	9.75 V	9.74 V	9.76 V
IDN1	5.95MA	5.65MA	5.35MA	5.45MA
IDN2	14.9MA	13.6MA	12.2MA	12.6MA
IDP1	-2.27MA	-2.24MA	-2.24MA	-2.29MA
IDP2	-4.98MA	-4.97MA	-4.85MA	-5.06MA
IOZ1	10.2UA	10.2UA	10.2UA	10.2UA
IOZ2	-74.0NA	-75.2NA	-78.3NA	-75.7NA
IOZ3	10.2UA	10.2UA	10.2UA	10.2UA
IOZ4	-74.7NA	-78.3NA	-78.2NA	-77.3NA
IOZ5	-10.2UA	-10.2UA	-10.2UA	-10.2UA
IOZ6	-54.8NA	-75.0NA	-65.8NA	-78.0NA
IOZ7	-44.3NA	-57.5NA	-50.7NA	-73.5NA
IOZ8	-65.6NA	-80.7NA	-73.0NA	-81.9NA

ILDP	260.UA
IL1	-35.0UA
IL2	-50.0UA
IL3	-35.0UA
IL4	-35.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

FAILED DATA RETENTION TEST ADD = 16 DIAG = 0 PIN: 017

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	260.N	220.N	100.N
DATA SETUP TIME	(TDS)	18.0N	16.0N	8.00N
DATA HOLD TIME	(TDH)	16.0N	16.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	4.00N	4.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	124.N	104.N	56.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-12.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	76.0N	68.0N	40.0N
CS1 SETUP TIME	(TCSS1)	0.00	0.00	70.0N
CS2 SETUP TIME	(TCSS2)	0.00	0.00	66.0N
CS1 HOLD TIME	(TCSH1)	0.00	0.00	14.0N
CS2 HOLD TIME	(TCSH2)	0.00	0.00	14.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	0.00	0.00	98.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	0.00	0.00	98.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	58.0N	50.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	300.N	300.N	28.0N
OUTPUT HOLD FROM CS2	(TDOH2)	300.N	300.N	26.0N
OUTPUT HOLD FROM MRD	(TDOH3)	138.N	116.N	36.0N
OUTPUT HOLD FROM MWR	(TPOH)	136.N	112.N	36.0N
READ CYCLE TIME	(TRC)	280.N	248.N	136.N
WRITE CYCLE TIME	(TWC)	224.N	200.N	128.N

	IIL	IIH	VIC1	VIC2
A0	-1.23UA	284.NA	3.04 V	-3.04 V
A1	-1.19UA	277.NA	3.10 V	-3.10 V
A2	-963.NA	230.NA	3.11 V	-3.13 V
A3	-741.NA	205.NA	3.12 V	-3.11 V
A4	-660.NA	201.NA	3.13 V	-3.14 V
A5	-288.NA	260.NA	3.03 V	-3.10 V
A6	-236.NA	241.NA	3.06 V	-3.09 V
A7	-205.NA	243.NA	3.07 V	-3.10 V
CS1	-184.NA	277.NA	3.10 V	-3.11 V
CS2	-240.NA	271.NA	3.13 V	-3.13 V
MWR	-440.NA	204.NA	3.05 V	-3.05 V
MRD	-265.NA	235.NA	3.09 V	-3.09 V
DI0	-190.NA	257.NA	3.18 V	-3.15 V
DI1	-190.NA	255.NA	3.15 V	-3.13 V
DI2	-206.NA	260.NA	3.18 V	-3.15 V
DI3	-211.NA	256.NA	3.17 V	-3.12 V

	D00	D01	D02	D03
VOL1	135.MV	145.MV	155.MV	150.MV
VOL2	145.MV	155.MV	175.MV	170.MV
VOH1	4.80 V	4.80 V	4.80 V	4.81 V
VOH2	9.72 V	9.72 V	9.71 V	9.72 V
IDN1	5.35MA	5.10MA	4.85MA	4.90MA
IDN2	13.3MA	12.2MA	10.9MA	11.3MA
IDP1	-2.05MA	-2.04MA	-2.00MA	-2.07MA
IDP2	-4.47MA	-4.47MA	-4.32MA	-4.56MA
IOZ1	10.2UA	10.2UA	10.2UA	10.2UA
IOZ2	-813.NA	-791.NA	-787.NA	-761.NA
IOZ3	10.2UA	10.2UA	10.2UA	10.2UA
IOZ4	-812.NA	-797.NA	-774.NA	-773.NA
IOZ5	-10.2UA	-10.2UA	-10.2UA	-10.2UA
IOZ6	-788.NA	-774.NA	-771.NA	-752.NA
IOZ7	-584.NA	-589.NA	-573.NA	-640.NA
IOZ8	-804.NA	-802.NA	-783.NA	-759.NA

ILDP	350.UA
IL1	-165.UA
IL2	-220.UA
IL3	-130.UA
IL4	-115.UA

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN: 33

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	200.N	175.N	80.0N
DATA SETUP TIME	(TDS)	24.0N	18.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	12.0N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	96.0N	84.0N	42.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	70.0N	62.0N	36.0N
CS1 SETUP TIME	(TCSS1)	150.N	130.N	68.0N
CS2 SETUP TIME	(TCSS2)	146.N	126.N	64.0N
CS1 HOLD TIME	(TCSH1)	46.0N	40.0N	24.0N
CS2 HOLD TIME	(TCSH2)	46.0N	40.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	196.N	172.N	88.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	194.N	168.N	86.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	46.0N	42.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	132.N	102.N	22.0N
OUTPUT HOLD FROM CS2	(TDOH2)	128.N	100.N	22.0N
OUTPUT HOLD FROM MRD	(TDOH3)	132.N	110.N	30.0N
OUTPUT HOLD FROM MWR	(TPOH)	124.N	106.N	30.0N
READ CYCLE TIME	(TRC)	216.N	192.N	120.N
WRITE CYCLE TIME	(TWC)	208.N	176.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-1.80NA	1.80NA	2.96 V	-2.93 V
A1	-1.60NA	2.60NA	2.97 V	-3.01 V
A2	-2.10NA	1.80NA	2.97 V	-3.00 V
A3	-3.00NA	1.80NA	2.98 V	-2.99 V
A4	-1.70NA	1.60NA	3.02 V	-3.05 V
A5	-1.50NA	1.90NA	2.94 V	-2.97 V
A6	-2.10NA	1.60NA	2.96 V	-2.98 V
A7	-2.00NA	1.90NA	2.97 V	-3.00 V
CS1	-2.10NA	1.50NA	3.01 V	-3.00 V
CS2	-1.90NA	1.70NA	3.01 V	-3.04 V
MWR	-2.10NA	2.00NA	2.96 V	-2.98 V
MRD	-1.60NA	1.80NA	3.00 V	-2.99 V
DI0	-2.00NA	1.70NA	3.09 V	-3.02 V
DI1	-1.90NA	1.60NA	3.05 V	-2.99 V
DI2	-4.30NA	1.90NA	3.09 V	-3.02 V
DI3	-1.90NA	1.70NA	3.07 V	-3.03 V

	D00	D01	D02	D03
VOL1	90.0MV	95.0MV	100.MV	100.MV
VOL2	100.MV	110.MV	125.MV	120.MV
VOH1	4.86 V	4.86 V	4.85 V	4.86 V
VOH2	9.80 V	9.80 V	9.78 V	9.80 V
IDN1	8.25MA	7.85MA	7.25MA	7.40MA
IDN2	19.2MA	17.4MA	15.3MA	15.8MA
IDP1	-2.74MA	-2.75MA	-2.65MA	-2.77MA
IDP2	-5.99MA	-6.02MA	-5.74MA	-6.08MA
IOZ1	16.9NA	19.9NA	15.7NA	20.2NA
IOZ2	19.7NA	16.9NA	18.6NA	17.0NA
IOZ3	15.7NA	19.9NA	16.7NA	17.7NA
IOZ4	14.2NA	22.3NA	14.1NA	21.2NA
IOZ5	21.3NA	15.5NA	20.7NA	16.0NA
IOZ6	21.3NA	15.8NA	20.5NA	15.8NA
IOZ7	21.3NA	15.5NA	20.0NA	15.8NA
IOZ8	20.8NA	16.1NA	19.9NA	16.0NA

ILDP	-5.00UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-5.00UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	195.N	170.N	70.0N
DATA SETUP TIME	(TDS)	24.0N	18.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	94.0N	80.0N	38.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	72.0N	62.0N	34.0N
CS1 SETUP TIME	(TCSS1)	144.N	124.N	62.0N
CS2 SETUP TIME	(TCSS2)	142.N	120.N	60.0N
CS1 HOLD TIME	(TCSH1)	40.0N	34.0N	22.0N
CS2 HOLD TIME	(TCSH2)	42.0N	36.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	190.N	160.N	84.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	186.N	158.N	82.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	42.0N	38.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	124.N	94.0N	18.0N
OUTPUT HOLD FROM CS2	(TDOH2)	122.N	94.0N	20.0N
OUTPUT HOLD FROM MRD	(TDOH3)	128.N	108.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	124.N	100.N	30.0N
READ CYCLE TIME	(TRC)	208.N	176.N	144.N
WRITE CYCLE TIME	(TWC)	224.N	184.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-200.PA	200.PA	3.01 V	-2.98 V
A1	-200.PA	600.PA	3.03 V	-3.06 V
A2	-300.PA	200.PA	3.02 V	-3.05 V
A3	-700.PA	200.PA	3.03 V	-3.04 V
A4	-300.PA	200.PA	3.07 V	-3.10 V
A5	-200.PA	300.PA	3.00 V	-3.02 V
A6	-300.PA	200.PA	3.01 V	-3.03 V
A7	-400.PA	300.PA	3.02 V	-3.05 V
CS1	-300.PA	200.PA	3.06 V	-3.05 V
CS2	-300.PA	200.PA	3.06 V	-3.10 V
MWR	-300.PA	300.PA	3.01 V	-3.03 V
MRD	-200.PA	300.PA	3.05 V	-3.04 V
DI0	-300.PA	300.PA	3.13 V	-3.08 V
DI1	-400.PA	200.PA	3.11 V	-3.04 V
DI2	-1.50NA	400.PA	3.13 V	-3.08 V
DI3	-300.PA	300.PA	3.12 V	-3.08 V

	D00	D01	D02	D03
VOL1	75.0MV	80.0MV	90.0MV	85.0MV
VOL2	85.0MV	95.0MV	105.MV	105.MV
VOH1	4.88 V	4.88 V	4.88 V	4.88 V
VOH2	9.82 V	9.83 V	9.82 V	9.82 V
IDN1	9.35MA	8.90MA	8.25MA	8.40MA
IDN2	22.0MA	20.0MA	17.7MA	18.3MA
IDP1	-3.22MA	-3.23MA	-3.14MA	-3.25MA
IDP2	-6.98MA	-7.05MA	-6.73MA	-7.09MA
IOZ1	2.60NA	4.90NA	2.90NA	3.00NA
IOZ2	300.PA	7.70NA	-100.PA	6.40NA
IOZ3	7.40NA	500.PA	6.20NA	800.PA
IOZ4	5.60NA	900.PA	5.90NA	-100.PA
IOZ5	500.PA	6.60NA	-200.PA	6.80NA
IOZ6	800.PA	6.80NA	-300.PA	6.60NA
IOZ7	500.PA	6.70NA	-300.PA	6.80NA
IOZ8	800.PA	6.70NA	-500.PA	6.70NA

ILDP	-10.0UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-5.00UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	195.N	160.N	65.0N
DATA SETUP TIME	(TDS)	30.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	14.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	90.0N	74.0N	34.0N
ADDRESS HOLD TIME	(TAH)	-14.0N	-12.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	70.0N	64.0N	32.0N
CS1 SETUP TIME	(TCSS1)	142.N	116.N	58.0N
CS2 SETUP TIME	(TCSS2)	152.N	128.N	62.0N
CS1 HOLD TIME	(TCSH1)	40.0N	36.0N	22.0N
CS2 HOLD TIME	(TCSH2)	28.0N	20.0N	12.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	186.N	154.N	80.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	196.N	164.N	86.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	38.0N	34.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	118.N	90.0N	18.0N
OUTPUT HOLD FROM CS2	(TDOH2)	140.N	110.N	20.0N
OUTPUT HOLD FROM MRD	(TDOH3)	126.N	106.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	122.N	102.N	28.0N
READ CYCLE TIME	(TRC)	200.N	176.N	104.N
WRITE CYCLE TIME	(TWC)	208.N	160.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	0.00 A	0.00 A	3.06 V	-3.04 V
A1	0.00 A	200.PA	3.09 V	-3.13 V
A2	-100.PA	100.PA	3.08 V	-3.12 V
A3	-200.PA	100.PA	3.10 V	-3.10 V
A4	-100.PA	0.00 A	3.13 V	-3.15 V
A5	0.00 A	100.PA	3.06 V	-3.09 V
A6	0.00 A	100.PA	3.08 V	-3.10 V
A7	-100.PA	100.PA	3.08 V	-3.12 V
CS1	-100.PA	0.00 A	3.13 V	-3.12 V
CS2	-100.PA	100.PA	3.13 V	-3.15 V
MWR	-100.PA	100.PA	3.08 V	-3.10 V
MRD	-100.PA	100.PA	3.12 V	-3.11 V
DI0	-100.PA	100.PA	3.18 V	-3.13 V
DI1	0.00 A	100.PA	3.16 V	-3.10 V
DI2	-600.PA	100.PA	3.19 V	-3.13 V
DI3	-100.PA	100.PA	3.18 V	-3.13 V

	DO0	DO1	DO2	DO3
VOL1	70.0MV	75.0MV	80.0MV	80.0MV
VOL2	75.0MV	85.0MV	95.0MV	90.0MV
VOH1	4.89 V	4.90 V	4.89 V	4.90 V
VOH2	9.85 V	9.85 V	9.84 V	9.85 V
IDN1	10.4MA	9.90MA	9.25MA	9.40MA
IDN2	24.8MA	22.7MA	20.2MA	20.8MA
IDP1	-3.73MA	-3.79MA	-3.67MA	-3.79MA
IDP2	-8.03MA	-8.23MA	-7.83MA	-8.20MA
IOZ1	-600.PA	5.30NA	-1.80NA	5.40NA
IOZ2	2.20NA	2.10NA	400.PA	2.80NA
IOZ3	2.10NA	700.PA	2.50NA	-100.PA
IOZ4	-1.20NA	4.70NA	-1.00NA	4.00NA
IOZ5	4.70NA	-700.PA	3.70NA	100.PA
IOZ6	5.20NA	-800.PA	3.60NA	-200.PA
IOZ7	5.10NA	-900.PA	4.10NA	-300.PA
IOZ8	5.60NA	-1.10NA	4.10NA	-500.PA

ILDP	-5.00UA
IL1	-5.00UA
IL2	-5.00UA
IL3	-5.00UA
IL4	-5.00UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	205.N	180.N	85.0N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	104.N	94.0N	48.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	80.0N	70.0N	42.0N
CS1 SETUP TIME	(TCSS1)	158.N	138.N	74.0N
CS2 SETUP TIME	(TCSS2)	154.N	134.N	70.0N
CS1 HOLD TIME	(TCSH1)	54.0N	46.0N	30.0N
CS2 HOLD TIME	(TCSH2)	56.0N	48.0N	28.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	208.N	184.N	98.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	204.N	180.N	96.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	44.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	136.N	106.N	24.0N
OUTPUT HOLD FROM CS2	(TDOH2)	132.N	104.N	26.0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	112.N	34.0N
OUTPUT HOLD FROM MWR	(TPOH)	128.N	108.N	34.0N
READ CYCLE TIME	(TRC)	224.N	200.N	128.N
WRITE CYCLE TIME	(TWC)	216.N	184.N	120.N

	IIL	IIH	VIC1	VIC2
A0	-26.0NA	25.4NA	2.94 V	-2.91 V
A1	-25.2NA	27.3NA	2.96 V	-3.00 V
A2	-26.2NA	25.5NA	2.96 V	-2.99 V
A3	-28.3NA	24.9NA	2.97 V	-2.98 V
A4	-24.1NA	24.0NA	3.00 V	-3.04 V
A5	-24.6NA	25.8NA	2.93 V	-2.95 V
A6	-26.4NA	25.3NA	2.95 V	-2.96 V
A7	-26.3NA	25.6NA	2.96 V	-2.99 V
CS1	-25.9NA	23.1NA	2.99 V	-2.99 V
CS2	-24.1NA	24.3NA	2.99 V	-3.03 V
MWR	-24.6NA	24.5NA	2.94 V	-2.96 V
MRD	-23.3NA	24.1NA	2.98 V	-2.98 V
DI0	-24.6NA	24.6NA	3.08 V	-3.01 V
DI1	-24.0NA	24.1NA	3.04 V	-2.97 V
DI2	-28.0NA	24.8NA	3.07 V	-3.01 V
DI3	-23.8NA	24.1NA	3.05 V	-3.01 V

	D00	D01	D02	D03
VOL1	105.MV	110.MV	120.MV	115.MV
VOL2	115.MV	130.MV	150.MV	145.MV
VOH1	4.83 V	4.83 V	4.82 V	4.83 V
VOH2	9.76 V	9.76 V	9.74 V	9.76 V
IDN1	7.10MA	6.70MA	6.20MA	6.35MA
IDN2	16.3MA	14.8MA	13.0MA	13.5MA
IDP1	-2.31MA	-2.31MA	-2.22MA	-2.34MA
IDP2	-5.05MA	-5.08MA	-4.82MA	-5.16MA
IOZ1	151.NA	158.NA	151.NA	147.NA
IOZ2	155.NA	150.NA	156.NA	147.NA
IOZ3	151.NA	153.NA	153.NA	146.NA
IOZ4	158.NA	147.NA	154.NA	150.NA
IOZ5	156.NA	152.NA	159.NA	152.NA
IOZ6	160.NA	156.NA	147.NA	160.NA
IOZ7	150.NA	159.NA	150.NA	148.NA
IOZ8	159.NA	150.NA	154.NA	153.NA

ILDP	-5.00UA
IL1	-20.0UA
IL2	-20.0UA
IL3	-20.0UA
IL4	-20.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=9V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	220.N	195.N	95.0N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	14.0N	14.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	6.00N	6.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	114.N	104.N	56.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-16.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	84.0N	76.0N	44.0N
CS1 SETUP TIME	(TCSS1)	166.N	146.N	80.0N
CS2 SETUP TIME	(TCSS2)	162.N	142.N	78.0N
CS1 HOLD TIME	(TCSH1)	54.0N	48.0N	30.0N
CS2 HOLD TIME	(TCSH2)	56.0N	50.0N	30.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	224.N	200.N	106.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	220.N	196.N	106.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	54.0N	50.0N	30.0N
OUTPUT HOLD FROM CS1	(TDOH1)	140.N	110.N	28.0N
OUTPUT HOLD FROM CS2	(TDOH2)	138.N	108.N	30.0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	114.N	36.0N
OUTPUT HOLD FROM MWR	(TPDH)	130.N	110.N	38.0N
READ CYCLE TIME	(TRC)	240.N	216.N	128.N
WRITE CYCLE TIME	(TWC)	224.N	200.N	128.N

	IIL	IIH	VIC1	VIC2
A0	-157.NA	150.NA	2.95 V	-2.91 V
A1	-154.NA	153.NA	2.97 V	-3.00 V
A2	-154.NA	148.NA	2.96 V	-3.00 V
A3	-157.NA	147.NA	2.98 V	-2.99 V
A4	-145.NA	141.NA	3.01 V	-3.05 V
A5	-151.NA	148.NA	2.94 V	-2.95 V
A6	-155.NA	148.NA	2.95 V	-2.97 V
A7	-157.NA	149.NA	2.97 V	-3.00 V
CS1	-152.NA	137.NA	3.00 V	-2.99 V
CS2	-142.NA	141.NA	3.00 V	-3.04 V
MWR	-143.NA	140.NA	2.95 V	-2.97 V
MRD	-143.NA	138.NA	2.99 V	-2.99 V
DI0	-146.NA	144.NA	3.09 V	-3.02 V
DI1	-144.NA	143.NA	3.05 V	-2.98 V
DI2	-146.NA	141.NA	3.08 V	-3.02 V
DI3	-142.NA	138.NA	3.06 V	-3.02 V

	D00	D01	D02	D03
VOL1	115.MV	125.MV	135.MV	130.MV
VOL2	130.MV	145.MV	170.MV	160.MV
VOH1	4.81 V	4.81 V	4.80 V	4.81 V
VOH2	9.72 V	9.72 V	9.71 V	9.72 V
IDN1	6.30MA	5.95MA	5.55MA	5.65MA
IDN2	14.4MA	13.1MA	11.5MA	11.9MA
IDP1	-2.07MA	-2.07MA	-2.02MA	-2.10MA
IDP2	-4.52MA	-4.55MA	-4.34MA	-4.61MA
IOZ1	643.NA	621.NA	612.NA	605.NA
IOZ2	643.NA	614.NA	606.NA	607.NA
IOZ3	637.NA	611.NA	609.NA	606.NA
IOZ4	642.NA	612.NA	600.NA	611.NA
IOZ5	649.NA	621.NA	621.NA	624.NA
IOZ6	643.NA	627.NA	603.NA	617.NA
IOZ7	635.NA	621.NA	609.NA	606.NA
IOZ8	645.NA	616.NA	608.NA	615.NA
ILOP	40.0UA			
IL1	-90.0UA			
IL2	-105.UA			
IL3	-85.0UA			
IL4	-70.0UA			

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 31 AUG 78 TEMP: 25 C SN: 34

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	270.N	220.N	85.0N
DATA SETUP TIME	(TDS)	24.0N	18.0N	8.00N
DATA HOLD TIME	(TDH)	10.0N	10.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	14.0N	12.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	134.N	110.N	48.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	72.0N	62.0N	38.0N
CS1 SETUP TIME	(TCSS1)	164.N	140.N	70.0N
CS2 SETUP TIME	(TCSS2)	160.N	138.N	68.0N
CS1 HOLD TIME	(TCSH1)	40.0N	36.0N	24.0N
CS2 HOLD TIME	(TCSH2)	42.0N	38.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	272.N	224.N	96.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	270.N	222.N	94.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	50.0N	44.0N	26.0N
OUTPUT HOLD FROM CS1	(TDOH1)	140.N	108.N	28.0N
OUTPUT HOLD FROM CS2	(TDOH2)	136.N	106.N	28.0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	112.N	34.0N
OUTPUT HOLD FROM MWR	(TPDH)	130.N	108.N	32.0N
READ CYCLE TIME	(TRC)	248.N	216.N	120.N
WRITE CYCLE TIME	(TWC)	256.N	184.N	112.N

	IIL	IIH	VIC1	VIC2
A0	-1.80NA	1.40NA	2.92 V	-2.91 V
A1	-1.90NA	1.90NA	2.98 V	-2.99 V
A2	-1.50NA	1.50NA	2.98 V	-3.00 V
A3	-1.30NA	1.90NA	2.98 V	-3.00 V
A4	-1.70NA	1.60NA	2.99 V	-3.00 V
A5	-1.80NA	1.70NA	2.94 V	-2.98 V
A6	-1.40NA	1.30NA	2.94 V	-2.98 V
A7	-2.10NA	1.60NA	2.95 V	-2.99 V
CS1	-1.30NA	1.50NA	2.98 V	-2.97 V
CS2	-1.50NA	1.50NA	3.02 V	-2.99 V
MWR	-1.60NA	1.40NA	2.96 V	-2.96 V
MRD	-1.60NA	1.80NA	2.97 V	-2.97 V
DI0	-2.10NA	1.80NA	3.02 V	-2.99 V
DI1	-2.00NA	2.20NA	3.03 V	-2.97 V
DI2	-1.80NA	1.90NA	3.03 V	-3.01 V
DI3	-1.40NA	1.80NA	3.01 V	-2.97 V

	DO0	DO1	DO2	DO3
VOL1	105.MV	110.MV	115.MV	115.MV
VOL2	110.MV	120.MV	135.MV	130.MV
VOH1	4.84 V	4.84 V	4.84 V	4.85 V
VOH2	9.78 V	9.78 V	9.77 V	9.78 V
IDN1	7.05MA	6.70MA	6.30MA	6.45MA
IUN2	17.3MA	15.8MA	14.1MA	14.6MA
IDP1	-2.51MA	-2.54MA	-2.48MA	-2.55MA
IDP2	-5.59MA	-5.62MA	-5.43MA	-5.68MA
IOZ1	28.9NA	20.8NA	26.0NA	19.7NA
IOZ2	26.0NA	21.8NA	24.1NA	20.5NA
IOZ3	22.9NA	25.2NA	20.0NA	25.3NA
IOZ4	26.5NA	21.9NA	23.2NA	21.7NA
IOZ5	23.0NA	25.1NA	21.9NA	23.0NA
IOZ6	23.6NA	24.5NA	21.5NA	23.4NA
IOZ7	22.8NA	24.9NA	21.5NA	22.7NA
IOZ8	22.7NA	24.3NA	21.0NA	23.1NA

ILDP	-10.0UA
IL1	-30.0UA
IL2	-35.0UA
IL3	-85.0UA
IL4	-80.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	290.N	220.N	80.0N
DATA SETUP TIME	(TDS)	26.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	10.0N	12.0N
ADDRESS SETUP TIME	(TAS1)	18.0N	14.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	132.N	106.N	42.0N
ADDRESS HOLD TIME	(TAH)	-16.0N	-14.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	76.0N	66.0N	36.0N
CS1 SETUP TIME	(TCSS1)	156.N	132.N	64.0N
CS2 SETUP TIME	(TCSS2)	154.N	130.N	62.0N
CS1 HOLD TIME	(TCSH1)	40.0N	34.0N	22.0N
CS2 HOLD TIME	(TCSH2)	42.0N	36.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	278.N	222.N	88.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	276.N	220.N	86.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	46.0N	40.0N	24.0N
OUTPUT HOLD FROM CS1	(TDOH1)	132.N	102.N	24.0N
OUTPUT HOLD FROM CS2	(TDOH2)	130.N	98.0N	24.0N
OUTPUT HOLD FROM MRD	(TDOH3)	132.N	110.N	30.0N
OUTPUT HOLD FROM MWR	(TPDH)	126.N	106.N	30.0N
READ CYCLE TIME	(TRC)	232.N	208.N	112.N
WRITE CYCLE TIME	(TWC)	240.N	176.N	104.N

	IIL	IIH	VIC1	VIC2
A0	-400.PA	200.PA	3.03 V	-3.02 V
A1	-500.PA	500.PA	3.09 V	-3.10 V
A2	-300.PA	300.PA	3.09 V	-3.11 V
A3	-200.PA	300.PA	3.09 V	-3.11 V
A4	-300.PA	300.PA	3.11 V	-3.11 V
A5	-400.PA	300.PA	3.05 V	-3.10 V
A6	-200.PA	200.PA	3.05 V	-3.09 V
A7	-500.PA	300.PA	3.06 V	-3.11 V
CS1	-200.PA	300.PA	3.10 V	-3.09 V
CS2	-300.PA	300.PA	3.13 V	-3.10 V
MWR	-300.PA	200.PA	3.07 V	-3.07 V
MRD	-300.PA	400.PA	3.08 V	-3.08 V
DI0	-400.PA	200.PA	3.13 V	-3.09 V
DI1	-400.PA	500.PA	3.14 V	-3.08 V
DI2	-300.PA	400.PA	3.14 V	-3.11 V
DI3	-200.PA	300.PA	3.13 V	-3.08 V

	D00	D01	D02	D03
VOL1	90.0MV	95.0MV	100.MV	100.MV
VOL2	95.0MV	105.MV	115.MV	110.MV
VOH1	4.88 V	4.87 V	4.86 V	4.88 V
VOH2	9.81 V	9.81 V	9.81 V	9.82 V
IDN1	7.95MA	7.60MA	7.20MA	7.30MA
IDN2	19.9MA	18.3MA	16.4MA	17.0MA
IDP1	-2.99MA	-3.01MA	-2.94MA	-3.04MA
IDP2	-6.58MA	-6.62MA	-6.41MA	-6.73MA
IOZ1	3.10NA	6.50NA	1.00NA	6.60NA
IOZ2	6.00NA	3.00NA	4.20NA	3.30NA
IOZ3	3.50NA	4.80NA	3.30NA	3.00NA
IOZ4	1.30NA	7.90NA	400.PA	6.70NA
IOZ5	8.50NA	1.00NA	6.50NA	1.30NA
IOZ6	8.20NA	1.00NA	6.90NA	1.00NA
IOZ7	8.50NA	900.PA	6.70NA	900.PA
IOZ8	8.30NA	1.00NA	7.00NA	900.PA

ILOP	-10.0UA
IL1	-25.0UA
IL2	-30.0UA
IL3	-70.0UA
IL4	-70.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	300.N	220.N	75.0N
DATA SETUP TIME	(TDS)	30.0N	22.0N	8.00N
DATA HOLD TIME	(TDH)	8.00N	8.00N	10.0N
ADDRESS SETUP TIME	(TAS1)	16.0N	10.0N	4.00N
ADDRESS SETUP TIME	(TAS2)	132.N	104.N	38.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-14.0N	-2.00N
WRITE PULSE WIDTH	(TWP)	80.0N	66.0N	32.0N
CS1 SETUP TIME	(TCSS1)	154.N	128.N	60.0N
CS2 SETUP TIME	(TCSS2)	152.N	126.N	58.0N
CS1 HOLD TIME	(TCSH1)	46.0N	38.0N	22.0N
CS2 HOLD TIME	(TCSH2)	46.0N	40.0N	22.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	294.N	224.N	84.0N
OUTPUT ACTIVE FROM CS2	(TDOA2)	292.N	222.N	82.0N
OUTPUT ACTIVE FROM MRD	(TDOA3)	42.0N	38.0N	22.0N
OUTPUT HOLD FROM CS1	(TDOH1)	126.N	94.0N	20.0N
OUTPUT HOLD FROM CS2	(TDOH2)	124.N	92.0N	20.0N
OUTPUT HOLD FROM MRD	(TDOH3)	130.N	108.N	28.0N
OUTPUT HOLD FROM MWR	(TPDH)	126.N	104.N	28.0N
READ CYCLE TIME	(TRC)	216.N	184.N	136.N
WRITE CYCLE TIME	(TWC)	200.N	168.N	96.0N

	IIL	IIH	VIC1	VIC2
A0	-100.PA	100.PA	3.13 V	-3.12 V
A1	-100.PA	100.PA	3.18 V	-3.19 V
A2	-100.PA	100.PA	3.18 V	-3.19 V
A3	0.00 A	100.PA	3.18 V	-3.20 V
A4	-100.PA	100.PA	3.19 V	-3.19 V
A5	-100.PA	100.PA	3.14 V	-3.19 V
A6	-100.PA	100.PA	3.15 V	-3.18 V
A7	-100.PA	100.PA	3.15 V	-3.19 V
CS1	0.00 A	100.PA	3.19 V	-3.18 V
CS2	0.00 A	100.PA	3.22 V	-3.18 V
MWR	-100.PA	0.00 A	3.16 V	-3.16 V
MRD	-100.PA	100.PA	3.17 V	-3.17 V
DI0	-100.PA	100.PA	3.23 V	-3.18 V
DI1	-100.PA	200.PA	3.23 V	-3.17 V
DI2	-100.PA	100.PA	3.24 V	-3.20 V
DI3	-100.PA	300.PA	3.22 V	-3.17 V

	D00	D01	D02	D03
VOL1	85.0MV	85.0MV	95.0MV	90.0MV
VOL2	85.0MV	90.0MV	100.MV	100.MV
VOH1	4.89 V	4.89 V	4.88 V	4.89 V
VOH2	9.84 V	9.84 V	9.84 V	9.84 V
IDN1	8.80MA	8.40MA	7.95MA	8.10MA
IDN2	22.2MA	20.5MA	18.5MA	19.0MA
IDP1	-3.44MA	-3.49MA	-3.42MA	-3.54MA
IDP2	-7.57MA	-7.67MA	-7.43MA	-7.79MA
IOZ1	-600.PA	5.80NA	-1.40NA	10.0NA
IOZ2	900.PA	3.40NA	-500.PA	8.50NA
IOZ3	3.60NA	-100.PA	3.80NA	3.40NA
IOZ4	200.PA	3.50NA	400.PA	6.60NA
IOZ5	3.70NA	800.PA	1.70NA	6.20NA
IOZ6	3.40NA	700.PA	2.10NA	6.40NA
IOZ7	3.70NA	800.PA	1.70NA	6.40NA
IOZ8	3.30NA	700.PA	2.10NA	6.60NA

ILDP	-2.80UA
IL1	-25.0UA
IL2	-30.0UA
IL3	-65.0UA
IL4	-65.0UA

PASSED GALPAT (WIDE LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=10V
PASSED GALPAT (TIGHT LIMITS) VCC=5V

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

PASSED DATA RETENTION TEST

		VCC = 4.5V	5.0V	10.0V
ADDRESS ACCESS TIME	(TAA)	270.N	225.N	95.0N
DATA SETUP TIME	(TDS)	24.0N	20.0N	8.00N
DATA HOLD TIME	(TDH)	12.0N	12.0N	14.0N
ADDRESS SETUP TIME	(TAS1)	8.00N	8.00N	4.00N
ADDRESS SETUP TIME	(TAS2)	132.N	110.N	54.0N
ADDRESS HOLD TIME	(TAH)	-18.0N	-16.0N	-4.00N
WRITE PULSE WIDTH	(TWP)	84.0N	72.0N	42.0N
CS1 SETUP TIME	(TCSS1)	170.N	148.N	76.0N
CS2 SETUP TIME	(TCSS2)	166.N	144.N	74.0N
CS1 HOLD TIME	(TCSH1)	54.0N	46.0N	30.0N
CS2 HOLD TIME	(TCSH2)	56.0N	50.0N	30.0N
OUTPUT ACTIVE FROM CS1	(TDOA1)	274.N	232.N	106.N
OUTPUT ACTIVE FROM CS2	(TDOA2)	270.N	230.N	104.N
OUTPUT ACTIVE FROM MRD	(TDOA3)	54.0N	48.0N	28.0N
OUTPUT HOLD FROM CS1	(TDOH1)	146.N	114.N	32.0N
OUTPUT HOLD FROM CS2	(TDOH2)	142.N	112.N	32.0N
OUTPUT HOLD FROM MRD	(TDOH3)	134.N	114.N	34.0N
OUTPUT HOLD FROM MWR	(TPDH)	132.N	110.N	36.0N
READ CYCLE TIME	(TRC)	256.N	224.N	128.N
WRITE CYCLE TIME	(TWC)	232.N	200.N	128.N

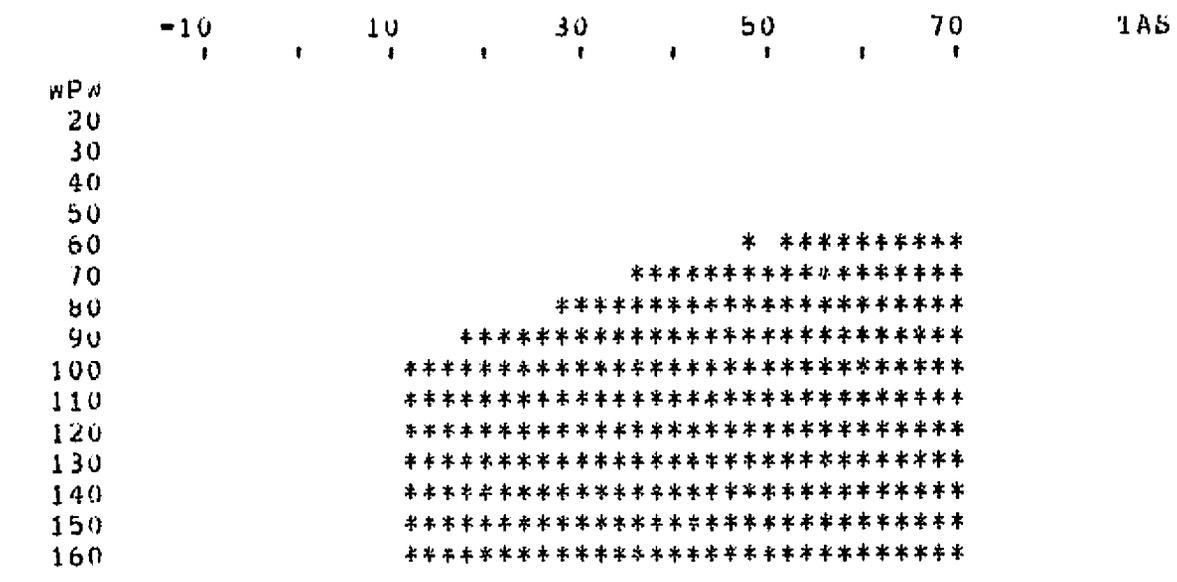
	IIL	IIH	VIC1	VTC2
A0	-17.7NA	18.8NA	2.87 V	-2.86 V
A1	-18.2NA	20.3NA	2.93 V	-2.94 V
A2	-17.9NA	17.9NA	2.93 V	-2.94 V
A3	-16.9NA	19.2NA	2.93 V	-2.95 V
A4	-17.6NA	17.9NA	2.94 V	-2.95 V
A5	-18.0NA	19.7NA	2.89 V	-2.93 V
A6	-29.2NA	191.NA	2.89 V	-2.92 V
A7	-18.5NA	19.8NA	2.89 V	-2.94 V
CS1	-17.5NA	18.7NA	2.93 V	-2.92 V
CS2	-17.3NA	18.4NA	2.96 V	-2.94 V
MWR	-17.1NA	17.2NA	2.91 V	-2.91 V
MRD	-17.3NA	19.2NA	2.92 V	-2.92 V
DI0	-19.9NA	21.5NA	2.97 V	-2.93 V
DI1	-19.6NA	21.9NA	2.98 V	-2.93 V
DI2	-17.8NA	20.0NA	2.98 V	-2.95 V
DI3	-17.4NA	19.7NA	2.96 V	-2.92 V

	DO0	DO1	DO2	DO3
VOL1	120.MV	130.MV	135.MV	135.MV
VOL2	130.MV	145.MV	160.MV	155.MV
VOH1	4.82 V	4.82 V	4.81 V	4.82 V
VOH2	9.73 V	9.73 V	9.72 V	9.74 V
IDN1	6.05MA	5.75MA	5.40MA	5.50MA
IDN2	14.6MA	13.4MA	11.9MA	12.4MA
IDP1	-2.13MA	-2.14MA	-2.09MA	-2.17MA
IDP2	-4.74MA	-4.75MA	-4.60MA	-4.83MA
IOZ1	232.NA	238.NA	220.NA	228.NA
IOZ2	225.NA	233.NA	223.NA	220.NA
IOZ3	223.NA	237.NA	220.NA	223.NA
IOZ4	225.NA	229.NA	225.NA	218.NA
IOZ5	226.NA	235.NA	227.NA	227.NA
IOZ6	236.NA	228.NA	228.NA	228.NA
IOZ7	228.NA	238.NA	219.NA	229.NA
IOZ8	227.NA	229.NA	230.NA	221.NA
ILDP	4.80UA			
IL1	-40.0UA			
IL2	-50.0UA			
IL3	-105.UA			
IL4	-100.UA			

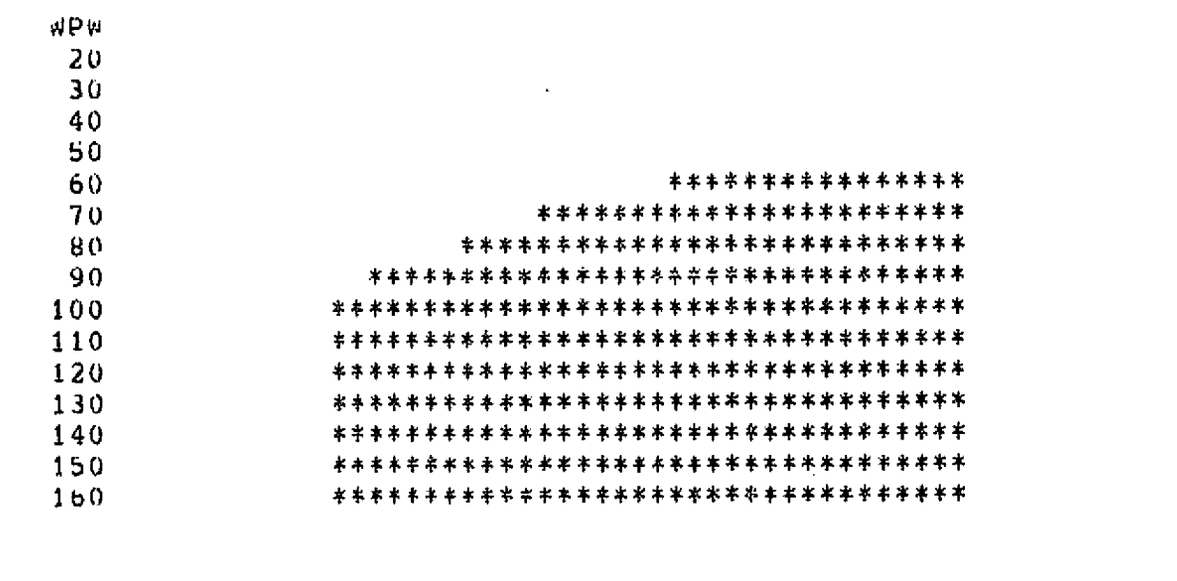
APPENDIX C
SCHMOO PLOTS

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 25 C SN: 2

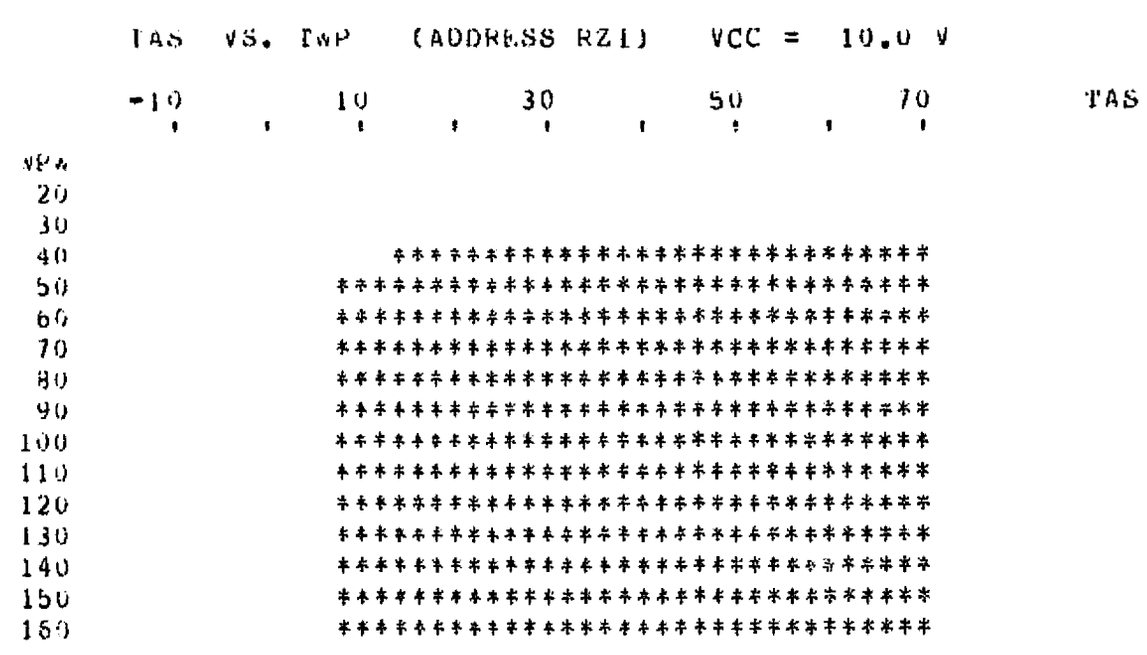
TAS VS. TWP (ADDRESS RZ1) VCC = 5.00 V

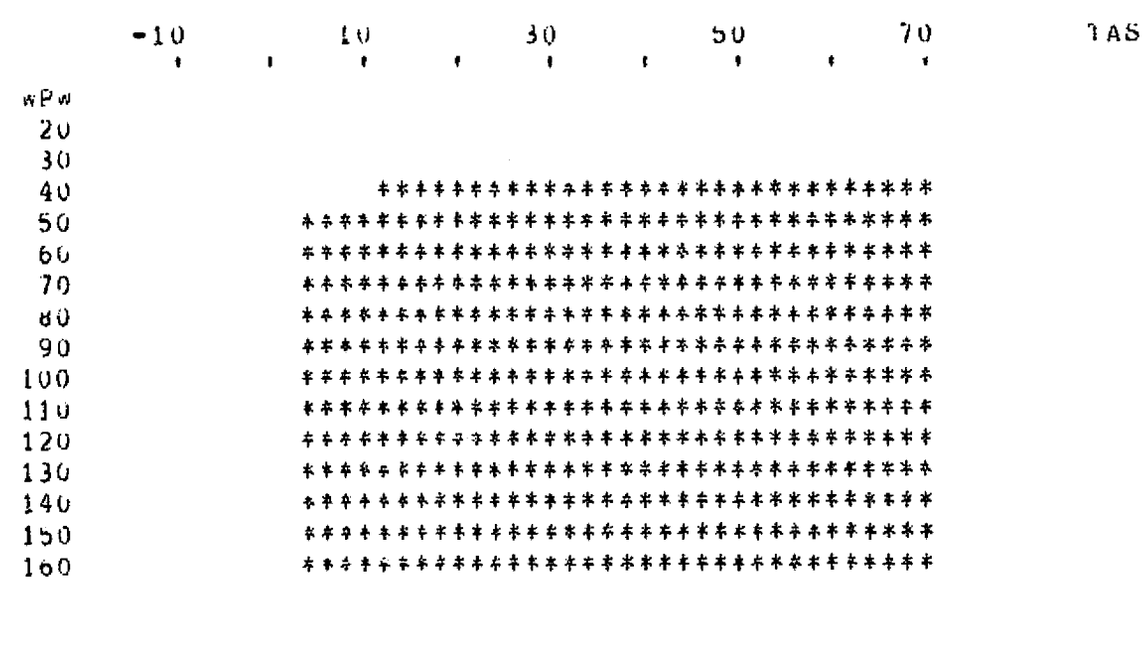


TAS VS. TWP (ADDRESS RZ) VCC = 5.00 V



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TAS VS. TWP (ADDRESS RZ1) VCC = 10.0 V
-10
10
30
50
70
TAS
TWP
20
30
40
50
60
70
80
90
100
110
120
130
140
150
160


TAS VS. TWP (ADDRESS RZ) VCC = 10.0 V
-10
10
30
50
70
TAS
TWP
20
30
40
50
60
70
80
90
100
110
120
130
140
150
160

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 25 C SN: 2

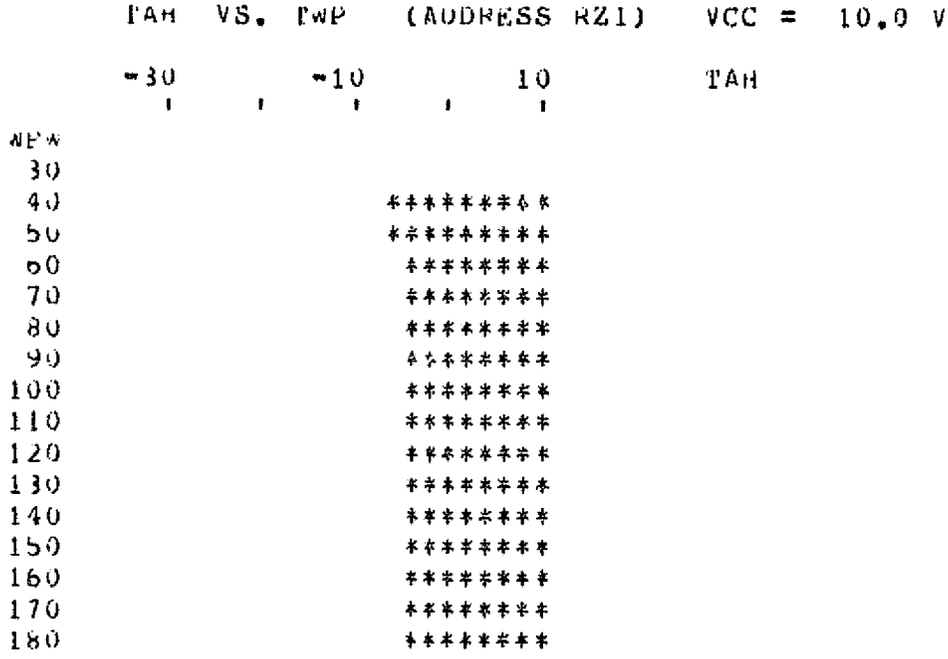
TAH VS. TWP (ADDRESS RZ1) VCC = 5.00 V

```
        -30        -10         10          TAH
          '     '     '     '     '
WPW
 30
 40
 50
 60              ***********
 70             ************
 80             ************
 90             ************
100             ************
110             ************
120             ************
130             ************
140             ************
150             ************
160             ************
170             ************
180             ************
```

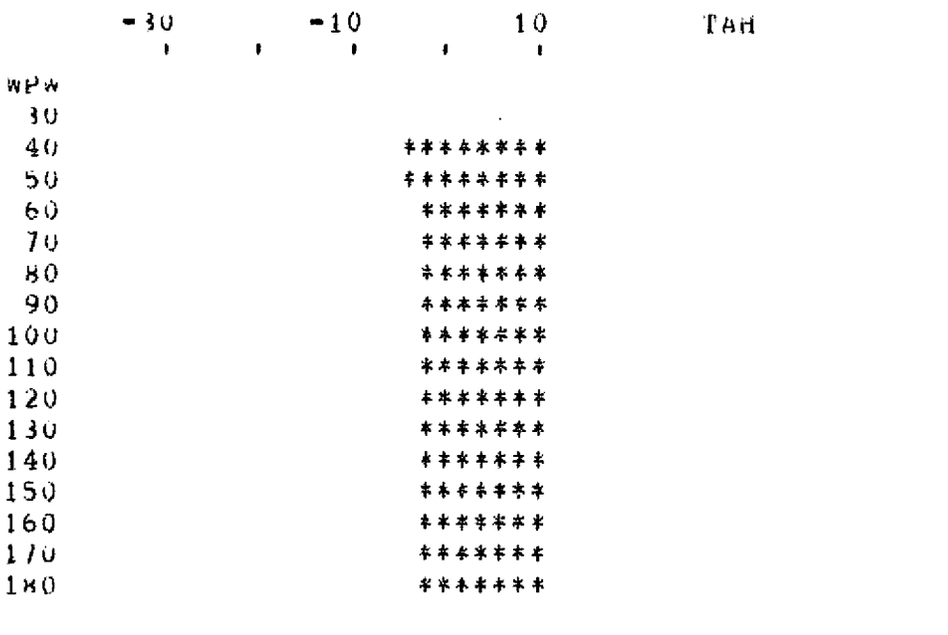
TAH VS. TWP (ADDRESS RZ) VCC = 5.00 V

```
        -30        -10         10          TAH
          '     '     '     '     '
WPW
 30
 40
 50
 60             ***********
 70             ***********
 80              **********
 90              **********
100              **********
110              **********
120              **********
130              **********
140              **********
150              **********
160              **********
170              **********
180              **********
```

TAH VS. TWP (ADDRESS RZ1) VCC = 10.0 V



TAH VS. TWP (ADDRESS RZ) VCC = 10.0 V



RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 25 C SN: 2

TDS VS. TWP (DATA RZ) VCC = 5.00 V

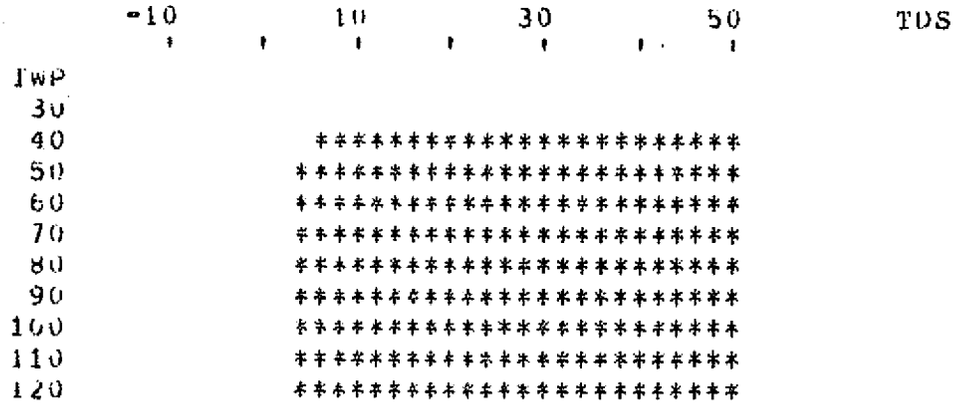
```
       -10        10        30        50        TDS
        '    '    '    '    '    '    '
TWP
 30
 40
 50
 60          ************************
 70          ************************
 80          ************************
 90          ************************
100          ************************
110          ************************
120          ************************
```

TDS VS. TWP (DATA RZ) VCC = 5.00 V

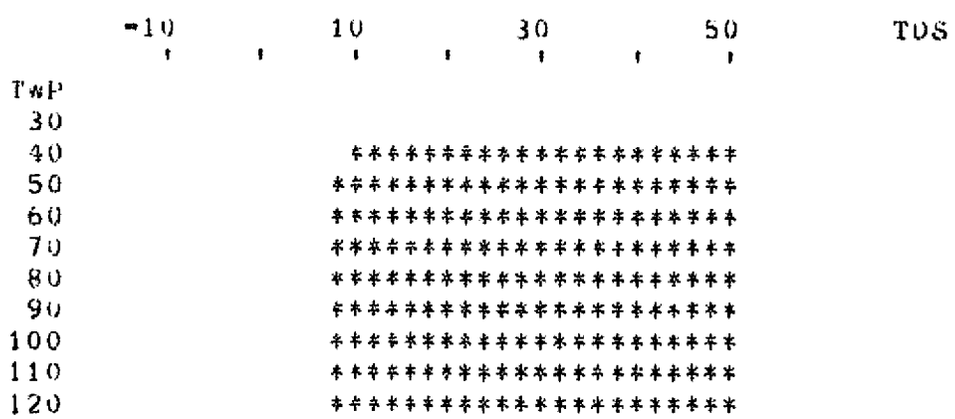
```
       -10        10        30        50        TDS
        '    '    '    '    '    '    '
TWP
 30
 40
 50
 60               ******************
 70               ******************
 80               ******************
 90               ******************
100               ******************
110               ******************
120               ******************
```

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ORIGINAL PAGE IS POOR

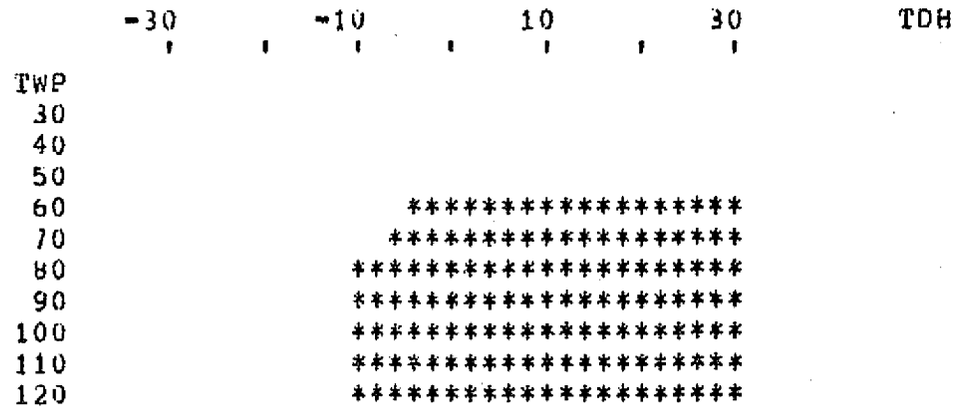
TDS VS. TwP (DATA RZ1) VCC = 10.0 V



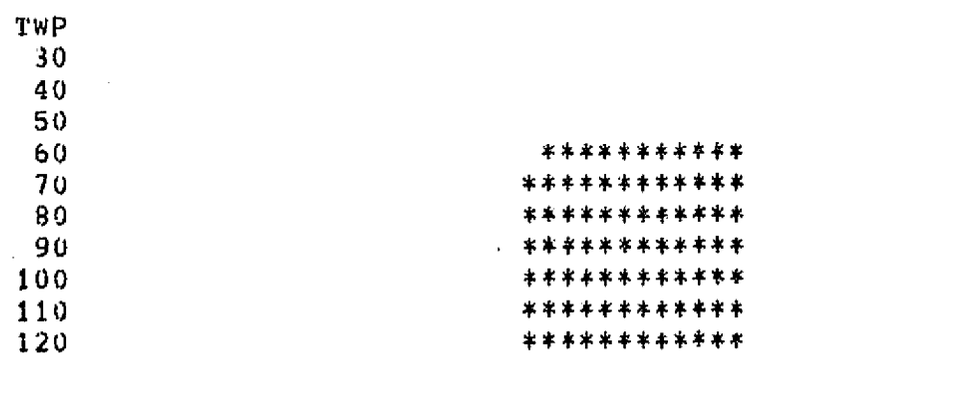
TDS VS. TwP (DATA RZ) VCC = 10.0 V



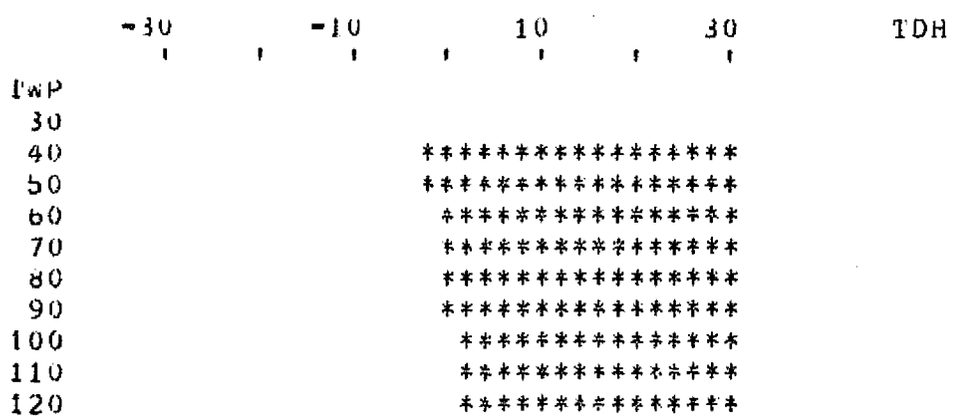
TDH VS. TWP (DATA RZI) VCC = 5.00 V



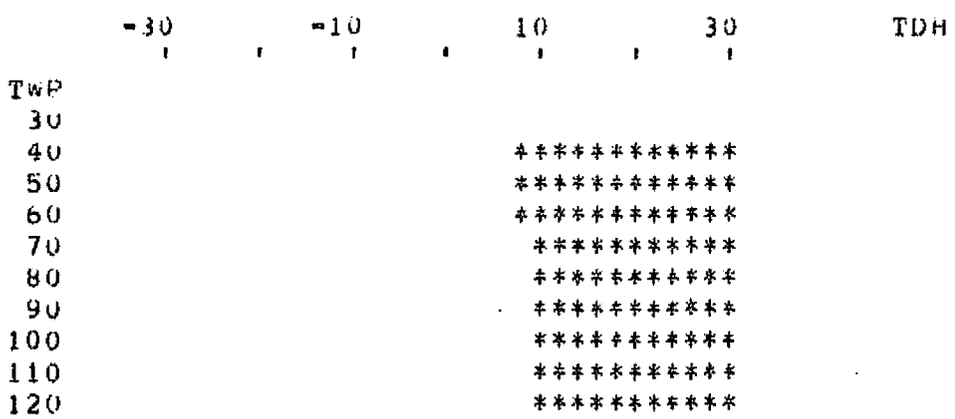
TDH VS. TWP (DATA RZ) VCC = 5.00 V



TDH VS. TWP (DATA RZ1) VCC = 10.0 V

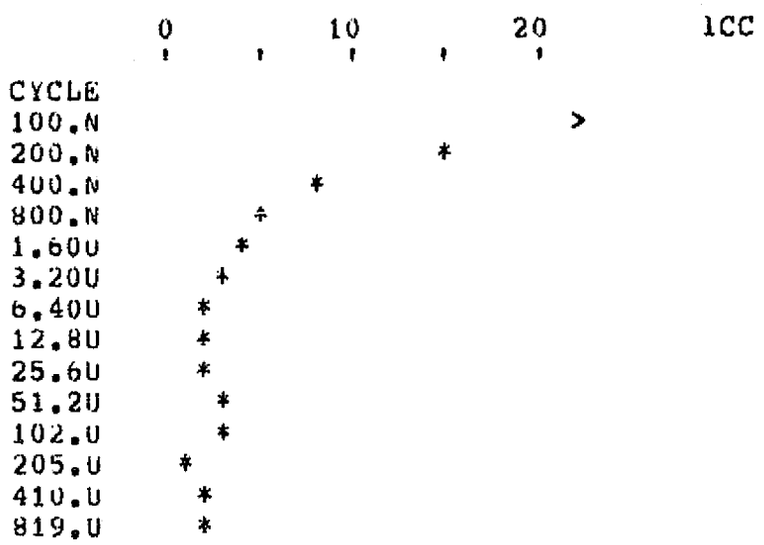


TDH VS. TWP (DATA RZ) VCC = 10.0 V



RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 25 C SN: 2

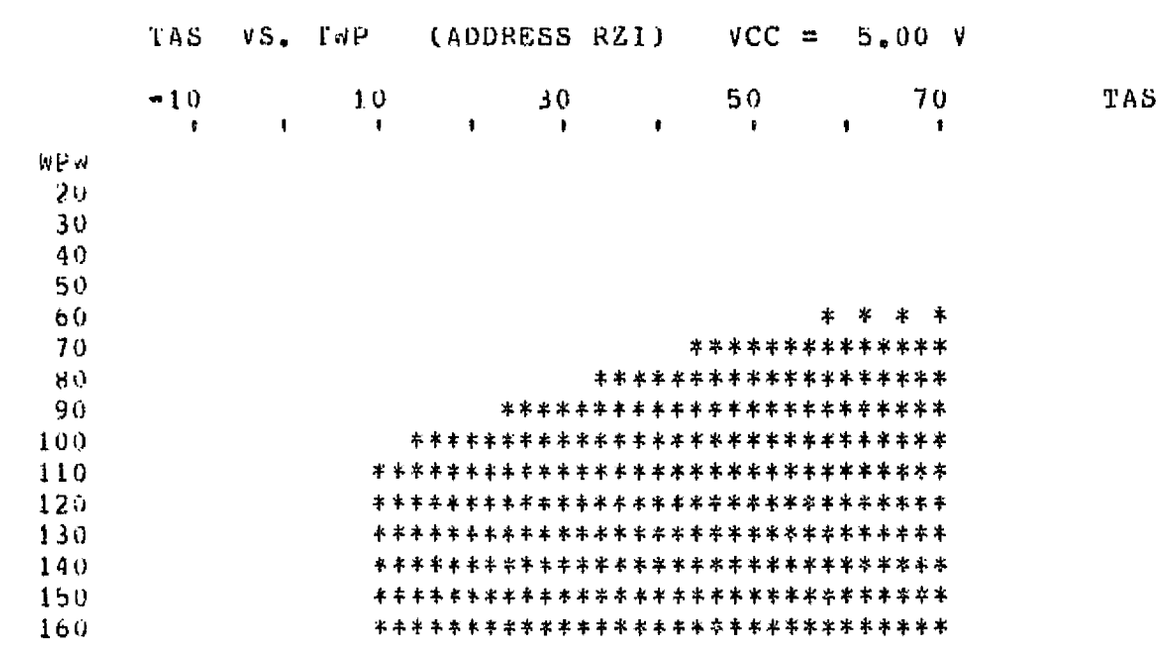
ICC VS. CYCLE TIME VCC = 10.0V

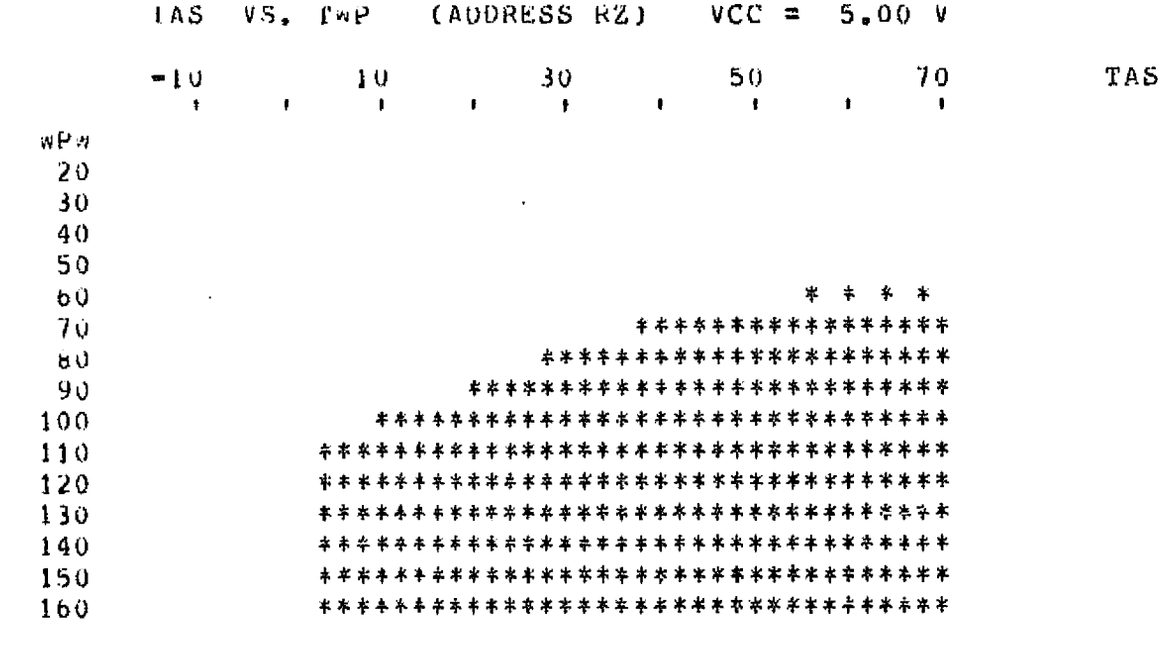


DEVICE PASSED ALL TESTS

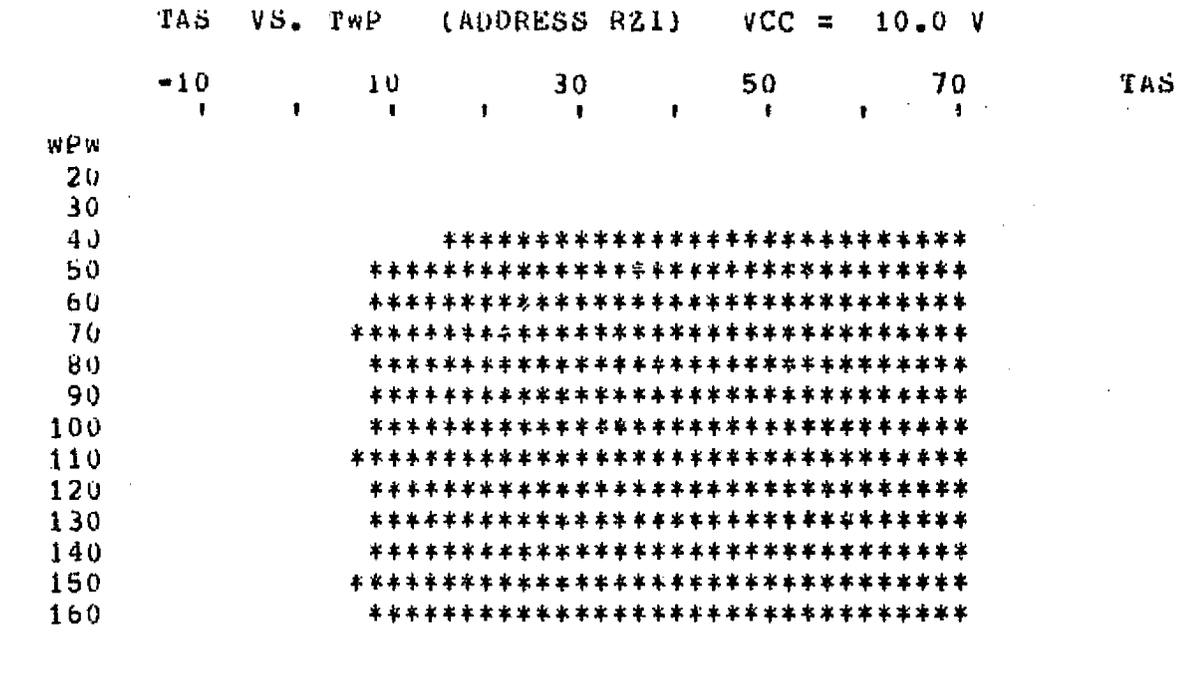
REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

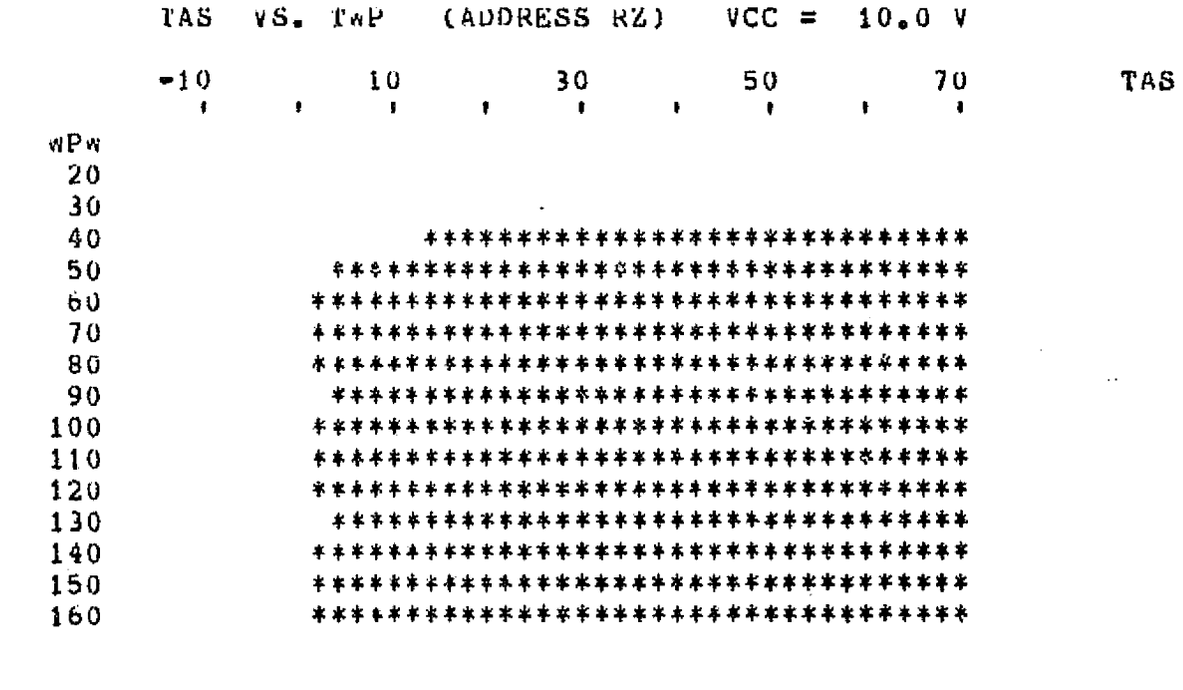
RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 25 C SN: 2



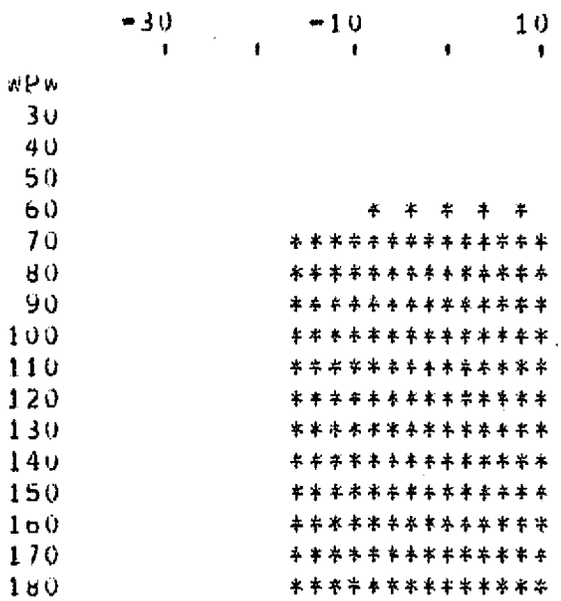


RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 25 C SN: 2

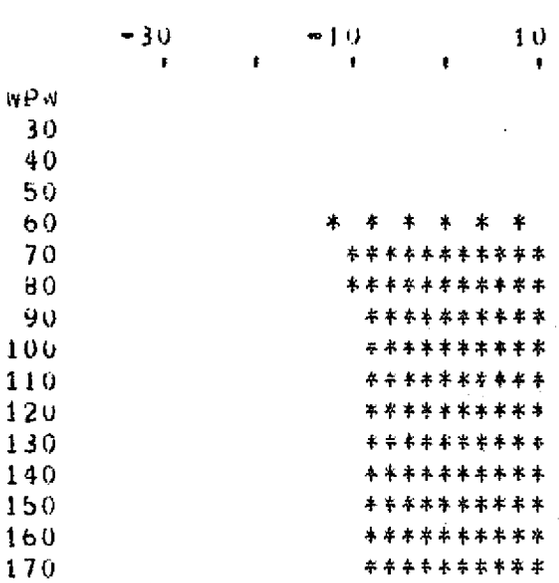




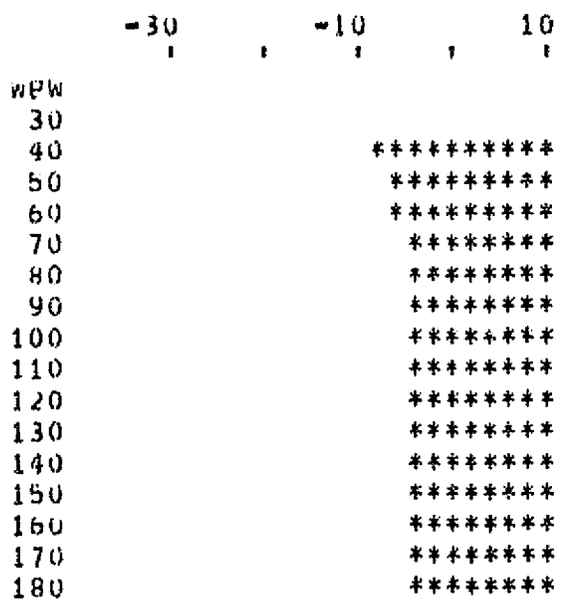
TAH VS. TWP (ADDRESS RZ1) VCC = 5.00 V



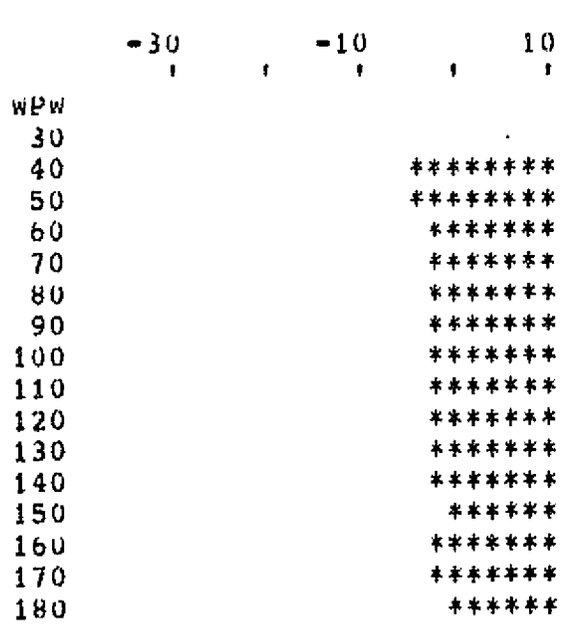
TAH VS. TWP (ADDRESS RZ) VCC = 5.00 V



TAH VS. TWP (ADDRESS RZ1) VCC = 10.0 V



TAH VS. TWP (ADDRESS RZ) VCC = 10.0 V



REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

RCA COP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 25 C SN: 2

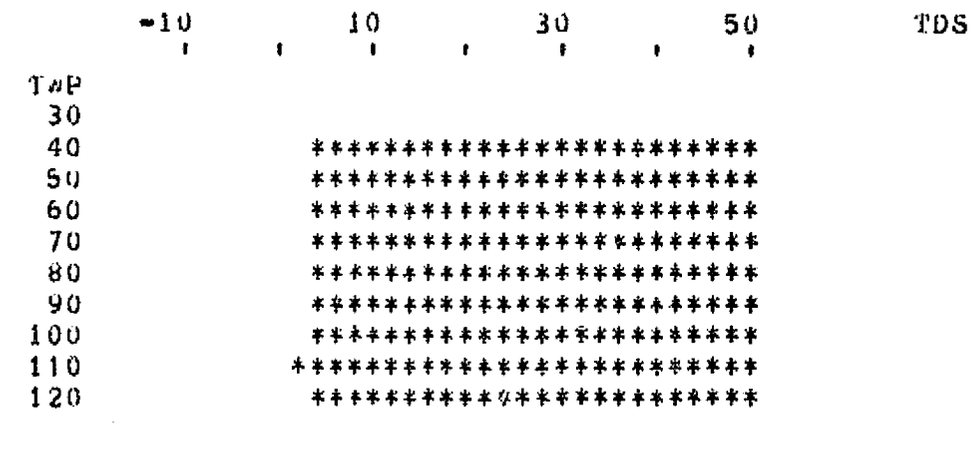
TDS VS. TWP (DATA RZI) VCC = 5.00 V

```
        -10        10        30        50        TDS
         '    '    '    '    '    '    '
TWP
 30
 40
 50
 60          ************************
 70          ************************
 80          ************************
 90          ************************
100          ************************
110          ************************
120          ************************
```

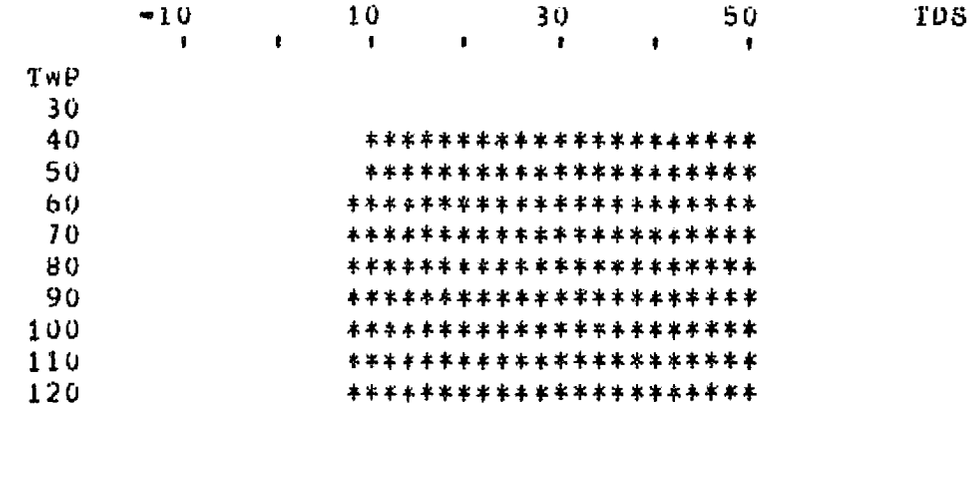
TDS VS. TWP (DATA RZ) VCC = 5.00 V

```
        -10        10        30        50        TDS
         '    '    '    '    '    '    '
TWP
 30
 40
 50
 60               ****************
 70              ****************
 80              ****************
 90              ****************
100              ****************
110              ****************
120              ****************
```

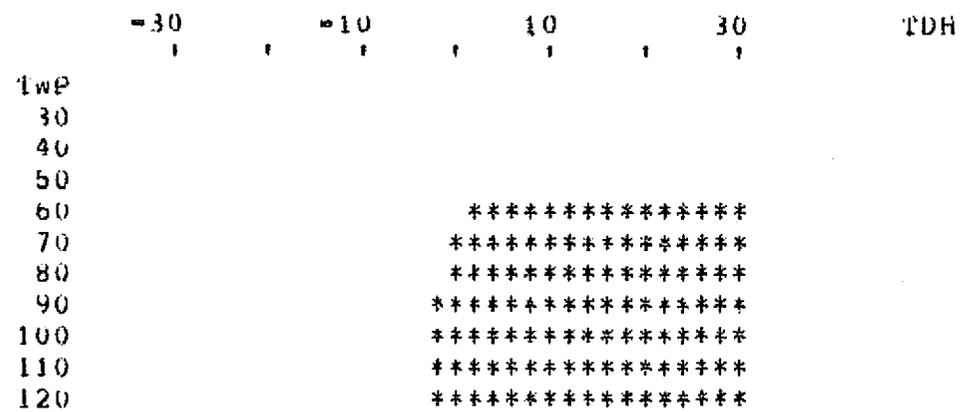
TDS VS. TWP (DATA RZ1) VCC = 10.0 V



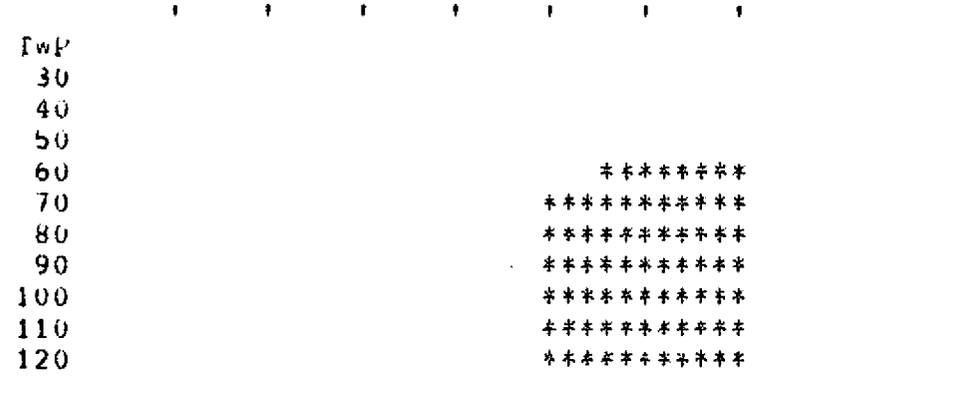
TDS VS. TWP (DATA RZ) VCC = 10.0 V



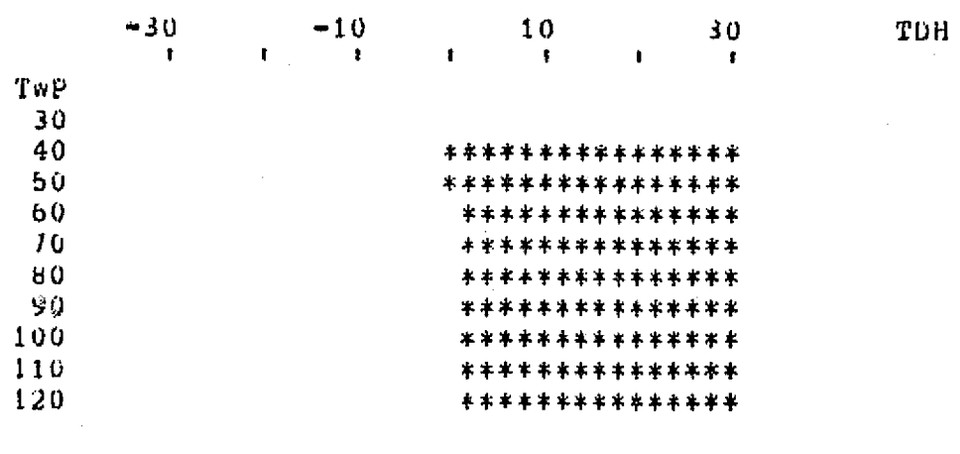
TDH VS. TwP (DATA RZI) VCC = 5.00 V



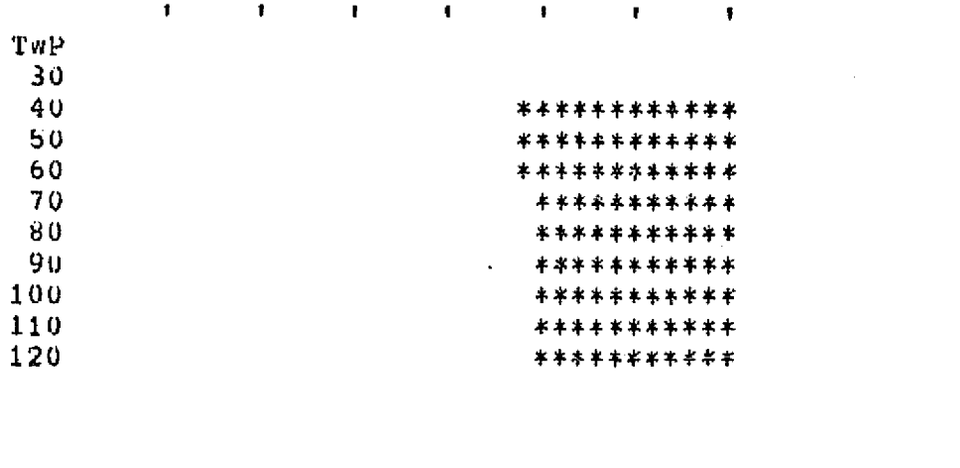
TDH VS. TwP (DATA RZ) VCC = 5.00 V



TDH VS. TWP (DATA RZI) VCC = 10.0 V



TDH VS. TWP (DATA RZ) VCC = 10.0 V



REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

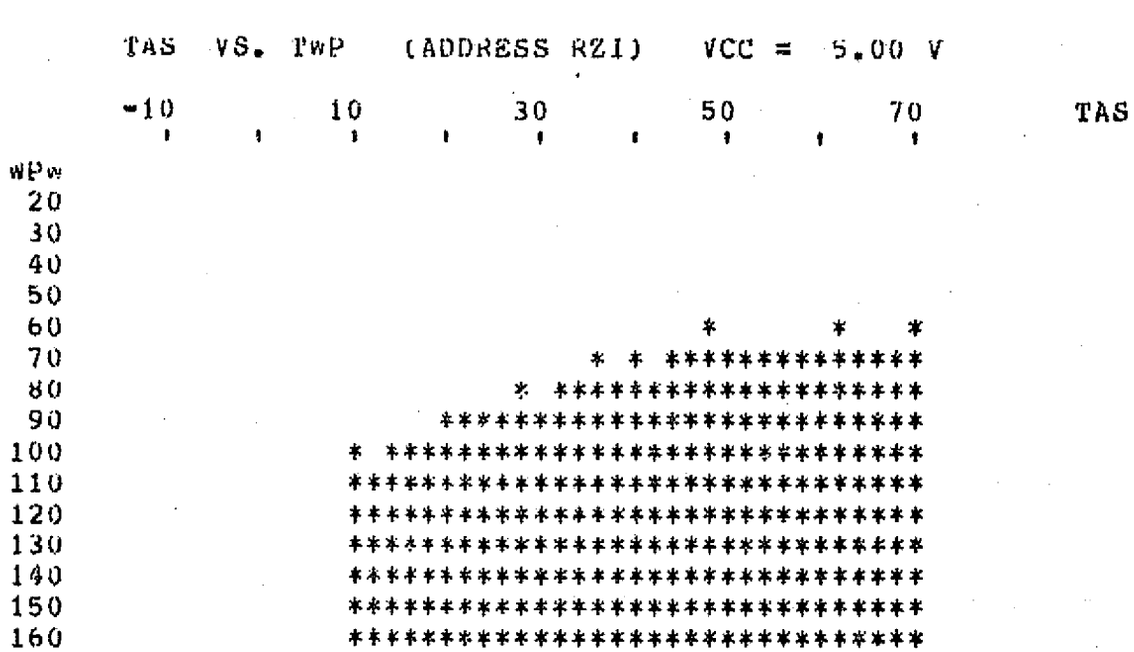
RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 25 C SN: 2

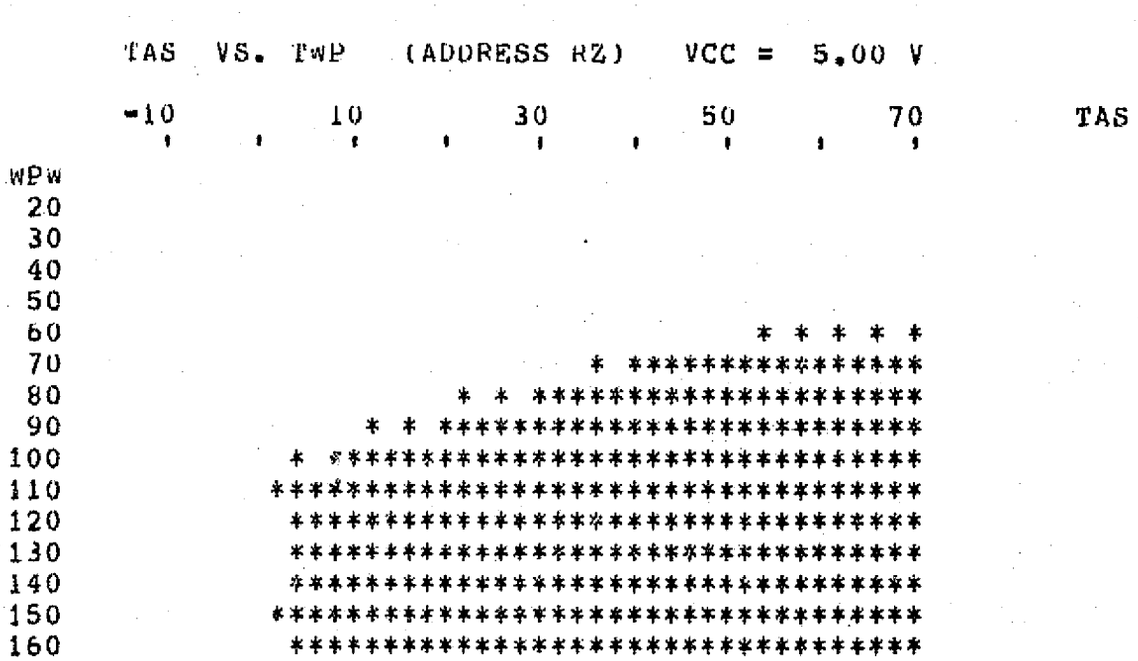
ICC VS. CYCLE TIME VCC = 10.0V

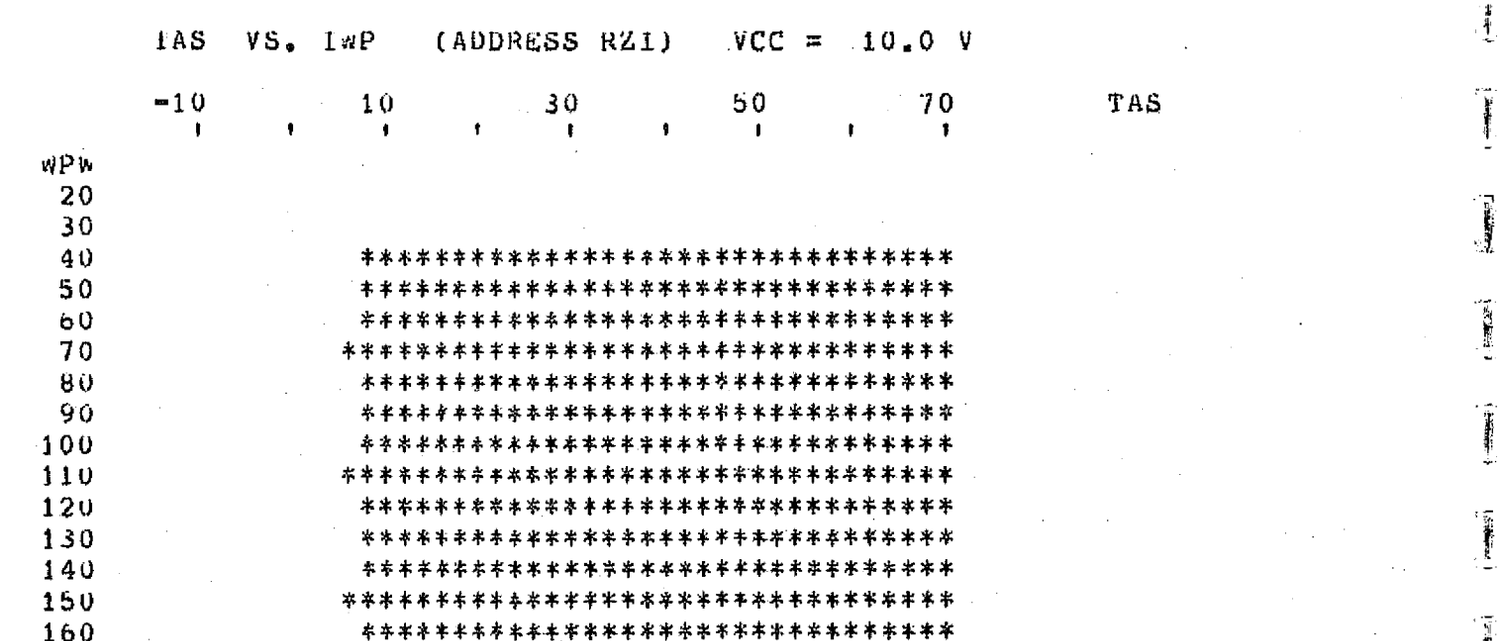
```
          0         10        20        ICC
          '    '    '    '    '
CYCLE
100.N                        >
200.N                   *
400.N              *
800.N            *
1.60U           *
3.20U          *
6.40U        *
12.8U         *
25.6U        *
51.2U         *
102.U         *
205.U     *
410.U      *
819.U     *
```

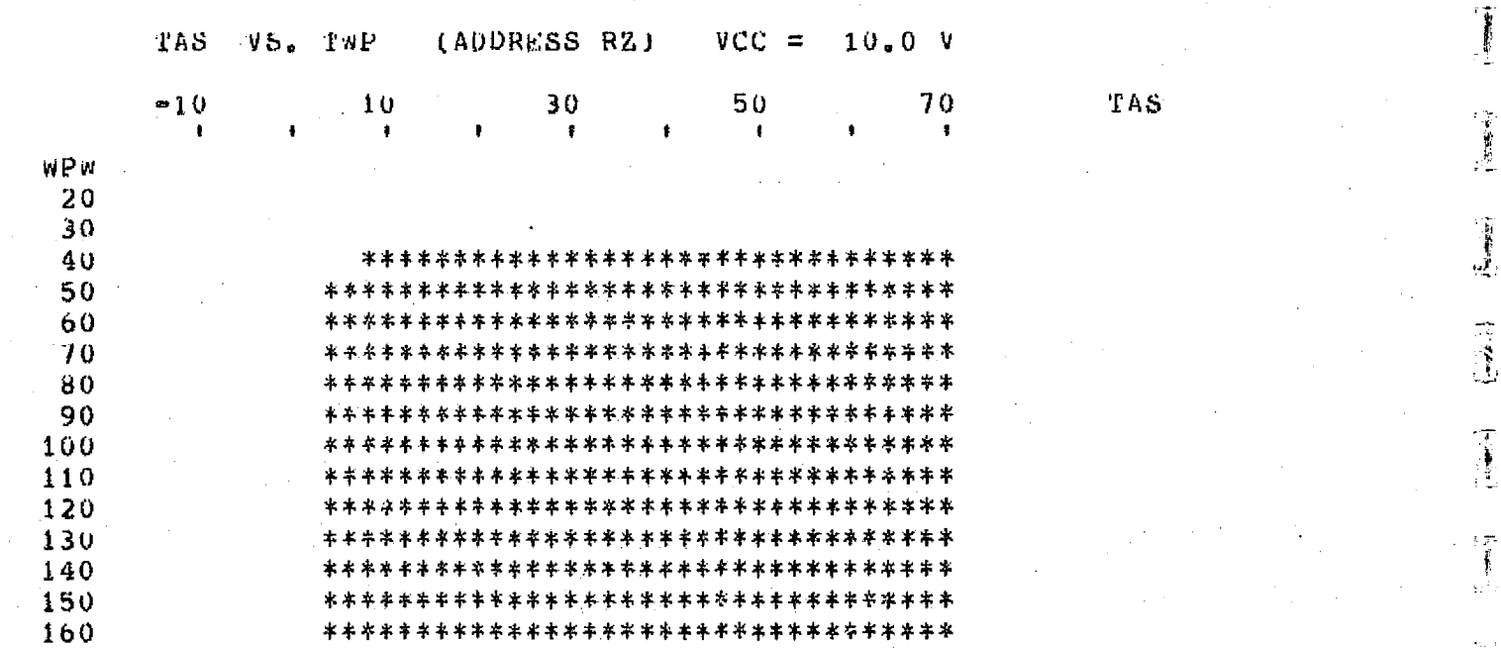
DEVICE PASSED ALL TESTS

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: -55 C SN: 2



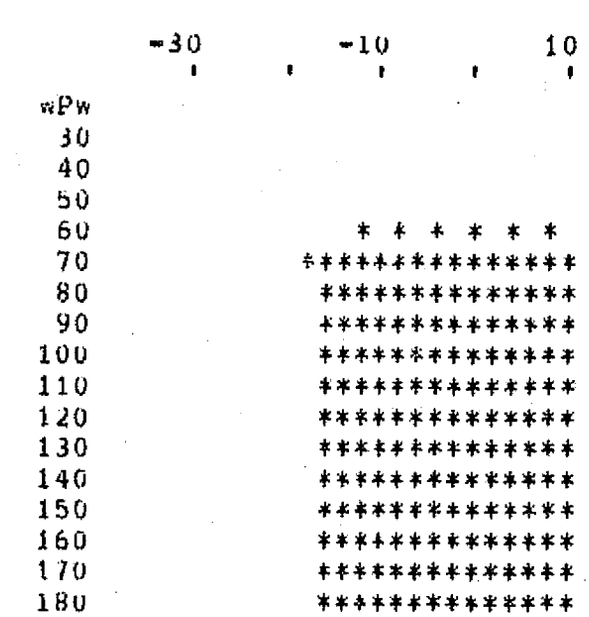



TAS VS. TWP (ADDRESS RZI) VCC = 10.0 V
-10
10
30
50
70
TAS
TWP
20
30
40
50
60
70
80
90
100
110
120
130
140
150
160

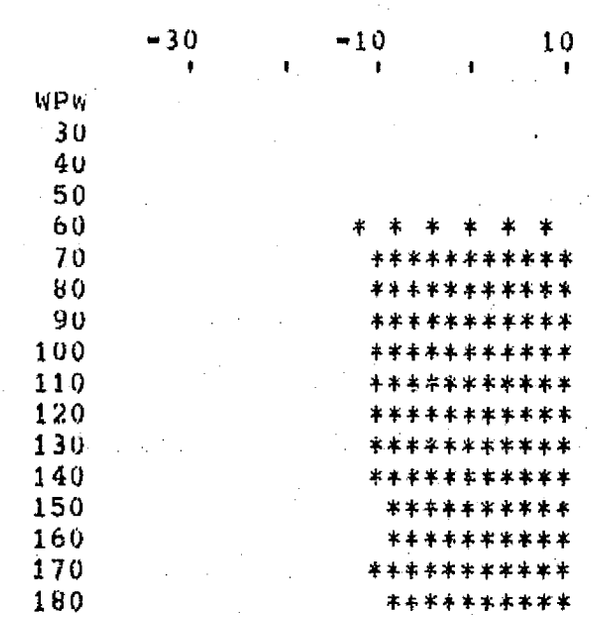

TAS VS. TWP (ADDRESS RZ) VCC = 10.0 V
-10
10
30
50
70
TAS
TWP
20
30
40
50
60
70
80
90
100
110
120
130
140
150
160

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: -55 C SN: 2

TAH VS. TWP (ADDRESS RZ1) VCC = 5.00 V



TAH VS. TWP (ADDRESS RZ) VCC = 5.00 V



REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

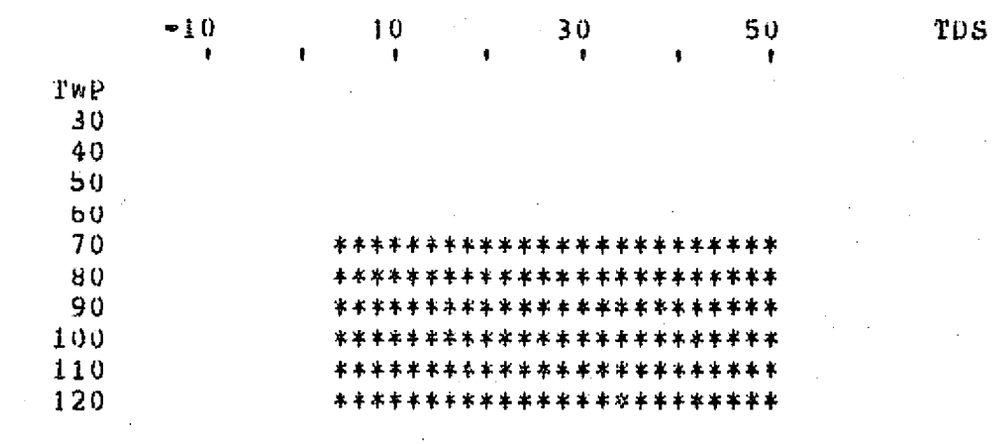
TAH VS. TWP (ADDRESS RZI) VCC = 10.0 V

```
        -30        -10         10          TAH
          '     '     '     '     '
WPW
 30
 40                    *********
 50                     ********
 60                     ********
 70                     ********
 80                     ********
 90                     ********
100                     ********
110                     ********
120                     ********
130                     ********
140                     ********
150                     ********
160                     ********
170                     ********
180                     ********
```

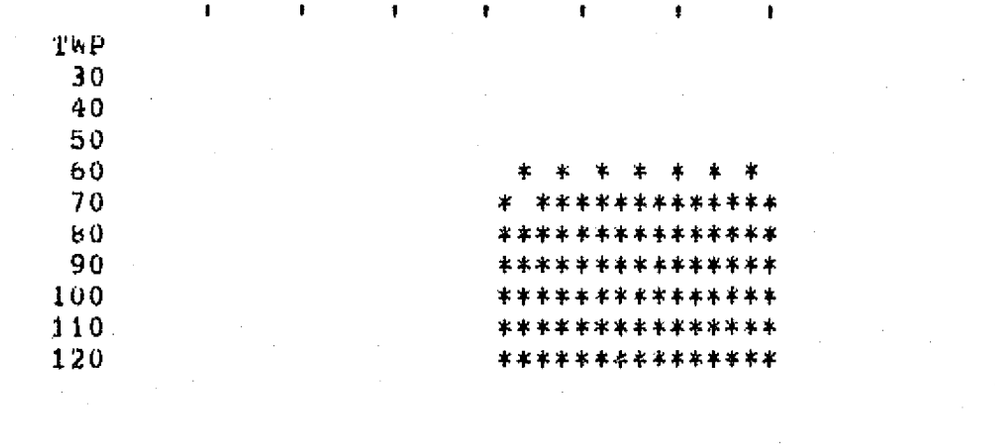
TAH VS. TWP (ADDRESS RZ) VCC = 10.0 V

```
        -30        -10         10          TAH
          '     '     '     '     '
WPW
 30
 40                    ********
 50                     *******
 60                     *******
 70                     *******
 80                     *******
 90                     *******
100                      ******
110                      ******
120                      ******
130                      ******
140                      ******
150                      ******
160                      ******
170                      ******
180                      ******
```

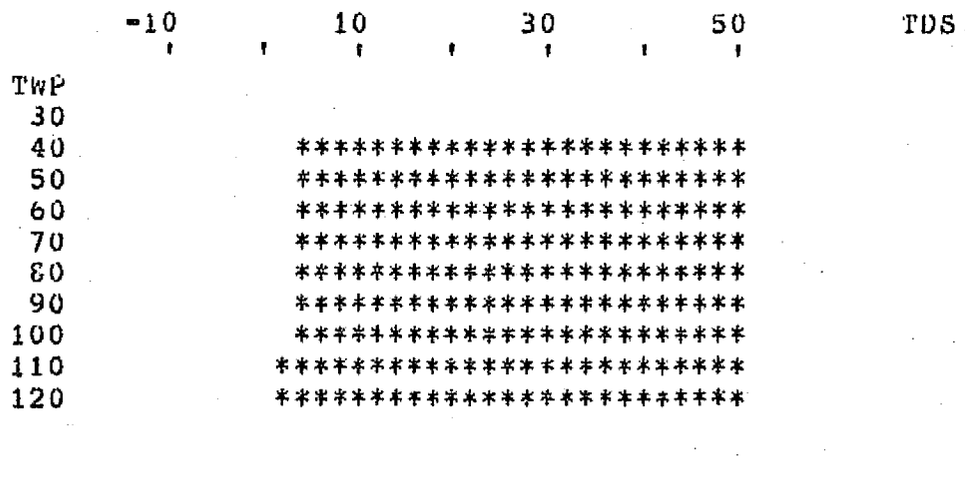
TDS VS. TWP (DATA RZ1) VCC = 5.00 V



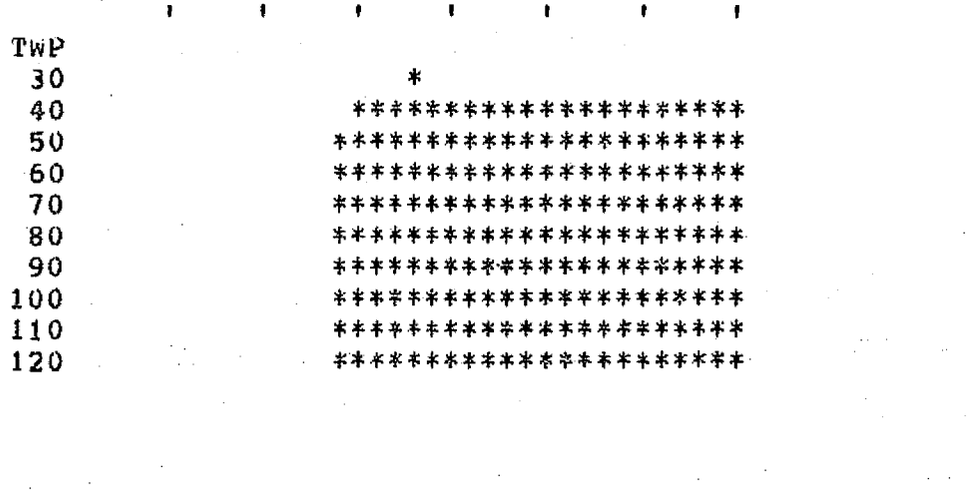
TDS VS. TWP (DATA RZ) VCC = 5.00 V



TDS VS. TWP (DATA RZ1) VCC = 10.0 V



TDS VS. TWP (DATA RZ) VCC = 10.0 V



TDH VS. TWP (DATA RZ1) VCC = 5.00 V

```
        -30        -10         10         30          TDH
         '    '     '     '     '     '     '
TWP
 30
 40
 50
 60
 70                  **********
 80                 **********
 90                 **********
100                 **********
110                 **********
120                 **********
```

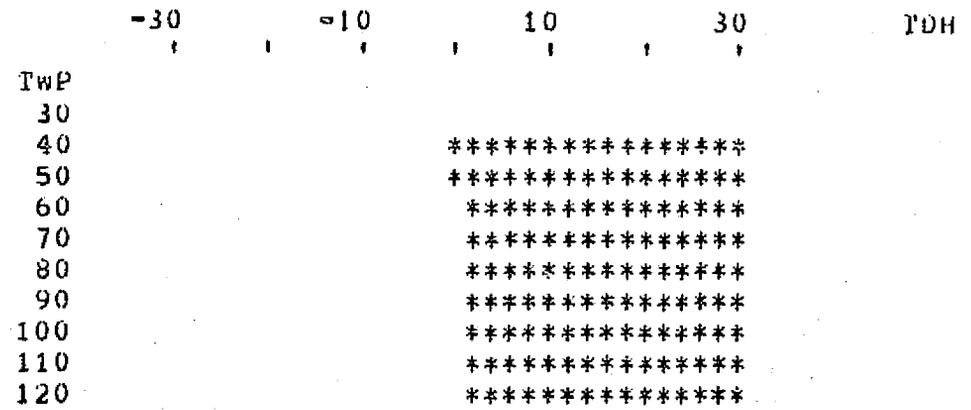
TDH VS. TWP (DATA RZ) VCC = 5.00 V

```
        -30        -10         10         30          TDH
         '    '     '     '     '     '     '
TWP
 30
 40
 50
 60
 70                   **********
 80                  **********
 90                  **********
100                  **********
110                  **********
120                  **********
```

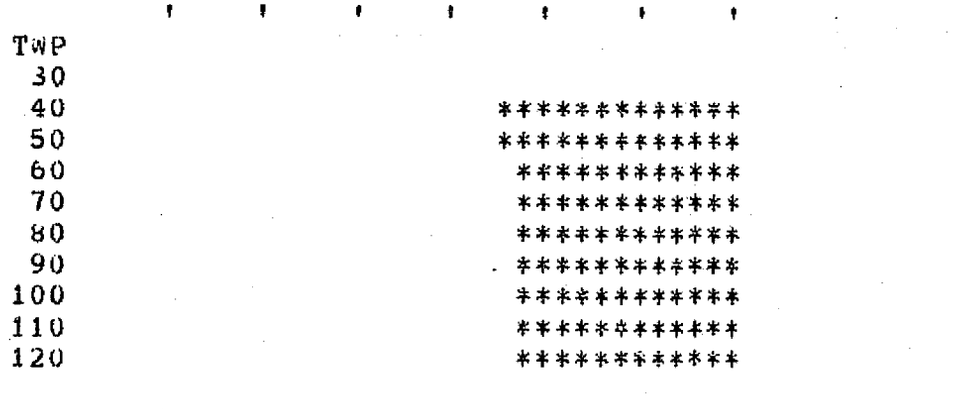
REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: -55 C SN: 2

TDH VS. TWP (DATA RZI) VCC = 10.0 V

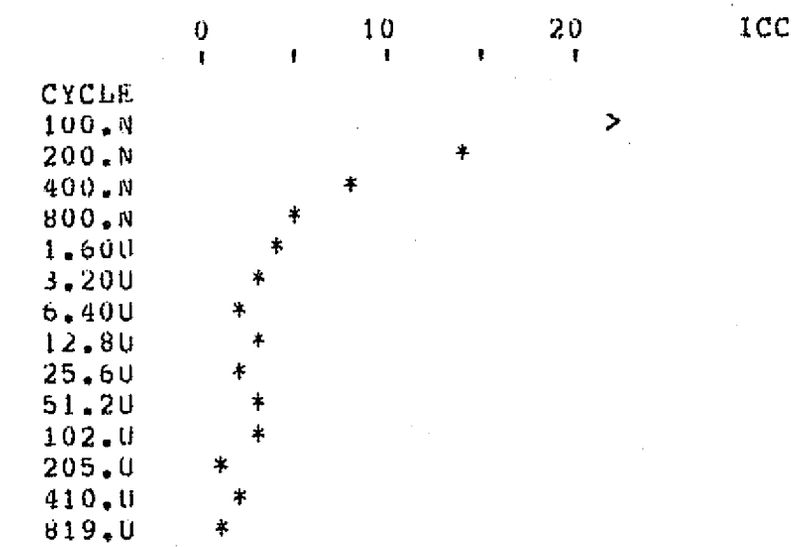


TDH VS. TWP (DATA RZ) VCC = 10.0 V



RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: -55 C SN: 2

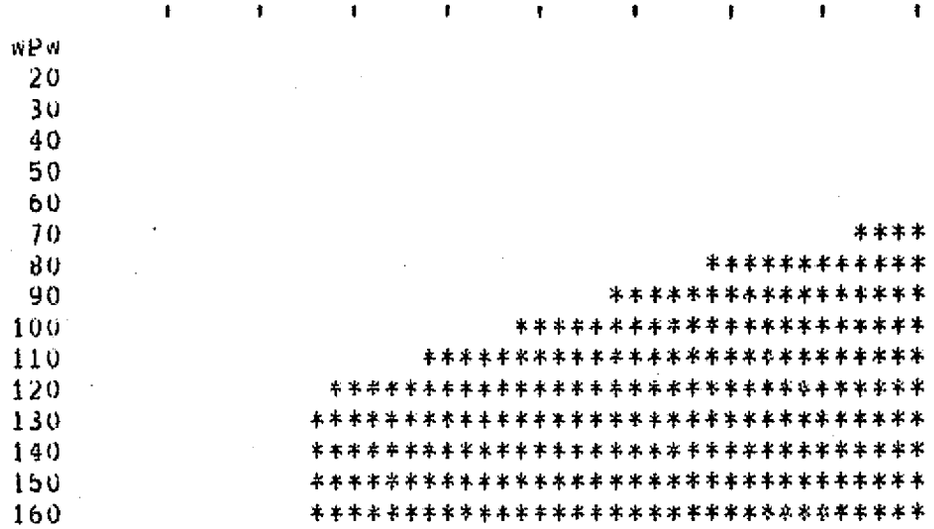
ICC VS. CYCLE TIME VCC = 10.0V



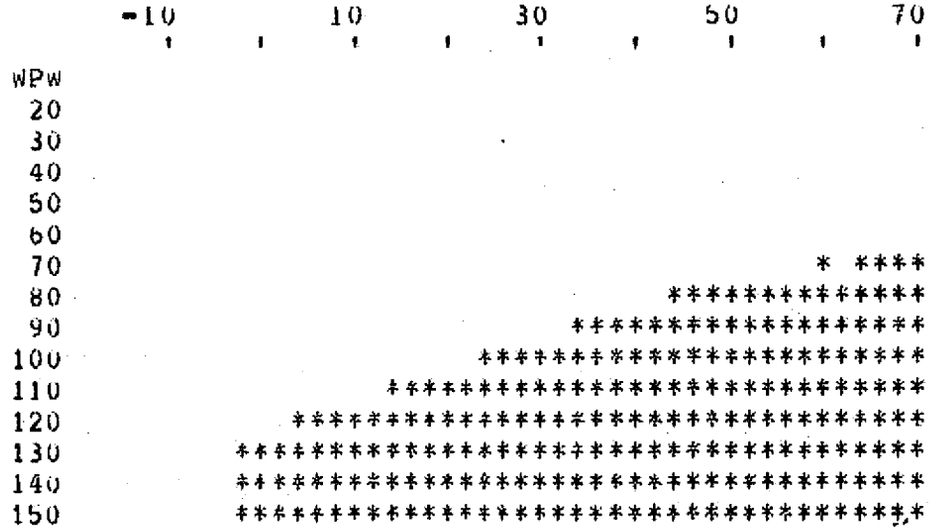
DEVICE PASSED ALL TESTS

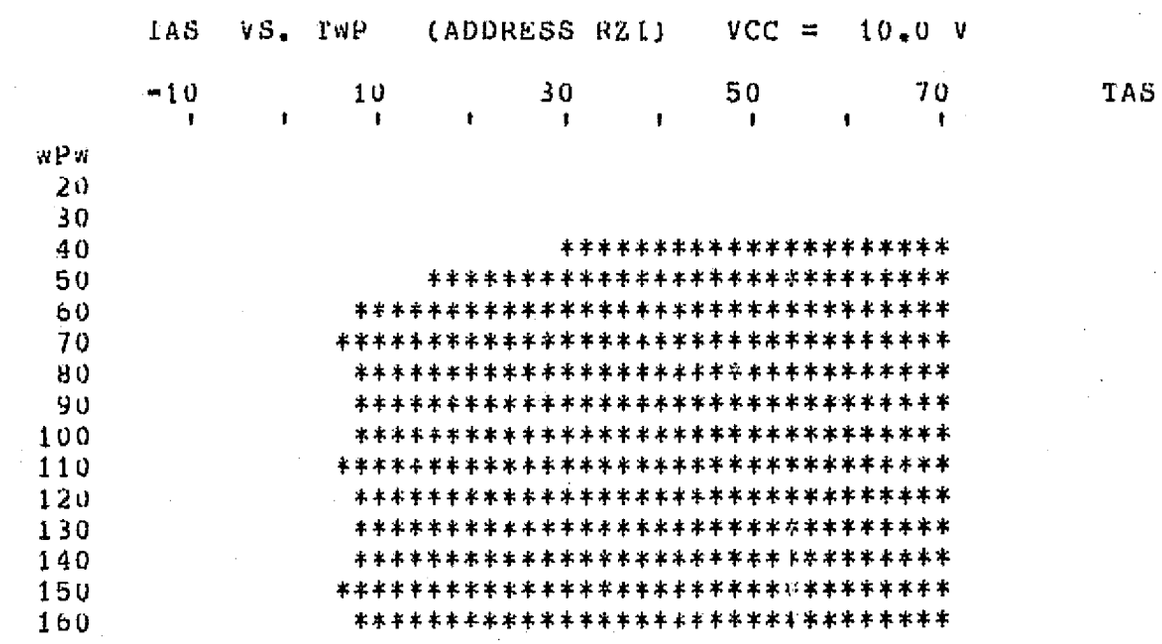
RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 125 C SN: 2

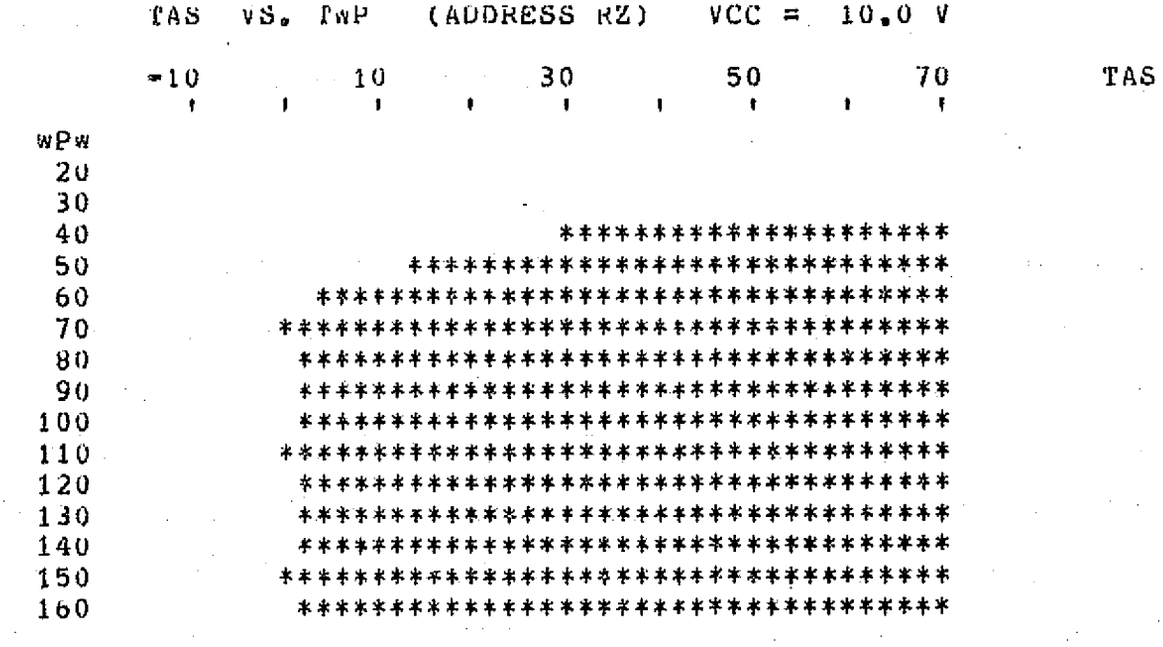
TAS VS. TWP (ADDRESS RZI) VCC = 5.00 V



TAS VS. TWP (ADDRESS RZ) VCC = 5.00 V







REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

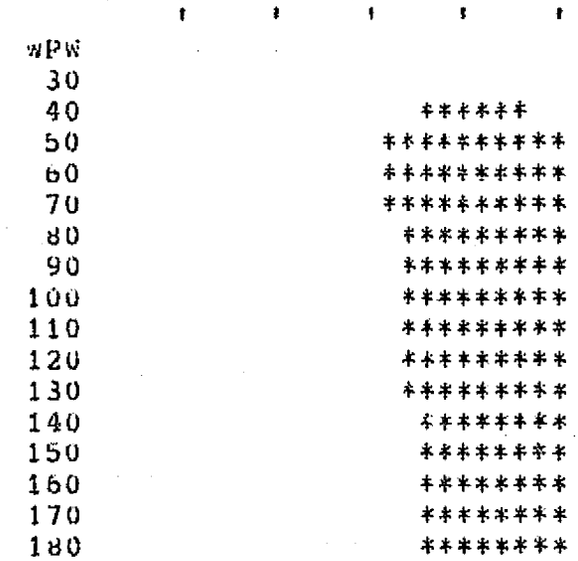
TAH VS. TWP (ADDRESS RZI) VCC = 5.00 V

```
        -30        -10         10         TAH
         '     '     '     '     '
WPW
 30
 40
 50
 60
 70              ***********
 80            ***************
 90             ***************
100             ***************
110             ***************
120             ***************
130             ***************
140             ***************
150             ***************
160             ***************
170             ***************
180             ***************
```

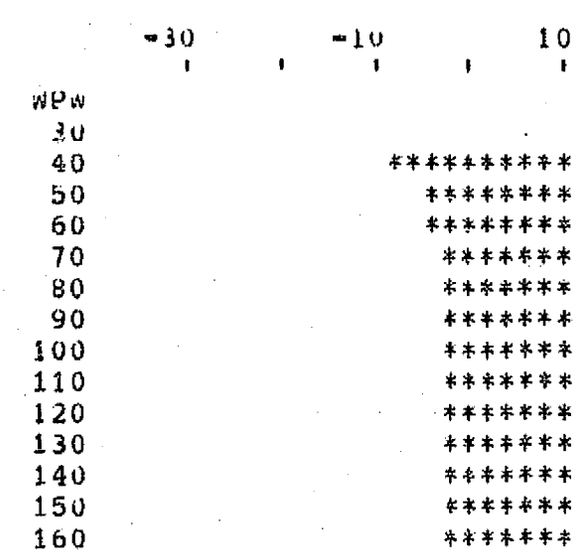
TAH VS. TWP (ADDRESS RZ) VCC = 5.00 V

```
        -30        -10         10         TAH
         '     '     '     '     '
WPW
 30
 40
 50
 60
 70             **************
 80               ***********
 90               ***********
100                **********
110                **********
120                **********
130                **********
140                **********
150                **********
160                **********
170                **********
180                **********
```

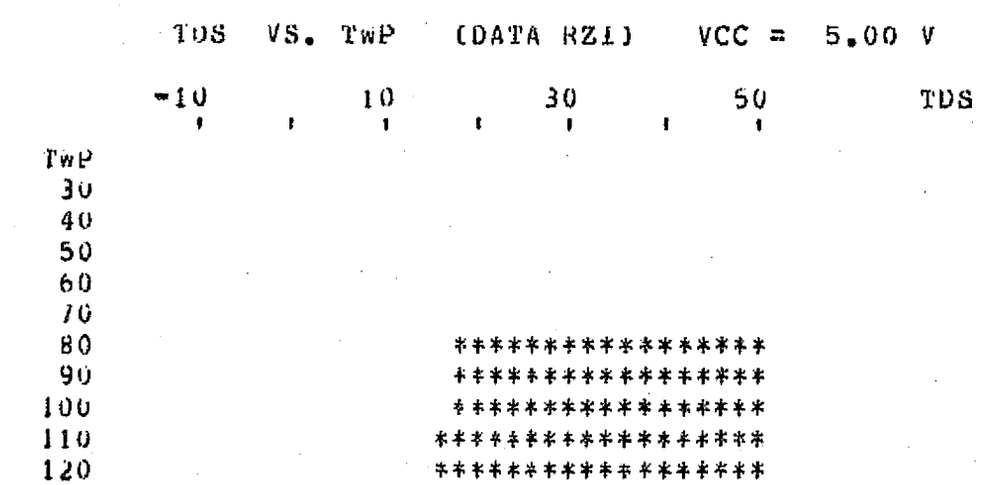
TAH VS. TWP (ADDRESS RZI) VCC = 10.0 V

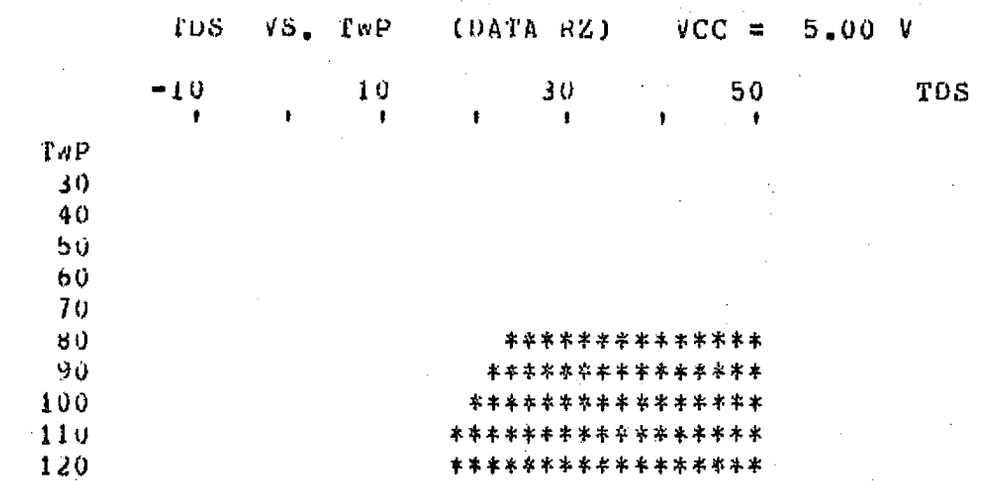


TAH VS. TWP (ADDRESS RZ) VCC = 10.0 V

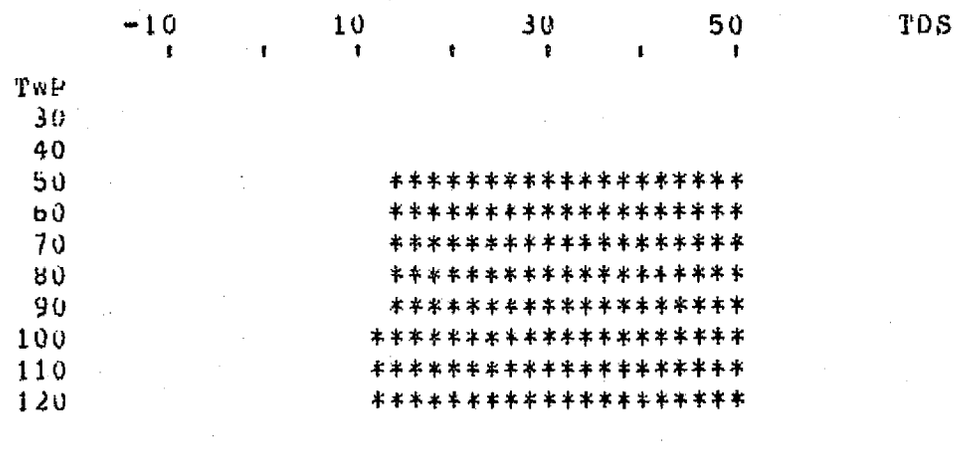


RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 125 C SN: 2

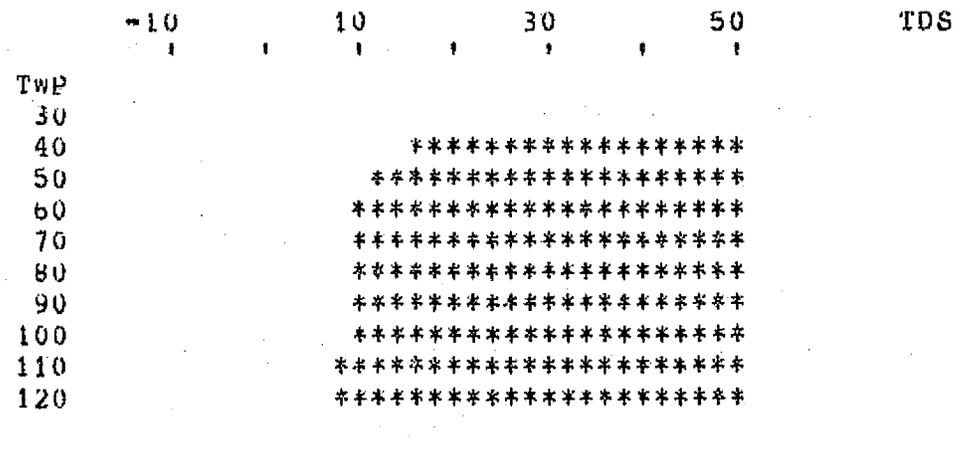




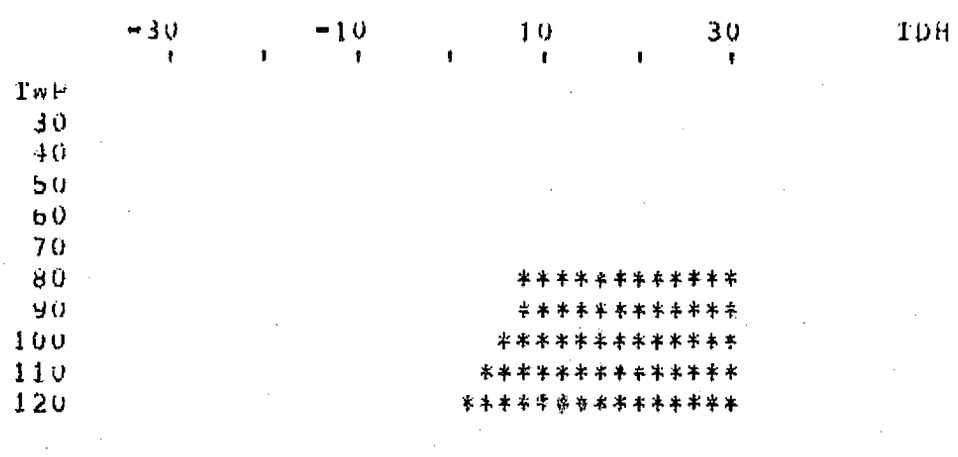
TDS VS. TWP (DATA RZI) VCC = 10.0 V



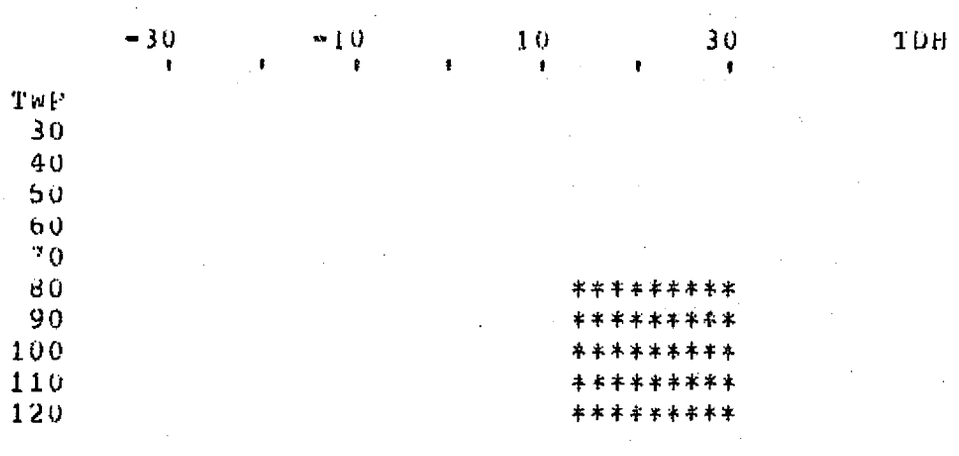
TDS VS. TWP (DATA RZ) VCC = 10.0 V



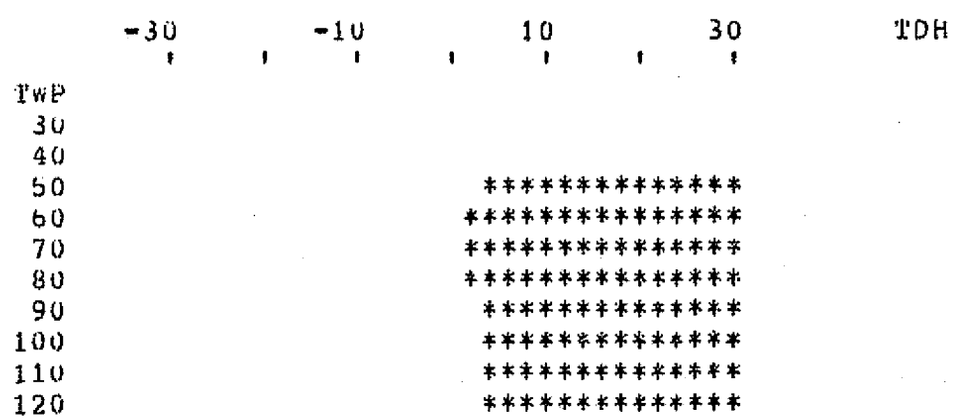
TDH VS. TWP (DATA RZ') VCC = 5.00 V



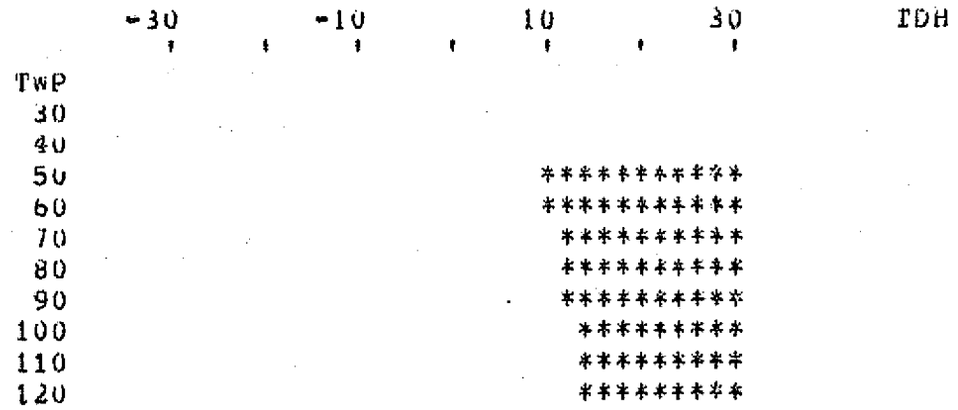
TDH VS. TWP (DATA RZ) VCC = 5.00 V



TDH VS. TWP (DATA RZI) VCC = 10.0 V



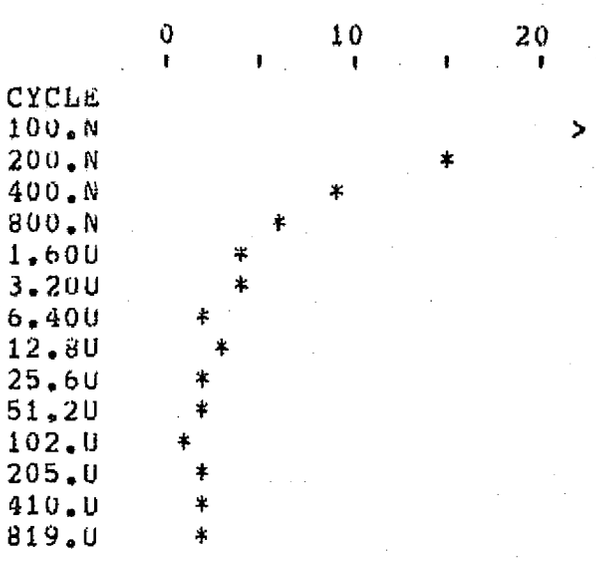
TDH VS. TWP (DATA RZ) VCC = 10.0 V



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ORIGINAL PAGE IS POOR

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 125 C SN: 2

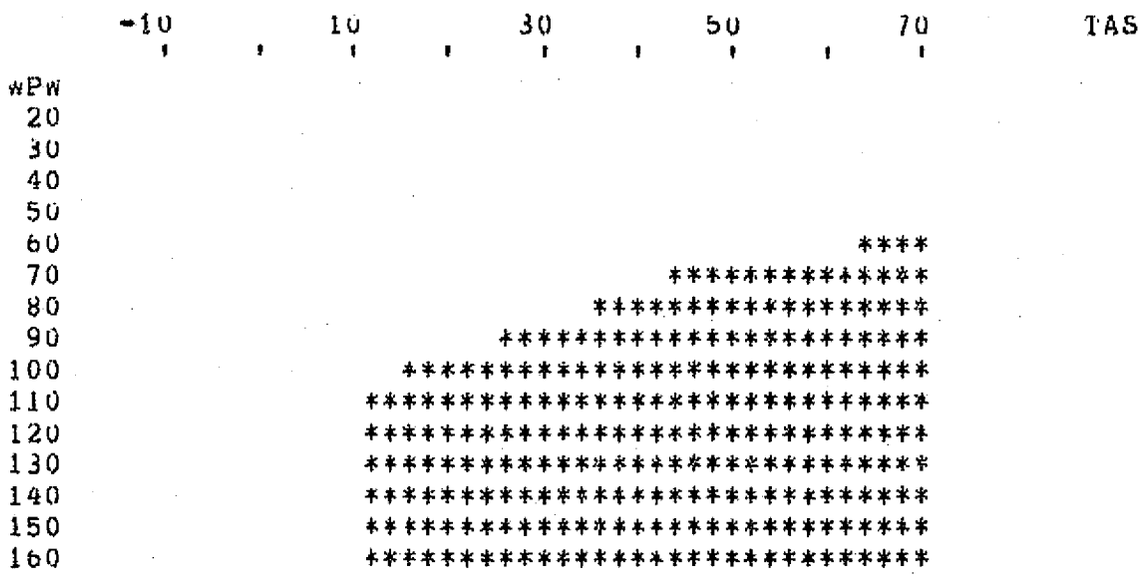
ICC VS. CYCLE TIME VCC = 10.0V



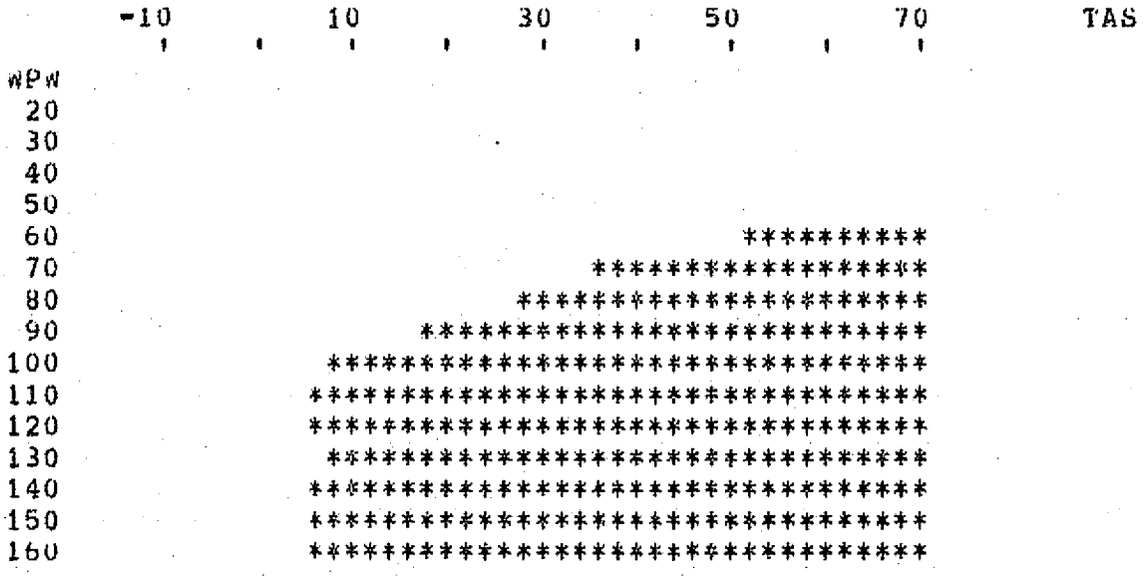
DEVICE PASSED ALL TESTS

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 25 C SN:

TAS VS. TWP (ADDRESS RZ1) VCC = 5.00 V

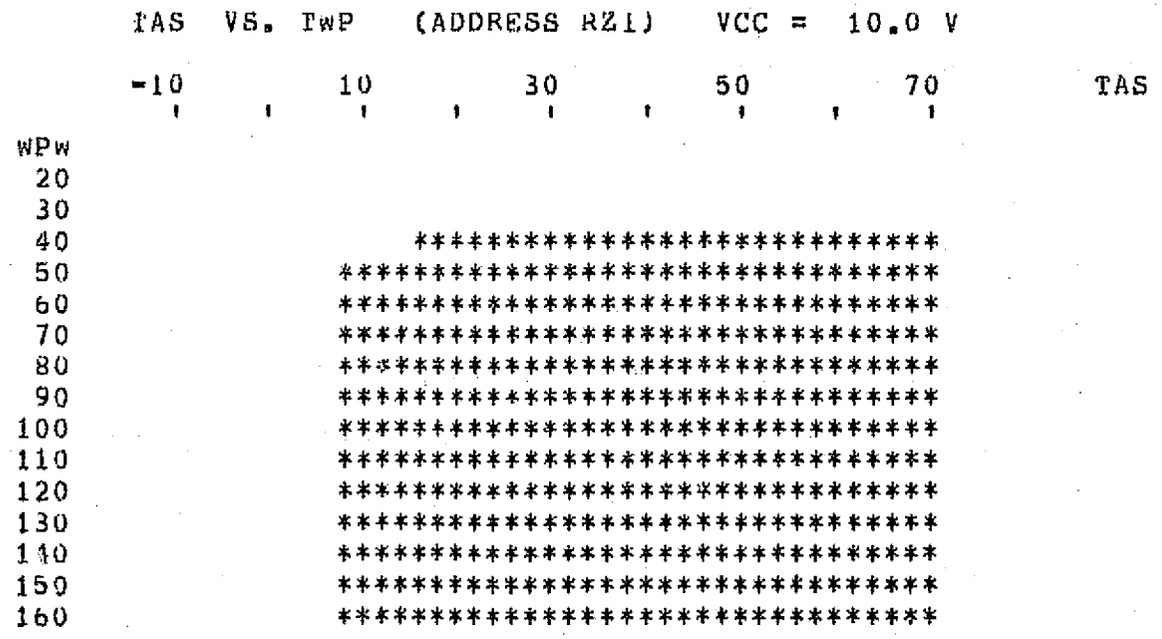


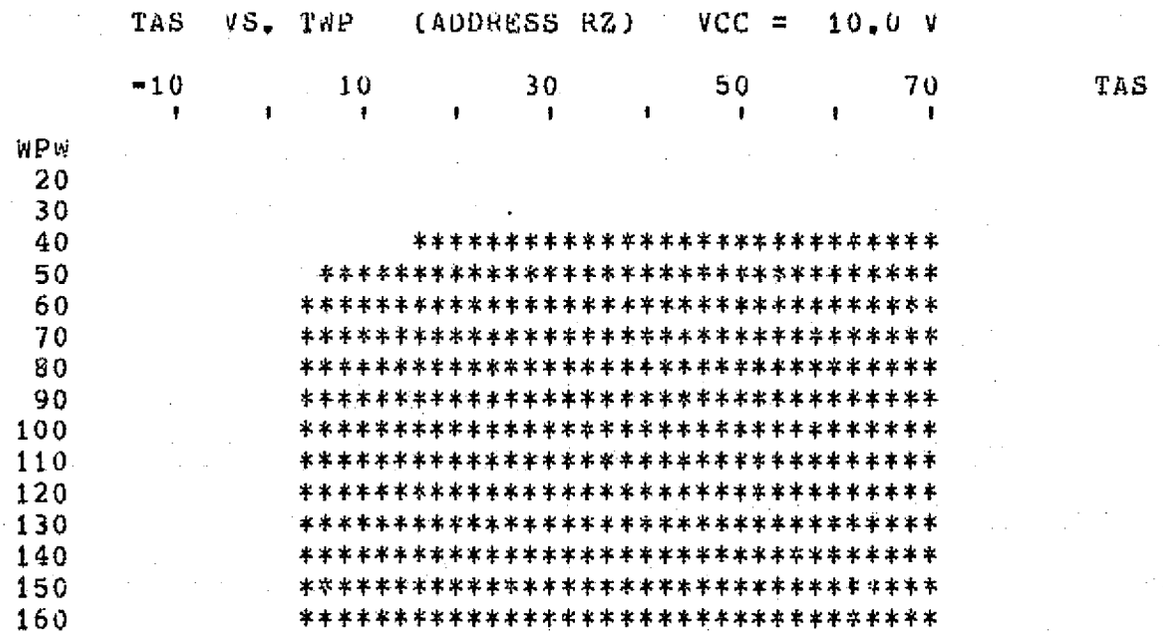
TAS VS. TWP (ADDRESS RZ) VCC = 5.00 V



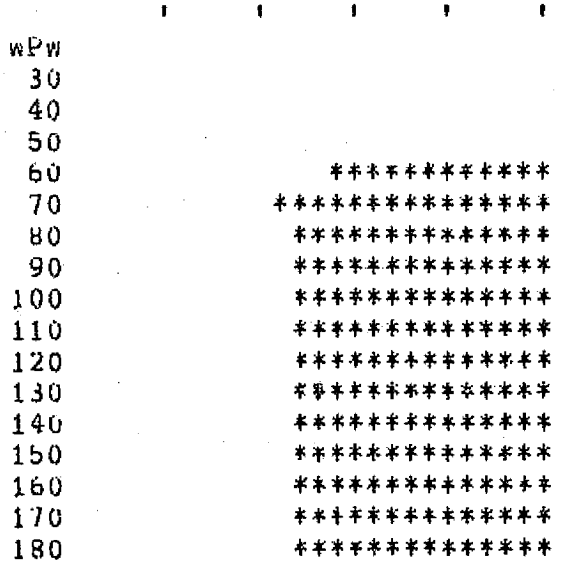
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ORIGINAL PAGE IS POOR

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 25 C SN: 3

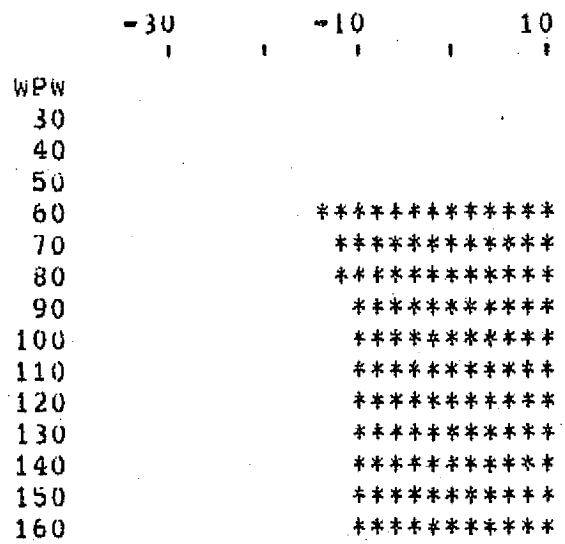




TAH VS. TWP (ADDRESS RZJ) VCC = 5.00 V



TAH VS. TWP (ADDRESS RZ) VCC = 5.00 V



TAH VS. TWP (ADDRESS RZI) VCC = 10.0 V

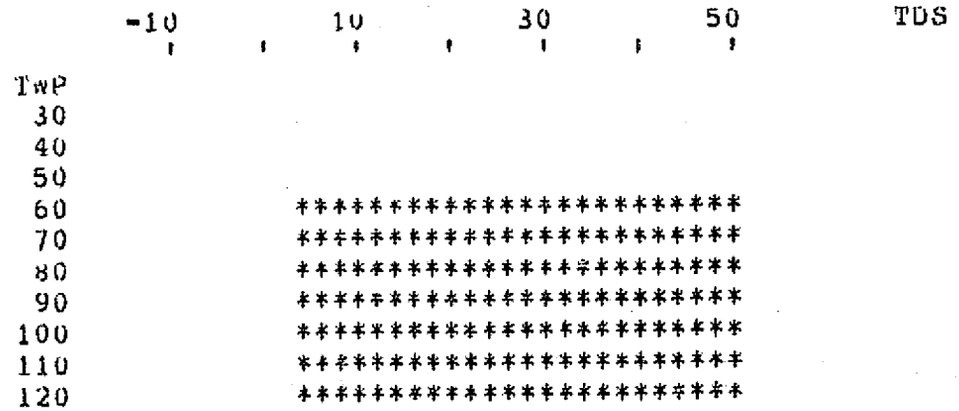
```
      -30        -10         10         TAH
       '    '     '     '     '
WPW
 30
 40                 **********
 50                 **********
 60                  *********
 70                  *********
 80                  *********
 90                  *********
100                  *********
110                  *********
120                  *********
130                  *********
140                  *********
150                  *********
160                  *********
170                  *********
180                  *********
```

TAH VS. TWP (ADDRESS RZ) VCC = 10.0 V

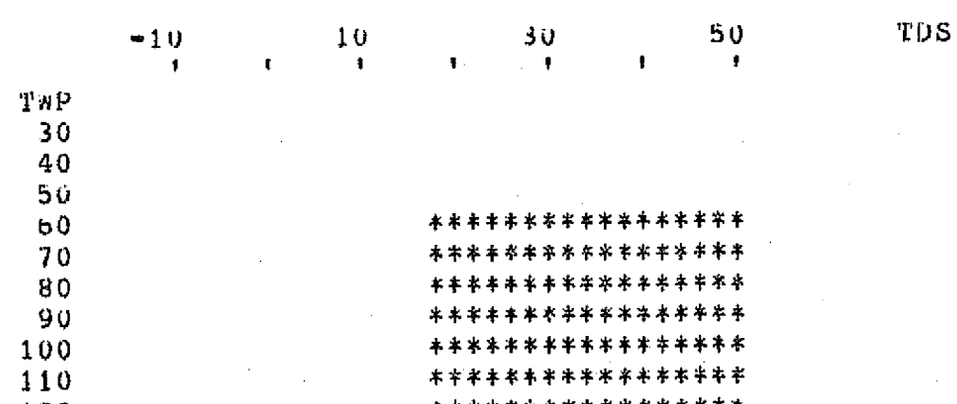
```
      -30        -10         10         TAH
       '    '     '     '     '
WPW
 30
 40                 *********
 50                  ********
 60                  ********
 70                  ********
 80                   *******
 90                   *******
100                   *******
110                   *******
120                   *******
130                   *******
140                   *******
150                   *******
160                   *******
170                   *******
180                   *******
```

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 25 C SN:

TDS VS. TWP (DATA RZ1) VCC = 5.00 V



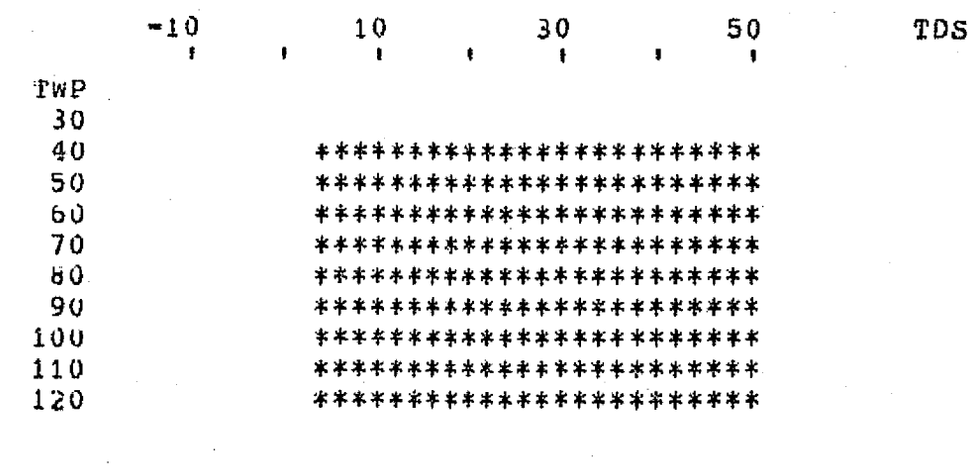
TDS VS. TWP (DATA RZ) VCC = 5.00 V



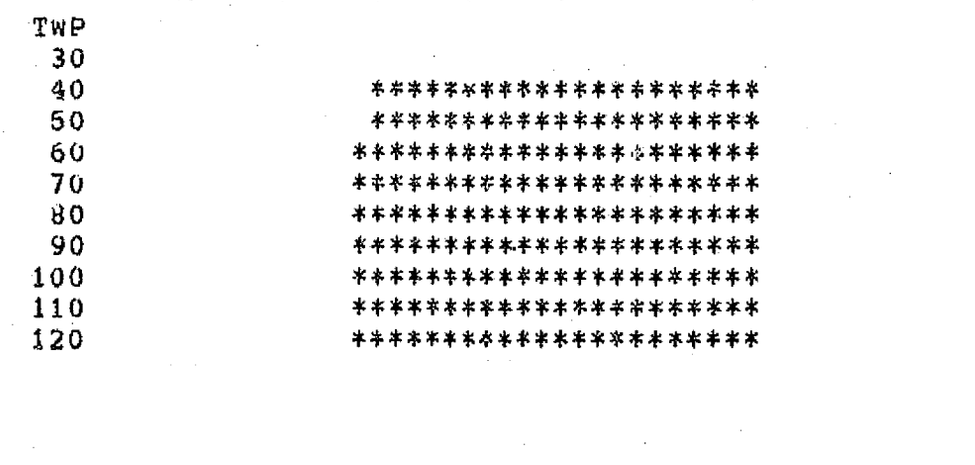
REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 25 C SN: 3

TDS VS. TWP (DATA RZI) VCC = 10.0 V

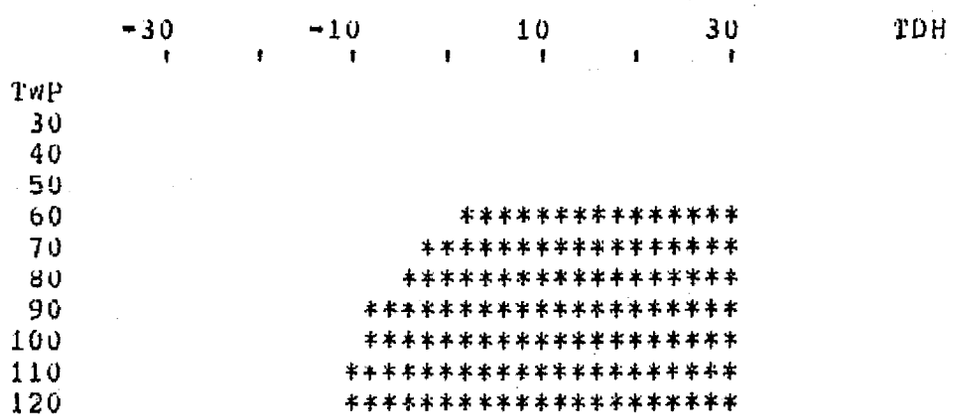


TDS VS. TWP (DATA RZ) VCC = 10.0 V

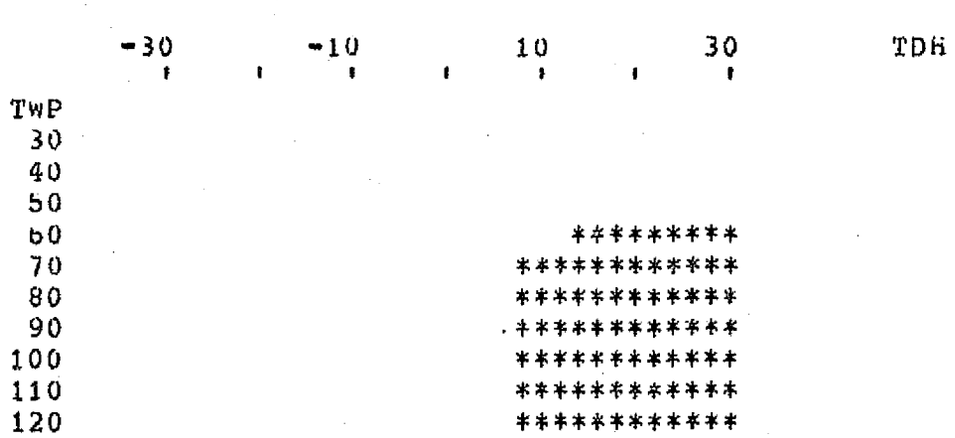


RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 25 C SN:

TDH VS. TWP (DATA RZ1) VCC = 5.00 V



TDH VS. TWP (DATA RZ) VCC = 5.00 V

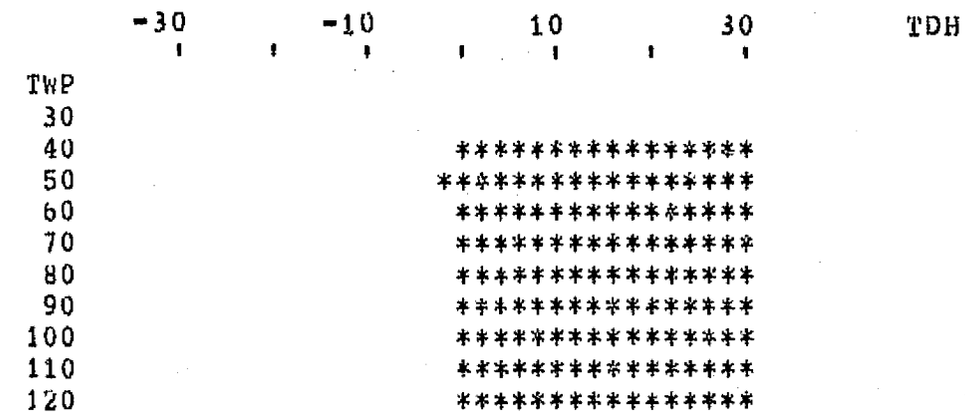


REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

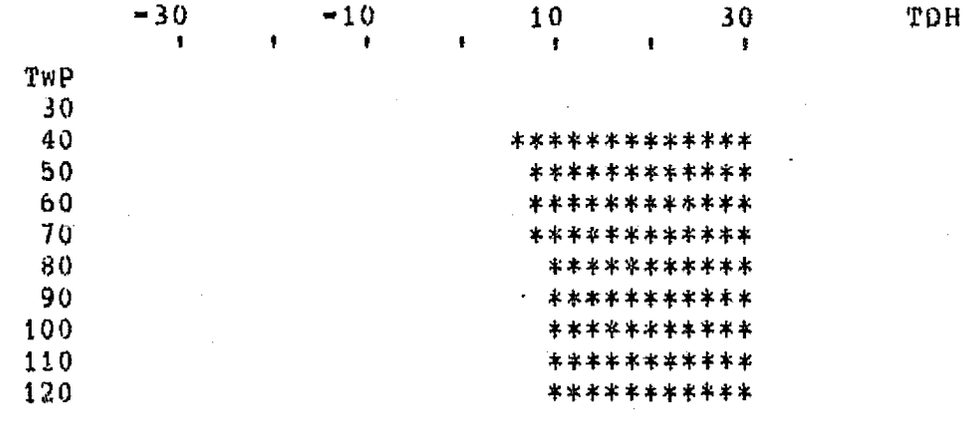
REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 25 C SN: 3

TDH VS. TWP (DATA RZ1) VCC = 10.0 V

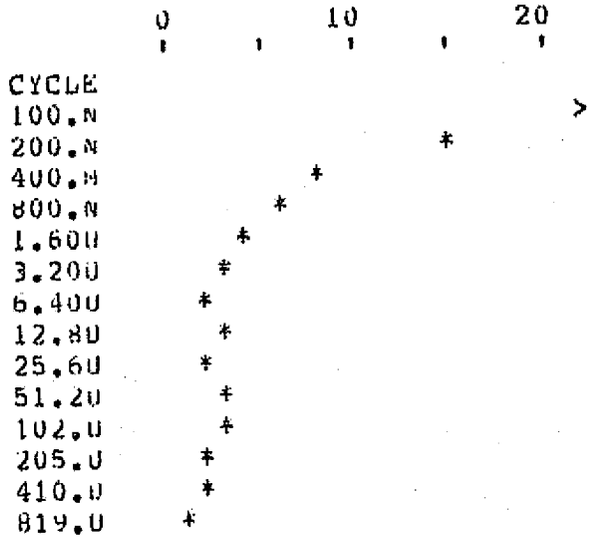


TDH VS. TWP (DATA RZ) VCC = 10.0 V



RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 25 C SN:

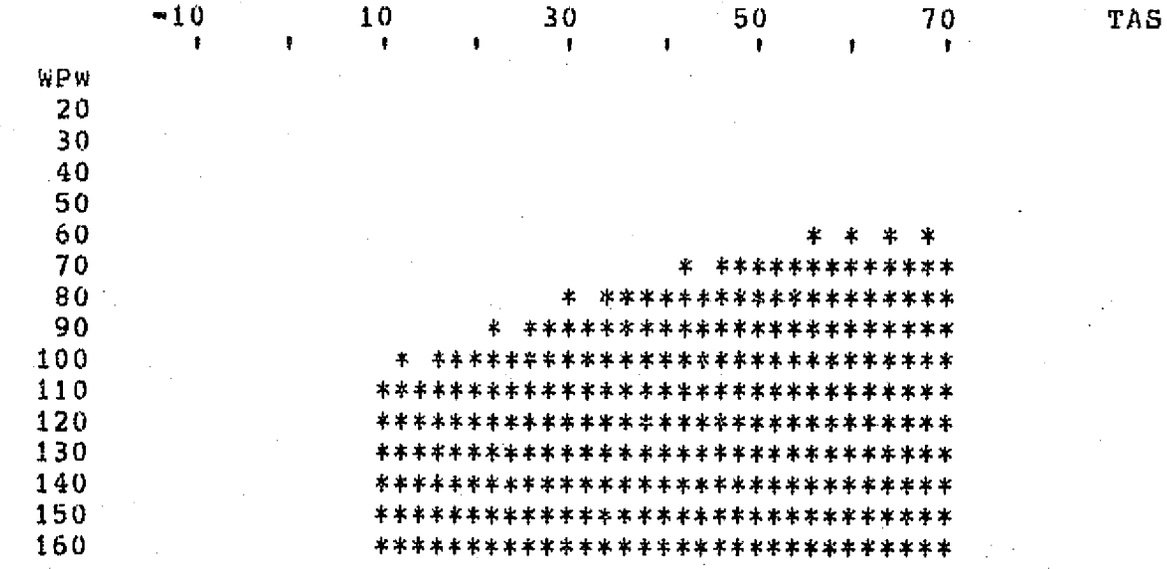
ICC VS. CYCLE TIME VCC = 10.0V



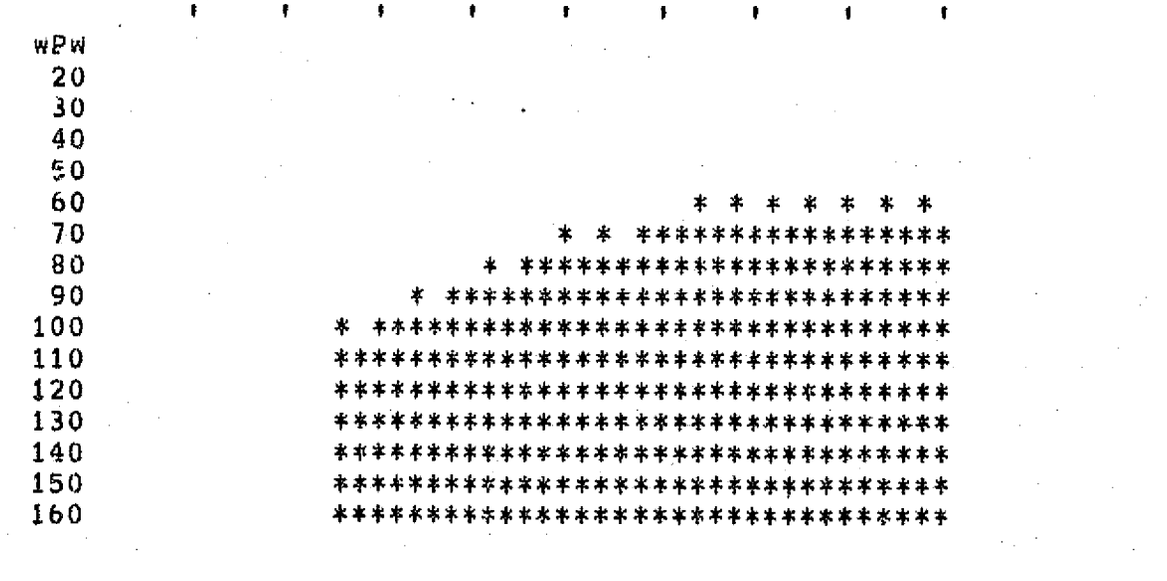
DEVICE PASSED ALL TESTS

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS PO

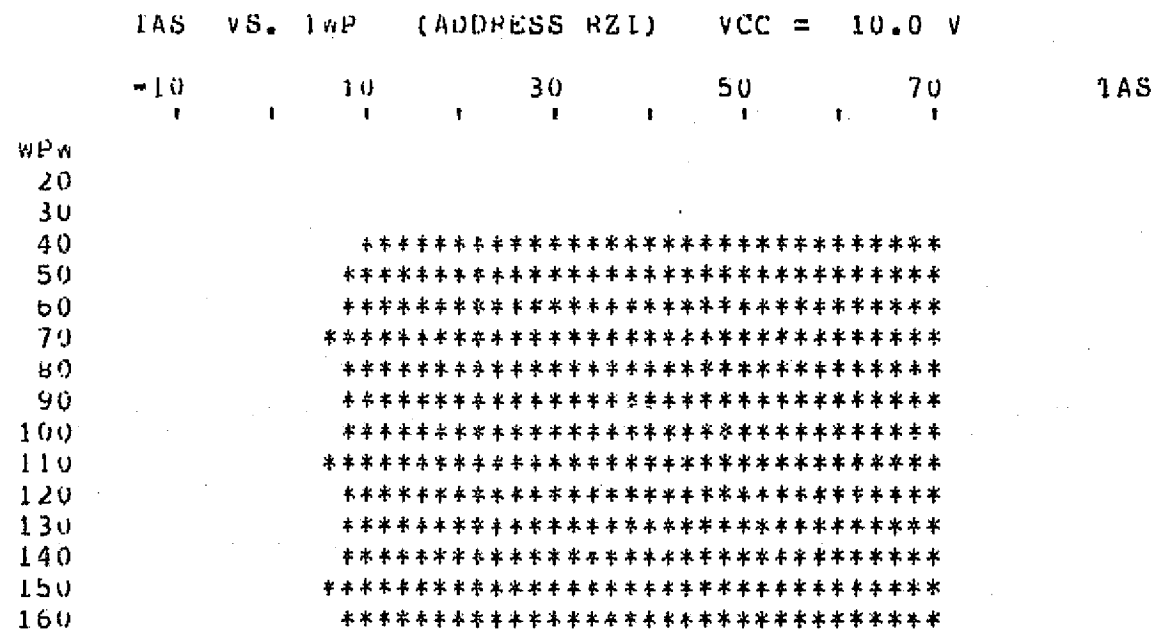
TAS VS. TWP (ADDRESS RZI) VCC = 5.00 V

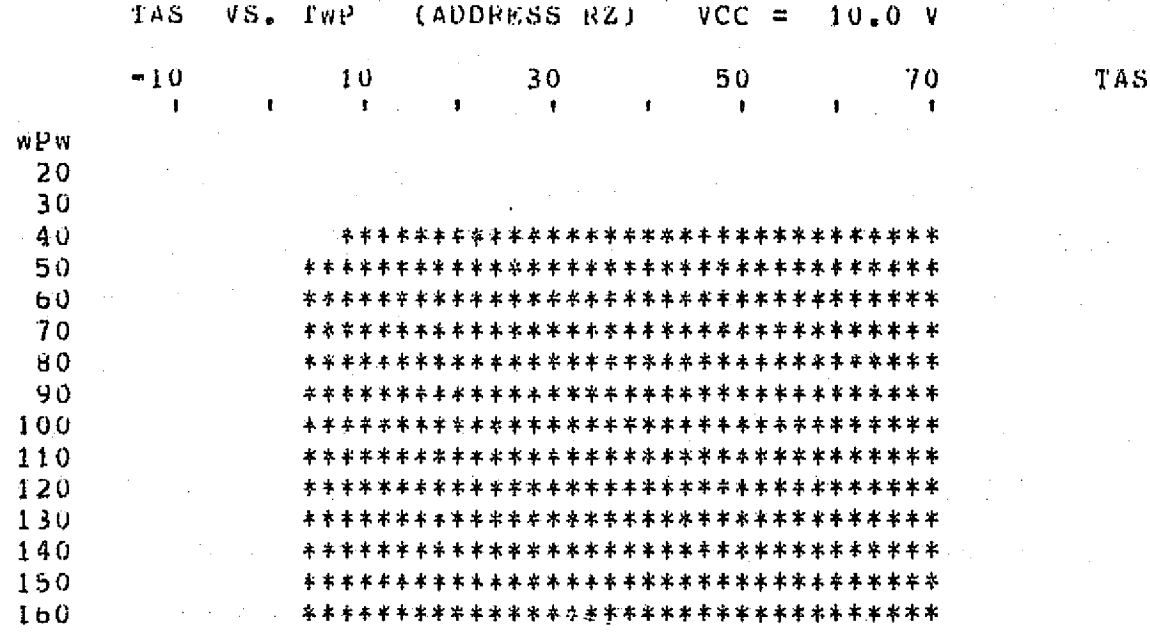


TAS VS. TWP (ADDRESS RZ) VCC = 5.00 V

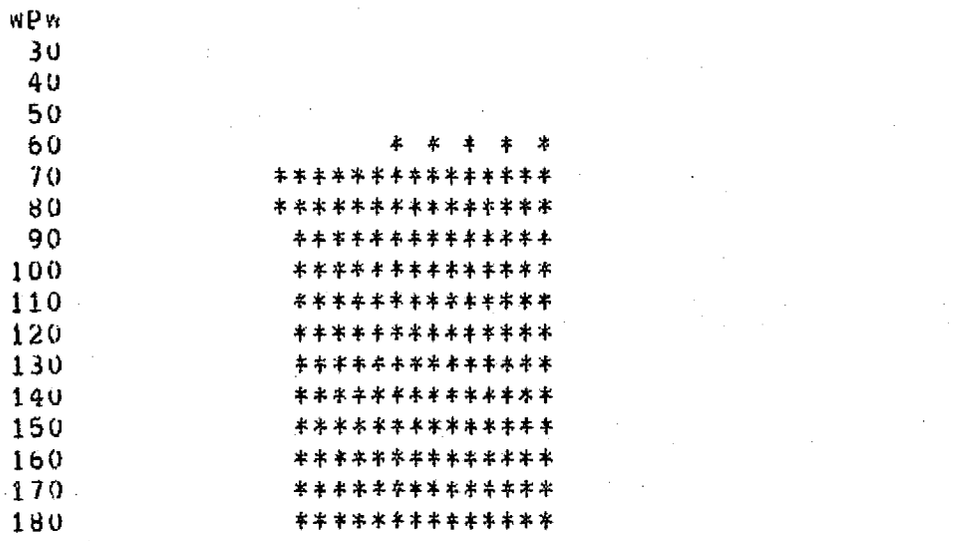


C-5

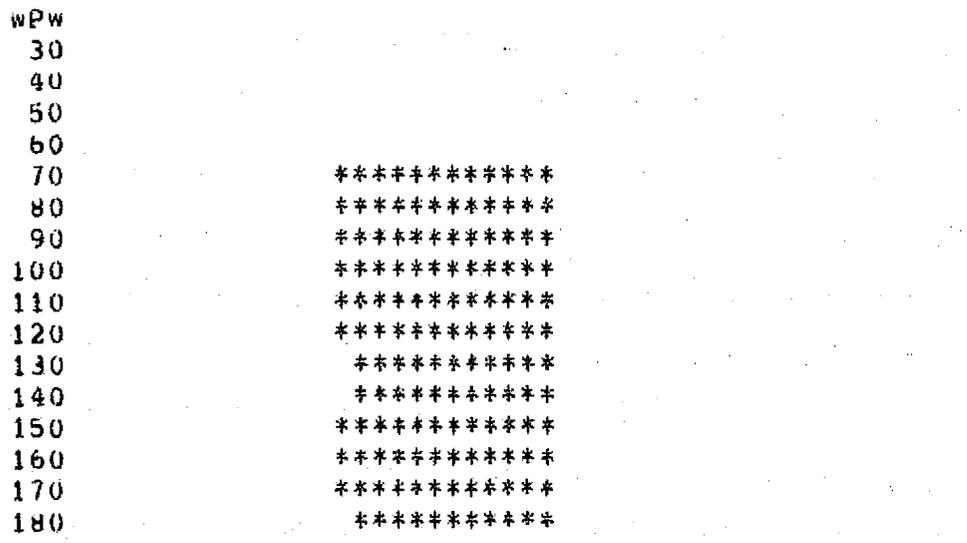

TAS VS. TWP (ADDRESS RZI) VCC = 10.0 V
-10
10
30
50
70
TAS
WPW
20
30
40
50
60
70
80
90
100
110
120
130
140
150
160


TAS VS. TWP (ADDRESS RZ) VCC = 10.0 V
-10
10
30
50
70
TAS
WPW
20
30
40
50
60
70
80
90
100
110
120
130
140
150
160

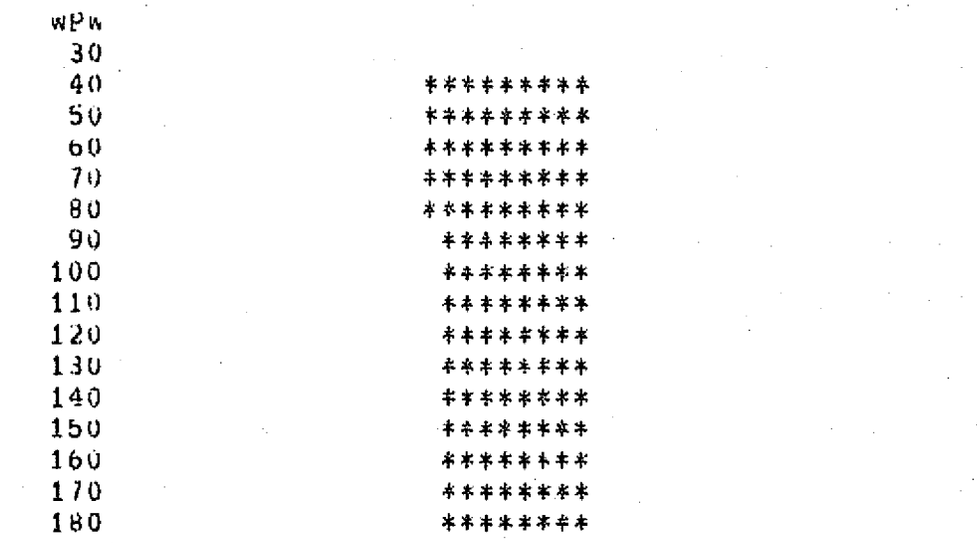
TAH VS. TWP (ADDRESS RZI) VCC = 5.00 V



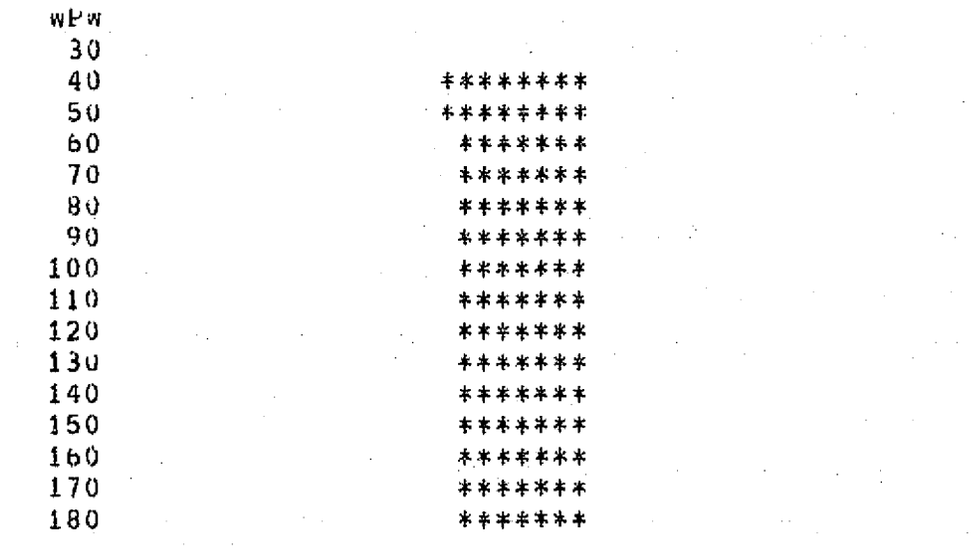
TAH VS. TWP (ADDRESS RZ) VCC = 5.00 V



TAH VS. TWP (ADDRESS RZI) VCC = 10.0 V



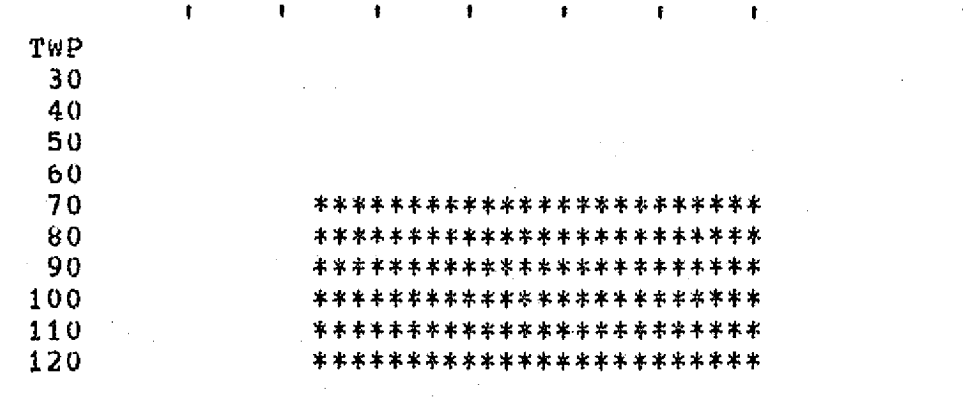
TAH VS. TWP (ADDRESS RZ) VCC = 10.0 V



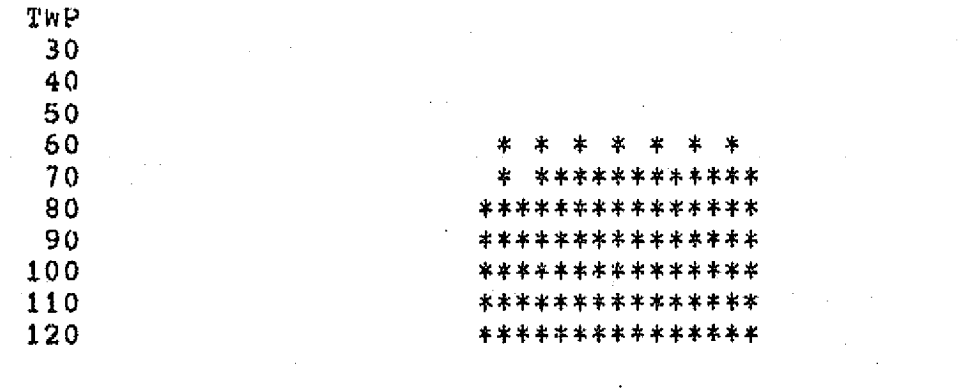
REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: -55 C SN: 3

TDS VS. TWP (DATA RZI) VCC = 5.00 V

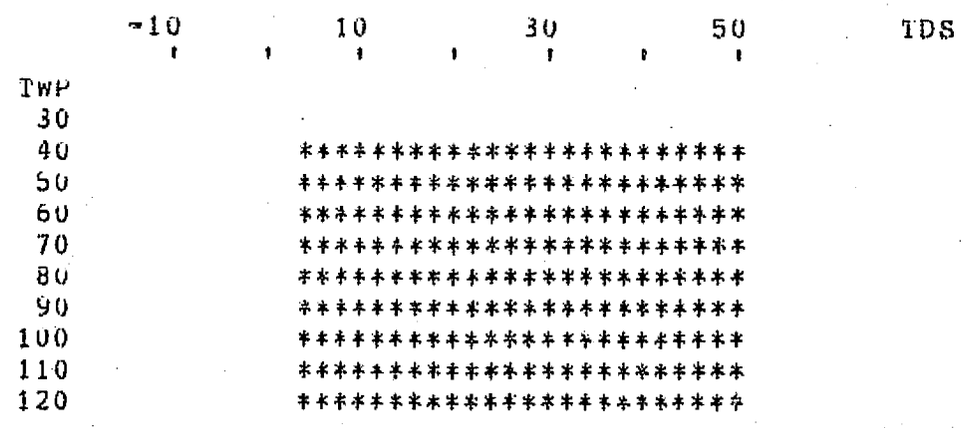


TDS VS. TWP (DATA RZ) VCC = 5.00 V

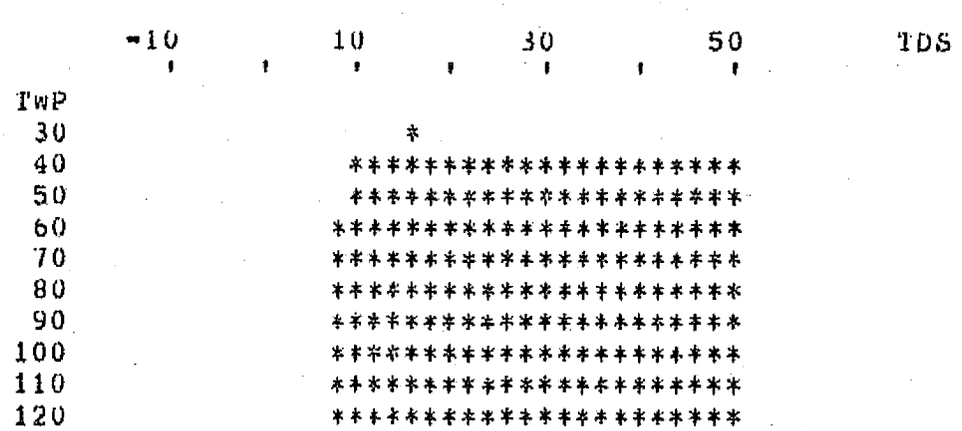


RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: -55 C SN:

TDS VS. TWP (DATA RZI) VCC = 10.0 V

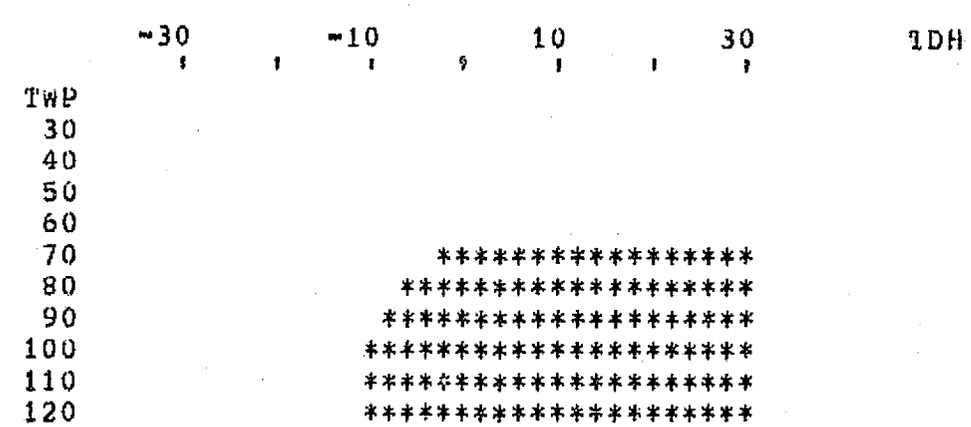


TDS VS. TWP (DATA RZ) VCC = 10.0 V

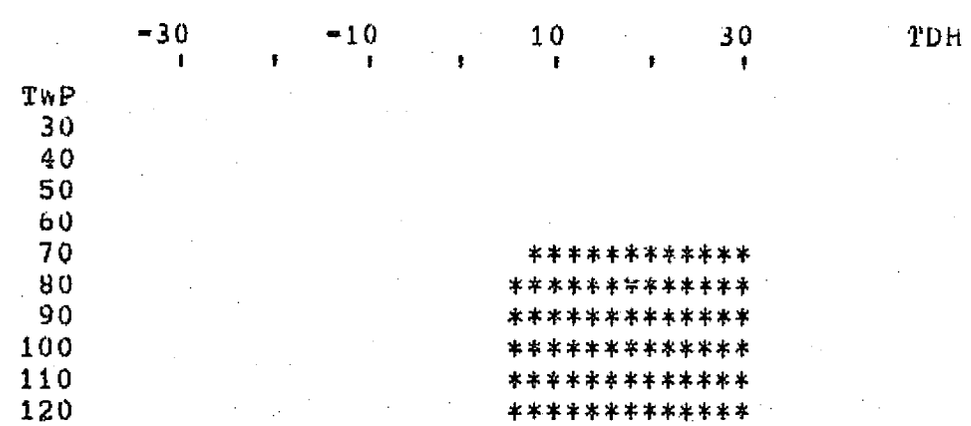


RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: -55 C SN: 3

TDH VS. TWP (DATA RZI) VCC = 5.00 V

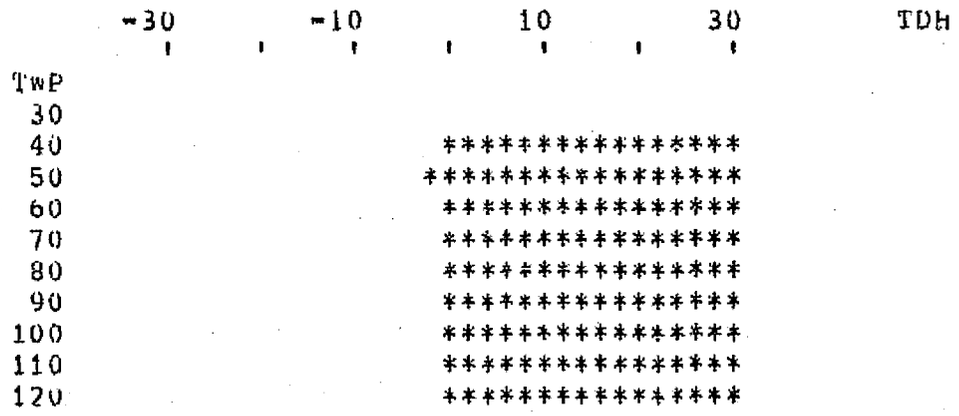


TDH VS. TWP (DATA RZ) VCC = 5.00 V

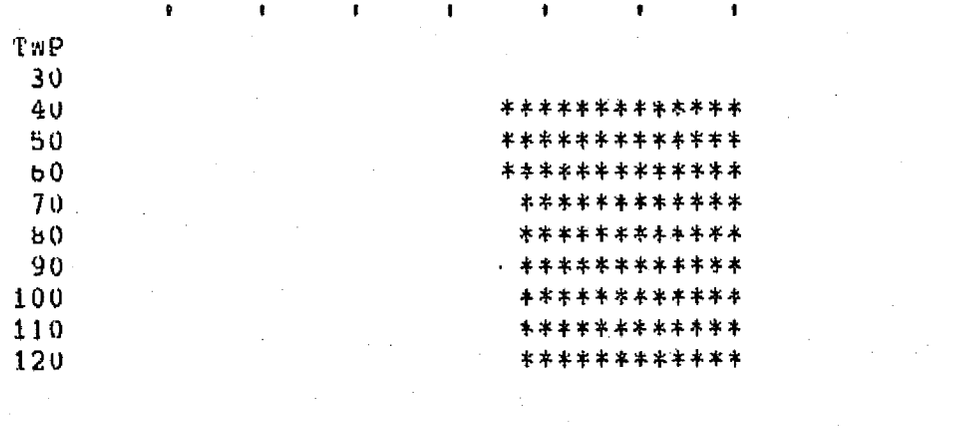


RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: -55 C SN:

TDH VS. TwP (DATA RZ1) VCC = 10.0 V



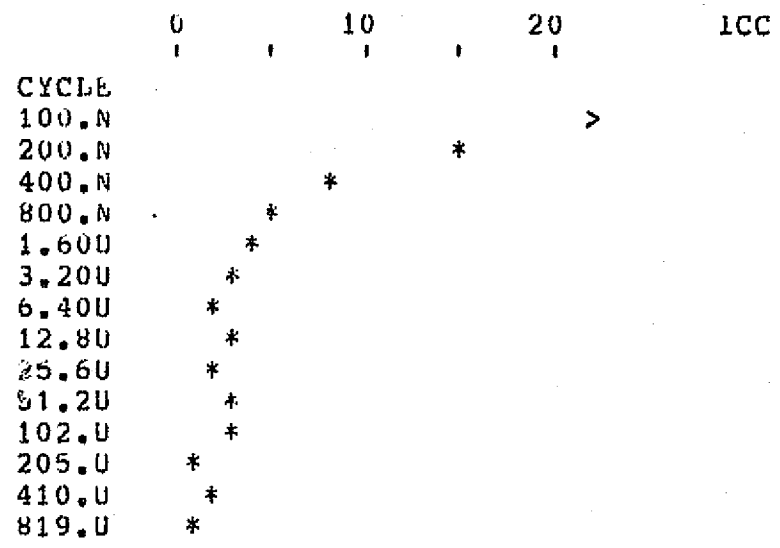
TDH VS. TwP (DATA RZ) VCC = 10.0 V



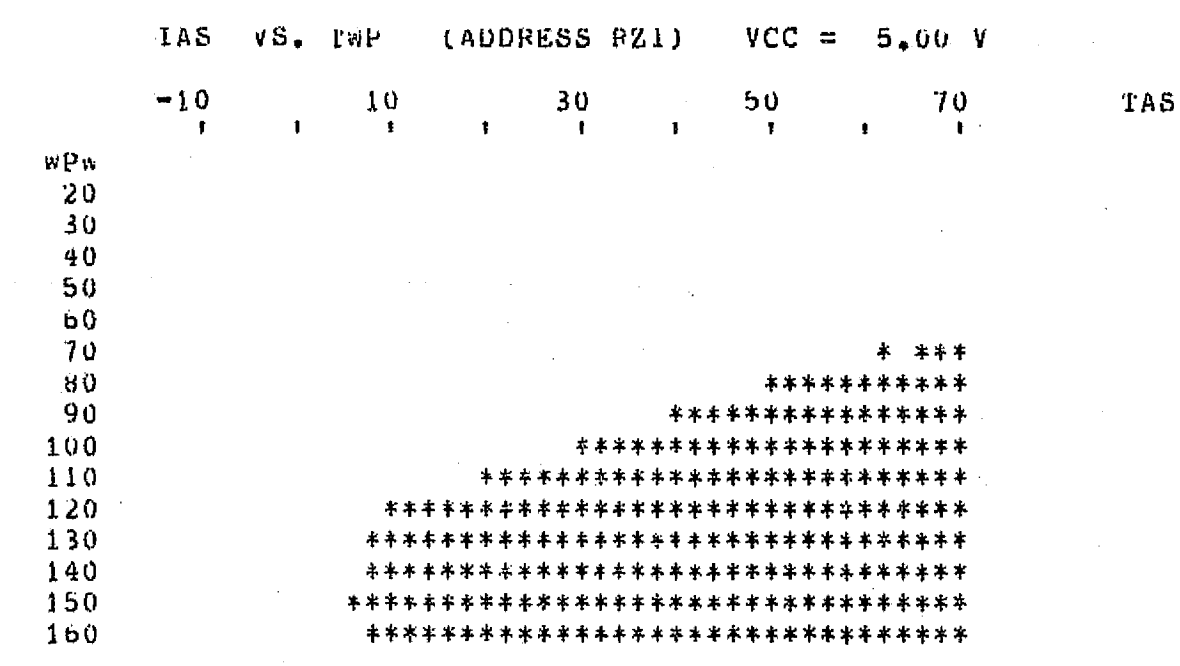
REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR.

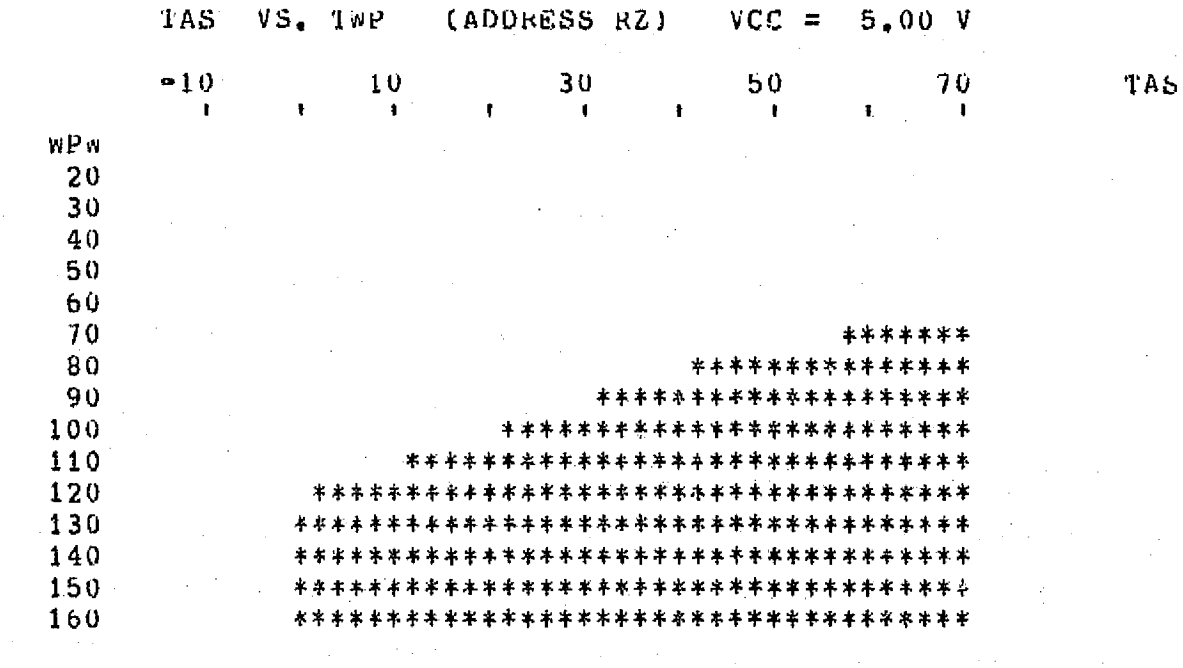
RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: -55 C. SN: 3

ICC VS. CYCLE TIME VCC = 10.0V

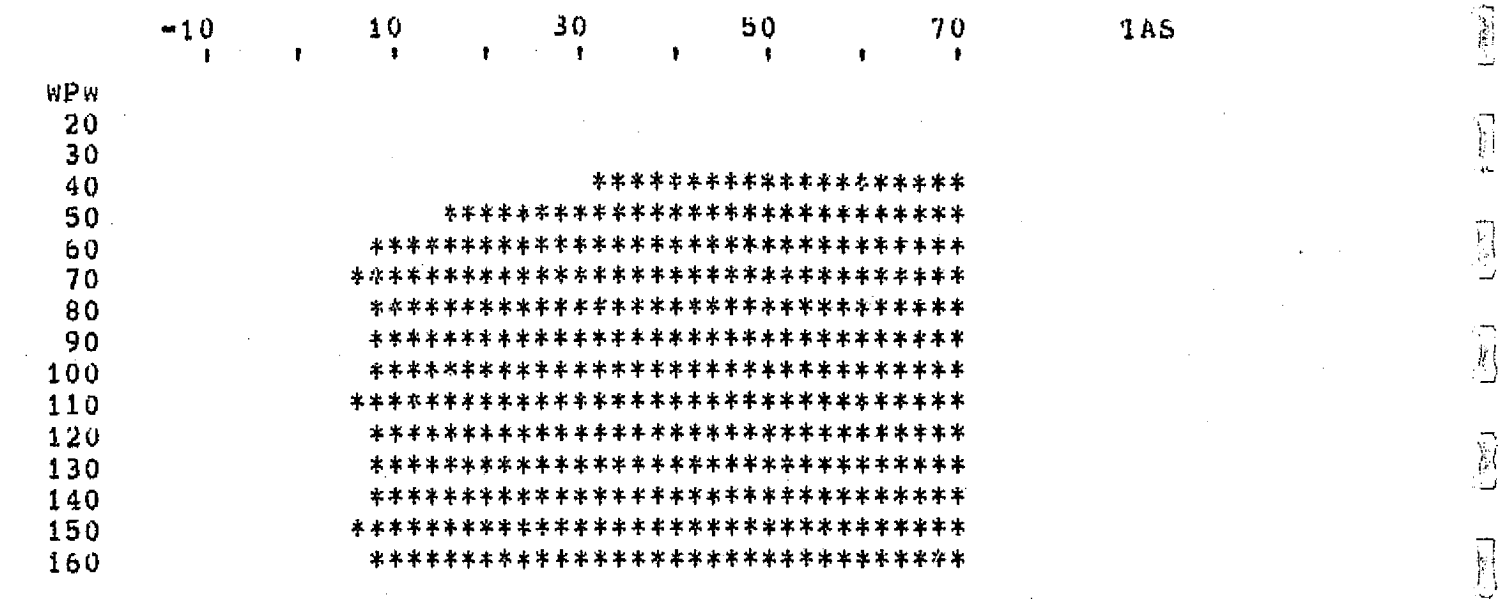


DEVICE PASSED ALL TESTS

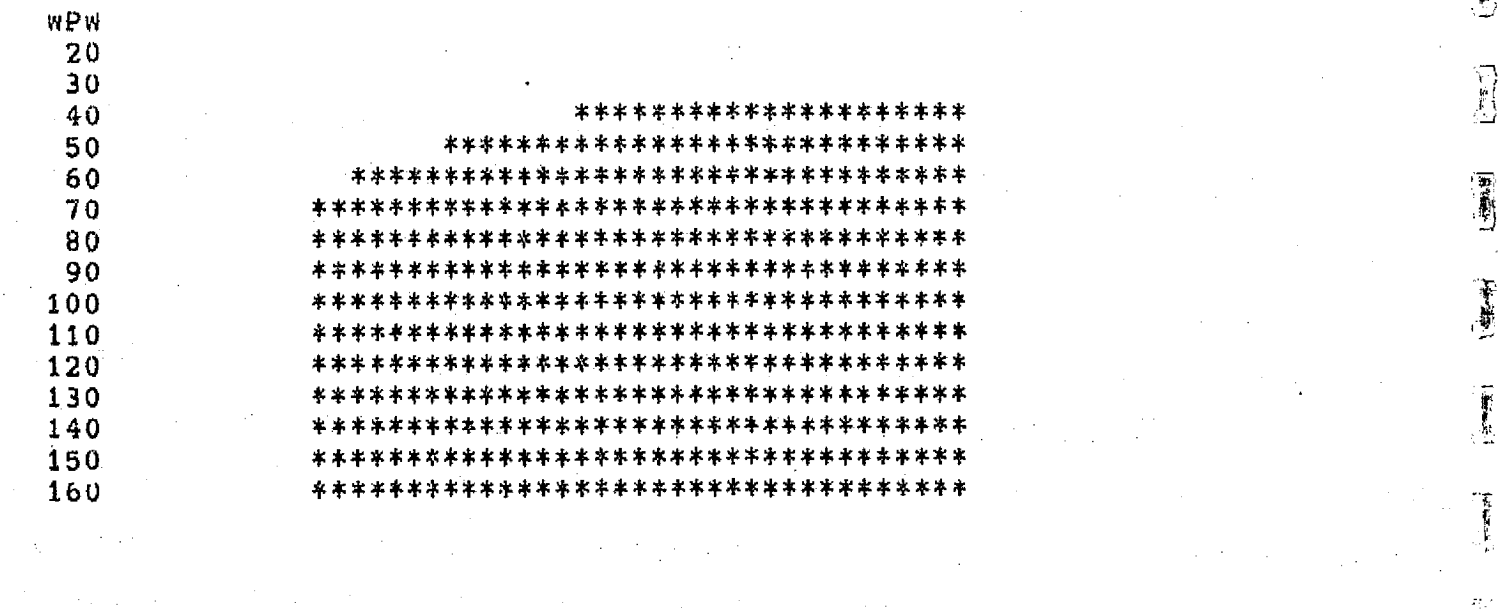

IAS VS. TWP (ADDRESS RZ1) VCC = 5.00 V
-10 10 30 50 70 TAS
WPW
20
30
40
50
60
70
80
90
100
110
120
130
140
150
160


IAS VS. TWP (ADDRESS RZ) VCC = 5.00 V
-10 10 30 50 70 TAS
WPW
20
30
40
50
60
70
80
90
100
110
120
130
140
150
160

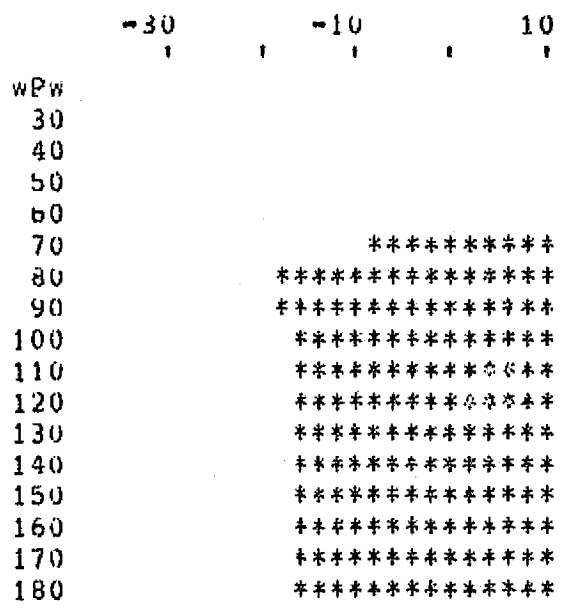
TAS VS. TWP (ADDRESS RZI) VCC = 10.0 V



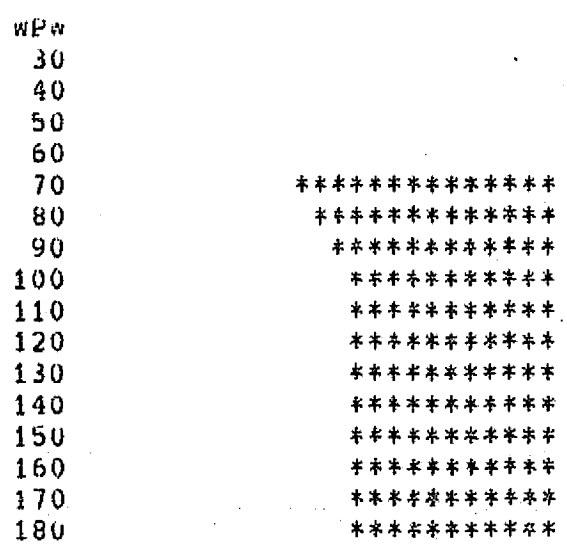
TAS VS. TWP (ADDRESS RZ) VCC = 10.0 V



TAH VS. TWP (ADDRESS RZI) VCC = 5.00 V

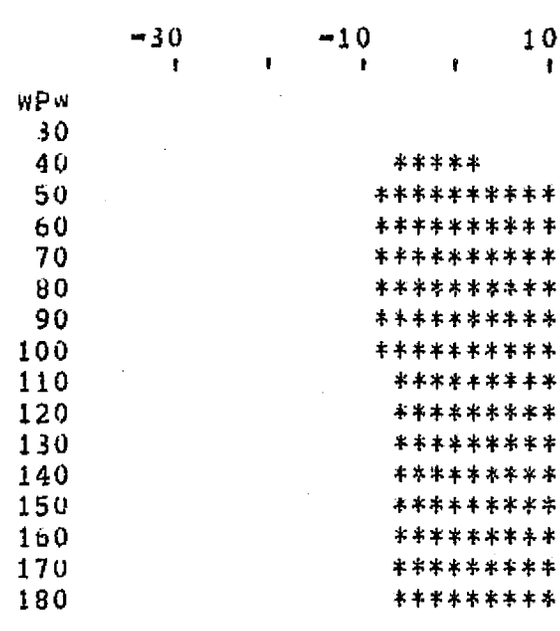


TAH VS. TWP (ADDRESS RZ) VCC = 5.00 V

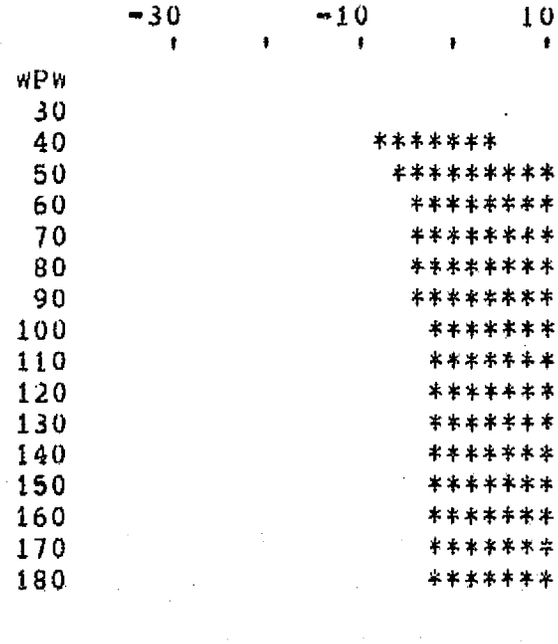


REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

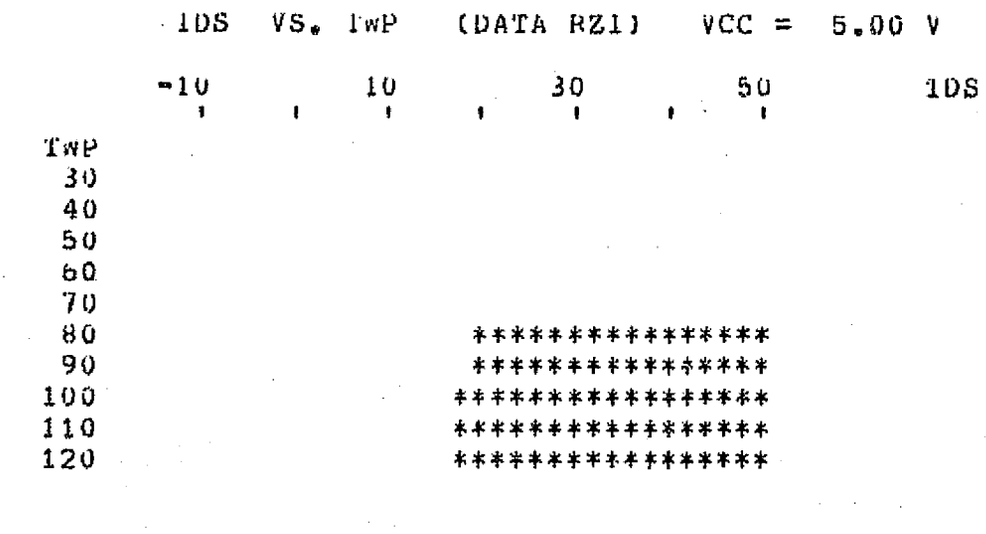
TAH VS. TWP (ADDRESS RZI) VCC = 10.0 V

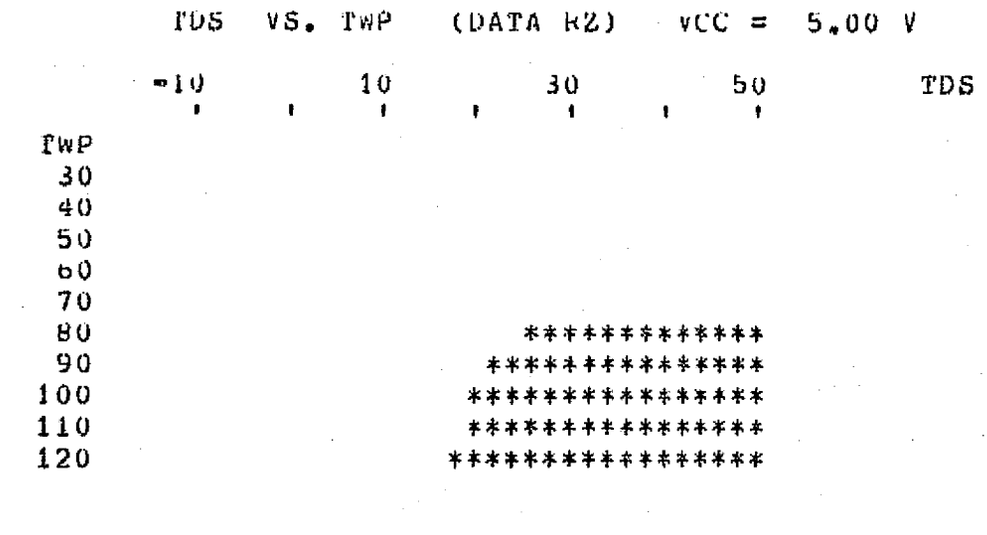


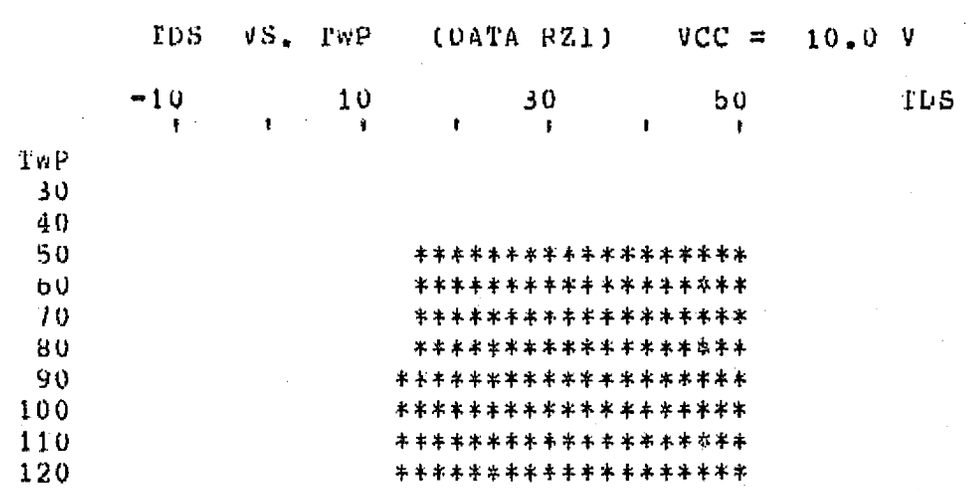
TAH VS. TWP (ADDRESS RZ) VCC = 10.0 V

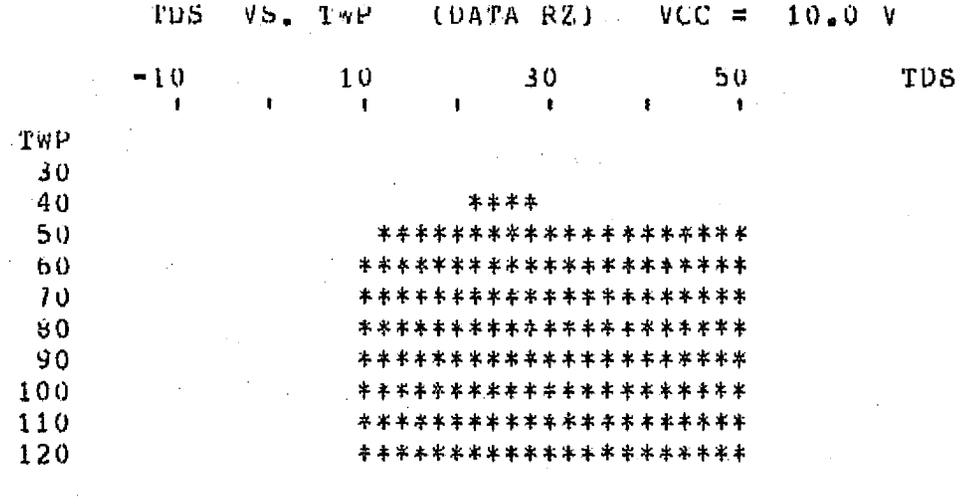


RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 125 C. SN:

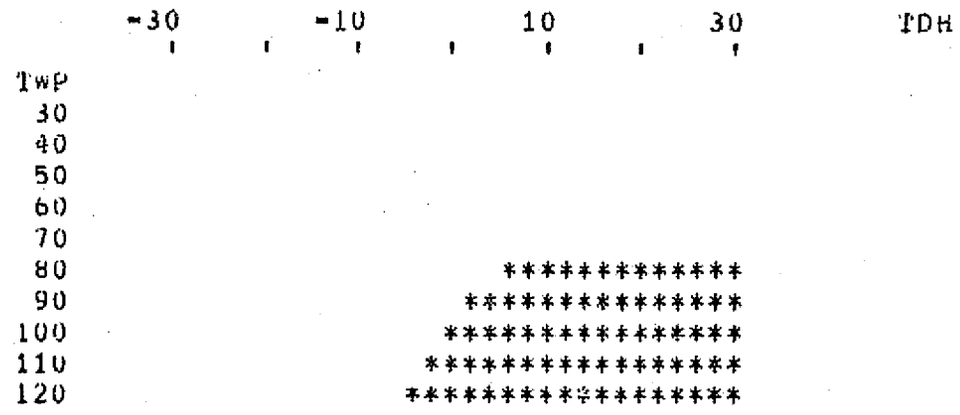




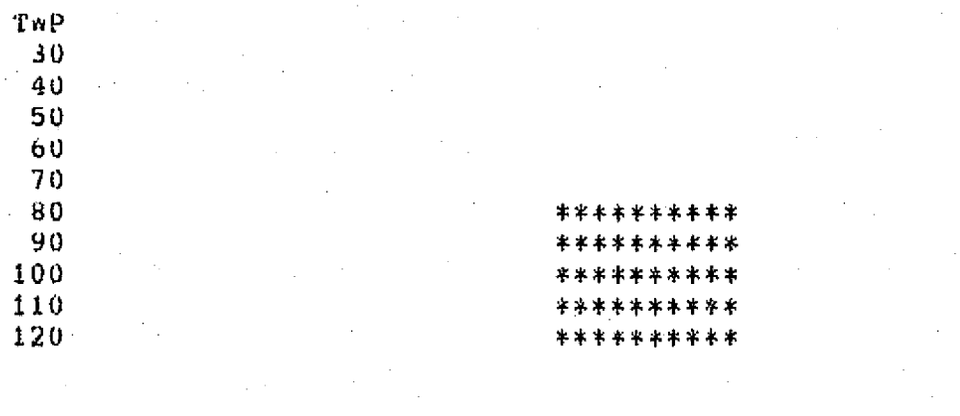

TDS VS. TWP (DATA RZ1) VCC = 10.0 V
-10
10
30
50
TDS
TWP
30
40
50
60
70
80
90
100
110
120


TDS VS. TWP (DATA RZ) VCC = 10.0 V
-10
10
30
50
TDS
TWP
30
40
50
60
70
80
90
100
110
120

TDH Vs. TWP (DATA RZ1) VCC = 5.00 V



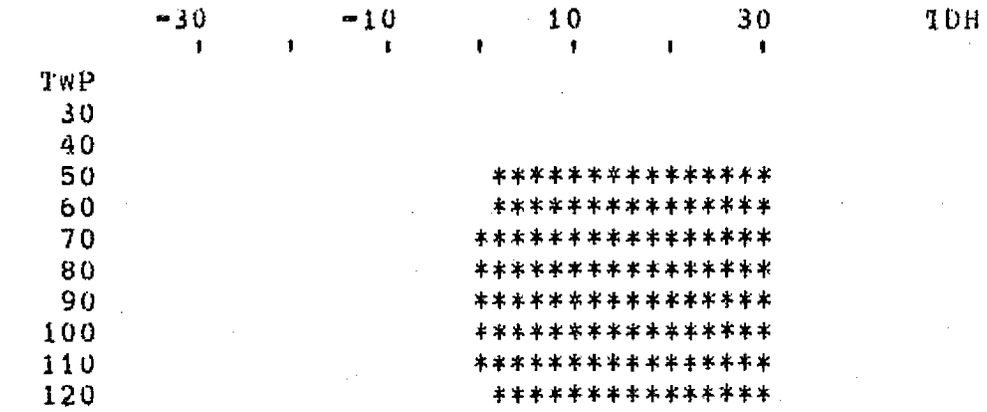
TDH Vs. TWP (DATA RZ) VCC = 5.00 V



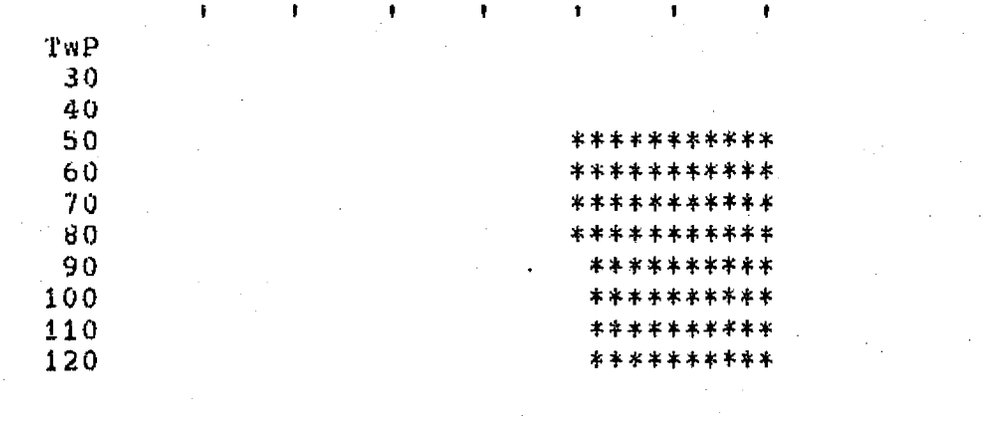
REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR.

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 125 C SN: 3

TDH VS. TWP (DATA RZ1) VCC = 10.0 V



TDH VS. TWP (DATA RZ) VCC = 10.0 V



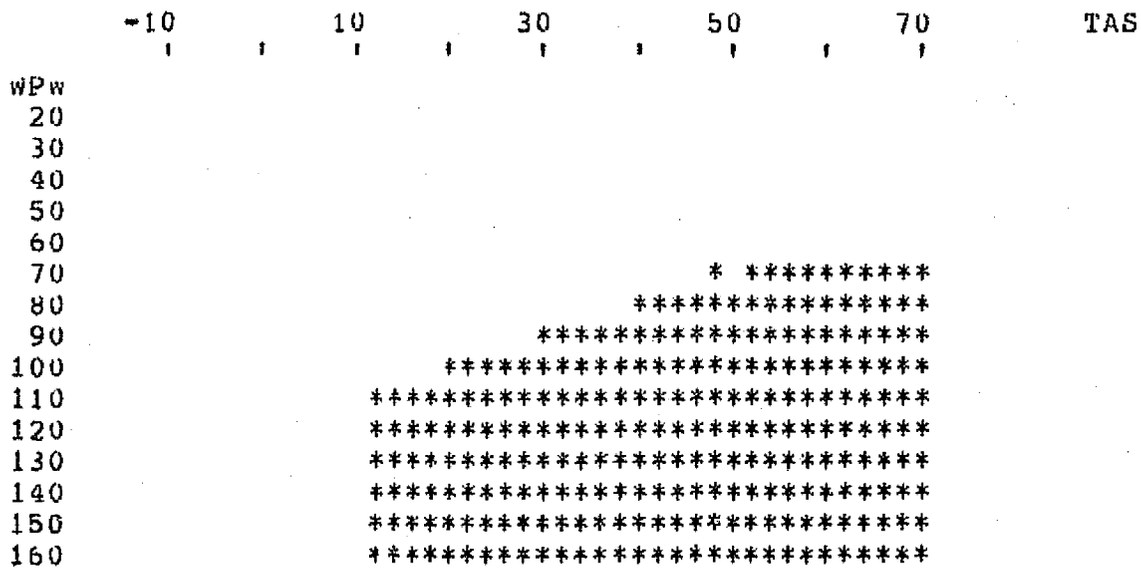
RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 125 C SN:

ICC VS. CYCLE TIME VCC = 10.0V

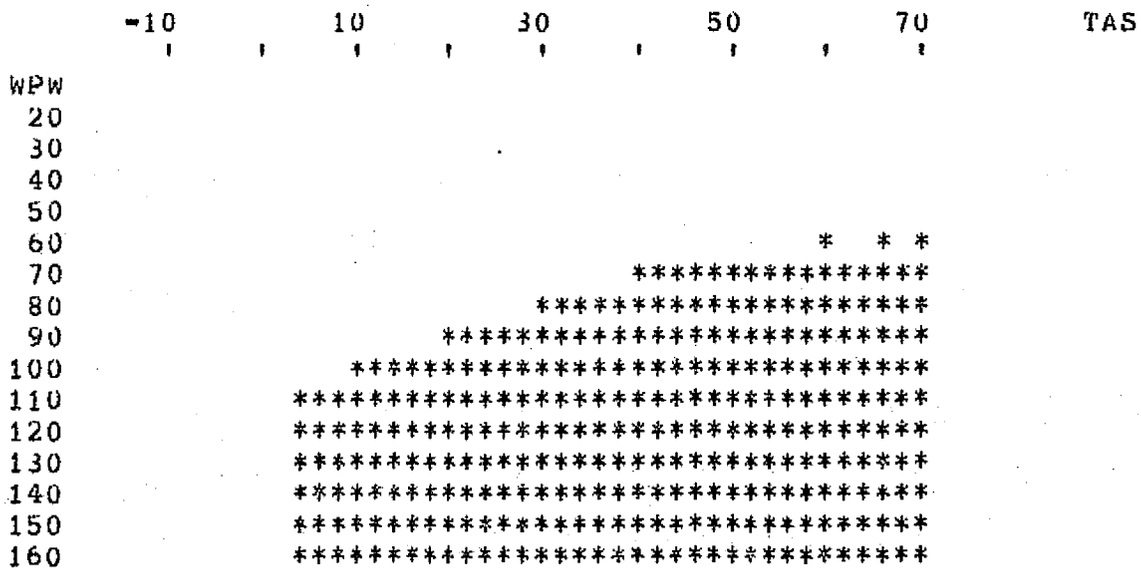
```
                0         10        20        ICC
                '    '    '    '    '
CYCLE
100.N                               >
200.N                         *
400.N                    *
800.N               *
1.600U             *
3.200U           *
6.400U         *
12.80U         *
25.60U       *
51.20U       *
102.0U       *
205.0U     *
410.0U     *
819.0U     *
```

DEVICE PASSED ALL TESTS

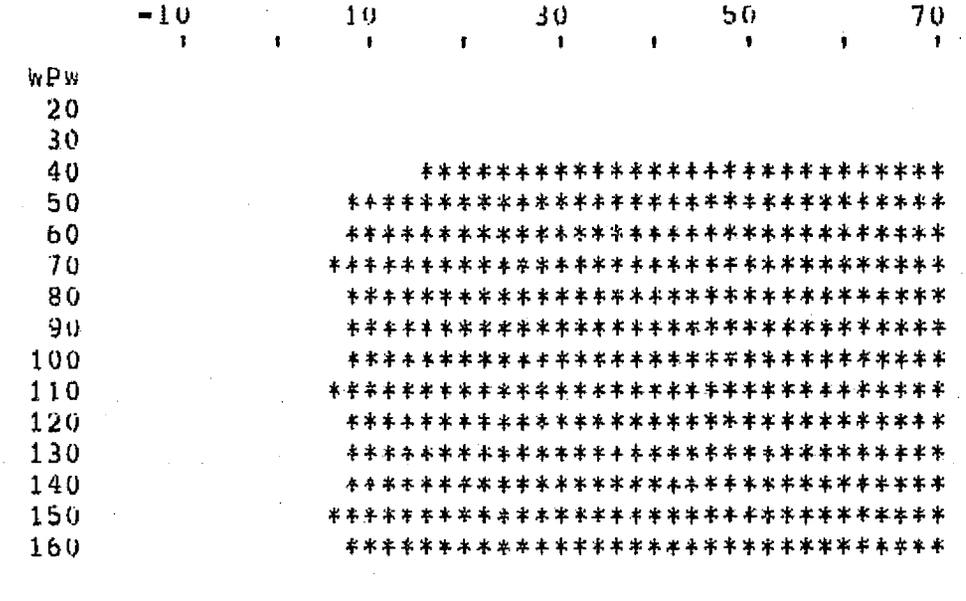
TAS VS. TWP (ADDRESS RZI) VCC = 5.00 V



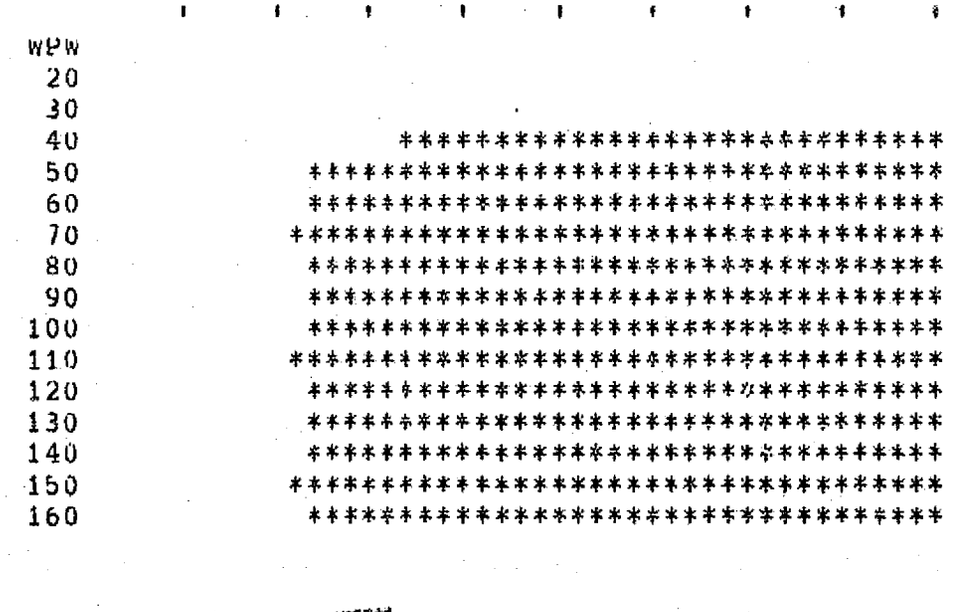
TAS VS. TWP (ADDRESS RZ) VCC = 5.00 V



TAS VS. TWP (ADDRESS RZ1) VCC = 10.0 V



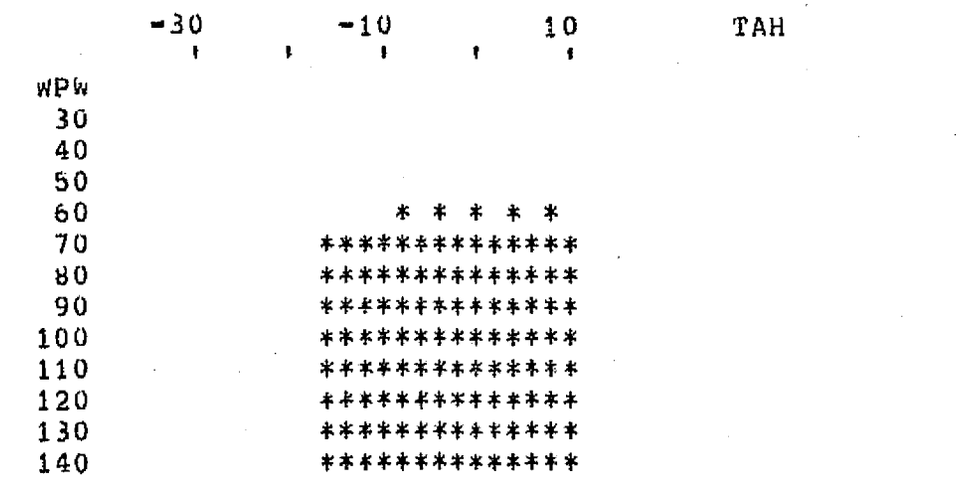
TAS VS. TWP (ADDRESS RZ) VCC = 10.0 V



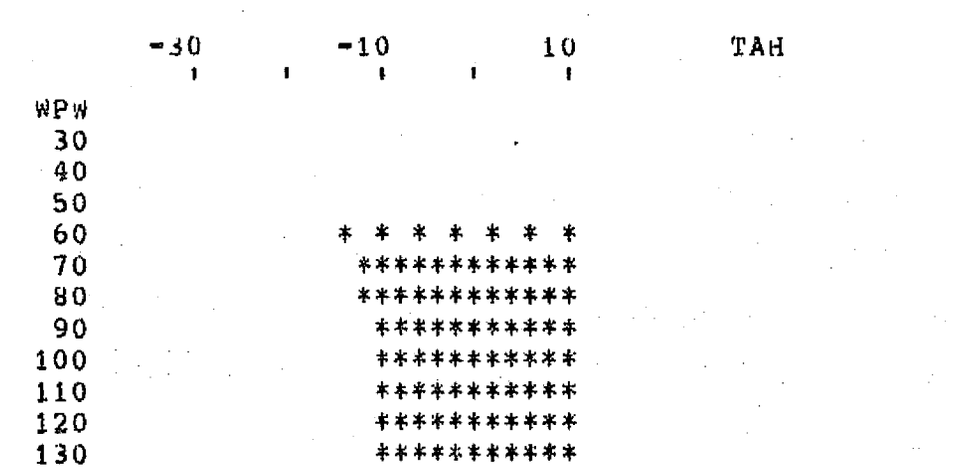
REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 25 C SN: 4

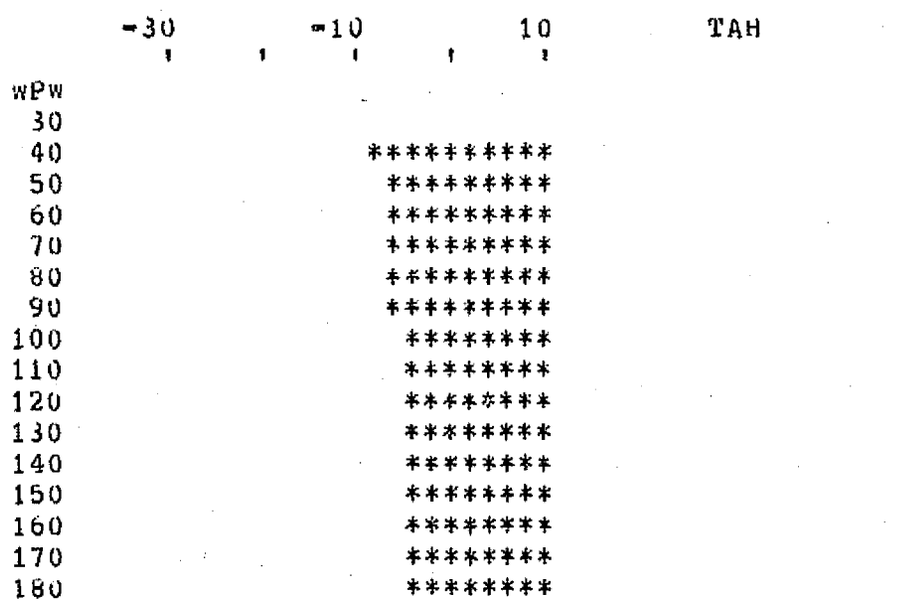
TAH VS. TwP (ADDRESS RZI) VCC = 5.00 V



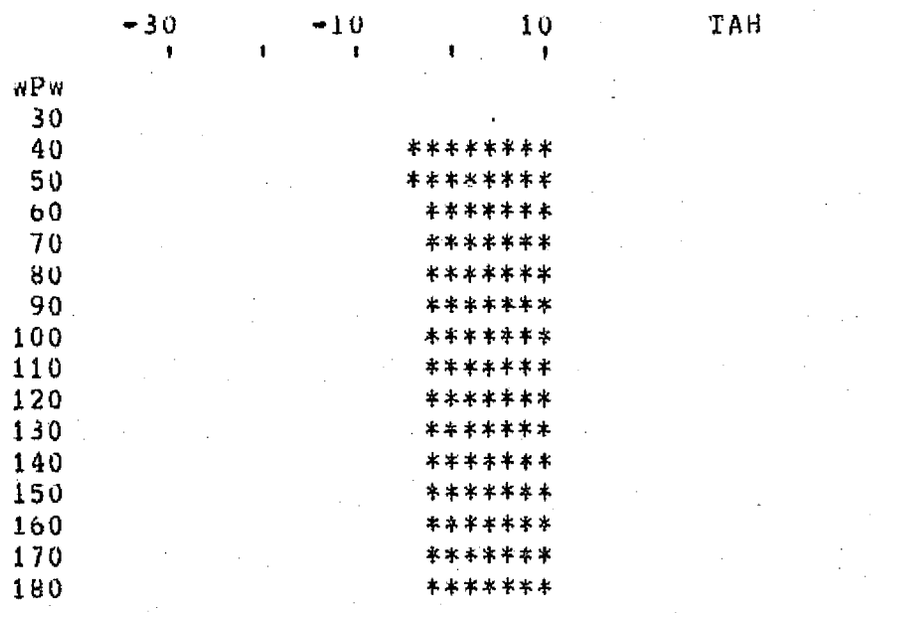
TAH VS. TwP (ADDRESS RZ) VCC = 5.00 V



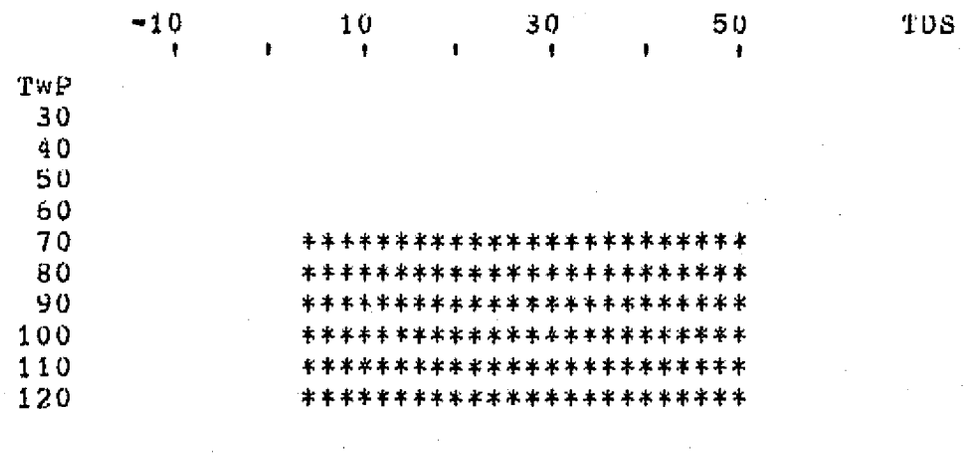
TAH VS. TWP (ADDRESS RZI) VCC = 10.0 V



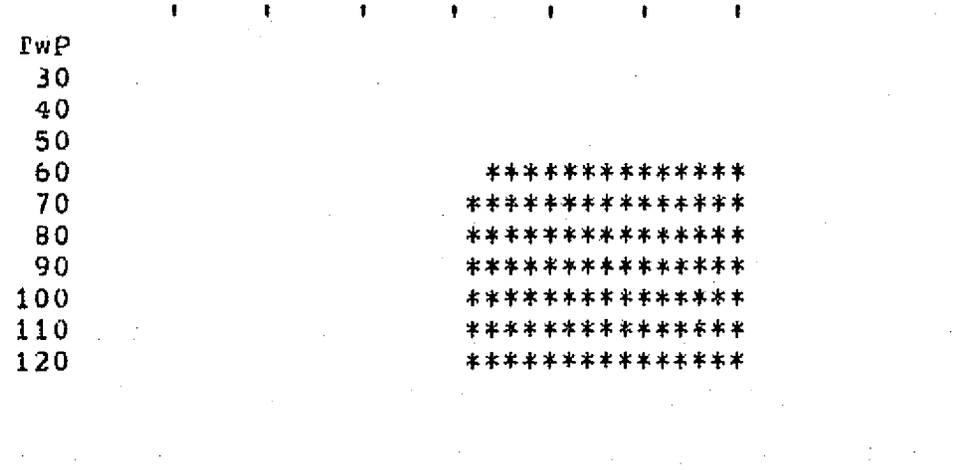
TAH VS. TWP (ADDRESS RZ) VCC = 10.0 V



TDS VS. TWP (DATA RZI) VCC = 5.00 V

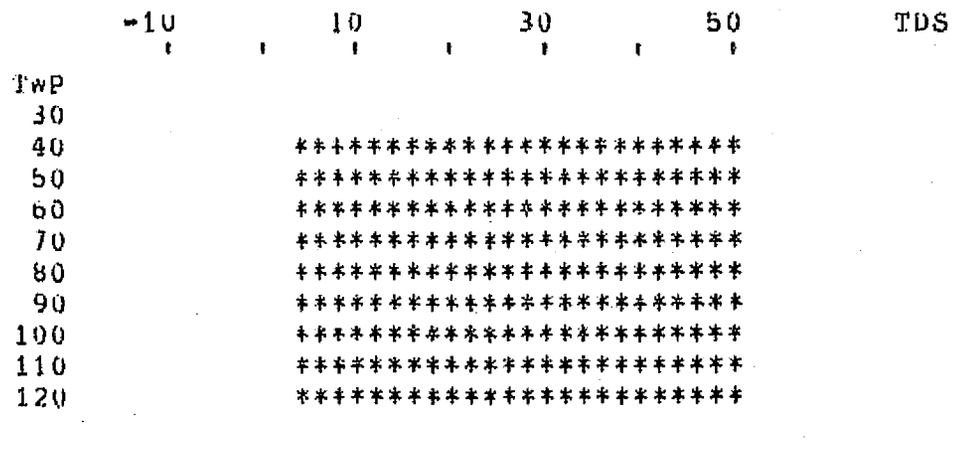


TDS VS. TWP (DATA RZ) VCC = 5.00 V

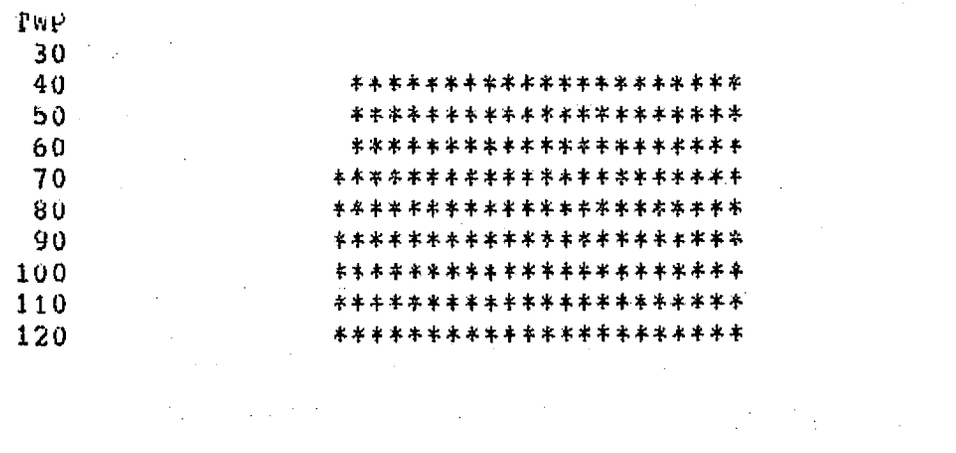


RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 25 C SN:

TDS VS. TwP (DATA RZI) VCC = 10.0 V



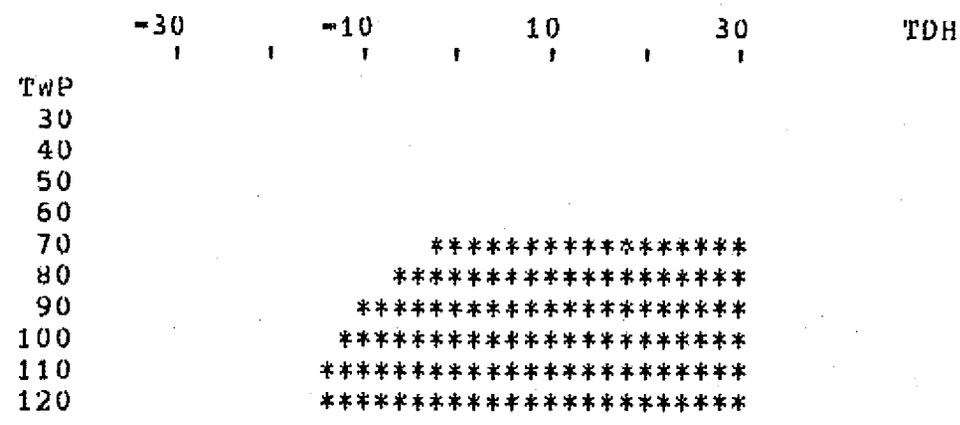
TDS Vs. TwP (DATA RZ) VCC = 10.0 V



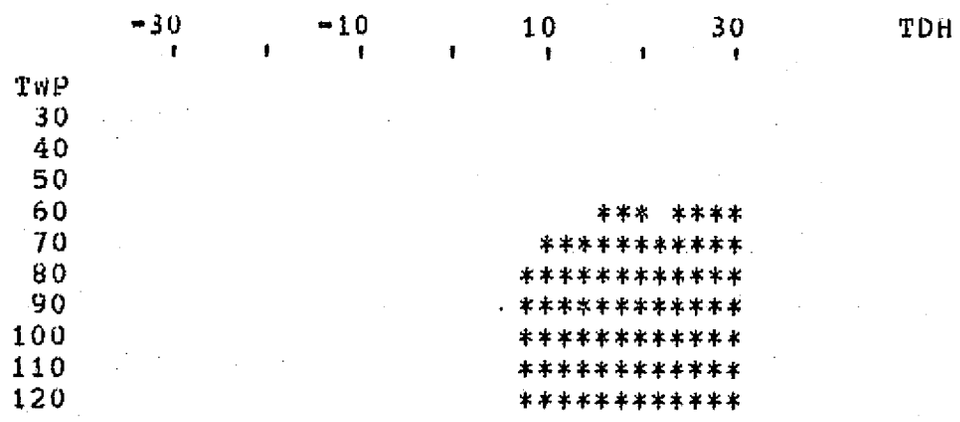
REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 25 C SN: 4

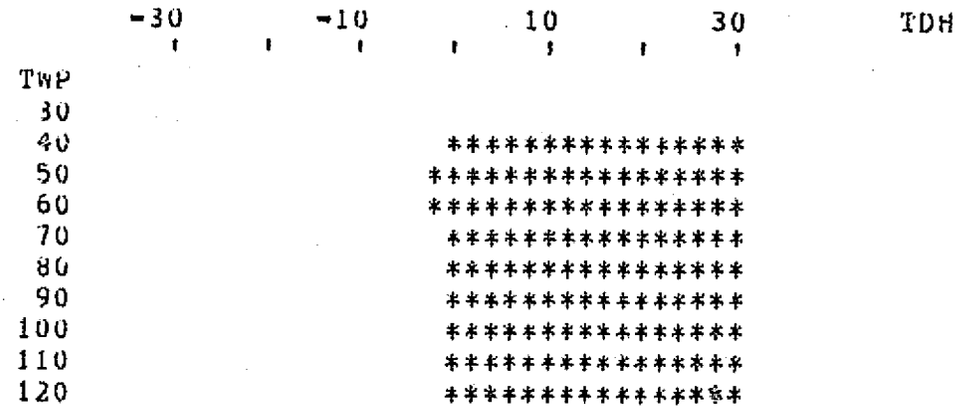
TDH VS. TWP (DATA RZI) VCC = 5.00 V



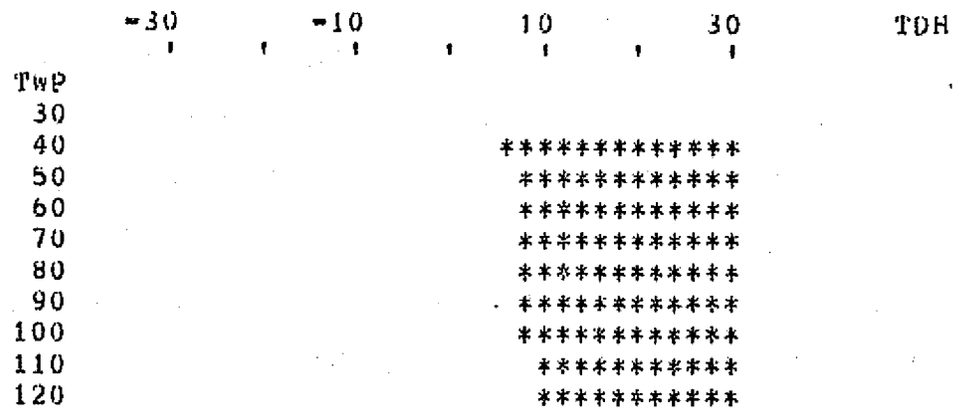
TDH VS. TWP (DATA RZ) VCC = 5.00 V



TDH VS. TWP (DATA RZI) VCC = 10.0 V



TDH VS. TWP (DATA RZ) VCC = 10.0 V



RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 25 C SN: 4

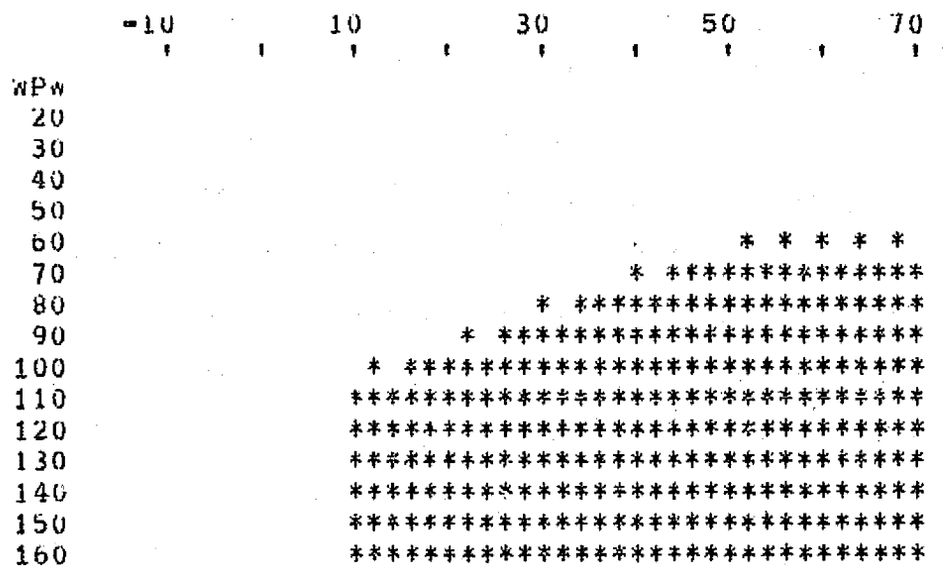
ICC VS. CYCLE TIME VCC = 10.0V

```
          0         10        20        ICC
          '    '    '    '    '
  CYCLE
  100.N                        >
  200.N                  *
  400.N             *
  800.N          *
  1.60U         *
  3.20U       *
  6.40U      *
  12.8U      *
  25.6U      *
  51.2U       *
  102.U    *
  205.U     *
  410.U     *
  819.U     *
```

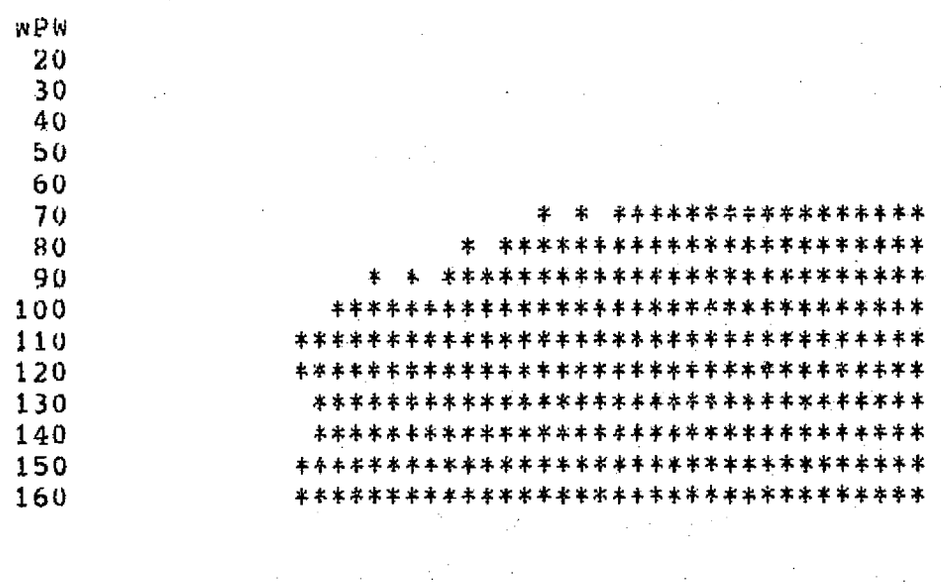
DEVICE PASSED ALL TESTS

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: -55 C SN:

TAS VS. TWP (ADDRESS RZI) VCC = 5.00 V

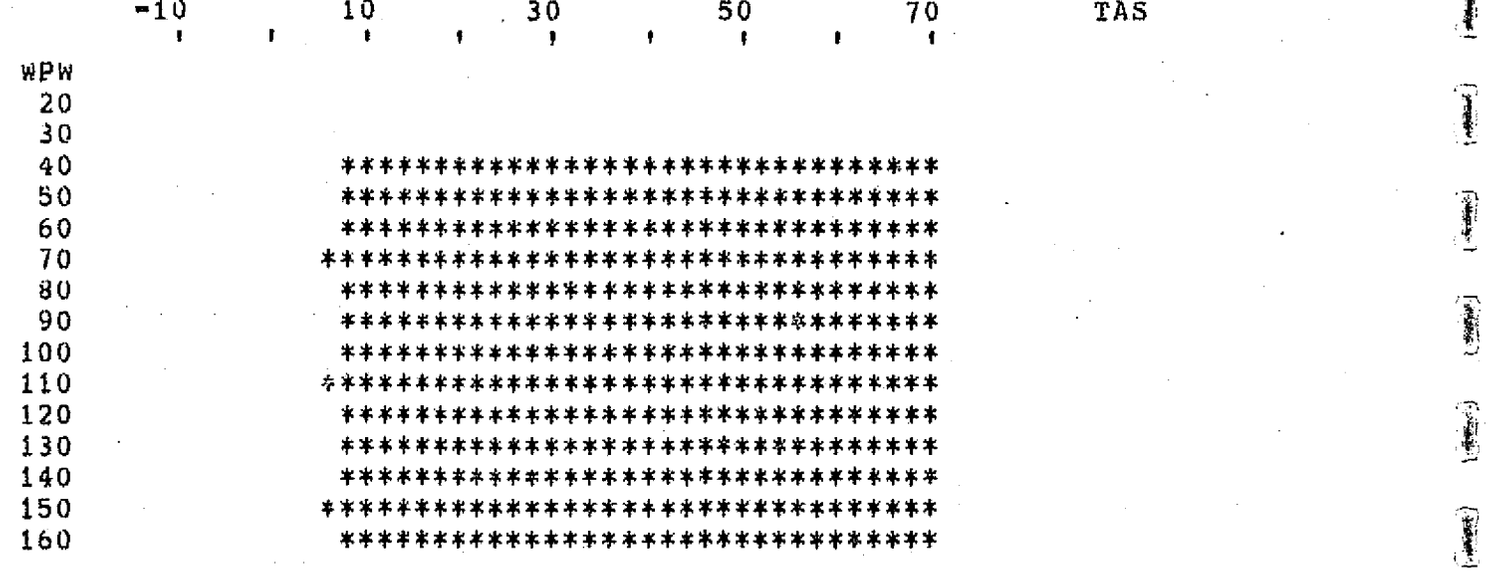


TAS VS. TWP (ADDRESS RZ) VCC = 5.00 V

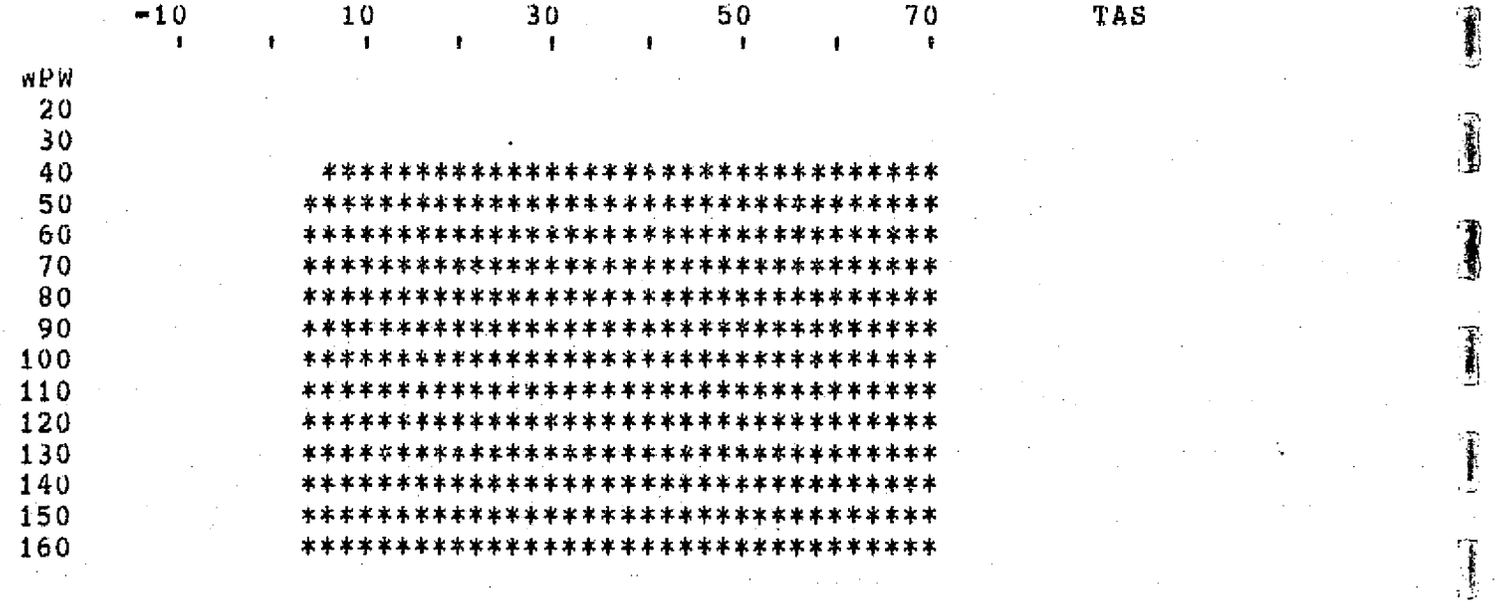


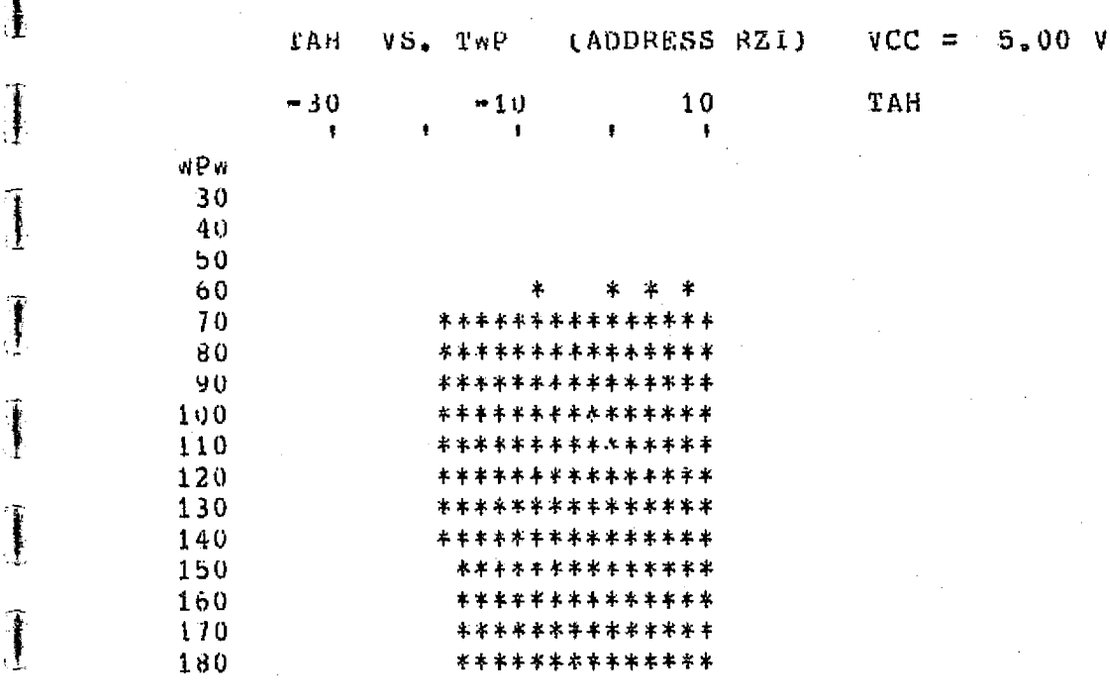
REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

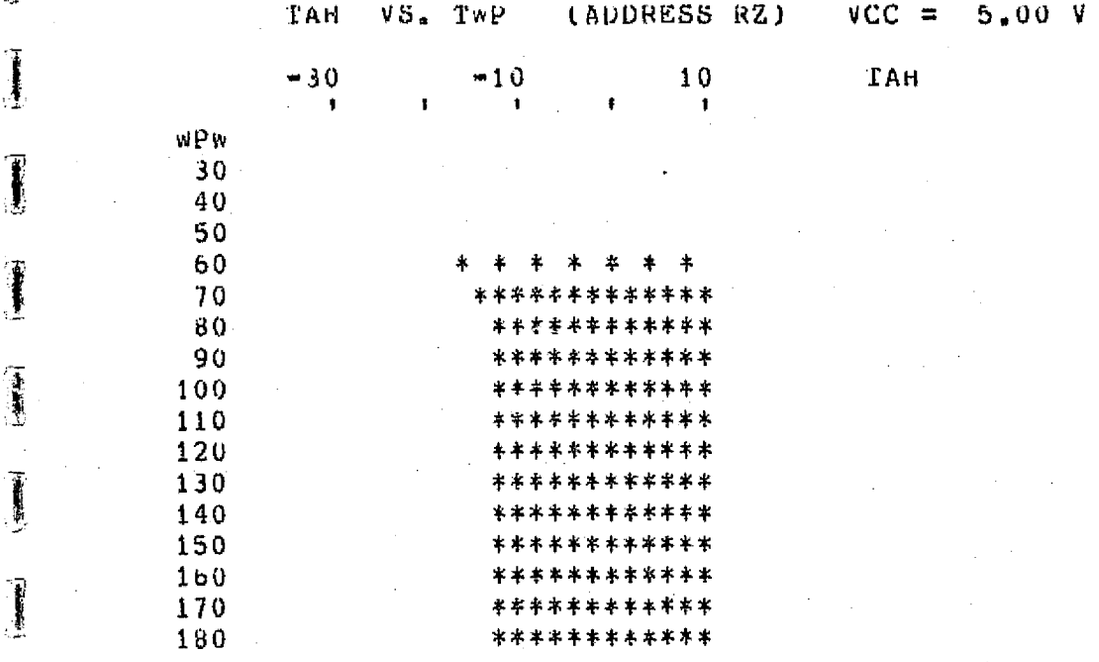
TAS VS. TWP (ADDRESS RZI) VCC = 10.0 V



TAS VS. TWP (ADDRESS RZ) VCC = 10.0 V




TAH VS. TwP (ADDRESS RZI) VCC = 5.00 V
-30
-10
10
TAH
WPw
30
40
50
60
70
80
90
100
110
120
130
140
150
160
170
180


TAH VS. TwP (ADDRESS RZ) VCC = 5.00 V
-30
-10
10
TAH
WPw
30
40
50
60
70
80
90
100
110
120
130
140
150
160
170
180

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: -55 C SN: 4

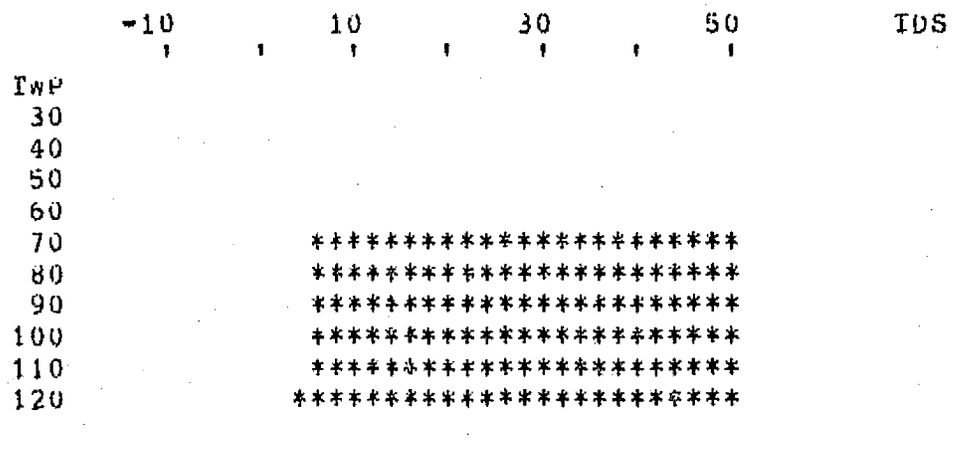
TAH VS. TWP (ADDRESS RZI) VCC = 10.0 V

```
        -30        -10         10        TAH
          '    '     '     '     '
WPW
 30                  *
 40                *********
 50                *********
 60                 ********
 70                 ********
 80                 ********
 90                 ********
100                 ********
110                 ********
120                 ********
130                 ********
140                 ********
150                 ********
160                 ********
170                 ********
180                 ********
```

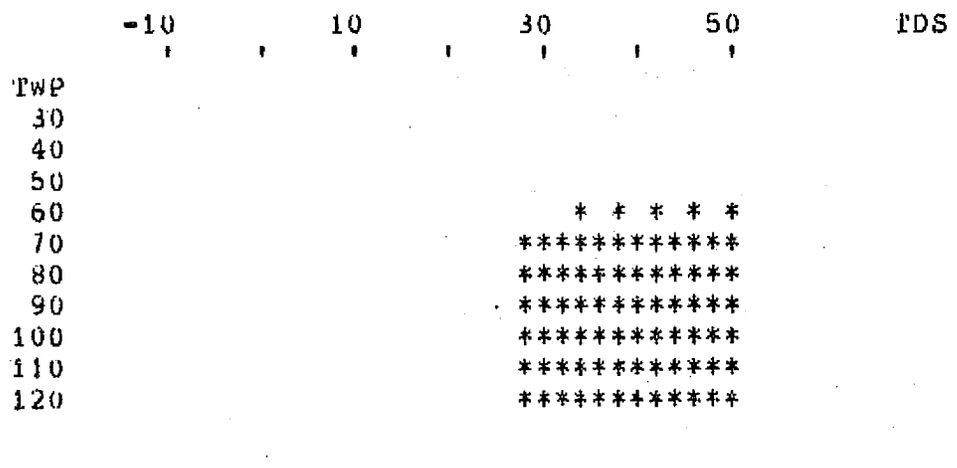
TAH VS. TWP (ADDRESS RZ) VCC = 10.0 V

```
        -30        -10         10        TAH
          '    '     '     '     '
WPW
 30                * *    .
 40                 ********
 50                  *******
 60                  *******
 70                  *******
 80                  *******
 90                  *******
100                  *******
110                  *******
120                  *******
130                  *******
140                  *******
150                  *******
160                  *******
170                  *******
180                  *******
```

TDS VS. TWP (DATA RZI) VCC = 5.00 V

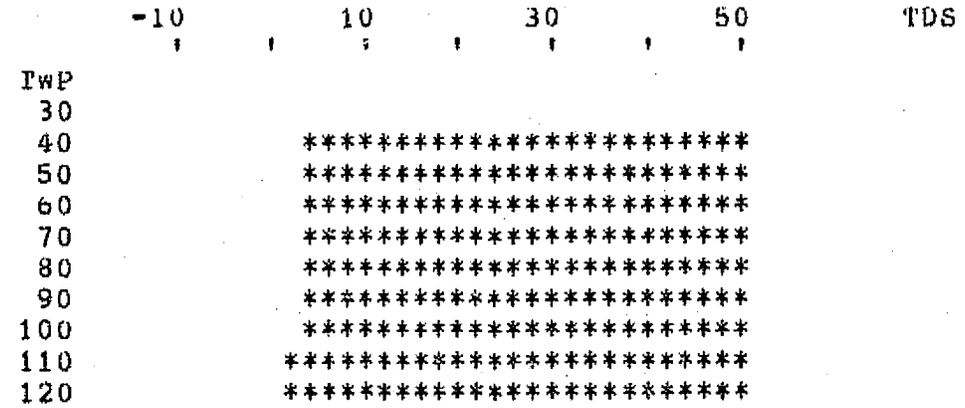


TDS VS. TWP (DATA RZ) VCC = 5.00 V

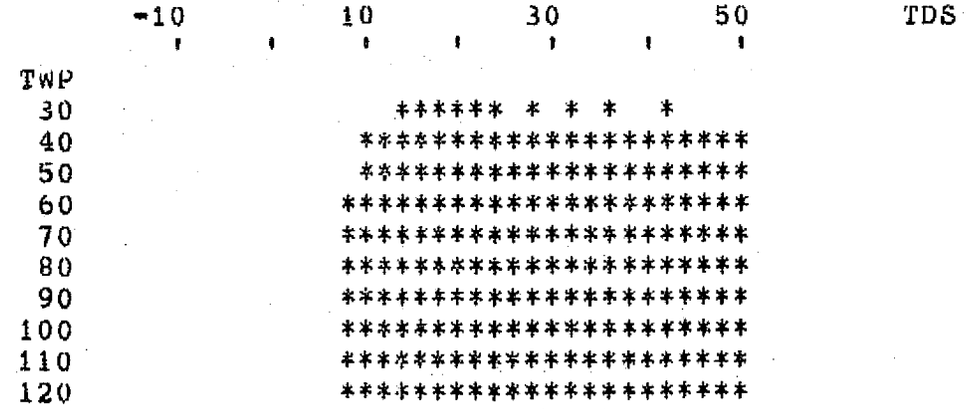


REPRODUCIBILITY OF THE
ORIGINAL PAGE IS P.

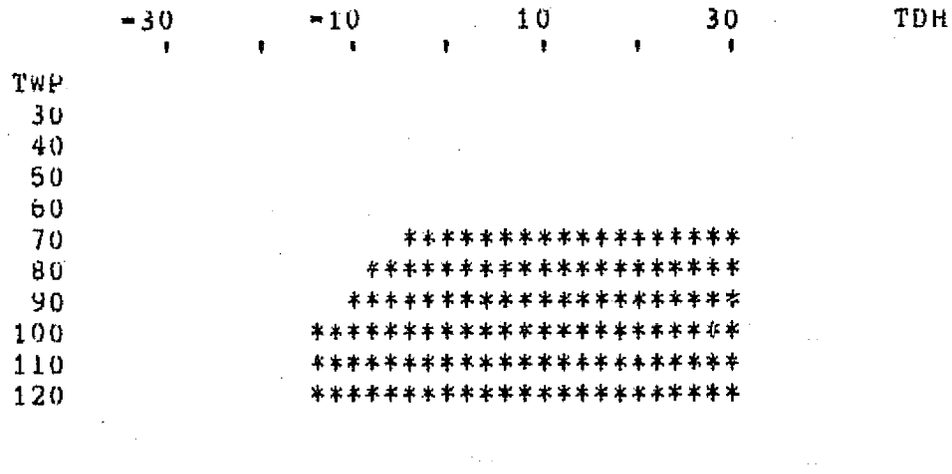
TDS VS. TWP (DATA RZI) VCC = 10.0 V



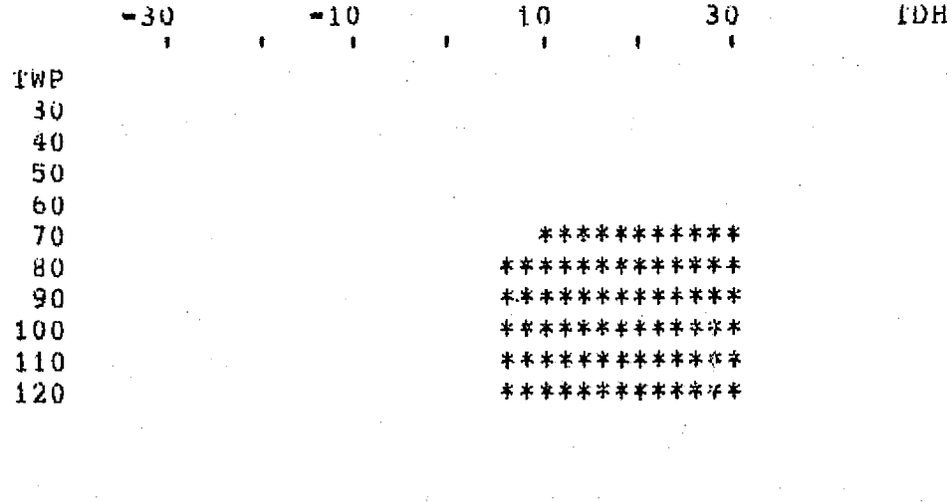
TDS VS. TWP (DATA RZ) VCC = 10.0 V



TDH VS. TWP (DATA RZI) VCC = 5.00 V



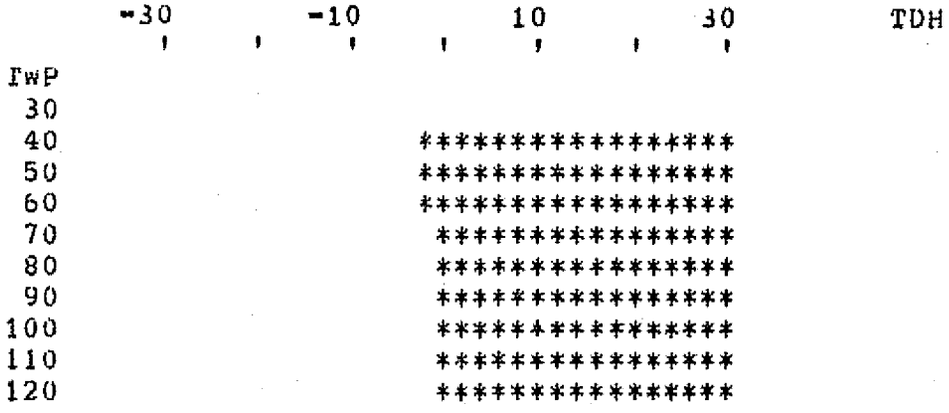
TDH VS. TWP (DATA RZ) VCC = 5.00 V



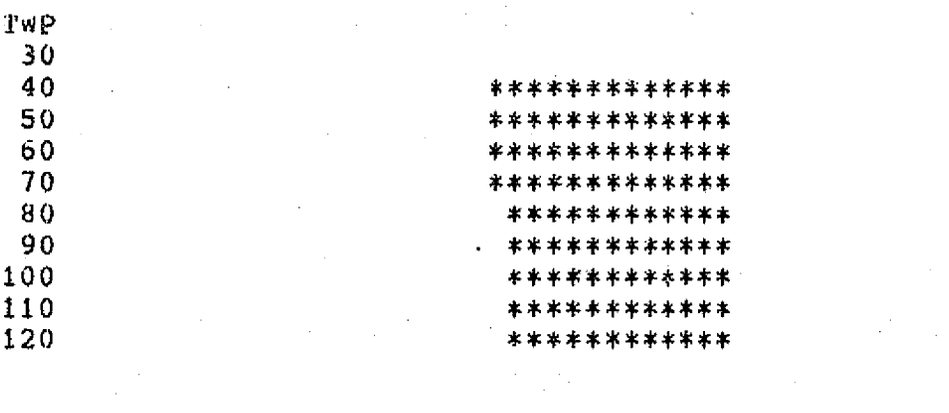
REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: -55 C SN: 4

TDH VS. TWP (DATA RZI) VCC = 10.0 V

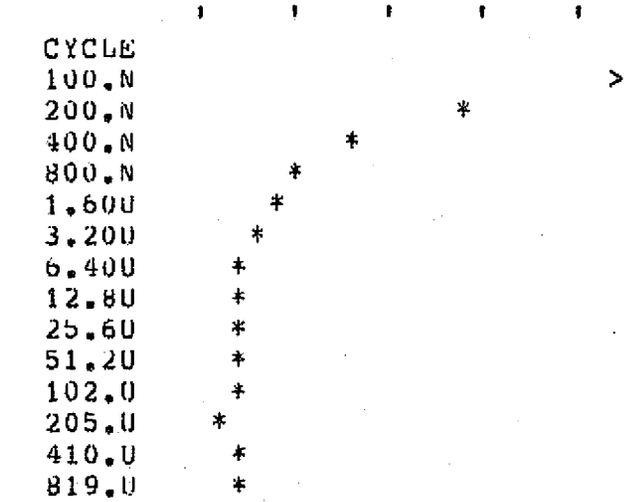


TDH VS. TWP (DATA RZ) VCC = 10.0 V



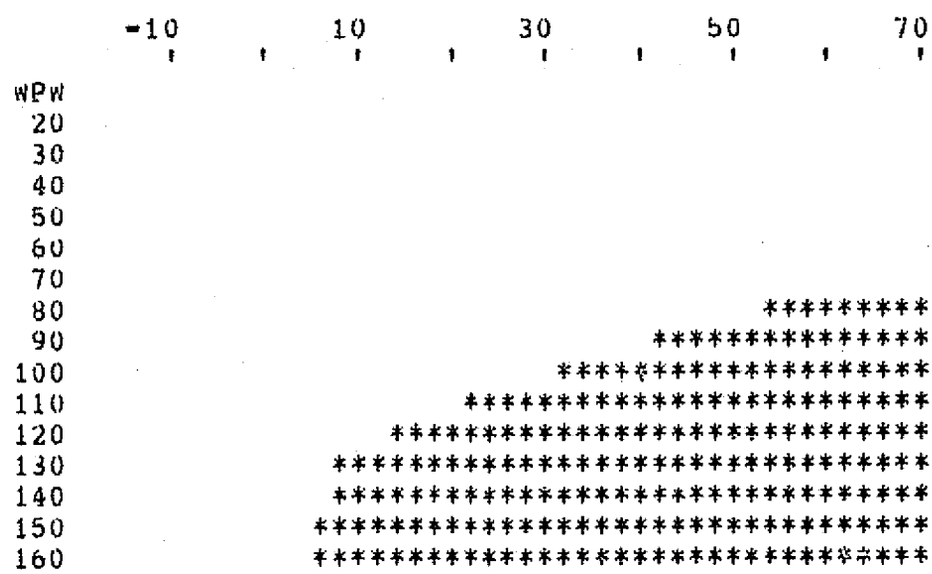
RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: -55 C SN: 4

ICC VS. CYCLE TIME VCC = 10.0V

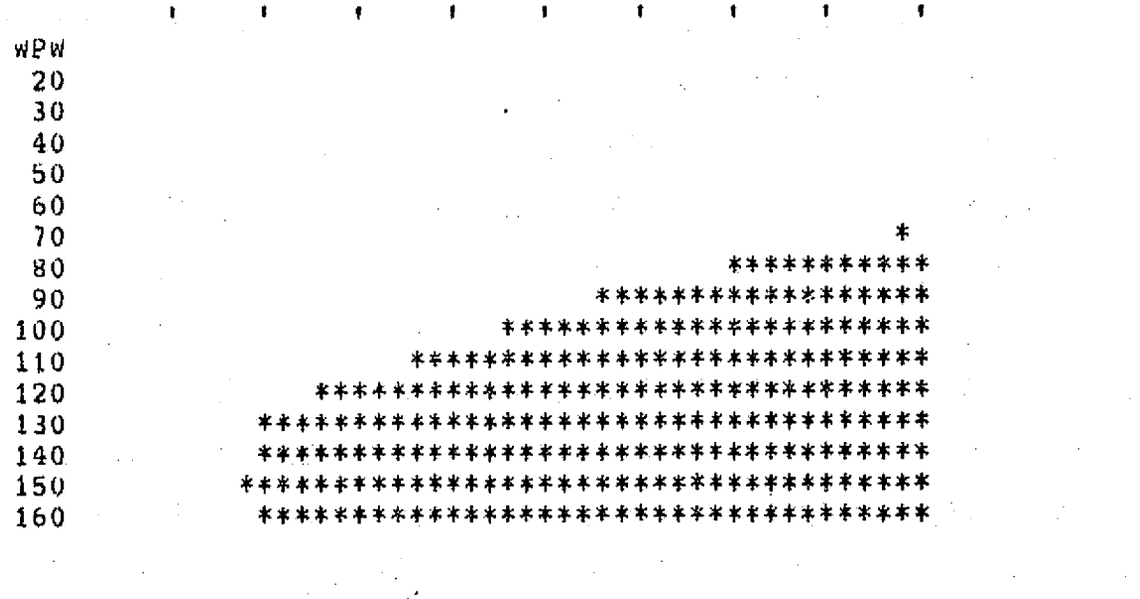


DEVICE PASSED ALL TESTS

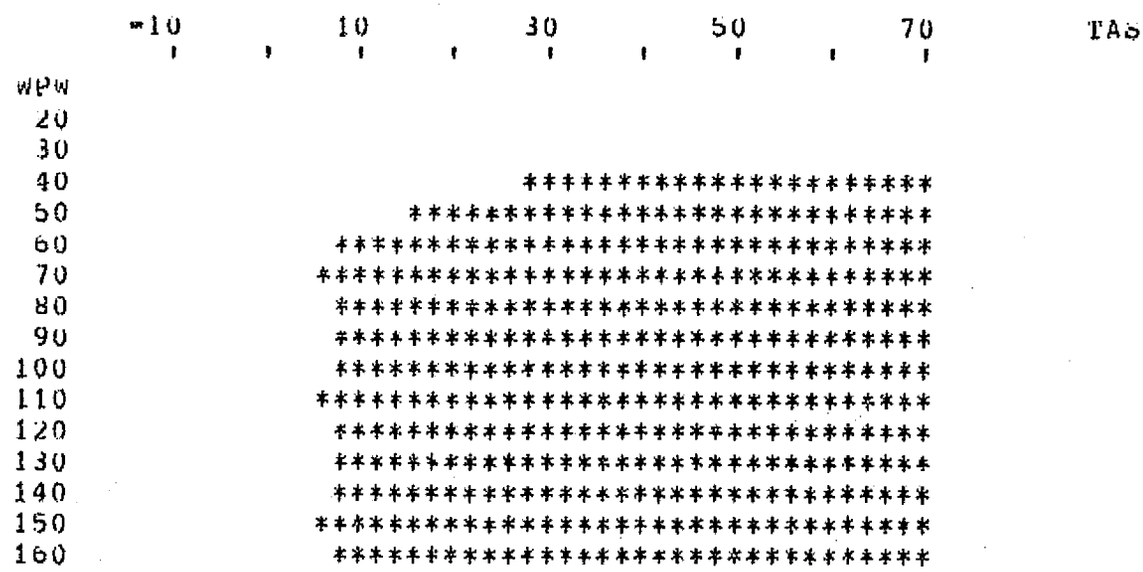
TAS VS. TWP (ADDRESS RZI) VCC = 5.00 V



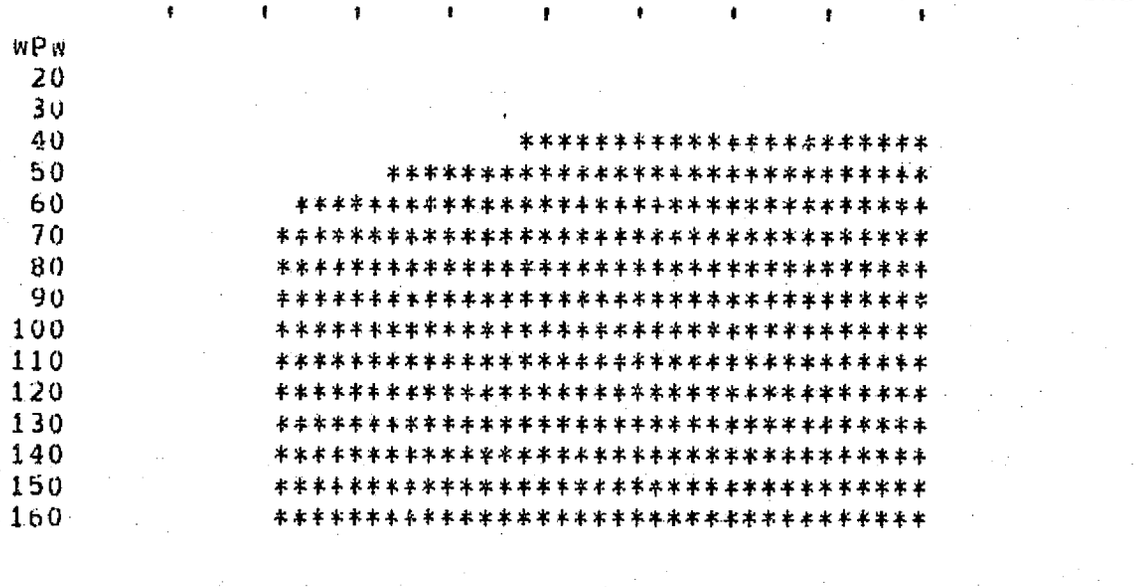
TAS VS. TWP (ADDRESS RZ) VCC = 5.00 V



TAS VS. TWP (ADDRESS RZI) VCC = 10.0 V



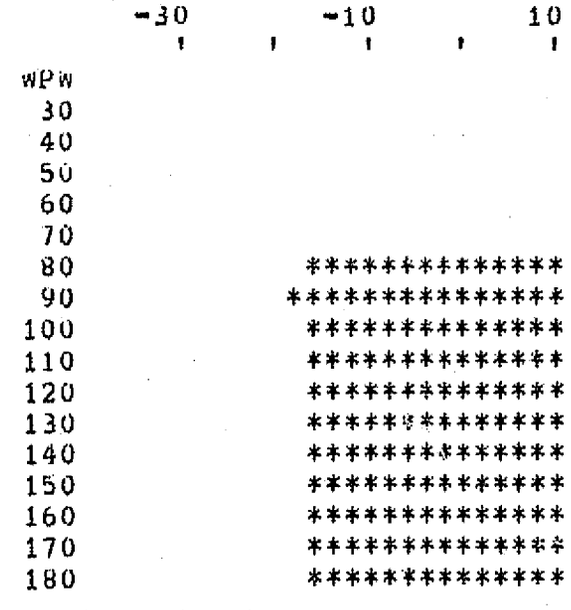
TAS VS. TWP (ADDRESS RZ) VCC = 10.0 V



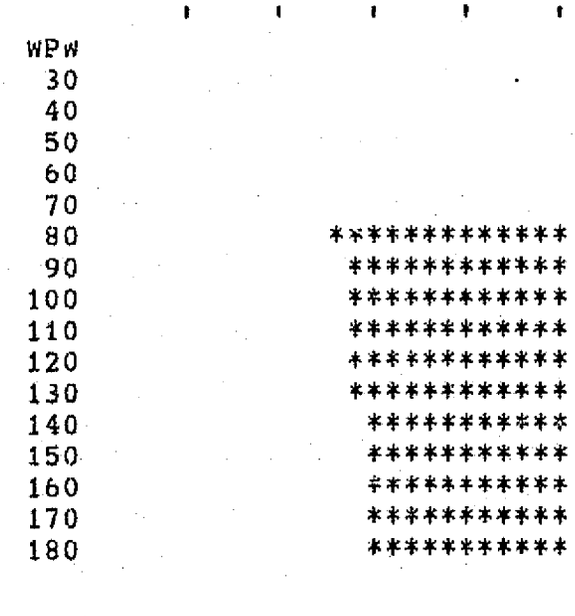
REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 125 C SN: 4

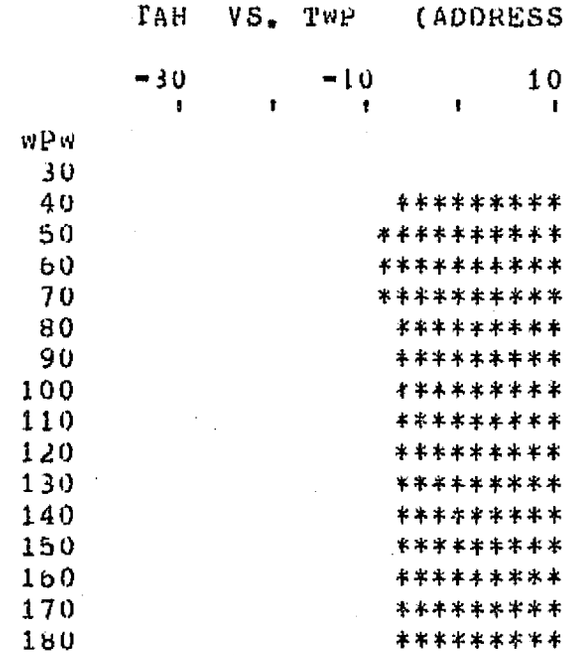
TAH VS. TWP (ADDRESS RZI) VCC = 5.00 V



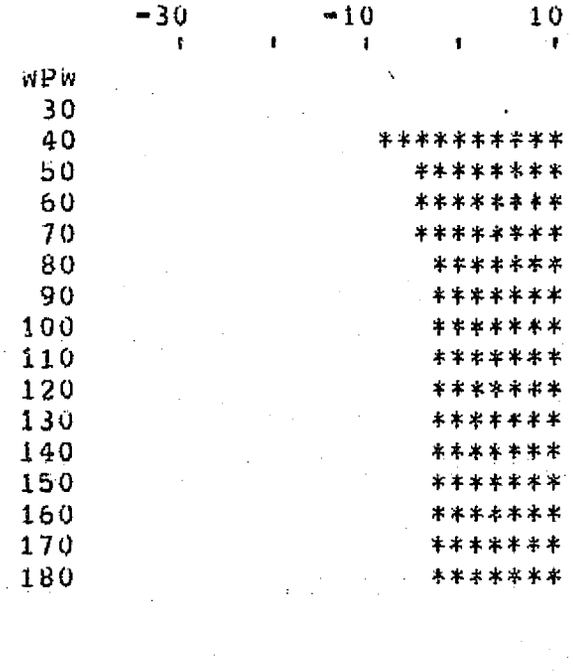
TAH VS. TWP (ADDRESS RZ) VCC = 5.00 V



TAH VS. TWP (ADDRESS RZ1) VCC = 10.0 V



TAH VS. TWP (ADDRESS RZ) VCC = 10.0 V



RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 125 C SN: 4

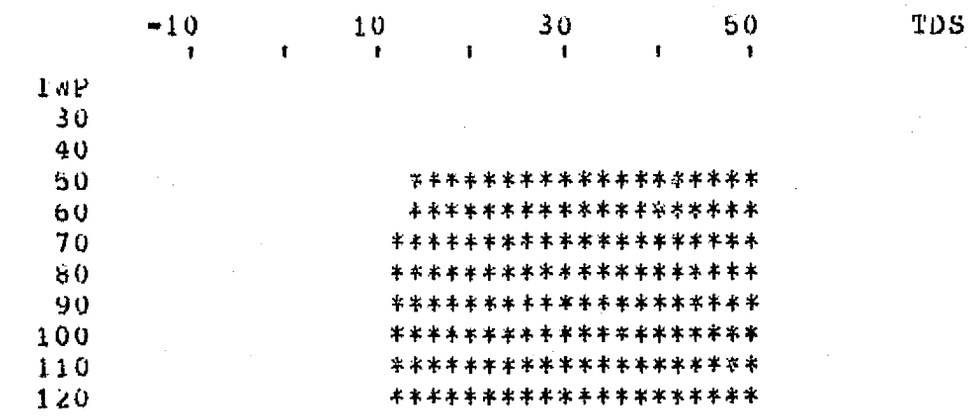
TDS VS. TwP (DATA RZI) VCC = 5.00 V

```
          -10         10         30         50         TDS
           '          '          '          '          '
TwP
 30
 40
 50
 60
 70
 80                  ******************
 90                  ******************
100                  ******************
110                 *******************
120                 *******************
```

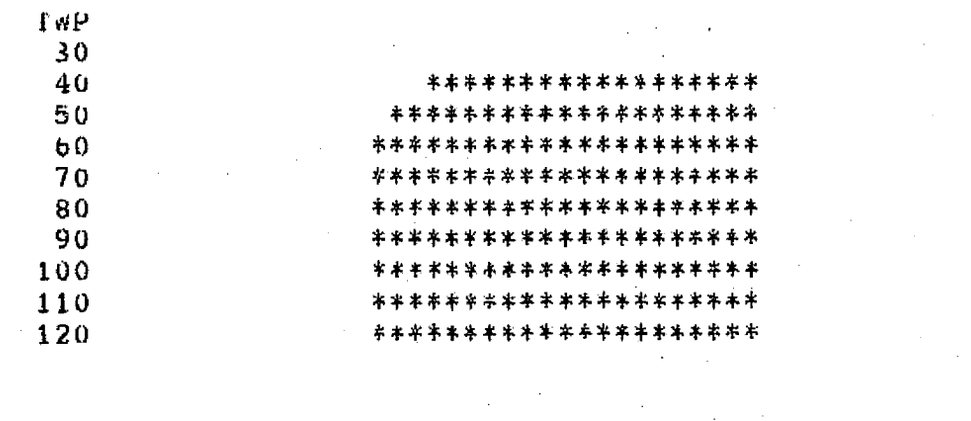
TDS VS. TwP (DATA RZ) VCC = 5.00 V

```
          -10         10         30         50         TDS
           '          '          '          '          '
TwP
 30
 40
 50
 60
 70
 80                     ************
 90                    *************
100                    *************
110                    *************
120                   **************
```

TDS VS. TWP (DATA RZ1) VCC = 10.0 V

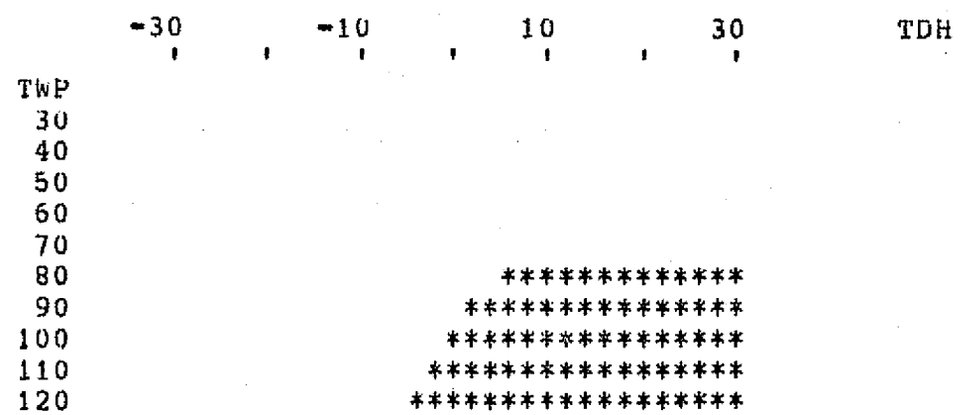


TDS VS. TWP (DATA RZ) VCC = 10.0 V

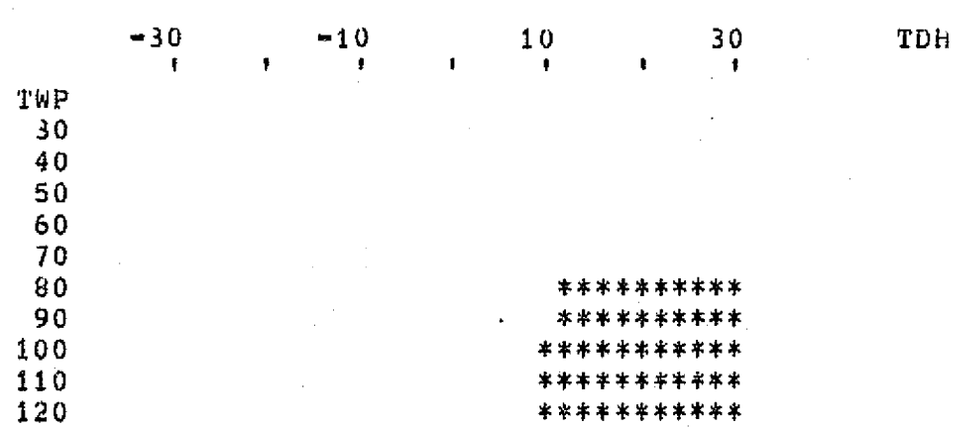


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TDH VS. TWP (DATA RZI) VCC = 5.00 V

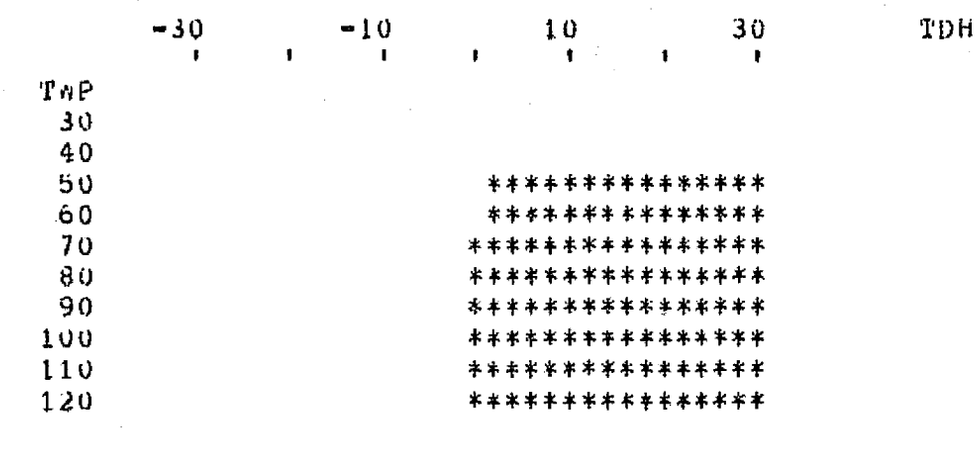


TDH VS. TWP (DATA RZ) VCC = 5.00 V

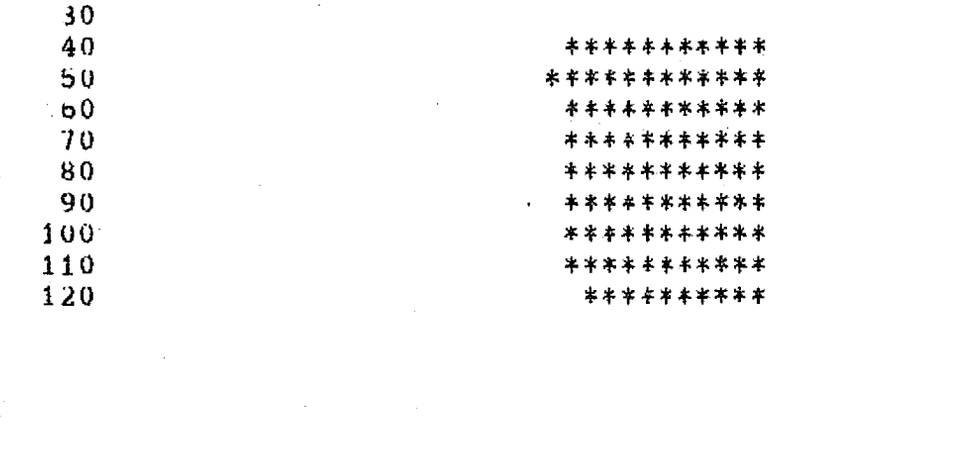


RCA CDP1822SD 256 x 4 CMOS STATIC RAM 08 MAY 79 TEMP: 125 C SN: 4

TDH VS. TWP (DATA RZI) VCC = 10.0 V



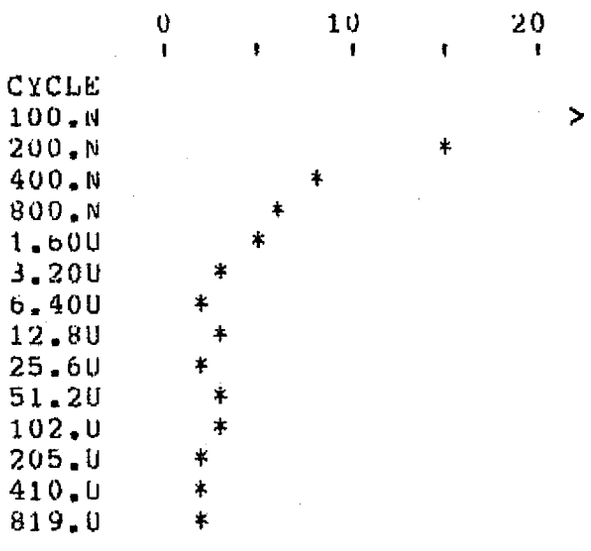
TDH VS. TWP (DATA RZ) VCC = 10.0 V



REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

RCA CDP1822SD 256 X 4 CMOS STATIC RAM 08 MAY 79 TEMP: 125 C SN: 4

ICC VS. CYCLE TIME VCC = 10.0V



DEVICE PASSED ALL TESTS