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ELECTRICAL CHARACTERIZATION OF HUGHES HCMP 1852D AND RCA CDP1852D 8-BIT, CMOS, I/O PORTS

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CULVER CITY, CALIFORNIA

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ELECTRICAL CHARACTERIZATION OF HUGHES HCMP 1852D and RCA CDP1852D 8-BIT, CMOS, I/O PORTS

FINAL REPORT

June 1979

Contract Number JPL 954789, Modification 1

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TEST ABSTRACT

Twenty-five Hughes HCMP 1852D and 25 RCA CDP1852D 8-bit, CMOS, I/O-port microcircuits were subjected to electrical characterization tests. All electrical measurements were performed on a Tektronix S-3260 Test System at the Hughes Aircraft Company Technology Support Division in Culver City, California. Before electrical testing, the devices were subjected to a 168-hour burn-in at 125°C with the inputs biased at 10V. The burn-in was performed at the JPL facilities in Pasadena, California.

Four of the Hughes parts became inoperable during testing. They exhibited functional failures and out-of-range parametric measurements after a few runs of the test program.

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1.0 INTRODUCTION

This report documents the results of electrical characterization tests performed to determine the electrical performance characteristics of 25 RCA CDP1852D and 25 Hughes HCMP 1852D CMOS integrated circuits. The performance characteristics were measured under various electrical conditions at five temperatures. The data was analyzed and tabulated to show the effect of operating conditions on performance and to indicate parameter deviations among the devices in each group. This information can be used in evaluating typical device performance and in determining specification limits. Accuracy was given precedence over time-efficiency where practical, and tests were designed to measure worst-case performance.

The tests were divided into three categories: functional, AC parametric, and DC parametric. The functional tests were performed on a pass/fail basis to verify that the device under test (DUT) was logically correct. All voltage and timing conditions (except supply voltage) were set to nominal values to distinguish between functional failures and statistically unusual devices. The AC parametric tests consisted of propagation delays, transition times, setup times, hold times, and pulse widths. These were measured either by a one-shot technique or by a moving-strobe method, depending on the nature of the measured parameter. The DC parametric tests were simple static measurements made by forcing specified conditions on the DUT and measuring a voltage or current.

All of these tests were performed under computer program control on a Tektronix S-3260 Automated Test System. All devices were subjected to the full set of tests at ambient temperatures of -55°C, -20°C, 25°C, 85°C, and 125°C. The temperature environment was provided by a Temptronic thermal airstream unit (TP450A) under program control.

Twenty-five devices from each manufacturer (RCA and Hughes) were tested. The data was tabulated and analyzed separately for each lot. There were no functional failures or significantly deviant devices in the RCA lot. In the Hughes lot, four devices failed the functional tests and yielded out-of-range or abnormal parametric values. These failures are discussed in detail in Section 4.0.

2.0 DEVICE DESCRIPTION

The RCA CDP1852D and Hughes HCMP 1852D are 8-bit, mode-programmable, parallel input/output ports for use in 1800-series microprocessor systems. They are capable of interfacing directly with the 1802 microprocessor without additional components. They use static silicon-gate CMOS circuitry and are compatible with 4000-series microcircuits. They are supplied in 24-lead, hermetic, dual-in-line, ceramic packages.

A brief functional description of the 1852 device is given in Paragraph 2.2. Pin connections are shown in Figure 1, and a functional diagram appears in Figure 2.

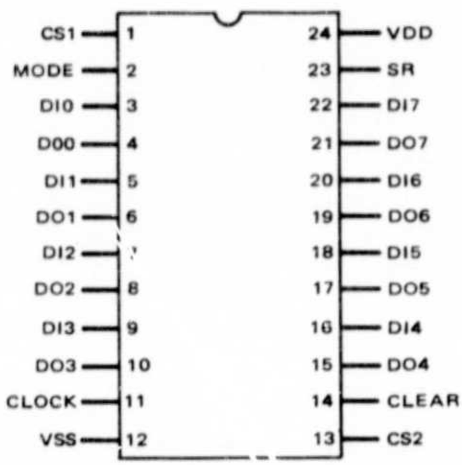

Figure 1. 1852 Pin Connections.

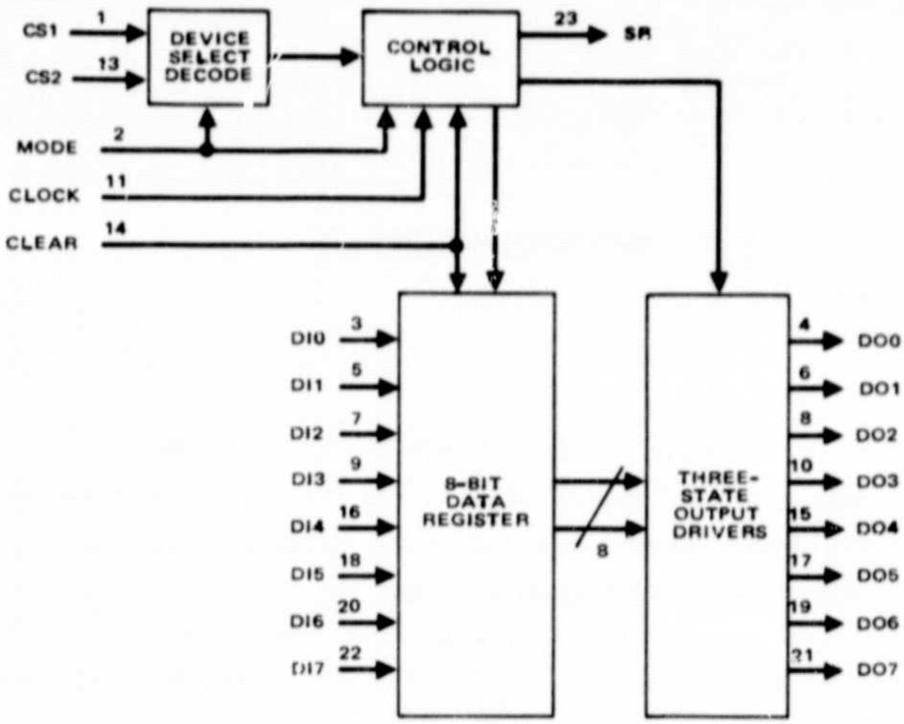

Figure 2. 1852 Functional Diagram

2.1 PIN DESCRIPTIONS

2.1.1 Mode Control Input (Mode)

The mode control input programs the device as an input port (MODE = 0) or an output port (MODE = 1).

2.1.2 Clock Input

The clock input enters data into the data register (see Figure 2) and affects the SR output.

2.1.3 Chip Select Inputs (CS1, CS2)

The chip select inputs enable or disable the tristate data outputs and affect the SR output and entry of data into the register.

2.1.4 Clear Input

The clear input clears the data register and resets the SR output.

2.1.5 Data Inputs (DI0 through DI7)

The data inputs provide the eight bits of data for the register.

2.1.6 Data Outputs (DO0 through DO7)

The data outputs are three-state (logic "1", logic "0", high-impedance) output drivers.

2.1.7 Service Request Output (SR)

The service request output provides the signal to the processor or output device. The output provides positive logic in the output mode and negative logic in the input mode.

2.2 OPERATION

2.2.1 Operation as Input Port

The data at the inputs is strobed into the data register when the clock pin is high (logic "1"). The data outputs are enabled when both chip selects are high (CS1•CS2 = 1). The service request output is set (SR = 0) by negative (high-to-low) transition of CLOCK. The service request output is reset (SR = 1) by negative transition of CS1•CS2 or negative transition of CLEAR. The data register is cleared (set to logic "0") when CLEAR = CLOCK = 0.

2.2.2 Operation as Output Port

The data is strobed into the register when CS1•CS2•CLOCK = 1. Data outputs are enabled at all times. The service request is set (SR = 1) by the negative transition of CS1•CS2. The service request is reset (SR = 0) by the negative transition of CLOCK or the negative transition of CLEAR. The data register is cleared when CLEAR = CLOCK = 0.

3.0 DESCRIPTION OF TESTS

Testing any parameter of an 1852 device involves applying stimuli to the device and observing its response. The details of these two actions define the specific test or measurement. Microcircuit tests can be divided into functional tests, AC parametric tests, and DC parametric tests. The following are brief explanations of the methods used with the Tektronix S-3260 to perform these tests.

3.1 FUNCTIONAL TESTS

Functional tests are performed on a pass/fail basis using a pattern of logical "1"s and "0"s. The pattern defines a series of stimuli to be presented at the DUT inputs and a series of results to be expected at the outputs. The input levels are provided by drivers whose voltage levels can be programmed individually for each input and whose state (1, 0, or inhibited) is controlled by the pattern. The expected DUT output levels are checked by comparators which are also individually programmable and under pattern control. The comparators are strobed so that the output is sampled only during a specific time interval. An error is detected under the following conditions:

1. During comparison for a 1, if the DUT output is less than the logic "1" compare level at any time during the compare window
2. During comparison for a 0, if the DUT output is greater than the logic "0" compare level at any time during the compare window (see Figure 3).

The placement and width of the compare window and the frequency at which the pattern is run are under program control.

The functional tests were performed using the pattern shown in Table 1. The test conditions are shown in Table 2.

3.2 AC Parametric Tests

AC parametric tests performed on the 1852 device include propagation delays, transition times, and input timing tests. The propagation delays were measured using a one-shot (real time) technique which makes a direct measurement of the time between two transitions. The trigger levels at which the measurement clock starts and stops are determined by comparator settings and are programmable.

Transition times are measured indirectly. Propagation delays are measured to the output-under-test at two trigger levels (usually 10 percent and 90 percent of output swing). The difference between the two delays is the transition time between the two levels.

Input timing is controlled on the S3260 by a number of programmable clock phases. An input may be programmed to assume one level (determined by the pattern and drivers) for an entire clock cycle or to appear as a pulse within the cycle. The start time and duration of this pulse are programmable, and several inputs can be pulsed differently within a clock cycle. This allows input timing conditions to be varied over a wide range so that their effect on device performance may be determined. Minimum timing conditions for proper device operation, such as set up and hold times, are measured by moving the pulse edges relative to one another while repeatedly running a functional test pattern (see Paragraph 3.1). If the parameter of interest is varied from a failing condition (for example, very short setup time) to a passing condition, the value at which the device first functions properly is the minimum. To ensure isolation of the parameter under test, the other timing conditions are greatly relaxed.

The following AC parameters were measured at VDD voltages of 5V and 10V (refer to Table 3 for test conditions):

Input Mode Propagation Delays

1. Clear to data outputs (TCLR, Figure 3)
2. Chip select to output on, low (TCAO, Figure 4)

TABLE 1. FUNCTIONAL TEST PATTERN

	Name	Pin	Time Slot																																	
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
Inputs	CS1/CS1	1	0	0	0	1	1	1	1	1	1	1																								
	CS2	13	0	1	0	0	1	1	1	1	1	1																								
	MODE	2	0	0	0	0	0	0	0	0	0	0																								
	CLOCK	11	0	0	0	0	0	1	0	0	1	1																								
	CLEAR	14	0	1	1	1	1	1	1	1	1	1																								
	DI 0	3	1				0			1		0	1	0	0	1	0	1	0	1	1	0	1	0	1	1	1	1	1	1	1	0	0	0	0	0
	DI 1	7	1				1			0		1	0	1	0	1	0	1	0	1	1	0	1	1	0	1						0				
	DI 2	7	1				0			1		0	1	0	1	0	1	1	0	1	1	0	1	1		0	1					0				
	DI 3	9	1				1			0		1	0	1	1	0	1	1	0	1	1	0	1	1			0	1				0				1
	DI 4	16	1				0			1		0	1	0	1	0	1	0	1	0	1	0	1	1				0	1			0			1	0
	DI 5	18	1				1			0		1	0	1	1	0	1	0	1	0	1	0	1	1					0	1		0		1	0	
	DI 6	20	1				1			0		1	0	1	0	1	0	0	1	0	1	0	1	1						0	1	0	1	0		
	DI 7	22	1				1			0		1	0	1	0	1	0	0	1	0	1	0	1	1							0	1	0			
Outputs	DO 0	4	X			X	0	0			1	0	1	0	0	1	0	1	0	1	1	0	1	0	1	1	1	1	1	1	1	0	0	0	0	0
	DO 1	6	X			X	0	1			0	1	0	1	0	1	0	1	0	1	1	0	1	1	0	1						0				
	DO 2	8	X			X	0	0			1	0	1	0	1	0	1	1	0	1	1	0	1	1		0	1					0				
	DO 3	10	X			X	0	1			0	1	0	1	1	0	1	1	0	1	1	0	1	1			0	1				0				
	DO 4	15	X			X	0	0			1	0	1	0	1	0	1	0	1	0	1	0	1	1				0	1			0				
	DO 5	17	X			X	0	1			0	1	0	1	1	0	1	0	1	0	1	0	1	1					0	1		1		1	0	
	DO 6	19	X			X	0	0			1	0	1	0	0	1	0	0	1	0	1	0	1	1						0	1	0	1	0		
	DO 7	21	X			X	0	1			0	1	0	1	0	1	0	0	1	0	1	0	1	1							0	1	0			
	SR SR	23	1	1	1	1	0	0	0	0	0																									

Notes:

X denotes high impedance state.

Blanks denote no change from previous state.

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(Table 1, continued)

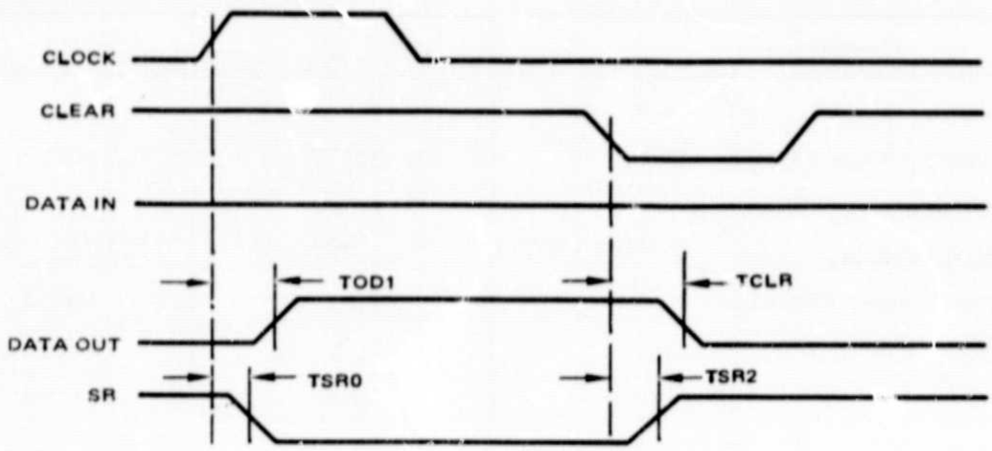
	Name	Pin	Time Slot 35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60
Inputs	CS1/CS1	1	1	1	1	1	1	0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	1	
	CS2	13	1	1	1	1	1	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0	0	1	1	0	
	MODE	2	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	CLOCK	11	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0	
	CLEAR	14	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	DI 0	3	0	0	1	1		0			1													1			0	
	DI 2	5	0	1	0	1		0			1													0			1	
	DI 3	9	0	0	0	1		0			1													0			1	
	DI 4	16	0	0	0	1		0			1													1			0	
	DI 5	18	0	0	0	1		0			1													0			1	
	DI 6	20	0	0	0	1		0			1													1			0	
	DI 7	22	0	0	0	1		0			1													0			1	
Outputs	DO 0	4	0	0	1	1		X			X	0							1						1		1	
	DO 1	6	0	1	0	1		X			X	0							1						0		0	
	DO 2	8	1	0	0	1		X			X	0							1						1		1	
	DO 3	10	0	0	0	1		X			X	0							1						0		0	
	DO 4	15	0	0	0	1		X			X	0							1						1		1	
	DO 5	17	0	0	0	1		X			X	0							1						0		0	
	DO 6	19	0	0	0	1		X			X	0							1						1		1	
	DO 7	21	0	0	0	1		X			X	0							1						0		0	
	SR/SR	23	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	

TABLE 2. FUNCTIONAL TEST CONDITIONS

Condition	At 3V	At 15V
Drivers, High (Logic "1")	3V	15V
Drivers, Low (Logic "0")	0V	0V
Comparators, High	1.5V	7.5V
Comparators, Low	1.5V	7.5V
Cycle Time, (Period)	16 μs	16 μs
Compare Window: Start	15.95 μs	15.95μs
Duration	8 ns	8 ns

TABLE 3. AC-PARAMETRIC TEST CONDITIONS

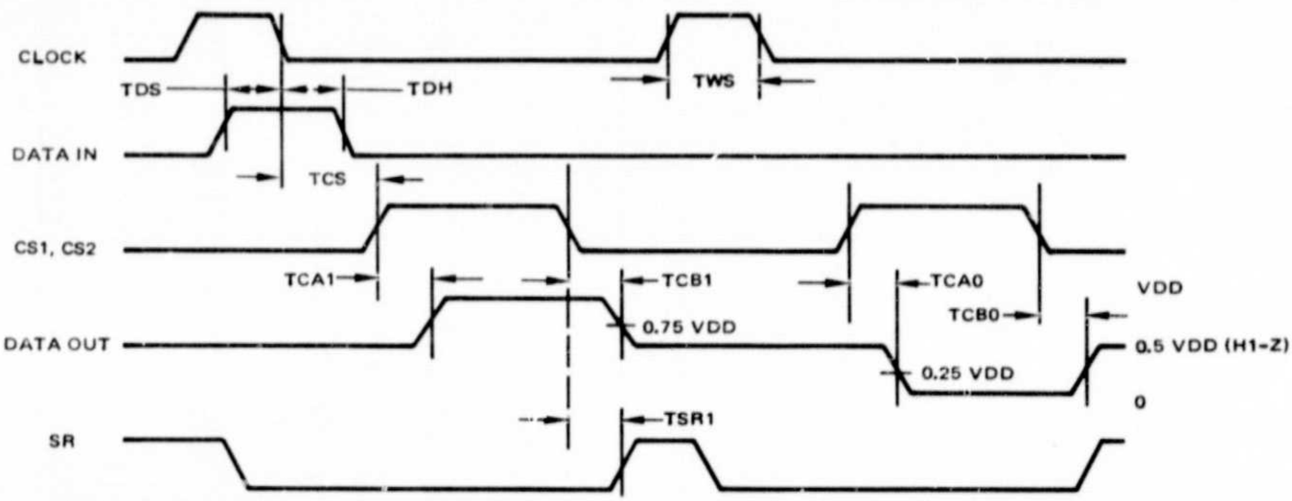
Parameters	At VDD = 5V	At VDD = 10V
Drivers, High	5V	10V
Drivers, Low	0V	0V
Comparators:		
Delays to On/Off:		
High	3.75V	7.5V
Low	1.25V	2.5V
Other Delays:		
High	2.5V	5V
Low	2.5V	5V
Input Timing:		
High	2.5V	5V
Low	2.5V	5V
Transition Time:		
High	4.5V	9V
Low	0.5V	1V
Cycle Time	5 μs	5 μs
Output Loads:		
On/Off	Figure 6	Figure 6
Other	Figure 7	Figure 7



INPUT PORT: MODE = 0 CS1 = 1 CS2 = 1

OUTPUT PORT: MODE = 1 CS1 = 0 CS2 = 1

Figure 3. Input-Port/Output-Port Timing



CLEAR = 1, MODE = 0

Figure 4. Input-Port Timing

3. Chip select to output on, high (TCA1, Figure 4)
4. Chip select to output off, low (TCB0, Figure 4)
5. Chip select to output off, high (TCB1, Figure 4)
6. Clock to service request (TSR0, Figure 3)
7. Chip select to service request (TSR1, Figure 4)
8. Clear to service request (TSR2, Figure 3)

Output Mode Propagation Delays

1. Clear to data outputs (TCLR, Figure 3)
2. Clock to data outputs, high (TOD1, Figure 3)
3. Clock to data outputs, low (TOD0, Figure 3)
4. Clock to service request (TSR0, Figure 3)
5. Chip select to service request (TSR1, Figure 4)

Input Mode Input Timing

1. Minimum clock pulse width (TWS, Figure 4)
2. Minimum data setup time (TDS, Figure 4)
3. Minimum data hold time (TDH, Figure 4)
4. Minimum time from clock 1 0 to chip select 0 1 (TCS, Figure 4)

Output Mode Input Timing

1. Minimum clock pulse width (TWS, Figure 4)
2. Minimum data setup time (TDS, Figure 4)
3. Minimum data hold time (TDH, Figure 4)

Transition Times

1. Output, low to high (TTLH, Figure 5)
2. Output, high to low (TTHL, Figure 5)

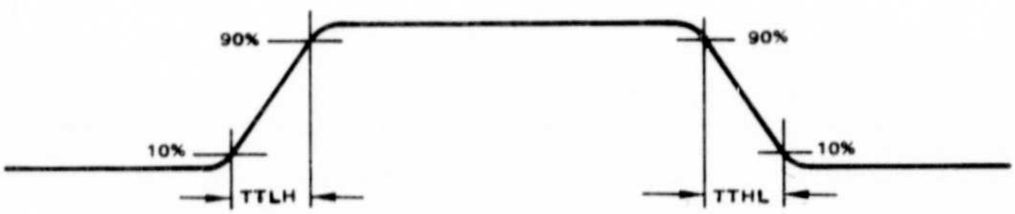
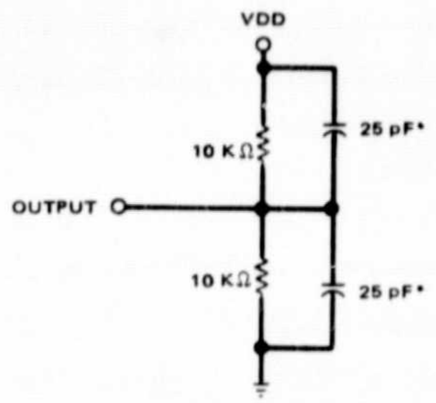
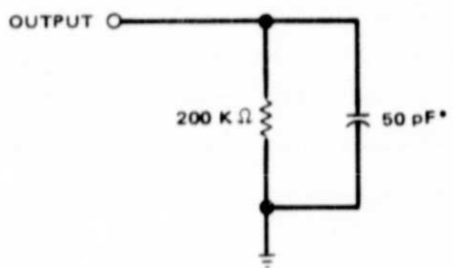


Figure 5. Transition Time



*Includes System Capacitance

Figure 6. Output Load (On/Off)



*Includes System Capacitance

Figure 7. Output Load

The input timing parameters TWS, TDS, and TDH were measured using time slots 9 through 38 of the functional test pattern (refer to Table 1). The parameter under test was varied in 1-nanosecond increments as shown in Table 4. The TCS parameter had no effect on the proper functioning of the device.

3.3 DC PARAMETRIC TESTS

Most of the DC parametric tests were performed in a straightforward manner. Input conditions were applied using the drivers as in the functional and AC tests, and the pin under test was forced with a regulated voltage or current supply (depending on the specific parameter). The desired parameter was then measured and recorded.

TABLE 4. AC PARAMETERS MEASURED WITH PATTERN

Parameter	Varied From (ns)	Varied To (ns)	TDS	TDH	TWS (μs)	Load (Fig.)
TWS	8	500	2μs	3μs	--	4
TDS	-200	300	--	700ns	1	4
TDH	-100	500	500ns	--	1.5	4
TCS	-500	500	1μs	4μs	1	5

The exceptions were the VIH (minimum logic "1" input voltage) and VIL (maximum logic "0" input voltage) tests. These were similar to the input timing tests, except that the input voltages were varied instead of the timing.

In the VIH test, all inputs except the one under test had drive levels of VDD and 0V. Timing conditions were nominal. The logic "0" level of the input under test was set at 0V, and the logic "1" level was set to a voltage low enough to ensure that the device would fail to function properly. The functional test was run repeatedly, with the logic "1" level on the input under test raised each time, until the device passed. The voltage at which the device first passed was the minimum logic "1" level for the input under test. The VIL test was performed in a similar manner.

Table 5 lists the DC parameters measured, with the exception of VIH and VIL. These two parameters were measured using the functional test pattern of Table 2. The timing conditions were the same as those for functional tests (refer to Paragraph 2.2). The input voltages were varied in 0.1-volt increments as shown in Table 6. Each input was tested separately at each voltage.

TABLE 5. DC-PARAMETRIC TESTS

Symbol	Parameter Name	Pin	Voltage/ Current Forced	VDD-VSS (V)	Comments
VICP	Positive input clamp voltage	Each input	1 mA	0	VDD and VSS tied to ground
VICN	Negative input clamp voltage	Each input	-1 mA	0	VDD and VSS tied to ground
IIH	Input current, high	Each input	15 V	15	0V on other inputs
IIL	Input current, low	Each input	0 V	15	15V on other inputs
IOH	Output current, low	Each input	4.6 V 4.5 V 9.5 V 9.0 V 10.5 V	5 5 10 10 12	Output under test is in high (logic "1") state
IOL	Output current, low	Each output	0.4 V 0.5 V 0.5 V 1.0 V 1.5 V	5 5 10 10 12	Output under test is in low (logic "0") state
IOZH	High-impedance output current, high	Each data output	12 V 15 V	12 15	0V on all inputs
IOZL	High-impedance, output current, low	Each data output	0 V 0 V	12 15	0V on all inputs
ISS	Quiescent supply current	VSS	0 V 0 V	10 15	Precondition by running functional test (Table 1) to vectors 1, 5, 7, 9, 21, 40, 44 and 51. Logic "1" = VDD-VSS, Logic "0" = 0V. Outputs open. Eight tests at each of two voltages.

TABLE 6. VIH AND VIL TEST CONDITIONS

Parameter	Varied		Pin Under Test		Other Pins		Compare Levels	
	From (V)	To (V)	VIH (V)	VIL (V)	VIH (V)	VIL (V)	High (V)	Low (V)
VIH (5V)	0	5	-	0	5	0	2.5	2.5
VIL (5V)	5	0	5	-	5	0	2.5	2.5
VIH (10V)	0	10	-	0	10	0	5	5
VIL (10V)	10	0	10	-	10	0	5	5
VIH (12V)	0	12	-	0	12	0	6	6
VIL (12V)	12	0	12	-	12	0	6	6

4.0 TEST RESULTS

4.1 SUMMARY

Three of the Hughes parts (serial numbers 31, 38, and 46) became inoperable during testing. They each performed normally through one or two runs of the test programs, then began to yield out-of-range values. Serial number 31 was the only device to fail both functional tests repeatedly. The other devices passed the functional test but yielded no reading on numerous parametric tests, particularly those performed at high voltages. Serial number 42 exhibited similar characteristics, beginning with the first iteration of the test program, and remained stable through subsequent runs.

None of the RCA parts failed the functional tests or yielded abnormal data.

4.2 DATA TABULATION

For each parameter, the data was tabulated by device serial number and temperature. The sign "<*" to the right of a value was used to indicate an out-of-range measurement. The minimum, maximum, mean, standard deviation, and median values were listed at the bottom of each temperature column. Out-of-range measurements were excluded from the statistics.

The RCA parts were numbered 3 through 27; the Hughes parts were numbered 28 through 52. The statistics for each group were calculated separately. Serial numbers 31, 38, 42, and 46 were excluded from the tabulations.

In addition to the printed data, histograms of some parameters wei provided. Each histogram displays data for one or more parameters at all five temperatures, in ascending order (-55°C, -20°C, 25°C, 85°C, 125°C). The histograms illustrate clearly both the effect of temperature and the distribution of devices for each parameter. RCA and Hughes parts were plotted separately. Table 7 is a list of the parameters plotted. The histograms are provided in Appendix A.

TABLE 7. LIST OF HISTOGRAMS

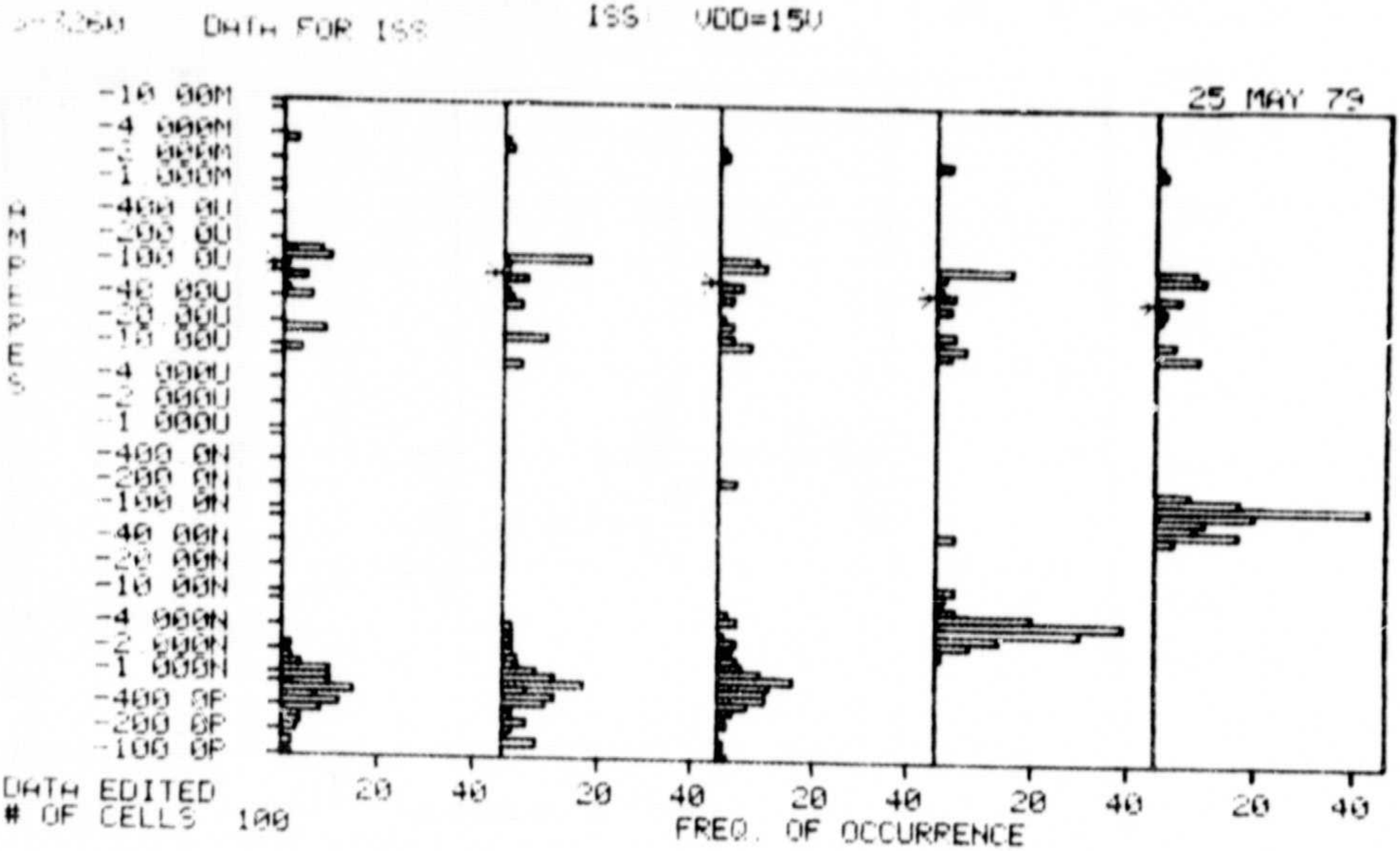
Parameter	Conditions
ISS	VDD = 15V
IOH	VDD = 5V, VO = 4.6V VDD = 10V, VO = 9.5 V
IOL	VDD = 5V, VO = 0.4V VDD = 10V, VO = 0.5V
TCA0 and TCA1 together	VDD = 5V
TCB0 and TCB1	VDD = 5V VDD = 10V
TOD0 and TOD1	VDD = 5V VDD = 10V

ELECTRICAL CHARACTERISTICS OF
HUGHES HCMP 1852D and RCA CDP1852D
8-BIT, CMOS, I/O PORTS

FINAL REPORT

APPENDIX A
HISTOGRAMS

HUGHES HCMP1852D



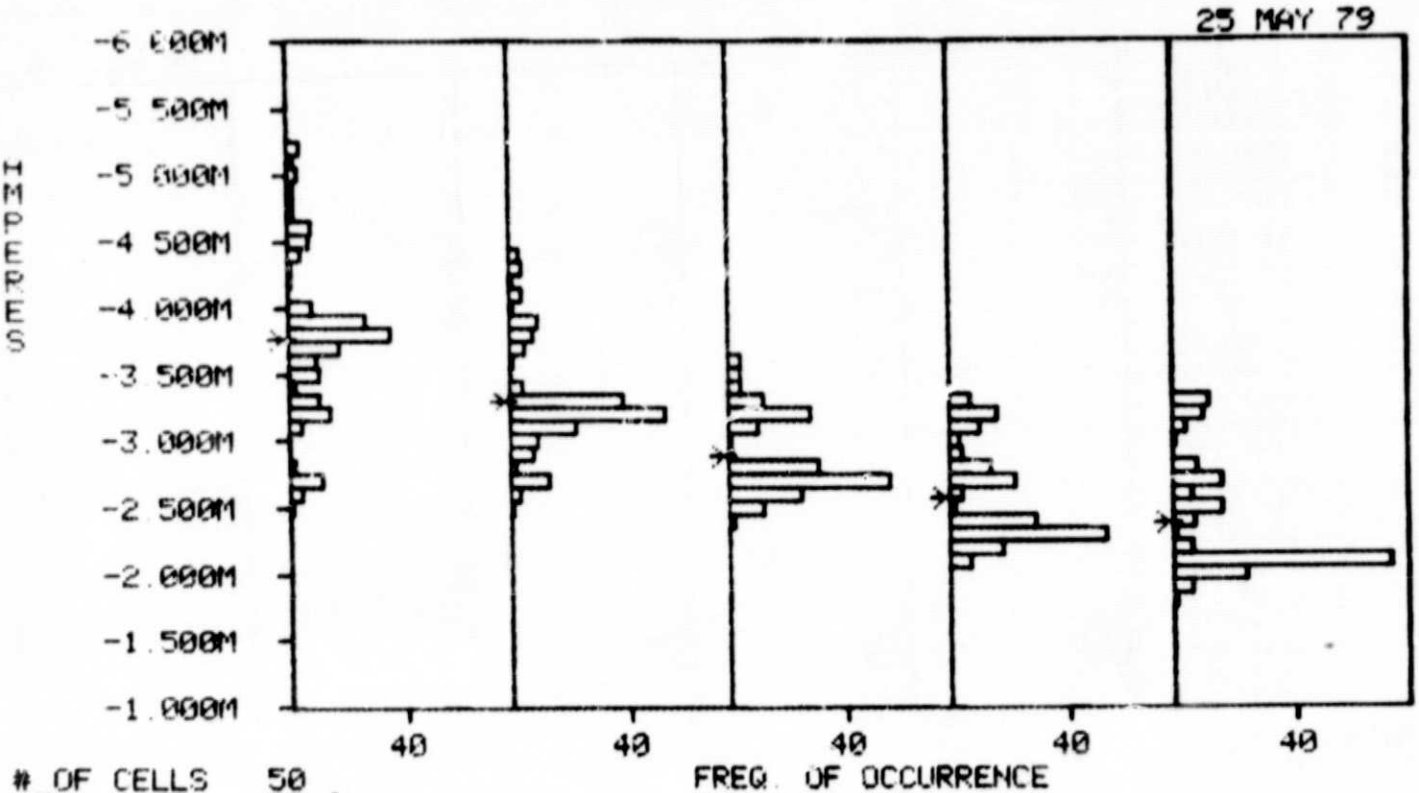
DATA EDITED
OF CELLS 100

READINGS	149	151	150	168	168
MAXIMUM	0.000	0.000	0.000	-2.000N	-51.50N
MEAN	-93.39U	-80.65U	-67.49U	-49.52U	-42.55U
MINIMUM	-3.605M	-3.110M	-2.575M	-2.080M	-1.760M
STD DEV	495.0U	424.3U	351.6U	268.3U	226.3U

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

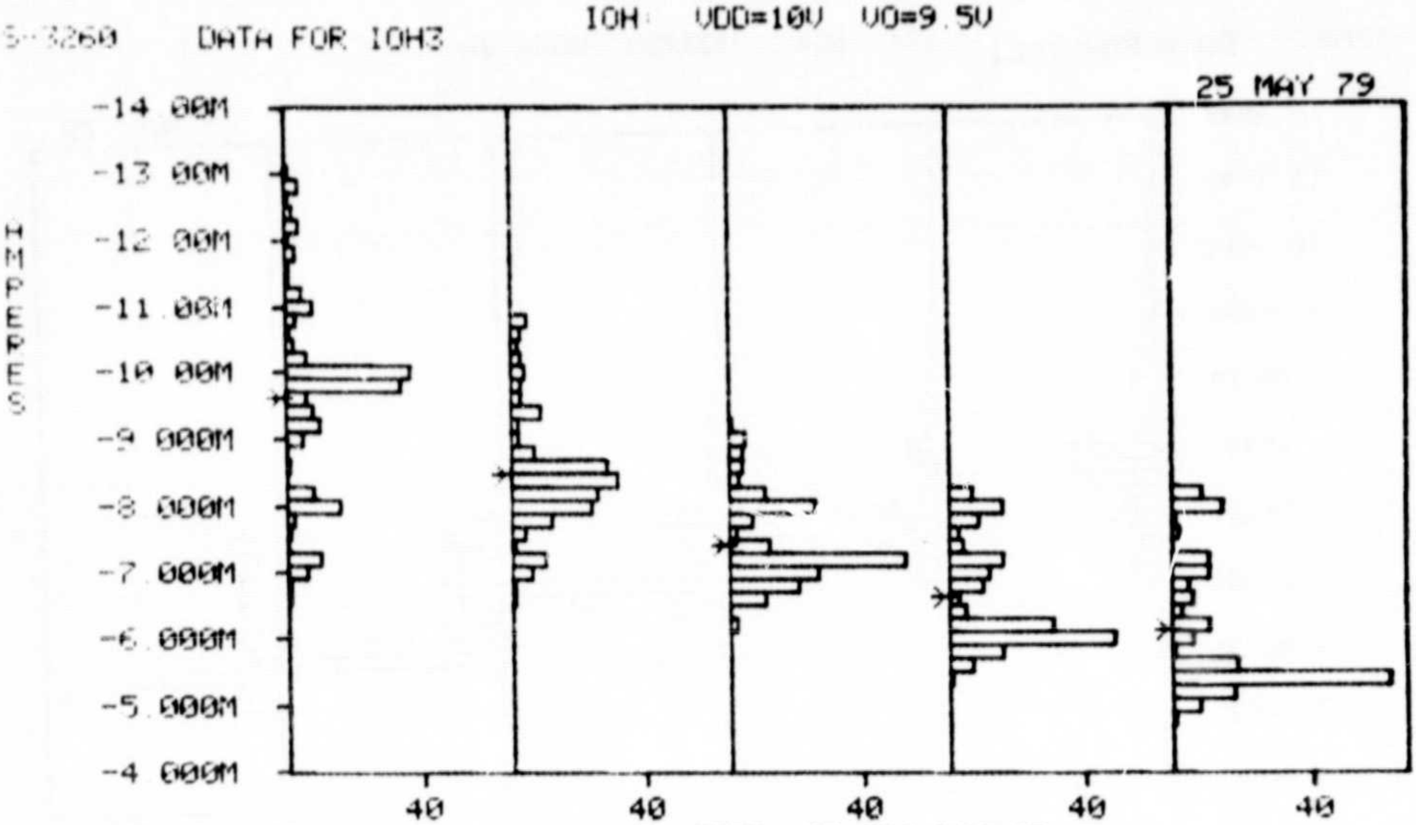
S-3260 DATA FOR IOH1

IOH: VDD=5V VO=4.6V



OF CELLS 50
CELL SIZE 100.0U

READINGS:	189	189	189	189	189
MAXIMUM:	-2.535M	-2.530M	-2.350M	-2.060M	-1.840M
MEAN:	-3.759M	-3.287M	-2.876M	-2.570M	-2.383M
MINIMUM:	-5.235M	-4.400M	-3.595M	-3.315M	-3.315M
STD DEV:	592.6U	382.1U	295.3U	355.8U	425.5U



OF CELLS 50
CELL SIZE 200.0U

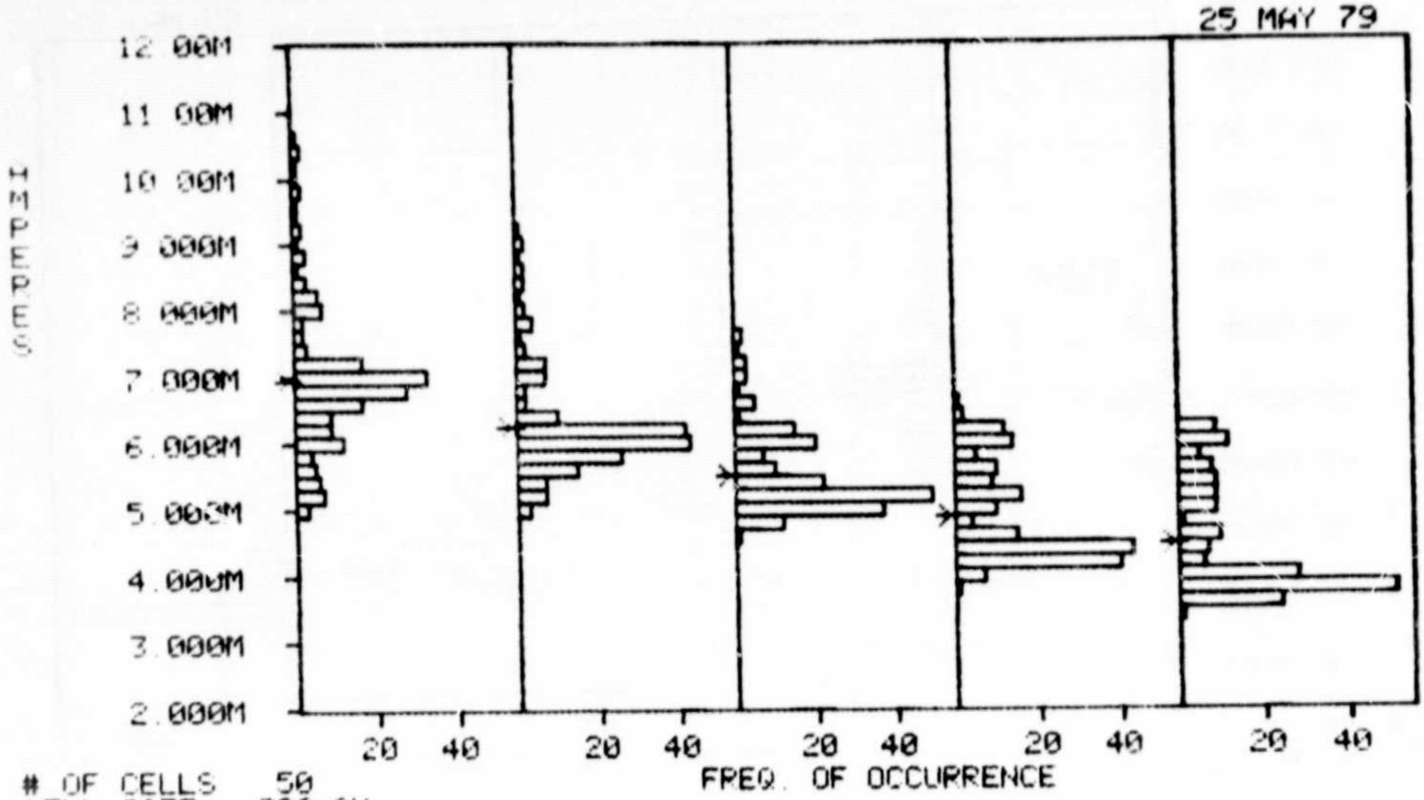
READINGS	189	189	189	189	189
MAXIMUM	-6.610M	-6.620M	-6.230M	-5.415M	-4.845M
MEAN	-9.607M	-8.471M	-7.428M	-6.619M	-6.119M
MINIMUM	-12.95M	-10.90M	-9.120M	-8.215M	-8.220M
STD DEV	1.398M	862.9U	619.2U	788.2U	994.7U

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

IOL: VDD=5V VO=0.4V

S-3260 DATA FOR IOL1

25 MAY 79



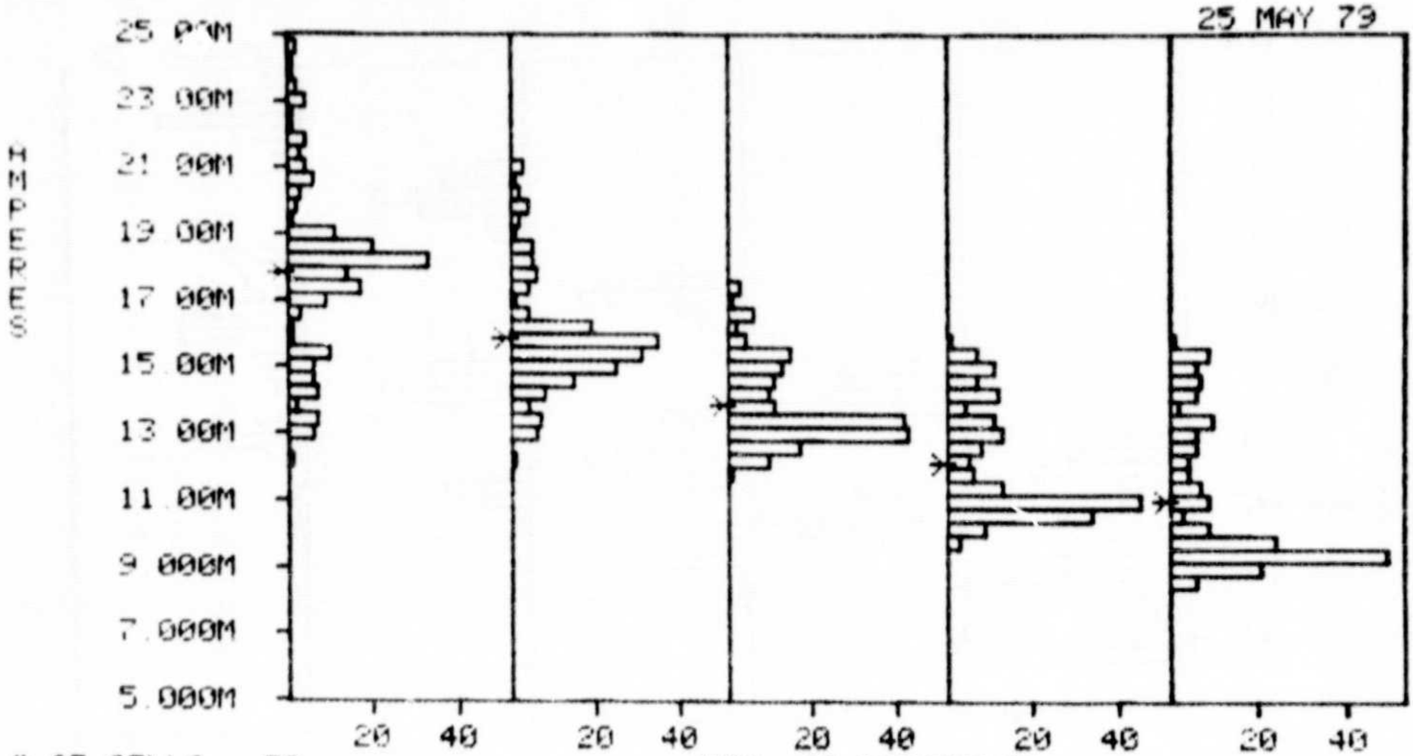
OF CELLS 50
CELL SIZE 200.0U

READINGS	189	189	189	189	189
MAXIMUM	10.60M	9.160M	7.640M	6.555M	6.270M
MEAN	6.947M	6.240M	5.509M	4.882M	4.468M
MINIMUM	4.955M	4.960M	4.640M	3.885M	3.440M
STD DEV	1.093M	785.9U	609.3U	707.9U	852.6U

S-3260 DATA FOR IOL3

IOL: VDD=10V VO=0.5V

25 MAY 79

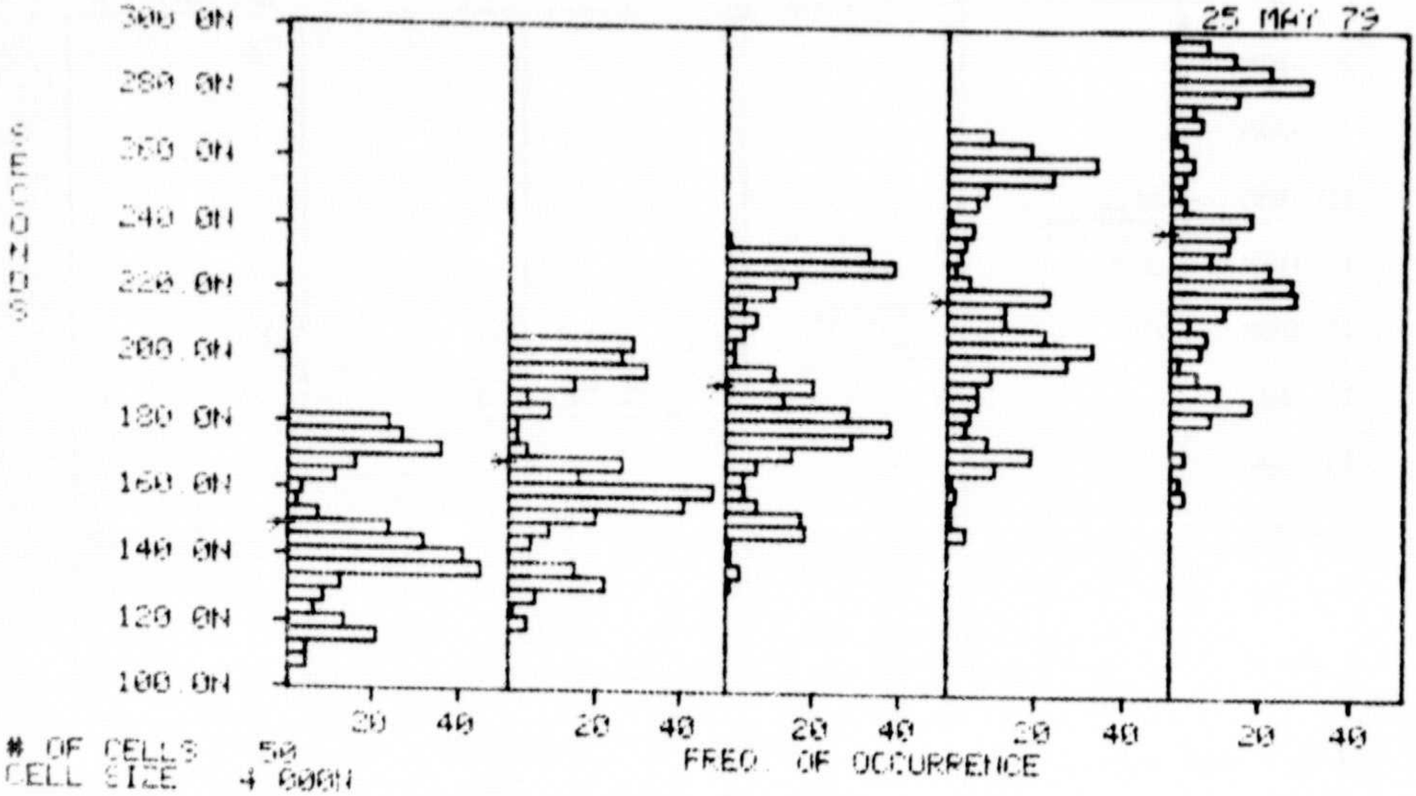


FREQ. OF OCCURRENCE

\# OF CELLS 50
CELL SIZE 400.0U

READINGS:	189	189	189	189	189
MAXIMUM	24.50M	21.10M	17.50M	15.60M	15.60M
MEAN	17.81M	15.83M	13.83M	12.13M	11.01M
MINIMUM:	12.40M	12.35M	11.75M	9.620M	8.435M
STD DEV :	2.580M	1.677M	1.215M	1.613M	2.107M

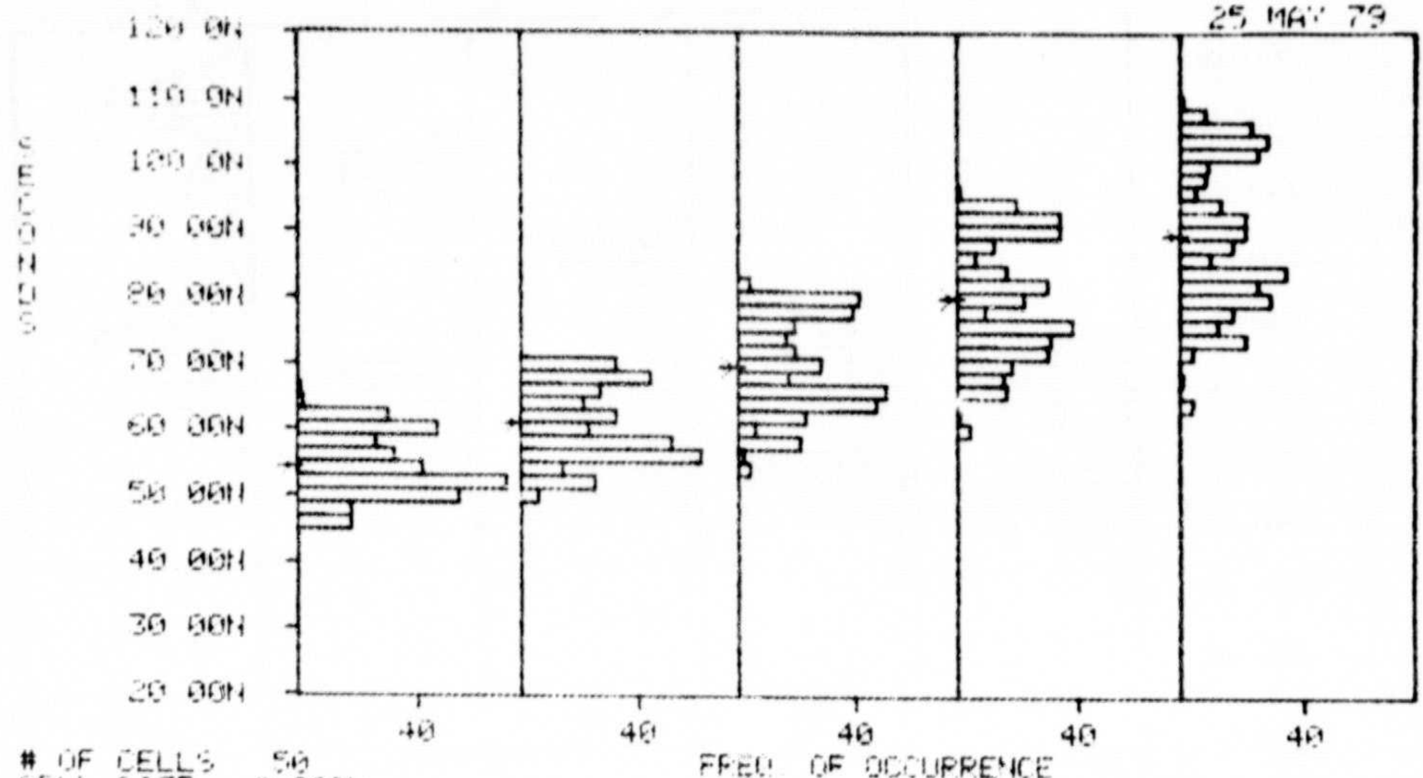
5-7260 DATA FOR TH01A TCA1, TCA0 VDD=5V



OF CELLS 50
CELL SIZE 4.000N

READINGS	336	336	336	336	336
MAXIMUM	182.0N	205.0N	235.0N	270.0N	299.0N
MEAN	148.7N	168.3N	192.1N	217.9N	239.4N
MINIMUM	107.0N	119.5N	133.5N	147.0N	160.0N
STD DEV	20.36N	23.57N	27.49N	32.19N	35.87N

S-3260 DATA FOR TA01B TCH1,TCA0 VDD=10V

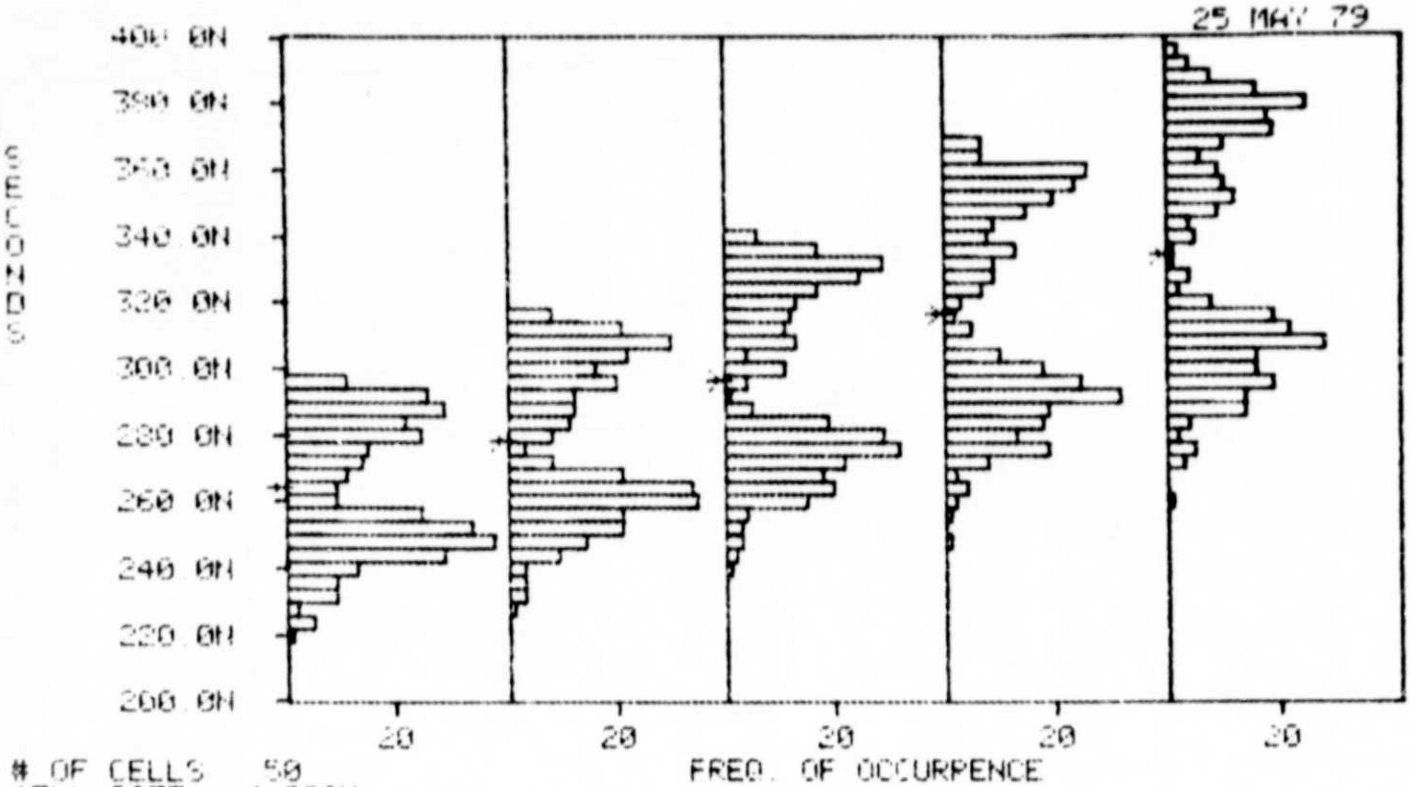


\# OF CELLS 50
CELL SIZE 2.000N

READINGS	336	336	336	336	336
MAXIMUM	66.05N	70.90N	81.90N	96.60N	110.0N
MEAN	54.23N	60.85N	69.63N	79.99N	89.38N
MINIMUM	45.25N	49.20N	53.65N	59.00N	64.45N
STD DEV	4.686N	5.768N	7.124N	8.918N	10.83N

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

S-32EA DATA FOR TE01A TCB0.TCB1 VDD=5V

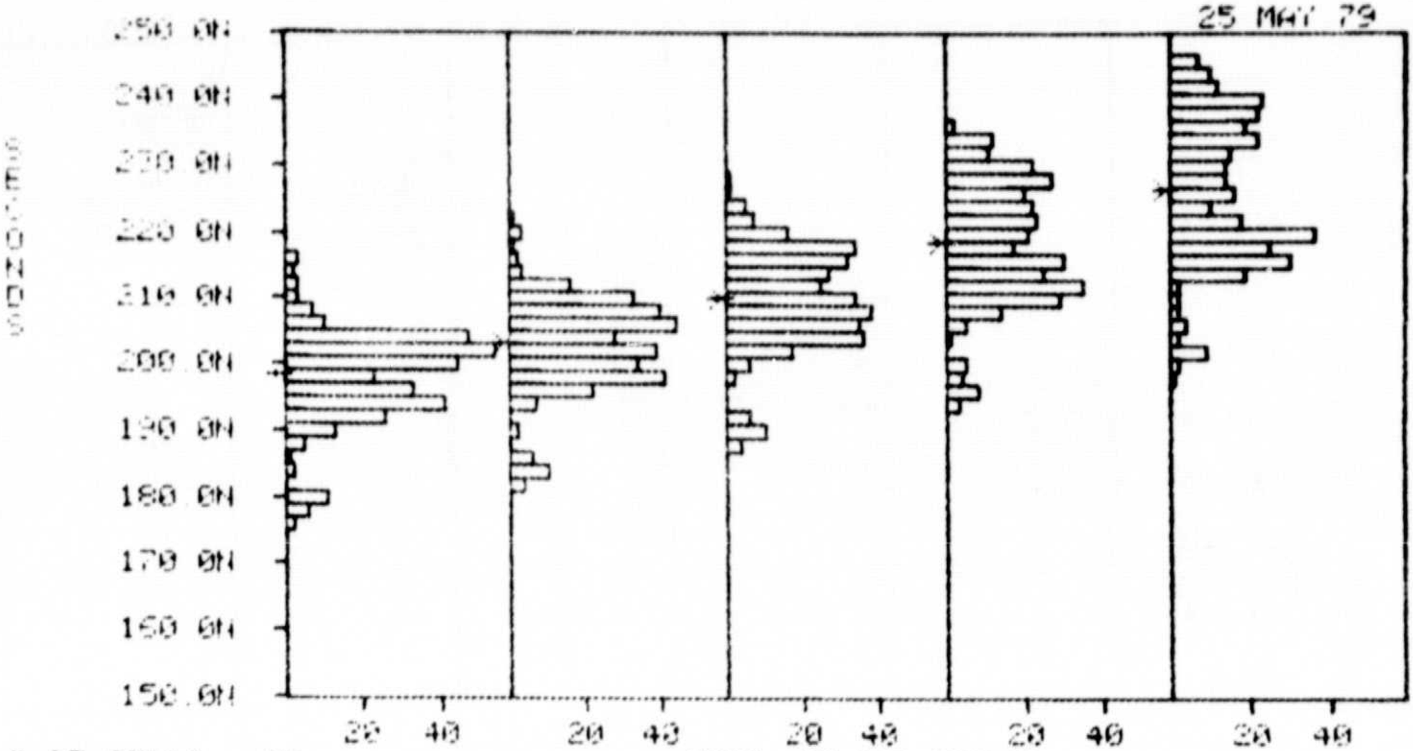


OF CELLS 50
CELL SIZE 4.000N

READINGS:	336	336	336	336	336
MAXIMUM:	297.5N	315.5N	340.5N	368.5N	394.5N
MEAN:	264.1N	279.3N	296.3N	316.4N	334.3N
MINIMUM:	222.0N	230.0N	239.5N	249.5N	259.0N
STD DEV.:	19.81N	23.17N	27.30N	32.17N	36.14N

5-3260 DATA FOR TB01B TCB0,TCB1 VDD=10V

25 MAY 79



FREQ OF OCCURRENCE

\# OF CELLS 50
CELL SIZE 2.000N

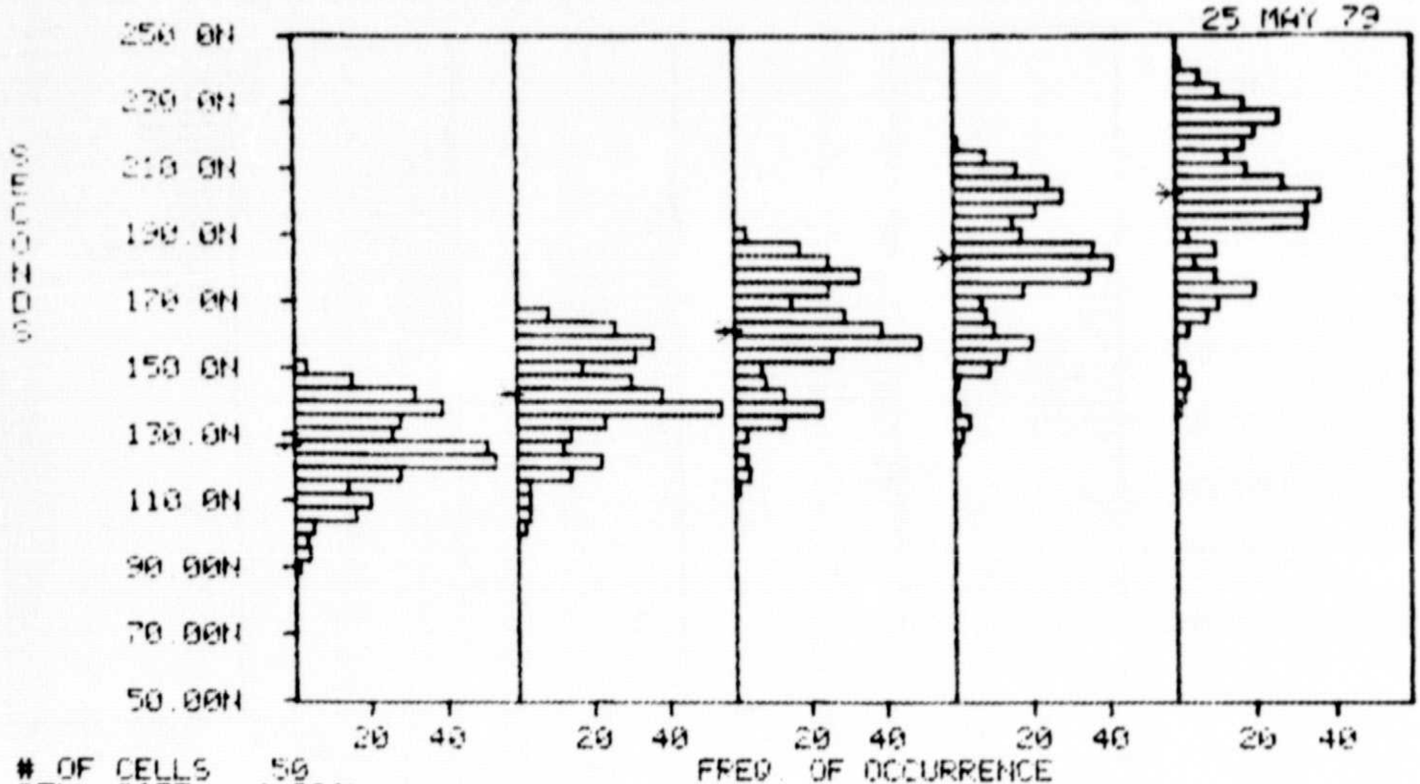
READINGS	336	336	336	336	336
MAXIMUM	216.0N	221.5N	227.5N	237.0N	247.0N
MEAN	198.1N	203.0N	210.0N	218.5N	225.5N
MINIMUM	176.5N	181.5N	187.5N	193.5N	198.5N
STD DEV	7.059N	7.097N	7.728N	9.294N	11.12N

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

S-3260 DATA FOR TD01A

TOD0.TOD1 VDD=5V

25 MAY 79



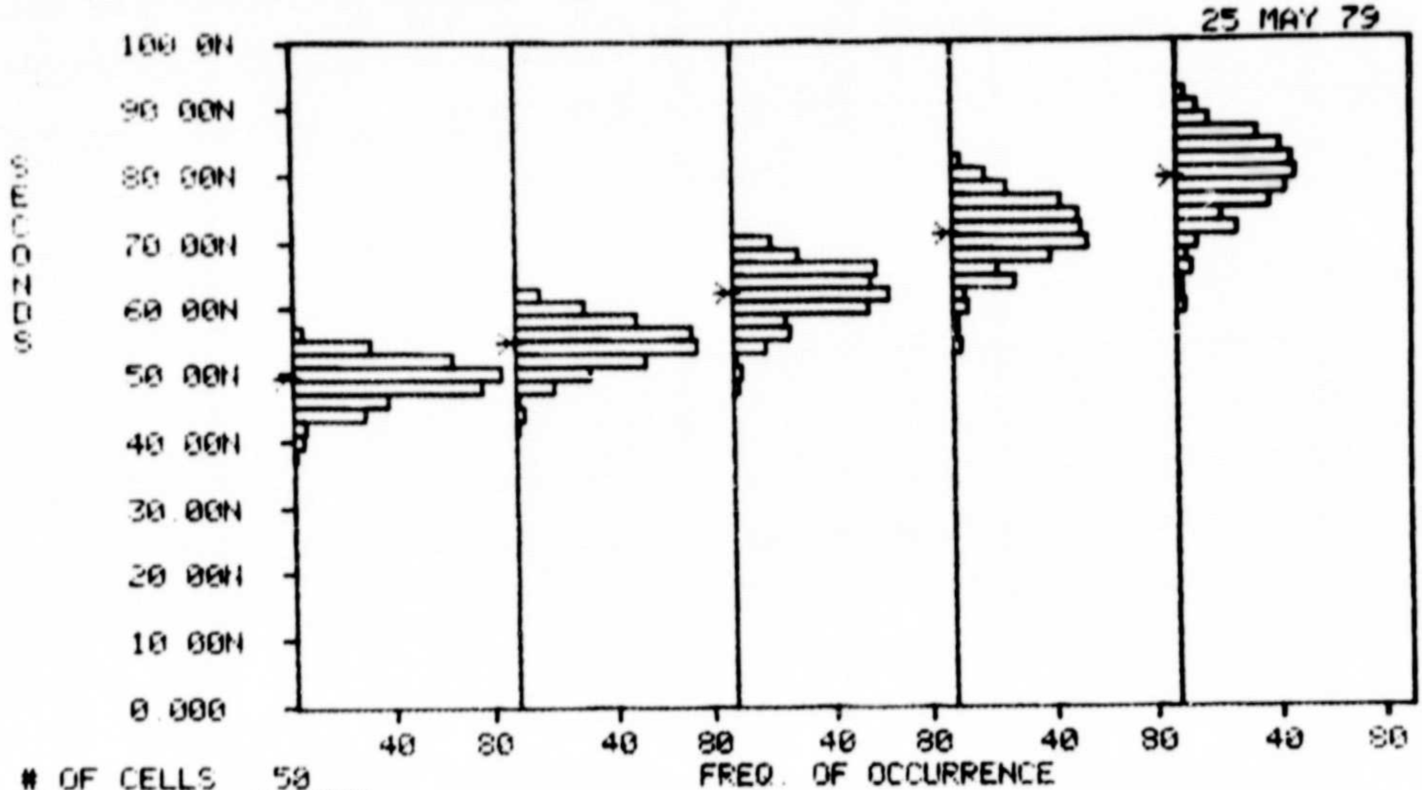
OF CELLS 50
CELL SIZE 4.000N

READINGS	336	336	336	336	336
MAXIMUM	149.0N	166.5N	189.0N	217.5N	241.0N
MEAN	126.3N	141.9N	161.3N	193.2N	202.3N
MINIMUM	91.40N	102.5N	114.5N	127.0N	139.5N
STD DEV	12.24N	13.91N	16.05N	18.80N	20.94N

S-3260 DATA FOR TD01B

TOD0,TOD1: VDD=10V

25 MAY 79



OF CELLS 50
CELL SIZE 2.000N

READINGS:	336	336	336	336	336
MAXIMUM:	56.35N	62.20N	70.80N	82.05N	92.00N
MEAN:	49.12N	54.66N	62.24N	71.18N	79.35N
MINIMUM:	38.70N	42.85N	48.45N	53.65N	59.55N
STD DEV:	3.145N	7.562N	4.260N	5.136N	5.881N

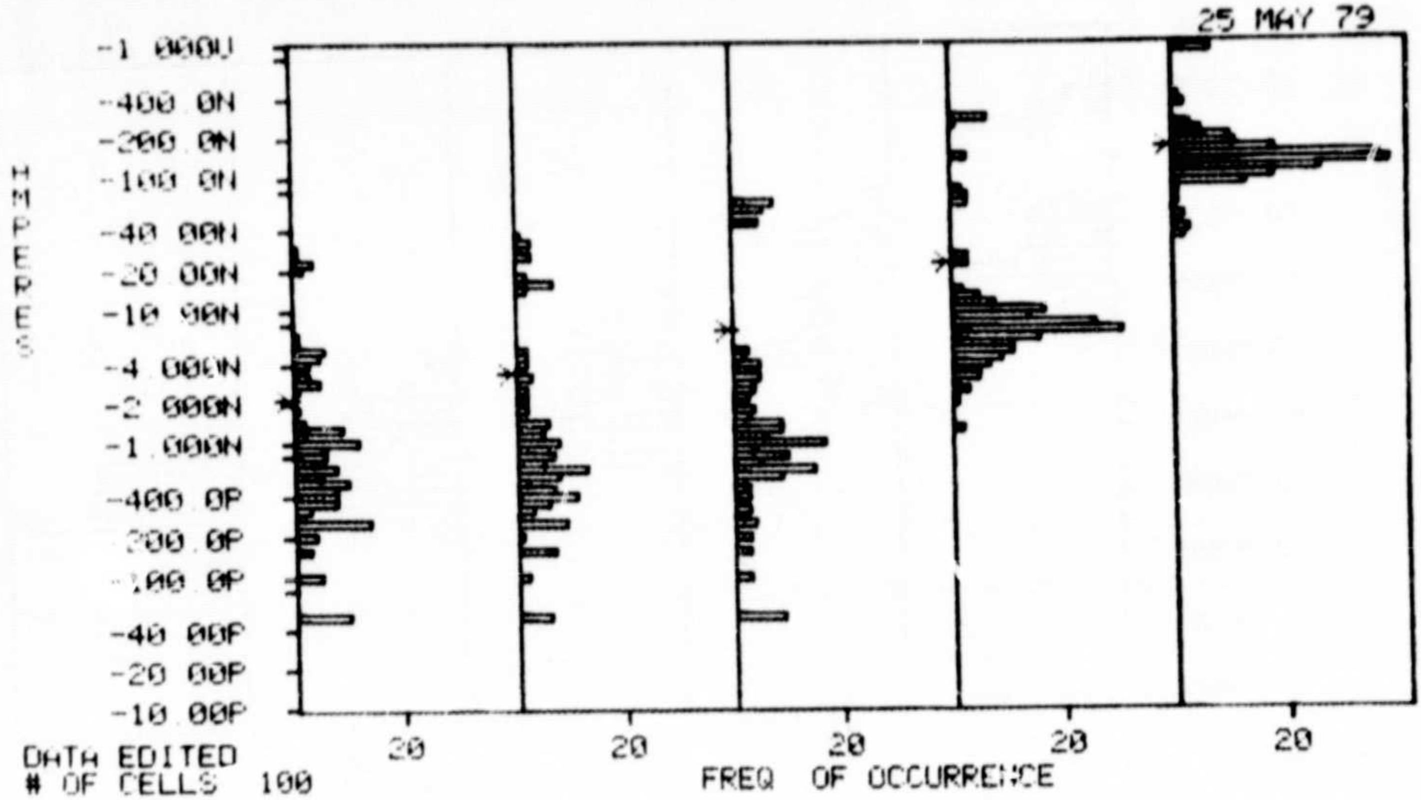
REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

RCA CDP1852D

S-3260 DATA FOR ISS

ISS VDD=15V

25 MAY 79

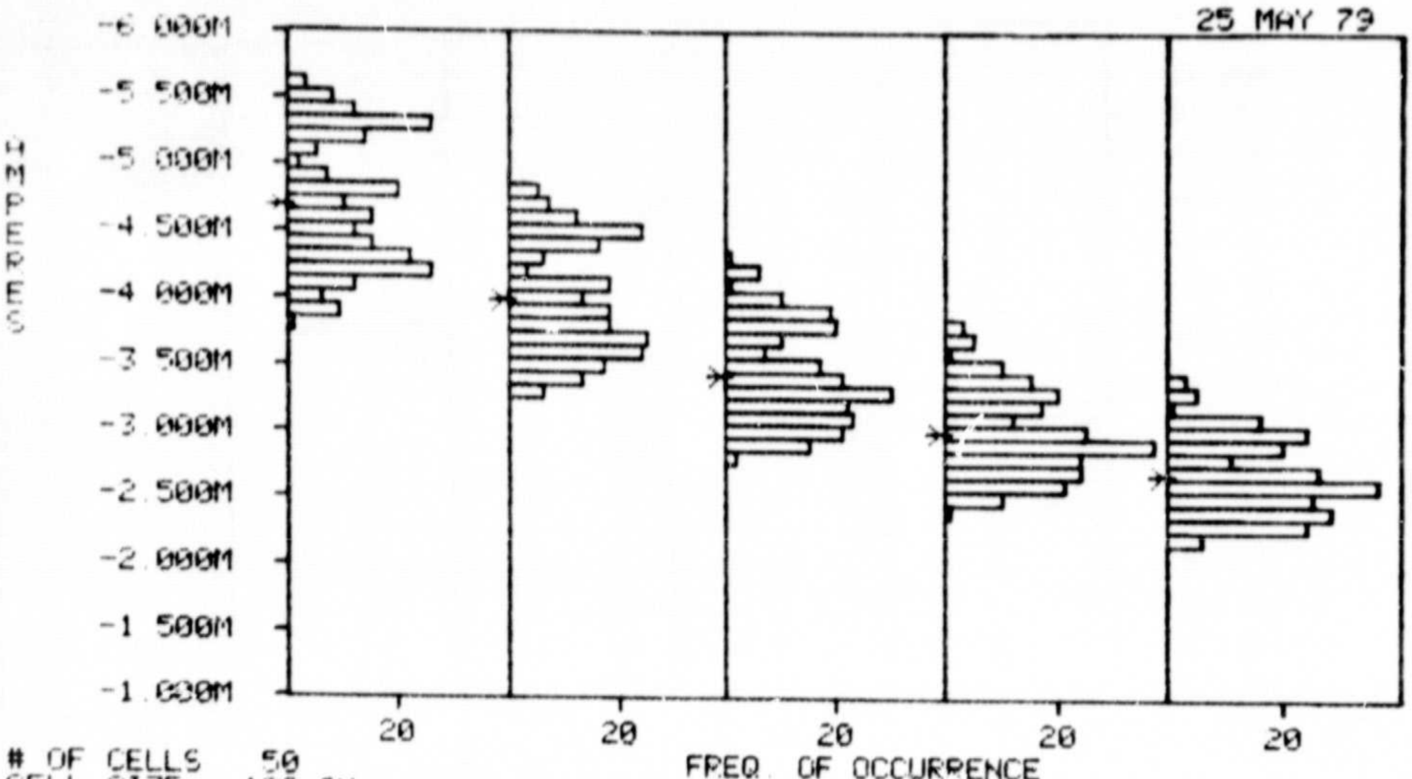


DATA EDITED
OF CELLS 100

READINGS	168	159	176	200	200
MAXIMUM	0.000	0.000	0.000	-1.200N	-35.45N
MEAN	-2.137N	-3.406N	-7.107N	-22.55N	-167.8N
MINIMUM	-28.85N	-33.95N	-65.00N	-271.0N	-955.0N
STD DEV.	4.831N	7.290N	17.15N	54.29N	161.9N

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

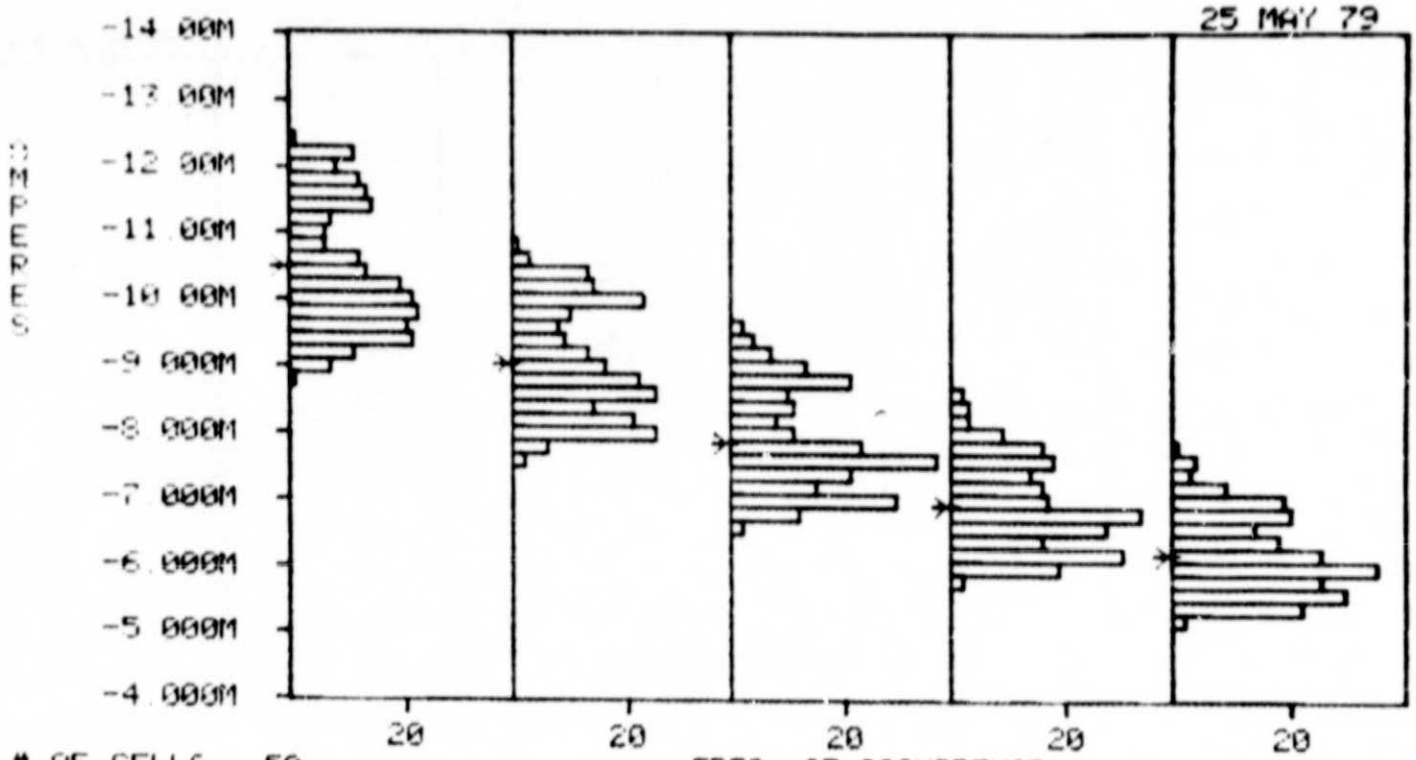
S-32[illegible]   DATA FOR IOH1   IOH: VDD=5V VO=4.6V



OF CELLS 50
CELL SIZE 100.0U

READINGS:	225	225	225	225	225
MAXIMUM:	-3.805M	-3.255M	-2.785M	-2.430M	-2.190M
MEAN:	-4.683M	-3.979M	-3.421M	-2.993M	-2.675M
MINIMUM:	-5.590M	-4.810M	-4.260M	-3.815M	-3.395M
STD DEV:	488.8U	417.3U	360.3U	314.1U	281.9U

S-3260 DATA FOR IOH3 IOH VDD=10V VO=9.5V

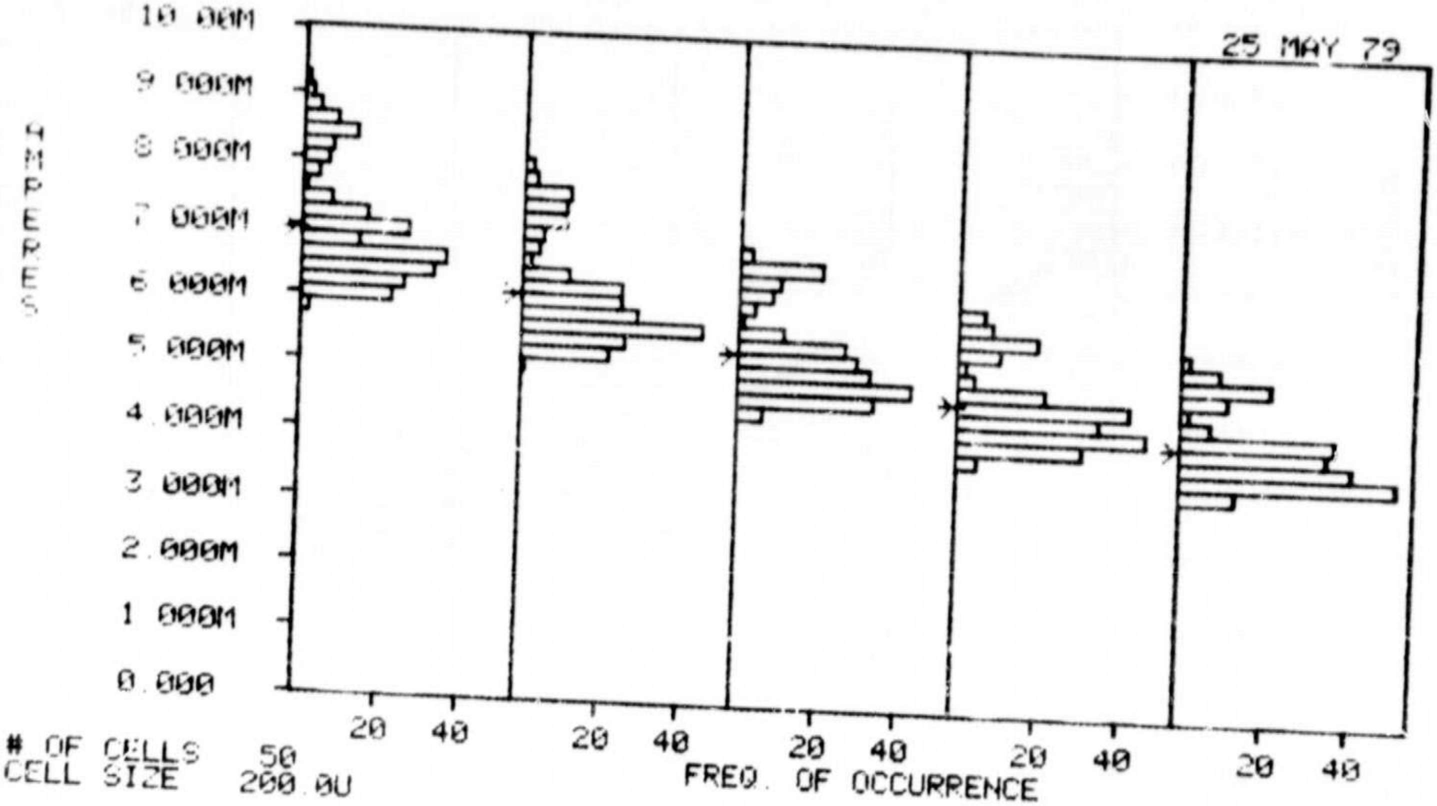


OF CELLS 50
CELL SIZE 200.0U

READINGS	225	225	225	225	225
MAXIMUM	-8.760M	-7.600M	-6.520M	-5.725M	-5.155M
MEAN	-10.45M	-9.049M	-7.862M	-6.914M	-6.210M
MINIMUM	-12.35M	-10.75M	-9.570M	-8.575M	-7.710M
STD DEV	953.3U	826.2U	743.9U	652.2U	589.8U

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

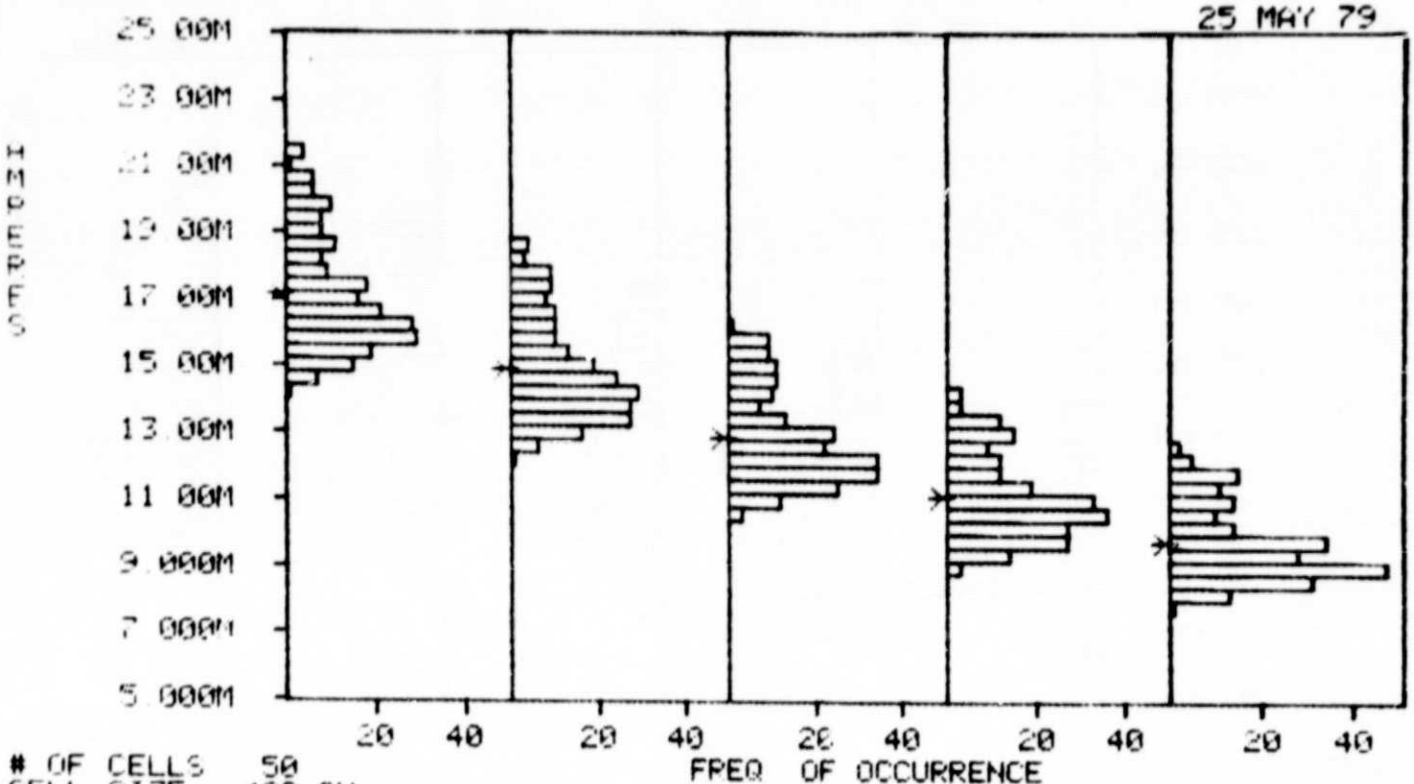
S-3260 DATA FOR IOL1 IOL: VDD=5V VO=0.4V



READINGS:	225	225	225	225	225
MAXIMUM:	9.110M	7.950M	6.850M	6.030M	5.340M
MEAN:	6.947M	6.072M	5.285M	4.616M	4.083M
MINIMUM:	5.830M	5.050M	4.360M	3.760M	3.320M
STD DEV :	816.6U	730.7U	652.9U	567.4U	512.6U

S-3260 DATA FOR IOL3 IOL VDD=10V VO=0.5V

25 MAY 79



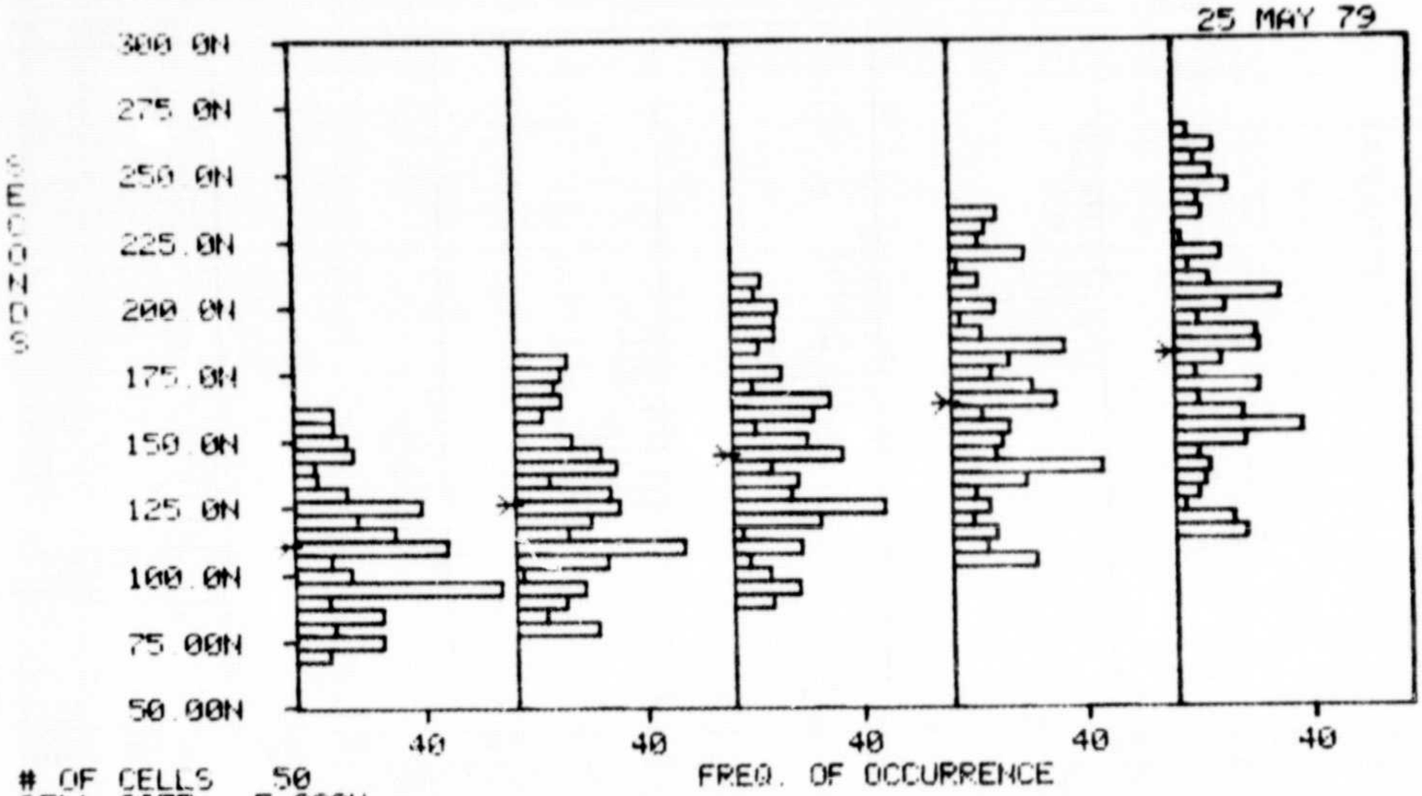
OF CELLS 50
CELL SIZE 400.0U

READINGS	225	225	225	225	225
MAXIMUM	21.50M	18.65M	16.05M	14.25M	12.55M
MEAN	17.11M	14.87M	12.84M	11.12M	9.753M
MINIMUM	14.20M	12.25M	10.50M	8.950M	7.880M
STD DEV	1.706M	1.525M	1.365M	1.212M	1.106M

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

S-3260 DATA FOR TA01A TCA0,TCA1: VDD=5V

25 MAY 79

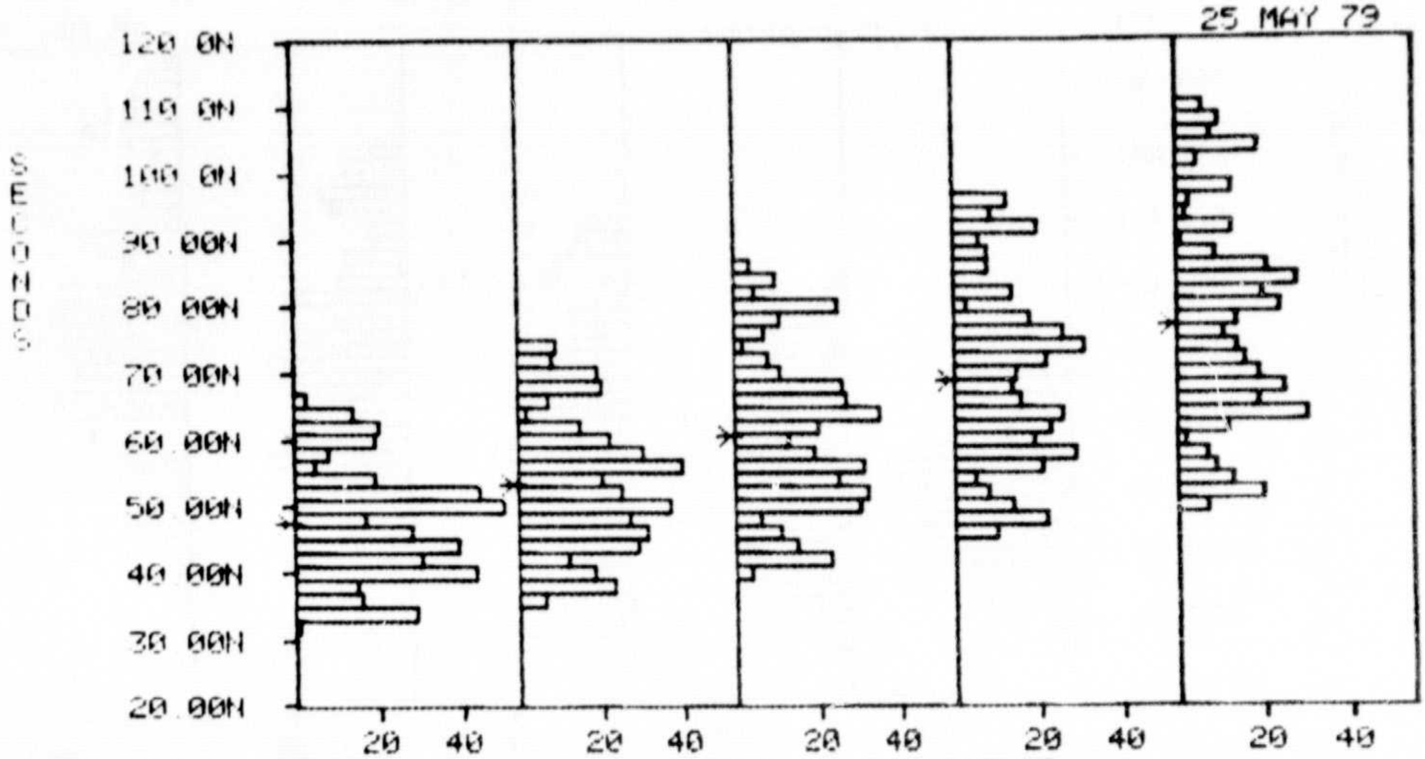


OF CELLS 50
CELL SIZE 5.000N

READINGS:	400	400	400	400	400
MAXIMUM:	160.0N	182.0N	210.0N	237.0N	263.5N
MEAN:	110.6N	125.3N	144.3N	163.7N	181.9N
MINIMUM:	71.00N	79.45N	90.60N	104.0N	114.5N
STD DEV:	23.90N	27.26N	31.44N	35.80N	40.42N

S-3260 DATA FOR TA01B TCA0,TCA1: VDD=10V

25 MAY 79

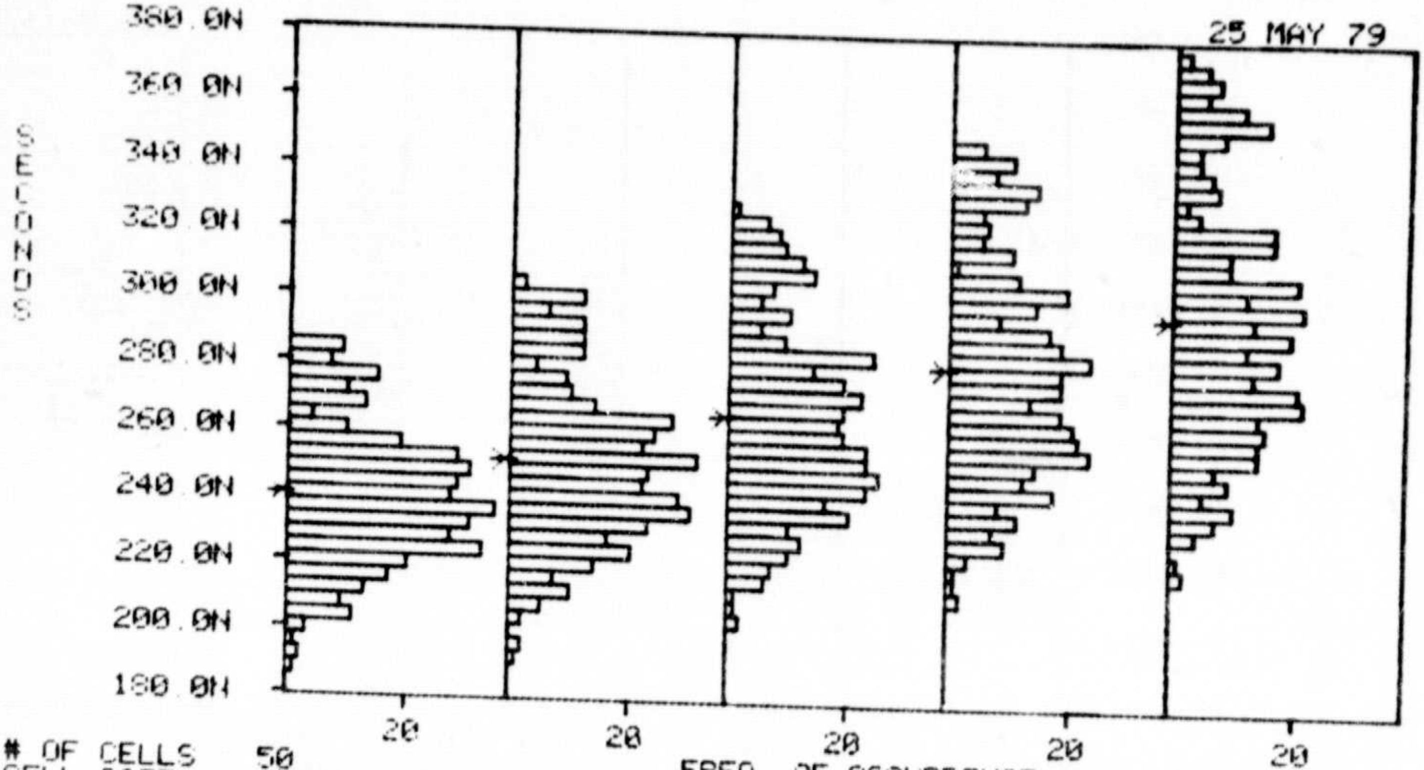


OF CELLS 50
CELL SIZE 2.000N

READINGS	400	400	400	400	400
MAXIMUM	65.50N	74.00N	85.30N	96.95N	110.0N
MEAN	47.45N	53.19N	60.59N	68.86N	76.90N
MINIMUM	32.75N	36.05N	40.50N	45.80N	50.30N
STD DEV	8.378N	9.738N	11.63N	13.59N	15.82N

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

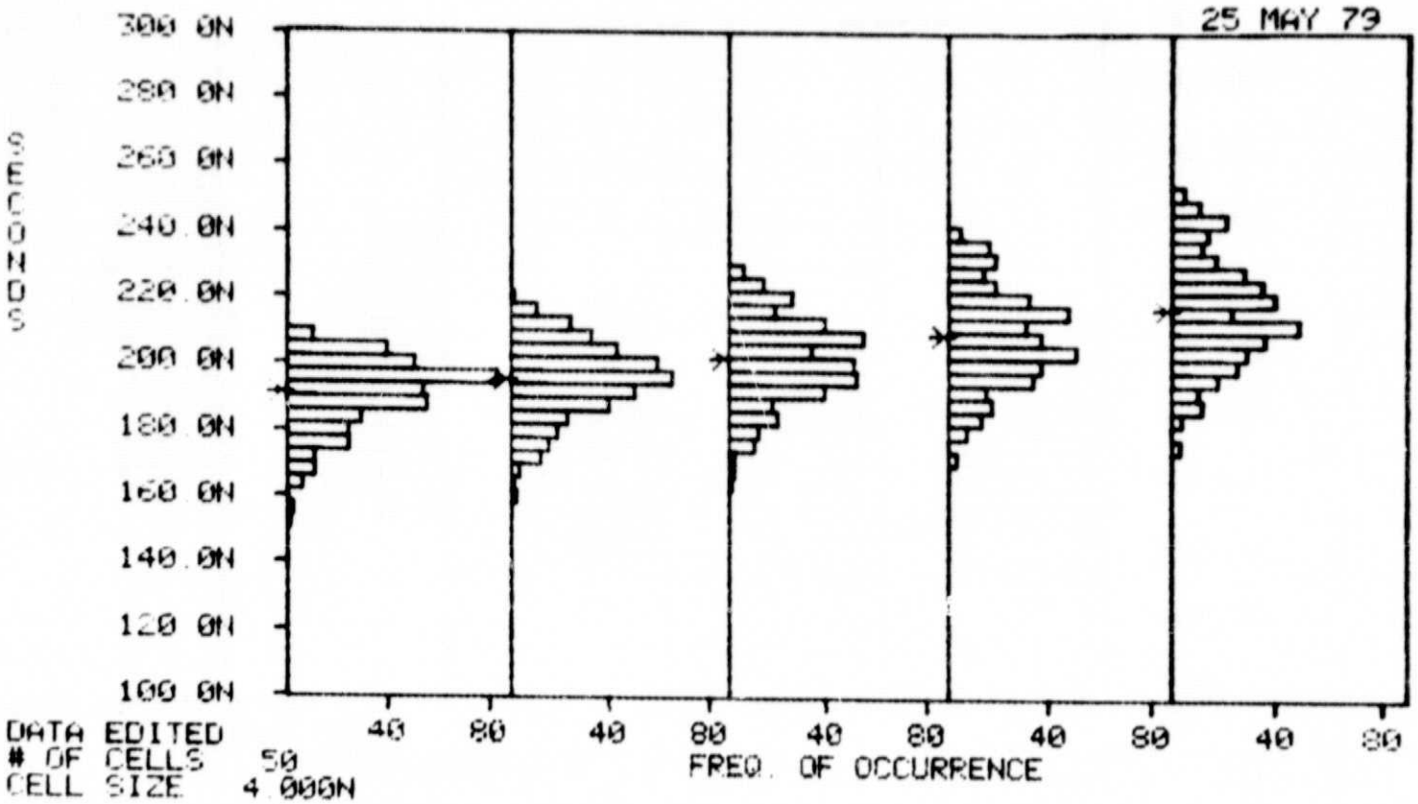
S-3260 DATA FOR TB01A TCB0,TCB1: VDD=5V



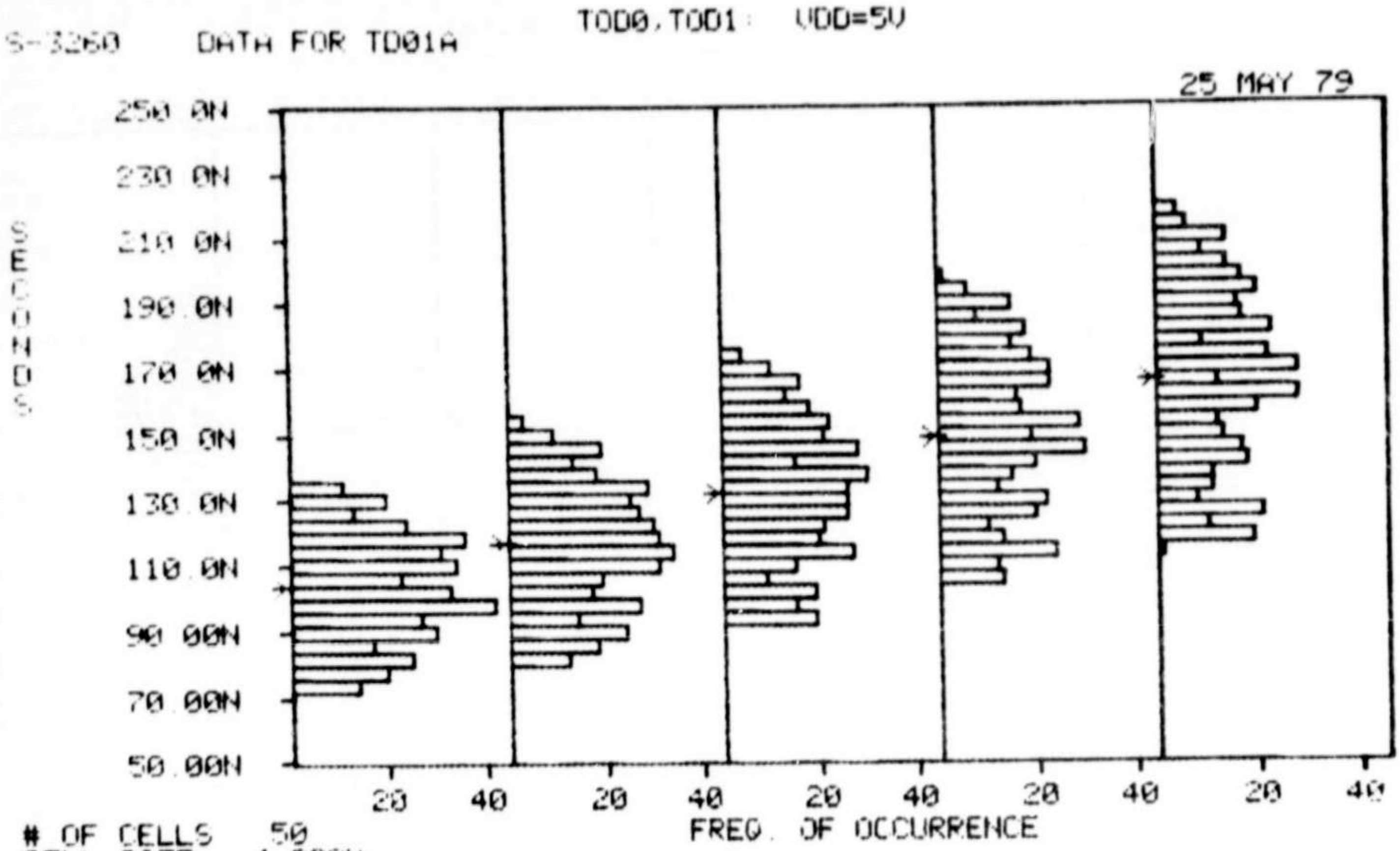
OF CELLS 50
CELL SIZE 4.000N

READINGS:	400	400	400	400	400
MAXIMUM:	295.5N	302.5N	327.0N	349.0N	376.0N
MEAN:	239.5N	251.1N	265.5N	281.2N	296.8N
MINIMUM:	188.5N	194.0N	203.0N	211.0N	219.5N
STD DEV:	20.38N	23.57N	27.90N	32.27N	36.65N

S-3260 DATA FOR TB01B TCB0,TCB1: VDD=10V



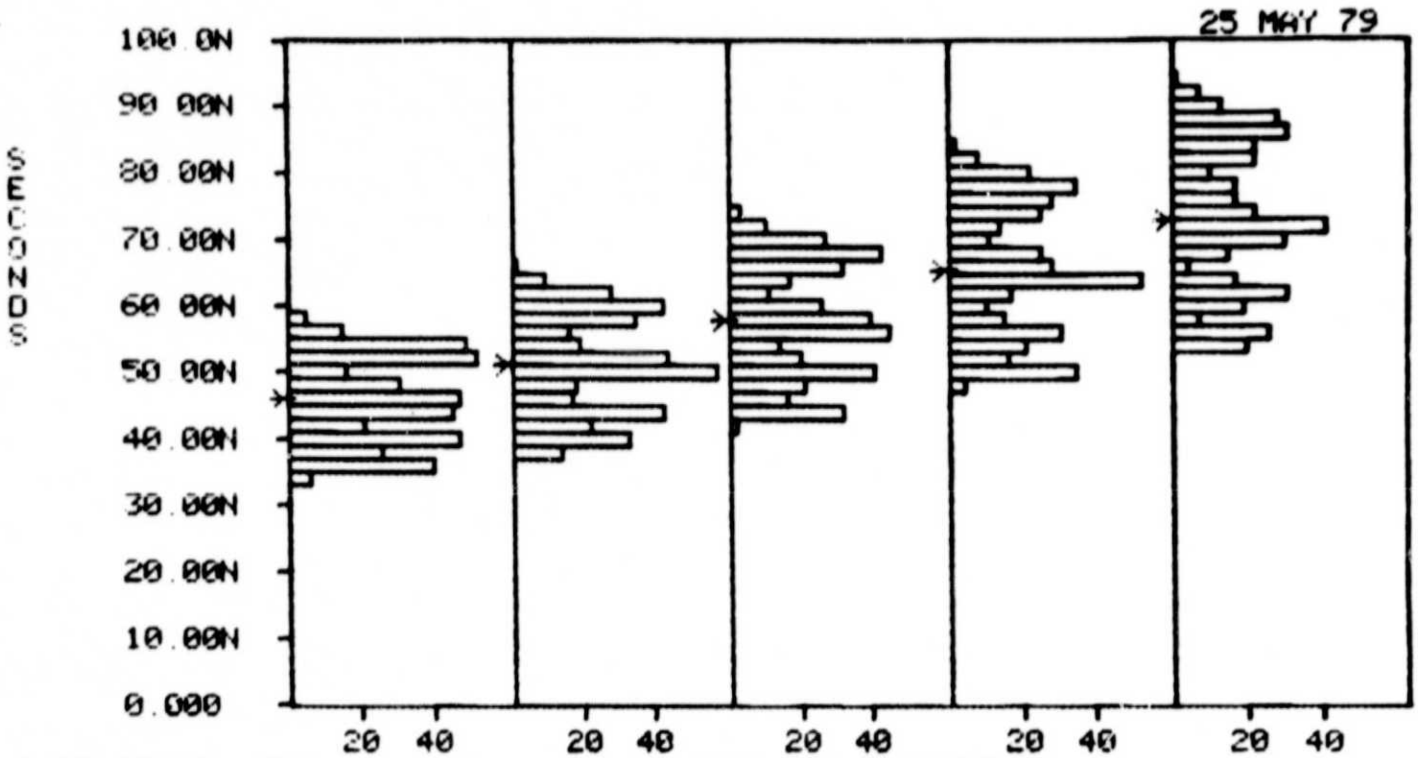
READINGS	398	400	400	398	392
MAXIMUM	209.5N	218.0N	229.5N	241.0N	253.5N
MEAN	190.7N	195.2N	201.5N	208.9N	216.6N
MINIMUM	152.5N	159.0N	165.5N	170.5N	175.5N
STD DEV	10.29N	10.82N	12.37N	14.23N	16.24N



\# OF CELLS 50
CELL SIZE 4.000N

READINGS:	400	400	400	400	400
MAXIMUM:	135.5N	153.0N	174.5N	196.5N	219.5N
MEAN:	103.6N	116.2N	132.1N	149.2N	165.9N
MINIMUM:	73.00N	81.60N	92.10N	104.5N	115.0N
STD DEV.:	16.04N	18.39N	21.22N	24.03N	27.19N

S-3260 DATA FOR TD01B TOD0,TOD1 VDD=10V



OF CELLS 50
CELL SIZE 2.000N

READINGS:	400	400	400	400	400
MAXIMUM:	58.35N	65.50N	74.45N	84.00N	94.00N
MEAN:	45.71N	51.00N	57.76N	65.38N	72.87N
MINIMUM:	33.85N	37.70N	42.80N	48.60N	53.10N
STD DEV.:	6.421N	7.403N	8.514N	9.797N	11.15N

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR