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SILICON-GATE CMOS/SOS PROCESSING

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STANDARD ABBREVIATIONS

Symbol	Definition
s	second
m	meter
l	liter
g	gram
V	volt
A	ampere
K	kelvin
Hz	hertz
cm^3	cubic centimeter
min	minute
in.	inch
mil	10^{-3} inch
C	Celsius
k	kilo, 10^3
M	mega, 10^6
c	centi, 10^{-2}
m	milli, 10^{-3}
μ	micro, 10^{-6}
n	nano, 10^{-9}

NONSTANDARD ABBREVIATIONS

Symbol	Definition
PMOS	P-channel Metal Oxide Semiconductor
IC	Integrated Circuit
MSFC	George C. Marshall Space Flight Center
NASA	National Aeronautics and Space Administration
LSI	Large Scale Integration
LSIC	Large Scale Integrated Circuit

Symbol	Definition
MSI	Medium Scale Integration
MSIC	Medium Scale Integrated Circuit
SSI	Small Scale Integration
SSIC	Small Scale Integrated Circuit
CAD	Computer Aided Design
ALU	Arithmetic Logic Unit
APARP	Automatic Placement and Routing Program
ATL	RCA Advanced Technology Laboratories
CMOS	Complementary Metal Oxide Semiconductor
DA	Design Automation
DIP	Dual In-Line Package
I^2 (I/N)	Ion Implantation (Intrinsic/N-type) Process
$2I^2$ (P/N)	Double Ion Implantation (Phosphorous/N-type) Process
I^2 (N/N)	Ion Implantation (N-type/N-type) Process
$2I^2$ (NP/N)	Double Ion Implantation (N-type and P-type/N-type) Process
LSH	Least Significant Half
MAPAR	Multiport Automatic Placement and Routing Program
MP2D	Multiport Automatic Placement and Routing Program
MOS	Metal Oxide Semiconductor
MSH	Most Significant Half
NMOS	N complement of CMOS
PR2D	Two Dimensional Placement and Routing Program
PLA	Programmed Logic Array
SOS	Silicon on Sapphire
SSTC	RCA Solid State Technology Center
SUMC	Space Ultrareliable Modular Computer
SUMC-DV	SUMC Demonstration Vehicle
SUMC-CVT	SUMC Concept Verification Test
V_{DD}	Power Supply Voltage

Section I

INTRODUCTION

This volume describes the major silicon-gate CMOS/SOS processes. Sapphire substrate preparation is also discussed, as well as each of the following process variations:

1. Double epi process

2. Ion implantation

   a. I^2(I/N) process

   b. I^2(N/N) process

   c. $2I^2$(P/N) process

   d. $2I^2$(NP/N) process

Section II

GENERAL

In the silicon-gate CMOS/SOS processing, the enhancement-mode transistors are fabricated in 0.6-μm thick isolated epi-islands of p-type and n-type single-crystal film on sapphire wafer. The epi-islands are provided by a two-step heteroepitaxial growth process or by implanting p-type and n-type dopant ions on a single-layer intrinsic epi-film. The flow diagram and cross-sectional view of the silicon-gate CMOS/SOS process are shown in Figs. 1 and 2.

The silicon is grown by the pyrolysis of silane in a multiwafer system on the face of polished sapphire substrates. The gate insulator of both devices is 1000 Å of thermally grown silicon dioxide. The polycrystalline silicon is deposited undoped by the pyrolysis of silane, and is subsequently doped using boron-doped oxide. Consequently, the silicon-gate electrodes of both n- and p-channel transistors are doped p-type. The source and drain areas are doped using boron- and phosphorus-doped oxides for the p-type and n-type transistors, respectively. The source-drain diffusion takes place in a single high-temperature step. The process is completed by opening contact holes and then evaporating approximately 1-μm thick aluminum for interconnection. A more detailed description of these processing steps is presented in Table 1.

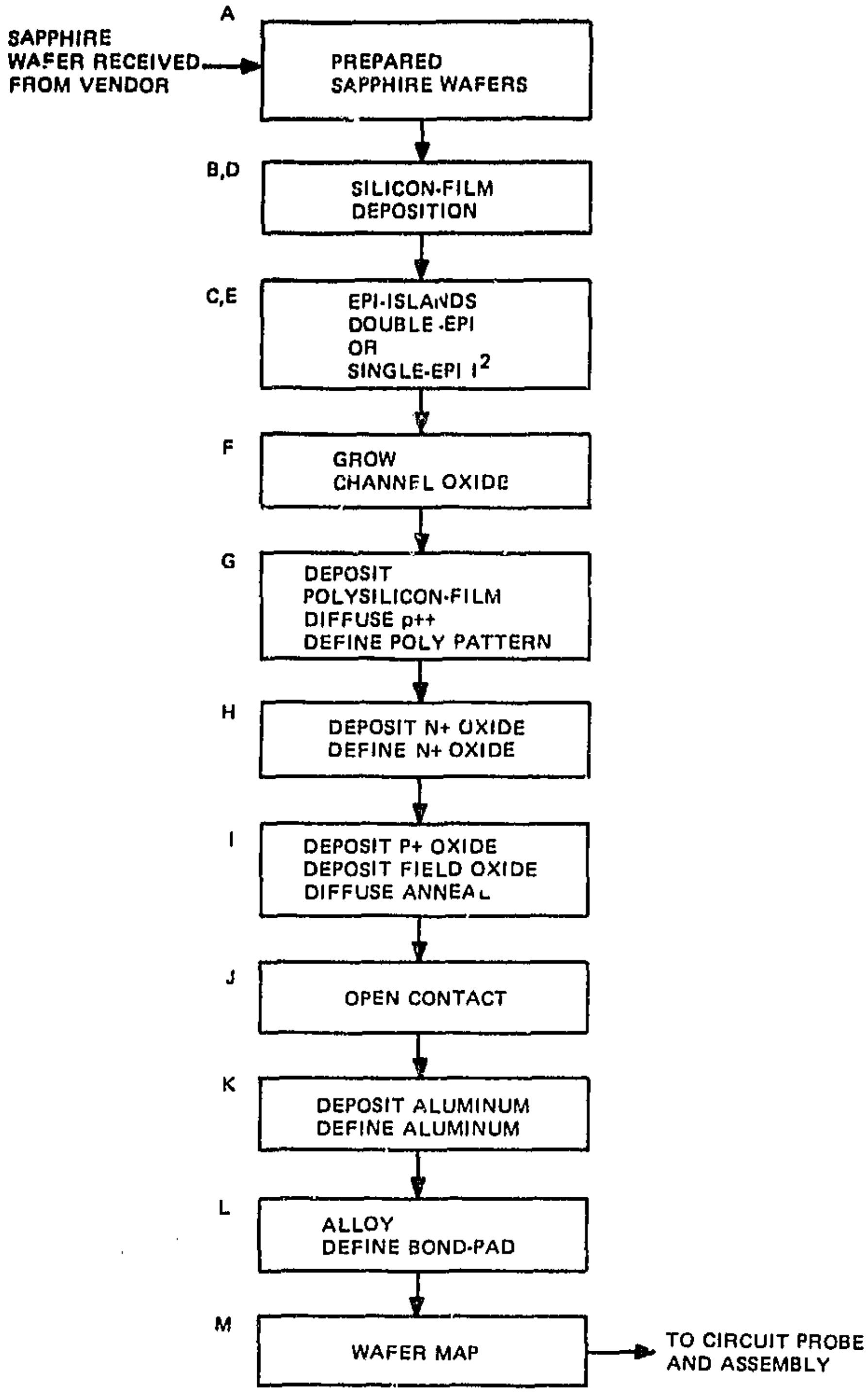


Fig. 1. Flow chart of silicon-gate CMOS/SOS process.

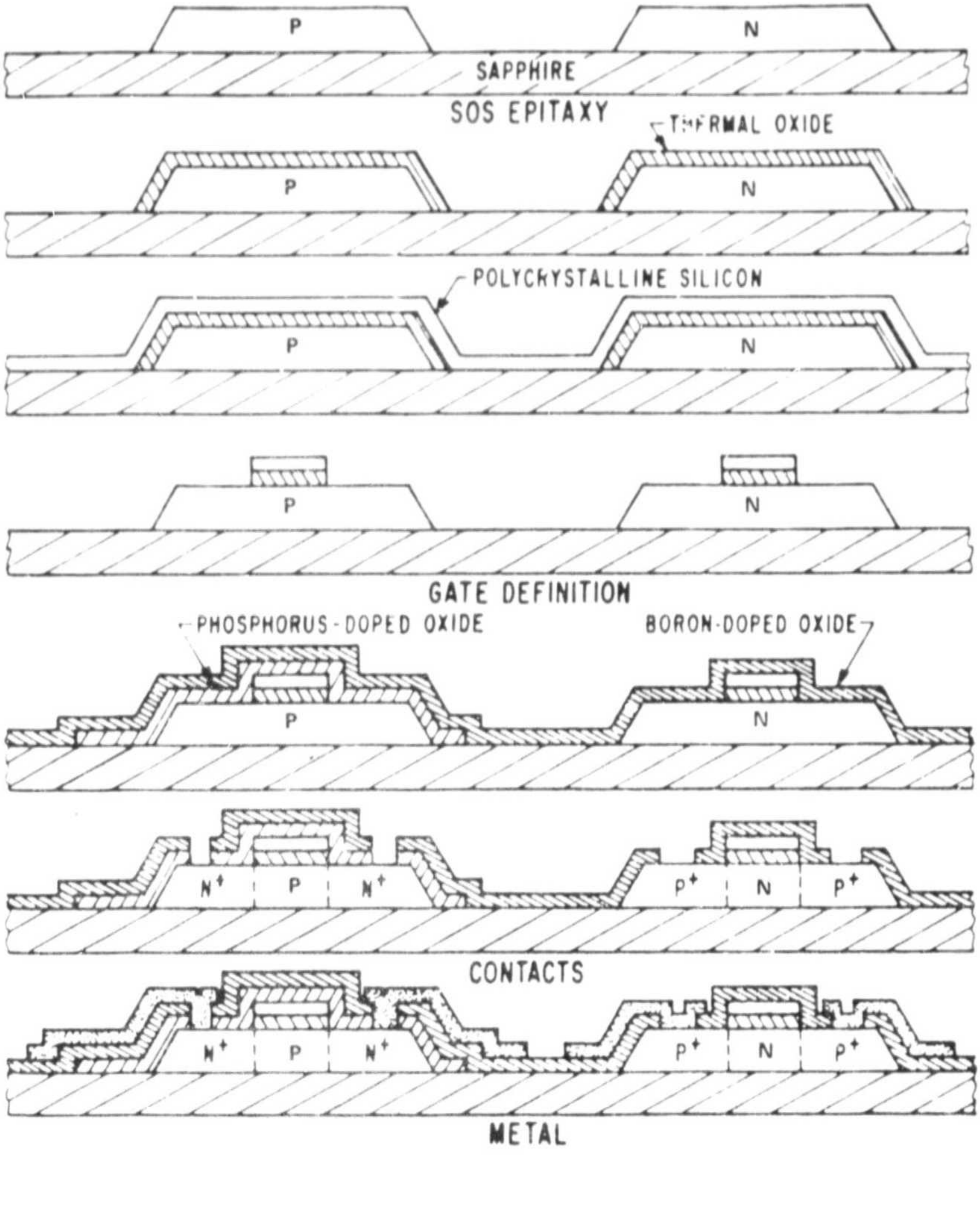


Fig. 2. Cross-sectional view of the double-epi silicon-gate CMOS/SOS process.

TABLE 1. PROCESS SEQUENCE FOR SILICON-GATE CMOS/SOS (Double-Epi Process)

- A. Sapphire Wafer
  - A1. Incoming inspection
  - A2. Sapphire clean
  - A3. Pre-deposition anneal
  - A4. Sapphire inspection
- B. Silicon-Film Deposition 1
  - B1. Deposit p-type silicon film
  - B2. Visual inspection
  - B3. Evaluate resistivity
  - B4. Measure thickness variation
- C. P-Island
  - C1. Standard clean
  - C2. Grow silicon dioxide
  - C3. Photoresist, mask #1
  - C4. Etch oxide, visual inspect
  - C5. Remove photoresist
  - C6. Etch silicon, inspect
- D. Silicon-Film Deposition 2
  - D1. Standard clean
  - D2. Deposit n-type silicon film
  - D3. Visual inspection
  - D4. Film evaluation
- E. N-Island
  - E1. Standard clean
  - E2. Grow silicon dioxide
  - E3. Photoresist, mask #2
  - E4. Etch oxide, visual inspect
  - E5. Remove photoresist
  - E6. Etch silicon, visual inspect
  - E7. Etch oxide
- F. Channel Oxide/Polysilicon Deposition
  - F1. Standard clean
  - F2. Grow channel oxide
  - F3. Deposit polysilicon
- G. Polysilicon Definition
  - G1. Standard clean
  - G2. Deposit p++ doped oxide
  - G3. Drive-in control wafer, check RS
  - G4. Photoresist, mask #3
  - G5. Etch oxide, visual inspect
  - G6. Standard clean
  - G7. Diffuse p++ into gate
  - G8. Etch oxide
  - G9. Etch silicon, visual inspect
  - G10. Etch oxide, visual inspect
- H. N+ Diffusion
  - H1. Standard clean
  - H2. Deposit n+ doped oxide
  - H3. Drive-in control wafer
  - H4. Check resistivity
  - H5. Photoresist, mask #4
  - H6. Etch oxide, visual inspect
  - H7. Remove photoresist
- I. P+ Diffusion
  - I1. Standard clean
  - I2. Deposit p+ doped oxide and field oxide
  - I3. Standard clean
  - I4. Drive-in control wafers
  - I5. Check resistivity
  - I6. Standard clean
  - I7. Diffuse
- J. Contact
  - J1. Photoresist, mask #5
  - J2. Etch oxide, visual inspect
  - J3. Remove photoresist
- K. Metallization
  - K1. Standard clean
  - K2. Deposit aluminum
  - K3. Check thickness
  - K4. C-V test
  - K5. Photoresist, mask #6
  - K6. Etch metal, visual inspect
  - K7. Remove photoresist
- L. Bond Pad
  - L1. Standard clean
  - L2. Deposit oxide
  - L3. Alloy aluminum
  - L4. Photoresist, mask #7
  - L5. Etch oxide, visual inspect
  - L6. Remove photoresist
- M. Wafer Map
- N. Circuit Probe

Section III

SAPPHIRE SUBSTRATES

The process sequence involved in the materials aspect of the fabrication of SOS devices is shown in Fig. 3. The problems associated with these steps, from a manufacturing point of view, are of varying degrees of seriousness. These problems and their solutions are discussed below.

A. INCOMING INSPECTION

The incoming sapphire substrate inspection deals almost wholly with mechanical and crystallographic parameters. This is to be contrasted with bulk silicon, where electrical properties such as carrier concentration, mobility, and lifetime are of prime importance. Sapphire is checked for surface finish and crystallographic orientation.

1. Surface Finish

This is of critical importance for epitaxial silicon quality and has a major impact on silicon resistivity control. Surface scratches will introduce various orientations of the silicon layer, thereby reducing the carrier mobility. The inspection method for surface finish which has been found to be readily applicable is a visual inspection under point-source illumination with a dark background. This has proved effective in rejecting badly scratched wafers. During the predeposition anneal, these regions are attacked more rapidly than the surrounding area. Cracks and the edge-chips are easily checked under a microscope. The surface damage due to polishing (mainly scratches which are not completely removed by a subsequent polishing) and dislocation density can be determined by an etching technique similar to the Sirtl etch technique used for bulk silicon. However, this technique is applied only on a sample basis because it is destructive.

2. Crystallographic Orientation

Single-crystal silicon of (100) orientation is obtained during epitaxy only if the substrate is oriented close to $(1\bar{1}02)$. The single-crystal silicon can be obtained with misorientation as large as 3°. The purchase specification calls for wafers to be cut within 1°, which is a realistic limit on the measurement accuracy obtainable with the simple X-ray diffraction patterns.

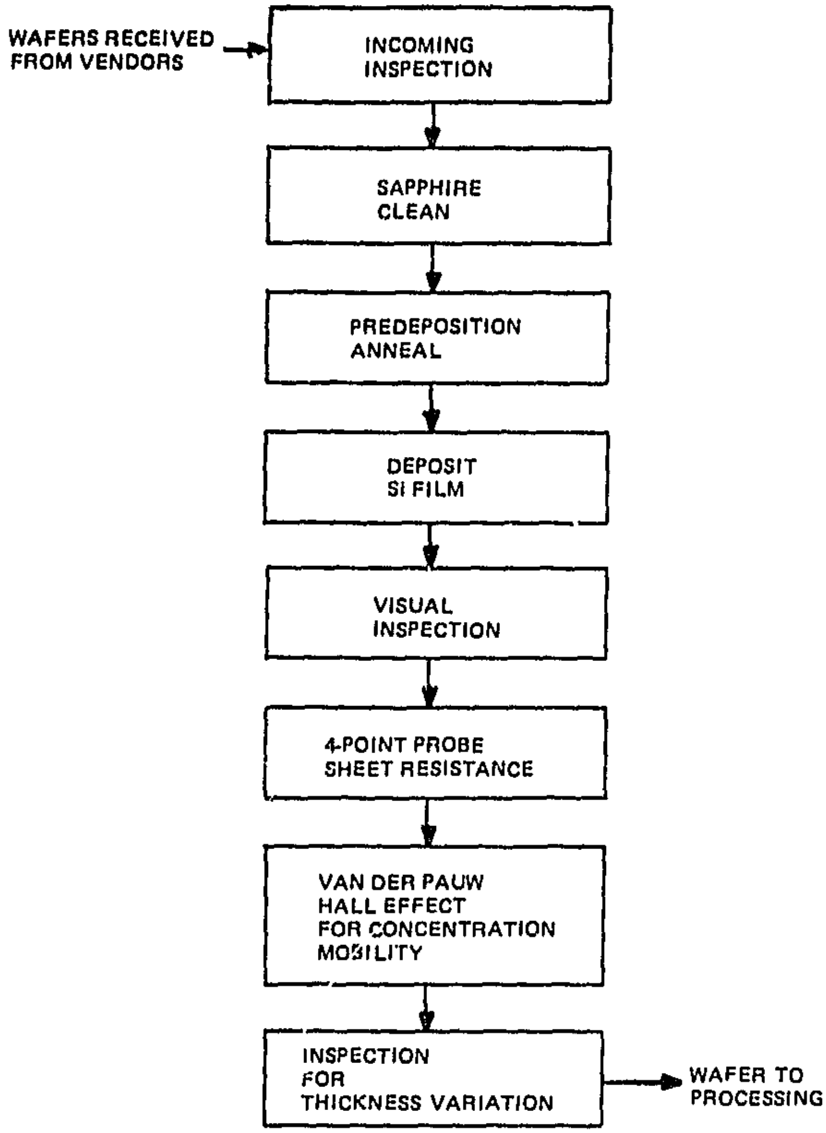


Fig. 3. Flow chart of silicon depositions on sapphire substrates.

B. CLEANING

The predeposition cleaning of the sapphire substrate is one of the most important procedures for achieving successful epitaxial growth for device fabrication. The substrates are individually scrubbed with a scrubber and followed by boiling in a standard acid cleaning solution.

C. PREDEPOSITION ANNEAL

The purpose of the anneal step is to remove the last vestiges of work damage introduced into the sapphire surface during the polishing operation. It is required because the quality of the substrate surface controls the quality of the epitaxial silicon films. Nucleation occurs preferentially on scratches, while the presence of work damage on the substrate surface presents a non-perfect lattice to the depositing atoms, resulting in films with poor crystallinity. Therefore, removal of the work damage introduced by the lapping-polishing operation is extremely important.

Section IV

SILICON EPITAXY

A. DEPOSITION

The epitaxial silicon-on-sapphire films are usually deposited in the dual chamber of the vertical AMV-1200 RF reactor in hydrogen by the pyrolysis of silane. Depositions are rigorously controlled by a mass-flow meter in the custom-design gas-control panel. The effects of gas flow on the film uniformity can be optimized by observing the interference patterns in the films using the ultraviolet light.

B. FILM EVALUATION

The silicon films are evaluated by making Van de Pauw, Hall, and resistivity measurements, all done nondestructively. These measurements appear to be reasonably reliable (within a factor of two) for the case of medium and highly doped films. For more lightly doped films, extrapolations of deposition time and/or dopant concentration in the reaction chamber are used.

On 2-1/4-inch diameter sapphire wafers, a thickness variation of ±500 Å for 0.6-μm thick silicon film is routinely obtained. If intrinsic silicon films are deposited for the ion-implantation process, the silane source should be extremely pure. It is extremely difficult to evaluate the electrical characteristics of intrinsic films.

Section V

EPI-ISLAND PREPARATION

The silicon-gate CMOS/SOS "standard" process requires two epi-islands (n-channel and p-channel). The range of the impurity concentrations of epi-film islands are 1.0×10^{14} to 5×10^{15} cm^{-3} of boron and phosphorus. The islands can be prepared in two ways: two-step epi-deposition with in-situ doping (double-epi process) and one-step epi-deposition with ion-implantation (I^2 process). Extremely careful doping control is needed in the double-epi process, because the doping levels are very light and the circuit performance is critically dependent upon them. One advantage of applying ion implantation to the CMOS/SOS process is that the very light epitaxial doping is uniform across the wafer and reproducible from run to run. Several other important advantages of ion-implantation are: (1) It requires only one epitaxial film growth. The film can be intrinsic and requires no impurity doping during the deposition cycle. Therefore, the same starting SOS wafers can be used for various processes; (2) Both n- and p-islands can be defined with one mask, thereby eliminating a critical photoresist and etching step and allowing closer spacing of the islands.

A. DOUBLE-EPI PROCESS

The double-epi process requires two successive epitaxial depositions (p- and n-type) and two photoresist and etching steps to define epi-islands. Figure 4 outlines the processing sequence for preparing the epi-islands. A more detailed description of the preparation of epi-islands can be found in Table 1.

B. ION-IMPLANTATION PROCESS

Following the writing of the original text of this report, the single-epi single-ion-implant self-aligned silicon-gate CMOS/SOS process (called the I^2 (N/N) process) has become the primary one used by the RCA Solid State Technology Center. For completeness, the two basic ion-implanting techniques (single, I^2, and double, $2I^2$, implanting) will be described. However, special attention will be given to the I^2(N/N) process description.

The intrinsic SOS film is grown in the standard manner with no additional doping. A thermal oxide is grown and is etched using a single mask to form the device islands for both n- and p-channel transistors. The epi-islands are etched, using the thermal oxides as an etch mask. One island is shielded from implanting ions by a photoresist film. By selecting a proper shield-mask (or well-mask) and ion species, various combinations of processes are possible. The n-channel island may be left intrinsic (I), implanted

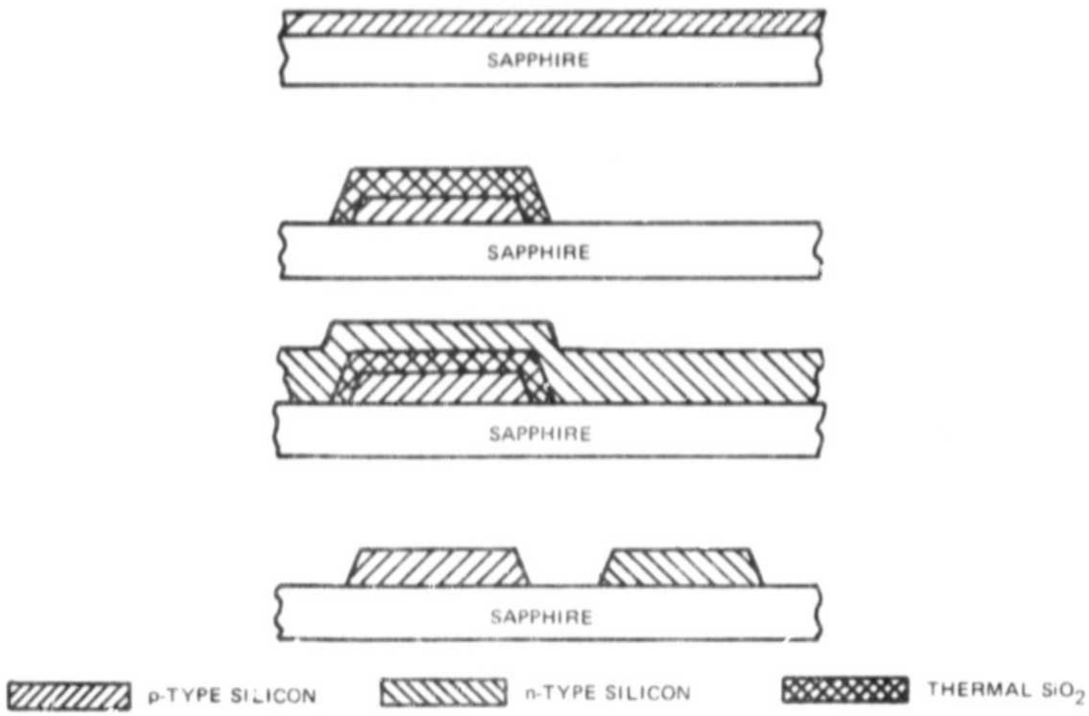


Fig. 4. Epi-island preparation using double-epi process. The processing sequence for preparing the p-type and n-type silicon islands is shown.

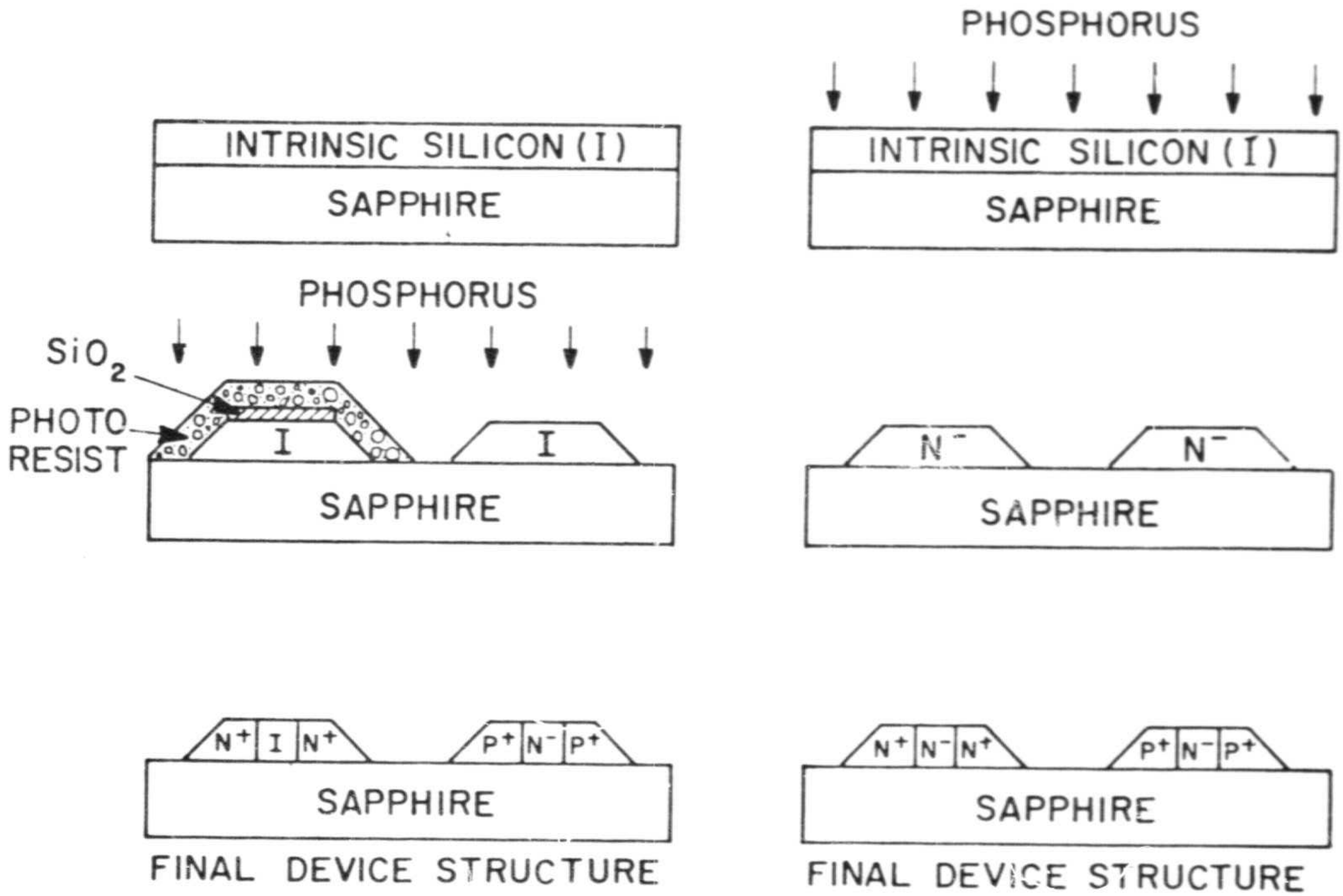
with p-type ions (P), or implanted with n-type ions and then compensated with p-type ions (NP), resulting in net p-type. A similar implantation scheme is applied to the p-channel island.

Two basic approaches that utilize the ion implanting technique are the single ion-implant ($1I^2$ or I^2) and double ion-implant ($2I^2$). Both approaches are possible alternatives to the double-epi process. The four processes most routinely using ion-implantation are I^2(I/N), I^2(N/N), $2I^2$(P/N), and $2I^2$(NP/N). The cross-sectional views of the above four processes are shown in Figs. 5 and 6.

1. I^2(I/N) Process

The intrinsic SOS film is grown and an implant-photoresist step is followed by the definition of epi-islands. In the implant-photoresist step, the oxide etching on the p-channel island is followed by an ion implantation step using phosphorus as the dopant. The oxide and photoresist films left on the n-channel island are used to shield the phosphorus ions. See Fig. 5a. After stripping the photoresist and removing the oxide, the 1000 Å channel oxide is grown. At this point, the n-channel is intrinsic (I) and the p-channel island is n-type (N). Therefore, the single implant process is named I^2(I/N) process.

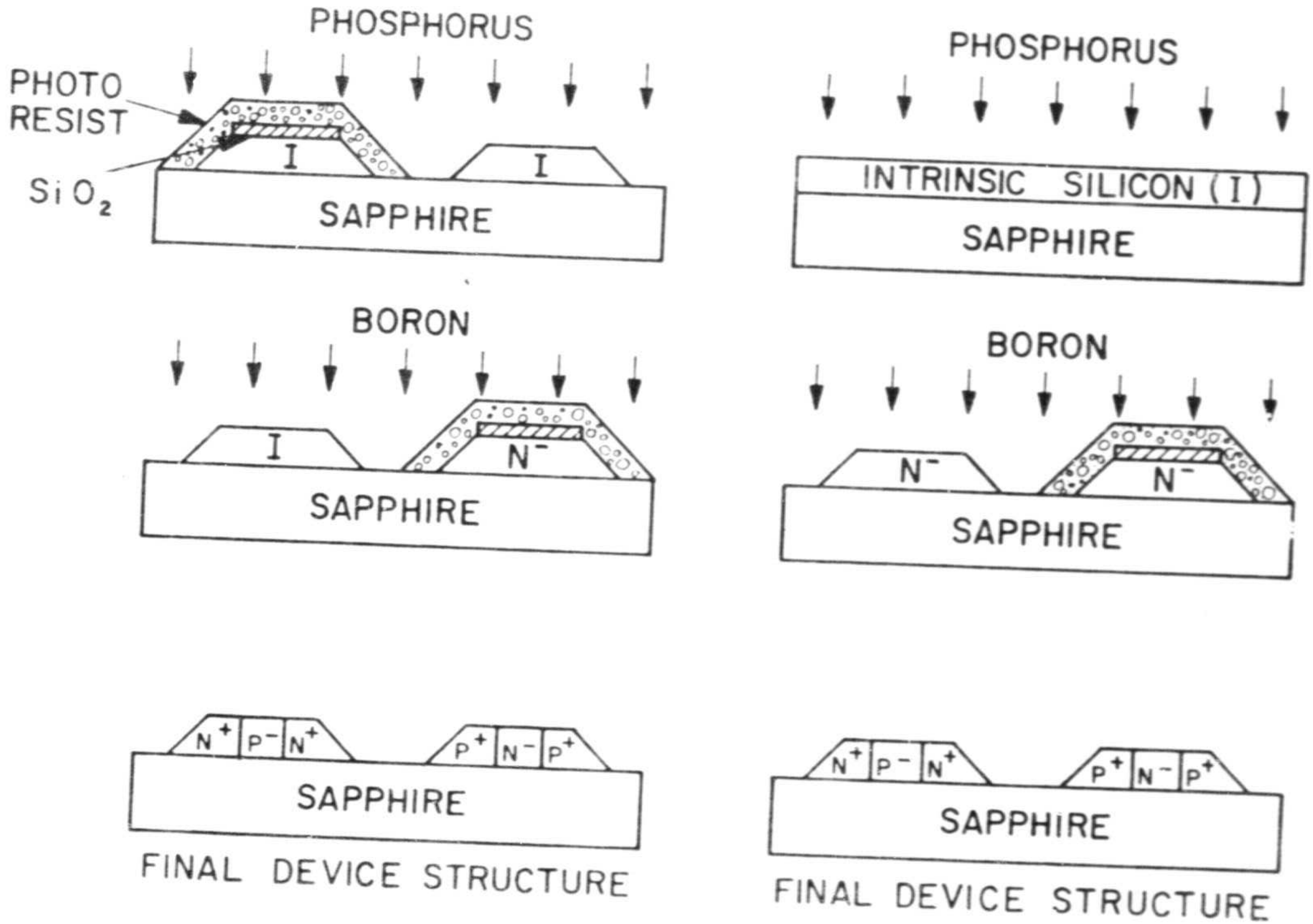
Next the standard process is applied to complete the device fabrication. See Table 1.



(a) I^2 (I/N) Process

(b) I^2 (N/N) Process

Fig. 5. Single ion implantation process.



(a) $2I^2$ (P/N) Process

(b) $2I^2$ (NP/N) Process

Fig. 6. Double ion implantation process.

2. I^2(N/N) Process

The above mentioned single ion implanted I^2(I/N) process is satisfactory for low-voltage circuits. However, it takes two photoresist steps: (1) Define the islands for the n and p transistors, and (2) Define and separate the n-transistors from the phosphorus implant. A single photoresist step can be used either (a) By implanting phosphorus over the entire surface of the intrinsic film and then defining the epi-islands or (b) By defining the intrinsic islands and then implanting the phosphorus. Figure 5b illustrates approach (a). With either approach, both islands have identical concentrations and are the same type (N/N).

A single-epi single-ion-implant self-aligned silicon-gate CMOS/SOS process, (called the I^2(N/N) process) is the primary one used by the RCA Solid State Technology Center. This process requires only six photolithographic steps:

Mask No.	Description
1	Both Islands
2	Polysilicon
3	N^+ Diffusion
4	Contact Opening
5	Aluminum
6	Protective Layer

The enhancement-mode transistors are fabricated in 0.6 ±0.1 μm thick isolated silicon epi-islands. The epi-islands are prepared by single-ion implantation with phosphorus on intrinsic epi-film. The flow diagram for this process is covered in Fig. 1. A cross-sectional view of the I^2(N/N) process is shown in Fig. 7.

The silicon is grown by the pyrolysis of silane (SiH_4) on the face of polished ($1\bar{1}02$) sapphire substrates. Phosphorus (n-type) is implanted over the entire surface of intrinsic film. The implantation condition is:

Source: phosphorus

Energy: 150 keV

Dose: $1.4 \times 10^{11}/cm^2$

Both islands are then defined by a single photolithographic step. With this approach both islands have identical concentration and are of the same type.

Even though the substrate of the n-transistor is n-type, circuitwise it is an enhancement-mode device due to the work function of the p^+ polysilicon gate.

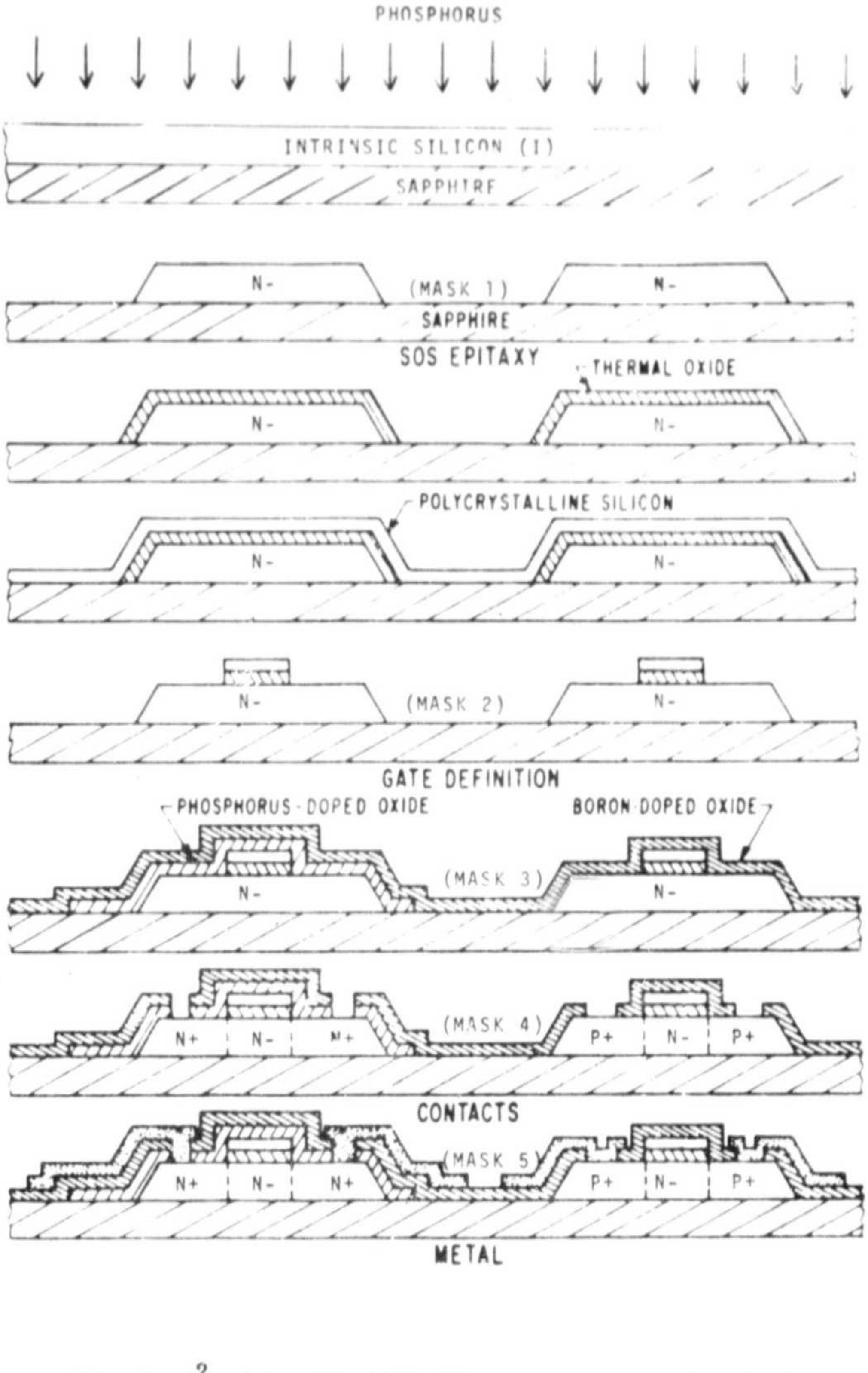


Fig. 7. I^2(N/N) CMOS/SOS silicon-gate process flowchart.

The gate insulator of both devices is 1100 Å ±5 Å of thermally grown silicon dioxide. The 5000 Å ±500 Å of polysilicon is deposited undoped by the pyrolysis of silane, and is subsequently doped using boron-doped oxide. Consequently, the silicon-gate electrodes of both n- and p-channel transistors are doped p-type. The source and drain areas are doped using boron- and phosphorus-doped oxides for the p-type and n-type transistors, respectively. The source-drain diffusion takes place in a single high-temperature step. The process is completed by opening contact holes and then evaporating 1.2 ± 0.2 μm thick aluminum for interconnection. A more detailed description of these processing steps is presented in Table 2, and an actual lot card is presented in Fig. 8.

3. $2I^2$(P/N) Process

The single implantation (I^2) processes described previously are essentially low-threshold-voltage processes. To increase both the temperature range and radiation resistance, it is desirable to increase the threshold voltage of n-transistors. This can be achieved by a double implant process ($2I^2$).

The same intrinsic SOS films can be used for a double implant process; i.e., both epi-islands are etched using the same photoresist step during the phosphorus ion implant operation. Similarly, p-transistor islands are shielded, using a third photoresist step, from the boron ion implant operation. The photoresist and oxide are removed, and the "standard" processing continues. Figure 5a illustrates this approach.

The standard process is applied to complete the process.

4. $2I^2$(NP/N) Process

The above mentioned $2I^2$(P/N) process gives the best control over both channels; however, it requires three photoresist steps to prepare the epi-island. One photoresist step can be eliminated by implanting phosphorus over the entire surface of the SOS wafer, defining the islands, and then implanting boron on n-transistor islands by shielding the p-channel islands with photoresist. See Fig. 6b. The n-transistor islands are exposed to two implantations, n-type and p-type (NP), resulting in a net p-type imparity.

The standard process is applied to complete the process.

TABLE 2. PROCESS SEQUENCE OF SILICON-GATE CMOS/SOS I^2(N/N) PROCESS

A. Sapphire Wafer
   1. Incoming inspection
   2. Sapphire clean
   3. Pre-deposition anneal
   4. Sapphire inspection

B. Silicon-Film Deposition
   1. Deposit intrinsic silicon film (0.6 μm =0.1 μm)
   2. Visual inspection
   3. Evaluate resistivity
   4. Measure thickness variation

C. Phosphorus Implantation
   1. Implant phosphorus
   2. E = 150 keV, Dose = 1.4×10^{11} ions/cm^2

D. Both Islands
   1. Standard clean
   2. Grow silicon dioxide (15 min steam at 940°C)
   3. Photoresist mask #1
   4. Etch oxide, visual inspection
   5. Remove photoresist
   6. Etch silicon (KOH-alcohol), visual inspection
   7. Etch oxide (5 min Buff-HF)

E. Channel Oxide/Polysilicon Deposition
   1. Standard clean
   2. Grow channel oxide (25-30 min HCl-steam at 940°C)
   3. Deposit polysilicon (5000 Å ±500 Å)

F. Polysilicon Diffusion/Definition
   1. Standard clean
   2. Deposit p^{++} doped oxide (800 Å ±50 Å)
   3. Deposit cap oxide (2000 Å ±200 Å)
   4. Drive-in control wafer (15 min N_2 at 1050°C)
   5. Check Rs
   6. Photoresist mask #2
   7. Etch oxide (Buff-HF), visual inspection
   8. Standard clean
   9. Diffuse p^{++} into gate (15 min N_2 at 1050°C)
   10. Etch oxide (1 min HF)
   11. Etch silicon (KOH-alcohol), visual inspection
   12. Etch oxide, visual inspection

TABLE 2. PROCESS SEQUENCE OF SILICON-GATE CMOS/SOS I^2(N/N) PROCESS (cont.)

G. n^+ Diffusion
 1. Standard clean
 2. Deposit n^+ doped oxide (500 Å ±50 Å)
 3. Deposit cap oxide (1200 Å ±100 Å)
 4. Drive-in control wafer (15 min N_2 at 1050°C)
 5. Check Rs
 6. Photoresist mask #3
 7. Etch oxide (Buff-HF), visual inspection
 8. Remove photoresist

H. p^+ Diffusion
 1. Standard clean
 2. Deposit p^+ doped oxide (1000 Å ±100 Å)
 3. Deposit field oxide (6000 Å ±500 Å)
 4. Standard clean
 5. Drive-in control wafers (15 min N_2 at 1050°C)
 6. Check Rs
 7. Standard clean
 8. Diffuse (15 min N_2 at 1050°C)

I. Contact
 1. Photoresist mask #4
 2. Etch oxide (Buff-HF), visual inspection
 3. Remove photoresist

J. Metallization
 1. Pre-metal clean
  Standard clean, 50:1 (H_2O:HF) dip
 2. Deposit aluminum (1.2 μm ±0.2 μm)
 3. Check thickness
 4. C-V test
 5. Photoresist mask #5
 6. Etch metal, visual inspection
 7. Remove photoresist

K. Bond Pad
 1. Standard clean
 2. Deposit protective oxide (6000 Å ±500 Å)
 3. Alloy aluminum (15 min FG at 450°C)
 4. Photoresist mask #6
 5. Etch oxide (Buff-HF, HAC), visual inspection
 6. Remove photoresist

L. Wafer Map

M. Circuit Probe

Silicon Gate CMOS/SOS Process Type ________ Lot No. ________

WO No. I^2 (N/N)

Step	Operation	Date	Init	No. of Waf	Conditions	Comments
1	Silicon Epi Phos. Implant				0.6± 0.1 μ	
2	Standard Clean (Control-C2)					
3	Oxidize (C2)				940°C Stm. 15 min.	
4	Islands Mask No. 1 Photoresist Islands					
5	Buffer Etch (Strip C_2)					
6	Silicon Etch—Alcohol / KOH					
7	SiO_2 Etch – Buff HF				5 Min.	

Quality Control MRB No. Insp. Date
Accept: ________ Defect: ________
N.S.Q.
Cause: ________
Disposition: ________
Follow Up ________
Comments ________ By: Eng. ________
Q.A. ________

Step	Operation	Date	Init	No. of Waf	Conditions	Comments
8	Stand Clean (N_1,N_2,N_3,N_4,N_5)					
9	Thermal Oxidation (N_1,N_2,N_3,N_4,N_5)				940°C-HCL Stm.25-30min.	
10	Poly Silicon (N_1,N_2,N_4)				5000± 500 Å	

Quality Control MRB No. Insp. Date
Accept: ________ Defect: ________
N.S.Q.:
Cause ________
Disposition ________
Follow Up ________
Comments ________ By: Eng. ________
Q.A. ________

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I^2 (N/N) Type ________ Lot No. ________

Step	Operation	Date	Init	No. of Waf	Conditions	Comments
11	Scrub Wafers					
12	Standard Clean (N_1,N_2,N_6,N_7)					
13	P_{++} Silane Oxide (N_1,N_2,N_6,N_7)				800/2200± 50 Å	
14	Diffuse Controls (N_1,N_6)				1050°C–N_2 15 min.	R_s (N_1Y) R_s (N_6)
15	Scrub Wafers					
16	Poly Silicon Mask No. 2 Photoresist Poly Silicon					
17	Buffer Etch (Strip N_7)					
18	Standard Clean (N_2)					
19	Diffuse Poly (N_2)				1050°C N_2 15min.	R_s (N_2Y)
20	SiO_2 Etch—HF				1 min.	
21	Poly Silicon Etch-Alcohol / KOH					

Quality Control MRB No. Insp. Date
Accept: ________ Defect: ________
N.S.Q.:
Cause ________
Disposition ________
Follow Up ________
Comments ________ By: Eng. ________
Q.A. ________

Step	Operation	Date	Init	No. of Waf	Conditions	Comments
22	Buffer Etch N_3					
23	Standard Clean (P_1,P_2,P_3,P_4)					
24	50:1 HF DIP				15 sec.	
25	Deposit N^+ Silane Oxide (P_1,P_2,P_3,P_4)				1200/800± 50 Å	
26	Diffuse Control P_1,P_4				1050°C–N_2 15 min.	R_s (P_1) R_s (N_4Y)
27	Scrub Wafers					
28	N Photoresist Mask No. 3 Photoresist N^+					
29	Buffer Etch – 50:1 (P_2)					
30	Strip Photorsist					

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Fig. 8. Lot card for silicon-gate CMOS/SOS I^2(N/N) process. (sheet 1 of 2)

I^2 (N/N) Type ____ Lot No. ____

Step	Operation	Date	Init	No. of Waf	Conditions	Comments
Quality Control	MRB No.		Insp.		Date	
Accept: ____	Defect: ____					
N.S.Q.: ____						
Cause ____						
Disposition ____						
Follow Up ____						
Comments ____			By:		Eng. ____	
					Q.A. ____	
31	Standard Clean (N_8,N_9,P_3)					
32	Deposit P^+ Silane Oxide (N_8,N_9,P_3)				1000 ± 100 Å	
33	Deposit Silane Oxide (N_8,N_9,P_3)				6000 ± 500 Å	
34	Scrub Wafers					
35	Diffuse Control N_8				1050°C—N_2 15 min	R_s (N_8)
36	Standard Clean					
37	Diffuse — Anneal (N_9,P_3)				1050°C — N_2 15 min.	
38	Oxidize				340°C — Sim. 15 min.	
39	Anneal (N_9,P_3)				500°C—F.G. 15 min.	R_s (N_9)
40	Contact Metal Mask No. 4 Photoresist Contacts					
41	Etch SiO_2 (P_3)					
Quality Control	MRB No.		Insp.		Date	
Accept: ____	Defect: ____					
N.S.Q.: ____						
Cause ____						
Disposition ____						
Follow Up ____						
Comments ____			By:		Eng. ____	
					Q.A. ____	

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I^2 (N/N) Type ____ Lot No. ____

Step	Operations	Date	Init	No. of Waf	Conditions	Comments
42	Standard Clean (N_5)					
43	50:1 HF DIP				15 sec	
44	Deposit Aluminum (N_5)				1.2 ± 0.2 μ	CV
45	Metal Definition Mask No. 5 Photoresist Metal					
46	Metal Etch / Chem.—Strip					
Quality Control	MRB No.		Insp.		Date	
Accept: ____	Defect: ____					
N.S.Q.: ____						
Cause ____						
Disposition ____						
Follow Up ____						
Comments ____			By:		Eng. ____	
					Q.A. ____	
47	Alloy				450°C—F.G. 15Min	
48	Deposit Silane (Control C3)				6000±500 Å	
49	Bond Pads: Mask No. 6 Photoresist Pads					
50	Buffer Etch—HAC (Strip C3)					
51	Strip—Chem. Strip					
Quality Control	MRB No.		Insp.		Date	
Accept: ____	Defect: ____					
N.S.Q.: ____						
Cause ____						
Disposition ____						
Follow Up ____						
Comments ____			By:		Eng. ____	
					Q.A. ____	
52	Wafer Mapping					

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Fig. 8. Lot card for silicon-gate CMOS/SOS I^2(N/N) process. (sheet 2 of 2)

Section VI

CONCLUSION

The major silicon-gate CMOS/SOS processes available at the RCA Solid State Technology Center have been described. It was noted that since the time of the original writing of this report the single-epi, single-ion-implant, self-aligned silicon-gate CMOS/SOS process (called the $I^2(N/N)$ process) has become the primary one used by the RCA Solid State Technology Center.

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