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EXPANSION OF CMOS ARRAY DESIGN TECHNIQUES

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FOREWORD

This report is the final technical report on NASA contract NAS8-31325, which was performed under the direction of John Gould, Technical Program Director.

This report discusses various aspects of the CMOS/SOS high speed standard cell circuit family, validation of the CMOS/SOS circuits, circuit simulation techniques, and improvement of the Double-Entry (Multiport) Automatic Placement and Routing Program.

Several self-aligned silicon gate CMOS/SOS processes are described in a separate report, "Silicon-Gate CMOS/SOS Processing," which was prepared under the same contract.

The design rules for the self-aligned silicon gate CMOS/SOS process are described in another report, "Design Rules for RCA Self-Aligned Silicon Gate CMOS/SOS Process," also prepared under the same contract.

The device model used in the FETSIM circuit simulation program is described in still another report, "Device Model for FETSIM Circuit Simulation Program," also prepared under contract NAS8-31325.

ACKNOWLEDGMENTS

The authors wish to acknowledge other members of the RCA Advanced Technology Laboratories in Camden, N. J., who made significant contributions to this program. Included are: Mr. R. Noto, developer of the PR2D and MP2D Automatic Placement and Routing Computer programs, who made the additional improvements in the Double-Entry MP2D program delivered to NASA on this contract; Mr. A. Smith, Mr. T. Lombardi, Mr. R. Pryor, and Mr. R. Lisowski, who contributed to most of the other tasks successfully accomplished during this program; Mr. F. Bertino and Mr. J. DeLuca, who efficiently performed their responsibility in translating the cell designs to verified topological layouts, and in preparing the various magnetic tapes containing circuit and program information; Mr. W. Zlupko for his laboratory verification of chips containing many of the cells included in the delivered cell family.

The authors gratefully acknowledge and express their appreciation to the following members of the Solid State Technology Center (SSTC) in Somerville for their cooperation, consultation, materials information and services relating to the various aspects of the CMOS/SOS process reported herein. They include, but are not limited to, Messrs. H. Borkan, J. Fabula, D. Woo and S. Policastro.

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STANDARD ABBREVIATIONS

Symbol	Definition
s	second
m	meter
l	liter
g	gram
V	volt
A	ampere
K	kelvin
Hz	hertz
cm^3	cubic centimeter
min	minute
in.	inch
mil	10^{-3}
C	Celsius
k	kilo, 10^3
M	mega, 10^6
c	centi, 10^{-2}
m	milli, 10^{-3}
μ	micro, 10^{-6}
n	nano, 10^{-9}

NONSTANDARD ABBREVIATIONS

Symbol	Definition
PMOS	P-channel metal oxide semiconductor
IC	Integrated circuit
MSFC	George C. Marshall Space Flight Center
NASA	National Aeronautics and Space Administration
LSI	Large scale integration

NONSTANDARD ABBREVIATIONS (Continued)

Symbol	Definition
LSIC	Large Scale Integrated Circuit
MSI	Medium Scale Integration
MSIC	Medium Scale Integrated Circuit
SSI	Small Scale Integration
SSIC	Small Scale Integrated Circuit
CAD	Computer Aided Design
ALU	Arithmetic Logic Unit
APARP	Automatic Placement and Routing Program
ATL	RCA Advanced Technology Laboratories
CMOS	Complementary Metal Oxide Semiconductor
DA	Design Automation
DIP	Dual In-Line Package
I^2 (I/N)	Ion Implantation (Intrinsic/N-type) Process
$2I^2$ (P/N)	Double Ion Implantation (Phosphorous/N-type) Process
I^2 (N/N)	Ion Implantation (N-type/N-type) Process
$2I^2$ (NP/N)	Double Ion Implantation (N-type and P-type/N-type) Process
LSH	Least Significant Half
MAPAR	Multiport Automatic Placement and Routing Program
MP2D	Multiport Automatic Placement and Routing Program
MOS	Metal Oxide Semiconductor
MSH	Most Significant Half
NMOS	N Complement of CMOS
PR2D	Two-Dimensional Automatic Placement and Routing Program
PLA	Programmed Logic Array
SOS	Silicon on Sapphire
SSTC	RCA Solid State Technology Center
SUMC	Space Ultrareliable Modular Computer

NONSTANDARD ABBREVIATIONS (Concluded)

Symbol	Definition
SUMC-DV	SUMC Demonstration Vehicle
SUMC-CVT	SUMC Concept Verification Test
V_{DD}	Power Supply Voltage

Section I

INTRODUCTION

Over the past several years, the RCA Advanced Technology Laboratories (ATL) has developed a design automation (DA) technique for MOS LSI arrays. The method is particularly well-suited for those designs requiring only a modest production, and where the initial nonrecurring costs must be minimal and short design cycles are important. The approach has been developed under various NASA programs (SUMC-DV and SUMC-CVT), those of other government agencies, and RCA Independent Research and Development funding.

The DA technique consists of a series of computer programs, Standard Cell library tapes, and a series of user manuals. This report deals with the expansion of this system. The updating of the capability of the placement and routing (PR2D) program to process double-ended (or Multiport) SOS, high-speed cells is also covered; test cases are discussed. Finally, the extended, high-speed, SOS standard cell notebook and cell library are introduced.

Section II

TECHNICAL APPROACH

A. GENERAL

The principal objective of this program is to provide NASA with a significantly improved standard cell design automation (DA) capability for the metal gate and silicon gate CMOS/SOS technology. The basic approach to satisfy these objectives can be described as follows:

- Updating the two-dimensional placement and routing (PR2D) program(s) for single ended cells with the above technologies.
- Extending the PR2D programs capability to process double-ended (or Multiport) cell equivalents of the high-speed SOS standard cell family.
- Updating circuit type file and cell library tapes to include new cell designs.
- Extending and updating the Standard Cell Notebook and cell characterization data for the high-speed SOS standard cell family.
- Updating documentation relevant to the SOS process in the areas of topology design rules, processing parameters for cell characterization, and transistor modeling.

1. Enhanced Automatic Placement and Routing Program for Standard Cells

a. Single Entry Automatic Placement and Routing Program (PR2D)

The Single Entry Automatic Placement and Routing Program (PR2D) is the basic program for generating low-cost, quick-turnaround, random logic, custom LSI arrays using the standard cell approach with the CMOS technology and any one of its variants including CMOS/SOS. This program, originally developed with NASA support in 1969 for the CMOS bulk silicon technology, has been in a continual state of growth since then. The computer program has grown in two ways. It has grown substantially in its intrinsic capability, as several examples in the technical discussion will show, and it has been extended to cover several technologies and various standard-cell families in each technology, especially CMOS/SOS.

The PR2D program has been used to generate more than several hundred LSI array types. This includes more than 25 CMOS/SOS LSI arrays, 14 of which were designed for the 32-bit CMOS/SOS NASA SUMC computer now being designed for NASA-MSFC, Huntsville, Alabama. During the generation of these CMOS SOS arrays, various improvements were incorporated into the program as a result of the correction of errors and "bugs" that occurred during the generation of these various chip types. Other improvements were made in the program as a result of parameter changes and optimization that also occurred during the generation of these LSI arrays. These improvements were included in the PR2D computer program, which was delivered to NASA-MSFC during the course of this program.

Several of the SUMC CMOS/SOS LSI arrays that were designed and fabricated for the 32-bit CMOS/SOS NASA SUMC computer are illustrated and described in this report to demonstrate the effectiveness of the delivered PR2D computer placement and routing program.

To achieve the objectives of the project, a series of sophisticated and far-reaching algorithms and routines were incorporated into the Multiport Automatic Placement and Routing (MAPAR) program. This involved, for example, over several hundred variables, constants, and parameters which required definition and optimization in addition to the debugging normally required to render a computer program operational. In debugging the program, certain techniques used in the past to debug automatic placement and routing algorithms proved to be less than optimum for large LSI arrays, although they were more than adequate for smaller LSI chips. To minimize the ever-increasing costs associated with computer charges, the normal technique to debug programs of this type was to develop small test problems (small arrays) and use them to debug the algorithms and assign (at least in part) the various parameter and variable values. Because of the very large arrays with their complex wiring matrices, the debugging (and especially the parameter assignment) of small array types did not necessarily apply directly to the larger types. These larger units require debugging and characterizing at their particular levels. The continued debugging, especially for larger array types, was one of the objectives of this project.

b. Multiport (Double Entry) Automatic Placement and Routing Programs for Standard Cells

The Enhanced Automatic Placement and Routing Program, whose technical program name is the Multiport Automatic and Placement Routing Program (MP2D) is a computer program originally developed with support from the United States Army Electronic Command; Ft. Monmouth, N.J. Together with a new and advanced family of CMOS/SOS standard cell circuits, they constitute an LSI design approach that not only provides a low-cost, quick-turnaround capability, but also one that can yield the highest gate density yet achieved by design automation programs using completely automatic cell placement and interconnection algorithms.

To achieve these objectives of low design cost, short design time, and higher device density, a completely new approach for automatic placement and routing programs was developed. This new concept, called the Multiport LSI array approach, involved major innovations in both the Automatic Placement and Routing Program (APARP) and the associated standard cell circuits. One of these innovations enables the program (1) to automatically route interconnections to either the top or bottom of each cell in such a way as to minimize total wire length, as well as total wiring or interconnection surface; and (2) to make connections between cells on nonadjacent rows by routing the interconnections directly across or through other intermediate cell rows. If the intermediate rows contain any cells that are loads on the particular net being routed, the program will use the polysilicon gate as the direct feedthrough mechanism to reach other load cells on the nonadjacent rows. In this case, the polysilicon gate serves a dual role — as both the transistor control element and as a direct feedthrough connection — with a resulting reduction of wiring area.

If there are no load cells on the intermediate rows, the program will automatically generate a direct feedthrough by calling upon one of several "feedthrough cells" stored on the library tape. The program will place this direct feedthrough cell on the intermediate row on a vertical line closest to the driver and the remote load in such a way as to minimize the metal channels in the horizontal direction.

The combined effect of these novel capabilities is to eliminate all side routing or wraparound wiring that characterized previous standard cell design automation approaches, with the exception of any connections made to pads on the left or right side of the array. This has resulted in substantial saving of chip area because of the reduced area requirements of the wiring, previously the largest user of area on the standard cell automatic layouts.

The other major innovation relates to the unique feature of the circuit cell that permits the input-output connections of the circuit to be accessed at either the top or bottom of the cells. This circuit capability, combined with the polysilicon gate, provides a means of crossing the cell rows directly as opposed to the side wraparound wiring that characterized the previous single-ended automatic placement and routing LSI approaches.

2. High-Speed SOS Standard Cell Family

The NASA-MSFC, high-speed, CMOS/SOS, standard cell family was originally developed by RCA ATL under NASA program NAS12-2233. Expansion and additional characterization of the cell family was carried out jointly under NASA programs NAS12-2233 and NAS8-29072 and with RCA internal Independent Research and Development funding. Most recently, the SOS Standard Cell Notebook, circuit type file tape (pin data file tape), and the cell library tape have been updated by adding new cell designs to the library and file tapes and adding new characterization data to the Standard Cell Notebook. This was accomplished under NASA program NAS8-31325.

The circuit library was designed to be compatible with and maximize the performance of the PR2D (Automatic Placement and Routing) program, which was also originally developed under NASA program NAS12-2233. Together, the PR2D program and standard cell family provide the capability of generating high-speed, high-performance, random-logic, custom LSI arrays with quick turnaround, high density, and low static and dynamic power dissipation.

These cells are used in the generation of design automated custom LSI arrays in virtually the same manner as other RCA designed standard cell families. Briefly, this requires user-generated input data to the computer program, which consists of the net or connectivity list of circuit cells, as well as the cell or pattern identification number which is available from the data sheets. With this information, the PR2D program will provide an automatically generated layout and interconnection in a data format consistent and compatible with an automatic precision mask artwork pattern generator.

The Standard Cell Notebook, distributed as a separate document*, contains cell data sheets for each of the cells. It contains a description of the general information and data that are contained on all data sheets. It also contains additional information and descriptions where appropriate.

In another section of this report, measured data for several SOS standard cell arrays are presented. Dynamic delays for individual chips and chips in a system environment (hybrid mounted) are compared with delay information calculated using the standard cell notebook.

3. SOS Processing, Layout Rules, and Circuit Analysis

The high-speed, 7-mil, CMOS/SOS standard cell family circuits are laid out in accordance with the RCA Solid State Technology Center's (SSTC's) silicon-gate SOS process design rules. However, since it is SSTC's policy to endeavor to maintain mask set compatibility for all of the major SOS processes, it is possible for SOS standard cell arrays to be fabricated with any of a wide spectrum of processes. These include the double-epitaxial diffused process through the single-epitaxial, double-ion implanted process. For radiation-hardened applications, the single-epitaxial, triple-ion implanted process is also an available option. Out of a basic set of seven masks, all of these processes can be used to fabricate the standard cell CMOS/SOS arrays or any design laid out with the SSTC design rules. It is to SSTC's credit that process development and maturation has taken and is taking place, while simultaneously ensuring mask compatibility.

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*High Speed CMOS/SOS Standard Cell Notebook, developed and prepared by RCA ATL.

An authoritative description of SSTC's double-epitaxial and single-epitaxial processes is in a separate report entitled "Silicon-Gate CMOS/SOS Processing." For a definitive presentation of the RCA Solid State Technology Center's self-aligned silicon-gate SOS design rules, the reader is referred to a separate document entitled, "Design Rules for RCA Self-Aligned Silicon-Gate CMOS/SOS Process." The self-aligned silicon-gate SOS design rules describe the spacing and width requirements for each of the six design levels — the seventh level being used to define openings in the passivation level. These rules, together with the insight gained from the "Silicon-Gate CMOS/SOS Processing" report, are sufficient to initiate new standard cell designs.

A description of the MOS model used to characterize circuits designed with the SOS process may be found in a separate report entitled, "Device Model for FETSIM Circuit Simulation Program." The device parameters needed for the performance evaluations are also in this report.

B. TECHNICAL DISCUSSION

1. Multiport (Double Entry) Automatic Placement and Routing Program

As previously stated, the Multiport (double-entry) computer program was originally developed with support from the U. S. Army Electronic Command, Ft. Monmouth.[1] The program provided substantial improvement over the single-entry program. An example of this improvement is shown in Fig. 1 and 2, where the SUMC multiplexed eight-bit adder, described and discussed in section II.B.2, was used as the test vehicle. Figure 1 shows the eight-bit adder designed using the single-entry, high-speed, 7-mil-high CMOS/SOS standard cell family. The array reflects a significant amount of human intervention. The original version generated by the program was considerable larger. As shown in the figure, a large portion of the array is occupied by the wiring, which is about 63% of the total chip area. Of the total wiring area, the largest single user of area is the right and left side wraparound wiring, which amounts to about 30% of the total chip area. This chip contains 1640 devices and measures, from scribe line to scribe line, 229 by 229 mils. This corresponds to a device density of 32 square mils per device. Subtracting the border or pad area from the total chip area defines the active region of the array. For this area, the device density is approximately 28 square mils per device.

Figure 2 shows the layout of the multiplexed eight-bit adder generated by the early version of the MP2D program. The input data, (i.e. the logic being laid out) used for both layouts is identical. In addition, the identical circuitry is used in both chips. Therefore the area occupied by the cells is identical, 7840 square mils in each chip. Thus, the difference in the area between the two chips in Fig. 1 and 2 is a

[1]Under Contract DAAB07-74-C-0716

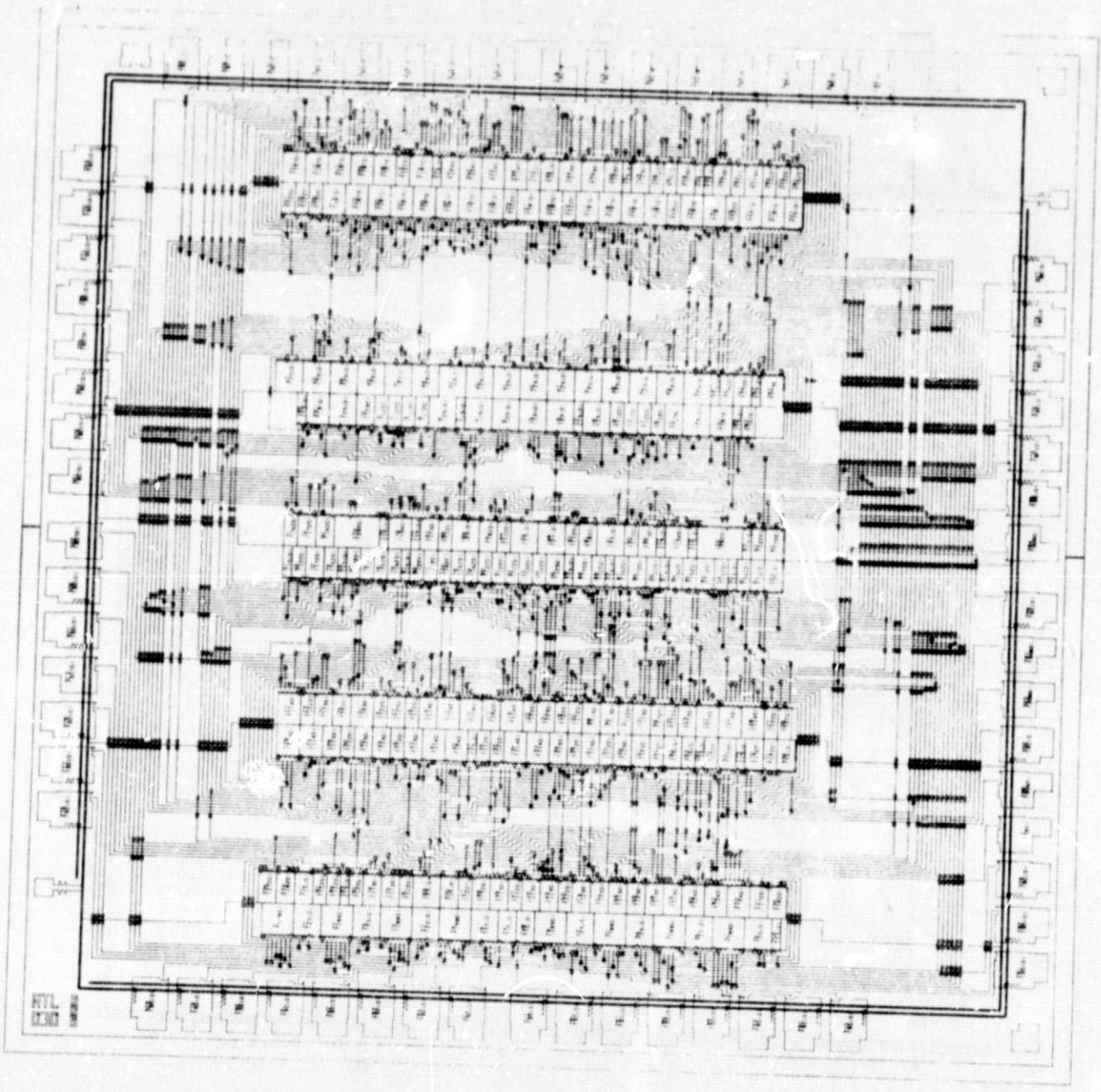


Fig. 1. Single-entry, CMOS/SOS, multiplexed, 8-bit adder.

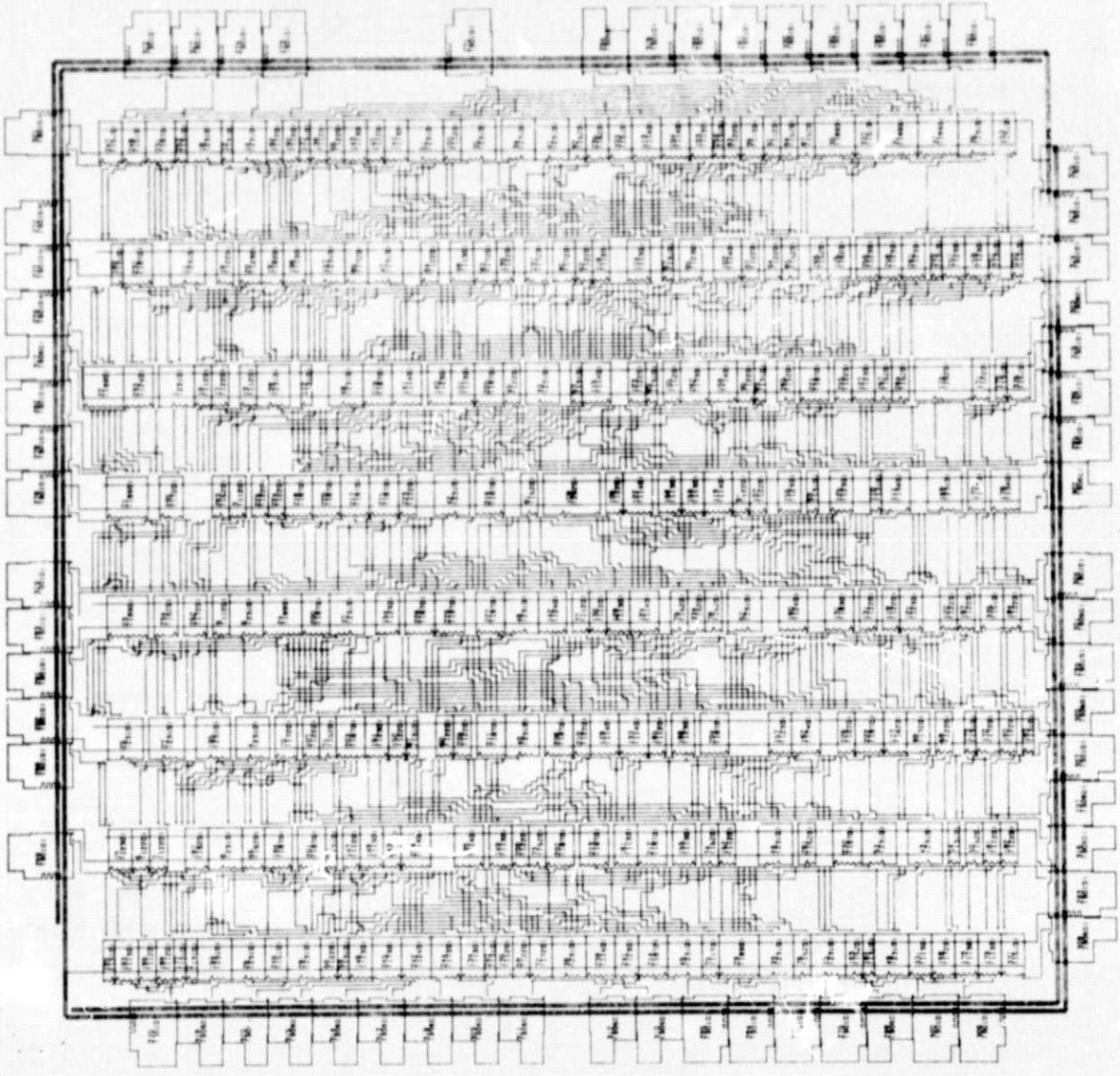


Fig. 2. Multiport, CMOS/SOS, 8-bit adder.

direct measure of the increased efficiency of the Multiport layout capability. The total scribe-line-to-scribe-line area of the chip in Fig. 2 is 200 x 194 square mils, a 26% reduction. This corresponds to a device of 24 square mils per device. Subtracting, as before, the border or pad area, the density of the active region is about 18 square mils per device. Since, as stated earlier, the single ended version in Fig. 1 had been optimized by extensive manual editing, the improvement is even more significant.

The decrease in wiring area from 33,369 square mils for the layout in Fig. 1 to 21,392 square mils, a reduction of 36%, is another measure of the effectiveness of the Multiport program, even in its early stages.

Work continued on this program to increase the area effectiveness of the Multiport program. Because of the huge complexity and sophistication and the relative newness of the program, various test cases, including some large complex examples, were exercised in order to locate and correct the various errors and "bugs" in the new program. Further, the test cases were used to evaluate certain algorithms and the methods used to implement them. In addition, the values of the various parameters and constants were defined and/or updated during this contract period. The result was an improved MP2D program which was delivered to NASA-MSFC in March 1976.

An example of this is shown in Fig. 3, which shows the Multiport layout of the Interface and Timing Array, the first Multiport CMOS-SOS array to be fabricated and used in this case in a non-military industrial application. This chip contains 1613 devices and occupies a total scribe-line-to-scribe-line area of 191 by 181 mils or 34,571 square mils.

This corresponds to a device density of 21.5 square mils per device. Because of some unusual specification, extremely large buffer-drivers, occupying considerable area, were designed for this chip and used in the pad or border area, making the border an unusually large percentage of the total area. Had the regular input-output buffer pads been used, as in the other chips, the device density from scribe line to scribe line would be 18.3 square mils per device. The device density of the active area, subtracting the pad or border area, is less than 15 square mils per device.

2. SOS Standard Cell Library

a. Design Verification

The CMOS/SOS standard cell library is an open-ended collection of logic circuits designed for fabrication by any of the major RCA SOS processes. All the circuits have gate lengths of 0.25 mil for optimized performance.

All the standard cells have been defined, designed, and topologically configured in accordance with the standard set of SOS design and process constraints, then analyzed and permanently stored for future use on magnetic tape.

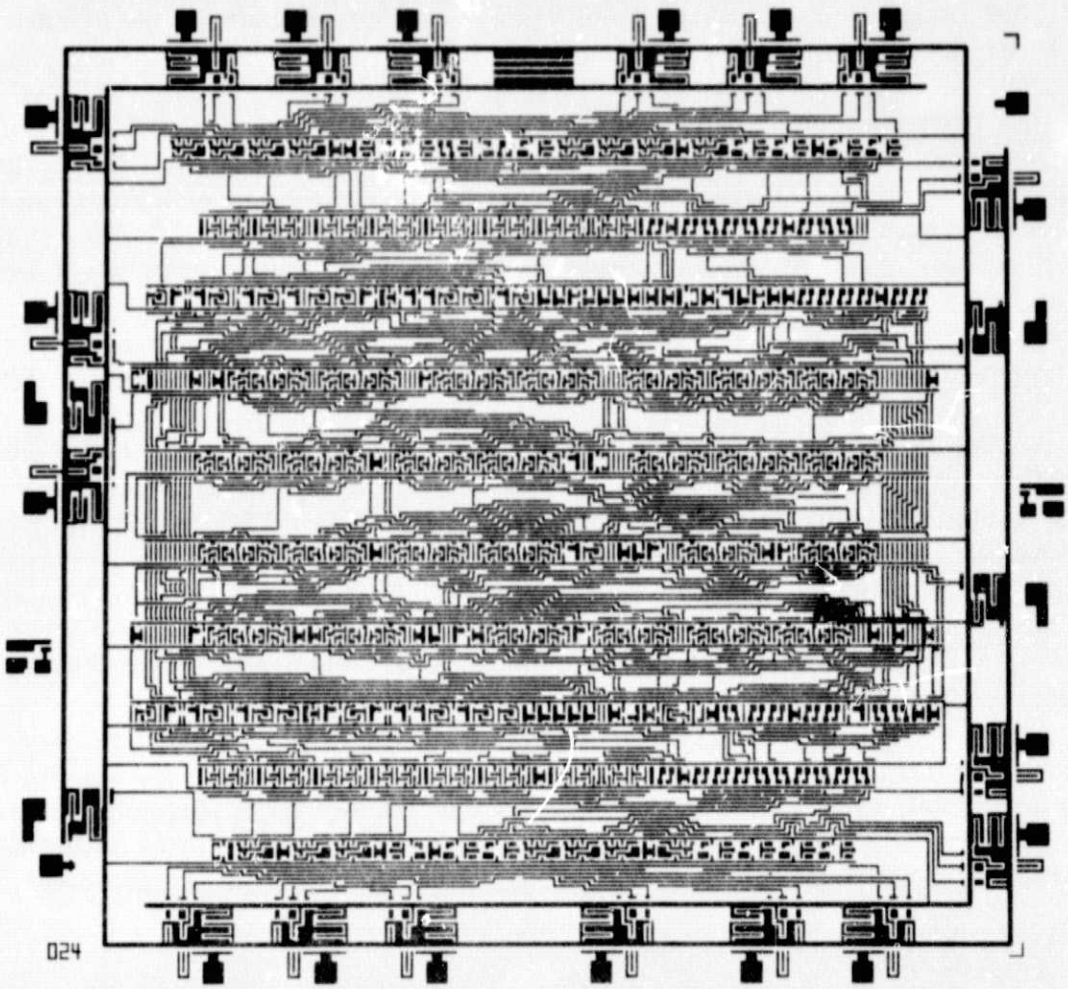


Fig. 3. Double-entry CMOS/SOS Interface and Timing Array.

There are 34 standard cell data sheets contained in the Standard Cell Notebook. A separate data sheet is provided for each cell, except for the eight input-output buffer pad cells. In these cases, one data sheet provides the necessary design information for the two slightly different versions of the same cell.

Of the 38 cells listed in the notebook, the following subset contains the cells that have already been used in at least one LSI array. The LSI arrays in which these cells were used were the chip complement of the 32-bit, general-purpose, IBM-compatible CMOS/SOS computer- the CMOS/SOS SUMC. (The Space Ultrareliable Modular Computer is under development for NASA Huntsville by ATL.) The verified cells are listed, along with usage verification, in Table 1.

b. Performance Verification

The correct functionalities of all these cell types were experimently verified from measurements made (on an IR&D program) on the various SUMC-SOS chip types. These include the TCS026, TCS027, TCS029, TCS030, TCS031, TCS032, and TCS033 CMOS/SOS chips. (The "TCS" prefix indicates that the arrays were processed by SSTC.) In addition, the dynamic performance of many of the cell types, as given in the data sheets, were also verified by these measurements. The method employed to obtain correlation data between the measured and predicted delay (at 10 volts nominal) involved the selection of a logic path considered important to the overall computer performance requirements. The propagation delay was then measured at 10-volt operating levels and at ambient temperature. Then, using the cell data sheets, the logic fanout, with its related capacitances and other relevant chip statistics, the delay of this path was estimated and compared to measured data.

c. Performance Correlation

The following paragraphs briefly describe five of the SUMC LSI arrays. The logic paths chosen for the measurements, the estimated path delays taken from the data sheets, and the actual measured delays are all given. An estimate of the measured SOS performance, at the system level is also given by comparing the measured and calculated performance for three array types connected on the complex Adder Hybrid. Table 2 includes a concise summary of both the measured and the estimated data (from the Standard Cell Notebook).

(1) Floating Point Multiplexer, ATL-026A (155 x 134 mils, ~163 gates)

This chip is a 2 x 1 shifting multiplexer. In the SUMC-CVT system, it operates on every fourth bit, either shifting ± 4 bit positions or passing the bits straight through. Provisions are included for mixing two extraneous inputs. The primary input path is eight bits wide, while the shifted output is nine bits wide. The chip is totally combinatorial.

TABLE 1. CELL VERIFICATION

Cell No. / Usage		Cell No. / Usage		Cell No. / Usage		Cell No. / Usage		Cell No. / Usage	
1120	abcdf	1310	bcdf	1640	af	2310	acdf	9070	abcdef
1130	a cdf	1340	d	1720	abcdf	2820	bcdf		
1140	a cd	1510	abcdef	1730	d	9010	abcdf		
1220	a cdef	1520	abcdef	1740	f	9020	b		
1230	abcdef	1620	abcdf	1870	b d	9050	b		
1240	def	1630	a cdf	1890	a cd	9060	abcdef		

a - indicates use on TCS026
b - indicates use on TCS027

c - indicates use on TCS029
d - indicates use on TCS030

e - indicates use on TCS031
f - indicates use on TCS032

The logic path chosen for measurement consists of six levels and is shown in Fig. 4. The recorded chain delay ranged from 17 ns to 34 ns. Figures 4a and 4b are photographs of the input and output waveforms for the 17-ns measurement. Averaging this time over the four standard cells yields 4.3 ns per cell. If, however, this delay were averaged over the actual number of logic levels used to implement the chain, the average delay per logic level would be closer to 2.9 ns.

Calculating the total chain delay with the standard cell data sheets, however, gives a predicted delay of 27 ns; and indeed when a larger number of ATL-026A arrays were examined, the average delay for the path did work out to be 23 ns. This is within 20% of the value obtained from the data sheets.

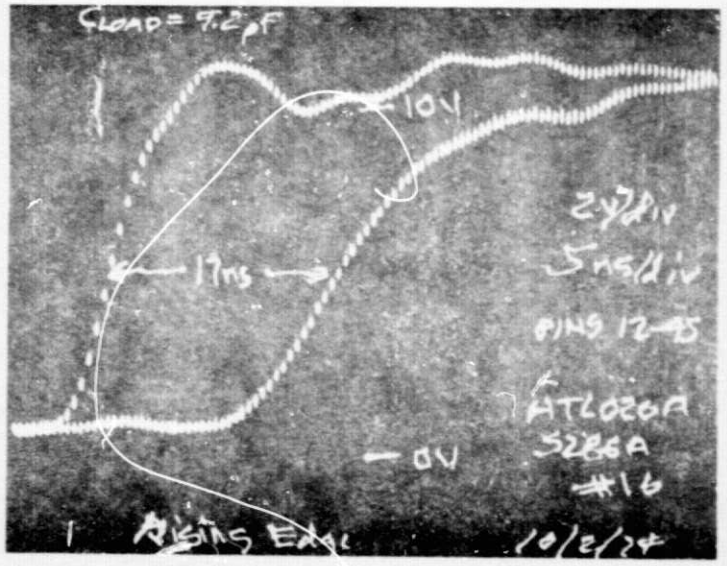
(2) Up/Down Counter Chip, ATL-027 (199 x 199 mils, ~ 300 gates)

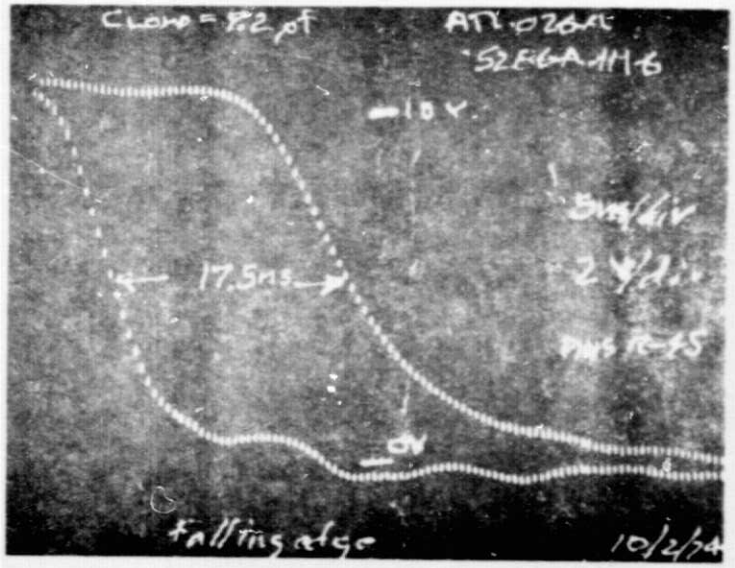
This array consists essentially of a 12-bit up/down counter divided into separate eight-bit and four-bit sections. Each has separate controls, but only the

TABLE 2. SUMC-CVT CMOS/SOS LSI ARRAY PERFORMANCE MEASUREMENTS*

Array Name	Total Delay (ns)		Measured Average Stage Delay (ns)	Estimated On-Chip Stage Delay (ns)	Off-Chip Load (pF)
	Measured (Average)	Calculated			
Floating Point Multiplexer (ATL-026A)	23	27	4.3	---	12
Up/Down Counter (ATL-027)	52	46	5.8	---	10
8-Bit Adder (ATL-030)	73	75	5.2	5.3	15
	105	103	---	---	100
9-Bit 4 x 2 Multiplexer (ATL-031)	60	50	8.0	3.6	100
Adder-Multiplexer Controls (ATL-032)	67	66	5.2	4.8	18
	76	71	---	---	40

*All delay measurements at 10 V.





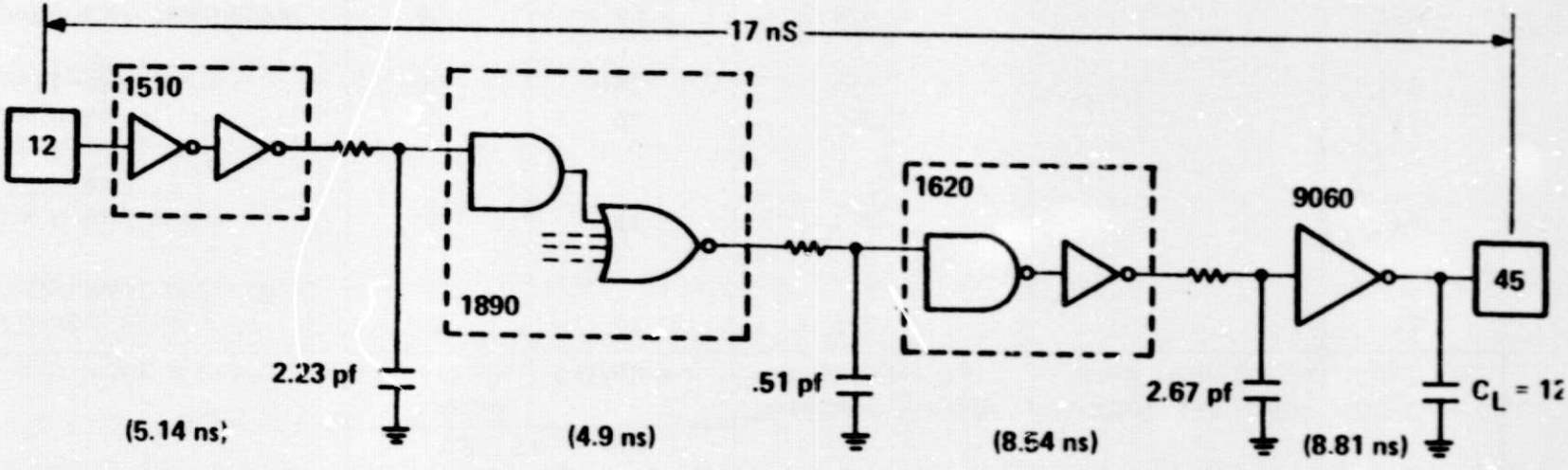


Fig. 4. Measured delay for floating point multiplexer.

eight-bit section has carry and borrow outputs for expansion. Each stage has a two-input multiplexer for pre-setting the count value. Counting is done in a ripple carry/borrow full adder subtracter. The counter outputs are tri-state, buffered elements.

Figure 5 illustrates the logic path to be used in chip operation. It contains six cascaded standard cells or eight levels of logic. The "clock" is used to transfer data from the 2820 storage elements to the output which, as shown, is loaded with 10 pF. For these measurements, the external chip controls are set to toggle the flip-flop with every clock pulse. Delays are measured between the 50% point of the negative-going clock to the 50% point of the output. Delay results for several packaged units ranged from 42 ns to 59 ns, with an average delay of 52 ns. Calculations based on the standard cell data sheets predict 46 ns for the same path (which is correlation to within 11%). On a per-stage basis, the measured average is: (52 ns ÷ 9 stages) = 5.8 ns.

(3) Eight-Bit Adder, ATL-030 (229 x 229 mils, ~ 450 gates)

This array is an eight-bit binary or decimal adder. It is fully expandable and has carry anticipate logic for fast arithmetic operations, a multiplexed B input, a data complement and logical capability, and several special-condition outputs. The logic path examined is a portion of the SUMC-CVT 32-bit adder's critical path. It is composed of 11 cascaded standard cells. Depending upon the method used, this works out to be 11 to 13 levels of logic. Figure 6 illustrates this path. Measurements are made from the 50% point of signal at the input to the 50% point of output signal. Data were taken at both the packaged device (64-pin DIP) and wafer probe levels. For a 15-pF output load, packaged device delays averaged 73 ns. The average measured device delay is 73 ns ÷ 12 stages = 6 ns. For an output load of 100 pF, the total delay averages 105 ns. Figure 7 shows typical photos of the input and output waveforms of the 64-pin DIP packaged unit measurements. In terms of the SUMC-CVT program, the 15-pF load measurements are more directly applicable than the 100-pF load case since 15 pF is more typical of the anticipated on-hybrid loading.

From a system point of view, the adder path is extremely critical. With this in mind, calculations were performed based on the 7.0-mil SOS standard cell data sheets. From the CalComp checkplot of the adder array, the additional loading contributed to the output of each cell in the adder path by the wiring crossovers was precisely accounted for. Figure 6 shows the crossovers on each output in the critical path. It also includes the calculated delays on a cell basis. From these calculations, it is possible to discount the large buffer delay associated with going off-chip. If this is done, the estimated on-chip delay is 5.4 ns/logic level. Totaling all calculated delays for the path, we arrive at a total estimated delay of 75 ns, which closely correlates with the measured average of 73 ns.

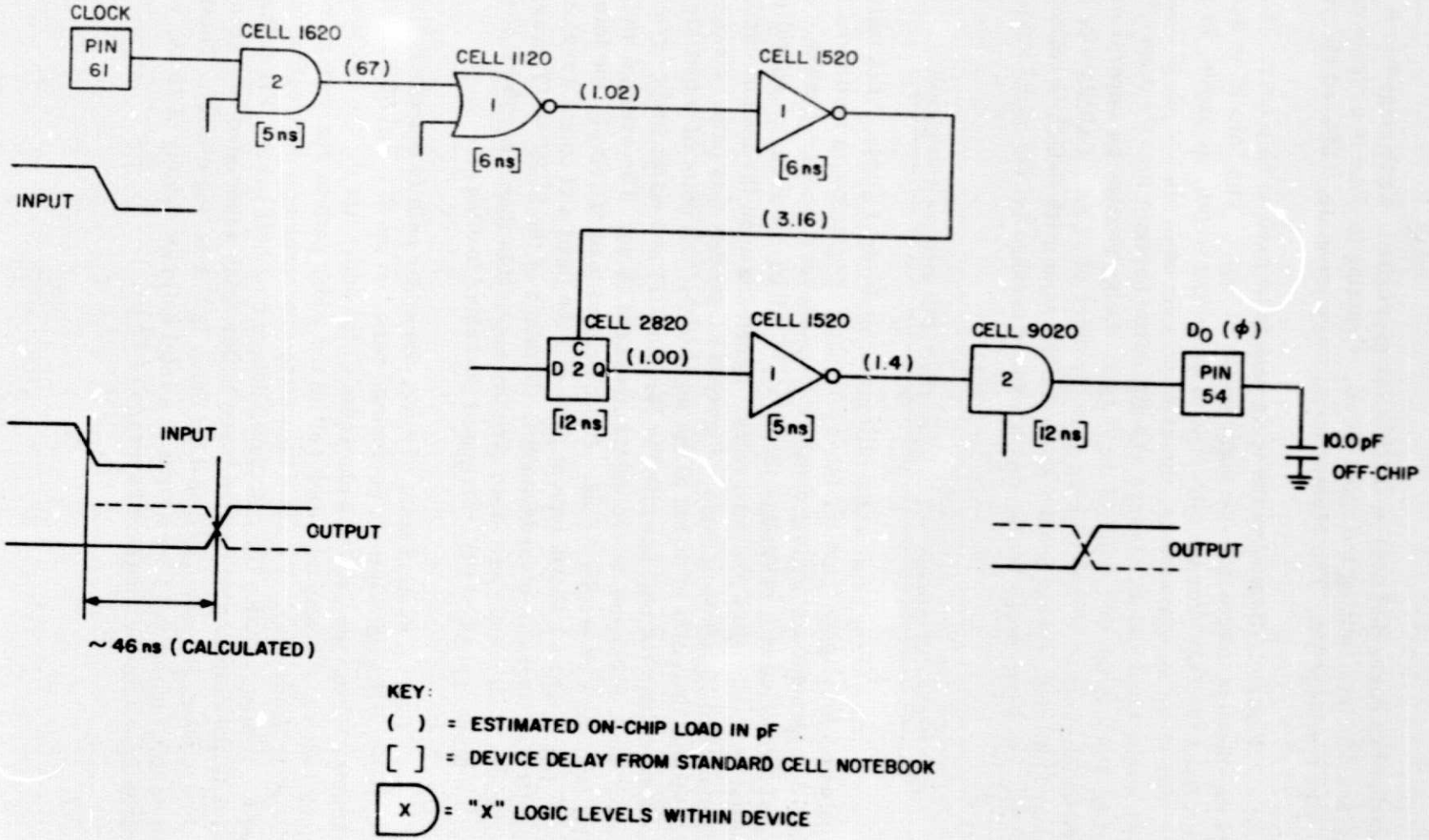


Fig. 5. Calculated delays for up/down counter.

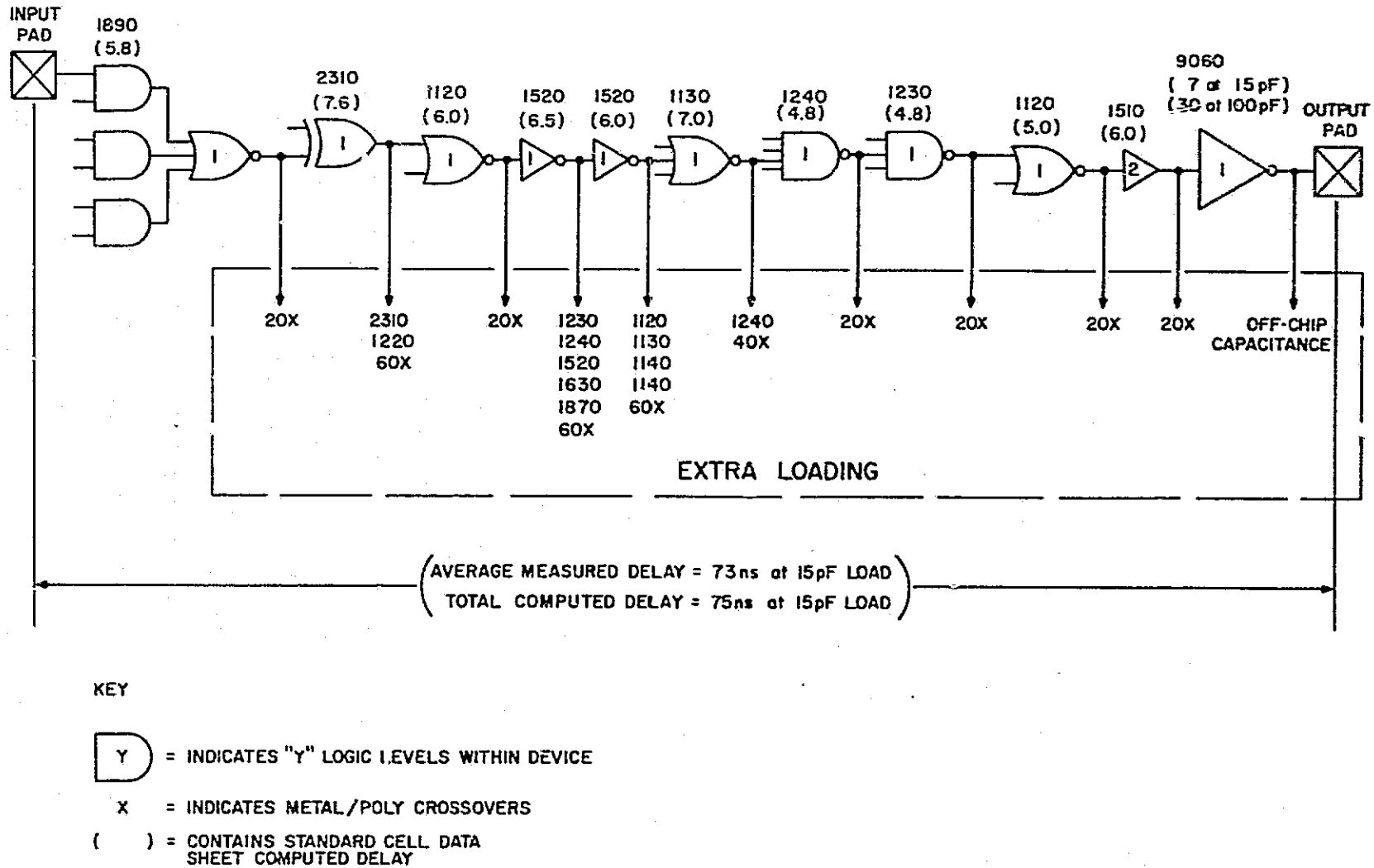


Fig. 6. Critical path of 8-bit multiplexed input adder.

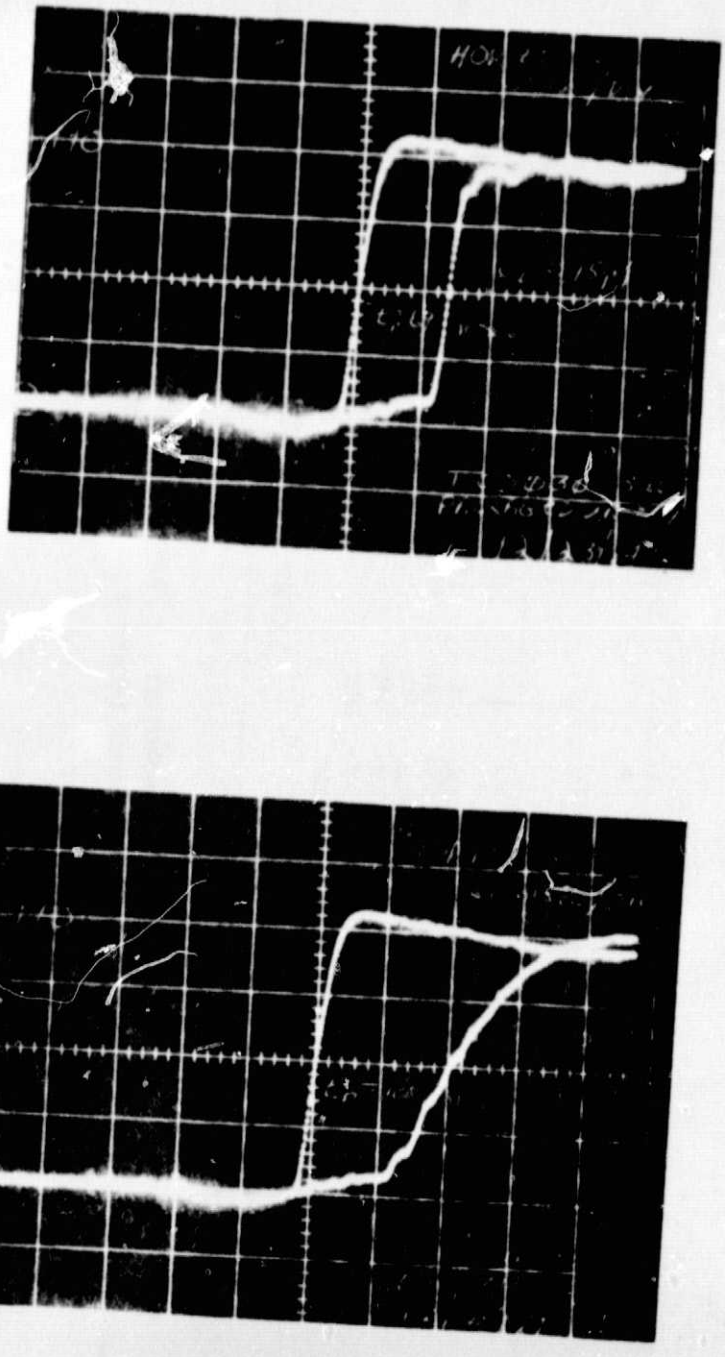


Fig. 7. Typical input-output waveforms of 8-bit adder.

A further investigation was carried out. It centered on the n- and p-type transistor saturation currents assumed for the standard cell data sheet delay curve calculations and those of the actual devices on the fabricated arrays. (The actual device currents were measured on the array's output inverters and were within 10% of those assumed for the delay curve calculations.)

(4) Nine-Bit 4 x 2 Multiplexer, ATL-031 (172 x 175 mils, ~ 150 gates)

This array is a flexible multiplexer that may be used as either a nine-bit 4 x 2 multiplexer or an 18-bit 2 x 1 multiplexer. Its mode of operation is determined with four independent control lines. The chip is 100% combinatorial. The longest logic path on the chip is five cells long, or in terms of logic levels, six levels deep. Figure 8 shows a small portion of the array's logic. The path over which measurements are taken has been highlighted. Dynamic measurements were made between the 50% levels of the input and output signals. Measurements made at the wafer probe level produced a range of delays for the six logic levels from 50 to 80 ns. This included the loading effects of the test equipment cables which was measured at more than 100 pF. The average total delay was approximately 60 ns. From the standard cell data sheets, the total path delay is calculated to be 50 ns; most of which is due to the output stage. By separate measurements, the cabling alone introduces 12 ns of delay. Taking this into account, we have an average measured delay of (60 - 12) ÷ 6 = 8 ns/stage. (This figure drops considerably when the delay of the output buffer is neglected. Under these conditions, we have (60 - 12 - 30) ÷ 5 = 3.6 ns/stage.)

(5) Adder-Multiplexer Control, ATL-032 (154 x 139 mils, ~ 166 gates)

This array houses the special random control logic which combines the ROM outputs with data dependent conditions. The array outputs serve to route the adder inputs and specify the adder operations appropriate to the instruction being executed. Figure 9 shows the logic path used to examine the array's performance. It was chosen primarily because of its length -- 10 standard cells long. In terms of the way the cells are implemented, this path may be considered to be 13 levels of cascaded logic. Measurements are made from the 50% point of the input clock signal to the 50% point of the output signal. The "clock" is used to transfer data from the 2820 storage element to the output. The output is connected back to another chip input, which provides for flip-flop toggle action on every "clock" pulse. Measured delay data, on packaged units, averages 67 ns for the path when the off-chip loading is 18 pF. It averages 76 ns for the path when an external load of 40 pF is used. For an 18-pF load, the average measured device delay is: 67 ÷ 13 = 5.2 ns.

Calculations for the same path were made using the standard cell data sheets and a CalComp checkplot of the array's topology. The latter provides a precise count of metal/polysilicon crossovers at each cell's output. The crossovers

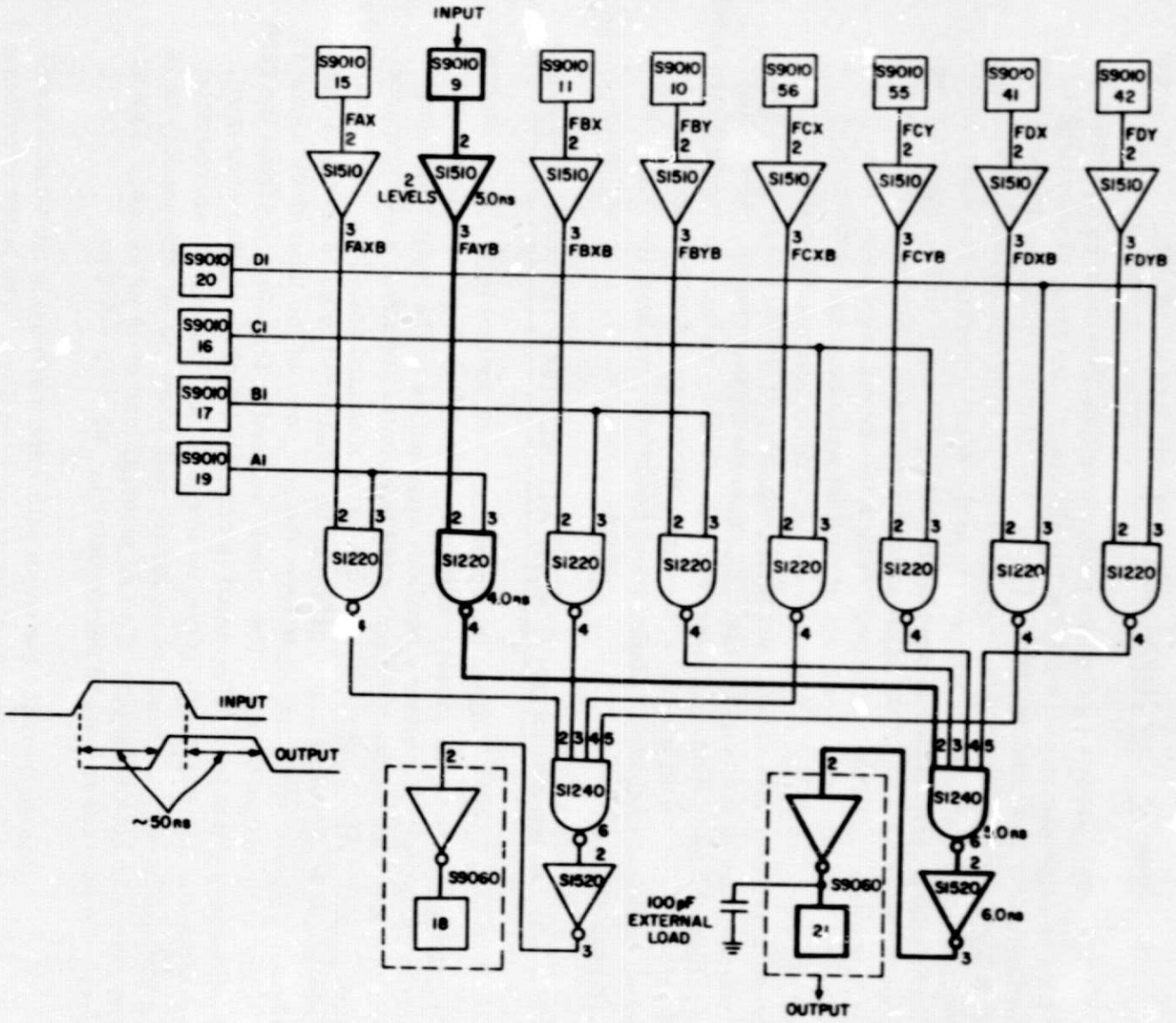


Fig. 8. Calculated delays for nine-bit 4 x 2 multiplexer.

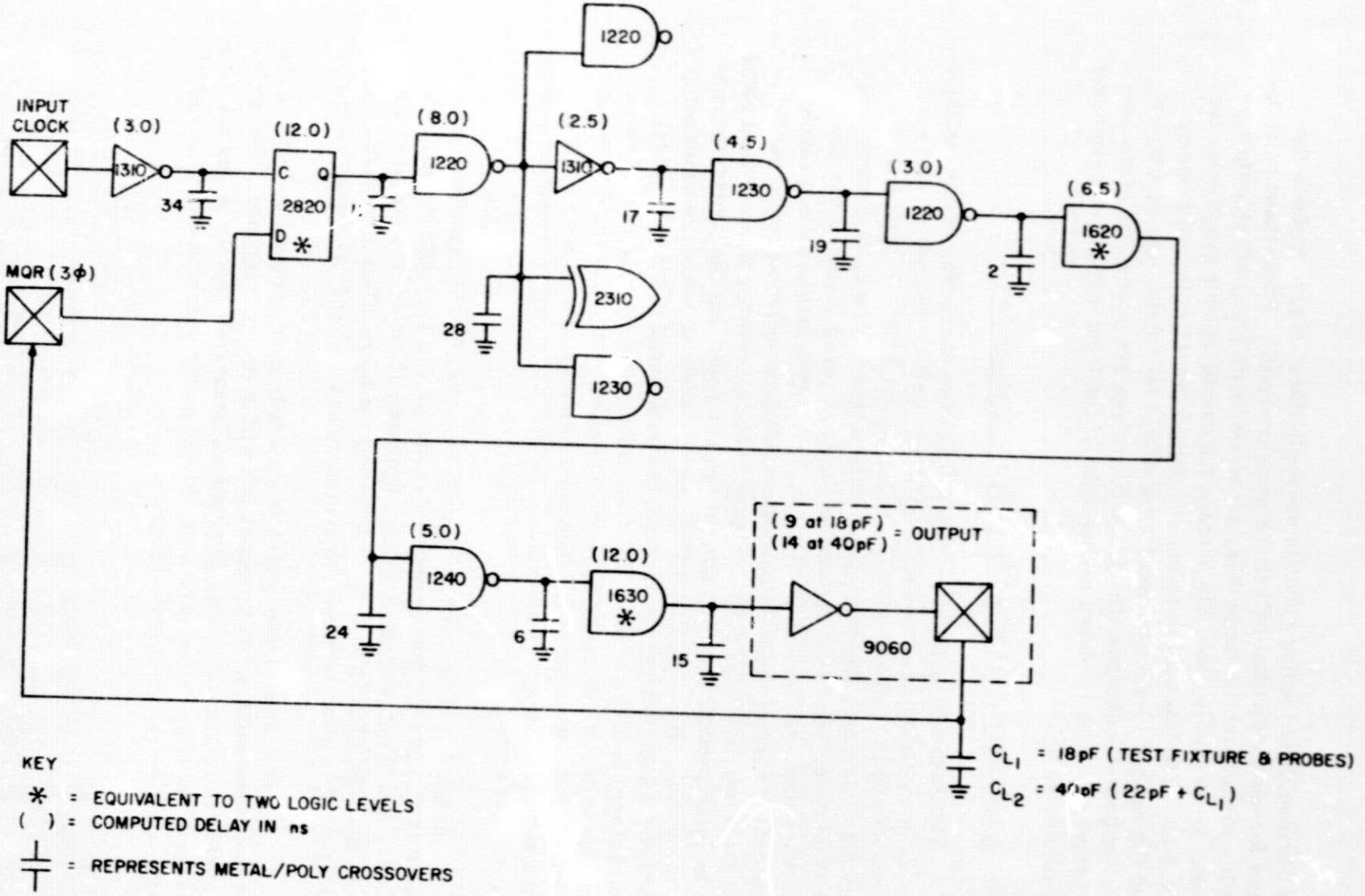


Fig. 9. SUMC-CVT CMOS/SOS adder control chip measurement path.

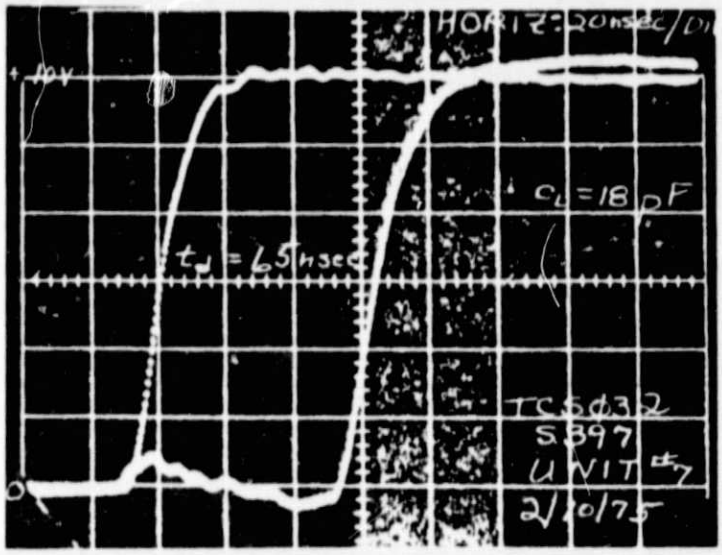
are considered because their loading effect is not negligible. Figure 9 shows the calculated delays for each individual cell in the measured path. From these calculations it is possible to discount the large delay associated with going off-chip through the 9060 element. When this is done, the average measured on-chip stage delay is: $(67 - 9) \div 12 = 4.8$ ns. Totaling all the calculated delays for the path, we come up with 65.5 ns for the case of 18-pF external load and 70.5 ns for the case of a 40-pF external load. For both calculations, the predicted values are within 10% of the average measured values. Figure 10 shows photographs of the input and output waveforms for loads of 18 pF and 40 pF.

(6) Adder Hybrid, 11 SOS LSI Arrays - 3,541 gates

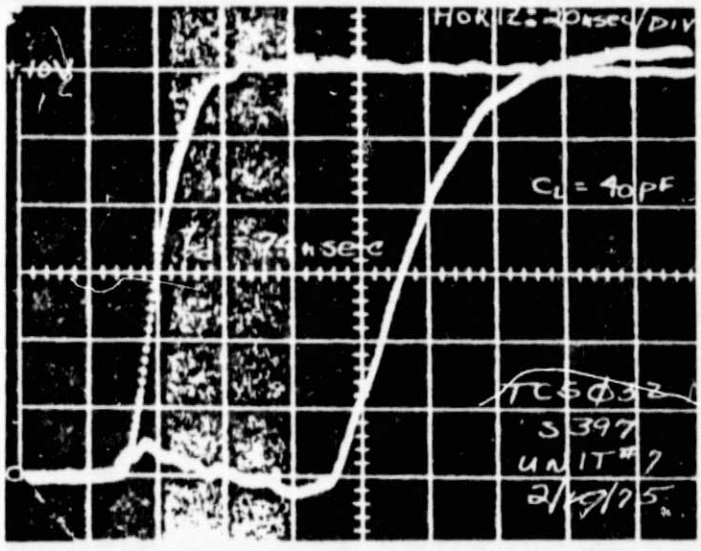
The Adder Hybrid is the equivalent of two cascaded, 16-bit, arithmetic logic units. It is expandable to two cascaded 32-bit ALUs. Therefore, one such hybrid may serve as either the LSH or MSH of a full 32-bit ALU. Functionally the hybrid provides for binary add, logical, and complement operations, fast carry look-aheads, I/O multiplexing, 1-to-4-bit operand shifts, and result status indicators (such as overflow, zeros, etc.). The purpose of the adder hybrid is (1) to provide critical portions of the system logic with a low-capacitance interconnection environment and (2) to increase packing density. Figure 11 illustrates one of the hybrid paths over which delay measurements were taken. It is to be noted that the hybrid environment has permitted SOS chips to maintain their high on-chip performance while going off-chip. Measured delays through the 22 logic stages average 4.3 ns per stage. Figure 12 is a photograph of the 11-SOS/LSI-Chip Adder Hybrid. The chips are attached to the substrate with an epoxy adhesive and electrically connected to the substrate wiring with 1-mil bonding wires. The substrate measures 1.8 by 4.2 inches and contains the equivalent of 3,541 CMOS logic gates. All signal interconnect routing was 100% program generated.

Table 3 is a compilation of the measured and calculated on-chip/off-chip delays for five SUMC-CVT SOS arrays. The delays are averaged overall logic levels in the path, and in some cases averaged over only those cells internal to the array. The latter calculation is done by discounting the large off-chip buffering delays. Very good correlation is noted between the average measured and calculated delays.

As seen in the table, there is generally good correlation between the predicted and measured results. Differences fall within design tolerance. The major significance of the correlation between predicted and measured results is that the circuit speeds achieve the dynamic performance objectives for which they were designed--the NASA SUMC-CVT computer system program.

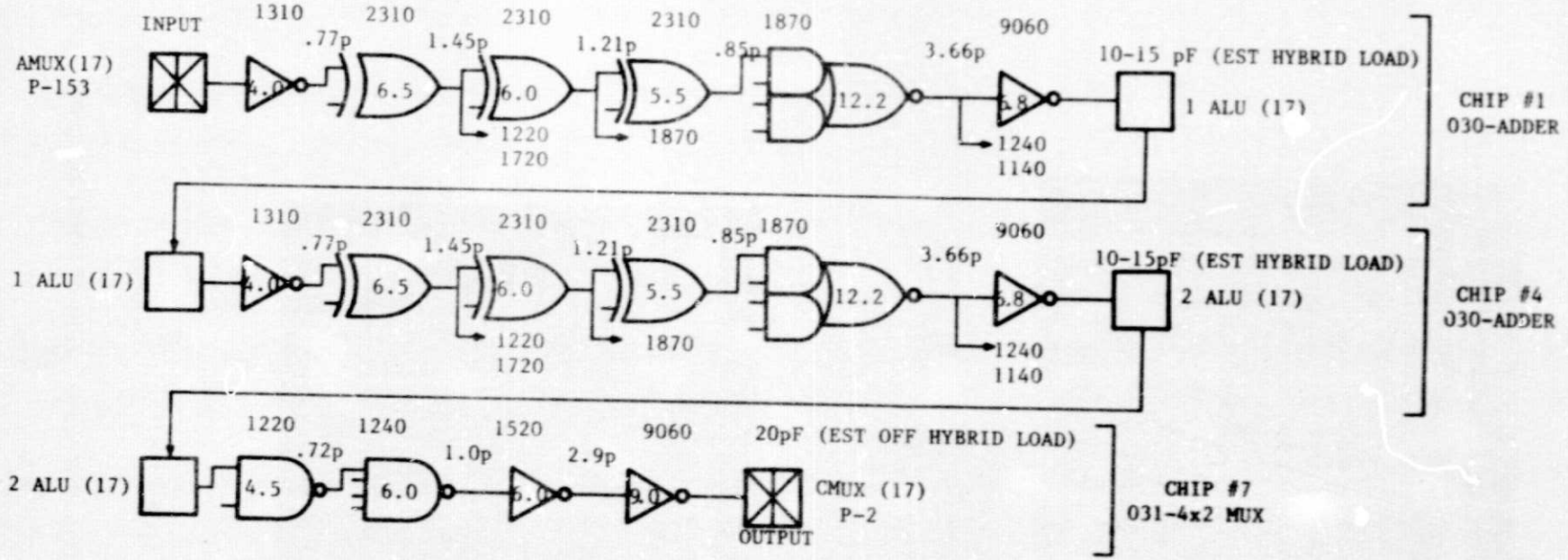


(a) $C_{OFF\text{-}CHIP}$=18 pF



(b) $C_{OFF\text{-}CHIP}$=40 pF

Fig. 10. Typical input-output waveforms of adder control.



- INDICATES HYBRID I/O PIN

- INDICATES CHIP I/O PIN

* FROM STANDARD CELL NOTEBOOK WITH 0.4 pF ASSUMED INTERCELL LOADING

CALCULATED DELAY* - 105.9 ns ⟶ 109.9 ns	4.8 ⟶ 5.0 ns/STAGE
MEASURED DELAY - 95 ns	4.3 ns/STAGE
STAND-BY CURRENT - 0.80 mA AT 10 V	

Fig. 11. Adder hybrid delay measurements.

Fig. 12. D/A generated adder hybrid.

TABLE 3. MEASURED VS. ESTIMATED SOS PERFORMANCE

Custom Standard Cell CMOS/SOS Array Types	Computer Predicted Delay (ns)	Average Measured Delay (ns)	Measured Average Stage Delay (ns)
Floating Point Multiplexer	27	23	4.3
Up/Down Counter	46	52	5.8
8-Bit Adder with Carry Prediction	75 103	73 105	6.0
9-Bit 4x2 Multiplexer	50	60	8.0
Adder-Multiplexer Control	66 71	67 76	5.2
Adder Hybrid Path (8-Bit Adder 8-Bit Add Adder 9-Bit 4x2 MUX)	108	95	4.3

d. Standard Cell Data Sheets

To facilitate the addition of new cells to the standard cell library as well as to facilitate their use as a design tool, the data sheets listing the properties and performance of the cell family and the necessary supporting instructions are described in a separate document — the CMOS/SOS Standard Cell Notebook. The Notebook contents and its use are briefly described in the following paragraphs. Table 4 lists the cells that currently make up the CMOS/SOS standard cell family.

Each data sheet contains the following information:

- Cell family technology.
- Descriptive name of the cell indicating its function.
- Cell identification or pattern number. This number identifies the cell in the input data to the automatic placement and routing program.
- Supply voltage for which the given propagation delay and transition times are applicable.
- Width of the cell in mils.
- Circuit schematic of the logic configuration including the numbering of each input and output connection. These numbers provide the means by which the chip interconnection or net list is generated.
- Capacitance at each input and output connection. This capacitance is computed on the basis of the geometry, topology, and materials associated with the capacitor. The Miller effect is not included in the value. It is automatically included when the device is analyzed by computer simulation techniques.
- Logic symbol plus the Boolean equation describing the cell function.
- Truth table.
- Dynamic performance data.

The propagation delays and transition times, as given on the data sheets, were originally generated using the RCA CMOS/SOS circuit simulation program. The device, circuit, and process parameters used in the simulation were based heavily on the parameters determined from measurements on SOS standard cell test chips.

TABLE 4. HIGH SPEED CMOS/SOS STANDARD CELL LIBRARY

Cell Number	Cell Function	Description/Comments
1120	Two-Input NOR	Logical NOR
1130	Three-Input NOR	Logical NOR
1140	Four-Input NOR	Logical NOR
1220	Two-Input NAND	Logical NAND
1230	Three-Input NAND	Logical NAND
1240	Four-Input NAND	Logical NAND
1310	Buffer Inverter	On-chip operation with loads up to 4 pF
1340	Inverting 2x1 Multiplexer	When the control is in the high state (10 V), the output is $\overline{A}$. When the control is low, the output is $\overline{B}$.
1370	Low-Z Transmission Gate	Electronic equivalent of a single pole, single throw switch. When the control is in the low state, the input and output are effectively disconnected and the other node either floats or is defined by other circuit elements. In the high state, the transmission gate is in the 'ON' state with the output connected to the input with a series resistance of approximately 2000 ohms.
1510	Non-Inverting Buffer	Primarily designed for 'on chip' use, this cell can be used to reduce delays when the load capacitance exceeds 2 pF.
1520	Double Buffer Inverter	For capacitance loads in excess of 4 pF.

TABLE 4. HIGH SPEED CMOS/SOS STANDARD CELL LIBRARY (Continued)

Cell Number	Cell Function	Description/Comments
1570	On-Chip Tristate	This cell is a tristate device designed for on-chip use. A control is available to determine the operation mode of this cell. With the control high the cell operates as an inverter buffer capable of driving heavy on chip loads. With the control low, the cell is in the 'off' state, with an extremely high output impedance — in the order of a tenth picofarad. This permits the use of bidirectional buses on the chip.
1620	Two-Input AND	Logical AND through two functional stages
1630	Three-Input AND	Logical AND through two functional stages
1640	Four-Input AND	Logical AND through two functional stages
1720	Two-Input OR	Logical OR through two functional stages
1730	Three-Input OR	Logical OR through two functional stages
1740	Four-Input OR	Logical OR through two functional stages
1870	Two, Two And-Two NOR	This cell performs the function $Z = \overline{AB+CD}$. Drive capability and performance are similar to the 1120 type cell.
1890	Two , Two, Two And-Three NOR	This cell performs the function $Z = \overline{AB+CD+EF}$. Drive capability and performance are similar to the 1130 type cell.
2000	J/K Flip Flop with Set/Reset	This cell is one of the more complex of the standard cells. Both the set and the reset are unconditional except that the two positive pulses must not be applied simultaneously. The truth table, shown below, was extracted from the data sheet.

TABLE 4. HIGH SPEED CMOS/SOS STANDARD CELL LIBRARY (Continued)

Cell Number	Cell Function	Description/Comments
		C J K S R Q ↓ 0 0 0 0 Q_{n-1} ↓ 1 0 0 0 1 ↓ 0 1 0 0 0 ↓ 1 1 0 0 $\overline{Q}_{n-1}$ ↓ * * 0 0 Q_{n-1} * * * 1 0 1 * * * 0 1 0 * * * 1 1 Prohibited Note: Q_{n-1} is state of flip-flop before last clock transition * - Don't care condition
2020	D-Type, M/S, S/R Flip-Flop	This is another of the more complex of the standard cells. Both the set and reset are unconditional except that the two positive pulses must not be applied simultaneously. The truth table, shown below, was extracted from the data sheet. C_{lock} D R S Q $\overline{Q}$ ↓ 0 0 0 0 1 ↓ 1 0 0 1 0 * * 1 0 0 1 * * 0 1 1 0 * * 1 1 * * * - Don't Care Case * - Undefined Output Case
2310	Exclusive OR	Exclusive OR through a unique combination of four transistors.
2570	Off-Chip Tristate Pad	A special off-chip tristate device with 5 times the drive power of the 9020/9050 cell.

TABLE 4. HIGH SPEED CMOS/SOS STANDARD CELL LIBRARY (Continued)

Cell Number	Cell Function	Description/Comments
2810	D Flip-Flop with Inverter Output	This cell is one of three latches in the cell family. This cell provides all the functions of the 2830 cell except that it provides an output in which the polarity of the data is inverted.
2820	D Type Master-Slave Flip-Flop	See page 33.
2830	D Flip-Flop with Open Feed-Back Loop	This cell performs the function $Q=D\overline{C} + Q_{n-1} C$ where D is the data input, C is the clock or control element, Q is the output of the latch and Q_{n-1} is the state of the latch prior application of the negative clock. This cell can be used as an input or output register element, for buffering, for temporary storage and as a control flip-flop.
2840	D Flip-Flop with Reset	This cell is the third of the latch type cells in the CMOS-SOS cell family.
7000	PLA Input Decoder	This cell, together with the 7010, provide a PLA function. This cell provides a full three input decoded output with an inhibit control that permits expandability. Functionally the cell consists of eight four input gates with each providing the full 3 data input decoding.
7010	PLA Output Function String	This cell provides the programmable part of the PLA through mask programming. It essentially provides the 'OR' function and may be cascaded serially to provide more complex logic functions.

TABLE 4. HIGH SPEED CMOS/SOS STANDARD CELL LIBRARY (Continued)

Cell Number	Cell Function	Description/Comments
9020/ 9050	Off-Chip Tristate Pad	These cells are tristate high current drivers designed to drive high capacitance 'off-chip' loads. The state of these cells are determined by a control input. When the control is high the cells are low Z, non-inverting buffers. When control is low, devices become high impedance devices that may be common bussed or phantom ORed. The two cell types are distinguished by their location and orientation in the street area.
9030/ 9040	Input Inverter Buffer Pad	As input pad that provides both waveform shaping buffering and signal inversion.
9060/ 9070	Off-Chip Inverting Buffer Pad	See page 34.
9130/ 9140	Buffered Non-Inverting Input Pad	An Input pad that provides both waveform shaping & buffering with no signal inversion.

The dynamic format for each cell depends upon the function of the cell. Generally, performance information is presented as a straight-line graph with load capacitance and performance scales plotted on the X-axis and Y-axis, respectively. The points located on each graph define the nominal performance of each cell as a function of loading. Therefore, the propagation delay curves define estimated delays that are expected to occur for each cell.

Dynamic performance data at V_{DD} = 10 V is provided for each logic cell. This data may be presented in several ways. These include propagation delay on a per-stage basis, transition time, clock rate, minimum or maximum pulse width, delay measured with respect to the clock, or combinations of the preceding. In all cases, the dynamic data is given as a function of load capacitance.

For logic cells like the 1120, 1130, 1140, 1220, 1230, 1240, 1310, 1520 and the 1620, the delay is given in the form of curves showing stage delay and transition times as functions of capacitive loading. The stage delay is the average of the propagation delay as measured at the 50% signal swing level for positive and negative going input signals. Similarly, the transition time is measured over the 10 to 90% rise and fall times. The input signal to these circuits during the generation of this data is the output of a inverter stage, which acts as a buffer against the programmed input pulse. The principal objective of this buffer is to minimize the effect of the transition time of the input on the dynamic data. The dependency, nevertheless, exists and should be considered.

In contrast to this, the dynamic data for those circuits which contain storage devices is given in terms of the minimum pulse width required to transfer new data into the master and slave storage elements as well as propagation delay data. In the latter case, the delay is specified from the 50% level of the negative transition of the clock to the 50% level of the output of the slave.

As new cells are added to the CMOS/SOS family, they will be dynamically characterized in a manner that will optimize the usefulness of the cells to the system designer.

e. Performance Characterization

The dynamic data shown on the data sheets are based on computer simulation techniques using a RCA developed computer circuit analysis and simulation program. Primarily developed for integrated circuit application, the program contains specially developed device models with parameters expressed in process parameters as well as circuit parameters. To characterize a particular process, the parameters of the device models are provided values that correspond directly to the process being used.

A detailed description of how the dynamic data was generated can be found in a previous report.[2]

Briefly, however, each cell was simulated as follows. All transistors were simulated by a device model that included its mask geometries; electrical characteristics like threshold voltages; intrinsic capacitances, process parameters values for mobility, gate oxide, field oxide thickness and permitivity; effect of lateral diffusions expressed in terms of modified channel length; and resistance associated with the polysilicon gate and intracell connections. Each cell was analyzed with a load that consists of a series resistor and capacitive load. The series resistor represents

[2]"CMOS Array Design Automation Techniques", Final Report, Contract NAS12-2233 Mods. 6 and 11, NASA MSFC, May 1975.

the anticipated average resistance that a typical cell will be driving as a result of polysilicon interconnections. In addition, the cell being analyzed is driven by an inverter circuit which is designed to provide a signal that simulates the input signal it normally encounters in a CMOS/SOS LSI array environment.

A key to the accuracy and reliability of the results produced by the analysis and simulation techniques lies in the accuracy and validity of the values used to define the parameters of the device models. To date, RCA has produced more than 50 CMOS/SOS LSI arrays including at least four test chips. Although all of the test chips, including the one described in the referenced NASA final report,[3] were designed for different purposes, each one had special circuits designed to characterize the process and generate device-model parameter values. Then as the various functional CMOS/SOS arrays were fabricated and tested, the values of the parameters were both improved and updated. In this way, the accuracy and validity of the model are established with a corresponding increase in the accuracy and validity of the performance predicted by the simulation techniques. And, as additional CMOS/SOS LSI arrays are produced using the CMOS/SOS standard cell family, the model and its parameter values will continue to be improved and updated.

Although the stage propagation delays and transition times given in the data sheets are specifically for a 10-volt V_{DD}, they can be used to a first-order approximation to provide corresponding cell information at supply voltages other than 10 volts. For example, at 5-volt V_{DD} and assuming a threshold voltage for both P and N at 1.5 volts, the delay will be increased as compared to the 10-volt data as follows:

$$\text{Increase in stage delay at 5 V} = \left(\frac{(10 - 1.5)^2}{(5 - 1.5)^2}\right) \bullet \left(\frac{5}{10}\right) \bullet (0.8) = 2.4$$

The 0.8 factor in the equation is an empirical parameter.

f. Additional Cell Data

(1) D-Type, Master/Slave Flip-Flop (Cell No. 2820)

This cell is a true master-slave flip-flop designed for various register applications. With the addition of an external inverter, such as the 1310 or 1520 cell, it may be used for counter and toggle applications. Information is stored by means of tristate type devices, ensuring a data input characteristic that is purely capacitive. Data present at the "D" input is transferred to the "Q" output during the negative-going transition of the clock pulse. Loading the master flip-flop is initiated on the positive-going edge of the clock pulse.

[3] Ibid.

Operating Characteristics

- Clock should remain in the high state for a minimum of 22 ns to ensure a proper transfer of the data information into the master flip-flop.
- The clock should remain in the low state for a minimum of 20 ns to ensure a proper transfer of the master data to the slave flip-flop.
- The clock transition (10-90%) edge time should be kept below 60 ns.
- For output loading on "Q" greater than 0.4 pF, a minimum of 26 ns must be allowed to transfer the data to the slave and latch it in.

The cell is implemented with a combination of functional, transmission gate, and tristate logic. The transmission devices are used to connect (and disconnect) the master and slave storage devices from the "D" input and master rank, respectively. Each storage element is implemented with a single inverter and a low conductance feedback tristate device. Information is held by means of the smaller, high-impedance tristate inverter. The outputs of these tristate inverters are disconnected while their particular flip-flop is being loaded. Latch-up occurs during the transition time of the clock signal - during the falling edge for the master flip-flop and during the rising edge for the slave flip-flop. At this time, the transmission devices are disconnecting. When the clock signal is high, the logical level at the "D" input is propagated through the first transmission device and loaded into the inverter of the master flip-flop. When the clock signal goes from a high to a low (1 to 0) state, two simultaneous events occur. The master's tristate begins to maintain and define the logical level at the input to the master rank, and the input transmission device begins to isolate the master rank from the "D" input. Concurrent with these events, the second transmission device begins to connect the slave to the master. Opposition from the slave's feedback tristate is eliminated by disconnecting the output from this node.

(2) Off-Chip Inverting Buffer Pad (Cells No. 9060 and 9070)

These cells are designed for driving large off-chip capacitive loads. In order to increase the gate density of the arrays using the drivers, the cells have been incorporated into an output pad design. Consequently, they are placed in the pad area. The two cells differ only in their ground and power bus connection.

Section III

CONCLUSION AND RESULTS

The characterization and documentation of the CMOS/SOS high-speed, single-ended, standard cell family was expanded to 38 cells, which had been developed on other programs that included both government supported efforts and internal programs. To facilitate the addition of new cells to the library in the event that the need arises, as well as to facilitate the cell data sheets as design tools, the cell data sheets were documented in the High Speed CMOS/SOS Standard Cell Notebook.

To demonstrate the high speeds achievable in CMOS/SOS LSI chips made with these standard cells, as well as to demonstrate the correlation between measured results and performance predicted by computer simulation and analysis techniques, experimental results obtained from measurements on five different CMOS/SOS LSI chip types are included and described in this report. Measurements on these arrays, as well as on a complex multilayer ceramic substrate containing 11 CMOS/SOS LSI arrays (the equivalent of 3500 gates, which are used on a 32-CMOS/SOS computer being constructed for MSFC, Huntsville, Ala.) shows stage delays, in the actual chip environment, in the 4- to 6-ns range. The measured results, as shown in the technical discussion of the report, correlate very closely with the delays estimated on the basis of the delay and dynamic data included on the standard cell data sheets. In effect, then, the accuracy of the information on the data sheets, especially for those particular cells on the various chips made to date, is demonstrated to be within reasonable design limits and constraints.

Debugging and exercising of the enhanced automatic placement and routing programs, which includes the multiport (double entry) automatic placement and routing programs in addition to the single input version, eliminated a substantial number of 'bugs', normal to new and large programs, and resulted in substantially improved programs in terms of their operational characteristics.

Section IV

RECOMMENDATIONS

Although the CMOS/SOS circuits in general and the standard cells in particular have already achieved 4 to 5 ns stage delay in a system environment as evidenced by the measured LSI data on the NASA-MSFC SUMC-III program, even higher speeds will be realized when mask channel widths of 0.25 (effective 0.2 mil) are incorporated into future designs. These further channel width reductions will be the result of improvements in current processes as well as the maturing of new processes in which effective channel width is determined by diffusion techniques. However, the further reduction of channel width to the 0.15 to 0.2 mil length (or even smaller) strains the applicability of a one-dimensional model as is currently used in the MOS simulation technique. It is necessary to develop, evaluate, and validate a two-dimensional model so as to extend the accuracy of the simulation technique to narrow channel devices. Such validation should include a theoretical description of such a model and a test device from which experimental measured results can be obtained.

Although the Double-Entry Automatic Placement and Routing Program is a recently developed capability, it has already produced some of the densest LSI chips yet generated by completely automatic layout techniques. Still, there is considerable potential for improvements in the capability and performance of the program as well as in the applications and technologies to which it can be applied. One of the ways in which the program can be further improved significantly relates to the 'Natural Flow' concept for defining, designing, and interconnecting standard cell logic. 'Natural Flow' refers to a recently developed standard cell concept in which the cells and their interconnections have characteristics that closely parallel the input-output locations of the logic gates and the interconnectivity of the original logic input data. Further effort in this particular area is recommended.

In addition to this, a new application area for the standard cell approach is being recommended for further effort — Integrated Injection Logic. An initial effort has already been started, with the specific objective of defining the optimum way in which to develop the first successful and useful bipolar standard cell capability using some form of Integrated Injection Logic. Continued effort in developing and demonstrating the cell family whose design approach was determined and selected during these previous efforts is highly recommended.

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