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NASA Technical Memorandum 79262

MULTIPLE SPEED EXPANDABLE
BIT SYNCHRONIZER

James M. Budinger
Lewis Research Center
Cleveland, Ohio

August 1979
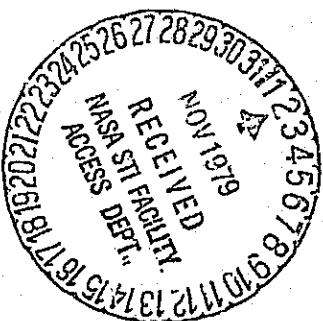
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INTRODUCTION

Several digital codes are appropriate for high density data recording on instrumentation magnetic tape. One commonly used is Biphase-Level (BIΦ-L) code. Embedded within BIΦ-L data is Non-Return-to-Zero Level (NRZ-L) code and a synchronous clock. Code conversion is accomplished through the use of a bit synchronizer. After first extracting the clock from the BIΦ-L data, the bit synchronizer uses it and the BIΦ-L to generate the NRZ-L data (see references).

Single speed bit synchronizers are commercially available for a specified data rate. In some units, interchangeable plug-in modules are used to accommodate data rate changes. This paper describes a bit synchronizer designed to operate over a range of four recorder playback speeds in the basic version. Through a simple expansion, operation can be extended to eight or more multiples of a base data rate. Since the clock and NRZ-L are both generated directly from the BIΦ-L data, the bit synchronizer accepts fluctuations in data bit rate (due to recorder playback error) with no loss of accuracy.

Although commercially available bit synchronizers offer data conversion without initial calibration for specific data rates, this design offers many features which make it a more desirable alternative. First, its simple layout makes it ideal for implementation within existing equipment so that no external synchronizing unit is necessary. As such, the bit synchronizer may be especially useful in applications where size and weight constraints are significant.

Secondly, the circuit is easily initialized to operate at the user's specific data rates and can be just as easily modified if requirements change. In addition, its expandable nature and operation at multiples of a base data rate make this bit synchronizer directly compatible to standard instrumentation tape recorders which have multiple speed increments. Finally, the savings in cost and power consumption are substantial when compared to elaborate signal conditioner/bit synchronizers which may in certain applications possess more capability than is actually needed. In general, this design meets the requirements for an easily fabricated, low-cost, auto-sensing bit synchronizer in systems utilizing four or more multiples of a base BIΦ-L data rate from less than 1 bit/second to over 1×10^6 bits/second.

GENERAL DESIGN EXPLANATION

Within each data cell (time allocated for one bit) the BIΦ-L makes one level transition according to the logic state of the bit. A low to high transition

represents a "zero" (0 volts) data bit, and a high to low transition represents a data "one" (+5 volts). These transitions are present at the center of every data cell and are referred to in this paper as primary transitions. Secondary transitions are generated when successive data bits are the same logic state. These transitions are nonperiodic and must be disregarded by the circuitry which generates the clock.

A block diagram of bit synchronizer functions is shown in figure 1. Input BIΦ-L is referenced to TTL compatible levels with zero-crossing points determining the TTL edge locations. In order to select the proper clock to be synchronized to the data, the bit synchronizer counts the number of BIΦ-L transitions in a specific timing period. Based on the transition count, a clock rate decision is made and the proper timing components are selected.

A dual one-shot extracts the clock from BIΦ-L using the timing components to accurately position the clock edges. NRZ-L is generated from the clock and BIΦ-L by an edge triggered flip-flop. The relationship between BIΦ-L and the embedded clock signal and NRZ-L is shown in a timing diagram (fig. 2). In extracting the clock, this bit synchronizer introduces a 90° phase shift so that the clock and NRZ-L will lock on to only the primary BIΦ-L transitions, and accept temporary data rate fluctuations of up to one-half the frequency of the base data rate.

DETAILED CIRCUIT DESCRIPTION

As shown in figure 3, this design employs standard 7400 series TTL logic. For additional power savings and an increased upper limit on bandwidth, the 74LS00 series can be used. Circled letters "A" through "G" in the schematic show the location of logic traces displayed in both Timing Diagrams (figs. 4 and 5).

BIΦ-L data greater than 0.8 volt p-p in magnitude is the only input necessary to accurately extract synchronized NRZ-L data and clock (fig. 4(a)).

After inversion in the 741 op amp (IC1) a differential signal is applied to the 8820 line receiver (IC2). Accepting a maximum input voltage of 30 volts p-p, the line receiver produces a zero referenced, TTL compatible signal. The Schmitt-trigger NAND inverts the BIΦ-L back to normal and squares up both edges of the data (fig. 4(b)).

Each one-shot in IC4 senses either the positive or negative transitions of the BIΦ-L and outputs inverted 1 microsecond pulses for every edge detected. The gating of these two signals yields a positive pulse train (fig. 4(c)). Selection of the proper clock rate is made according to the number of transition

pulses in a given timing period. These pulses are sent serially to three 7493 divide-by-eight counters (IC5, IC6, IC7). At the same instant, the first pulse of the train activates the timing period (IC8a), and resets the counters. Additionally, the stream of pulses is used to produce the leading edge of the clock in IC16a.

During the timing period, the three counters output a 12 bit word indicating the total transition count since they were last reset. A 7475 quad latch (IC9) monitors four of the most significant bits of that word.

When the first one-shot in IC8 completes the timing period, the $\overline{Q}$, output transitions to a high level. This level enables the quad latch where inverted data is transferred to the $\overline{Q}_n$ latch outputs. The next pulse in the train starts the timing period again causing $\overline{Q}_1$ in IC8a to return low. This negative going transition latches the data that was present on IC9 at the time of the transition. Finally a 2 μS pulse resets the counters when the same negative edge is sensed by the second one-shot, IC8b.

A Priority Encoder (IC10) selects the highest-order data line from among the four latch outputs. The selected line is encoded into two bit binary. Once a clock rate selection is made by the priority encoder, its output will remain constant unless a different input bit rate is chosen. This binary output is decoded into one line by a three-to-eight line decoder (IC11). More of the decoder capacity may be used in the expanded version.

Both clock offset and duty cycle adjustments are made through one-shot timing resistor selections. Dual Clock Drivers (Motorola MMH0026) and diodes (1N916) isolate all but the selected timing resistors from power supply voltages. To insure stable clock output, the offset one shot (IC16a) must lock on to the primary transitions of the BIΦ-L and disregard the secondary ones (fig. 4(d)). Selecting the timing resistor/capacitor combination for 90° phase offset from the primary transitions allows for the greatest fluctuation in bit rate. Gating of the $\overline{Q}_n$ output of IC16a with the BIΦ-L prevents false triggering of the one-shot.

Data conversion errors will only occur momentarily during start-up sequences or input data rate changes. Should the offset one-shot fire on a secondary transition immediately following start-up, it will lock there only until the first time successive data bits change state. From that point on, the leading edge of the clock will be properly offset to 90° phase lag from the primary transitions.

Varying the timing resistance for one-shot IC16b controls the duty cycle of the clock (fig. 4(e)). Increasing the current drive through an open collector inverter allows the clock to be used in driving additional circuitry. For both

the offset and duty cycle one-shots, precision timing components should be used. Resistor and capacitor values should be selected within the manufacturer's recommended ranges for one-shot operation.

Extracting NRZ-L data from the BIΦ-L is easily accomplished once a 90° phase offset clock has been derived. A 7474 positive edge-triggered D-type Flip Flop produces NRZ-L corresponding to the BIΦ-L state on its data input at the instant of the negative going clock transition (fig. 4(g)). Both normal and inverted data are available as outputs. Actual circuit traces at the locations lettered in the schematic are shown in figure 5.

TIMING PERIOD SELECTION

The timing period is selected so that the most significant bit of the BIΦ-L transition count has just changed state prior to completion of that period. During a constant timing period, each higher multiple of base data rate will yield twice the transition count of the next lower speed. Ideally the timing period should end immediately following the state change of the most significant bit.

As shown in figure 6, n bits of BIΦ-L data contain 2n transitions when the data is a repetition of one level. When the data is a continuous high to low level alternation of n bits there are only n transitions. An "average" line of BIΦ-L data would contain elements of each – that is, both high and low bit levels and bit level repetitions and alternations. Accordingly, n bits of average BIΦ-L data must contain between n and 2n transitions. A count of about 1.5 n might be expected.

Once the slowest data playback bit rate has been established, the proper timing period can be determined. If for example a data tape contains 1000 BIΦ-L bits/second recorded at $3\frac{3}{4}$ inches/second, a 1-second segment of that tape will contain between 1000 and 2000 transitions when played back at the same speed. In this case a timing period of 1 second might be chosen. Within that period a binary count of 2^{10} or 1024 transitions would most likely be reached. However, the next greater significant bit representing a count of 2^{11} or 2048 would never change state.

In general, the timing period is selected so that the total transition count during that period falls between two significant bit changes, 2^{n} and 2^{n+1}. If in the preceding example the tape was played back at $7\frac{1}{2}$ inches/second instead of $3\frac{3}{4}$, the transition count would reach between 2^{11} and 2^{12} during the 1 second timing period. Only one initial adjustment of the timing period is necessary. Within that period each of the four most significant bits will represent one data rate.

The longer the timing period, the higher the percentage of accuracy in determining the proper clock rate. A new clock rate decision is made at the end of every timing period. However the circuitry beyond the priority encoder operates consistently based on the last decision. Consequently, the only clock dropout occurs when the change in data input rate approaches a factor of 2.

EXPANDED VERSION REQUIREMENTS

A desirable feature of this bit synchronizer design is its simple expansion to eight data rates. The expanded version is ideally suited to operation with seven speed digital recording equipment (15/16 in/sec to 60 in/sec).

One additional cascaded binary counter and one quad latch are required for operation at greater than 4 data rates. Both the priority encoder and octal decoder will handle up to eight data rate selections.

To generate the clock for each supplemental data rate, two additional clock drivers, diodes, precision resistors and potentiometers are required. Each configuration supplies power to a separate timing resistor just as in the four-speed version. The factor limiting expansion of the basic design as previously described is the range of pulse widths obtainable from the offset and duty cycle one-shots using a single value of timing capacitance.

CONCLUDING REMARKS

The multiple speed expandable bit synchronizer was designed for installation in an Inertial Navigation System Data Decoder. Presently, two bit synchronizers, both wire-wrapped in the four-speed version (BIΦ-L data rates from 1725 to 13 800 bits/sec), are in use in separate Data Decoders. The requested feature that initiated this design was the ability to automatically sense the BiΦ-L data rate and synchronize the proper clock to the data. This design eliminated a front panel Tape Speed Select control and an external signal conditioner/bit synchronizer unit. For systems utilizing a range of BIΦ-L recording rates, this design offers accurate, auto-sensing bit synchronization.

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Del Guercio, Vito: Bit Synchronizer Needs no Adjustments as Data Rate Varies. Eng. Design News, vol. 21, no. 1, Jan. 5, 1976, pp. 70-71.
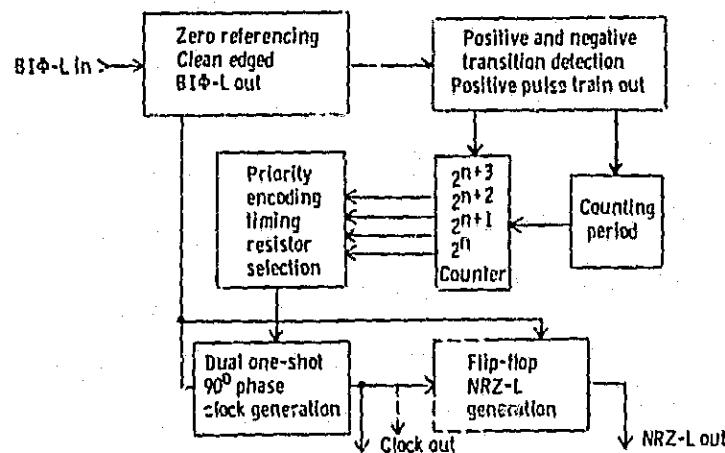
Figure 1. - Block diagram of multiple speed bit synchronizer functions,
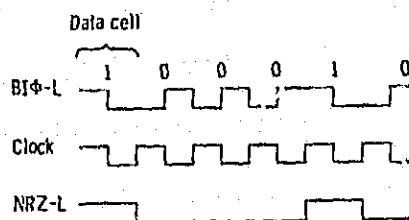
Figure 2. - Timing diagram showing relationship between clock and NRZ-L levels embedded in BIΦ-L data.
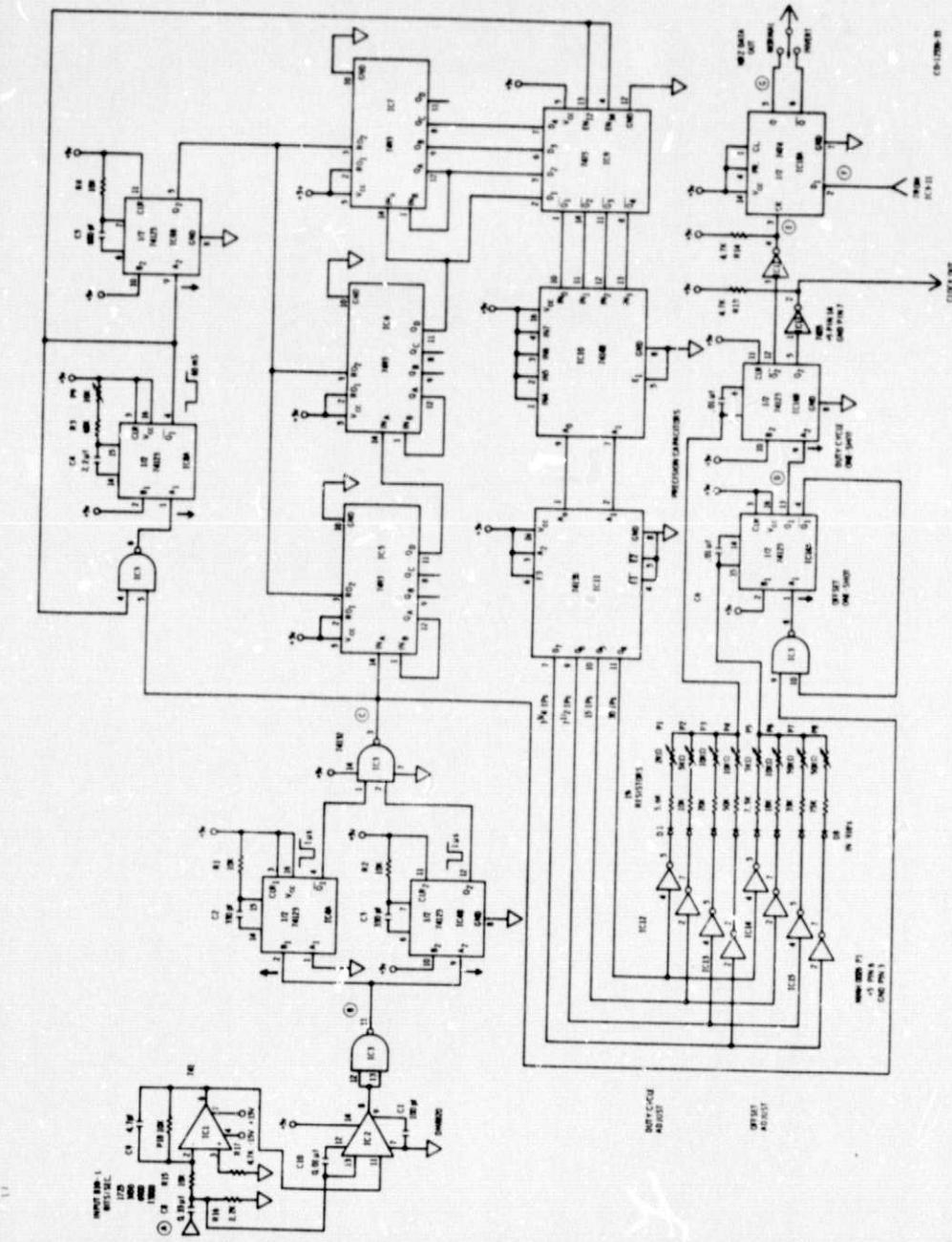
Figure 3. - Four speed expandable BIO-L to NRZ bit synchronizer JMB 12/13/77.
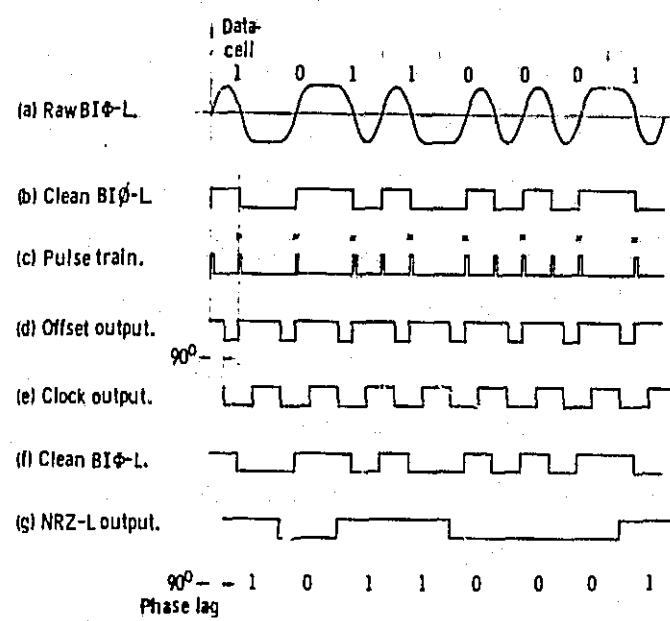
Figure 4. – Timing diagrams (see circuit diagram fig. 3 for trace locations).
(a) BIΦ-L recorder output; (b) Clean BIΦ-L TTL compatible levels; (c) Transition pulse train – x denotes primary transitions; (d) Offset one-shot Q output – note 90° phase offset from primary transition; (e) Duty cycle one-shot Q output - clock; (f) Clean BIΦ-L repeated for convenience; and (g) Extracted normal NRZ-L output.
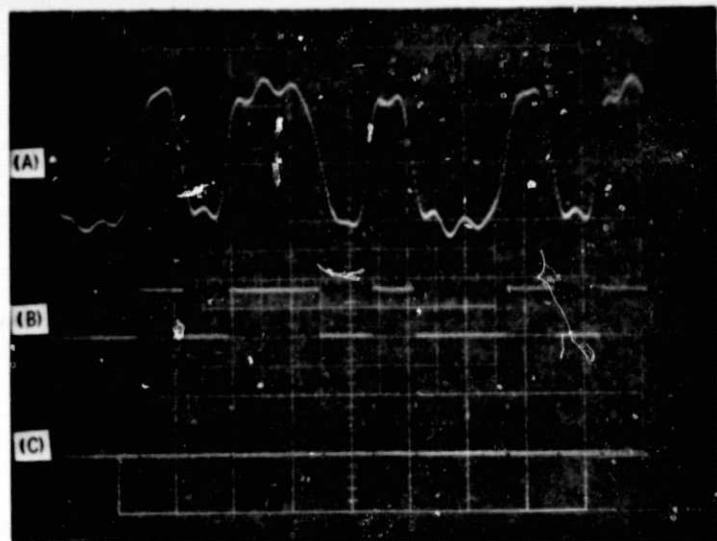
Trace A   1 volt/cm
Trace B   5 volts/cm   Sweep 0.1 ms/cm
Trace C   5 volts/cm
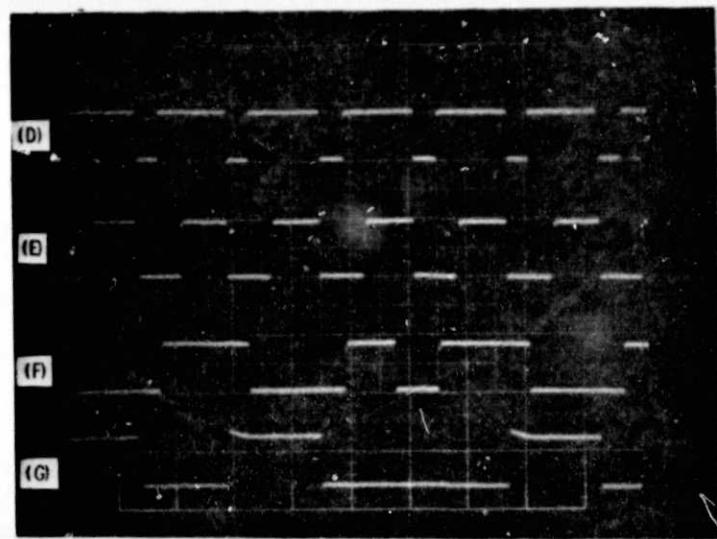
Trace D, E, F, G   5 volts/cm
Sweep 0.1 ms/cm

Figure 5. – Actual circuit traces corresponding to the timing diagrams of Fig-
ure 4. (A) BIφ-L recorder output, (B) clean BIφ-L, TTL compatible levels,
(C) positive pulse train, (D) offset one-shot output, (E) duty cycle one-shot
output, (F) clean BIφ-L, and (G) NRZ-L extracted from BIφ-L in trace (F).
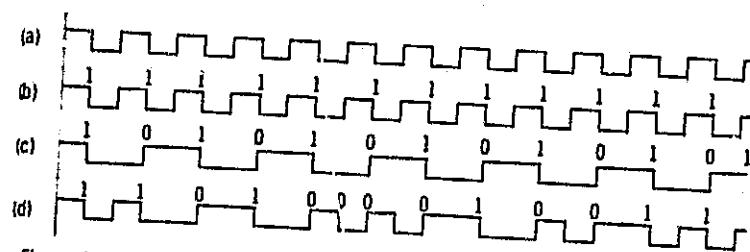
Figure 6. - n-Bit transition diagrams: (a) Clock in sync with BIΦ-L; (b) Repetition of one data state; 2n transitions; (c) Alternation of data status; n transitions; (d) Average BIΦ-L (see text); ~1.5 n transitions.
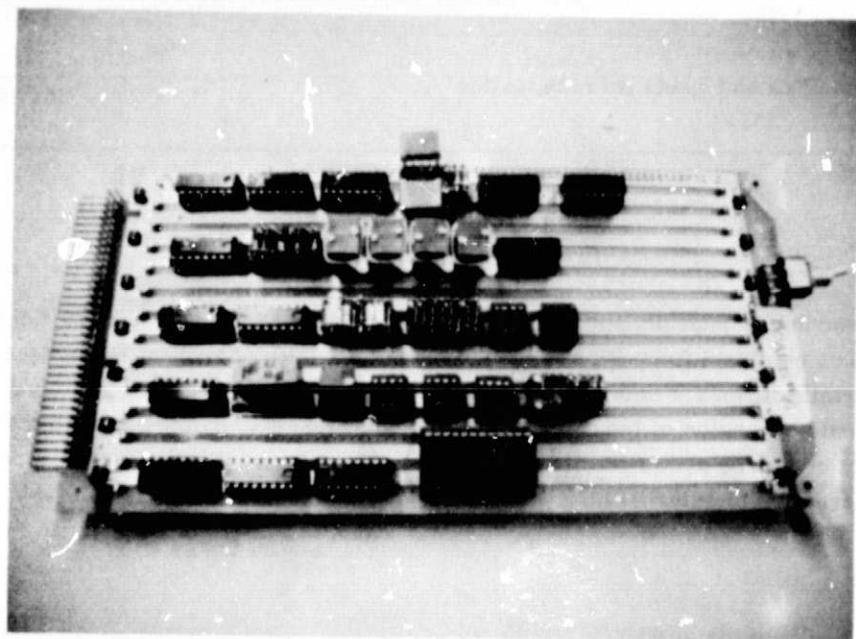
Figure 7. - Wire-wrapped four-speed version bit synchronizer.