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DEVELOPMENT AND FABRICATION OF LOW 'ON' RESISTANCE HIGH CURRENT VERTICAL VMOS POWER FETS

by

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16. Abstract

This report describes the design of a VMOS Power FET exhibiting low 'ON' resistance, high current as well as high breakdown voltage and fast switching speeds. The design which is based on a 1st-order device model, features a novel polysilicon-gate structure and a field-plated groove termination to achieve high packing density and high breakdown voltage, respectively.

One test chip, named VNTKI, can block 180 V at an 'ON' resistance of 2.5 ohm. A 150 mil x 200 mil (.19cm2) experimental chip has demonstrated a breakdown voltage of 200 V, an 'ON' resistance of 0.12 ohm, a switching time of less than 100 ns, and a pulsed drain – current of 50 A with 10 V gate drive.

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NOTE: Figure numbers 21, 38, 51, 52, 63, 64, and 65 were not used in this report.

1.0 SUMMARY

The objective of this program was to develop a low 'ON' resistance, high current Vertical Metal-Oxide-Semiconductor (VMOS) power Field-Effect-Transistor (FET). Specifically, the program objectives called for development and fabrication of a 200 Volt, 0.1 ohm, 20 Ampere experimental VMOS power FET.

Various MOSFET technologies were analyzed with respect to four key parameters:

* 'on' resistance ($R_{DS(on)}$)
* current ($I_{D(on)}$)
* breakdown (BV_{DSS})
* switching speed (t_{on} and t_{off})

VMOS was selected based on the above criteria.

D.C. parameters of VMOS FETs were then modeled. The study identified two major components of 'ON' resistance ($r_{DS(on)}$): channel resistance (r_{ch}) and drift resistance (r_{drift}). To lower r_{ch}, high packing density was required. This would also increase transconductance (gm). To lower r_{drift}, which was sometimes the single most dominant component for $r_{DS(on)}$, two additional factors were considered: one was the percentage utilization of the epitaxial (epi) cross-sectional area, the other was the use of low epi resistivity and a thin epi layer to achieve the specified breakdown voltage.

To maximize utilization of the epi cross-sectional area, the source, gate and drain electrodes were put on a different plane so that they could overlap one another. This was termed the "three-plane conduction" concept. One way to implement this concept was to put the drain contact at the bottom of the chip, the source metal on top of the chip and the gate electrode of polysilicon sandwiched in between. One practical way to

realize this sandwiched poly-gate was to arrange the V-grooves in what we termed K-structure. In this way no inactive silicon real estate was necessary for source bus bars and source bonding pads. Besides, the V-grooves could be arranged closer. The result was extremely high packing density with normal design rules.

Placing of the source metal on top of the chip, in turn, caused one very important consequence: the current carrying capacity of metallization on the chip was increased tremendously. In fact, for normal operation, the current density in the source metal was not a limiting factor anymore.

To use low epi resistivity and thin epi to achieve high breakdown voltage, a novel V-groove termination with source field plate (SFP) was developed. This termination scheme was supplemented by a recessed charge-control (RCC) ring to control surface ion spreading, thus ensuring device stability and reliability.

The above features were incorporated into a test chip named VNTKI. With an active area of .01 cm^2, an $r_{DS(on)}$ of 2.5Ω at 180V breakdown voltage was achieved.

The final step was the fabrication of an experimental device named VNS. With an active chip area of 23,330 mil^2 or .145 cm^2, the ratio of channel width (W) to channel length (ℓ) approached three quarters of a million. Initial results showed that project goals were within reach: $r_{DS(on)}$ of .12Ω and a BV_{DSS} of 200V were achieved on separate wafers. Switching speed of about 100 ns and pulsed drain current of 50A with 10V gate drive were also achieved. These initial results indicated a step-function improvement over the existing VMOS power FET designs. In fact, the era has come whereby VMOS power FETs are competing very aggressively with bipolar power transistors in power handling capability on a chip size basis.

2.0 INTRODUCTION

The trend for future electrical power processing systems is increased voltage and/or current (power) levels with a faster switching speed. Availability of new and better power transistors is an important key to realizing this trend. In 1976, Siliconix of Santa Clara, California, announced and marketed commercially a new family of devices called VMOS power Fet's. This new device quickly established itself to be an important factor in the power transistor market.

The device, being a MOSFET, is easy to drive and offered switching speeds in the nano second range. An experimental device also demonstrated that it was capable of blocking reverse breakdown voltages in the 200 to 400 V range. The lower limits of drain to source 'ON' resistance ($r_{DS(on)}$) however, was left to be explored. The $r_{DS(on)}$ is an important parameter, as it determines directly the power dissipation of the switching device when the device is conducting high current. Exploring low 'ON' resistance per unit area was the goal of this program.

This report documents the results of the first 15 months of effort funded by NASA under contract number NAS3-21034. The primary objective of the program was to develop a design concept and a basic processing technique to explore the lower limits of MOSFET 'ON' resistance. The secondary objective was to determine the maximum current we could produce from the device. These objectives were to be achieved in conjunction with comparable blocking voltage and switching speed.

Specifically, the program called for the development and fabrication of experimental power MOSFET switching devices. The device would be capable of blocking at least 200 volts D.C. when OFF, switching 10 amperes D.C. with a drop of 1 volt or less ($r_{DS(on)} \leq .1\Omega$) when ON and operating at a switching speed of about 50 nano seconds. The above major specifications must be achieved with a reasonable and practical chip size. The key parameters used were, in order of importance:

1. 'ON' resistance ($r_{DS(on)}$) per unit area

2. Current ($I_{D(on)}$)

3. Voltage (BV_{DSS})

4. Switching speed (t_{on} and t_{off})

You will find that throughout the report, the discussion is centered on these four key parameters.

The strategy used to meet these objectives is as follows:

First: Survey MOSFET technology in breadth and study vertical VMOS device modeling in depth. The purpose of this phase was to identify the best technology. Section 3.0 of this report entitled "Preliminary Technical Discussions" reports the reasons that the polysilicon gate VMOS process was selected.

Second: Identify the critical problem areas. By means of test patterns, carry out an experimental investigation to verify and optimize the tradeoffs for the design concepts and processing technique proposed. Section 4.0 entitled "Polysilicon-Gate VMOS Process Development", covers the activities and results of this second phase.

Third: Fabricate the experimental device using the design and process developed in the second phase. Section 5.0 entitled "Fabrication of Experimental Device (VNS)", covers the activities and initial results of this phase.

By the time the second phase of the program was completed, it became apparent that 100% completion of phase 3 (which is design, fabrication and testing of experimental device) was too ambitious for the timing and funding the program originally planned. Therefore, it was agreed that phase 3 would be pursued to the point

where the initial results of the first wafer run could be evaluated.

This report was designed to reflect the highly exploratory nature of this program. Great emphasis was placed on discussing the reasons behind the choice of the technology, and the results of feasibility studies. Areas such as manufacturability, reliability, packaging, characterization and circuit application were considered, but no specific efforts were investigated in these areas. Also, the reader's basic knowledge of the physics of operation and the fabrication technology of transistors and microcircuits was assumed.

3.0 PRELIMINARY TECHNICAL CONSIDERATIONS

This section begins our survey of MOSFET technologies associated with power MOSFET switching devices. The d. c. VMOS model will then be described. The third topic of this section summarizes the reasons for selection of the VMOS technology.

3.1 Survey of MOSFET technology.

The objective of this task was to put the various MOSFET technologies in perspective so that the most promising technology could be selected to meet the objectives of this project. These technologies will be discussed with respect to the following major parameters with cost and reliability assumed to be comparable.

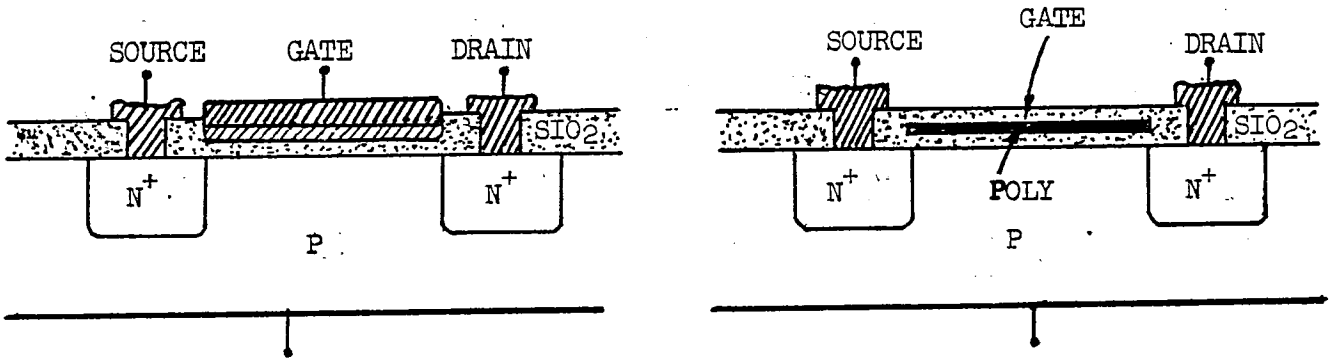
1. 'ON' resistance
2. Current
3. Voltage
4. Switching Speed

Please note that discussion is restricted to the N-ch enhancement-mode MOSFET only.

3.1.1 Conventional MOSFET

The conventional MOSFET structure shown in Figure (1) has many inherent advantages. It is voltage controlled and has a high input impedance. Therefore, it is easy to drive. It is also inherently fast because it is a majority-carrier device. However, the source and the drain are delineated photolithographically. Furthermore, the channel or body region has lower carrier concentration than that of the source and drain. Finally, all source, gate and drain contacts are on the same side of the chip. These three factors severely limit the structures' usefulness in power device application because of:

1. low packing density leading to associated high 'ON' resistance and low current;
2. low voltage (typically 30-40V) breakdown; and,
3. low power handling capability.



(A) METAL GATE

(B) SILICON GATE

Figure (1) Conventional MOSFET Structure (Lateral)

3.1.2 Offset-gate MOSFET

To increase the breakdown voltage of a convention MOSFET, an offset-gate (or stacked-gate) was developed (ref. 1 and 2). In an attempt to get higher power, a vertical offset-gate MOSFET was also developed. See Figures 2 and 3, (ref. 3)

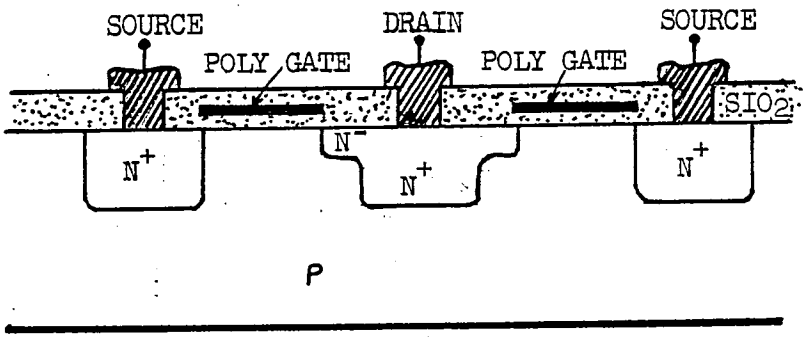


Figure (2) Offset-gate (lateral MOSFET)

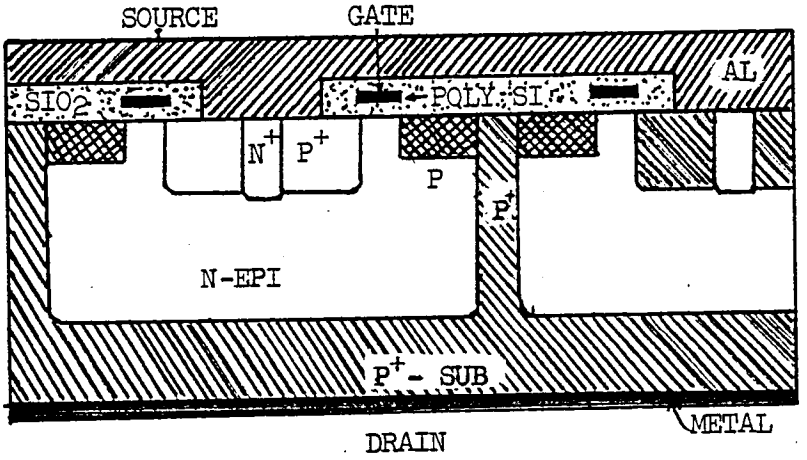


Figure (3) Offset-gate (vertical MOSFET)

In this new structure, the source and drain are still delineated by photolithography. Higher BV_{DSS} (approximately 200V) was achieved by having the gate offset from the drain and completing the channel with a lightly-doped impurity of proper dopant between the drain and the edge of gate region. Because the n+ drain was still in contact with the relatively heavily- doped body region (approximately $10^{16}cm^{-3}$), the maximum voltage capability was limited by junction breakdown. Therefore, it was concluded that an offset-gate MOSFET was suitable for medium BV_{DSS} and medium $r_{DS(on)}$ applications only.

A close 'cousin' of the offset-gate structure is the development of 200V lateral MOS switch using a field plate and a floating intermediate drain, as shown in Figure (4) (ref. 7).

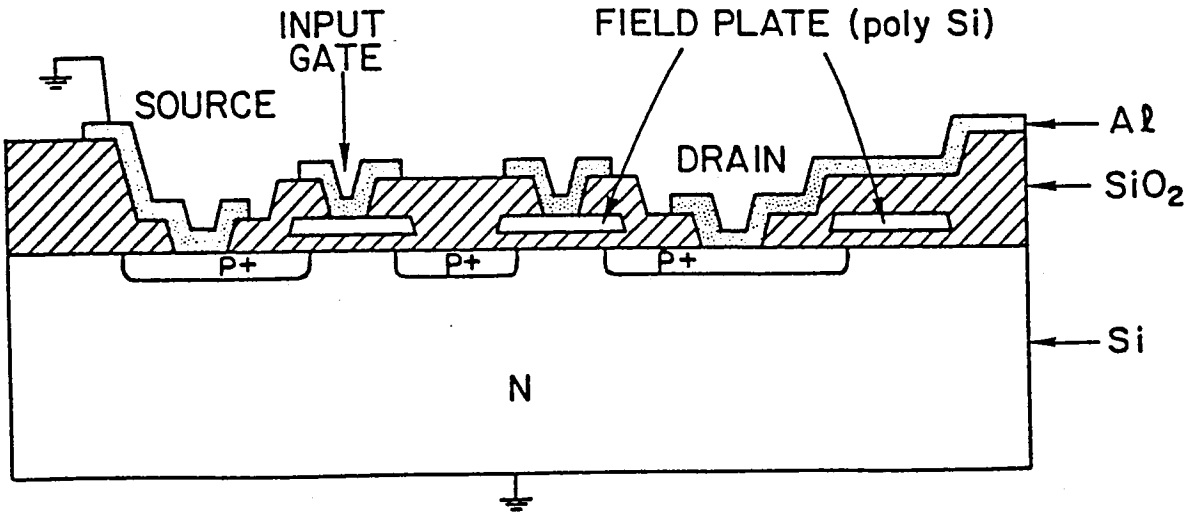


Figure (4) High Voltage MOSFET Switch Using Field Plate and a Floating Intermediate Drain

It can be seen in Figure (4) that this device is suitable for integrated- circuit applications. It has the same problem as other offset-gate structures in getting low $r_{DS(on)}$ per unit area.

3.1.3 DMOS - (Double diffused MOS)

A major milestone in the MOSFET development was the development of DMOS. (ref. 5) As the name implies, channel length was defined by the difference of two diffusion junction depths. Thus, a short channel length (approximately 1μ), and therefore high g_m, could be obtained.

One major feature of DMOS was the incorporation of a lightly doped drift region which served as 'buffer' between body (channel) and drain contact. Incorporation of this drift region had many consequences. On the minus side, this had resulted in an additional component for $r_{DS(on)}$. This additional component was called r_{drift}. On the plus side, channel length modulation was kept to a minimum because the body was more heavily doped than the drift region. By the same reason, a high BV_{DSS} was possible because of higher punch-through and junction breakdown. The third advantage of having this drift region was lower junction capacitance resulting in faster switching speed. See Figures (5 and 6)

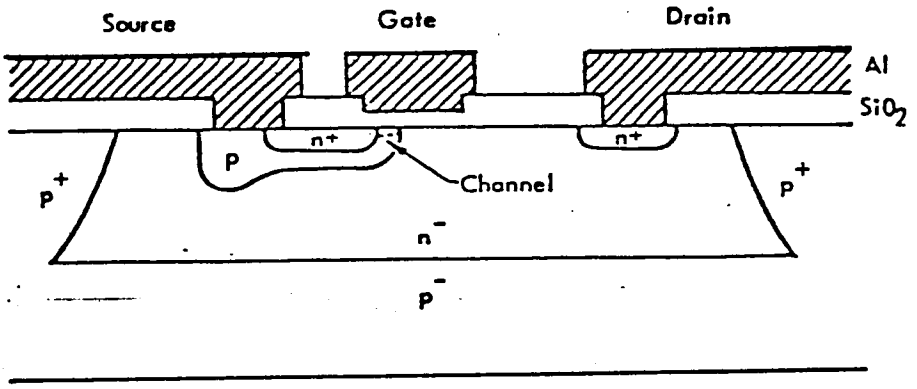


Figure (5) Lateral DMOS FET Structure

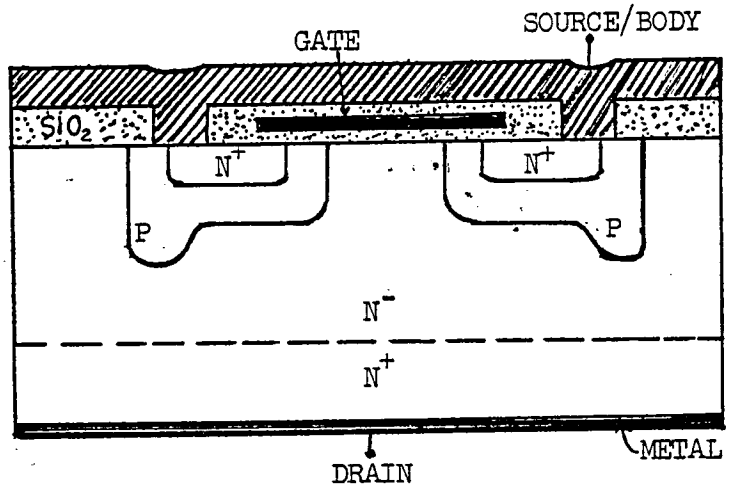


Figure (6) Vertical DMOS FET

3.1.4 VMOS

Pioneered principally by Siliconix, vertical VMOS was similar to DMOS except for the V-groove notch. It was this V-groove notch, however, that has pushed the performance of MOS power FETs to a new frontier never attained before. By virtue of the V-groove notch, the short channel length which is approximately vertical to the surface plane of chip can be realized not only by a double diffusion, but also by a double epi as well. The latter has made threshold control as simple as with the regular MOSFET.(ref. 6) It has also added flexibility in device fabrication. In addition, the V-groove notch results in lower $r_{DS(on)}$ because the vertical channel gives a shorter drift region for the carriers to travel. When operating in the linear region, the drift region underneath the V-groove gate is heavily accumulated. Thus, depending on the degree of V-groove penetration inside the drift region, the 'effective drift region' is even shorter which gives lower $r_{DS(on)}$ in terms of lower r_{drift}. See Figure (7).

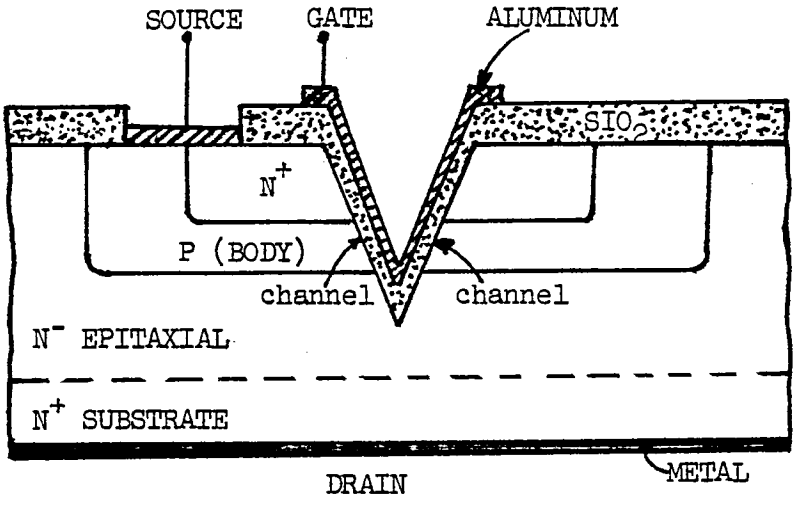


Figure (7) Vertical VMOS Power FET

VMOS technology can also take full advantage of several techniques used in bipolar technology to increase the breakdown voltage. Techniques such as mesa isolation, single or multiple field-limiting rings and a field plate (which help to push the junction breakdown to its theoretical limit) are possible with VMOS.

3.1.5 VMOS Selection Summary

From a power handling viewpoint, it is practical to eliminate all the lateral MOS approaches (i.e. source, gate and drain on the same side of the chip). From the $r_{DS(on)}$ and voltage breakdown viewpoint, we can eliminate the vertical offset-gate approach. The remaining technologies, vertical DMOS and vertical VMOS, can achieve high breakdown voltage. However, when it comes to $r_{DS(on)}$ per unit area, vertical VMOS has a decisive edge. The reasons are as follows:

1. The carriers of DMOS have to travel through a longer drift region thereby incurring more resistance due to the drift region.
2. For the same chip size, DMOS uses less epi cross-sectional area, thereby increasing the resistance (due to the drift region).

By this method of elimination, we concluded that vertical VMOS stands the best chance to get the lowest $r_{DS(on)}$ per unit area.

3.2 Basic Modeling of Critical Parameters (VMOS)

Once the vertical VMOS technology was selected as the vehicle to achieve the intended device specification, the next step was to predict the critical parameters, and to optimize the trade-offs.

The critical parameters are:

1. Threshold voltage (V_{th});
2. $r_{DS(on)}$ and g_m ($I_{D(on)}$);
3. Breakdown voltage; and,
4. Capacitances and switching speed.

3.2.1 Threshold voltage:

With about 2μ of channel length, VMOS is physically a short-channel device. Due to the drift region, which can be of one to two orders-of-magnitude lower in carrier concentration than that of the channel or body region, we see none of the so-called "short channel effect". The reason is that when a voltage is applied to the drain, most of the depletion layer of PN junction extends into the drift region rather than into the channel region. So the body charge underneath the gate oxide is relatively unaffected. In other words, the threshold voltage is independent of drain voltage. This is confirmed by Figure (8) where the 'body effect' of VMOS is measured, and we find that ΔV_{th} is a linear function of $\sqrt{V_{BS}}$. Therefore, the classical V_T equation applies; and the threshold voltage at room temperature is calculated as follows:

$$V_{TN} = -\left|\phi_{ms}\right| + \left|2\phi_f\right| - \left|\frac{Q_{ss}}{C_o}\right| + \left|\frac{Q_B}{C_o}\right| \qquad (1)$$

$$\left|\phi_{ms}\right| = .96V$$
$$\left|2\phi_f\right| = .52V$$
$$\left|\frac{Q_{ss}}{C_o}\right| = \frac{(2 \times 10^{11}) \times (1.6 \times 10^{-19})}{2.9 \times 10^{-8}} = 1.1V$$

$$Q_{ss} = (2 \times 10^{11})\ (q)$$

$$q = 1.6 \times 10^{-19} \text{ coul}$$

$$C_o = 2.9 \times 10^{-8} \text{ F}$$

$$\left|\frac{Q_B}{C_o}\right| = \frac{68.98 \times 10^{-9}}{2.9 \times 10^{-8}} = 2.38 \text{ V}$$

$$Q_B = \left(2\varepsilon_{si} \times \varepsilon_o \times q\ (NA)\ 2\ \phi_f\right)^{1/2}$$

$$= -68.98 \times 10^{-9} \text{ coul/cm}^2$$

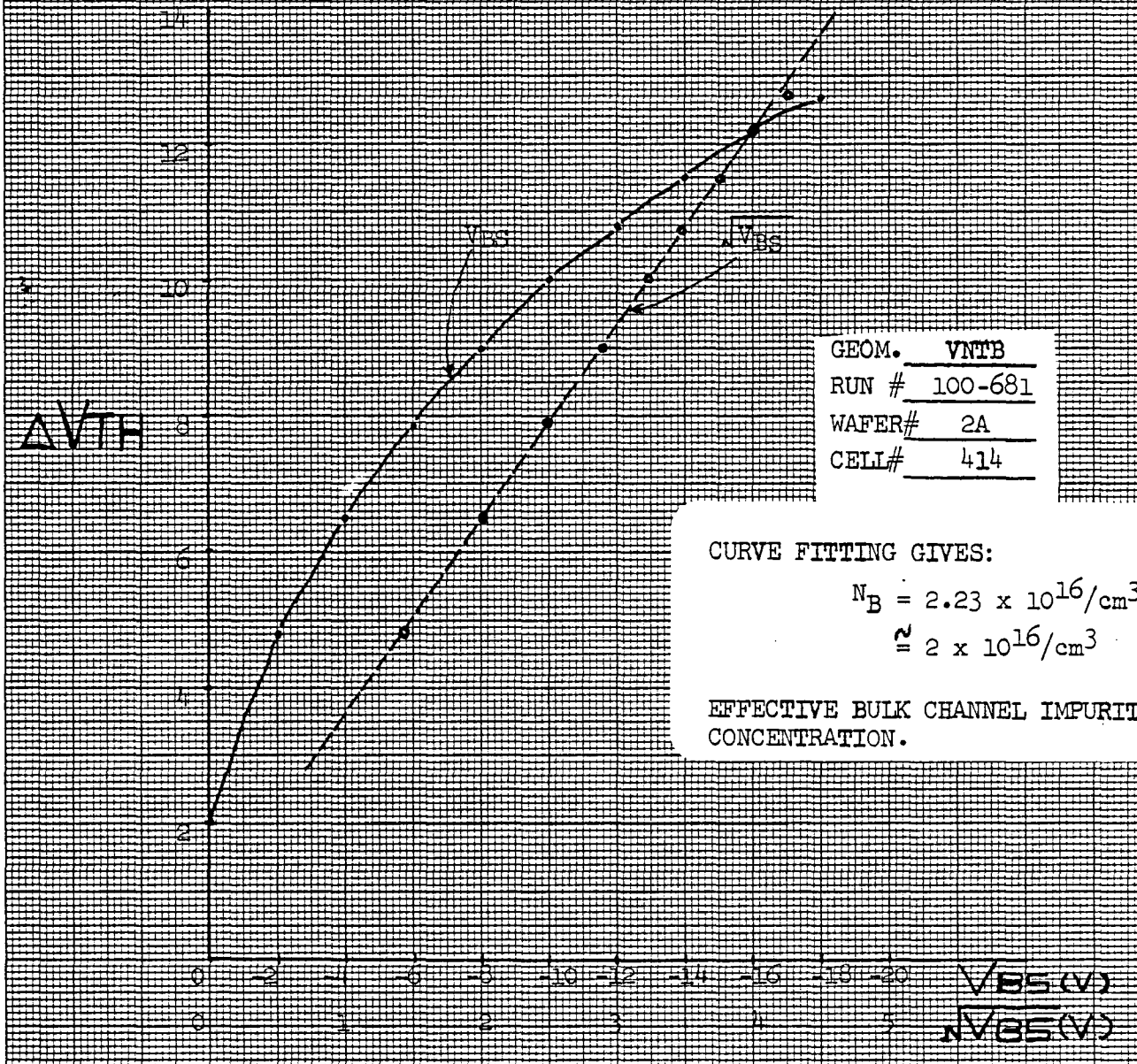
$$\varepsilon_{si} = 12$$
$$\varepsilon_o = 8.85 \times 10^{-14} \text{ f/cm}$$
$$NA = 2 \times 10^{16}/\text{cm}^3 \text{ (from figure (8))}$$

(The symbols are defined in reference 19.)

Substituting these values into equation (1), we get:

$$V_{TN} = -(.96) + (.52) - (1.1) + (2.38) = +0.84V$$

VTH vs VBS & √VBS



GEOM.	VNTB
RUN #	100-681
WAFER#	2A
CELL#	414

CURVE FITTING GIVES:

$N_B = 2.23 \times 10^{16}/cm^3$

$\cong 2 \times 10^{16}/cm^3$

EFFECTIVE BULK CHANNEL IMPURITY CONCENTRATION.

Figure (8) V_{th} vs V_{BS} α $\sqrt{V_{BS}}$

3.2.2 $r_{DS(on)}$

For the MOSFET, the linear region is characterized by $r_{DS(on)}$ and the saturation region by g_m which also determines drain current, $I_{D(on)}$. For VMOS, like the MOSFET, $r_{DS(on)}$ is the sum of all the resistive components encountered from source to drain, i.e.

$$r_{DS(on)} = r_S + r_{ch} + r_{drift} + r_{sub} + r_{contact} \qquad (2)$$

Generally speaking, $r_S + r_{sub} + r_{contact}$, take up only a small percentage of the total $r_{DS(on)}$. The important components are r_{ch} and r_{drift}.

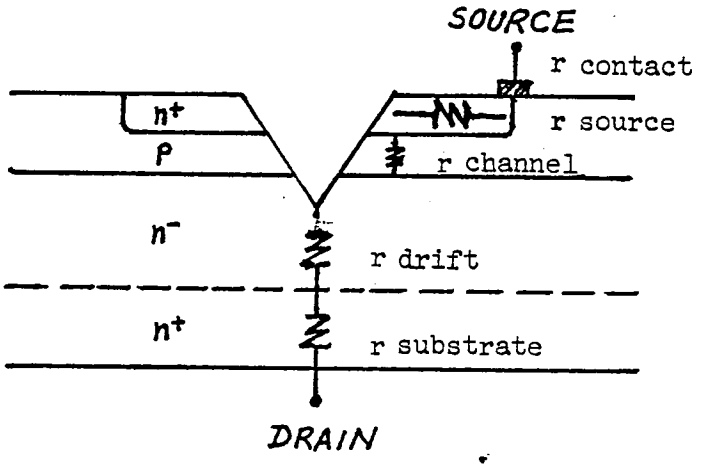


Figure (9) Resistive Components of VMOS

3.2.2.1 r_{ch}

r_{ch} is the channel 'ON' resistance. Since VMOS has no short-channel effect, one-dimensional analysis of the channel region holds, and r_{ch} can be estimated by the standard equation for long-channel MOSFET's.

$$r_{ch} = \frac{t_{ox}}{\mu_n E_{ox} E_o} \times \frac{\ell}{W} \times \frac{1}{V_{GS} - V_T - V_{DS}/2} \quad (3)$$

where t_{ox} is gate oxide thickness
E_{ox} is oxide dielectric constant (=4)
E_o is permittivity of free space (=8.86 x 10^{-14} F/cm)
ℓ is channel length
W is channel width
μ_n is mobility of electrons

3.2.2.2 r_{drift}

This is the spreading resistance due to the drift region or N-epitaxy layer. Generally, it can be broken down into two components: r_1 and r_2 (See Figure (10)).

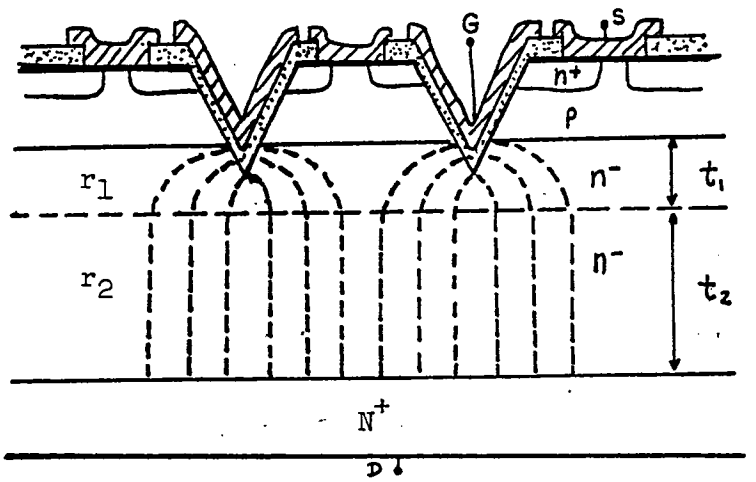


Figure (10) Two Components of r_{drift}

r_2 can be estimated by the well-known resistance equation:

$$r_2 = \rho \frac{t_2}{A} \qquad (4)$$

where ρ = n- epi resistivity
t_2 = epi thickness
A = active epi cross-section area

The exact calculation of r_1 is complex because of its spreading nature. However, by making some reasonable assumptions, a simple equation can be formulated to estimate r_1 (for the practical V-groove width).

The derivation of r_1 is given in Appendix A. From Appendix A, we find that r_1 is the product of epi resistivity, ρ, times a geometry factor, Σ, or

$$r_1 = \rho \times \Sigma \qquad (5)$$

Σ is a function of layout structure.

For an interdigitated structure,

$$\Sigma = \frac{1}{2(x_2-y_2)} \left[\ell n \frac{(2t_1 + y_2)}{2t_1 + x_2} - \ell n \frac{y_2}{x_2} \right] \qquad (6)$$

(t_1, x_2, y_2 are defined in page 112A)

For K-structure (See Figure (72)),

$$\Sigma = \frac{1}{4a} \left[- \ell n \frac{(a-b)}{(a+b)} \right] \qquad t_1 = b/2 \qquad (7)$$

(a and b are defined in page 109)

To see how well the equations predicted the measured values, we cut a number of single 10-mil long VMOS FETS, the difference being the V-groove width "x". Figure (11) showed the measured values of $r_{DS(on)}$

as a function of different V-groove width x. The epi resistivity was 2Ω - cm. It should be noted that $r_{DS(on)}$ saturated to a constant value, indicating that the constant potential line assumption was no longer valid for large x. For x > .4mil. The sheet resistance of the accumulation layer was significant; and the calculated values would be lower than the measured values.

Figure (12) showed the calculated and measured $r_{DS(on)}$ as a function of V_{GS}, with a constant V-groove width x. For this figure x = .2 mil. From the figure, we noted that calculated values tracked measured values fairly well.

3.2.2.3 $r_{DS(on)}$ Discussion

r_{ch} and r_{drift} have been identified as the dominant $r_{DS(on)}$ components. At low V_{GS}, r_{ch} dominates, at high V_{GS}, r_{drift} dominates.

Again, as the breakdown voltage requirement increases, higher epi resistivity and thickness are required, r_{drift} will increase and eventually become the single dominant component. Figure (13), which was based on equations (3) and (6) gave us some quantitative ideas. From Figure (13) we found that for 5Ω-cm, 15μ of epi, r_{drift} was 80% of $r_{DS(on)}$. For 20Ω-cm, 50μ epi, r_{drift} was 95% of $r_{DS(on)}$. Therefore, we concluded that the key to lower $r_{DS(on)}$ was to lower r_{drift}. Also, the key to lower r_{drift} was to make more efficient use of epi cross-sectional area in conjunction with the lowest possible epi resistivity and thickness. This was the major motivation for developing silicon-gate VMOS.

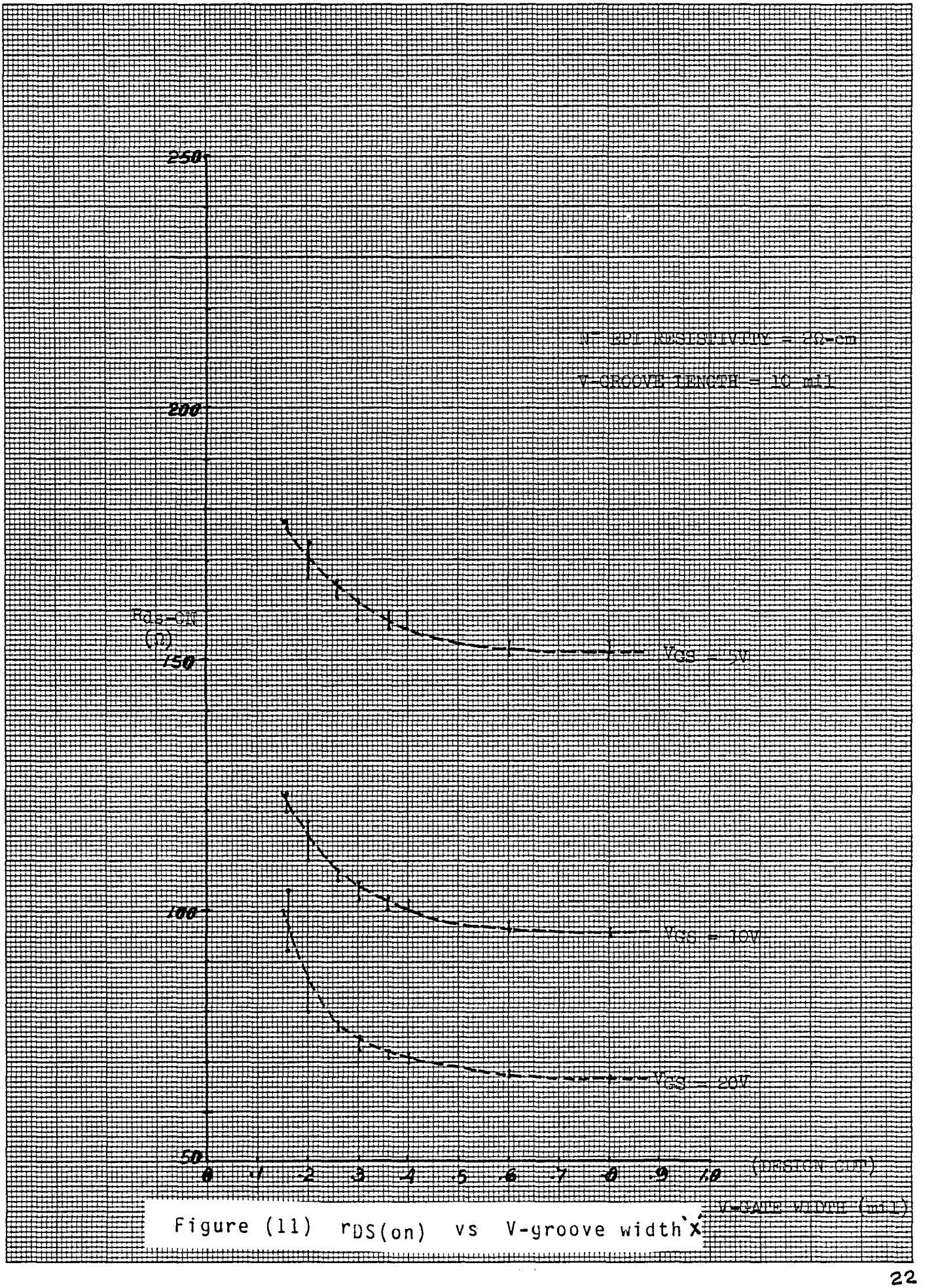


Figure (11) $r_{DS(on)}$ vs V-groove width

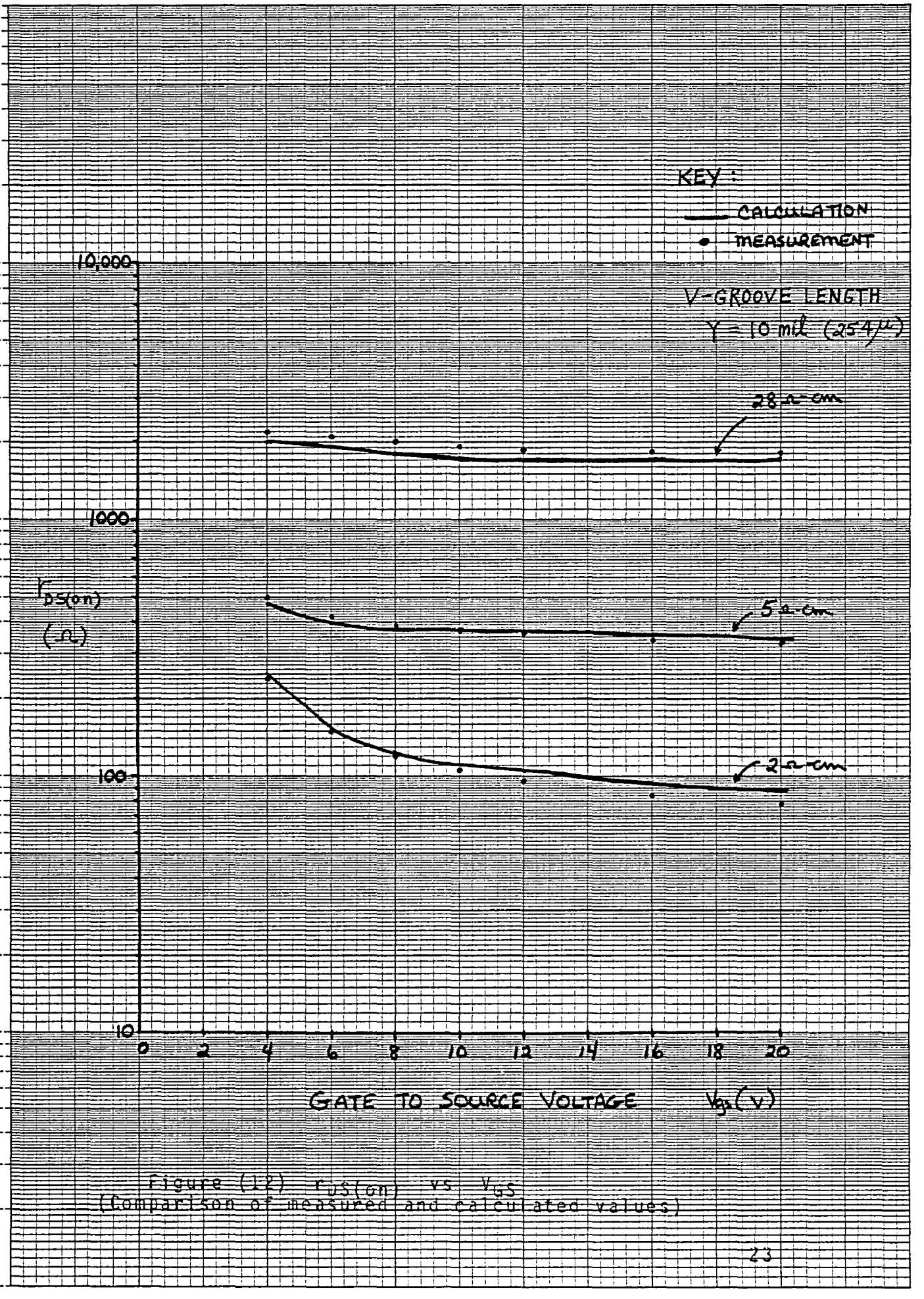


Figure (12) $r_{DS(on)}$ vs V_{GS}
(Comparison of measured and calculated values)

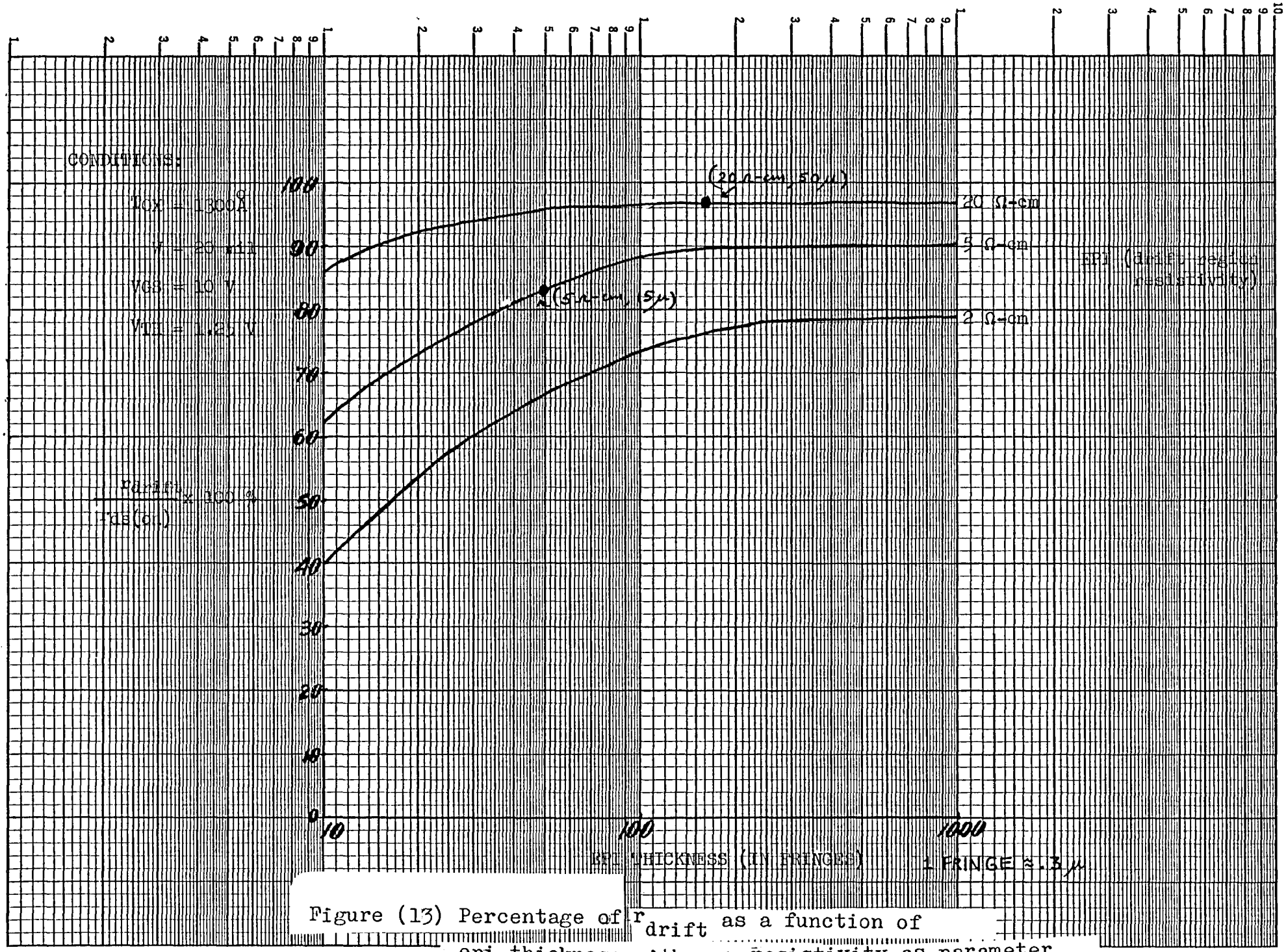


Figure (13) Percentage of r_{drift} as a function of epi thickness with epi resistivity as parameter

3.2.3 g_m Calculation

The saturation region of VMOS can best be described by the $I_{DS(on)}$ vs V_{GS} transfer curve, with V_{DS} set at the saturation drain voltage. (See Figure 14) From the figure, it is observed that the curve can be broken up into three regions:

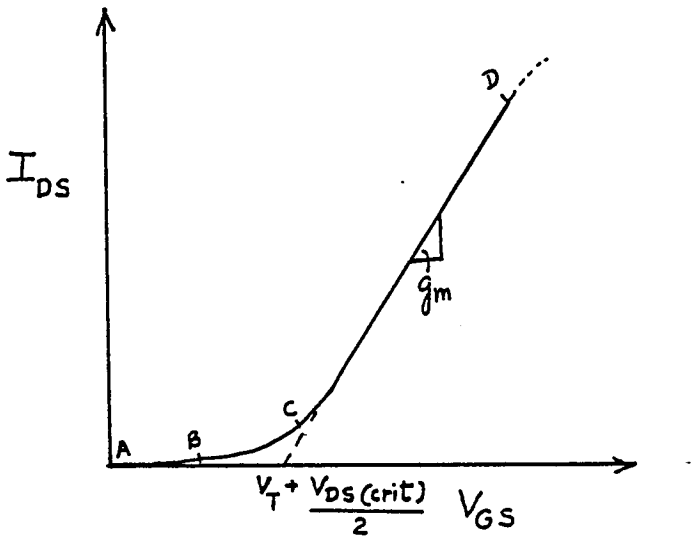


Figure (14) Transfer Curve of VMOS Transistor

A-B is the sub-threshold region;
B-C square law region; and,
C-D constant g_m region where scattering limited velocity of carriers is reached.

From the practical device design viewpoint, region C-D was the most important one. This section was primarily addressed to the derivation of a simple equation and physical interpretation of parameters pertaining to this region.

As a direct consequence of short-channel length (approximately 2 μ) the scattering-limited velocity of the channel carriers was reached at some moderate drain voltage (which was designated as $V_{DS(crit)}$). It follows that $I_{D(sat)}$ was linearly proportional to V_{GS}. In other words, g_m was constant. Again, because the depletion layer extending primarily into the drift region, we could assume constant Q_B and therefore $I_{D(sat)}$ could be derived from the simplified version of the conventional MOS equation. (See Appendix B for the derivation). The equation is given by:

$$I_{D(sat)} = WC_o\mathcal{V}'_{sat} \times \left(V_{GS} - \left(V_T + \frac{V_{DS(crit)}}{2}\right)\right) \quad (8)$$

$$\text{and } g_m = WC_o\mathcal{V}'_{sat} \quad (8a)$$

where W = channel width

C_o = gate oxide capacitance per unit-area

$\mathcal{V}'_{sat}$ = effective scattering limited velocity of carriers.

$V_{DS(crit)}$ = drain voltage at which scattering limited velocity of carriers is reached.

g_m = transconductance $\left(\frac{\Delta I_D}{\Delta V_{GS}}\right)$

Equation (8) predicted that the transfer curve of $I_{D(sat)}$ vs V_{GS} was a straight line with a slope equal to g_m; the line intercepted the V_{GS} axis at $(V_T + V_{DS(crit)}/2)$. See figure (14).

Data on the transfer characteristics (I_{DS} vs V_{GS}) in the saturation region were obtained from a number of test cells of different channel widths. Figure (15) presents the data obtained from such measurements.

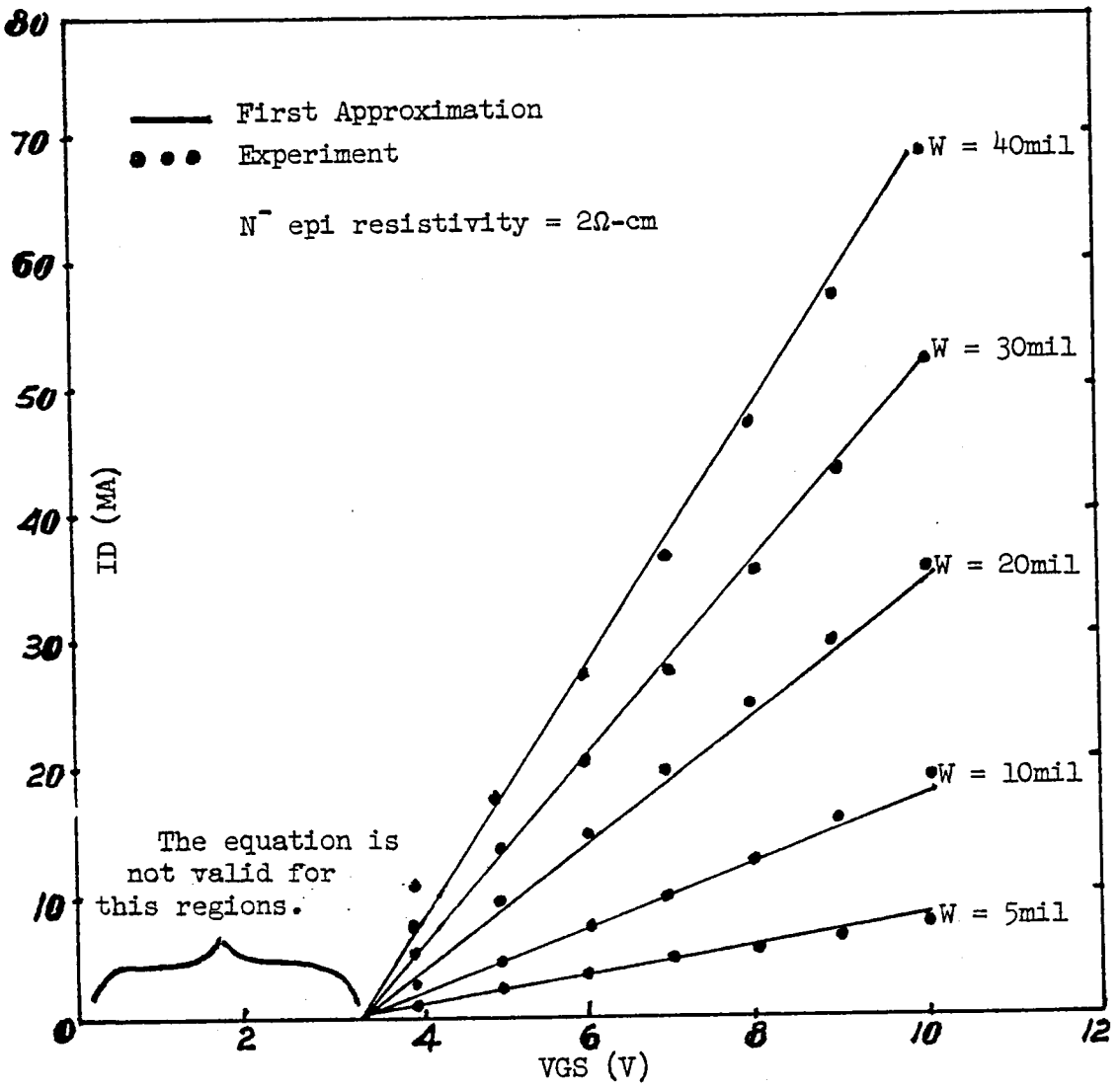


Figure (15) Transfer Characteristics of VNTB: various channel widths

From the Figure we concluded:

$$\mathcal{V}'_{sat} = 4 \times 10^6 cm/sec$$

$$V_{DS(crit)} = 4 - 6V$$

But, $$V_{DS(crit)} = \ell \times E_{crit}$$

$$E_{crit} = 2 - 3 \times 10^4 \ V/cm$$

These values are well within the range found in the literature. Note that equation (8) was valid only when the carriers were moving with their scattered limited velocity. In this region, channel length (ℓ) was absent from the equation. g_m was determined by C_o and W only since $\mathcal{V}'_{sat}$ was a constant value.

So far, we have had good definition of $r_{DS(on)}$, g_m and $I_{DS(sat)}$. From the practical view point, this was all we needed to know in order to predict the I-V characteristic of VMOS power FETs.

(From the data, it is observed that $V_{DS(sat)}$ follows roughly the locus of $(V_{GS}-V_T)$).

3.2.4 Complete I-V Characteristics

From a modeling point of view, the Siliconix VMOS FET is composed of two components, viz., an N-ch (or P-ch) MOSFET in series with a fixed resistor (mainly r_{drift}). The schematics of this model is shown in Figure (16).

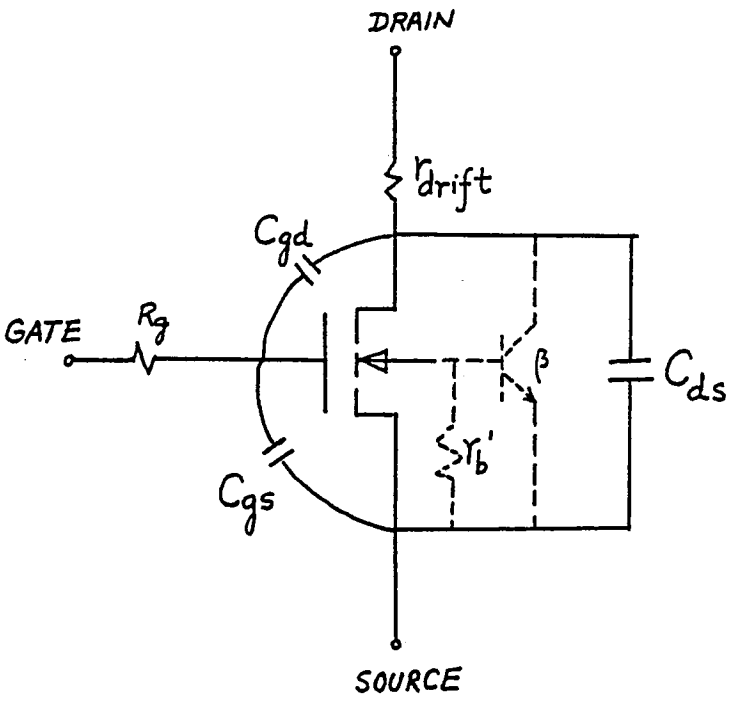


Figure (16) Schematic Representation of the VMOS Transistor

Putting the results of the previous section together, the measured and calculated I-V curves for a W=20 mil single VMOS Fet is shown in Figure (17).

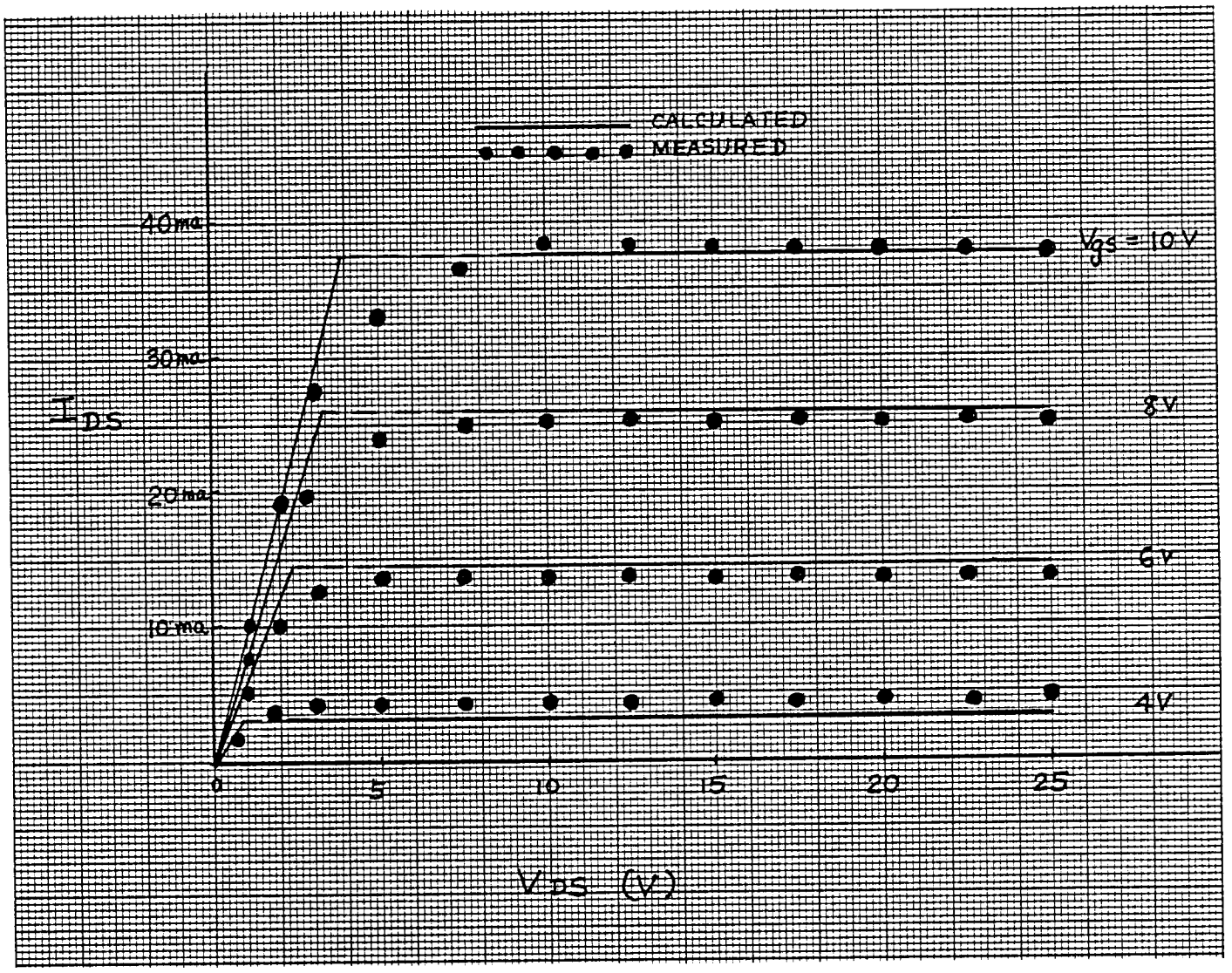


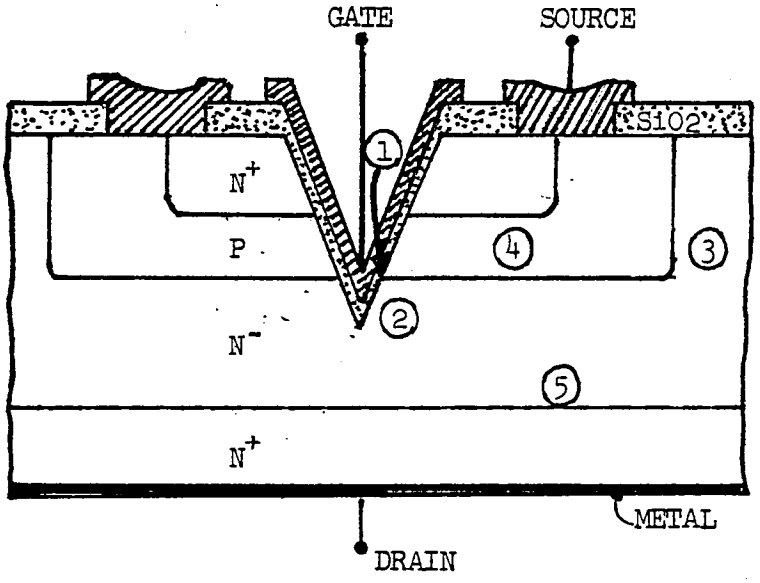
Figure (17) Drain Characteristics of VMOS Transistors

3.2.5 Breakdown in VMOS Structures

Factors affecting the breakdown voltage of VMOS are considered to adequately define the Safe Operating Area (SOA) of the device.

3.2.5.1 Breakdown Mechanisms

VMOS has both the surface structure of a MOS device and the bulk structure of a bipolar device. Thus, all breakdown mechanisms of both types of devices exist within the VMOS structure. See Figure (18)



1. Dielectric Breakdown
2. Breakdown Underneath V-groove
3. Avalanche Breakdown
4. Punch-through Breakdown
5. Reach-through Breakdown

Figure (18) Breakdown Mechanism of VMOS Structure

3.2.5.1.1 Dielectric Breakdown (① in Figure 18)

High voltages could develop between the drift region which is considered part of the drain, and the gate. However, when this happens, the silicon underneath the V-groove is deeply depleted. In this case, a situation exists where the full voltage drop between drain and gate is seen by two capacitors in series, as shown in Figure (19).

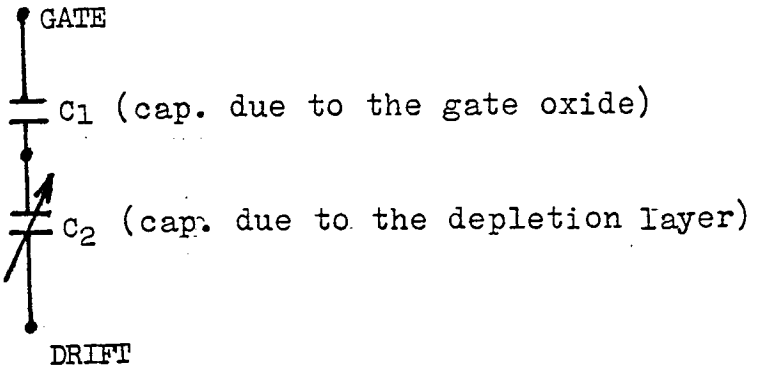


Figure (19) Drain MOS Capacitance
C_1 and C_2 Series

By placing C_1 and C_2 in series, this has greatly relieved C_1 from having to shoulder the full voltage drop by itself. Consequently, by having reasonable oxide thickness, no dielectric breakdown problem is expected.

3.2.5.1.2 Breakdown Underneath V-groove (② in Figure 18)

Normal V-grooves have sharp edges. Their effect on an equipotential plot is crowding of potential lines in these regions. See Figure (20) In other words, a high electric field can develop in this region thus initializing breakdown.

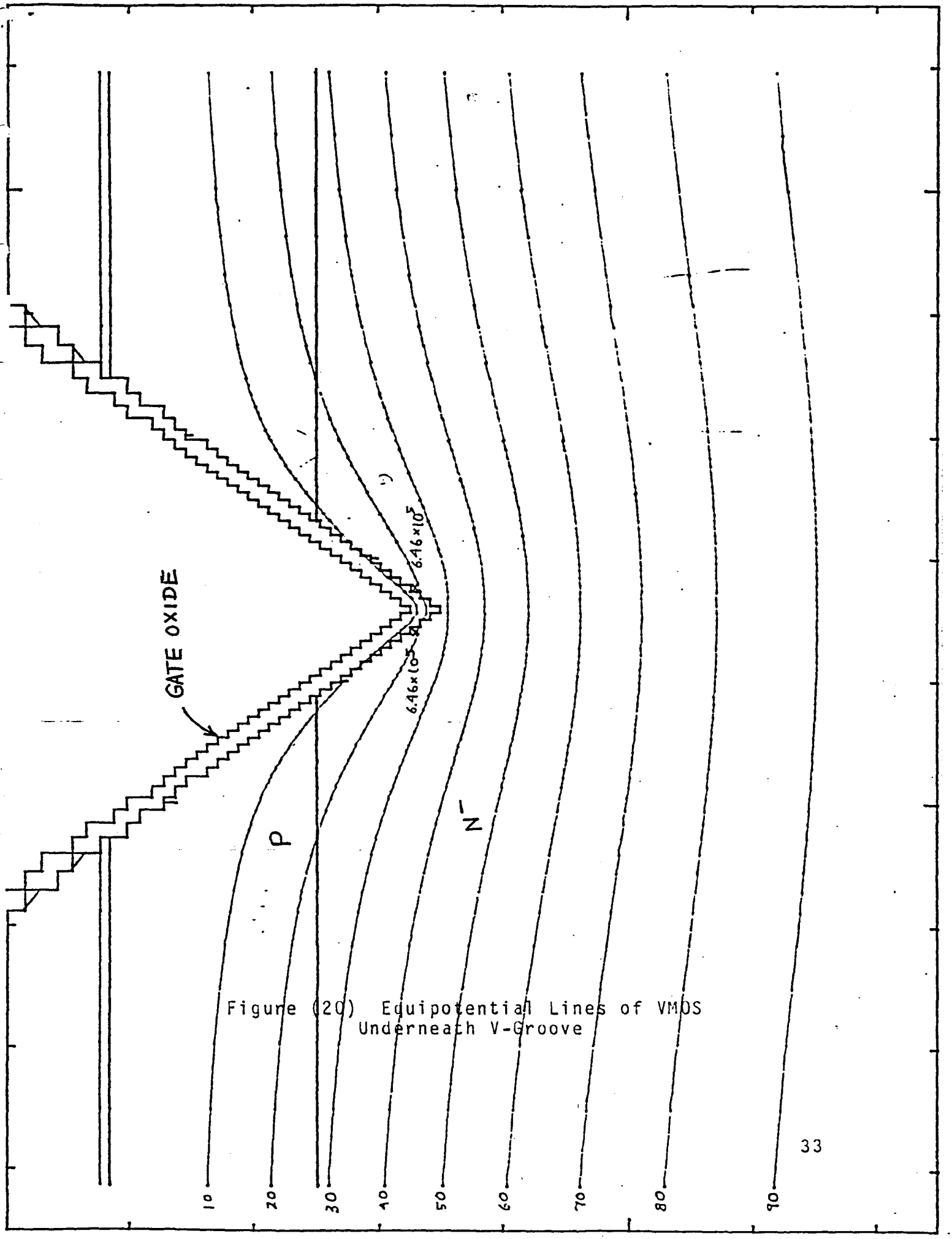


Figure (20) Equipotential Lines of VMOS Underneath V-Groove

3.2.5.1.3 Avalanche Breakdown (③ in Figure 18)

Avalanche breakdown can occur at the PN junctions. Therefore, to achieve low $r_{DS(on)}$, it was very important to get the PN junction breakdown to be as close to the ideal PN junction breakdown as possible.

3.2.5.1.4 Punch-through Breakdown (④ in Figure 18)

Because of the drift region which is one or two orders of magnitude more in carrier concentration than that of the body or channel, the VMOS device could withstand as high as 400V of punch-through breakdown with just 2μ of 'base width'. This mode was not considered a limiting factor.

3.2.5.1.5 Reach-through Breakdown (⑤ in Figure 18)

This breakdown depends on epi resistivity and thickness and is not a limiting factor.

3.2.5.2 Discussion of Breakdown

The limiting factors of VMOS structure are either breakdown underneath the V-groove or breakdown at the PN junction. In addition, since the VMOS structure includes a parasitic npn bipolar transistor and a n-(epi) α n+(substrate) interface, the device can break into either switch-back or secondary breakdown when care is not exercised in device design. With proper device layout and process, however, the switch-back phenomenon that was present in the earlier generation of VMOS can be completely eliminated . The device can display a true MOS drain characteristic. The SOA of the device can extend to the full voltage and current ratings simultaneously.

3.2.6 Capacitances in VMOS Structure

Switching speed depends primarily on both the conductance and the capacitance present on the chip.

As a part of the RC time-constant, two resistance components are important. The first is the resistance in the input circuit or gate series resistance, r_g (if polysilicon gate was used). The other is the resistance in the output or $r_{DS(on)}$. We discussed $r_{DS(on)}$ at length in Paragraph 3.2.2. The r_g depends to a great extent on the layout and the sheet resistance of the polysilicon gate material.

In addition to the two resistance components mentioned above, the r_b' of the parasitic npn bipolar also affects switching speed through its influence on the body charge underneath the active gate region.

We are interested in the minimization of capacitances from two viewpoints:

1) ease of drive; and
2) faster switching speed.

For VMOS structures, there is one junction capacitance and 6 MOS capacitance components. They are identified with the aid of Figure (22).

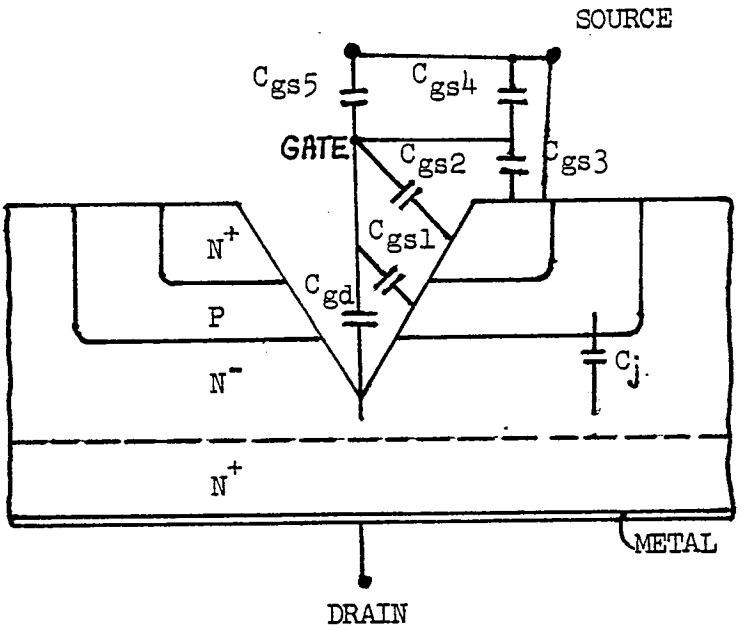


Figure (22) Capacitance Components of VMOS Structure

1) C_j Junction capacitance between body and drift region;
2) C_{GS1} MOS Capacitance beween gate and channel (channel shorted to source);
3) C_{GS2} MOS capacitance between gate and source (Gate oxide as dielectric);
4) C_{GS3} MOS capacitance between gate and source (source oxide as dielectric);
5) C_{GS4} MOS capacitance between gate and source (silox between poly and metal as dielectric); and,
6) C_{GS5} MOS capacitance between gate and source (gate bonding pad). and,
7) C_{GD} MOS capacitance between gate and drain. This is the so called Miller feedback cap. It is composed of two capacitors in series as discussed in paragraph 3.2.5.1.1.

As we increased W by increasing the packing density, C_{GS1} increased. There was very little that could be done about this parameter. The challenge was to keep the gm/C_{in} ratio as low as possible.

In a typical data sheet, the capacitances of a device are characterized into:

C_{iss}, C_{oss} and C_{rss} measured at F = 1MHz

C_{iss} = common source input capacitance.
This is the capacitance measured from the input (gate) to the source with the drain biased with respect to the source.

C_{oss} = common source output capacitance.
This is the capacitance measured from the output (drain) to the source with the gate shorted to the source.

C_{rss} = common source reverse capacitance.
This is the capacitance measured from the drain to the gate.

(The dynamic input characteristic of the VMOS power switch is treated in detail in Ref. 8.)

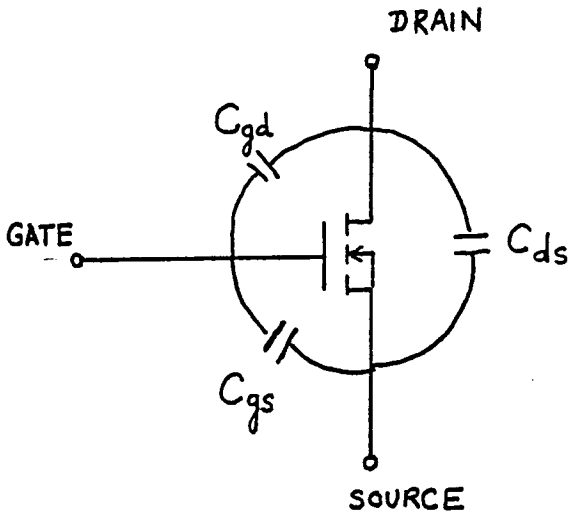


Figure (23) Terminal Capacitance of a MOSFET

These capacitances are related to the terminal capacitance of a MOSFET as follows:

$$C_{iss} = C_{gs} + C_{gd}$$

$$C_{rss} = C_{gd}$$

$$C_{oss} = C_{gd} + C_{ds}$$

(all at V_{DS} = 25V and F = 1mHz.)

The test circuits are shown in Figure (24)

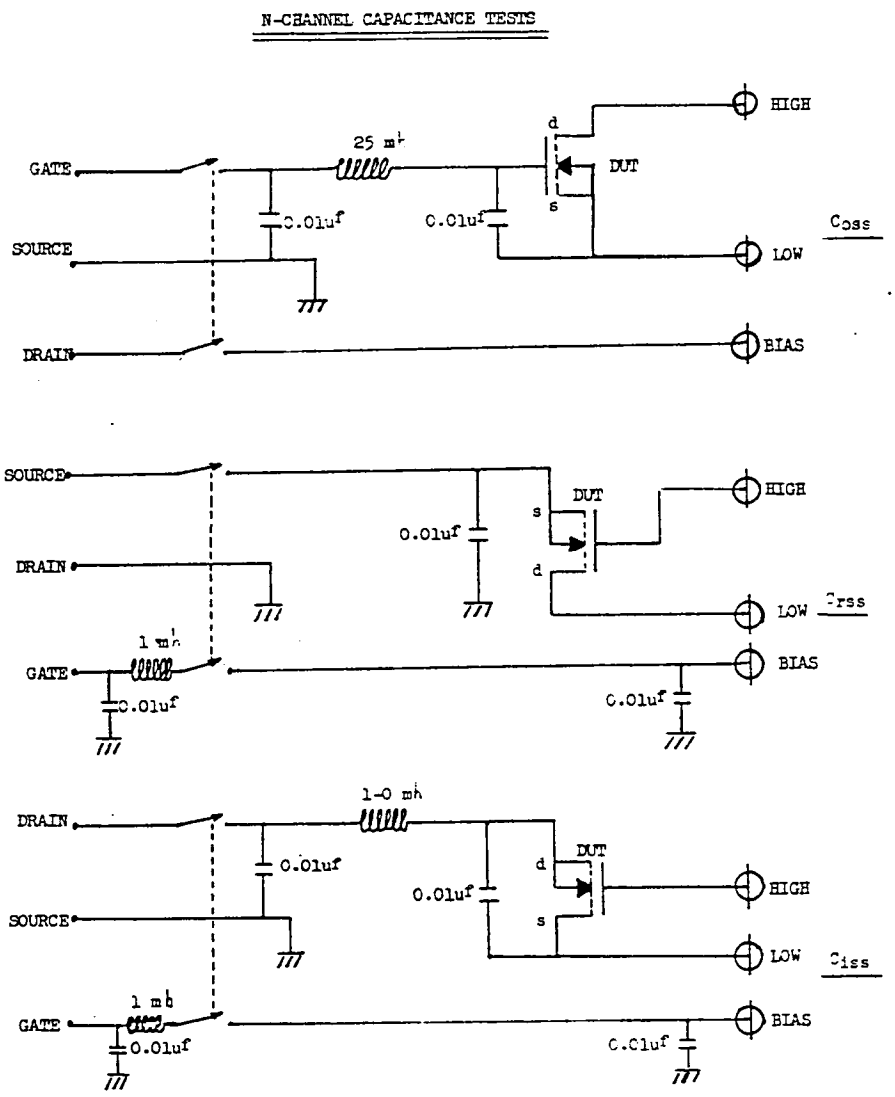


Figure (24) Test Circuits to Determine Capacitances

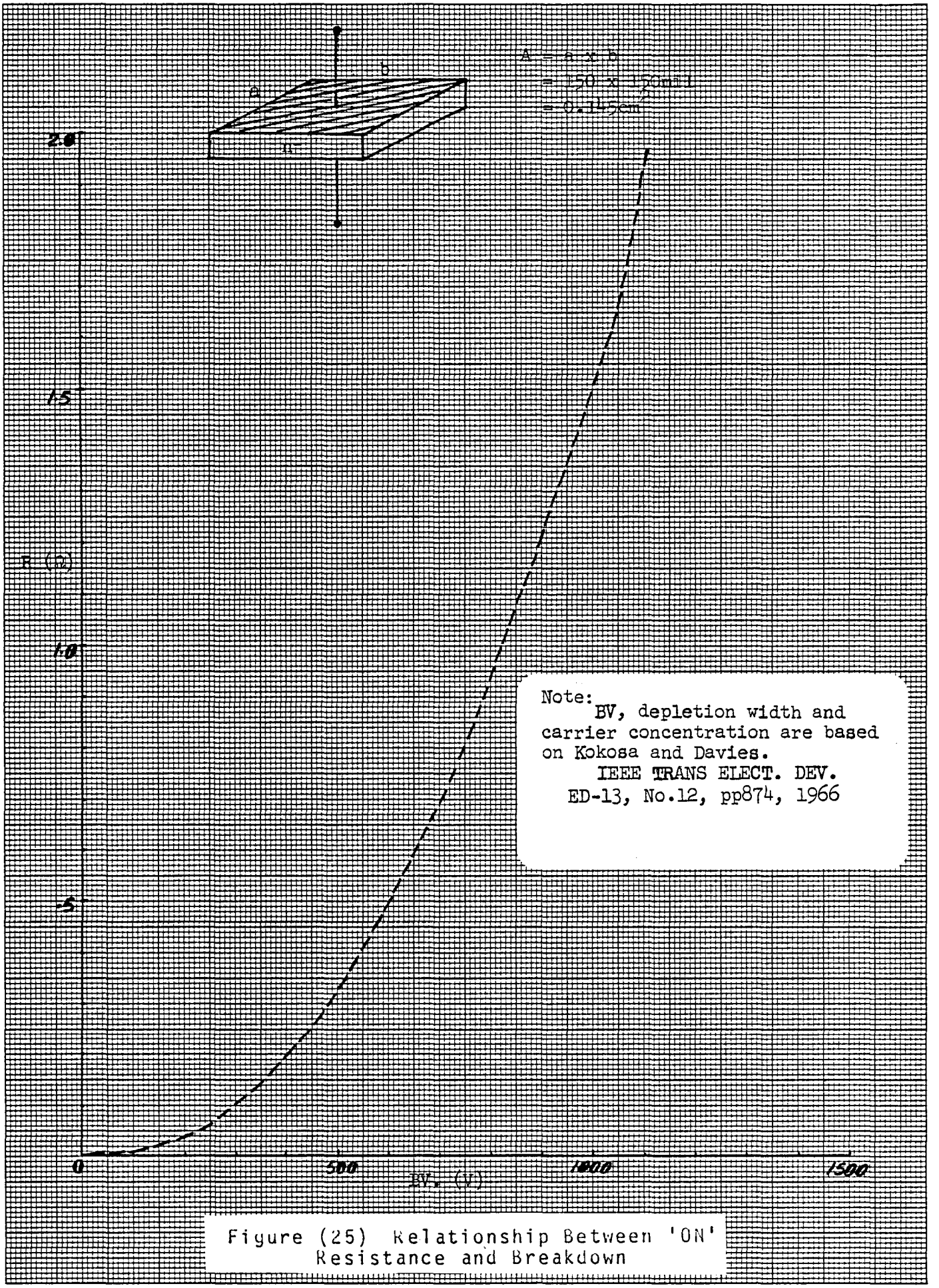
3.2.7 Optimization of Trade-offs

There were two major trade-offs. One was the trade-off between 'ON' resistance and breakdown voltage. To get low $r_{DS(on)}$, we needed low epi resistivity and thin epi thickness. However, high voltage required high epi resistivity and thick epi thickness. Figure (25) shows the relationship between 'ON' resistance and BV. From the figure we find that:

$$r_{DS(on)} \propto BV^{2.2}$$

So it was vitally important that for the specified breakdown, we wanted to get it with the lowest possible epi resistance and thickness.

The other trade-off was between 'ON' resistance and capacitance which affects switching speed. One way to lower $r_{DS(on)}$, was to increase the channel width, W. This meant larger overlapping areas between gate and source plus channel. This would increase C_{iss}. The other way to lower $r_{DS(on)}$ was to increase the overlapping area between the grooves and the N- epi drift region (x_2 in figure 71). This would increase C_{rss}, which, in turn, would slow down the device's switching characteristics.



Note:
BV, depletion width and carrier concentration are based on Kokosa and Davies.
IEEE TRANS ELECT. DEV.
ED-13, No.12, pp874, 1966

Figure (25) Relationship Between 'ON' Resistance and Breakdown

3.3 Why Polysilicon Gate VMOS Process

The vertical MOS process development is still in its early life history. By combination and permutation, there are at least more than a dozen ways of producing VMOS. To select the proper process, various criteria were evaluated.

In the burgeoning power switching application, we need low $r_{DS(on)}$, high current, high voltage and fast switching speed. The metal gate VMOS presently manufactured is capable of high voltage (400V) and fast switching speed (approximately 50ns). Resistance and current handling capacity leave room for improvement. The reason is that both 'ON' resistance and current take up silicon real estate. It is not uncommon for high current VMOS such as 20A - 30A, to find that 50% of the chip area is taken up by the source metal alone, and all of this area is non-active. It is imperative that we put gate and source electrodes on different planes so that they can cross each other. One method of accomplishing this is the polysilicon gate VMOS process. Figure (26) illustrates this three-plane conduction concept.

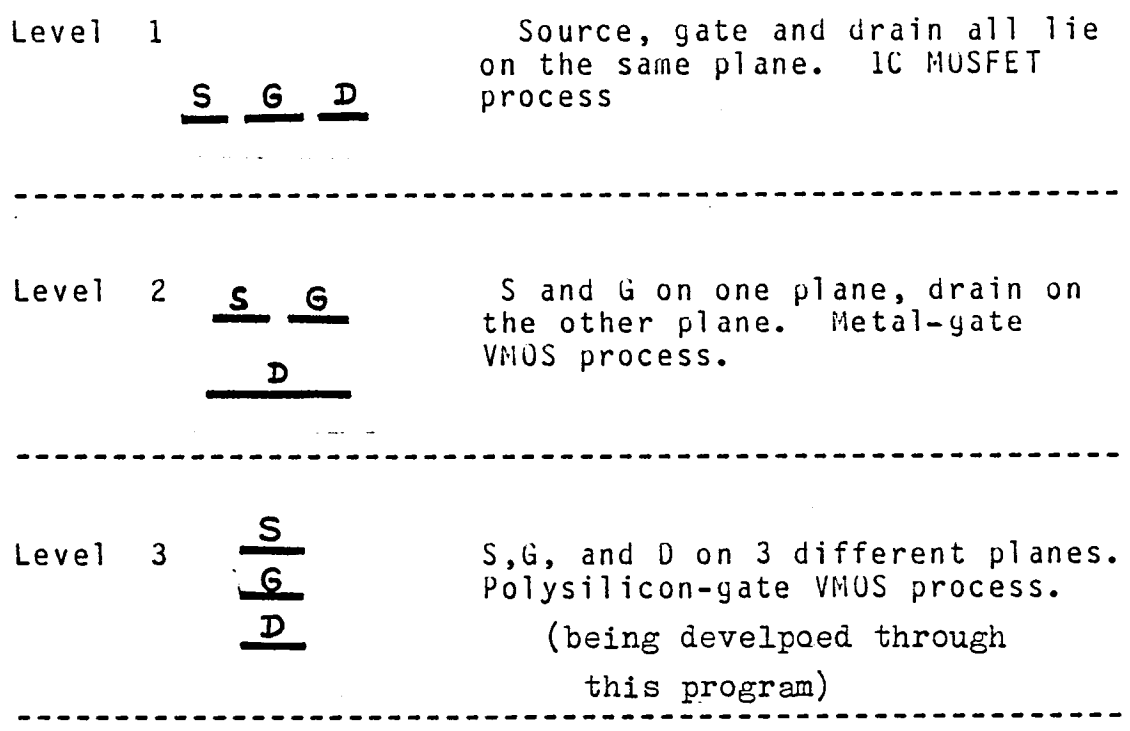
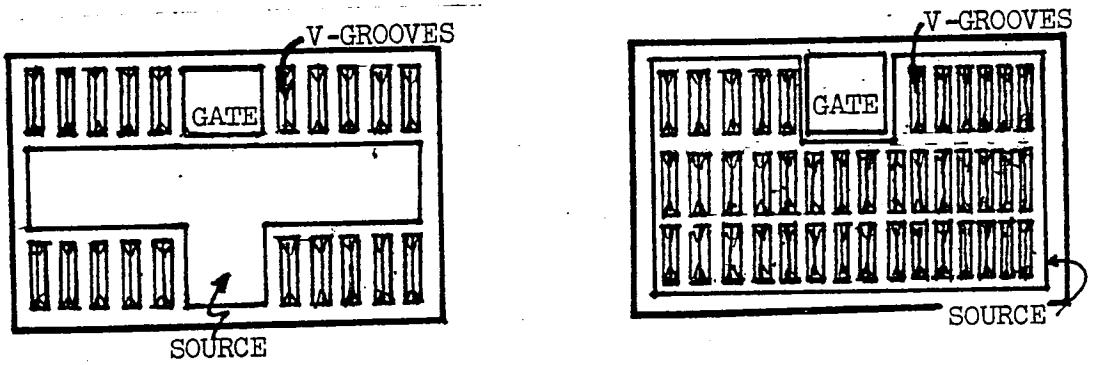


Figure (26) Evolution of
Three-Plane Conduction

One way to implement this three-plane conduction concept is shown in Figure (27), which illustrates an important point. From Figure (27 a), we see that using a metal gate we are getting 30% to 40% active area out of the total chip; (and that is a trade-off with total current), the polysilicon approach in Figure (27 b) can give us over 80% of active area.



(A) Metal-gate (B) Silicon-gate

Figure (27) Illustration of Layout Difference Between Metal-Gate and Silicon-Gate VMOS

This means that for a given chip size we can approach the theoretical limit in utilizing the drift epi cross-sectional area. In other words, we are maximizing the area factor of the well-known equation for resistance:

$$R = (\rho \times \ell)\ (1/A) \qquad (9)$$

From Figure (27 b), we also see that a whole plate of source metal is placed on top of the chip. This means that current is no longer limited by the current density consideration of the source metal. In fact, the metal on the chip is now capable of carrying whatever current the device can deliver without running into high current density or electromigration problems. (The heat sinking effect of whole source metal is also a welcomed feature.) In other words, the new process is approaching the theoretical limit in current carrying capability.

What about breakdown voltage? From equation (9), we note that resistance was a volume concept. Maximizing the area factor by pushing epi cross-sectional area was only half of the story. We needed to minimize the (ρ x ℓ) factor also. The issue here was how could we use the lowest epi resistivity and thinnest epi thickness to support the specified breakdown voltage. In other words, how to get a breakdown that was approaching the ideal pn junction breakdown.

Many techniques exist today, but in Section 4.1.2 we have developed a novel V-groove termination technique that gave 200V on 5Ω -cm epi, thus approaching 80% of ideal junction breakdown.

What about switching speed? Generally, we have to accept the fact that silicon- gate VMOS is slower than that of metal-gate VMOS. However, by optimizing both the process and the layout, we could push switching speed very competitive with that of metal-gate. In Section 5.2, we are going to find that large area silicon-gate VMOS can switch in less than 100ns.

Why polysilicon-gate VMOS process? The answer is simple: if the application calls for low $r_{DS(on)}$, high current, high voltage and fast switching speed, then from the analysis above, we conclude that the three-level polysilicon-gate VMOS is to be preferred.

4.0 POLYSILICON-GATE VMOS PROCESS DEVELOPMENT

A comprehensive test chip called VNTK was designed as a vehicle for layout and process development. The test chip was composed of six blocks. Each block was devoted to evaluate some specific parameters as described below:

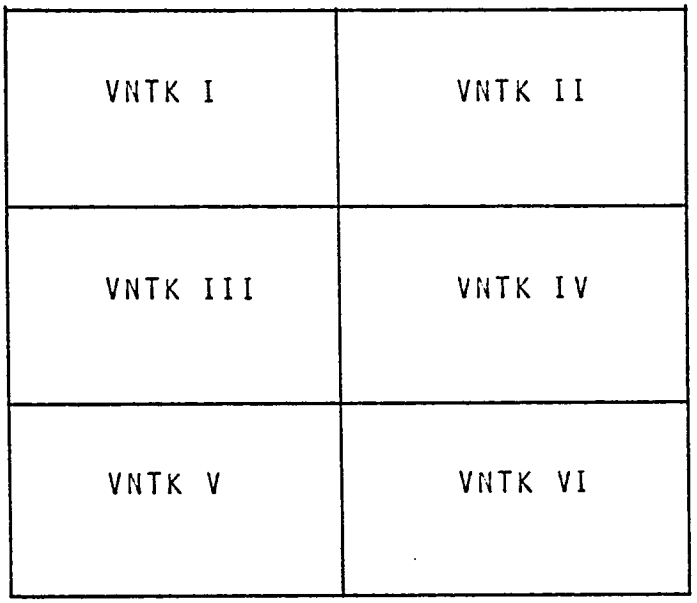


Figure (28) Block Designation of VNTK Test Chip

VNTK I — One silicon-gate VMOS FET prototype about one-twentieth of the experimental device. The end objective of this development phase was to make this transistor work and achieve 180-200V breakdown with $r_{DS(on)}$ between 2Ω and 3Ω.

VNTK II One metal-gate VMOS FET was intended as back-up (we found this back-up was not necessary).

VNTK III Test structures to study breakdown voltages.

VNTK IV Test structures to develop polysilicon technology and to provide other processing information.

In addition to the above four blocks, two more blocks were added as follows:

VNTK V To study stability of device if needed.

VNTK VI To optimize breakdown of V-groove termination with source field plate (SFP) and recessed charge control (RCC) ring.

Figure (30) is the composite of the VNTK test chip.

When the VNTK mask set was available the development activities were broken down to the following three tasks.

Task 1 Study and optimize pn diode breakdown of different V-groove termination schemes. VNTK III and VI were used for this purpose.

Task 2 Concurrent with Task 1, develop basic polysilicon technology. VNTK IV was used for this purpose.

Task 3 After Task 1 and Task 2 had been completed, develop the polysilicon-gate VMOS FET process. VNTK I was used for this purpose.

Figure (29) summarizes these activities.

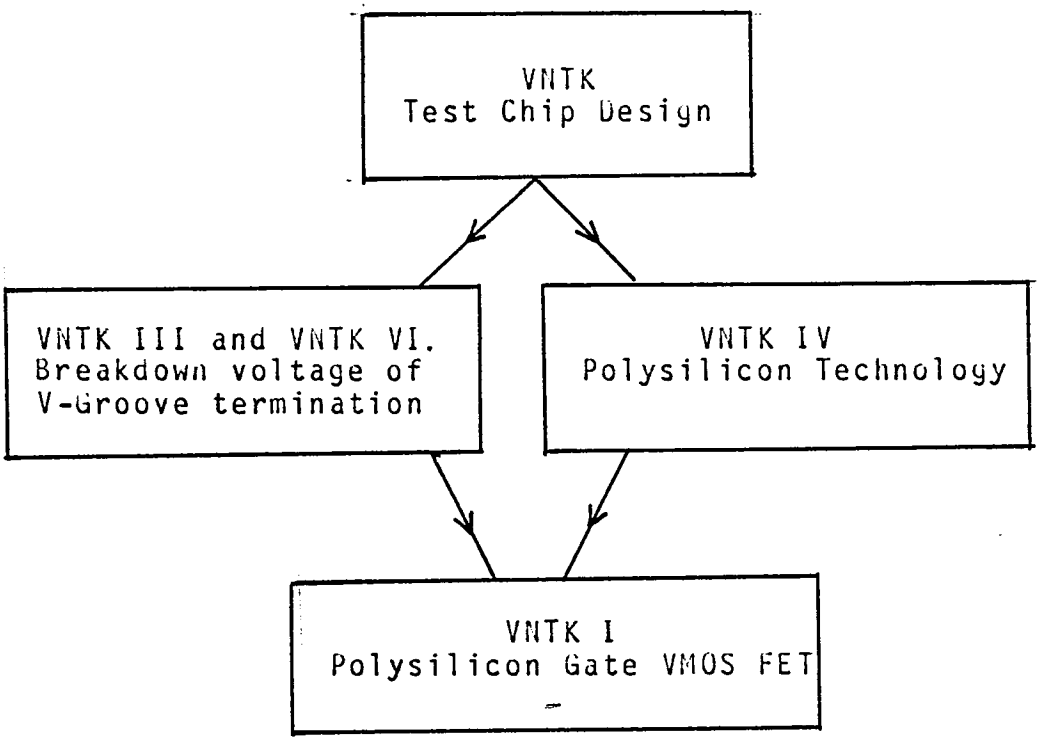


Figure (29) Flow Chart of
Polysilicon-Gate VMOS Process Development

These activities and their results are elaborated in the following three sections:

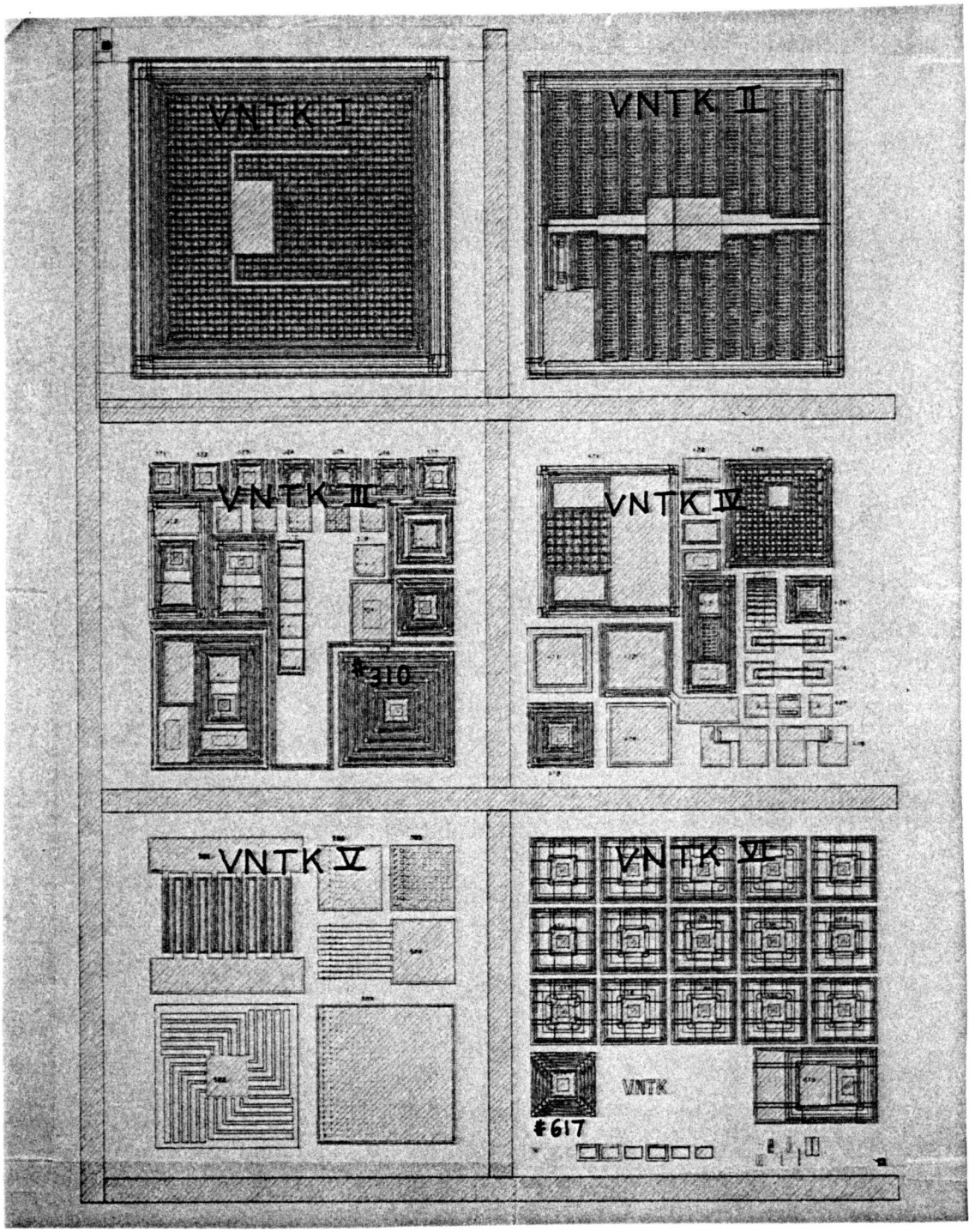


Figure (30) Composite of VNTK

4.1 Breakdown Study of V-Groove Termination

For VMOS, the basic question about breakdown was how to achieve the specified breakdown with the lowest epi resistivity and thinnest epi. The major trade-off was 'ON' resistance per unit area. This was in sharp contrast with the bipolar power transistor where the major issue is achieving specific breakdown with lowest epi resistivity. Epi thickness was of secondary importance because of a phenomena called "conductivity modulation." To assist us in the selection of a termination scheme for the poly-gate VMOS FET, we established the folowing criteria.

1. Capable of approaching ideal pn junction-breakdown voltage.

2. Not sensitive to process latitude, and easy to manufacture.

3. Economical use of Silicon area and shallow in structure.

4. Stable and reliable.

4.1.1 Selection of Termination

Based on the criteria established, three V-groove termination schemes were evaluated. All three schemes made use of the three-dimensional nature of V-grooves.

4.1.1.1 V-Groove Field Limiting Rings

Test cell no. 617 of VNTK VI was devoted to this structure. Figure (31) is the cross-section structure.

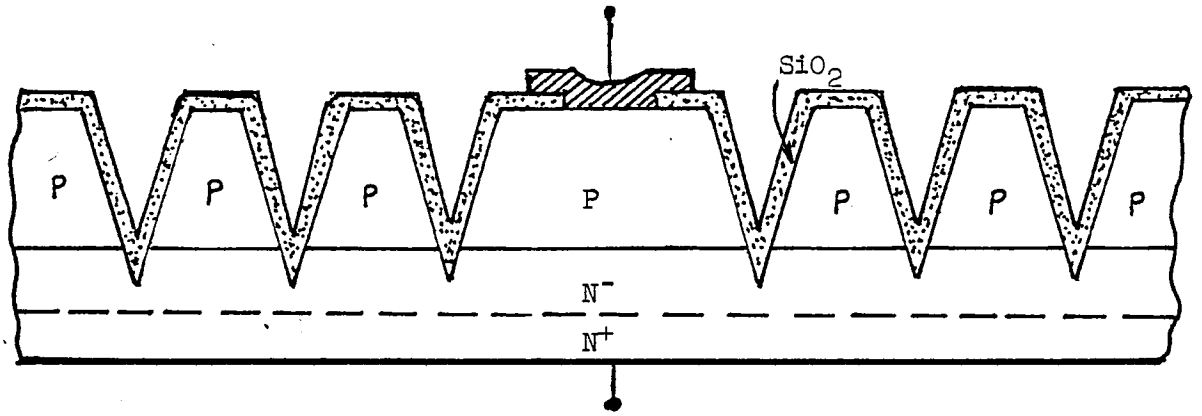


Figure (31) V-Groove Field
Limiting Ring Structure

As you can see in Figure (31), this structure operated on the same principle as a junction field limiting ring. (Reference 17) The difference was that the floating rings were created by V-grooves. Theoretically, a near-ideal pn junction breakdown voltage could be realized. However, the scheme was dismissed from a practical standpoint. One disadvantage was that it was very difficult to control the floating ring spacing because of the corner-effect of V-groove etching. We also observed some stability problem at room temperature.

4.1.1.2 V-Groove Voltages Step-down Rings

Test cell no. 310 was devoted for this struction. Figure (32) illustrates the structure.

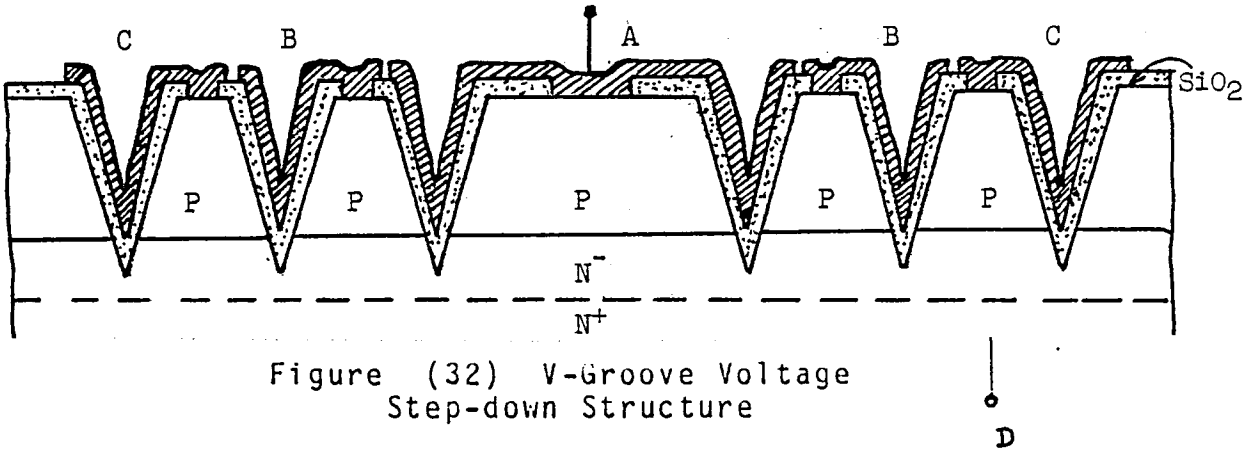


Figure (32) V-Groove Voltage Step-down Structure

This structure was based on the principle that for a MOS transistor; when gate and drain are tied together, the voltage at the source terminal was one threshold voltage lower than at drain terminal. Thus, as shown in Figure (33), if the field threshold voltage of the parasitc p-ch devices were 25V each, then, by having 3 rings, we could step down 75V. In other words, if we applied 200V at the drain the actual voltage the last ring sees was only 125V. The scheme however, was dismissed later because, to be effective in high voltage, it takes up too much area.

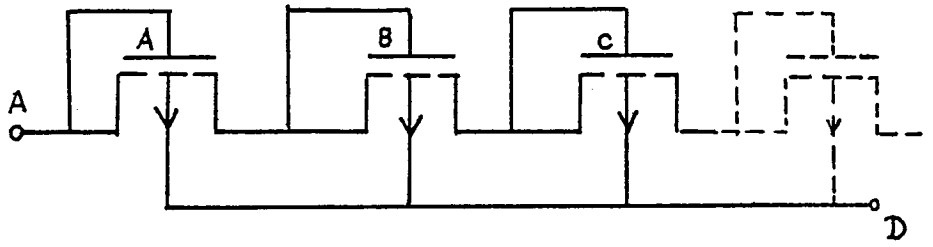


Figure (33) Schematic Representation of V-Groove Voltage Step-down Structure

4.1.1.3 V-Groove Termination With Source-Field-Plate and Recessed-Charge-Control Ring

Test cell no. 601 to 615 from VNTK VI were devoted to this structure Figure (35). Figure (34) shows the cross-section of this structure:

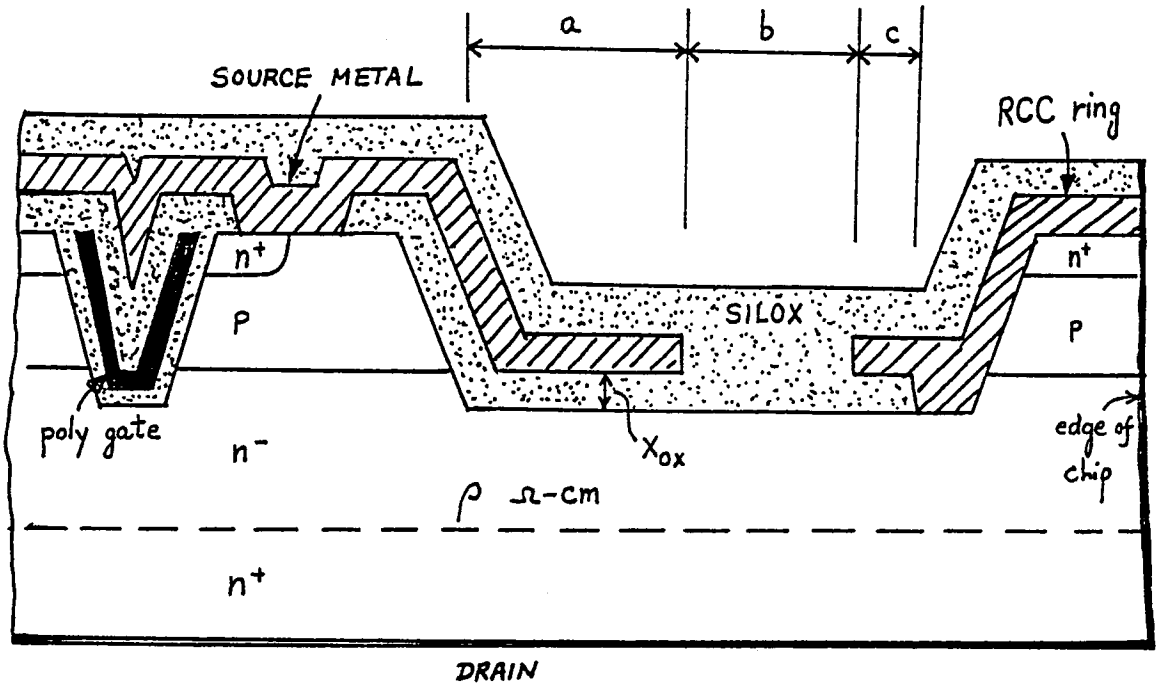


Figure (34) V-Groove Termination With Source Field-Plate and Recessed-Charge-Control Ring

We chose this termination scheme because it met all the criteria established. The scheme is elaborated in the following section.

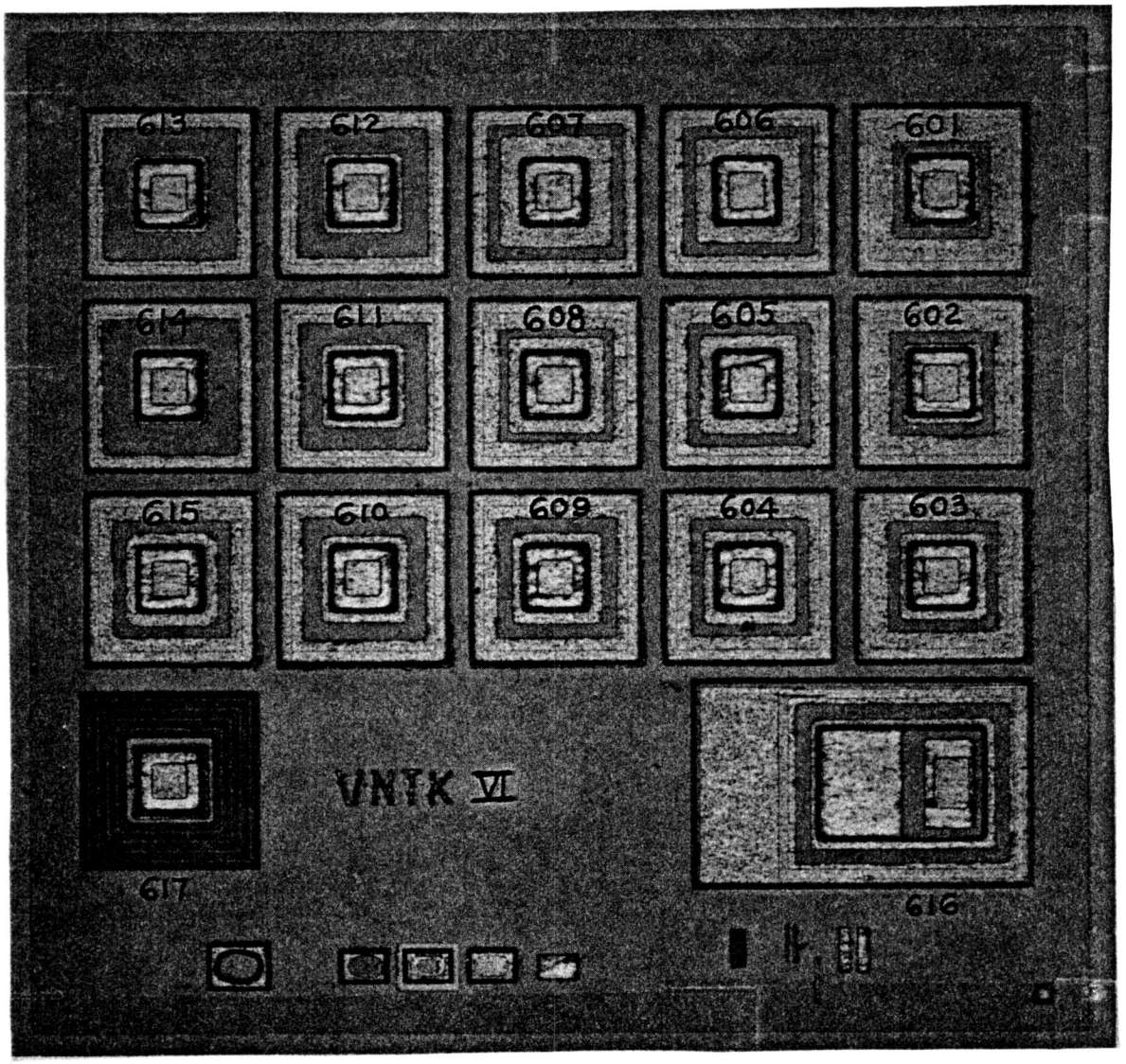


Figure (35) VNTK VI
Photomicrograph of VNTK VI

4.1.2 Experimental Results of V-Groove Termination with SFP and RCC Ring

This termination scheme was very similar to the planar-gated diodes. The basic theories have been well treated by a number of workers. (Reference 9, 10, and 11) It operated on the principle of charge neutrality. The charge on the field plate was balanced by the space-charge of the depletion layer in the semiconductor bulk. Thus, by applying voltage of proper polarity on the field plate we could control the curvature of depletion layer, hence, its breakdown voltage in the region near the surface.

For the present scheme, we tied the field plate to the source and body regions. Therefore, we called it source field plate or SFP. A V-groove termination with SFP alone does not assure us of a stable device. The problem was that the oxide had a finite conductivity. The conductivity was a strong function of the humidity and the contamination level of the oxide surface. Any charge on the field plate would extend over the surrounding oxide. The silicon surface under the surrounding oxide would be depleted. The net observable effect is charging up of drain current on the curve tracer. This was the case where the oxide surface conductivity was extremely high. For low oxide conductivity the device would function normally at room temperature. However, it would fail in leakage current after the high temperature reversed-biased stress test. To control the surface ion migration, a metal ring which is tied to the drift region was placed around the field plate. We called this ring the Recessed Charge Control or RCC ring.

Important layout parameters are:

1. Overlapping dimension of SFP over N^- drift region ("a" in Figure 34).

2. Spacing between SFP and RCC ring ("b" in Figure 34).

3. Overlapping dimension of RCC ring over N^- region (toward SFP only)

("c" in Figure 34).

4. Lateral radius of curvature of SFP.

Important processing parameters are:

1. Field oxide thickness (X_{ox})

2. Epi resistivity.

The equipotential lines of a non-planar gated diode is expected to be smoother at the pn metallugical junction than those of a planar-gated diode. Figure (36) and Figure (37) illustrate this point.

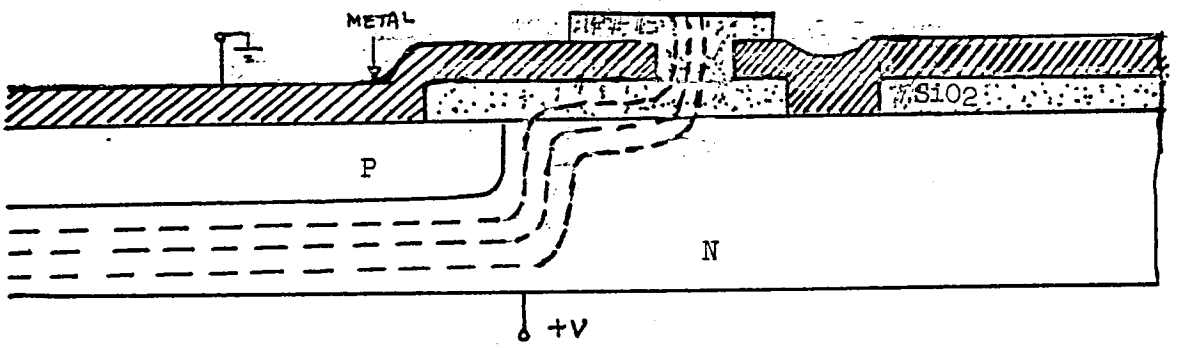


Figure (36) Equipotential Line
of Planar Gated Diode

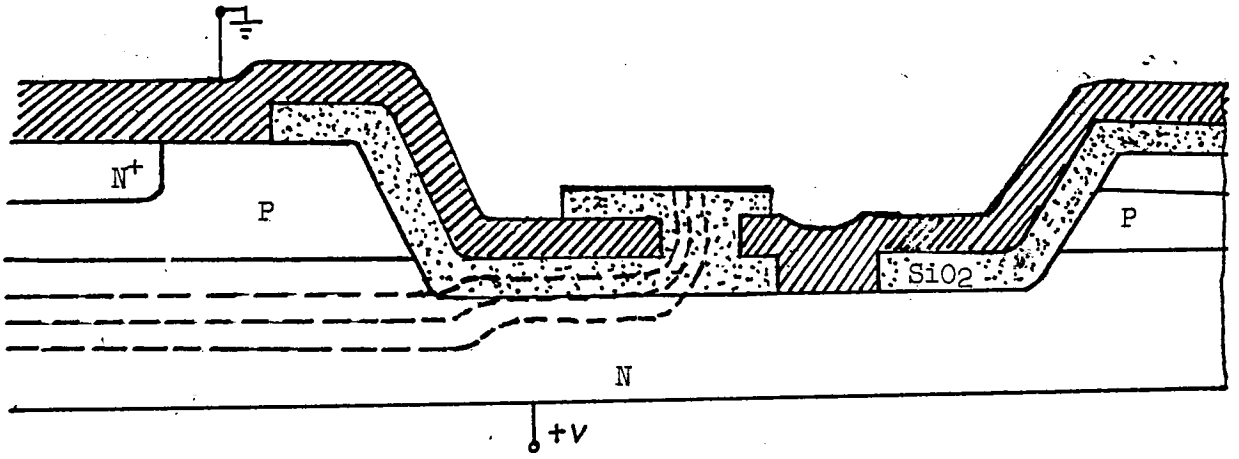


Figure (37) Equipotential Line
of Non-Planar Gated Diode

However, as in the case of the planar-gated diode, there was one optimize oxide thickness which gave the highest breakdown voltage for one epi resistivity.

4.2 Polysilicon Technology Development

Polysilicon gates for MOSFETs is a mature technology. A considerable amount of information is already available in the literature (Reference 12, 13, and 14). What we are doing here is to use the technology to implement the 'three-plane conduction' concept in VMOS power FETs.

Because of the three-dimension nature of the VMOS power FET, the classical self-aligned feature of IC silicon gate techniques cannot be readily applicable for our purpose. On the other hand, since the poly-gate is treated as another electrode, we can dope it either P or N to control the threshold voltage and sheet resistance.

Using VNTK IV, the polysilicon was evaluated in the following areas:

1. Polysilicon coverage over V-groove.
   The result is excellent. See Figure (39).

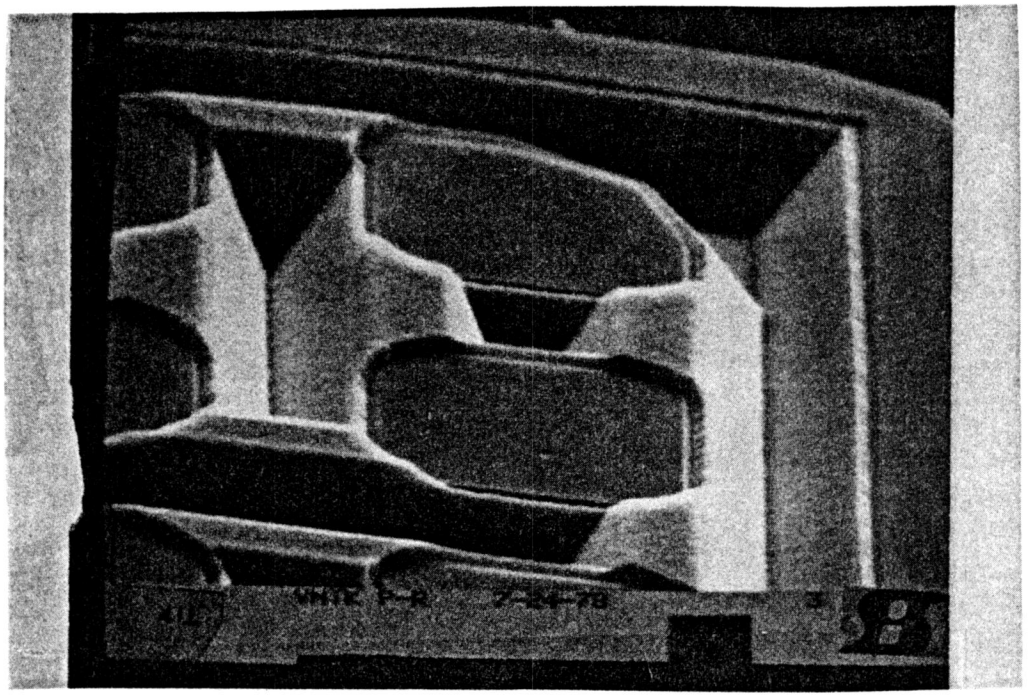


Figure (39) SEM of Polysilicon
Coverage Over K-Structure V-Grooves

2. Optimize doping 7000 Å of polysilicon film using LPCVD.

The following graph (figure 40) shows how the V/I of polysilicon goes down with predeposition time.

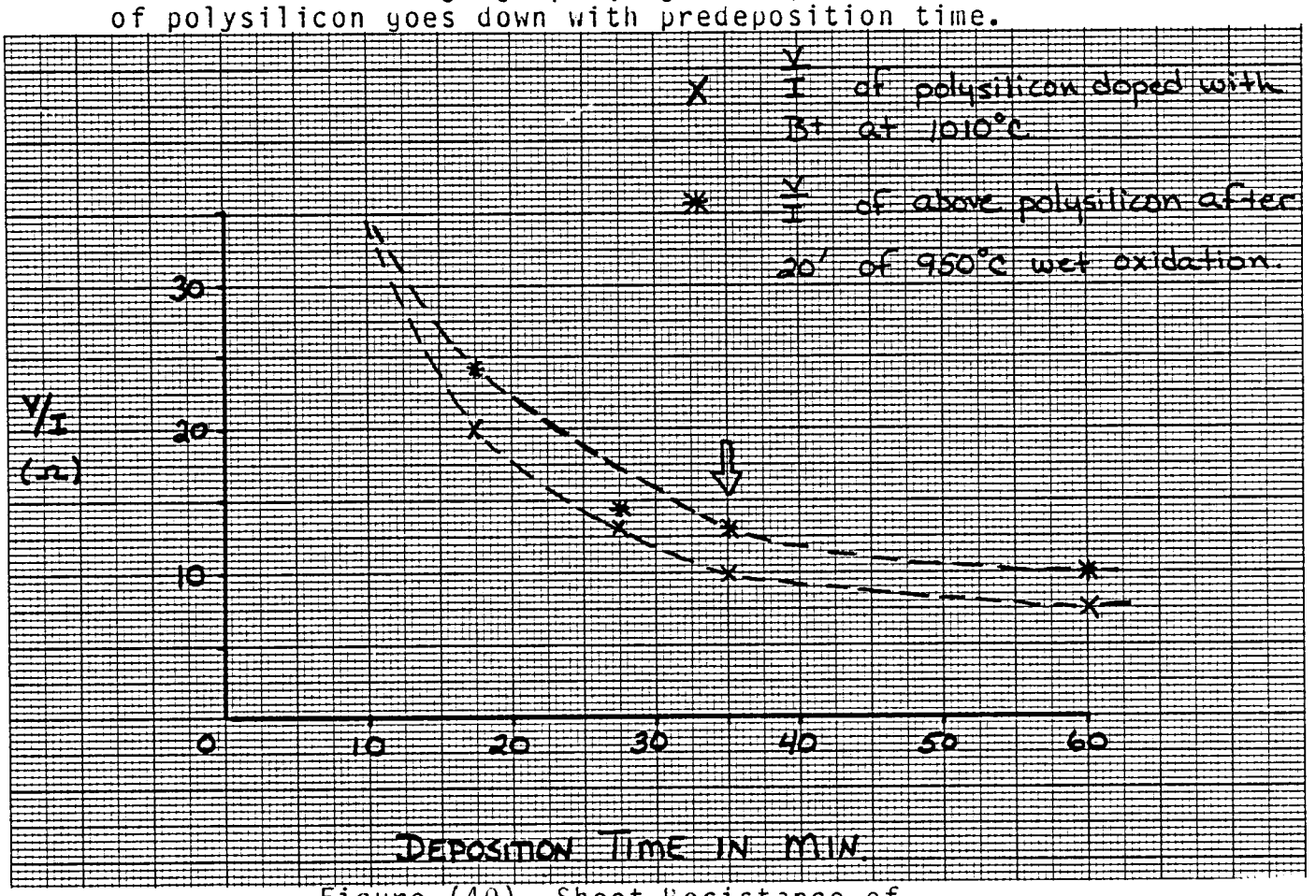


Figure (40) Sheet Resistance of Polysilicon vs Predeposition Time

Based on the data shown, 35 minutes was selected as the doping time for VMOS power FET process.

The result of a test polysilicon resistor located inside VNTK Block IV gave typically 40 - 60Ω/□ polysilicon sheet resistance.

3. Silox reflow was studied for two purposes:

   a. To get good metal step coverage over contact window; and,
   b. To avoid bumps on top of the chip. This was necessary to enable bonds to be placed directly over the active area.

Figure (41) shows that the steps over the V-groove can be considerably smoothed out by Silox reflow.

4. Miscellaneous

   a. Polysilicon film thickness control.
   b. Polysilicon grain size.
   c. Polysilicon etching.
   d. V-groove gate dielectric breakdown with poly as electrode.
   e. High temp CV for poly gate.

These were either considered or evaluated.

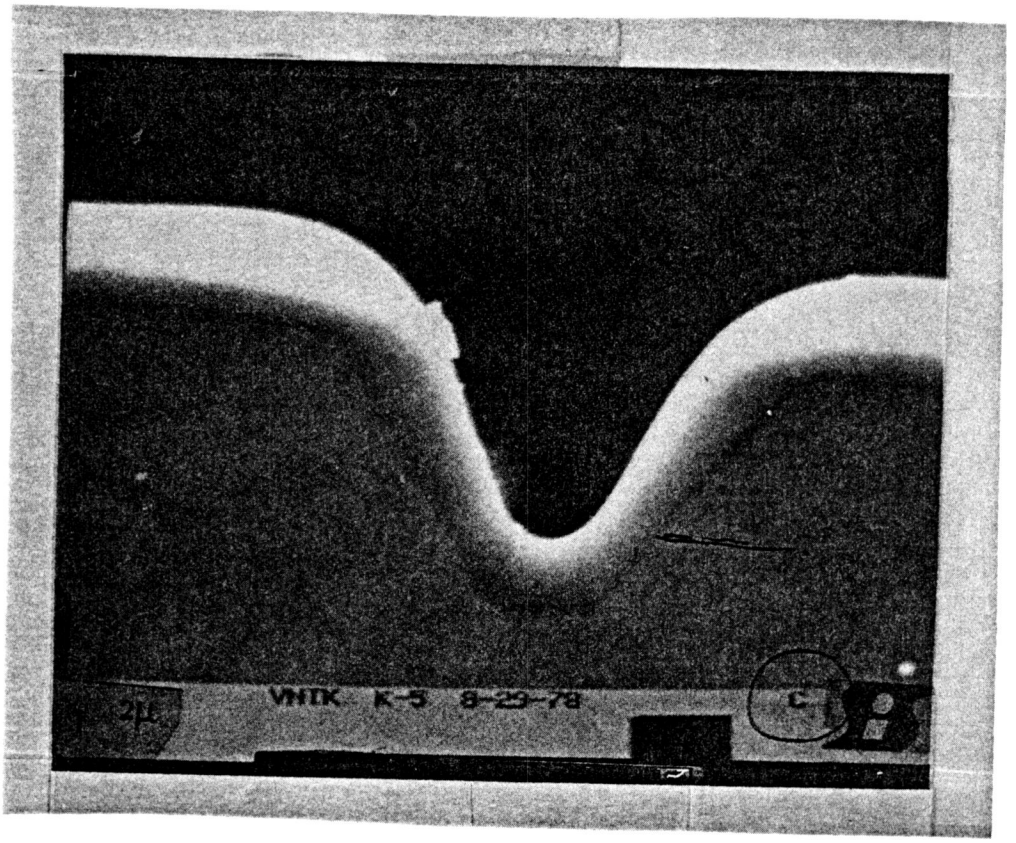


Figure (41) SEM of Reflowed Silox

4.3 Polysilicon-Gate VMOS FET Process Development

Now that a non-planar termination had been developed and the basic silicon-gate technology worked out, we proceeded to put them to use and develop a poly-gate VMOS Field-Effect-Transistor.

In this section we discuss:

1. VNTK I Design layout,

2. Polysilicon-gate VMOS fabrication steps, and

3 Evaluation of wafer runs.

4.3.1 VNTK I Design Layout

VNTK I was used as test vehicle to demonstrate the feasibility of all the concepts developed so far. Figure (42) is the photomicrograph of the chip. The chip was terminated by a V-groove with an SFP and KCC ring. Active area was 1,764 mil^2 (or .01 cm^2). The V-grooves are arranged in what is called the K-structure. In this structure, V-grooves surround the source/body contact. The results are:

1. Increase gate width (W) packing density. This means low r_{ch} and high g_m.

2. Increase epi cross-section utilization area. This means lower r_{drift}.

Figure (42A) is a SEM picture of VNTK I topology.

Figure (43) illustrates the K-structure. From Figure (43), ABCD is considered one basic cell. Different design rules could be applied. For VNTK I, a basic cell of 1.69 mil^2 was used. The total W was about 4 inch or 10 cm. This gave a W/ℓ ratio of about 5 x 10^4.

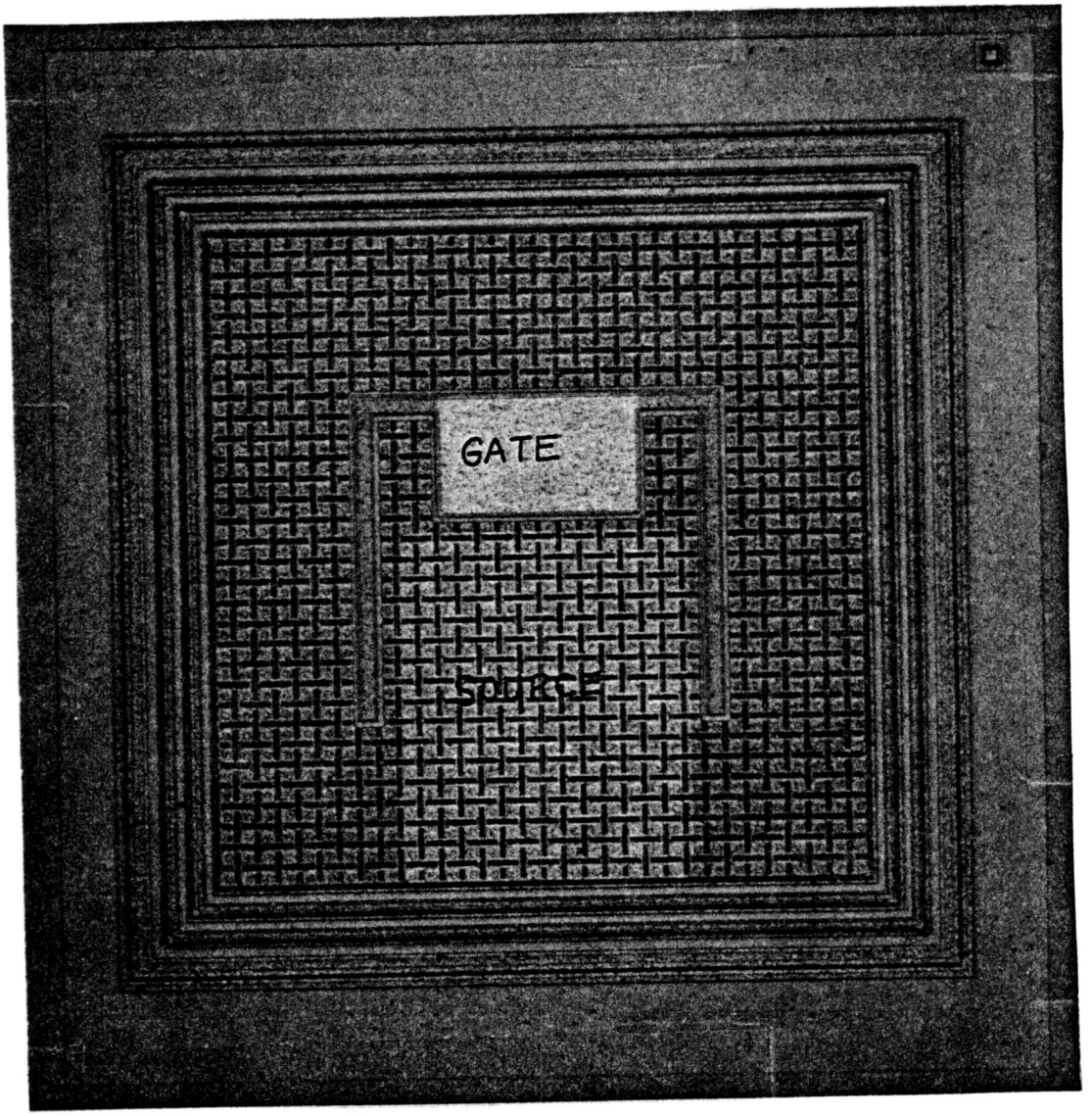


Figure (42) Photomicrograph of VNTK I

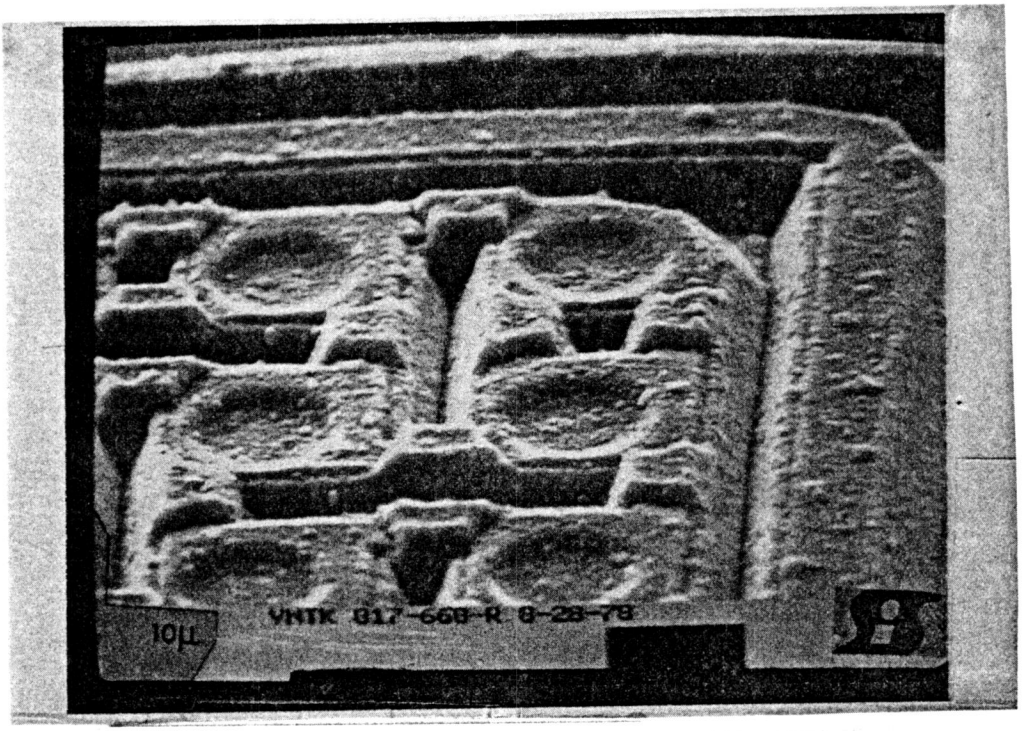


Figure (42A) SEM of VNTK I Topography

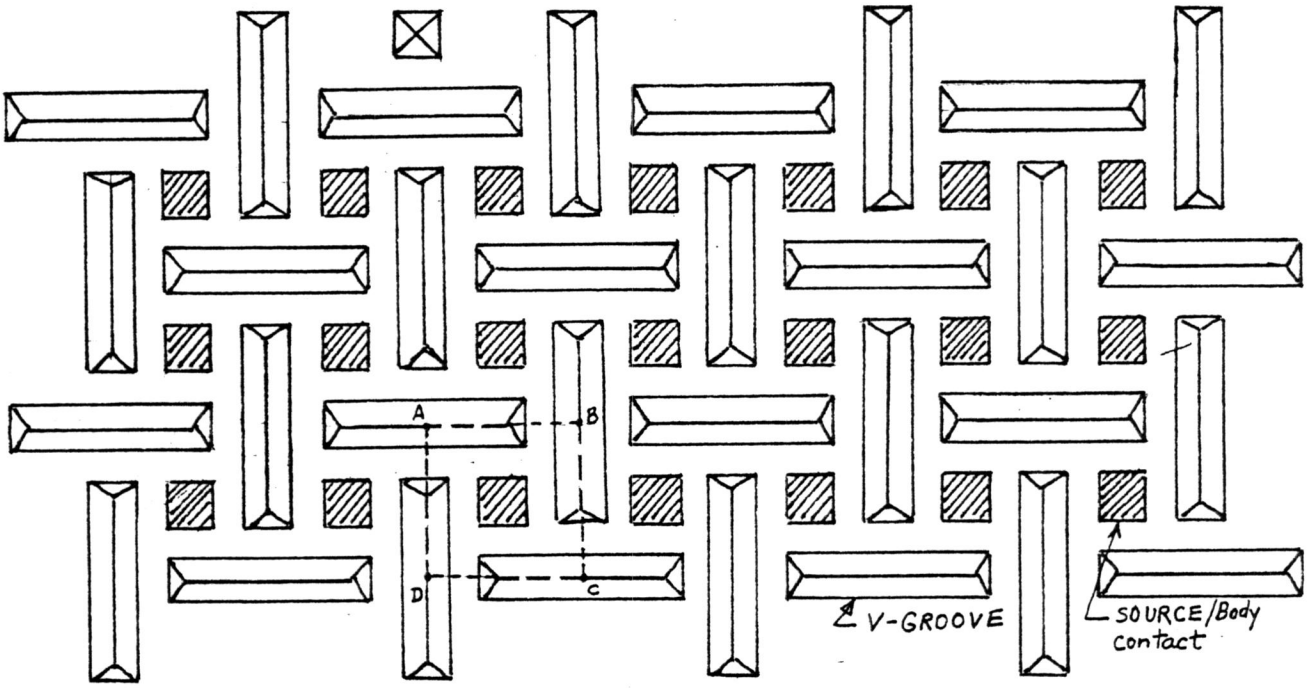


Figure (43) K-Structure
ABCD is One Basic Cell

We then calculated the $r_{DS(on)}$ of one basic cell and compared it with experimental value.

For one basic cell, W was roughly 3.75 mil, and channel length was taken as .1 mil.

Therefore: From Equation (3)

$$r_{ch} = \frac{tox}{\mu_n \epsilon_o \epsilon_{ox}} \times \frac{\ell}{W} \times \frac{1}{V_{GS} - V_T}$$

$$= \frac{.15 \times 10^{-4}}{450 \times 4 \times 8.85 \times 10^{-14}} \times \frac{.1}{3.74} \times \frac{1}{V_{GS}-2} \qquad (10)$$

Case (1) $r_{ch} = 314\Omega$ ($V_{GS} = 10V$)

Case (2) $r_{ch} = 140\Omega$ ($V_{GS} = 20V$)

Also from Equation (7)

$$r_{drift} = \frac{\rho}{4a} \left(-\ell n \frac{(a-b)}{(a+b)} \right) \quad \text{for } t_1 = b/2$$

Take $\rho = 5\Omega$ -cm,
$a = 1.3$
$b = 1.1$

$$\text{Then } r_{drift} = \frac{5 \times 393.7}{4 \times 1.3} \left[-\ell n \frac{(1.3 - 1.1)}{(1.3 + 1.1)} \right]$$

$$= 956\Omega$$

Allow 5% for other resistive components,

Therefore: $r_{DS(on)} = 314 + 956 + 63.5 = 1333\Omega$ $(V_{GS} = 10V)$

$r_{DS(on)} = 140 + 956 + 54.8 = 1150.8\Omega$ $(V_{GS} = 20V)$

Now there are 926 cells in VNTK I.

Case (1) $r_{DS(on)} = 1.44\Omega$ $(V_{GS} = 10V)$

Case (2) $r_{DS(on)} = 1.25\Omega$ $(V_{GS} = 20V)$

Experimental results on VNTK wafer no. 811-083-R gives:

Case (1) $r_{DS(on)} = 1.5\Omega$ $(V_{GS} = 10V)$

Case (2) $r_{DS(on)} = 1.3\Omega$ $(V_{GS} = 20V)$

Now review the VNTK I layout again. There is no source bonding pad, per se. The source bonds are placed directly over the active area. A 'U' shape gate bus is used to reduce the effect of polyresistance in series with the gate. Figure (44) illustrates the equivalent resistance network the input pulse sees.

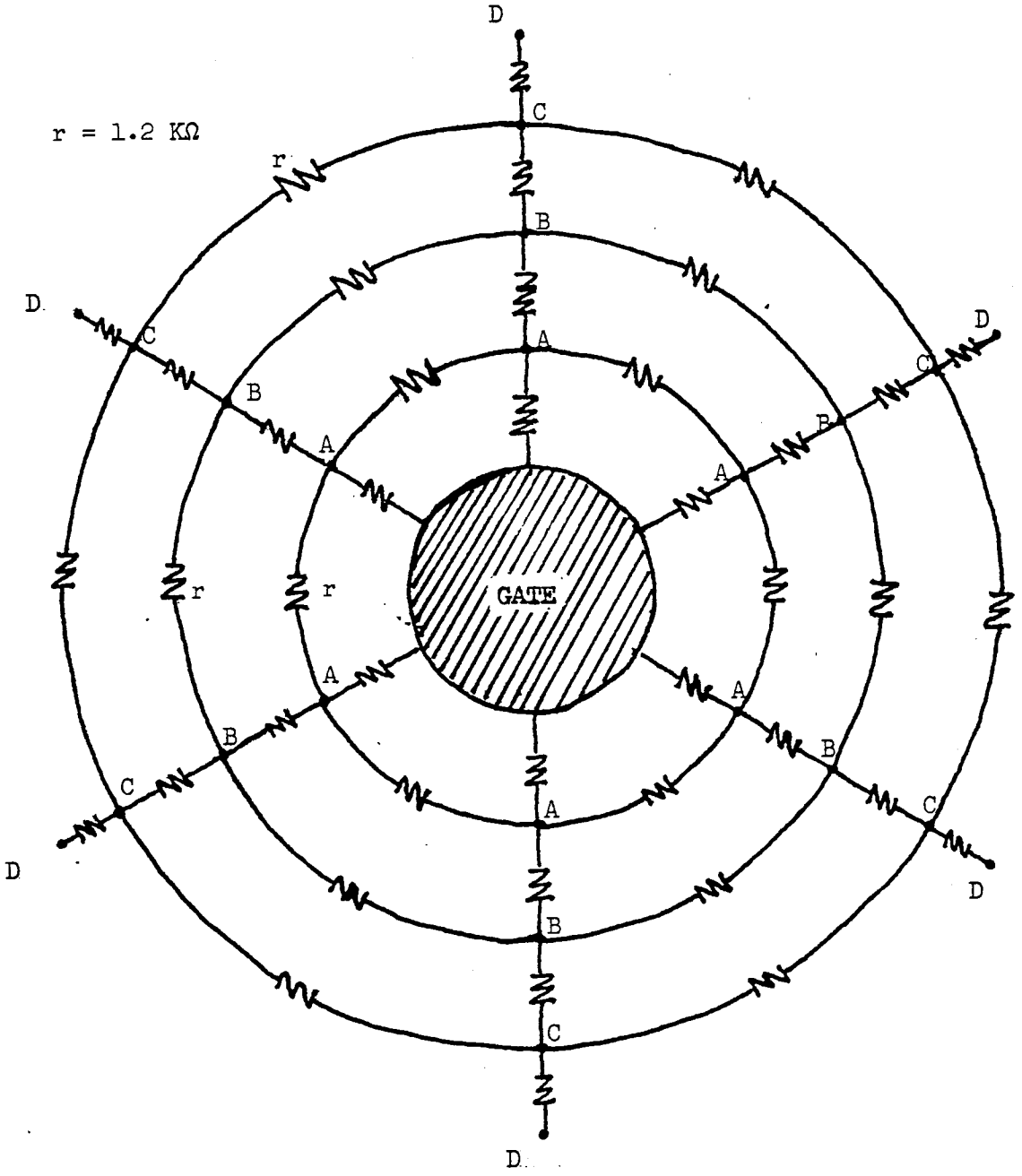


Figure (44) Resistance Network
the Input Pulse at Gate Bonding Sees

It can be shown mathematically that the max resistance between any node and gate pad is $2 * r$ We took a number of 1.2 K Ω resistors, and hooked them up according to Figure (44). The resistance between the nodes and gate are shown in Figure 45.

NODE	OHM BETWEEN GATE AND NODE
A	.47 K Ω
B	.70 K Ω
C	.97 K Ω
D	2.05 K Ω

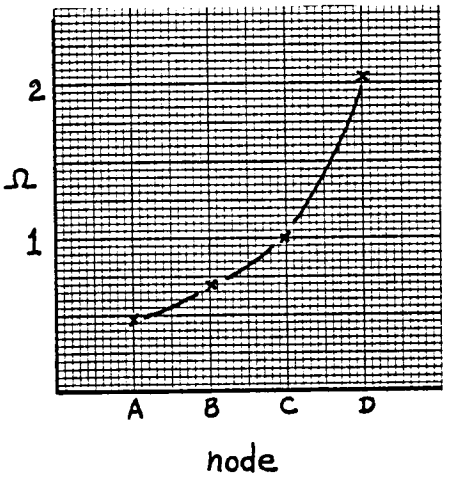


FIGURE (45) Resistance Between the Nodes and Gate

This exercise confirmed that a 'U' shape gate bus layout was an effective way to reduce the input resistance of the polysilicon gate.

4.3.2 Fabrications Steps

Many processing options are available. One option is outlined below:

Fabrication steps of a typical polysilicon-gate VMOS process.

1. Starting material

2. Epi (N^-)

3. Epi (P)

4. Source Predep and Diffusion

5. V-Groove mask and V-Groove etch

6. Gate Oxidation

7. Poly Deposition and Doping

8. Silox Deposition and Reflow

9. Contact Mask

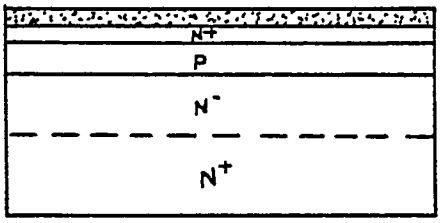
10. Metal Evaporation

11. Metal Mask

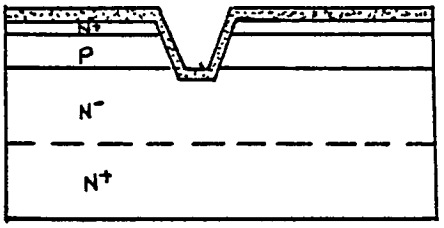
12. Top Silox Deposition

13. Top Glass Mask

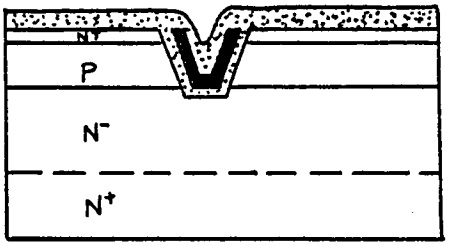
These steps are illustrated in Figure 46.



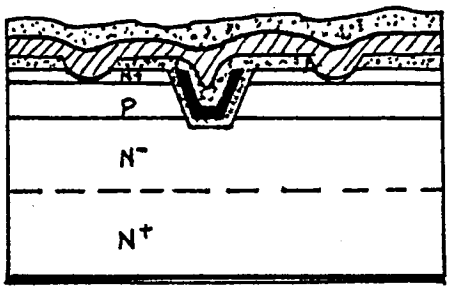
N^+ STARTING MATERIAL
N^-/P EPI
N^+ SOURCE PREDEP/DRIVE-IN



V-GROOVE MASK
GATE OXIDATION



POLY DEP
POLY MASK
SILOX



CONTACT MASK
METAL
METAL MASK
SILOX
GLASS MASK

Figure (46) Fabrication Steps of
Poly-Gate VMOS FET

4.3.3 Wafer Run Evaluations

Using VNTK I, we processed three wafer runs. (VNTK 811-083; VNTK 817-667 and VNTK 817-688). The aim of these wafer runs is first to ascertain that the concept works and second to achieve $r_{DS(on)}$ between 2 - 3Ω with breakdown between 180 - 220V. The results were positive. During the third run (namely 817-668-R) we achieved 2.5Ω $r_{DS(on)}$ and 180V BV_{DSS}. This section details the results of evaluation on 2 of 3 runs.

4.3.3.1 Evaluation Results of Wafer Run 817-668

Dies from wafer no. 11, run no. 817-668 were packaged in TO-39. The units were serialized and evaluated in terms of D.C. and A.C. parameters. Table (I) on page (73) summarizes the major D.C. parameters measured with Tektronix curve tracer 576. From the table, we see that $r_{DS(on)}$ is typically 2.5Ω; threshold voltage is around 2V, and breakdown voltage is centered at 180V.

Figure (48) on page (74) are photographs showing the family curves of unit no. 11. In Figure (48b) we see the BV_{DSS} of 200V. The units had been walked out from about 185V.

Unit no.'s 4, 5, 11, 12, 15, 16 and 31 were further evaluated. Table (II) on page (75) summarizes the D.C. parameters.

Then, the paralleling effect of $r_{DS(on)}$ of multiple units were tested. On page (77), Table (III b) summarizes the $r_{DS(on)}$ vs. V_{GS} of 2 units in parallel. Table (III c) summarizes $r_{DS(on)}$ vs. V_{GS} of 4 units in parallels. Figure (49) on page (78) is the graphical form of the three tables mentioned. From these tables and graphs, we see that the $r_{DS(on)}$ of VMOS closely obeys the parallel resistance law.

	$r_{DS(on)}$
Single Unit	2.18
2 Units in parallel	1.11
4 Units in parallel	.58

Figure (47)

Figure (47) lists the $r_{DS(on)}$ of different combinations for the case where V_{GS} = 20V.

The results showed that by increasing the active area of VNTK I 20 times, we can be assured that the $r_{DS(on)}$ will go down by 20 times or around .1Ω (Note, initial results of the experimental device VNS confirmed this point).

The capacitances of two units (no. 11 and 31 were evaluated. Figure (50) is a plot of C_{iss}, C_{oss} + C_{rss} vs V_{DS}.

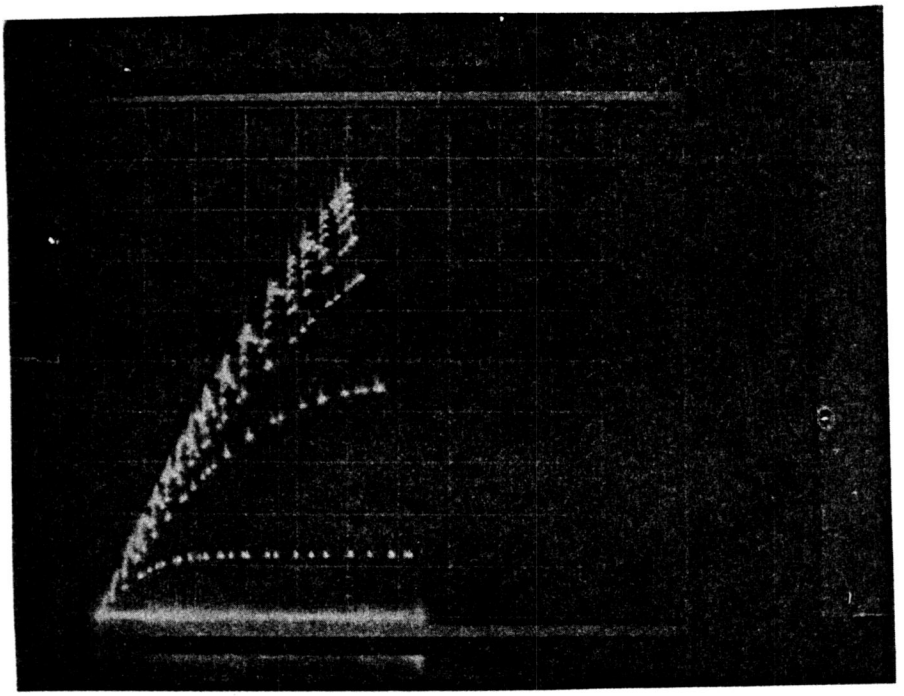
The switching speed of VNTK I was tested using the test circuit shown in Figure (53 a). Figure (53 b) shows the switching characteristics. Siliconix standard VMOS product 2N6661 was used as a control. We found that the switching characteristics of the 2N6661 did not differ significantly from that of VNTK I. Therefore, it is concluded that the switching speed measured was not the inherent switching speed of the VNTK I. The switching speed of VNTK I is faster than that shown in Figure (53 b).

TABLE I

THE MAJOR D.C. PARAMETERS OF VNTK
817-668R PACKAGED IN TO-39

Part No.	$r_{DS(on)}$ V_{GS} = 20V I_D = 1A	V_{TH} I_D = 1mA	BV_{DSS} I_D=100μA	$I_{D(OFF)}$ at 50V	
1	2.25Ω	1.8V	180V	20μA	
3	2.25Ω	1.9V	176V	4μA	
4	2.6Ω	2.1V	188V	1.5μA	
5	2.5Ω	2.0V	184V	2.5μA	
6	2.5Ω	2.2V	180V	6μA	
7	2.5Ω	2.0V	192V	30μA	
8	2.4Ω	2.1V	180V	10μA	
9	2.5Ω	2.2V	180V	5μA	
10	2.5Ω	1.9V	180V	<1μA	
11	2.6Ω	2.0V	190V	<1μA	**
12	2.5Ω	1.9V	188V	2μA	
14	2.3Ω	1.9V	176V	10μA	
15	2.4Ω	2.0V	180V	4μA	
16	2.2Ω	1.9V	170V	4μA	
17	2.5Ω	2.1V	180V	10μA	
19	2.5Ω	2.1V	180V	8μA	
20	2.4Ω	2.1V	180V	<1μA	
21	2.3Ω	2.0V	176V	25μA	
22	2.4Ω	2.1V	176V	<1μA	
23	2.4Ω	1.9V	180V	20μA	
25	2.2Ω	2.0V	170V	<1μA	
28	2.6Ω	2.2V	180V	12μA	
30	2.3Ω	2.2V	180V	1μA	
31	2.3Ω	2.1V	180V	1μA	
Mean	2.42Ω	2.03V	---------	7.28μA	
Stud. Dev.	0.124	0.114	---------	8.26	

** (See Polaroid Pictures)



HORI : 1V/DIV

VERT : .2A/DIV

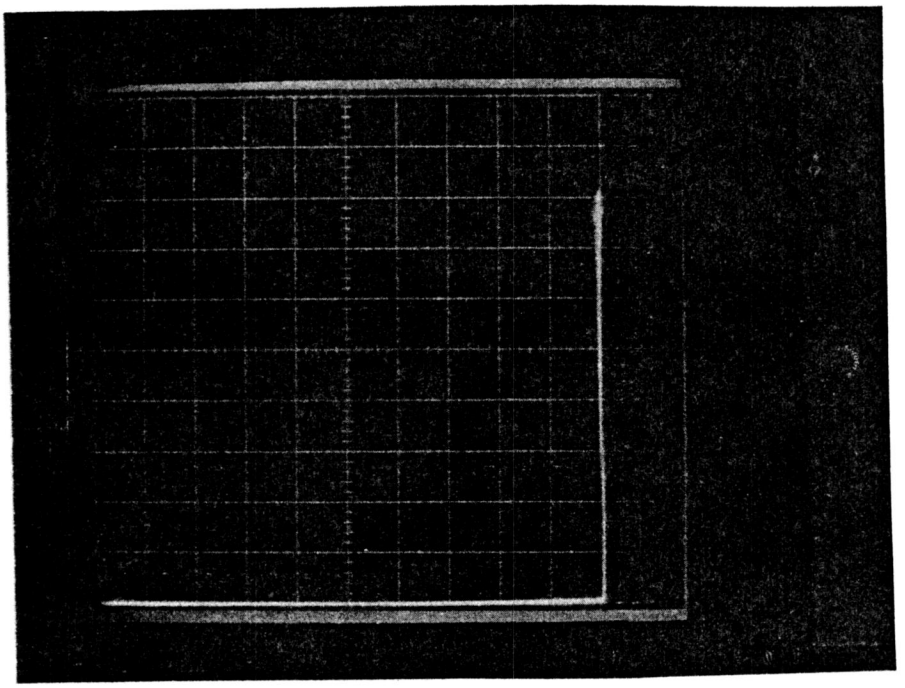
2V/STEP

10 STEPS

$r_{DS(on)}$

$= 2.5\,\Omega$ @ $V_{GS} = 20\,V$

(a)



HORI : 20V/DIV

VERT : 10μA/DIV

BVDSS : 200V

(b)

Figure (48) Drain Characteristics of VNTKI 817-668-R

WAFER #11, UNIT #11, TO 39

TABLE, II

VNTK CHARACTERIZATION

817-668-R no. 11									
Characteristic	Part Number							Unit	Test Conditions
	4	5	11	12	15	16	31		
B_{VDSS}	190	188	190	188	180	170	180	volts	V_{GS}=0, I_D=100μA
V_{GS} (th)	2.03	1.96	2.00	1.91	1.91	1.84	2.06	volts	V_{DS}=V_{GS}, I_D=1mA
I_{GSS}	0.4	0.6	0.2	0.6	0.6	0.7	0.2	nA	V_{GS}=15V, V_{DS}=0
$I_{D(on)}$	2.95	3.05	2.97	3.10	3.25	3.40	3.0	A	V_{DS}=25V, V_{GS}=10V
$V_{DS(on)}$	.360	.348	.360	.348	.333	.310	.345	volts	V_{GS}=5V, I_D=0.1A
	1.36	1.31	1.36	1.34	1.29	1.19	1.27	volts	V_{GS}=10V, I_D=0.5A
	3.04	2.86	3.05	2.92	2.75	2.54	2.83	volts	V_{GS}=10V, I_D=1.0A
	6.7	6.2	7.2	6.5	6.0	5.6	6.2	volts	V_{GS}=15V, I_D=2.0A
G_m	333	333	333	333	333	333	333	mμ	V_{DS}=25V, I_D=0.5A
I_{DSS}	4.62	13.6	2.25	6.86	18.6	20.4	7.5	μA	V_{DS}=100V, V_{GS}=0

TABLE III

VNTK - $r_{DS(on)}$ vs. V_{GS} at V_{DS} = 0.1V

(a) Part Number (single devices)

4		5		12		15		16	
$r_{DS(on)}$	V_{GS}	$r_{DS(on)}$	V_{GS}	$r_{DS(on)}$	V_{GS}	$r_{DS(on)}$	V_{GS}	$r_{DS(on)}$	V_{GS}
1000Ω	1.78V	1000Ω	1.70V	1000Ω	1.65V	1000Ω	1.67V	1000Ω	1.60V
400	1.87	400	1.78	400	1.74	400	1.76	400	1.69
200	1.95	200	1.86	200	1.82	200	1.84	200	1.76
100	2.03	100	1.95	100	1.91	100	1.92	100	1.84
40	2.19	40	2.11	40	2.06	40	2.06	40	1.98
10	2.67	10	2.58	10	2.54	10	2.50	10	2.38
4	4.33	4	4.16	4	4.11	4	3.95	4	3.65
3.55	5.0	3.44	5.0	3.44	5.0	3.31	5.0	3.09	5.0
2.93	7.0	2.85	7.0	2.86	7.0	2.78	7.0	2.61	7.0
2.30	15.0	2.23	15.0	2.26	15.0	2.20	15.0	2.07	15.0
2.18	20.0	2.15	20.0	2.16	20.0	2.11	20.0	1.99	20.0

PART NUMBER

(b)		(c)	
Two Parallel Devices 4 and 5		Four Parallel Devices 4, 5, 12, 15	
$r_{DS(on)}$	V_{GS}	$r_{DS(on)}$	V_{GS}
1000Ω	1.67V	1000Ω	1.55V
400	1.76	400	1.64
200	1.83	200	1.71
100	1.91	100	1.78
40	2.03	40	1.89
20	2.15	20	1.99
10	2.32	10	2.11
4	2.83	4	2.35
2	4.28	2	2.77
1.77	5.0	1.0	4.30
1.46	7.0	0.89	5.0
1.28	10.0	0.75	7.0
1.17	15.0	0.67	10.0
1.11	20.0	0.61	15.0
		0.58	20.0

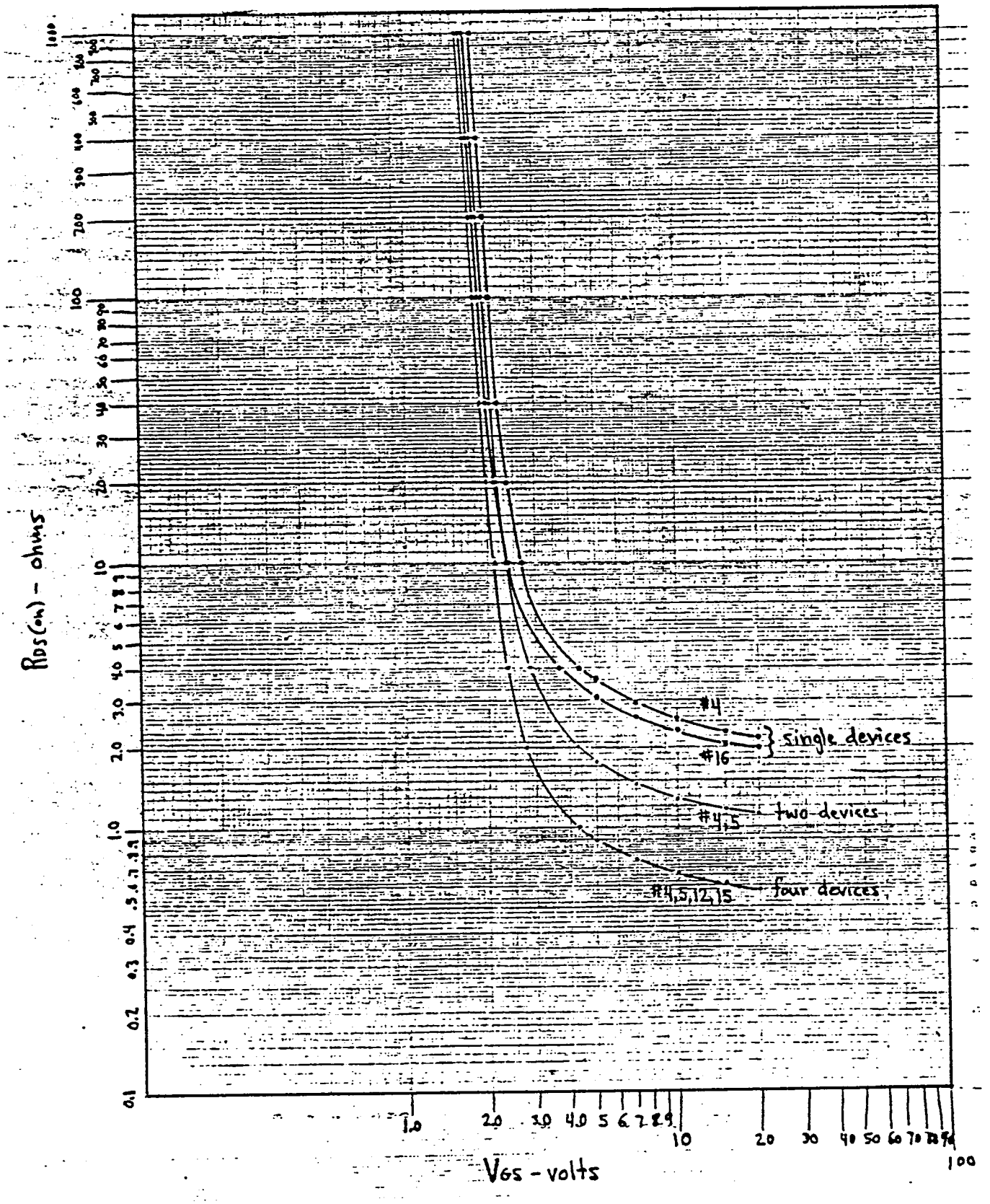


Figure (49) VNTKI—$r_{DS(on)}$ vs V_{GS}— for Single and Paralleled Devices

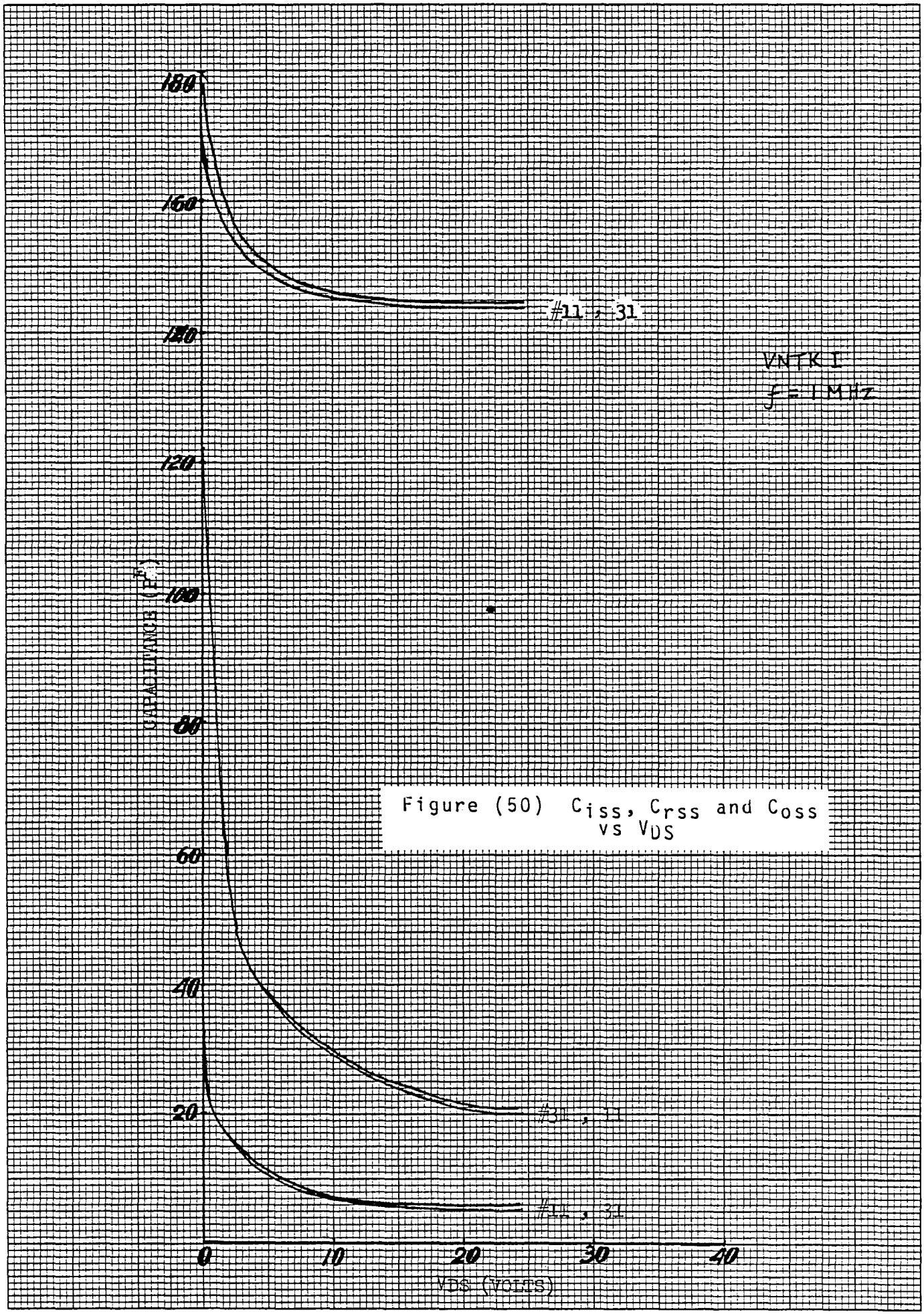
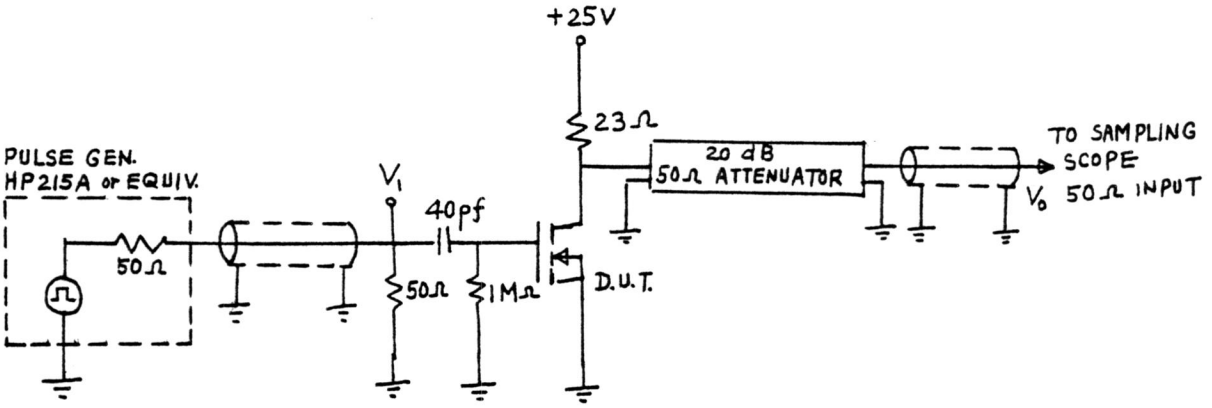
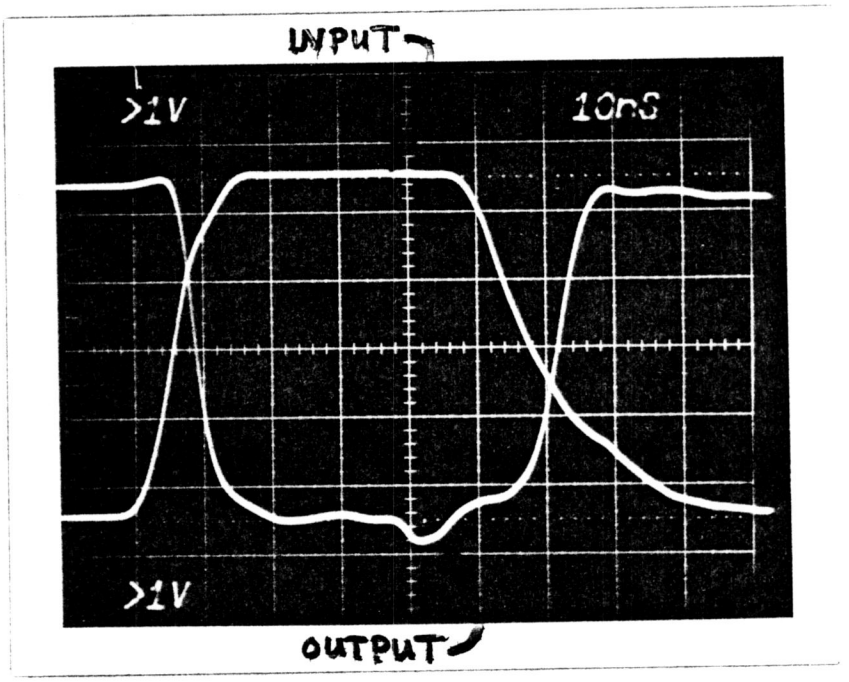


Figure (50) C_{iss}, C_{rss} and C_{oss} vs V_{DS}



(a)

SWITCHING TEST CIRCUIT



(b)

Figure (53) VNTK Switching Characteristics

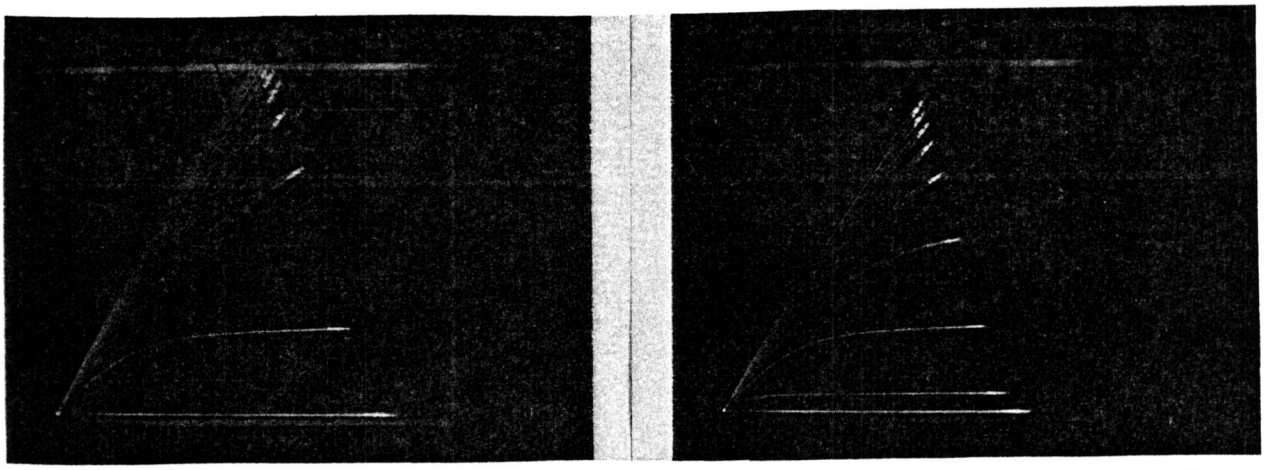
4.3.3.2 Evaluation Results of Wafer Run no. 811-083

Wafer run no. 811-083 was the first of three runs processed to demonstrate the feasibility of the poly-gate concept. Evaluation results were positive. They are described in this section.

The typical $r_{DS(on)}$ is 1.5Ω for V_{GS} = 10V and 1.3Ω for V_{GS} = 20V. (See Figure (54)) From section 4.3.1, we find that these values followed very closely with the calculated values which are 1.44Ω and 1.25Ω respectively. The transconductance is about 700 mμ and the drain current is about 5A at V_{GS} = 10V. Figure (55) is the transfer curve of wafer no. 295C1. The result of velocity saturation of carriers is evident by virtue of the constant slope.

The W/ℓ ratio of VMOS is a big number. For example, for VNTK I, it is approximately 5×10^4. (For the experimental device which is about twenty times the size of VNTK I, the ratio is in the neighborhood of 750,000.) We measured the drain current as a function of gate-to-source voltage again. This time in the sub-threshold region. Figure (56) shows the graphical data. From Figure (56), we see that exponential function of I_D on V_{GS} is clearly evident. The pn junction leakage is about 10 na. This occurs at V_{GS} up to 1.5V. From V_{GS} = 1.5V on, drain current is an exponential function of V_{GS} until V_{GS} approaches 4.0V.

Frequency response of the VNTK I, which is a poly-silicon gate VMOS FET, and the VNA, which is an interdigitated metal-gate device, were compared in a small-signal class A amplifier configuration. Figure (57) and Figure (58) show the results. It is found that the two devices are about the same. Again, we attribute this to be limitation of the test Jig.



HORI: .5V/DIV 2V/STEP
VERT: .2A/DIV 10 STEPS

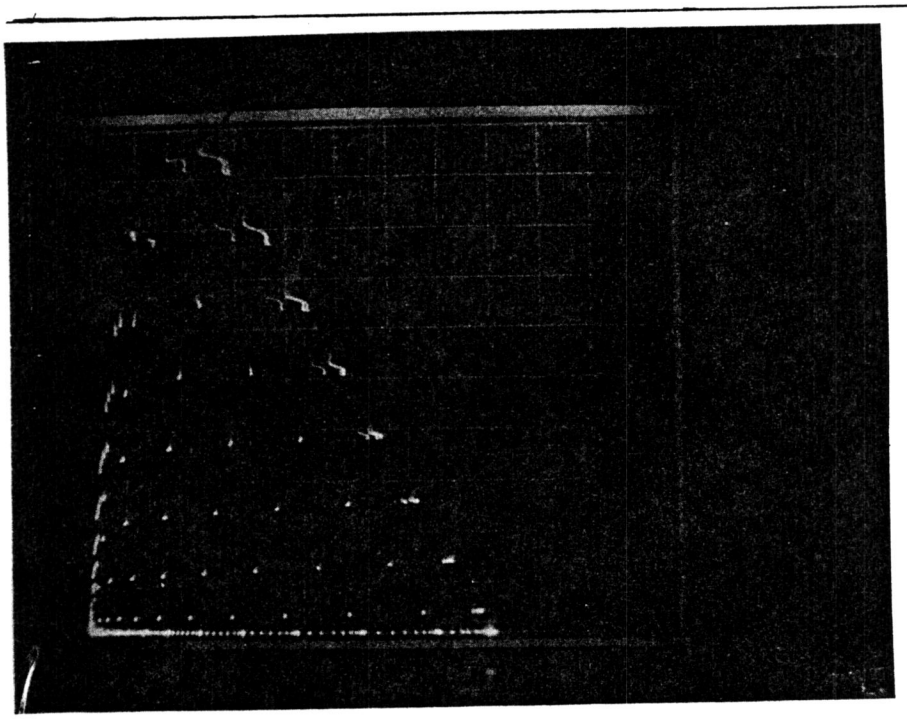
$r_{DS(on)} = 1.3\ \Omega$ at $V_{GS} = 20\ V$

(a)

HORI: .5V/DIV. 1V/STEP
VERT: .2A/DIV. 10 STEPS

$r_{DS(on)} = 1.5\ \Omega$ at $V_{GS} = 10\ V$

(b)



HORI: 10V/DIV.
VERT: .5A/DIV.
1 V/STEP
10 STEPS

$g_m \cong 700\ mU$

(c)

Figure (54) Typical Drain Characteristics of VNTK I 811-083-R

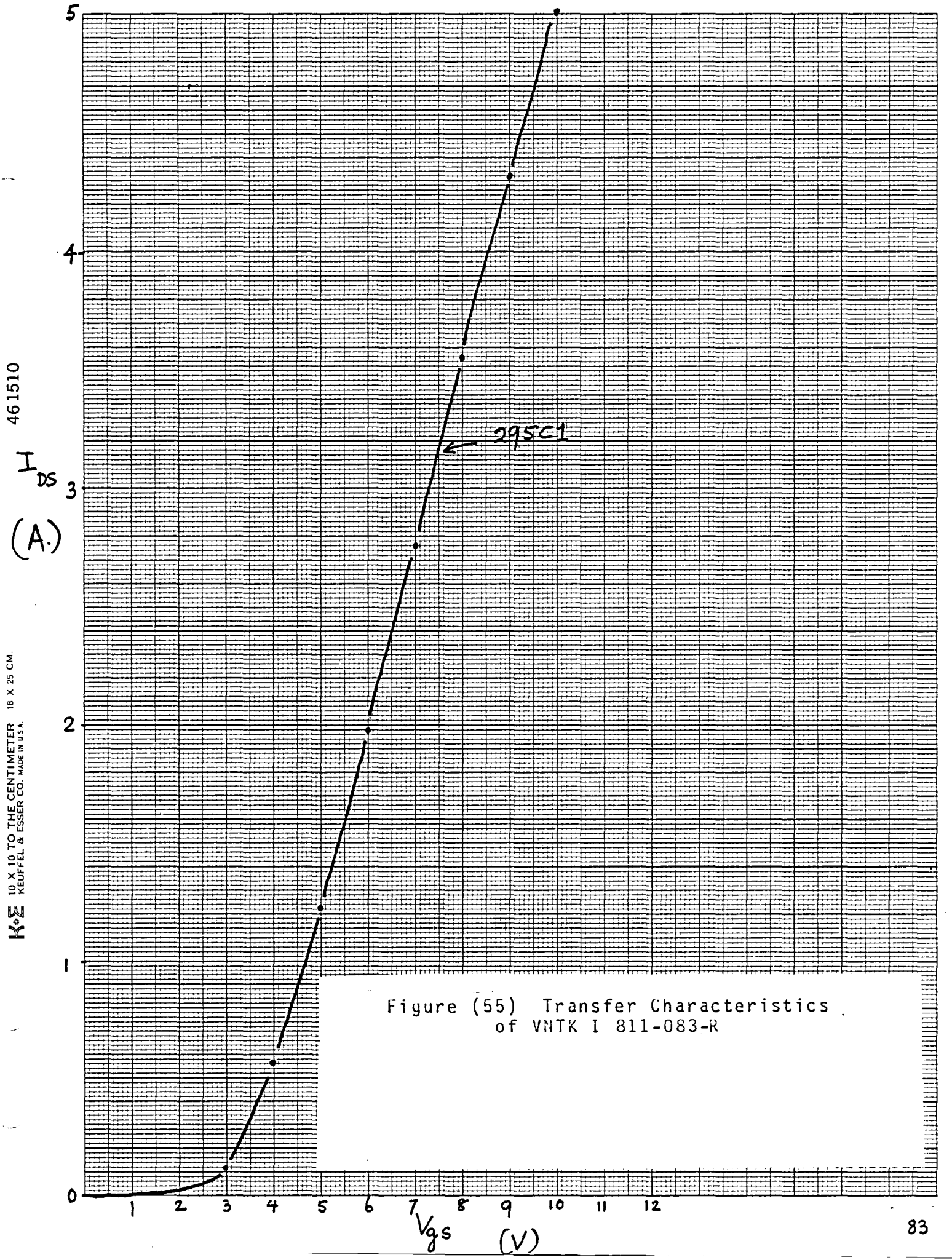


Figure (55) Transfer Characteristics of VNTK I 811-083-R

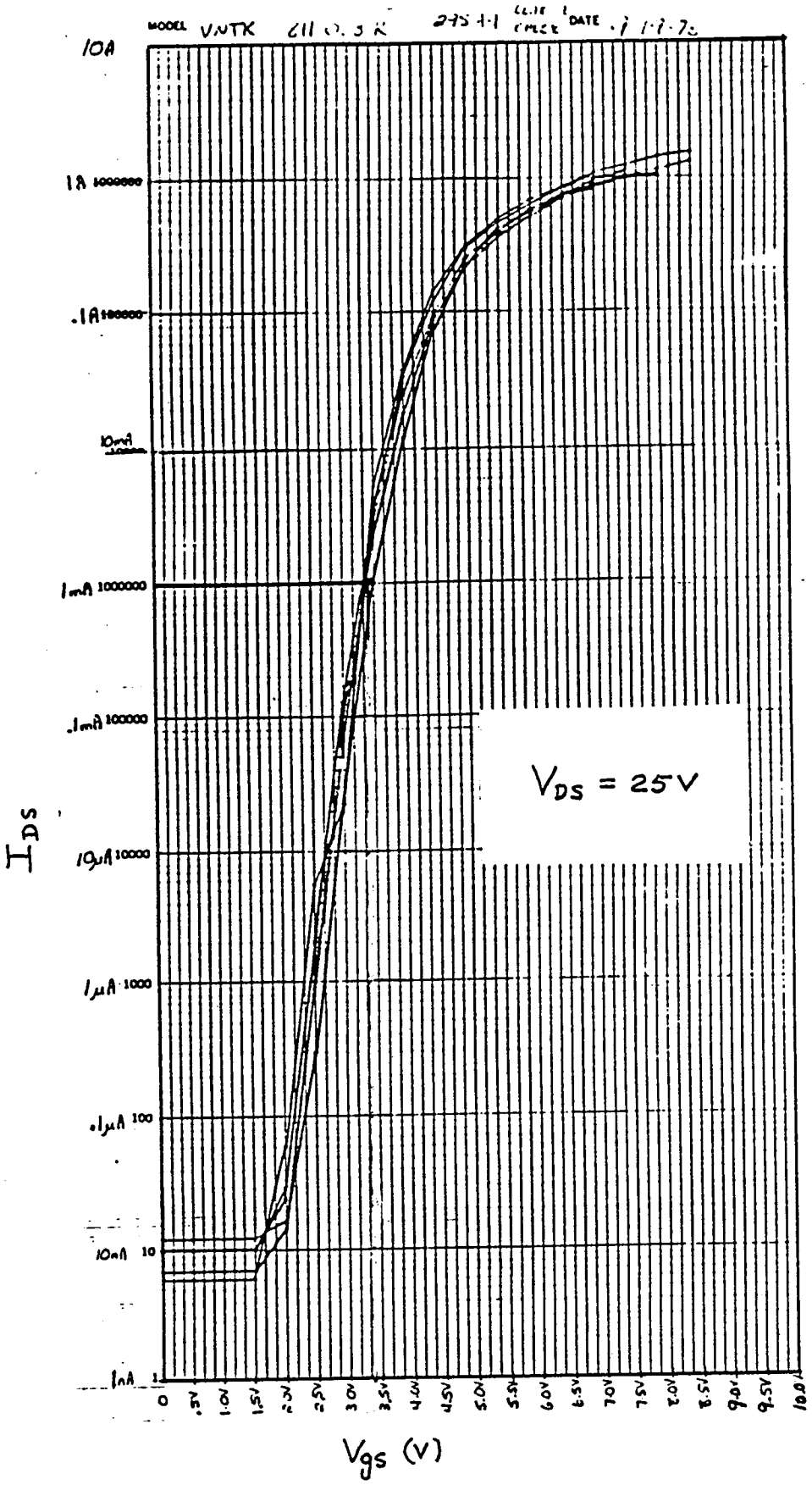


Figure (56) Transfer Characteristics
of VNTK I 811-083-R
Exponential Region

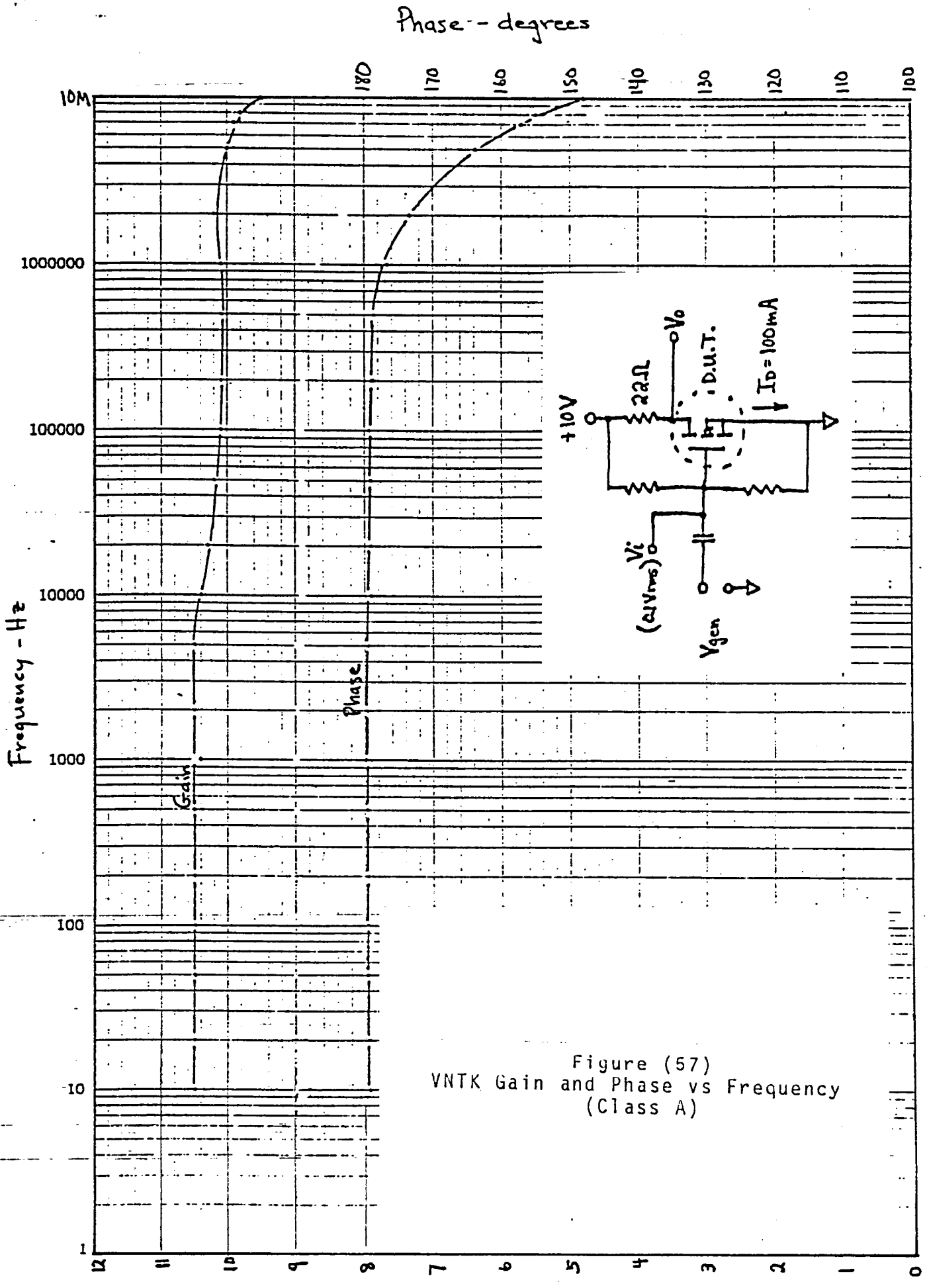


Figure (57)
VNTK Gain and Phase vs Frequency
(Class A)

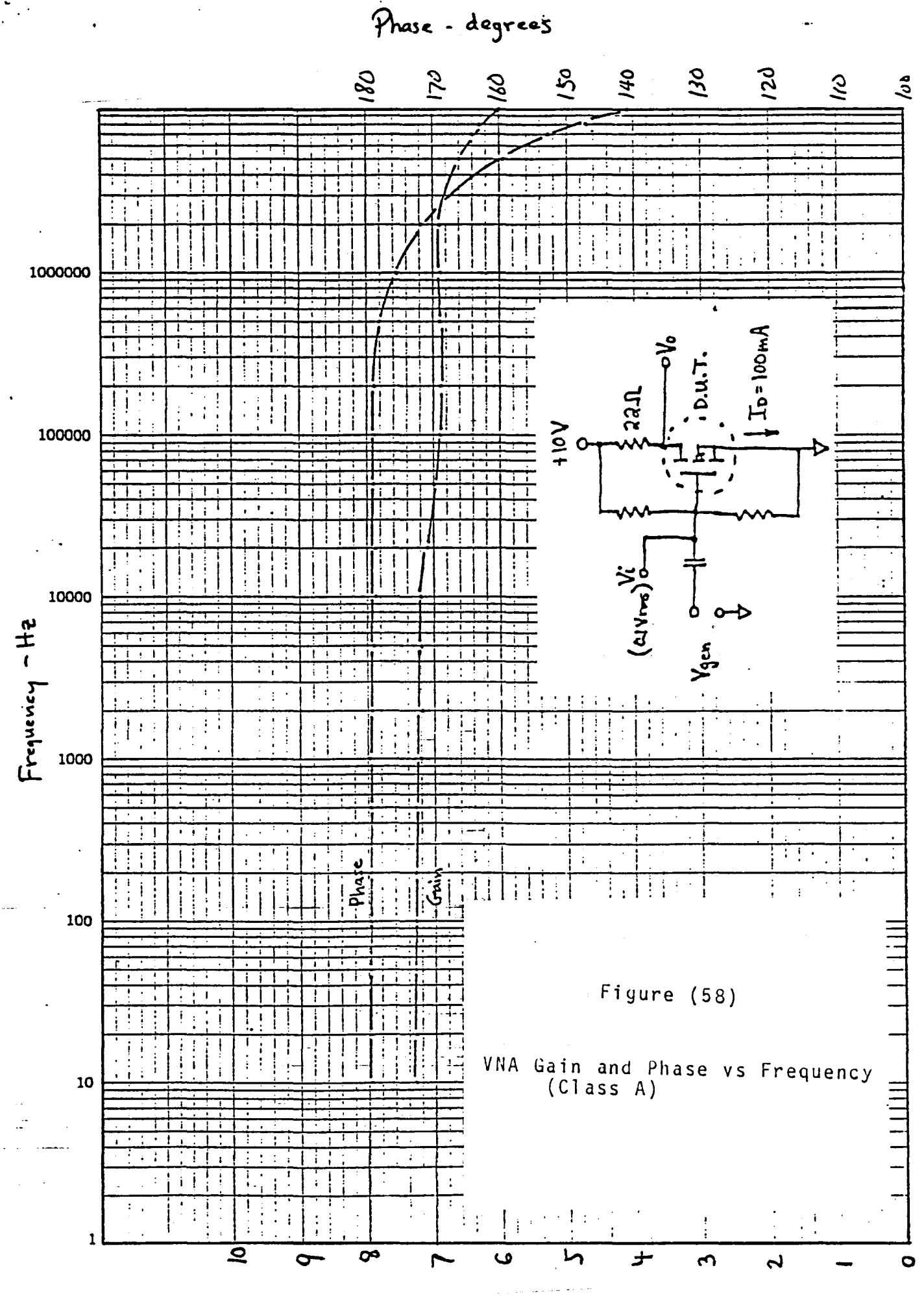


Figure (58)

VNA Gain and Phase vs Frequency
(Class A)

5.0 FABRICATION OF EXPERIMENTAL DEVICE (VNS)

The VNTK I was expanded about twenty times. The result was a new geometry, termed VNS.

In this section, the VNS design layout and the initial results achieved are discussed.

5.1 VNS Layout

Figure (59) is the photomicrograph of the experimental device, VNS. The basic layout is that of a VNTK I, namely a poly-gate with K-structure. Unit cell size is 1 x 1 mil^2. The termination scheme is again a V-groove termination with SFP and RCC ring. To reduce the series-gate resistance, an 'E' shape gate metal bus is employed. The total chip size including scribe-line area is 150 x 200 mil^2 or .19 cm^2. The 'net' active area excluding the gate metal bus is 23330 mil^2 or .15 cm^2. The percentage ratio of the net active area to total chip size is 80%. (For a single layer metal gate, the ratio is between 30% to 50% depending on current rating.) The total W is (77856 x .80) 62284 mil. If we take ℓ as .08 mil, then a W/ℓ ratio of 778,560 is realized.

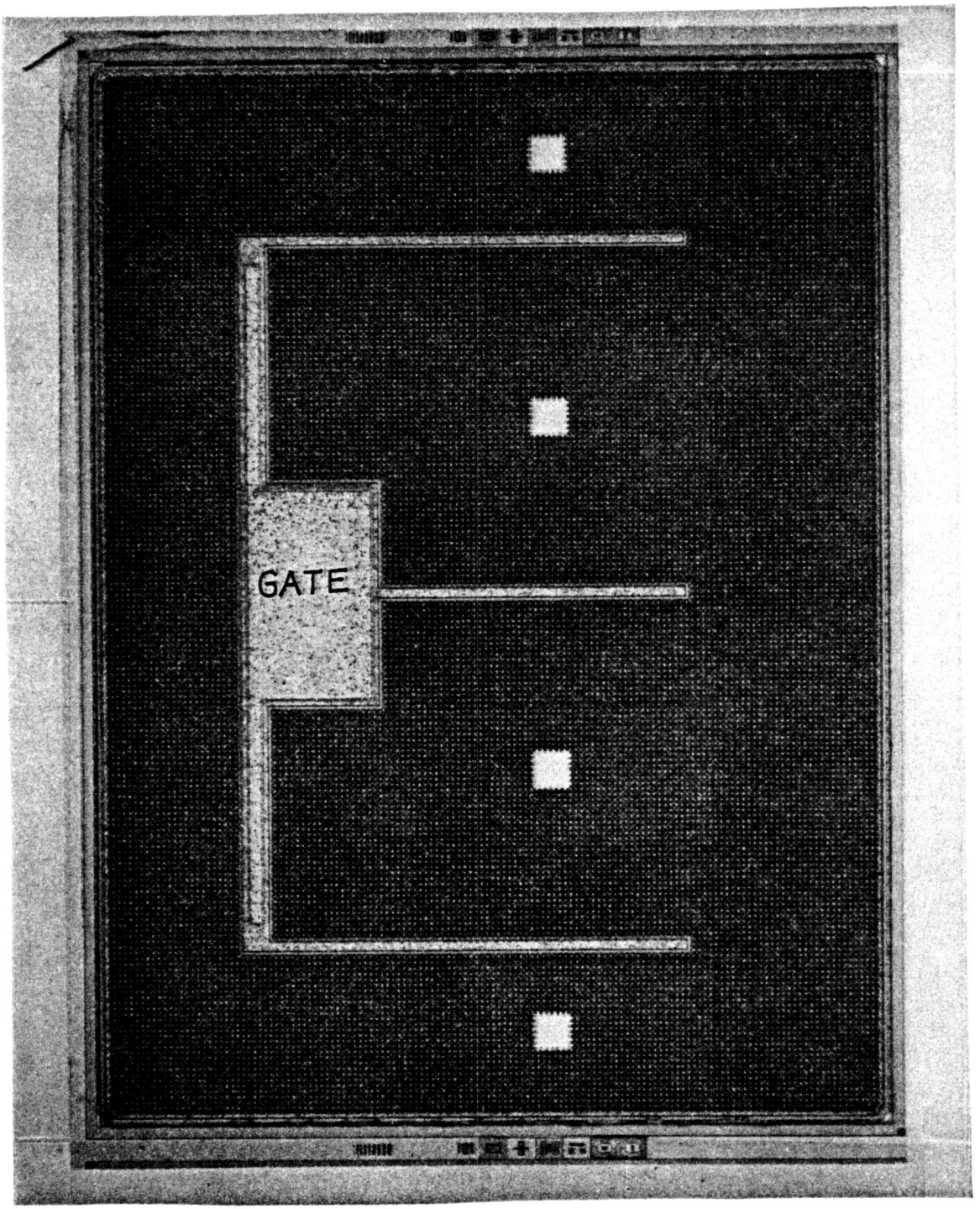


Figure (59) Photomicrograph of VNS

The 'ON' resistance is calculated as follows: The ratio of one basic cell size of VNS to that of VNTK I is 1:1.69.

From paragraph 4.3.1 the rDS(on) of 1 VNTK I basic cell is:

Case 1 1333Ω for VGS = 10V

Case 2 1150Ω for VGS = 20V

Therefore, we estimate that rDS(on) for one VNS basic cell - -

Case 1 1333 x 1.69 = 2752 (VGS = 10V)

Case 1 1150 x 1.69 = 1943 (VGS = 20V)

The total number of unit cell is 23330.

Therefore, the rDS(on) for VNS is

Case 1 $\frac{2752}{23330} = .096\ \Omega$

Case 2 $\frac{1943}{23330} = .08\ \Omega$

From the above calculation, it is seen that .1 ± 20% Ω at room temperature is realizable.

5.1.1 Switching Speed Simulation

The short-channel MOSFET model of ISPICE, (available through National CSS, Inc.) was modified to take low output conductance, constant g_m and fixed r_{drift} resistance into consideration to simulate the Siliconix VMOS. The parameters are determined as follows: (Ref. 18)

Using the data on V_T versus back-gate bias, Figure (8) page (16) the effective bulk channel impurity concentration was determined to be $2 \times 10^{16}/cm^3$. r_{drift} per centimeter of channel width (W) takes the place of RD. LAMBDA, which determines the amount of channel length modulation (and hence the output conductance), was fixed as IE-6. UO is assumed to be 450 $cm^2/V\text{-sec}$.

$$PHI = 2\phi f = \frac{2 \times KT}{q} \ln \frac{NB}{Ni} = .736$$

$$(NB = 2 \times 10^{16}/cm^3).$$

$$PB = KT/q \ \ln(N_A N_D/N_i 2) = .677$$

$$\simeq .7 \ (N_A = 2 \times 10^{16};\ N_D = 2 \times 10^{15})$$

KN and MN are two empirical constants for carrier mobility reduction due to the normal field (gate voltage). KL and Ecrit are constants to account for the scattering limited velocity of carriers due to the lateral field (drain voltage). Beta and Gamma are calculated internally. The following is the list of parameters used for VMOS simulation:

		Values	Unit
VTO	Zero-bias threshold voltage	1.5	V
PHI	Surface potential	.7	V
UO	Zero-bias surface mobility	450	cm^2/V-sec
NB	Substrate doping concentration	2E16	cm^{-3}
RD*	Drain ohmic resistance per unit channel width	3.25	Ω per cm
RS*	Source ohmic resistance per unit channel width	.05	Ω per cm
CO	Gate oxide capacitance per unit area	2.9 E-8	F per cm^2
C1**	Gate to source overlap cap/unit W	9E-12	F per cm
C2**	Gate to drain overlap cap/unit W	3E-12	F per cm
CBD**	Bulk to drain zero-bias cap/unit W	11.8E-12	F per cm
CBS**	Bulk to source zero-bias cap/unit W	0	F per cm
PB	Bulk junction potential	.7	V
IS	Bulk junctional saturation current	1E-14	Amps
KN	Normal field mobility coefficient	.00125	--
MN	Normal field mobility exponent	1.12	--

		Values	Unit
KL	Lateral field mobility parameter	20	--
ECRIT	Velocity limiting lateral field	1E5	V/cm
BETA	Transconductance factor	Calculated internally	$Amps/V^2$
GAMMA	Bulk threshold parameter		V
LAMBDA	Channel length modulation parameter	E1-6	am/V-1/2

* This parameter is multiplied internally by channel width

** This parameter is divided internally by channel width

Using these values, we have simulated the VNS on a computer to get some ideas about t_{on} and t_{off}. Figure (60) is the plot of the simulation result.

```
16.17.16 >print vmos2 model

.VMOS2
NSCM(VTO=1.5,PHI=.7,UO=450,NB=2E16,RD=3.25,RS=.05,&
CO=2.9E-8,C1=9E-12,C2=3E-12,CBD=11.8E-12,PB=.7,&
KN=.00125,M=1.12,KL=20,ECRIT=1E5,LAMBDA=1E-6)
```

Vk ckt

```
VDD 5 0 50V
VIN 1 0 PULSE (0V,20V,1NS,1NS,1NS,200NS,5US)
RG 1 3 8
RD 5 4 5
M1 4 3 0 0 VMOS2 6.6E4MI 0.1MI
EOF:
```

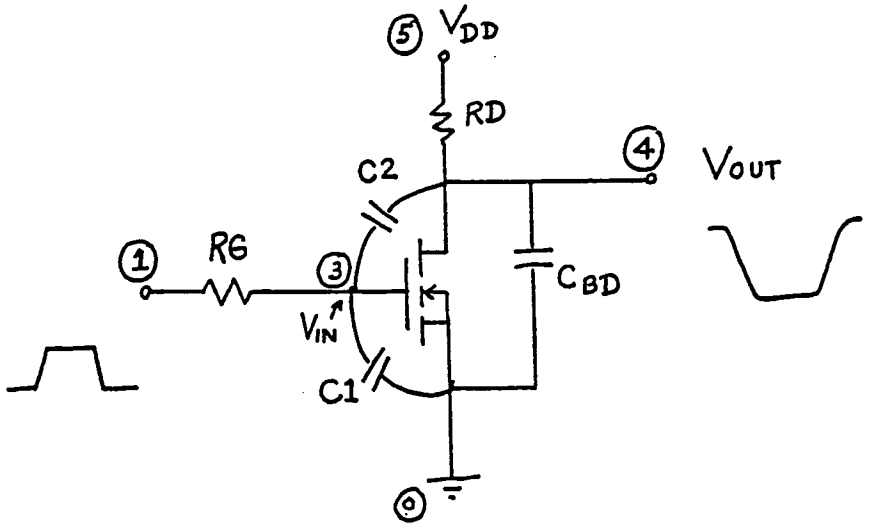


Figure (60) Simulated Switching Characteristics

OVER →

Figure (60) Continued

5.2 Initial Results

The first VNS wafer run was processed on 4-6 Ω - cm epi resistivity material. The run was split into different groups. Table (IV) summarizes the evaluation data in the wafer form. Figure (61) and (62) are pictures of the drain characteristics.

	$r_{DS(on)}$ (Ω)	g_m	BV_{DSS} (volt)	Gate-to-Source Leak
Group I	.14 - .2	6-8	100-120V	Yes and No
Group II	.3 - .6	4-5	180-200V	Yes
Group III	——————(Non Functional)——			No

Table IV Evaluation Summary of 1st VNS Run

From the data, we noted that none of the group met the intended spec. However, each group supplements what the other group lacks. For example, GROUP I shows that the $r_{DS(on)}$ and g_m are on target. The device can deliver over 50A of pulsed drain current with 10V gate drive. It is short in breakdown voltage. The gate and source are leaky due to processing flaws. GROUP II exhibits 200V breakdown voltage, but is shy on $r_{DS(on)}$ and g_m. This group also magnifies the gate-to-source leaks. GROUP III, although non-functional because of a severe source-to-drain short, proves that the gate-to-source leak is a processing flaw in GROUP I and GROUP II.

We took a GROUP I wafer, and packaged die in TO-3 packages. Unit 1, 4, 5, and 7 were further evaluated. Table (V) show the D.C. parameters.

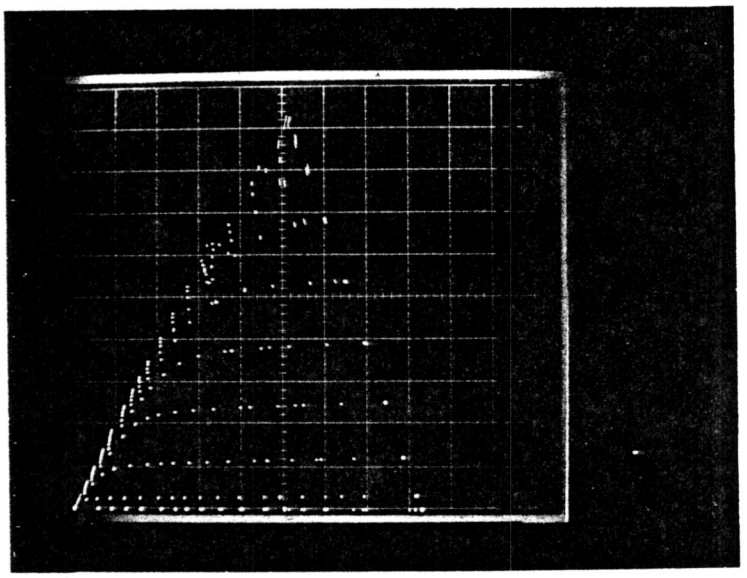
Figure (66) shows $r_{DS(on)}$ vs V_{GS} for unit no. 5. From the figure, it is seen that $r_{DS(on)}$ is .12Ω at V_{GS} = 20V. Note that this $r_{DS(on)}$ is achieved with the same 5Ω - cm epi which gives 200V in group 2. If V-groove width x is increased, $r_{DS(on)}$ is expected to get lower.

The terminal capacitances vs drain - to - source voltage are shown in figure (67).

Figure (68) shows the switching waveform. It is noted that with 50 ohm source impedance, the input drive is loaded down with the relatively high input capacitance of VNS. Under this drive condition, the t_{off} is about 100 ns. Faster switching speeds are possible with drive of lower source impedance.

Figure (68A) shows the dv/dt test. The test circuit is enclosed in the insert. It has been demonstrated that the device can withstand a dv/dt in excess of 7.5V/ns without damage.

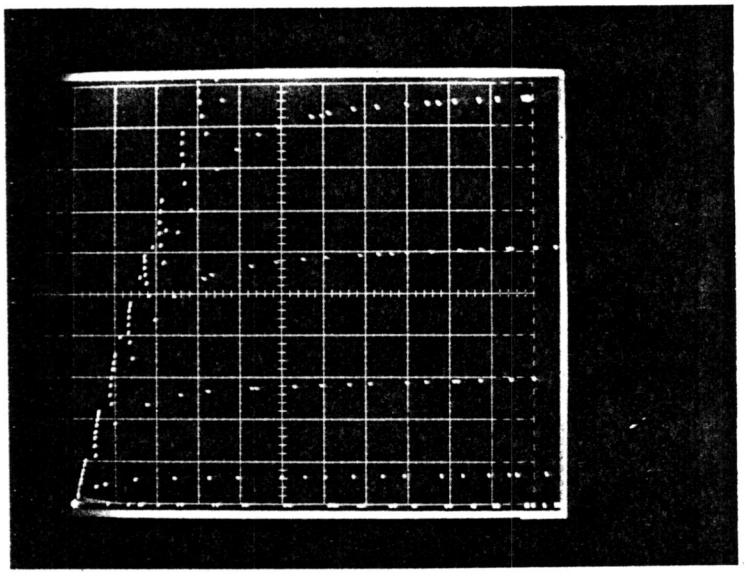
Figure (69A) and figure (69b) are pictures of VNS in TO-3.



VERT: 5A/DIV.
HORI: 2V/DIV.
1V/STEP
10 STEPS

$I_{D(ON)} \geq 50A$
at $V_{GS} = 10V$

(a)

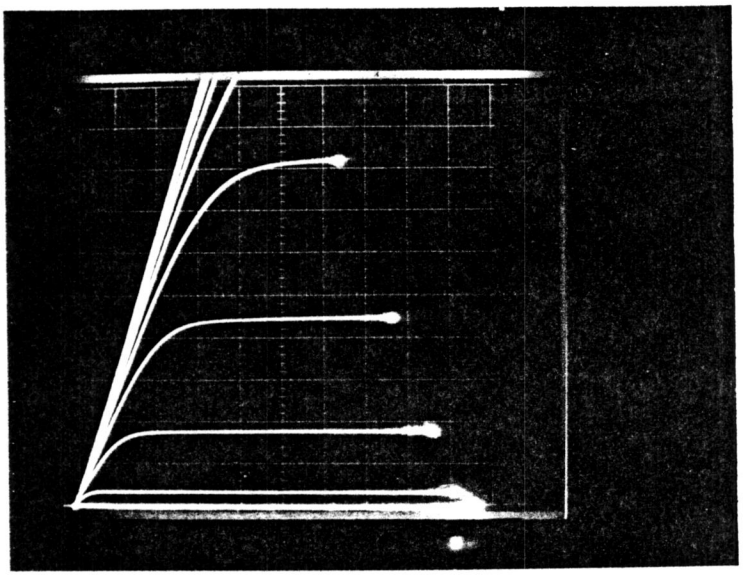


VERT: 2A/DIV.
HORI: 1V/DIV.
1V/STEP
10 STEPS

ON RESISTANCE
$= .14\Omega$ at $V_{GS} = 10V$

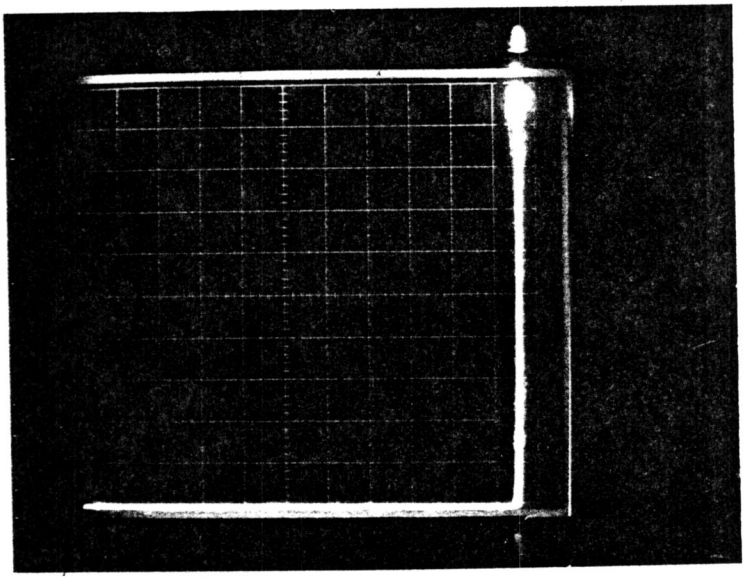
(b)

Figure (61) VNS (1st run) Group 1
Drain Characteristics



VERT: .5A/DIV
HORI: 1V/DIV
1V/STEP
10 STEPS

(a)



VERT: 20 MA/DIV.
HORI: 20V/DIV

$BV_{DSS} \geq 200V$

(b)

Figure (62) VNS (1st run) Group 2 (WAFER #3)
Drain Characteristics

TABLE V

VNS CHARACTERIZATION in TO-3

group 1

TEST	1	4	5	7	UNITS	TEST CONDITIONS
BV_{DSS}	110	109	96	116	Volts	V_{GS}=0, I_D=150mA
I_{SB}	150	150	300	170	mA	V_{GS}=0, V_{DS}=BV_{DSS}
$r_{DS(on)}$	-	0.119	0.119	0.141	↑	V_{DS}=0.1V, V_{GS}=20V
	-	0.127	0.122	0.147	Ω	" V_{GS}=15V
	-	0.149	0.139	0.167	|	" V_{GS}=10V
	-	0.244	0.206	0.253	↓	" V_{GS}= 5V
V_{GS} (th)	-	2.26	2.33	2.28	Volts	V_{GS}=V_{DS}, I_D=50mA
I_{DSS}	-	15.8	21.0	23.0	mA	V_{DS}=25V, V_{GS}=0
I_{GSS}	-	2	2	* 23μA	nA	V_{DS}=0, V_{GS}=25V

* This part has a "fixed" G-S short.

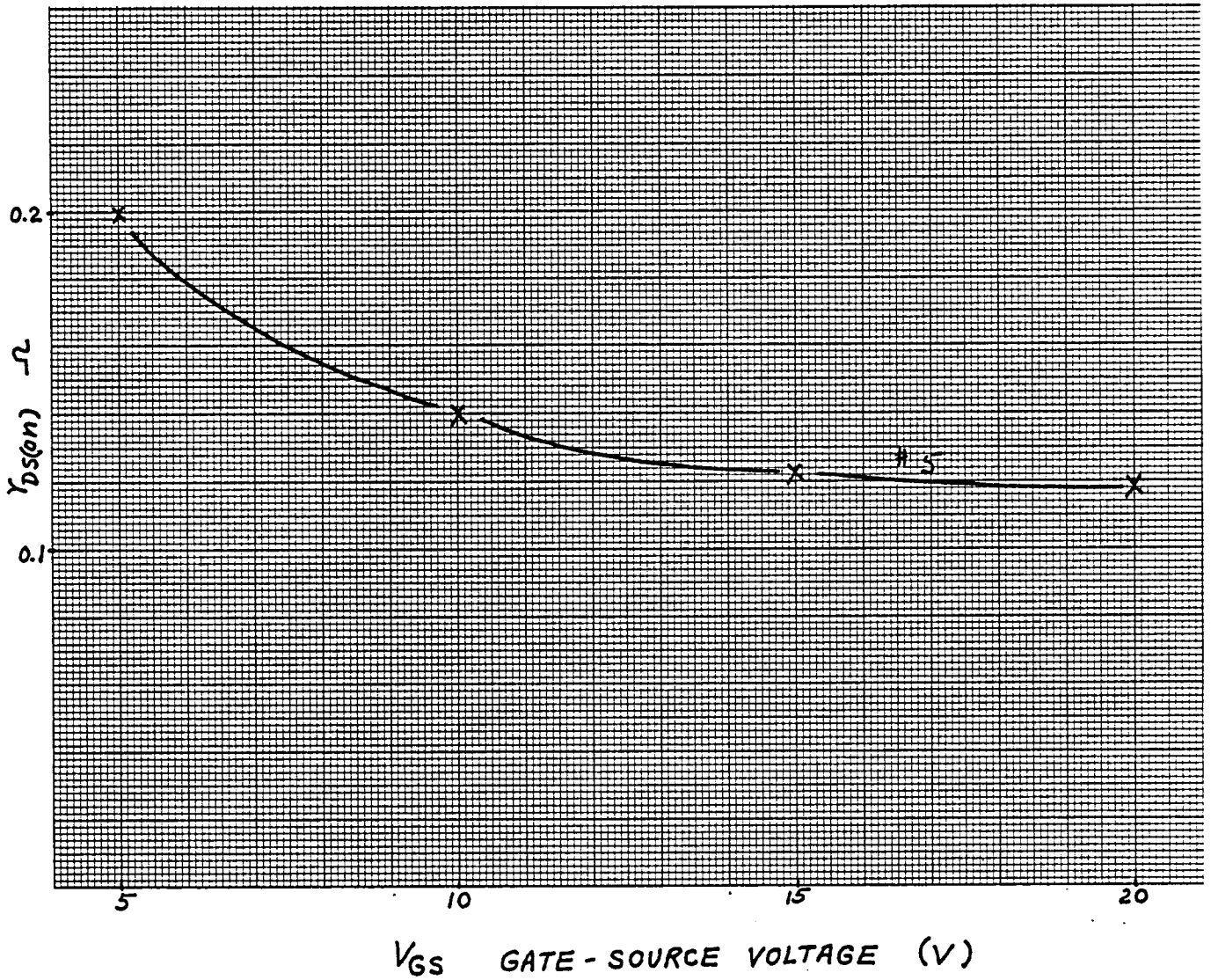


Figure (66) VNS 'ON' Resistance vs
Gate-Source Voltage

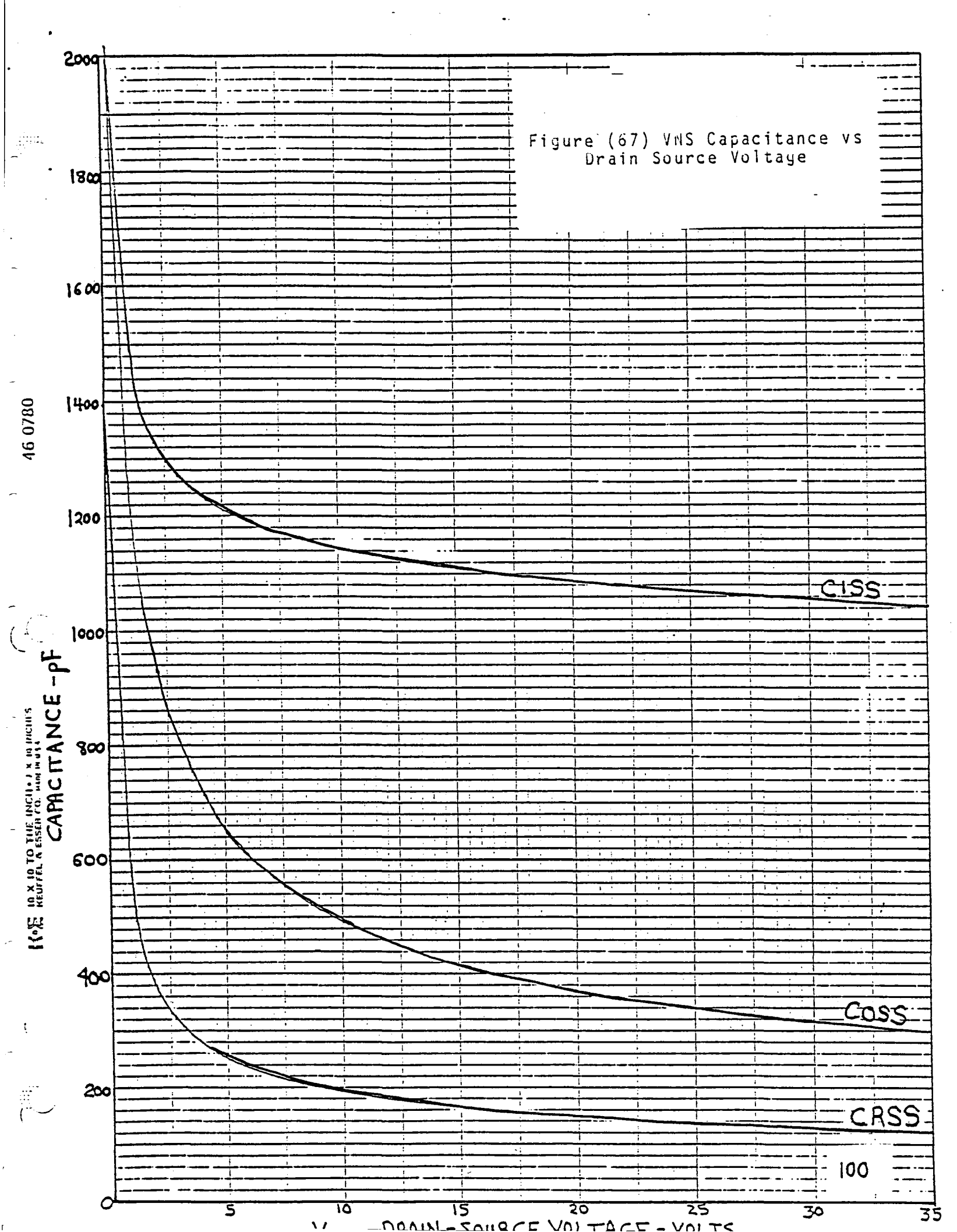
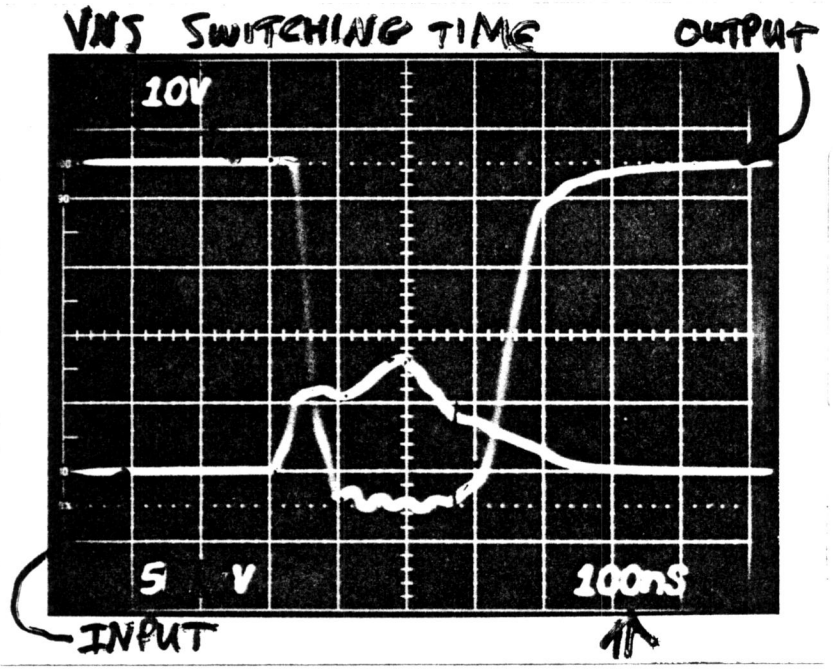


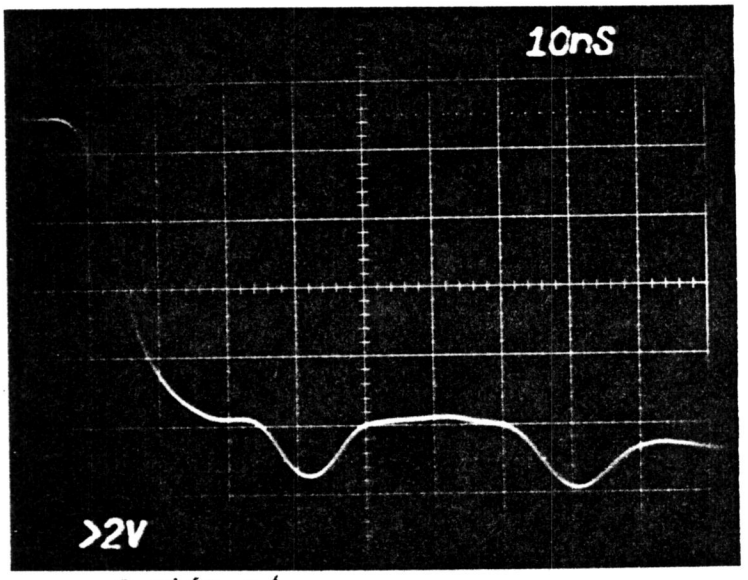
Figure (67) VNS Capacitance vs Drain Source Voltage
CAPACITANCE - pF
2000
1800
1600
1400
1200
1000
800
600
400
200
0
5
10
15
20
25
30
35
CISS
COSS
CRSS
100
46 0780



Input: Vert. 5V/div.
Hori. 100ns/div.

Output: Vert. 10V/div.
Hori. 100ns/div.

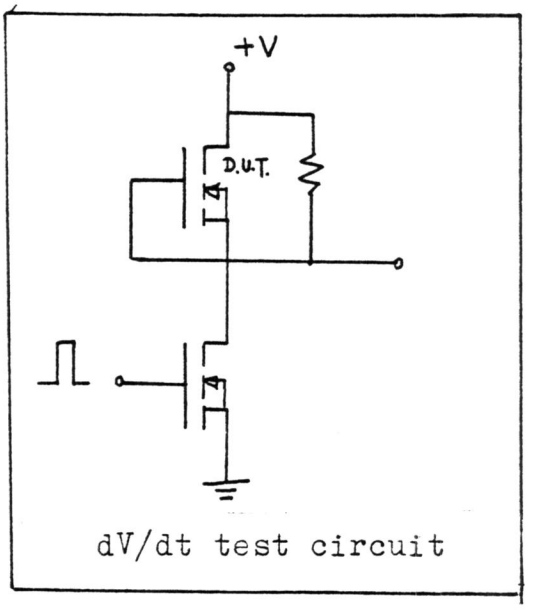
Fig.(68) VNS Switching waveform



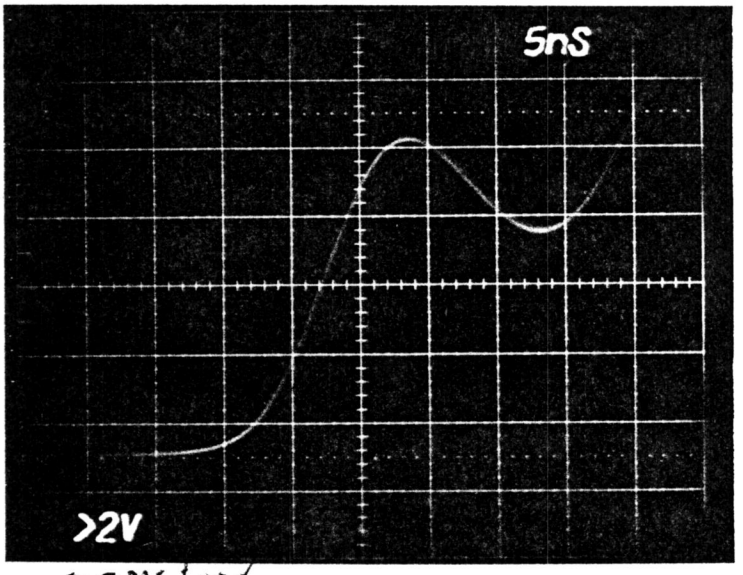
>20V/DIV

Vert. 20 V/div.

Hori. 10ns/div.



dV/dt test circuit

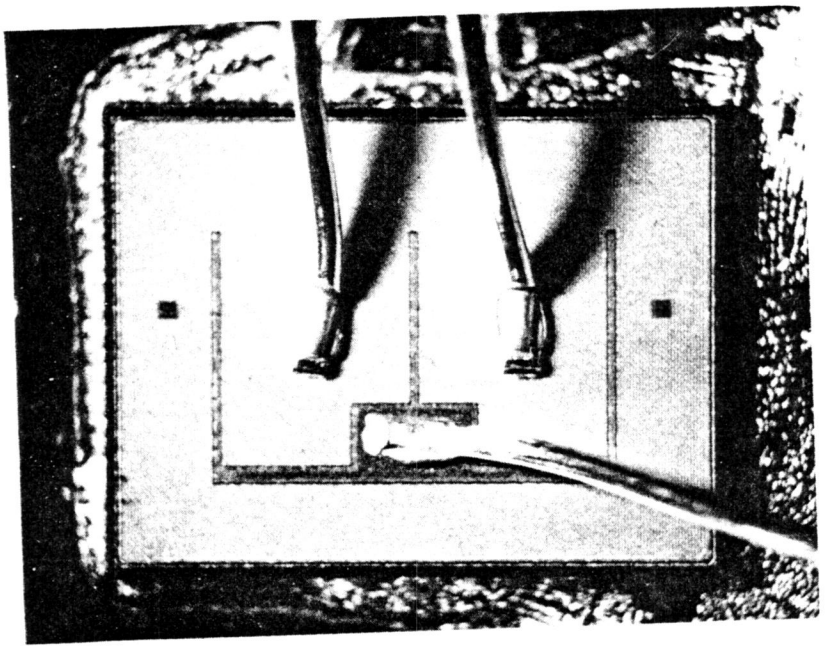


>20V/DIV

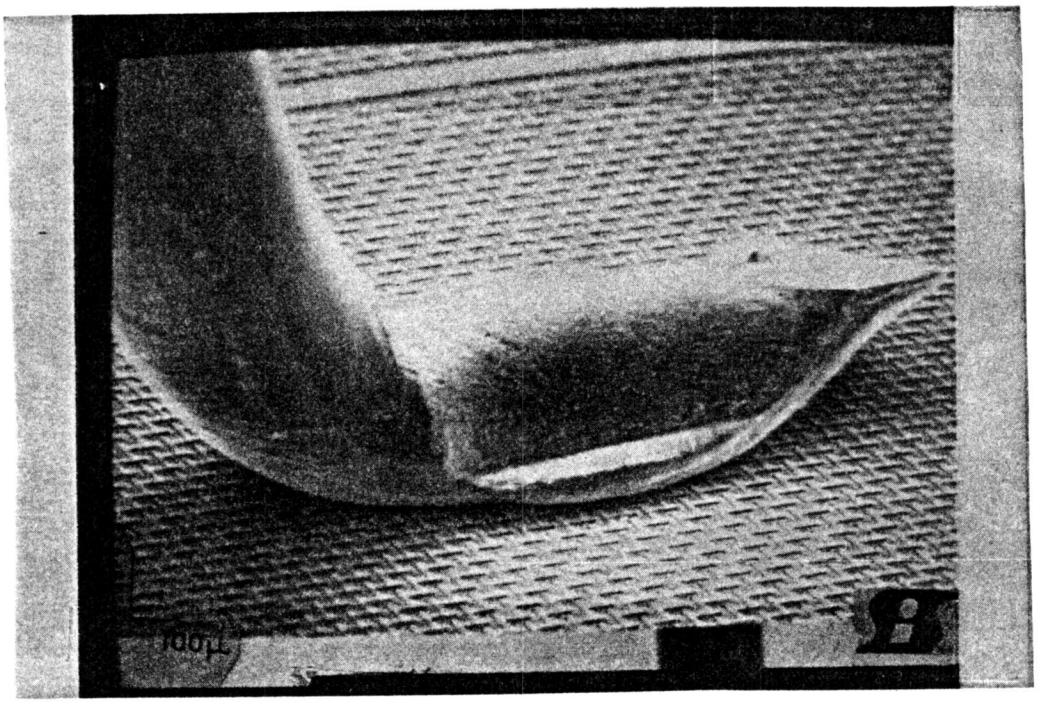
Vert. 20V/div.

Hori. 5ns/div.

Fig.(68A) VNS dV/dt Waveform Result: dV/dt > 7.5V/ns



(a)
One VNS device packaged in TO-3 using
10-mil Wire (Othodyne Electronics Model 20)



(b)
SEM of VNS packaged in TO-3
Figure (69)

6.0 CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

By use of a test pattern (VNTK), a new layout and basic processing technique to fabricate poly-gate VMOS power FETs has been explored and found to be highly feasible. An experimental device (VNS) was designed; and the initial results confirmed that the new device is capable of low 'ON' resistance, high current, as well as high voltage and fast switching speeds.

'ON' resistance: The poly-gate K-structure based on the 'three-layer-conduction' concept, has resulted in extremely high packing density. This high packing density, in turn gives low 'ON' resistance. The layout concept is capable of still lower 'ON' resistance if we are willing to accept higher C_{rss} per unit area.

Current: Because of the high packing density, the new layout gives very high g_m per unit area. This has resulted in high drain current. The new structure not only can deliver high current, but also can conduct the current without having to run into current density problem. This is accomplished by having the source metal covering practically the entire chip surface.

Voltage: Another way to lower the 'ON' resistance is to increase the pn junction breakdown voltage efficiency. The new field-plated groove termination is an effective way to relieve the electric field in the peripheral area. It has been found (by experiment) that the new termination can achieve 450V with close to 80% breakdown efficiency.

Switching Speed: By using the gate bus bar, no appreciable delay has been found with polysilicon gate of moderate sheet resistance (40-60Ω/□). With a pulse generator of 50Ω source impedance, 75 to 100 ns of turn-off time has been achieved. With lower source impedance such as 8Ω, it is possible to achieve t_{off} in about 50 nano seconds. The major trade-off is 'ON' resistance. Therefore depending on market and application, the device can be optimized for either 'ON' resistance or switching speed.

Power Handling Capability: By virtue of its high

packing density the new poly-gate power FETs can handle higher power density than the metal-gate interdigitated-structure VMOS FETs. In fact, it is competing very aggressively with bipolar power transistors in this area. With proper design layout and process, the forward-biased second breakdown we often see in bipolars, is practically non-existent. The device is capable of delivering high current (in 10's of amperes) out to the avalanche breakdown voltage (in 100's of volts) simultaneously. The ON-state D.C. power dissipation of the new device, as it has been developed today, is still about twice that of equivalently-sized bipolar at room temperature. However, since the VMOS FET can switch ten times faster, (with a commutation time in the 10's of nano-second range,) we can use the new FET to switch power in the kilowatt range.

FUTURE WORK:

This development, rather than being an end in itself, opens up a new avenue for further improvement. The suggested future work involves:

1. Increase breakdown voltage to kilovolt range.

2. Understand 2nd-order effects of VMOS power FETs.

3. Develop new packaging technology to take full advantage of the high current that the device can deliver.

ACKNOWLEDGEMENTS

The author wishes to thank Dr. Eng Tsan Gaw for fruitful discussion on termination schemes, C.T. Trieu for non-planar photo – resist technology development, and Dave Mele for testing of finished devices. Encouragement and support by Seigi Tadokoro and John Hulme are also acknowledged.

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APPENDIX A

r_{drift} Equation Formulation

The calculation of the resistance in the drift region was rather complex because of the current spreading effect which was complicated by the surface accumulation layer underneath the V-groove. However, by making some reasonable assumptions, it was found that a simple equation could be formulated which predicted the rdrift and hence the $r_{DS(on)}$ with less than ± 20% error within the range of V_{GS} and V-groove widths that we're interested. The following is a brief derivation:

For low V_{GS}, $r_{DS(on)}$ was dominated by what goes on in $r_{channel}$. When the device was turned on with a relatively high V_{GS}, $r_{channel}$ goes down and r_{drift} becomes important. Under this condition, the epi region underneath the V-groove was heavily accumulated. For a first approximation, we assumed that the region was a constant potential plane (this assumption was found to be valid for the V-groove width of interest i.e., .2 to .4 mil. Beyond this range, the series resistance for this region was appreciable so it could not be ignored.) Again, because the substrate was heavily doped to approximately .01Ω- cm, we assumed that little voltage drop occurred in this region. Therefore, we said that the n- n+ interface was also a constant potential plane. Thus, to calculate an approximate value for the r_{drift} component the problem was simplified to calculating the spreading resistance of a slab of semiconductor material with a multiple 'source' electrodes on one surface and a n electrode covering entirely the other surface. One more simplification was made; the boundary of the spreading resistance 'cone' was at a 45° angle to the plane surface. (See Figure (70))

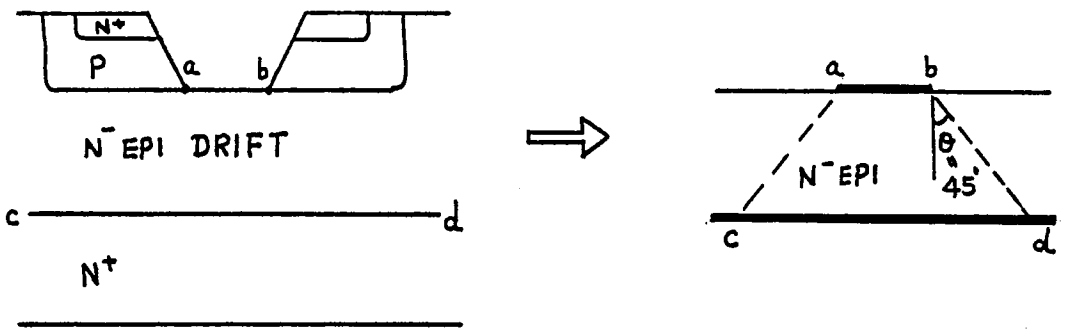


Figure (70) Simplification of Spreading Resistance in drift (epi) region ab and cd are Assumed To Be Equipotential Lines

Therefore, we reduced the r_{drift} calculation to a trapesoidal approximation.

The derivation was then straight forward. We shall do the following two structures:

1. Interdigitated Structure
2. K-Structure (one basic cell)

1.) Interdigitated Structure:

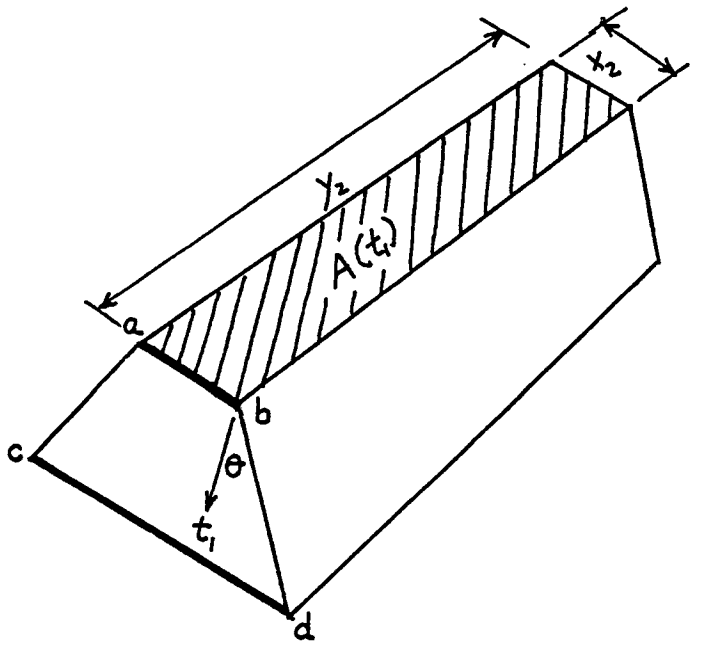


Figure (71) Drift Region of Interdigitated Structure

Cross-sectional area equation:

$$A(t) = (X_2 + 2\tan\theta t_1)\ (Y_2 + 2\tan\theta t_1) \qquad (A)$$

$$d\, r_{drift} = \rho\ \frac{dt_1}{A(t)} \qquad (B)$$

Intergrating:

$$r_{drift} = \rho \int_0^{t_1} \frac{dt_1}{(X_2 + 2\tan\theta t_1)\ (Y_2 + 2\tan\theta t_1)}$$

$$r_{drift} = \left(\frac{\rho}{2 \tan \theta \, (X_2 - Y_2)} \right) \times$$

$$\left(\ln \frac{(2 \tan \theta t_1 + Y_2)}{(2 \tan \theta t_1 + X_2)} - \ln \frac{Y_2}{X_2} \right) \qquad (C)$$

Equation C was general for all angles θ. For the first approximation θ can be assumed to be 45°. Since tan 45° = 1, equation C becomes:

$$r_{drift} = \frac{\rho}{2(X_2 - Y_2)} \left(\ln \frac{2t_1 + Y_2}{2t_1 + X_2} - \ln \frac{Y_2}{X_2} \right) \qquad (D)$$

2.) K-Structure (one basic cell)

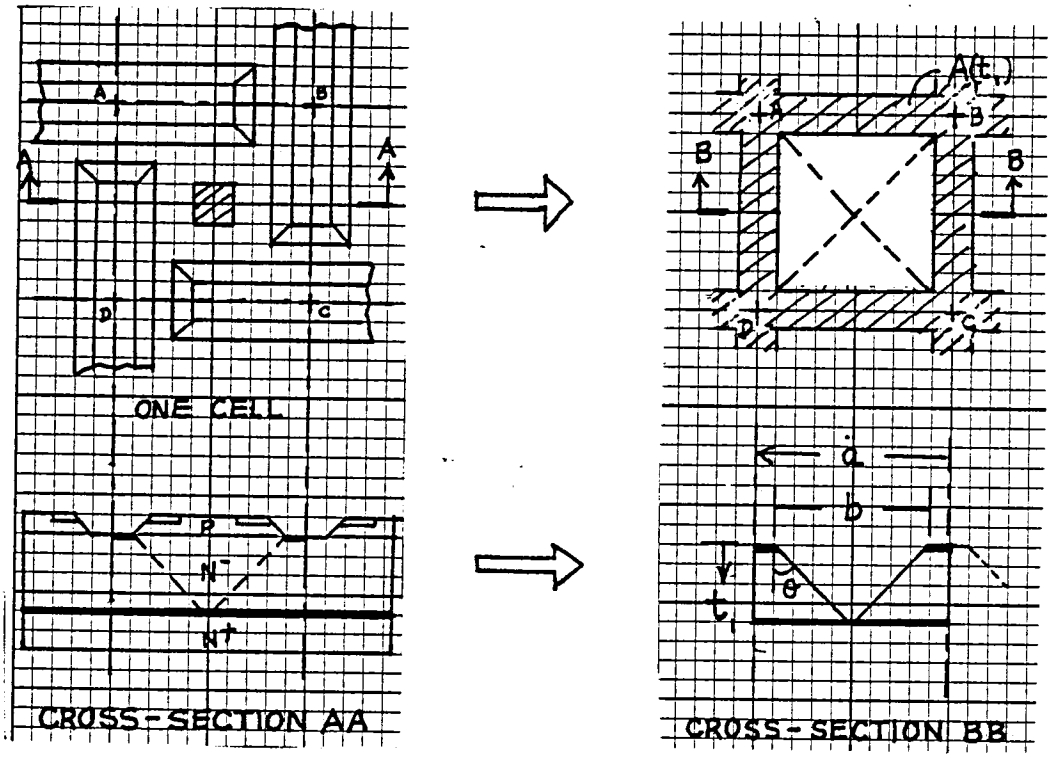


Figure (72) Drift Region of K-Structure (one basic cell)

$$\text{Area} = a^2 - (b - 2\tan\theta t_1)^2$$

$$= (a + b - 2\tan\theta t_1)(a - b + \tan\theta t_1)$$

$$\therefore\ dr_{drift} = \frac{\rho\, dt_1}{(a+b - 2\tan\theta t_1)(a-b + 2\tan\theta t_1)}$$

Integrating from $t_1 = 0$ to $t_1 = t_1$,

$$r_{drift} = \int \left(\frac{1}{(2\tan\theta)(a+b) - (-2\tan\theta)(a-b)}\right) \times$$

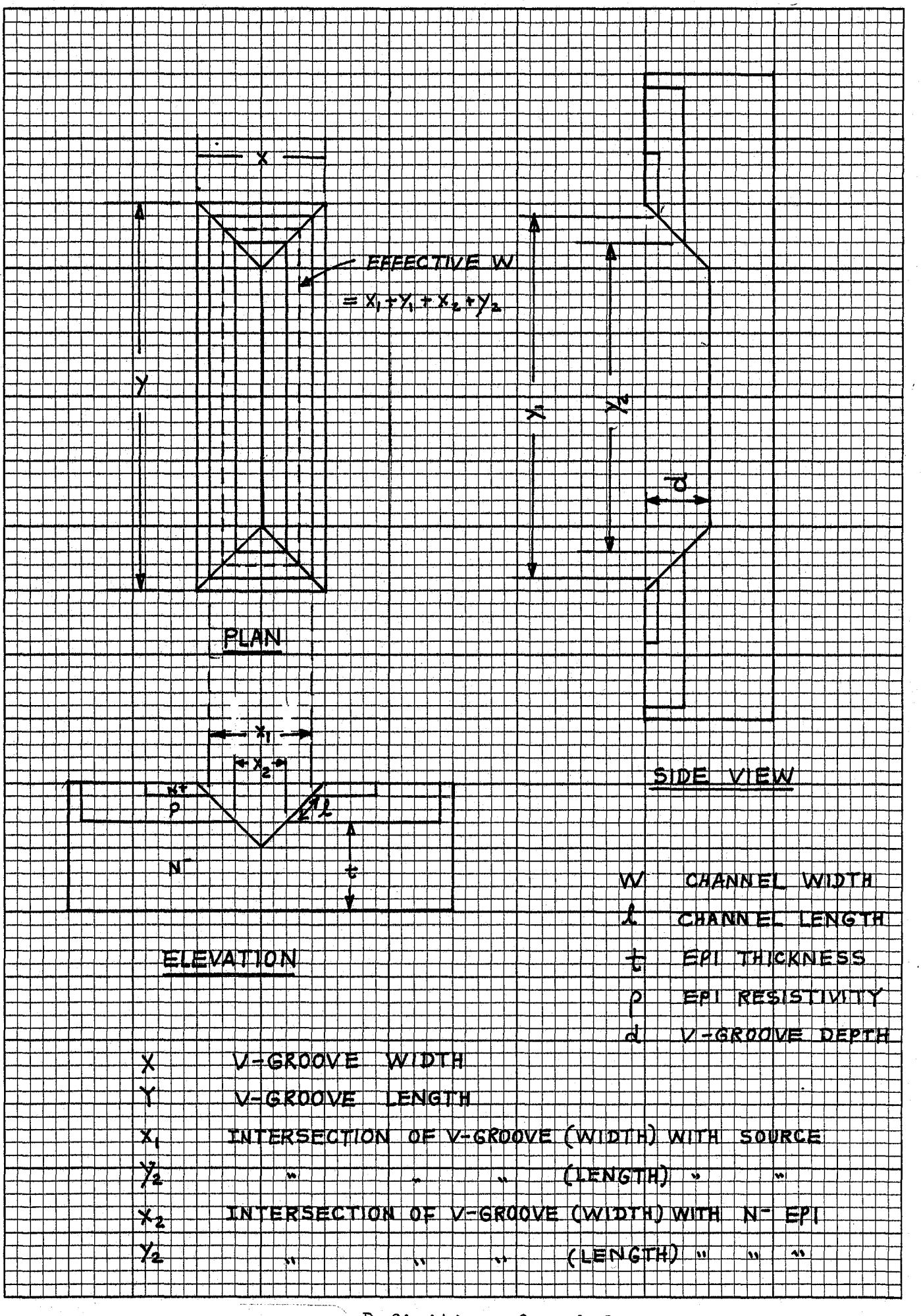
$$\left(\ln \frac{2\tan\theta t_1 + (a-b)}{2\tan\theta t_1 + (a+b)} - \ln \frac{(a-b)}{(a+b)}\right)$$

for $\theta = 45°$
$\tan\theta = 1$

$$\therefore\ r_{drift} = \frac{\rho}{4a}\left(\ln \frac{2t_1+a-b}{2t_1+a+b} - \ln \frac{a-b}{a+b}\right)$$

if $t_1 = b/2$

$$r_{drift} = \frac{\rho}{4a}\left(-\ln \frac{a-b}{a+b}\right)$$



W CHANNEL WIDTH

l CHANNEL LENGTH

t EPI THICKNESS

ρ EPI RESISTIVITY

d V-GROOVE DEPTH

X V-GROOVE WIDTH

Y V-GROOVE LENGTH

X_1 INTERSECTION OF V-GROOVE (WIDTH) WITH SOURCE

Y_2 " " " (LENGTH) " "

X_2 INTERSECTION OF V-GROOVE (WIDTH) WITH N⁻ EPI

Y_2 " " " (LENGTH) " " "

APPENDIX B

Formulation of $I_{DS(sat)}$ Equation:

With the application of drain voltage, the depletion layer between the body and the drain extended primarily into the drift region. Therefore, we assumed that the substrate charge (Q_B) remained fairly constant. Using the simplified version of the standard MOS equation, we get

$$I_{DS} = \mu\, Co \frac{W}{\ell} \left((V_{GS} - V_T) - \frac{V_{DS}}{2} \right) V_{DS} \qquad (E)$$

Because the channel length (ℓ) was short (approximately 2μ), scattering limited velocity of the channel carriers was reached at some moderate drain voltage ($V_{DS(crit)}$) or,

$$V_{DS} = V_{DS(crit)}$$

$$\frac{V_{DS(crit)}}{\ell} = E_{crit}$$

$$\mu\, E_{crit} = \gamma' \text{ sat (which is scattering limited velocity of carriers)}$$

Equation (E) becomes:

$$I_{DS(sat)} = C_o\, W\, \gamma' \text{ sat} \left(V_{GS} - \left(V_T + \frac{V_{DS(crit)}}{2} \right) \right) \qquad (F)$$