NASA CR-132694

FINAL REPORT

DEVELOPMENT OF AN INDIUM ANTIMONIDE CHARGE-COUPLED DEVICE (InSb CCD) FOR INFRARED IMAGER APPLICATIONS

Contract No. NAS1-13163

For - National Aeronautics and Space Administration
Langley Research Center
Hampton, Virginia

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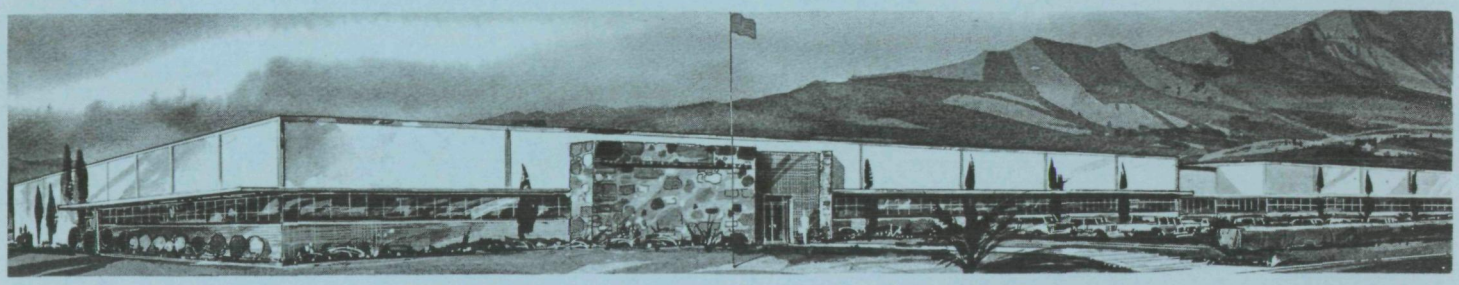

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1 May 1975

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FOREWORD

This final technical report was prepared by the Santa Barbara Research Center under Contract No. NAS1-13163. The work was sponsored by the National Aeronautics and Space Administration Langley Research Center. The Technical Representative for NASA was Herbert D. Hendricks. The technical effort was performed during the period 8 May 1974 to 8 April 1975.

The author acknowledges major technical contributions made to this study by Robert E. Eck, Mildred Dugger, Richard L. Nielsen, James D. Phillips, David M. Randall, Edgar E. Russell, and James B. Scorso.

Section 1
INTRODUCTION

The objective of this program was to continue development of indium antimonide charge-coupled devices (InSb CCDs) and charge-coupled infrared imaging devices (CCIRIDs) fabricated in this semiconductor material. The long-range objective of this effort is to develop a new concept in the 1- to 5-μm infrared imaging sensors utilizing charge transfer techniques. These infrared imaging devices are intended for use in future systems for remote sensing of the earth (from spacecraft and/or aircraft) and other objects in the solar system, for example, outer planet exploration. Development of such a technology would lead to the fabrication of 1- to 5-μm solid-state imaging devices that would allow significant reductions in sensor power and weight. In addition, improved performance could be obtained if the arrays are fabricated to use time delay and integration (TDI) of the infrared signals on the focal plane. The possibility of achieving TDI in real time, within the imaging device itself, is an important feature of the technology under development and could lower future sensor/spacecraft signal processing complexity.

The development of InSb CCDs began with a previous contract (NAS1-12087), Charge-Coupled Infrared Imaging Device Feasibility Study, in 1973. During that contract, the feasibility of an InSb imaging device based on the CCD principle was established by means of InSb MIS device fabrication and evaluation and theoretical calculations based on the experimental results.[1] Also during that contract a mask set was designed for fabrication of four-bit InSb CCDs and other test devices (designated as the 8580 mask). Fabrication trials with this mask set were performed which indicated that the dimensional

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[1] Charge-Coupled Infrared Imaging Device (CCIRID) Feasibility Study, Final Report, NASA CR-132383, Contract No. NAS1-12087, December 1973.

and multilayer requirements of the CCD devices could be achieved with InSb, although operating devices were not obtained before the end of the program.

The present program continued the work begun in the Feasibility Study with particular emphasis on the development of a successful InSb CCD processing procedure and demonstration of charge transfer in such a device. The principal accomplishments of the project were as follows:

1. A process technology for fabricating the required multilayer MIS structure on InSb to achieve a CCD device has been demonstrated. InSb CCD structures with up to six levels (three metallizations and three insulator layers) have been produced with this new process capability.
2. Control of the insulator-InSb interface properties has been improved to yield increased uniformity and repeatability of threshold voltages and storage times compared to the previous program. MOSFETs fabricated in InSb have shown field-effect mobilities comparable to silicon MOS devices, so that surface charge transit times from gate to gate in an InSb CCD will be equivalent to a silicon CCD of the same geometry.
3. Subsequent to the achievement of items 1 and 2 above, charge transfer in an InSb CCD was demonstrated with the four-bit, overlapping gate device on the 8580 mask. Several devices have been operated as analog shift registers with signal voltages applied to the input diffusion and appropriately delayed signals observed at the device output.
4. A new mask set was designed and procured for the fabrication of a developmental InSb imaging line sensor (designated the 8582 mask design), and devices have been fabricated.
5. Analysis of projected device performance and an exemplary earth surveillance sensor utilizing InSb CCDs in a TDI mode has been made which shows the potential utility of these indium antimonide charge transfer devices.

This report is organized as follows. Section 2 describes the device design on the two experimental mask sets (8580 and 8582), and the bounds on present InSb processing that led to the design philosophy of these devices. As will be shown in that section, the 8580 overlapping-gate device uses gate lengths and other dimensions larger than those found in typical silicon CCDs; the combination of dimensions, tolerances, and multilayer requirements of

the mask set were, however, heretofore unproven on InSb, thereby motivating this conservative first mask design. The subsequent 8582 design incorporates dimensions more consistent with normal silicon practice.

The development of the device fabrication technology is described in Section 3. As the program progressed, this aspect of the development emerged as that most crucial to the success of the project, and as a consequence, more than one-half of the total effort under this contract was ultimately devoted to the solution of the various structural and processing problems encountered. Accordingly, the results of the device fabrication effort are discussed in some detail in Section 3.

Section 4 describes the results of measurements on the first InSb CCDs and related test devices. InSb MOSFETs and partial CCD structures were investigated to determine threshold voltages, field-effect mobility, and other characteristics important to CCD operation. The delineation of a CCD channel by a field electrode was investigated and a single transfer of charge with a dual gate-plus-diode structure was observed.

The results of tests to date are presented on full shift register operation of the 8580 InSb CCDs. The transfer efficiency observed on these devices is approximately 85% to 90% per transfer at a 5-kHz clock frequency. This low efficiency is believed to be due in part to the excessively long gates on the 8580 device and the effect of limited potential well depths that can be formed on the moderately-doped (10^{15} cm^{-3}) substrates used. Both of these deficiencies can and will be improved with the shorter-gate 8582 design and the use of lower impurity concentration material in future fabrication lots. Calculations indicate that, with the same interface conditions, decreasing the gate length to 1 mil (25 μm) as on the 8582 device is anticipated to increase the efficiency to 97% per transfer, with better than 99% projected with further reduction in gate length. A preliminary analysis of InSb CCD transfer efficiency is given in Section 5.

Section 6 gives an analysis of projected device performance, and presents a 3.6- to 4.1-μm earth remote-sensing application as a vehicle to demonstrate the potential usefulness of the device. The principle and advantages of TDI are also discussed in this section.

Finally, Section 7 gives conclusions drawn from the contract effort.

The successful demonstration of charge-coupling in InSb represents an important milestone in this development, although considerable improvement in device design and performance is needed before the devices can be utilized in system applications. With continued development, InSb CCDs will provide an optimal solution to several types of 1- to 5-μm detection problems, particularly where high signal-to-noise ratios (SNRs), maximum array uniformity, and low weight and power per signal channel are required — all typical requirements for NASA payloads.

Section 2
InSb CCD DESIGN

InSb processing technology is relatively mature when compared to that of other narrow bandgap semiconductors; however, several limitations do exist related to CCD fabrication which affected the design of both the 8580 and 8582 masks. It will be helpful to summarize three of these prior to discussing the actual designs.

DIFFUSIONS

Diffusion and ion-implantation technology is limited relative to the state of the art in silicon. There are no overriding technical reasons for this; simply, infrared detector requirements have been largely satisfied over the past few years by one particular diffusion process, and no need has arisen to develop others. This diffusion process consists of a p^+ cadmium diffusion into n-type InSb, which produces a low-leakage diode (when the surface is properly stabilized) suitable for photodiodes and other purposes. The conventional process makes use of a diffusion over the full surface of the wafer, followed by a photolithographic step to form "mesa" diode structures. Fully planar diodes (where the wafer is selectively masked during diffusion) have also been fabricated at SBRC, but yield is appreciably lower than with the mesa diodes and leakage is higher. P^+-n junctions have also been formed by ion implantation at SBRC and Hughes Research Laboratories, Malibu, on previous contracts, but leakage currents are again higher than on those produced by the mesa process. Neither n-on-p nor n^+-n diffusions or implantations have been developed on InSb.

Since a CCD device requires the lowest possible leakage in the input and output diffusions, it was concluded that the standard p^+-n diffused mesa diode process would be used in the fabrication lots in this program. The

mesa etch time was shortened to decrease the mesa height to the minimum value without increasing leakage current. The resulting mesa height is about 1 μm.

CHANNEL STOP

The present unavailability of an n^+-n process placed a second limit on the InSb CCD design, namely this means could not be used to form a channel stop (diffusion) as typically done in silicon CCDs. To confine the charge to the channel region, it was elected on both the 8580 and 8582 designs to use a Channel Stop Metallization (CSM). The CSM is a large buried gate deposited on top of the gate insulator (thin oxide) and which covers the device surface except in the CCD channel region. The CSM is in turn insulated with a thick oxide which supports the bonding pads for the CCD gates.

By appropriately dc-biasing the CSM with respect to substrate, the surface potential in the region surrounding the channel may be independently controlled; this surface potential should be at all times less than the surface potential(s) in the channel so that the channel does not spill charge. The CSM serves a secondary function in controlling the reverse currents of both input and output diodes. The CSM bias affects both the breakdown and leakage characteristics of the in/out junctions in accordance with gate-controlled diode theory.

Although a stepped oxide can also create the required surface potential difference between the channel and outlying areas, the ratio of surface potentials is fixed dependent on the thickness ratio of the oxide step. It was concluded that the addition of the CSM was worthwhile to obtain maximum flexibility at this stage of development. Using the CSM, for example, possible spurious effects in the bonding and the clock line regions can be minimized.

DIMENSIONAL AND MULTILAYER CAPABILITY

Prior to this and the previous contract, the state of the art in InSb infrared devices was the capability to produce photodiode arrays with, normally, one insulator and one metal layer used to form expanded leads to the individual detector elements. Typically, metallization line widths of the expanded leads on these conventional arrays are no less than 2 mils. Further, the leads on these detector arrays are not required to cross other metallizations or steps except the steps of the mesa edges, which on the photodiode structures are covered with a thick (>1 μm) insulator rather than the thin oxide (<0.4 μm) encountered in the CCD structure. A considerable advance in technology was required to produce the multilayer CCD device. For example, there are six metal and insulator layers on the four-phase InSb CCD structure, to be discussed in more detail in Section 3. Typical dimensions required in CCD devices are in the submilli-inch range.

8580 FOUR-PHASE CCD

The 8580 mask set was used to process the CCD devices evaluated during this contract. This mask set produces dice, each containing: a MIS capacitor, a closed-geometry MOSFET (W/L = 30), a three-phase, four-bit CCD, and a four-phase, overlapping-gate, four-bit CCD. The latter device has been successfully fabricated and operated as a shift register.

The four-phase CCD is shown in Figure 2-1. Because of the uncertainty in line widths and device complexity that could be achieved, as discussed above, the dimensions of this first device were layed out conservatively, with a 2-mil minimum metallization width in the gate region. The buried gates are 2.5 mils long and the surface gates are 2.0 mils long, with a nominal overlap of 0.25 mil on each edge. The register has a channel 37 mils long by 8 mils wide, with an input and output diffusion at either end of the channel. The channel is defined by the CSM, which appears as the large rectangle in Figure 2-1.

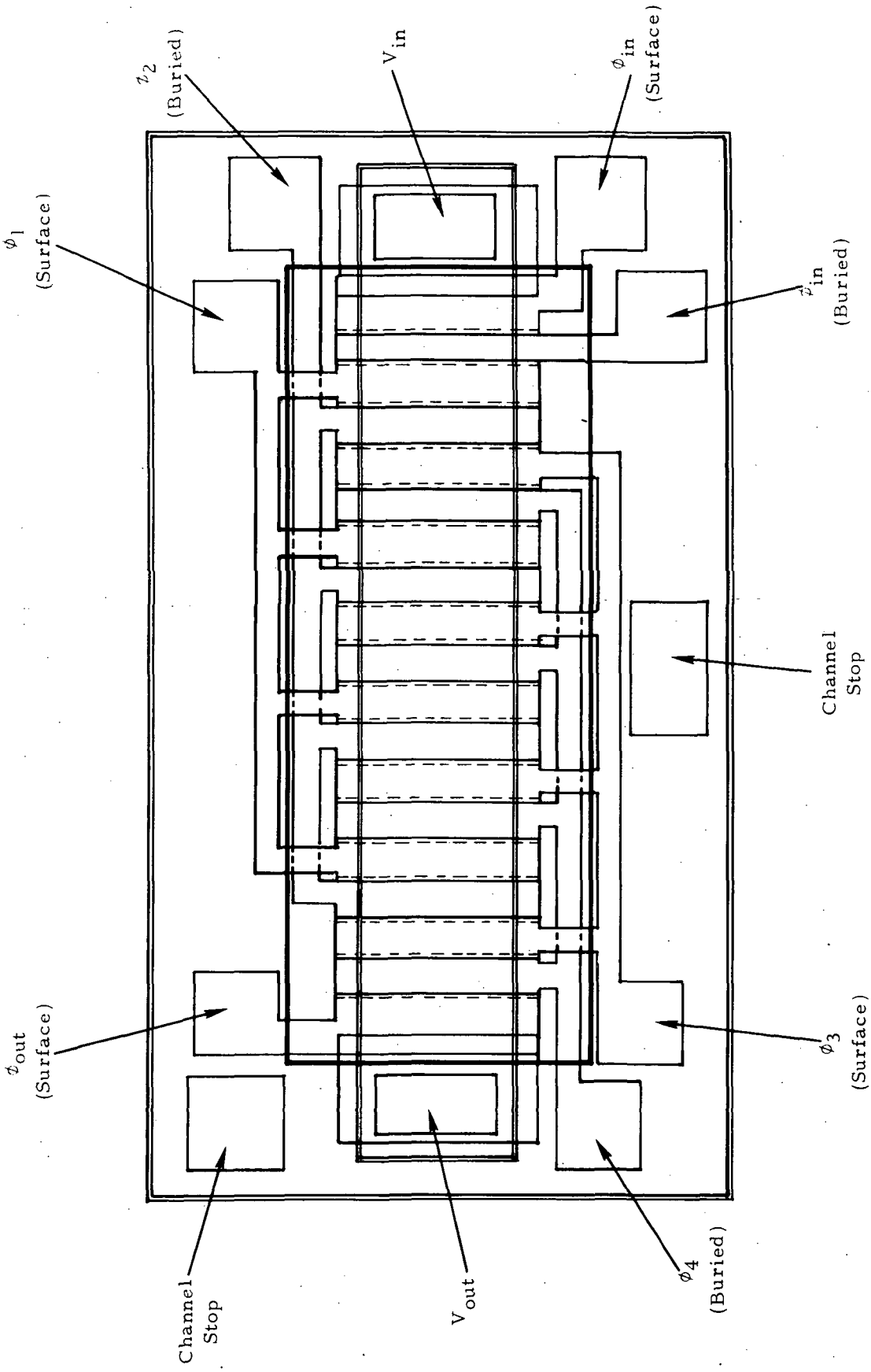


Figure 2-1. 8580 Four-Phase, Four-Bit InSb CCD

This device has two input gates, one buried and one surface metal gate, to provide flexibility for various electrical input schemes. An output gate (surface metal) serves to screen the output diffusion from the last clocked gate.

8582 LINEAR IMAGING DEVICE

The 8582 mask, designed midway in the program, contains a four-element linear array of InSb MIS detectors with a nine-bit, overlapping-gate InSb CCD readout register. A layout of this device is shown in Figure 2-2. The 8582 chip is a logical progression from the 8580, with twice the number of bits and most dimensions decreased by a factor of two or more. A comparison of the two mask designs is given in Table 2-1. The bit length on the 8582 was decreased to 4 mils, compared to 8 mils on the 8580, to improve device transfer efficiency. The smallest critical metallization line width was decreased to 0.5 mil. Four MIS detectors, 4 mils square, are positioned adjacent to the register along with a transfer gate for inputting the integrated detector charge into the CCD and a detector common bus. An input diode and a pair of input gates were also included to facilitate testing of the device with electrical as well as optical input.

Because of the position of the optical sensing elements, all clock lines were routed on the opposite side of the register. This creates the need for multiple crossovers of the four-phase clock lines as shown in Figure 2-2. Ultimately, packing density requirements on InSb CCD focal plane devices will be quite stringent; it was decided, therefore, to compress the line routing, crossovers, and vias (contact windows) in this region to approach anticipated future dimensional requirements, rather than fanning out the clock lines over a larger area which would have sufficed for this experimental device. This compression would offer a better test of the dimensional capabilities of the process during its development, and speed the realization of prototype devices later in the development cycle.

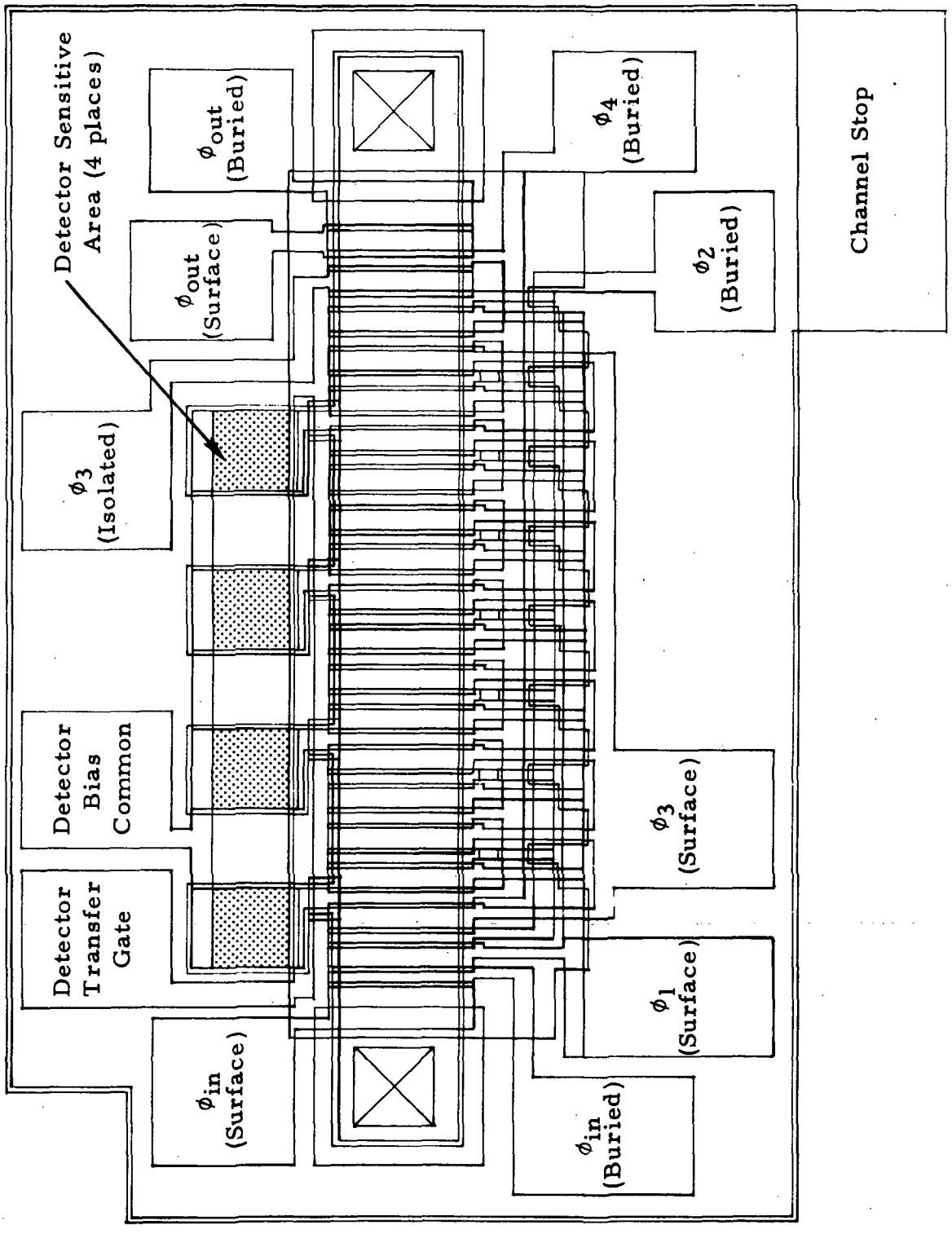


Figure 2-2. 8582 Linear Imager, a Nine-Bit CCD with Four MOS Detectors

Table 2-1. Summary of 8580 and 8582 Designs, Four-Phase InSb CCDs (all dimensions in milli-inches)

	8580	8582
Number of Bits	4	9
Number of Detectors	0	4
Detector Dimensions	--	4.0 × 4.0
Number of Mask Layers	7	8
Number of Insulator Layers	3	3
Number of Metallizations	3	4
Bit Length	8.0	4.0
Effective Gate Lengths		
Buried	2.5	1.0
Surface	1.5	1.0
Channel Width	8.0	6.0
Diode Dimensions	7.0 × 10.0	8.0 × 8.0
Smallest Critical Metallization Line Width	1.0	0.5
Smallest Critical Spacing	1.0	0.25
Smallest Via Dimension	4.0 × 4.0	0.4 × 0.8
Smallest Critical Dimension	0.25	0.25

The use of four-phase clocking on these devices is, like the CSM, intended to provide maximum flexibility. In an overlapping-gate structure, either a stepped oxide (two-phase), implanted barrier (two-phase), or four-phase clocking may be used to provide the necessary directionality. The 8580 and 8582 devices are fabricated with a stepped oxide structure and can be operated in a two-phase mode; however, charge capacity and performance in this mode are critically dependent on control of threshold voltages of the surface and buried gates, hence insulator thickness and other parameters. It was concluded that the additional layout complexity for a four-phase design would be worthwhile on these experimental masks to permit the maximum

freedom in clocking the device. Ultimately, however, as knowledge and control of thresholds improves and insulator deposition techniques are refined, two-phase, stepped-oxide InSb CCDs would be desirable. Thus the routing of the clock lines would be simplified compared to that needed on the 8582 device.

The 8582 mask also contains a two-bit CCD with the same gate lengths (1 mil) as the larger device, but without detectors, two MOSFETs of different geometries (W/L = 36 and 96), and two MIS capacitors, the latter devices for process evaluation.

Section 3
DEVICE FABRICATION

8580 CCD

Figure 3-1 shows two cross sections of the 8580 four-phase CCD: one perpendicular and one parallel to the channel. Three insulators and three metallizations are required in the structure, counting the basic gate insulator and channel stop metal layers, as identified in the figure.

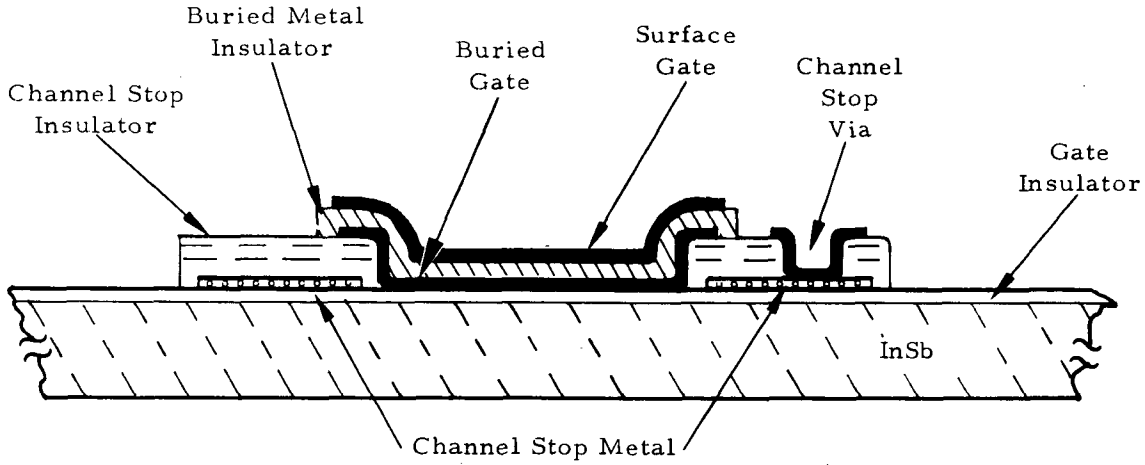
Operating 8580 four-phase CCDs with the structure shown in Figure 3-1 were successfully produced utilizing features of a metallization and delineation process previously developed by SBRC for the fabrication of InSb photovoltaic detector arrays. This process makes use of a titanium-gold (Ti-Au) metallization system, silicon oxide (SiO_x) for the dielectric layers, and a photolithographic technique that defines the Ti-Au metallization patterns without deleterious etching effects. Both the metals and SiO_x are thermally deposited, thus reducing the presence of stray charge in the evaporant stream and eliminating the possibility of X-ray flux, both of which can be troublesome in electron-beam deposition of materials.

Use of SiO_x as a gate insulator on InSb was evaluated in a company-funded project in early 1974. It was determined that the required storage times (>50 msec) and C-V characteristics could be achieved with this material; moreover, repeatability of interface conditions from wafer to wafer was found to be superior with the SiO_x insulator, as compared to results with Al_2O_3.

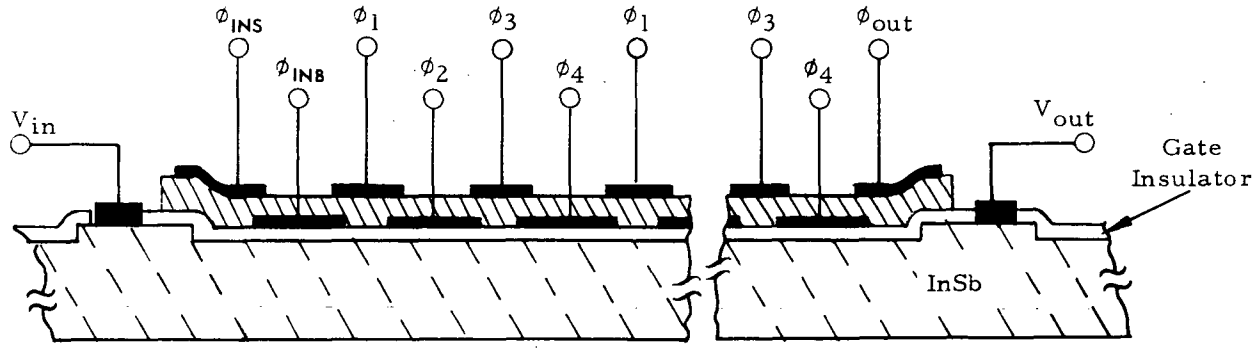
The processing sequence used for the 8580 overlapping gate device is as follows:

The wafer is first diffused as discussed in the previous section, forming a shallow p^+ layer over the surface of the wafer. Next, the surface of the wafer is etched to form the mesa diodes for input/output (mask level 1).

Subsequently, the SiO_x gate insulator is deposited; nominal thickness used has been in the range 1500 Å to 2000 Å. Vias delineated in the gate insulator (mask level 2) over the diodes are then plated through with gold, making contact to the input and output diffusions.



Cross Section Through the Channel



Cross Section Along the Channel

Figure 3-1. Cross Section of InSb Four-Phase CCD

The next step in the process is the formation of the channel stop structure. The channel stop metal is shown in the upper cross section of Figure 3-1; it consists of a thin metal evaporated on the gate insulator, on both sides of the channel in cross section. Thermally-evaporated titanium 200 Å thick is deposited to form the channel stop metallization and delineated (mask

level 3) into its required pattern. This is followed by the deposition of 5000 Å of SiO_x over the CSM to isolate it from the CCD electrodes and to serve as a support for the bonding pads. A mask step (mask level 4) is used to define this channel stop insulator as shown in Figure 3-1, such that it overlaps the CSM. Redundant vias are also formed in the 5000 Å SiO_x during this step for accessing the CSM; one of these is shown in the upper cross section.

The next level in the structure is the buried gate metallization. Titanium is also used for these gates. The thickness of this metal layer is <1000 Å; this has been varied to investigate yield effects. 400 Å of Ti was used on the first successful wafers; this was increased to 700 Å on later lots. A mask step (level 5) defines the ϕ_{INB}, ϕ_2, and ϕ_4 gates in this titanium metallization. This is followed by deposition of the buried metal insulator, another SiO_x dielectric layer. It is defined by another mask step (level 6). The buried metal insulator is ≤3000 Å thick. The devices reported in Section 5, in particular, have a 2200 Å thick buried metal insulator.

The final step in the wafer processing sequence is the deposition and delineation of the surface gate metallization (mask level 7). Gates ϕ_1, ϕ_3, ϕ_{INS}, and ϕ_{out}, are formed in this step. In addition, the bonding pad regions on the thin buried metal layer, along with the channel stop vias, are re-metallized for wirebonding purposes. 1000 Å of Ti-Au was normally used for the surface metallization.

A partial view of a completed 8580 four-phase CCD device is shown in Figure 3-2. This scanning electron microscope (SEM) photomicrograph clearly illustrates the excellent delineation capability that has been achieved on these devices. The top gates visible in the photograph are the 2.0-mil long Ti-Au surface metal gates, which overlap the buried gates by 0.25 mil at each edge. Also visible in the photo are the edges of the channel, defined by the channel stop insulator step, and the mesa diode with its Au contact.

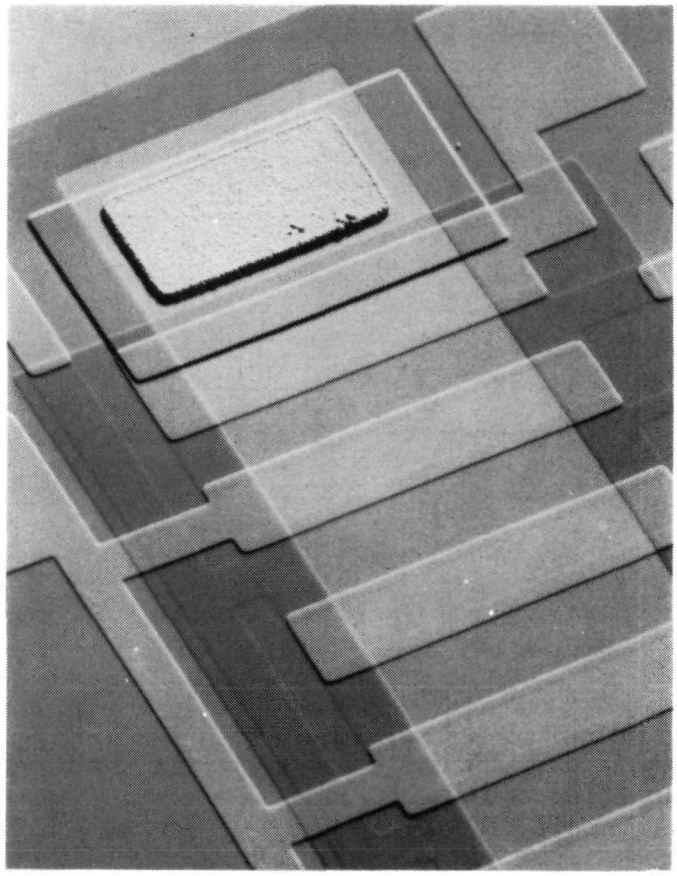


Figure 3-2. 8580 Four-Phase InSb CCD (200× SEM, Backscatter Mode)

8582 LINEAR IMAGING DEVICE

Processing of the 8582 imaging device is generally similar to the 8580 fabrication sequence. One additional photodelineation step (mask level 8) is needed to define the four MIS detector elements (photoelements). The MIS detectors are fabricated using a semitransparent Ti film approximately 50 Å thick deposited on the gate insulator. These semitransparent gates are tied with a common bias bus on the buried metal layer.

A partial view of a completely processed 8582 device is shown in Figure 3-3. The 2× reduction in most dimensions compared to the 8580 device is shown by SEM examination to be compatible with the process capabilities, as evidenced by this and subsequent photographs. The apparent curvature in Figure 3-3 is due to barrel distortion in the SEM CRT. Figure 3-4 shows a

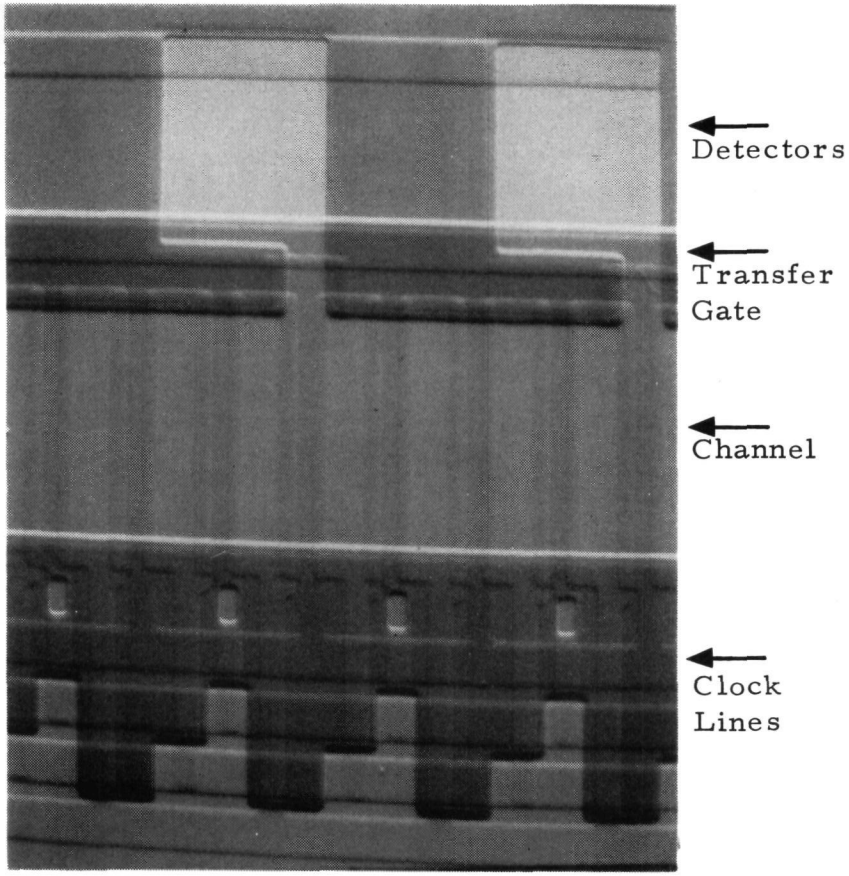


Figure 3-3. Partial View of 8582 InSb Linear Imaging Device (200× SEM, Backscatter Mode)

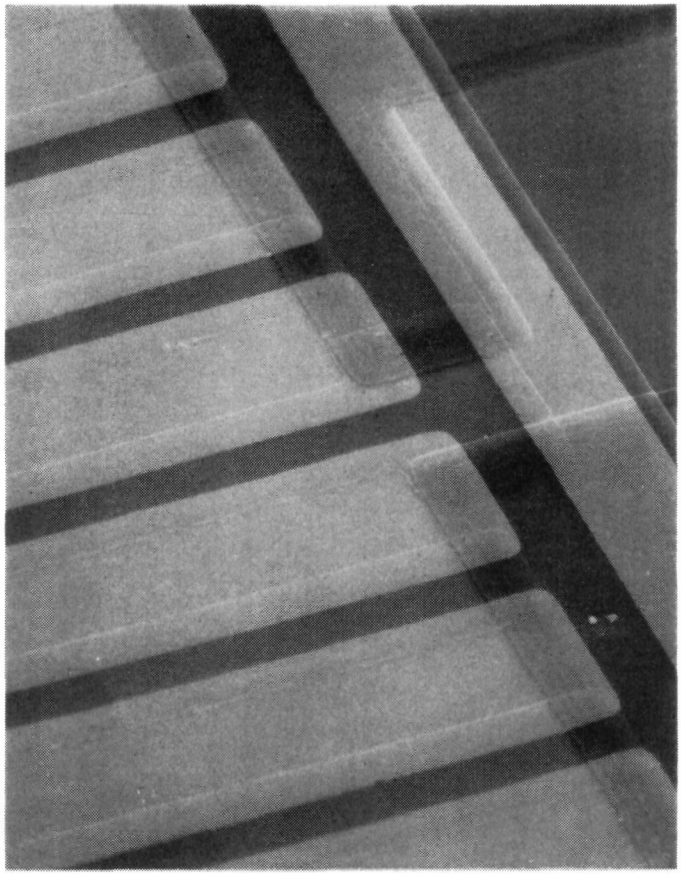


Figure 3-4. 8582 InSb Linear Imaging Device Detail (500× SEM, Secondary Emission Mode)

detail of one side of the channel at 500X. The Ti-Au surface gates, visible in this photomicrograph, are 1.5 mils in length with a 0.25-mil overlap at each edge to produce an effective gate length of 1.0 mil.

STEP COVERAGE AND DIMENSIONAL CAPABILITY

There are two particularly critical areas in the fabrication of the overlapping-gate, four-phase structure associated with the multilevel metal/dielectric process: the formation of electrically continuous gates over the edges of the channel stop structure (i.e., where the gates drop from the thick oxide onto the thin oxide in the channel region); and isolation of the buried and surface metal gates. These problems are interrelated, and in particular the ratio of buried metal insulator thickness to that of the buried metal must be carefully selected. The buried metal must be sufficiently thick to provide good step coverage over the channel stop step. At the same time, it should be thin enough such that it can be covered by the overlying insulator to produce adequate isolation (typically 20 volts, or more) between buried and surface metals, for a reasonable thickness ($\leq$3000 Å) of the insulator layer.

SEM examination has been valuable in assessing the structural characteristics of the wafer lots both during and after completion of processing. Figure 3-5 shows a highly magnified view of a 700 Å thick titanium surface metal gate crossing over the channel stop insulator step (on an 8582 device). By appropriate adjustment of deposition system geometry, good step coverage is achieved on these structures as evidenced in this photograph. Electrical continuity has been confirmed by gate resistance measurements.

A portion of the clock line crossover region of the 8582 device is shown in Figure 3-6. The delineation of the 1.0- and 0.5-mil wide clock lines is seen to be excellent. Figure 3-7 shows an enlarged view of three 0.5-mil wide clock lines in this area which connect individual CCD gates to their respective common clock buses. The via is 0.35 by 0.8 mil.

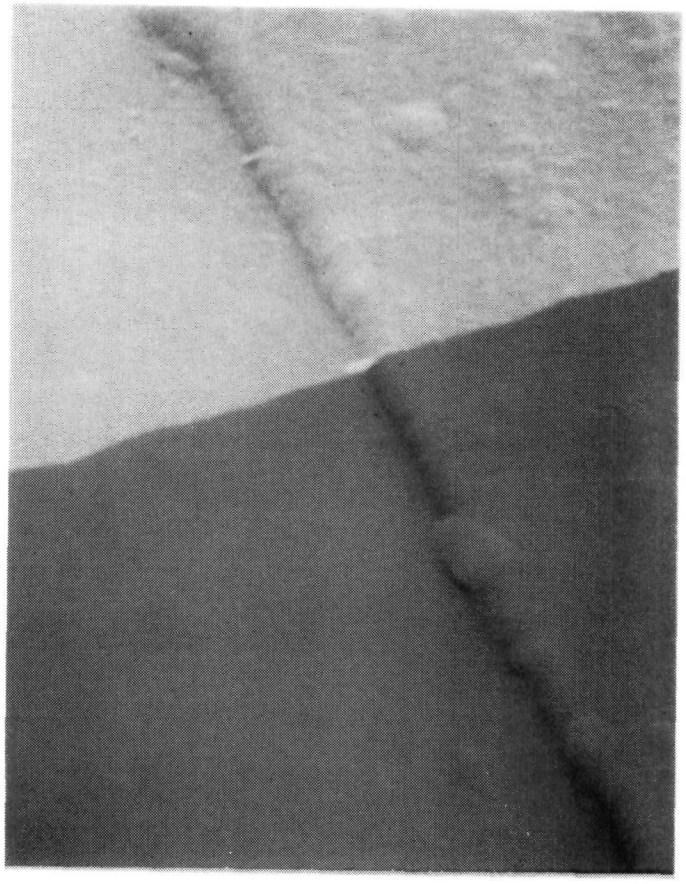


Figure 3-5. Titanium Surface Metal Gate (700 Å) Crossing Over Channel Stop Insulator Step (8582 Device, 10,000× SEM, Secondary Emission Mode)

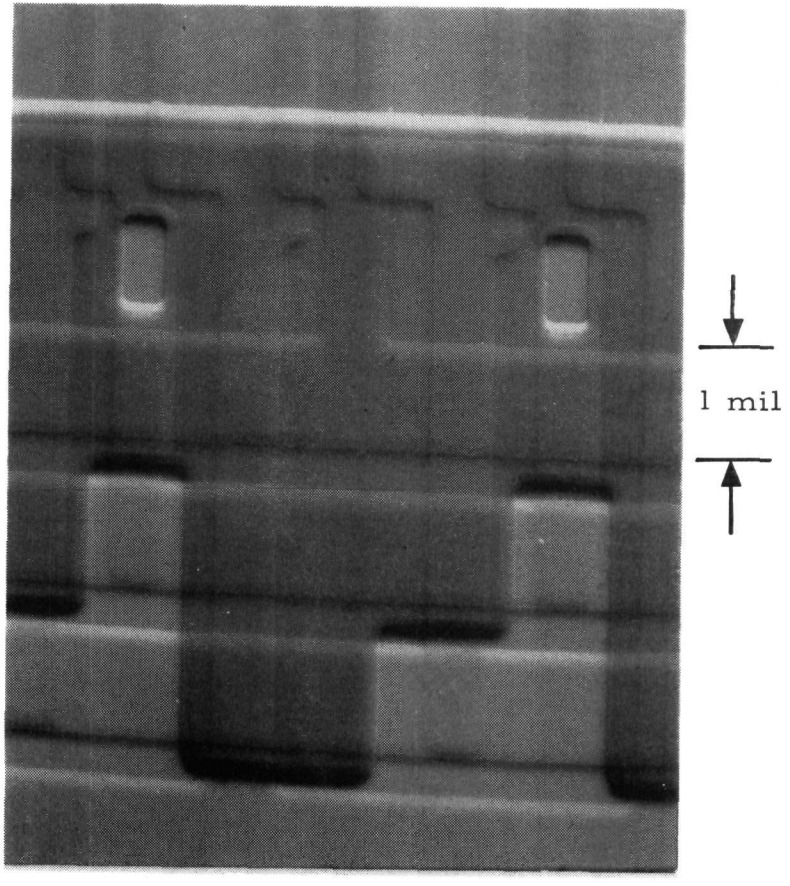


Figure 3-6. Detail of Clock Line Crossovers and Vias (8582 Device, 500× SEM, Backscatter Mode)

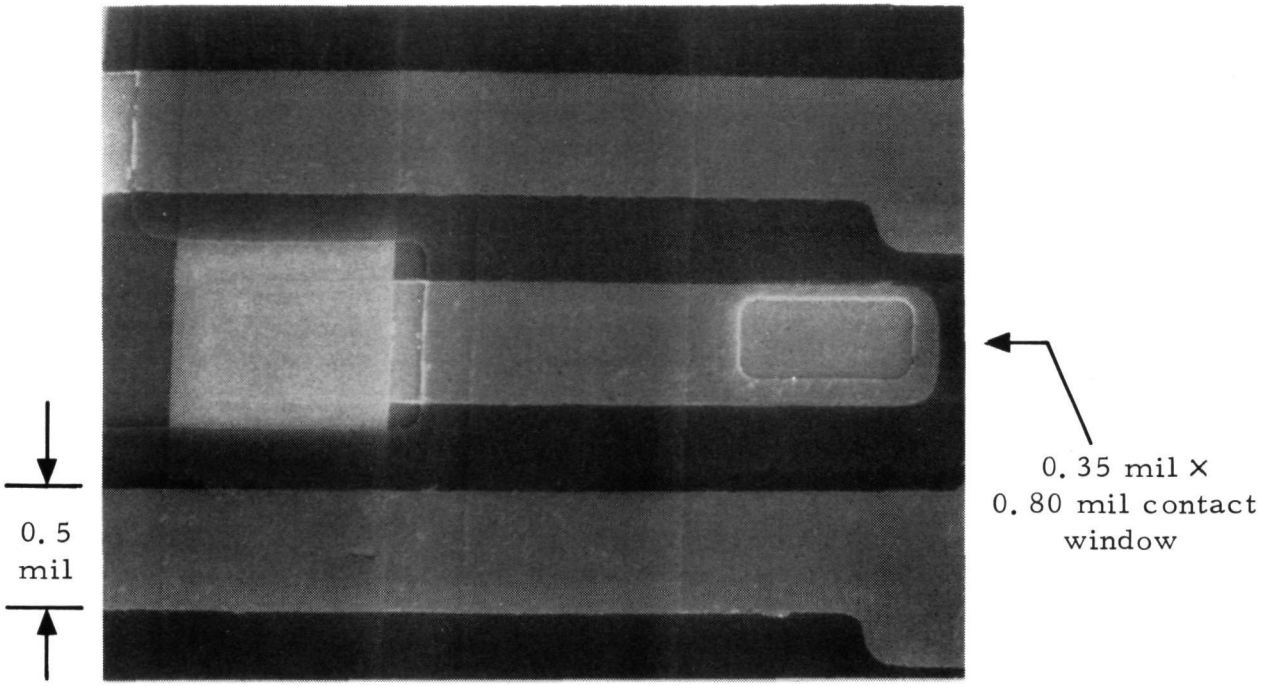


Figure 3-7. Detail of Clock Line Crossovers and Contact Window, 8582 Device (1000× SEM, Secondary Emission Mode)

The first wafers processed with the 8582 mask set indicate that 1-mil gate lengths can readily be achieved by this process. Further, examinations of the structures to date indicate that reducing gate length to 0.5 mil (13 μm) on a future mask would be feasible, with further reduction to 0.3 mil (8 μm) possible. Future mask sets will incorporate various gate lengths in the submilli-inch range to ascertain the ultimate capability of the present process.

Section 4
TEST RESULTS

TEST DEVICES FOR WAFER EVALUATION

Both the 8580 and 8582 masks contain MIS capacitors and MOSFETs as test devices for wafer evaluation. After completion of wafer processing, but prior to dicing of the wafers, these devices are checked on sample dice using a probe test station. The wafer is cooled to 77°K using a styrofoam boat filled with LN_2 and views normal room background radiation (2π FOV). After dicing the wafer, selected dice are packaged in TO-5 cans and wirebonded so that the capacitors and MOSFETs can be evaluated under 77°K, cold-background conditions.

The MIS capacitors are evaluated using capacitance-voltage (C-V) and pulsed capacitance (C-t) measurements. From these data the oxide capacitance (C_o), flatband voltage, storage time, and other parameters are determined. The measurement techniques have been described previously in Reference 1.

A representative C-V curve for a witness MIS capacitor from an 8580 CCD wafer is shown in Figure 4-1. Curve A in this figure is the quasi-equilibrium C-V curve obtained using a low-frequency ramp gate voltage. The high-frequency inversion capacitance is observed at the measurement frequency of 10 kHz (and maintained to frequencies to less than 100 Hz) because of the zero background conditions and the low surface and bulk thermal generation rates displayed by these devices. The plotted data points in Figure 4-1 are for the same device but a square-wave gate waveform in place of the low-frequency ramp was used (see figure inset). When the gate bias clock is off (at resting voltage V_1), the device is in equilibrium and the measured capacitance points (circled data points) coincide with the static C-V curve. When the gate clock switches on to voltage V_2, where $|V_2| > |V_1|$, the capacitor is pulsed to a deep depletion condition and then returns to equilibrium

through thermal generation of minority carriers (holes). The capacitance at the beginning of the C-t transient after switching to V_2 is the deep depletion capacitance; these points are plotted as curves B and C in Figure 4-1 for the clock levels noted in the figure.

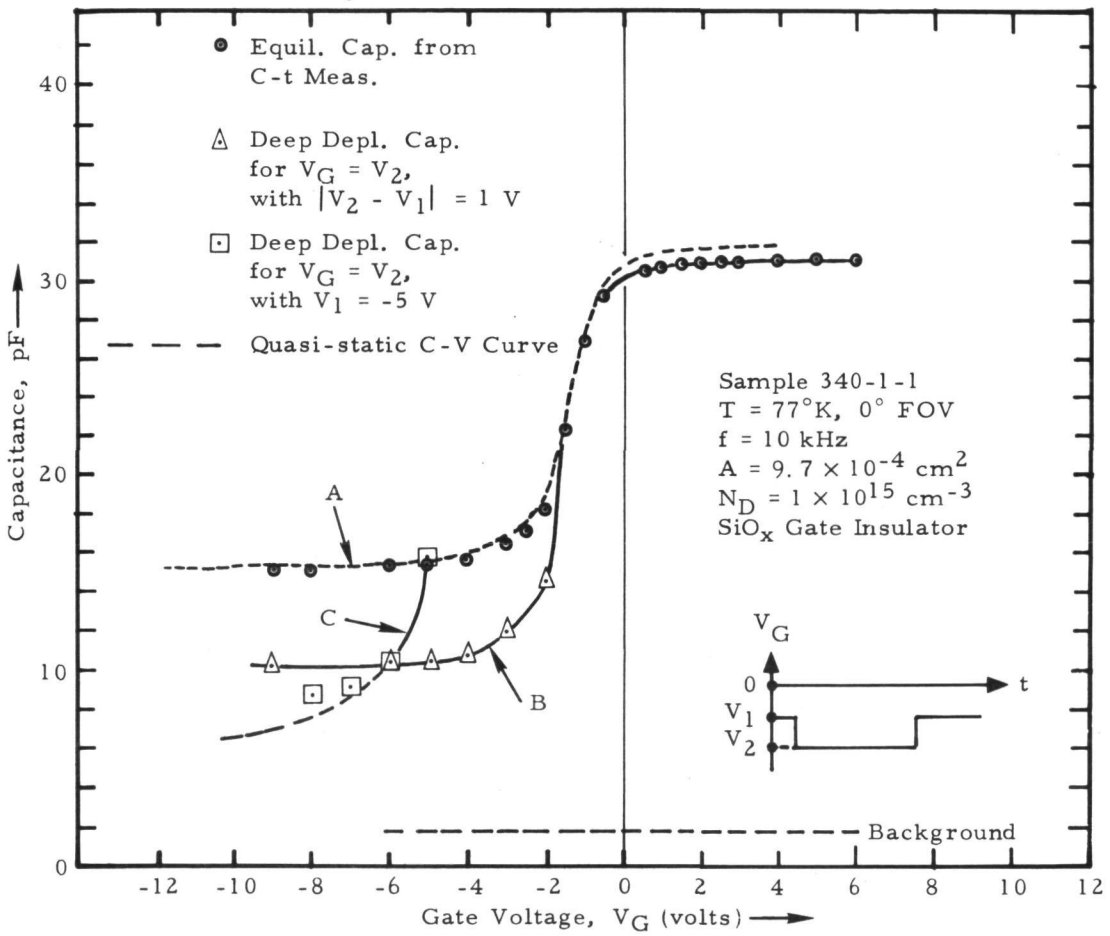


Figure 4-1. Equilibrium and Deep Depletion Capacitance Versus Voltage for InSb MIS Capacitor

The threshold voltage of the device in Figure 4-1 is approximately -4 V. Curve B plots the measured deep depletion capacitance for various values of V_2 from -2 V to -9 V while holding $|V_2 - V_1| = 1$ V. Full charge storage is seen to occur for $|V_2| \geq 4$ V. The charge stored in the well after establishment of equilibrium may be determined from the measured deep depletion capacitance and checked with the expected value which is:

$$Q_P = C_o \Delta V \qquad (4\text{-}1)$$
$$= (3.08 \times 10^{-8} \text{ f cm}^{-2})(1 \text{ V})$$
$$= 3.08 \times 10^{-8} \text{ c cm}^{-2}$$

The stored charge in terms of the measured deep depletion capacitance C_{DD} and equilibrium capacitance C_F is given by:

$$Q_P \simeq \frac{qN_D\epsilon_S (C_2^2 - C_1^2)}{2 K C_o} \qquad (4\text{-}2)$$

where

$C_2 = (C_o/C_F) - 1$

$C_1 = (C_o/C_{DD}) - 1$

q = electron charge = 1.6×10^{-19} c

N_D = substrate doping = 10^{15} cm^{-3}

ϵ_S = InSb permittivity = 17 ϵ_o

K = constant dependent on N_D and C_o where

$\psi_s \simeq K (V_G - V_{FB} - Q_P/C_o)$, $K < 1$

= 0.65 for thin oxide on these devices

From the data of curve B, $Q_P \simeq 2.8 \times 10^{-8}$ c cm^{-2} is obtained which is close to the predicted value for a ΔV of 1 V.

Curve C in Figure 4-1 similarly plots deep depletion capacitance but with V_1 held constant at -5 V (above threshold) and V_2 varied. At $|V_2 - V_1| \simeq 3$ V, the observed deep depletion capacitance saturates and begins to depart from the theoretical (dashed) curve. This limit to well depth is due to avalanche generation of minority carriers in the MIS structure, and is analogous to the usual avalanche breakdown in one-sided, abrupt junctions. The critical field for avalanche in InSb at 77°K is approximately 2.5×10^4 V cm^{-1} (one order of magnitude lower than for Si) corresponding to low breakdown voltages for InSb diodes (two orders of magnitude lower relative to Si) for comparable dopings. Similar breakdown voltages are observed on the InSb MIS structures. Typical avalanche surface potentials of 2.5 to 3 V are observed on 1×10^{15} cm^{-3} substrates with correspondingly higher values for lower impurity concentration

material ($BV \propto N_D^{-1}$). Since the dark current also increases as the substrate doping is decreased, a tradeoff must be made between breakdown and dark current effects. Material in the range of 7×10^{14} to 10^{15} cm^{-3} was used for the CCD processing during this program to keep dark current minimized; lower doping material will be used in future trials to study experimentally the lower range.

The MOSFET structure provides another useful test device that complements the MIS capacitor. In particular, the MOSFETs allow a rapid determination of threshold voltage and the effective mobility of carriers in the inversion layer. Drain curves for a typical witness MOSFET on an 8580 CCD wafer are shown in Figure 4-2. The MOSFET on the 8580 mask is a closed-geometry device with channel length L = 1 mil and W/L = 30, where W is channel width. The drain curves for these MOSFETs show that the devices generally follow ideal FET behavior, with good saturation and square-law characteristics in the saturation region. The FETs operate as p-channel enhancement-mode devices with threshold voltages of typically -5 V. The threshold voltage has been observed to vary with background illumination conditions during measurement, decreasing toward zero volts as the incident illumination is increased.

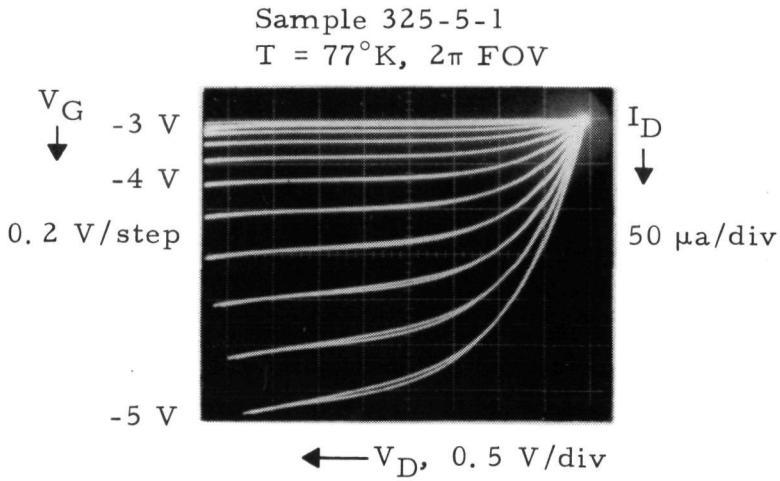


Figure 4-2. InSb MOSFET Characteristic Curves

In the saturation region, the drain current for an ideal FET is

$$|I_D| = \frac{\beta}{2} (V_G - V_T)^2 \qquad (4\text{-}3)$$

where $\beta = (W/L)\, C_o \mu$. Here, μ is the effective mobility of the holes in the inversion layer, V_G the gate voltage, and V_T the threshold voltage. From equation 4-3, a plot of square-root drain current $\sqrt{I_D}$ versus $(V_G - V_T)$ should yield a straight line, with slope = $\sqrt{\beta/2}$. Such a plot for three MOSFETs is shown in Figure 4-3 which shows the expected linear relationship. From the curves, one obtains β and, since W/L and C_o are known, the mobility may be determined. For the three devices in Figure 4-3, mobilities of 171, 160, and 171 $cm^2\ V^{-1}\ sec^{-1}$ are obtained.

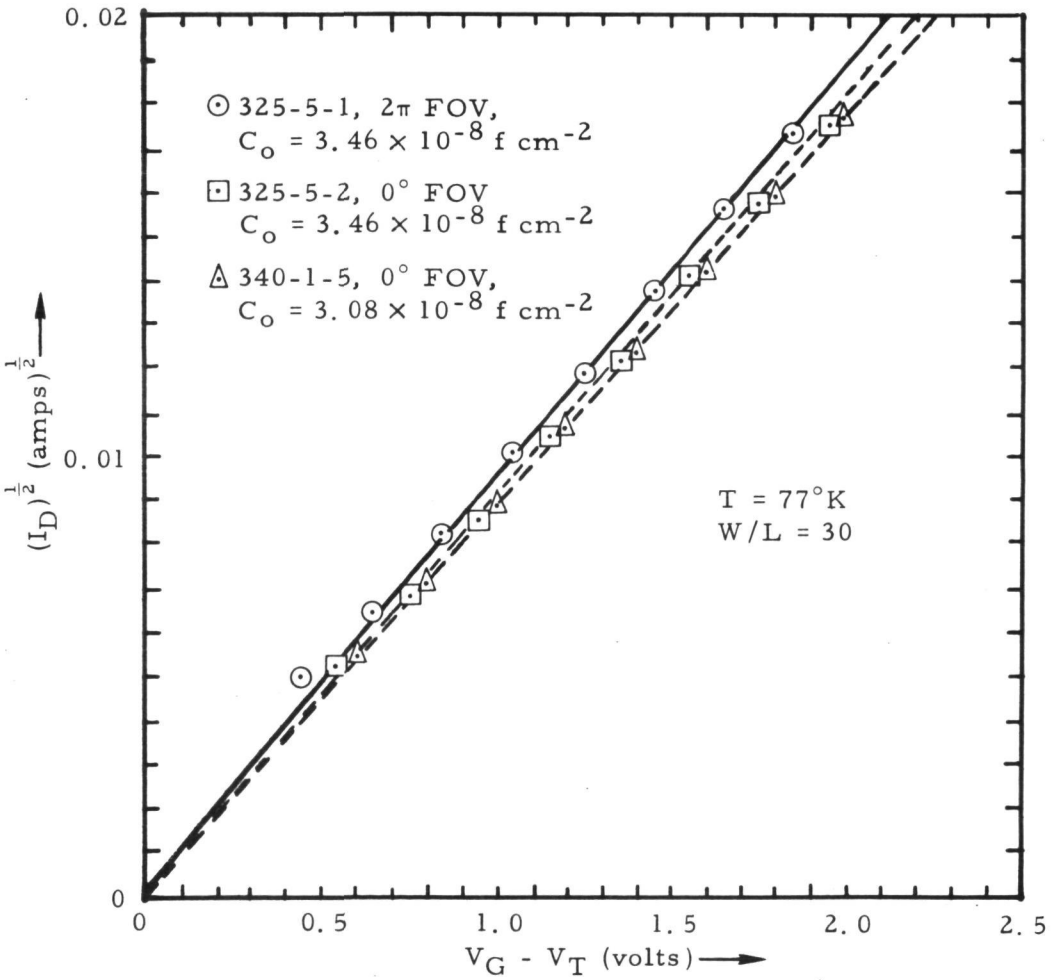


Figure 4-3. InSb MOSFET Transfer Characteristics

The channel mobility may also be determined from a measurement of the channel conductance g_D in the linear region. A plot of g_D versus $(V_G - V_T)$ should be linear in the ideal case with slope β. Curve A in Figure 4-4 shows a plot of this type for one of the devices in Figure 4-3. A higher effective mobility is deduced, $\mu = 280\ cm^2\ V^{-1}\ sec^{-1}$. The difference in mobility obtained in the linear and saturation regions is larger than can be accounted for by experimental error, and has been observed on all FETs examined to date. By measuring transconductance versus drain voltage at constant gate voltage, the effective mobility determined from the transconductance has been observed to decrease gradually with increasing drain voltage. This deviation from the simple model has not been investigated further. One possible explanation is a mobility dependence on drain (not gate) field, as suggested by some authors for silicon FETs.[2]

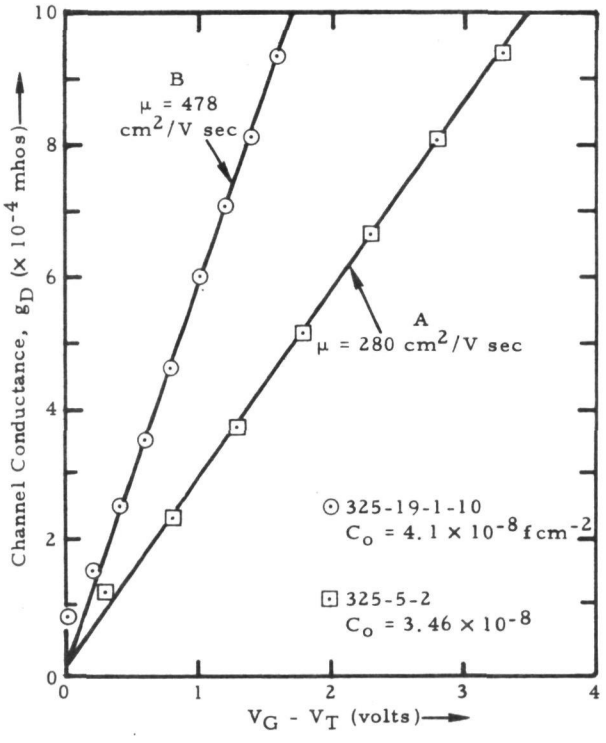


Figure 4-4. InSb MOSFET Channel Conductance in Linear Region Versus Gate Voltage ($T = 77°K$; $W/L = 30$; $|V_D| << |2\psi_B| \simeq 165$ mv)

[2] A. Bar-lev and S. Margalit, Solid-State Electronics 13, 1541 (1970).

The data thus far in this section have been for devices utilizing an SiO_x gate insulator approximately 1500 Å thick, which was utilized for all CCD devices discussed later in this section. MOSFETs processed in Company-funded studies and on a related contract[3] using Al_2O_3 as gate insulator have shown the highest mobilities we have observed to date. Curve B in Figure 4-4 shows the channel conductance curve for one of these FETs from which an effective mobility of nearly 500 $cm^2\ V^{-1}\ sec^{-1}$ is obtained. However, the SiO_x is more compatible with the present fabrication process than Al_2O_3.

It may be concluded that the effective mobility of the minority carriers in the InSb inversion layer is in the range of about 150 to 300 $cm^2\ V^{-1}\ sec^{-1}$ for the SiO_x devices, although the FETs are not adequately described by the simple FET model above.

PARTIAL CCD STRUCTURES

Prior to attempting operation of the full 8580 InSb CCDs, two partial structures were investigated: 1) an "undelineated" CCD structure; and 2) the last overlapping pair of gates plus output diodes of the 8580 four-bit CCD. These tests, coupled with the MOSFET results just described, established the operating voltages and other parameters needed for full CCD operation.

The "undelineated" CCD structures were processed as part of the four-phase device fabrication trials. When processing for the four-phase device with the 8580 mask set, the three-phase device also on the chip is completely processed at the same time, with the exception of the delineation of the gaps in the surface metal necessary to isolate the transfer electrodes. The resulting structure contains input/output diodes, a channel stop structure defining a channel 8 mils wide by 29 mils long, and a large "undelineated" surface metal gate. This constitutes a very long channel MOSFET. With

[3]Contract DAAK02-74-C-0241, U. S. Army Mobility Equipment Research and Development Center.

one diode tied to substrate (source), the other diode reverse-biased (drain), and with the CSM biased appropriately, biasing the gate above threshold should produce a channel current given by equation 4-3 for large drain voltages. A small current will be observed relative to the MOSFETs because of the large reduction in the channel W/L. The current should scale with W/L if the effective mobility in the inversion layer remains constant and the channel stop structure is functioning properly.

Devices of this type were tested and the expected magnitude of channel current was measured. Figure 4-5 shows square-root channel current versus gate voltage for one such device, for bias conditions given in the figure. Using the geometric (nominal) W/L of the channel = 0.275, an effective channel mobility of 160 $cm^2\ V^{-1}\ sec^{-1}$ was obtained from the data. This is in good agreement with that observed on MOSFETs from the same wafer (325-5). It is concluded, therefore, that the long channel of this device is effectively defined by the CSM to close to its geometric W/L value. No change in channel current was observed when the CSM bias was varied between zero to a few volts negative with respect to substrate, i.e., in the flatband and depletion ranges, as expected. Finally, this test offers indirect evidence that surface conditions over the large 8 × 29 mil gate area of this device are defect-free and reasonably uniform, which is of course a requirement for a CCD of the same area.

The second partial structure examined before full register testing consisted of the last two gates and the output diode of the 8580. With all other gates grounded, this portion of the device enabled a single transfer of charge from the last clocked gate into the output diffusion to be observed. The last clocked gate ϕ_4 (a buried metal gate) was clocked at a low frequency (e.g., 100 Hz) to obtain a quantity of charge in the ϕ_4 well due to thermal generation. The output gate ϕ_o, a surface metal gate which overlaps the ϕ_4 gate and output diffusion, was dc-biased such that the surface potential under this gate was less than the surface potential of the filled ϕ_4 well and the output diffusion. When the ϕ_4 clock turns off, the charge collected under ϕ_4 transfers

across the output gate and into the reverse-biased diffusion. This mode of operation was observed and established the voltages required on the output elements as well as the ability to transfer charge to the output. The required dc bias on ϕ_o was in the range of -10 to -14 V with respect to substrate, above the threshold voltage of the surface metal gates (3700 Å insulator thickness on the devices tested). Buried metal clock was typically -6 to -8 V, consistent with the data of Figure 4-1.

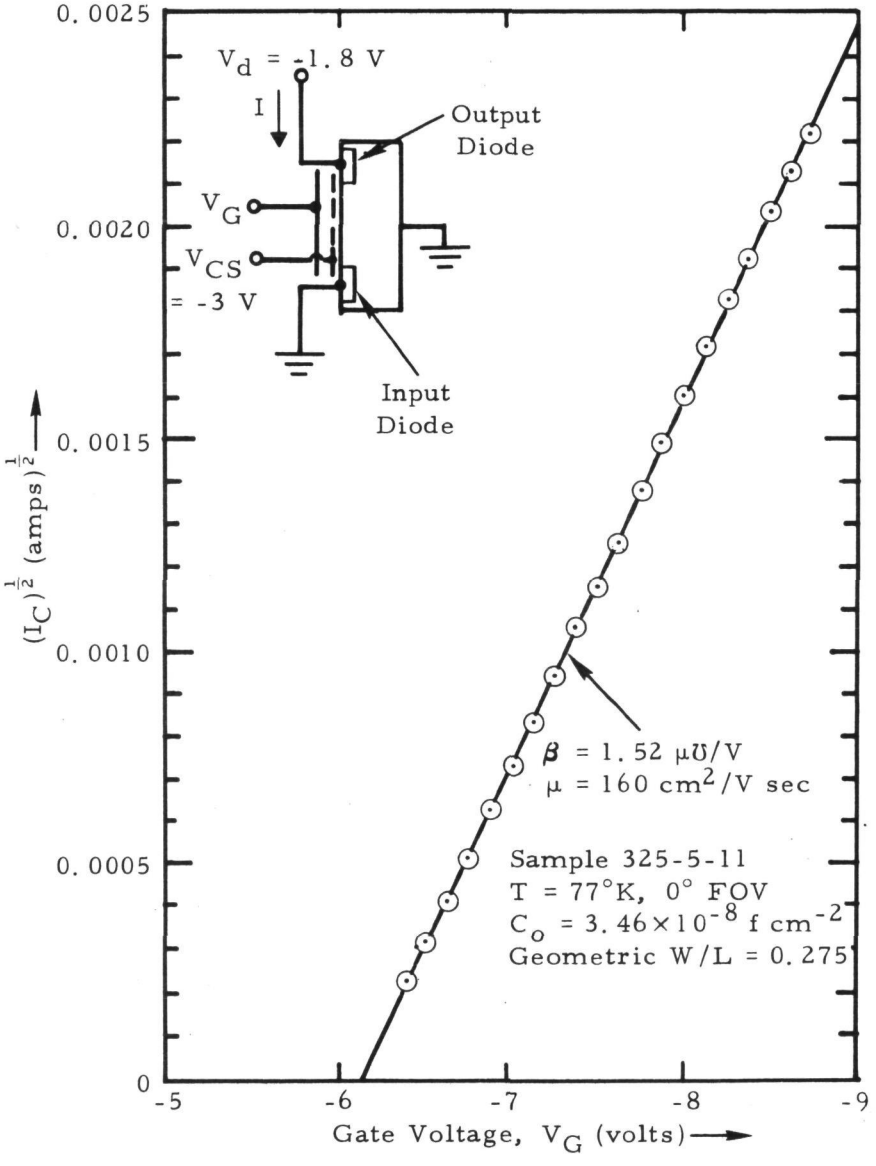


Figure 4-5. Channel Current Versus Gate Voltage for Undelineated InSb CCD Structure

Two output circuits were used in the partial CCD tests and the full register tests to follow. In the first tests, the output diffusion was reverse-biased through an output resistor R_o (100 KΩ to 1 MΩ) and ac-coupled to an external voltage amplifier, as shown in Figure 4-6. Any charge transferred to the output is collected by the reverse-biased diode, and the arrival of the charge is observed on the oscilloscope as a voltage across the output resistor. For full register tests, the value of R_o is chosen such that $R_o C_{out} < T_C$ where C_{out} is the output node capacitance and T_C the clock period. A source-follower stage may be mounted on the cold probe at 77°K adjacent to the InSb device to eliminate the contribution of cable capacitance to C_{out} for improving the speed of this direct output circuit.

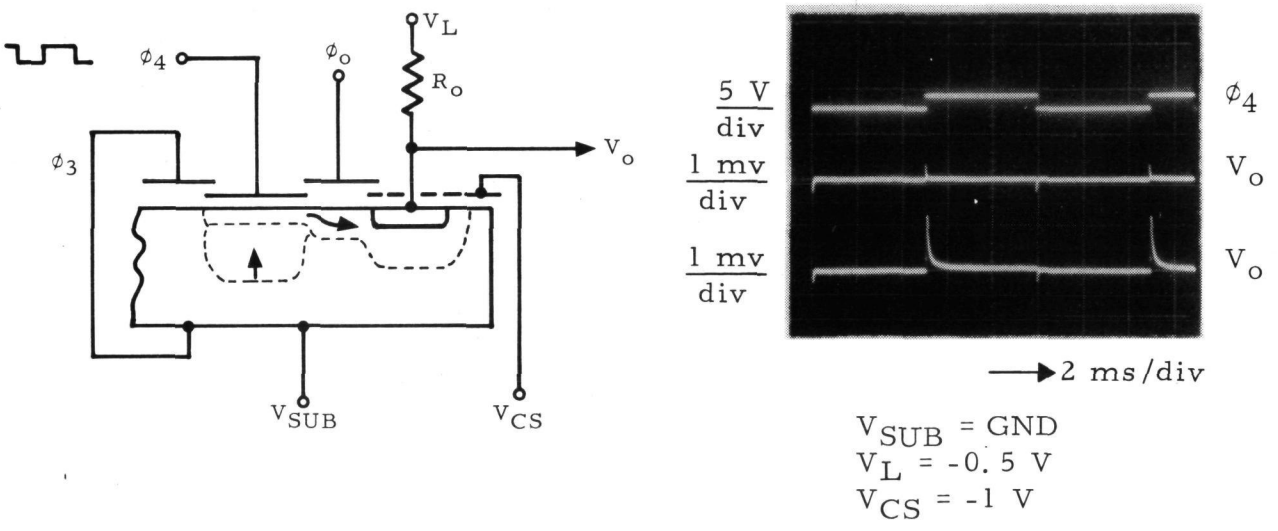


Figure 4-6. Single Transfer of Charge to Output Diffusion with Direct Output (T = 77°K, 0° FOV; Sample 340-1-7)

Transfer of thermal charge from ϕ_4 to the output diode using a direct output is shown in Figure 4-6. With the output gate on, a voltage pulse is observed across the 100 KΩ resistor when ϕ_4 turns off (lower trace in the oscilloscope photograph). With ϕ_o off, only the clock feedthrough is observed (center trace). For a long integration time relative to the storage time under the ϕ_4 electrode, nearly the full thermal equilibrium charge under this

well should be detected at the output. Integration of the output pulse to determine the transferred charge $Q = R_o^{-1} \int v dt$ was found to give values agreeing closely with the estimated values from equation 4-1.

The second circuit used was a discrete precharge (or reset) output amplifier using two low-noise silicon MOSFETs (see Figure 4-8 on page 4-13). Although this type of circuit is usually integrated on-chip to keep output and stray capacitances to minimum values, a functioning circuit may be built up in discrete form for test purposes although responsivity is low and feedthrough is increased. In this circuit, the diode functions as a charge-storage detector for signal charge. A reset MOSFET is used to set the output diode to a fixed reverse bias during the time when the CCD is not transferring charge into the diffusion. With the reset switch off, signal charge is transferred to the diode capacitance at the next transfer giving a corresponding voltage charge across the diode. A second MOSFET is used as a source-follower stage to sense the diode voltage and drive the following stages. The voltage responsivity of the circuit is A_v/C_{out} volts/coulomb where C_{out} is the total output node capacitance and A_v is the source-follower gain.

Transfer of thermal charge from ϕ_4 to the output using this circuit is shown in Figure 4-7. Because of the discrete FETs, the package and wiring capacitance, and the large size of the InSb output diode, the responsivity of the circuit is low, approximately 15 mv/pC including the 0.85 gain of the source follower. The reset clock feedthrough is large (0.6 V) due to the same factors. This circuit, however, gave about an order of magnitude higher signal levels compared to the direct output and was sufficient for the first CCD tests described in the next section, although significant improvements are needed in the implementation of this circuit in future work before quantitative gain tests are performed.

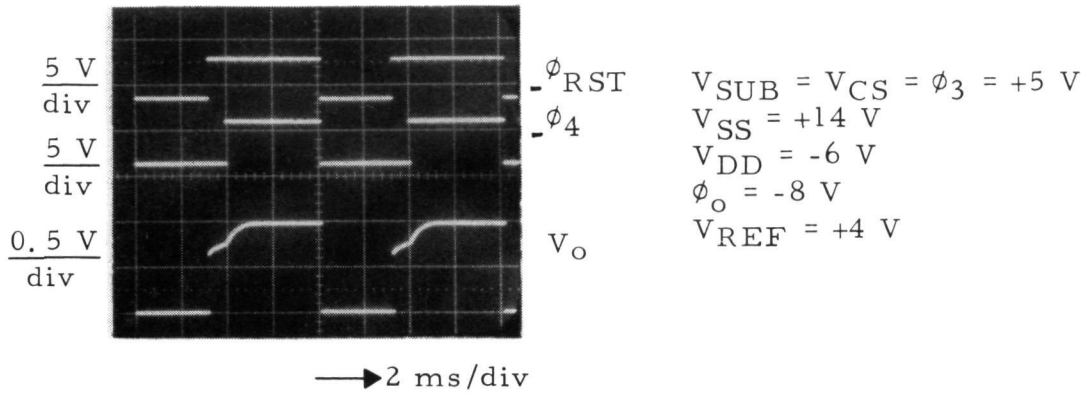


Figure 4-7. Single Transfer of Charge to Output Diffusion with Precharge Output (T = 77°K, 0° FOV; Sample 340-1-9)

8580 FOUR-PHASE CCDs

8580 four-phase CCDs have been operated as shift registers with signal voltages applied to the input and appropriately delayed signals observed at the output. Typical operating voltages are given in Table 4-1 with nomenclature shown in Figure 4-8.

The four-phase clock layout of the 8580 CCD allows the device to be clocked in several modes. The InSb CCDs have been operated with three clock timings: (a) simple four-phase mode; (b) four-phase mode with storage under buried gates only; and (c) simulated two-phase mode. In the simple four-phase mode, each phase is in the on state for approximately 1/4 T_C and the signal charge is stored sequentially under both surface and buried metal gates. This mode results in four transfers per bit. Modes (b) and (c) are shown in Figure 4-9. In mode (b), the buried metal gates are on approximately 1/2 T_C and the surface metal gates less than 1/2 T_C; the clock voltages are such that the surface gates ϕ_1 and ϕ_3 transfer charge from buried gate to buried gate (e.g., ϕ_2 to ϕ_4) without storage under the surface metal. This mode results in two transfers per bit. An advantage of this mode compared to conventional two-phase clocking is that the quantity of charge that can be stored under a storage gate is almost a full bucket since the preceding transfer gate can be turned off. The simulated two-phase mode (c) is similar to

the clocking in the familiar two-phase stepped-oxide structure. ϕ_1 and ϕ_2, and ϕ_3 and ϕ_4 are clocked in phase, but in this case the clock magnitudes of the surface and buried gates may be independently varied to create the optimum surface potential profile.

Table 4-1. Typical Operating Voltages for 8580 Four-Phase CCD

Function	Symbol	Voltage (volts)
Substrate	V_{SUB}	+5
Channel Stop	V_{CS}	+4 to +5
Input Diffusion	V_{INDC}	+4 to +5
Surface Metal Input Gate	ϕ_{INS}	-6 + SIG
Buried Metal Input Gate	ϕ_{INB}	-5
Transfer Gates, Surface Metal	ϕ_1, ϕ_3	-4 → -6
Transfer Gates, Buried Metal	ϕ_2, ϕ_4	-2 → -3
Output Gate	ϕ_o	-8
Output Reference Voltage	V_{REF}	+4 to +4.5
S. F. Drain	V_{DD}	-6
S. F. Source	V_{SS}	+14
Output Circuit Reset	ϕ_{RST}	+5 → 0 ~ in phase with ϕ_4

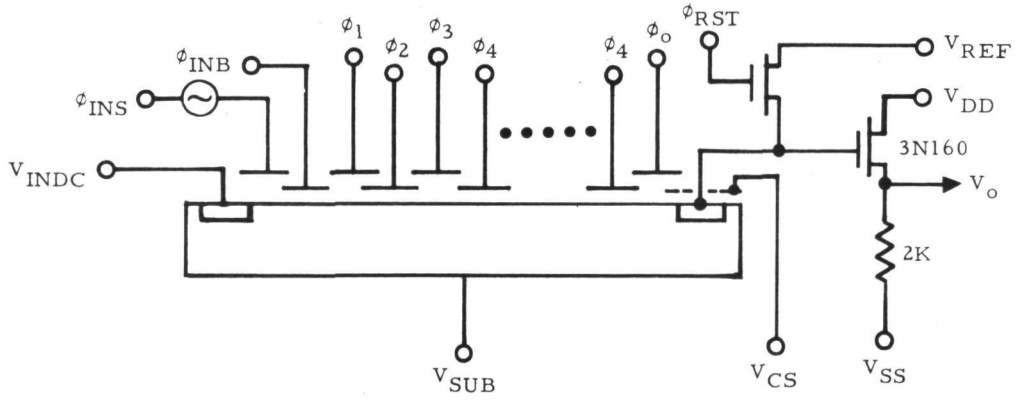


Figure 4-8. Four-Phase InSb CCD Schematic

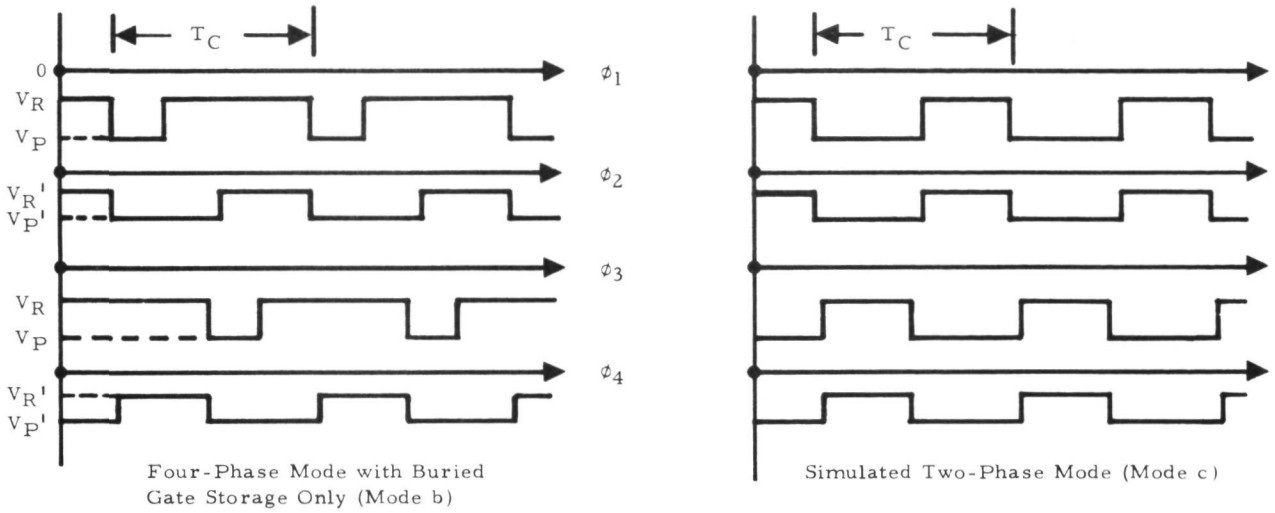
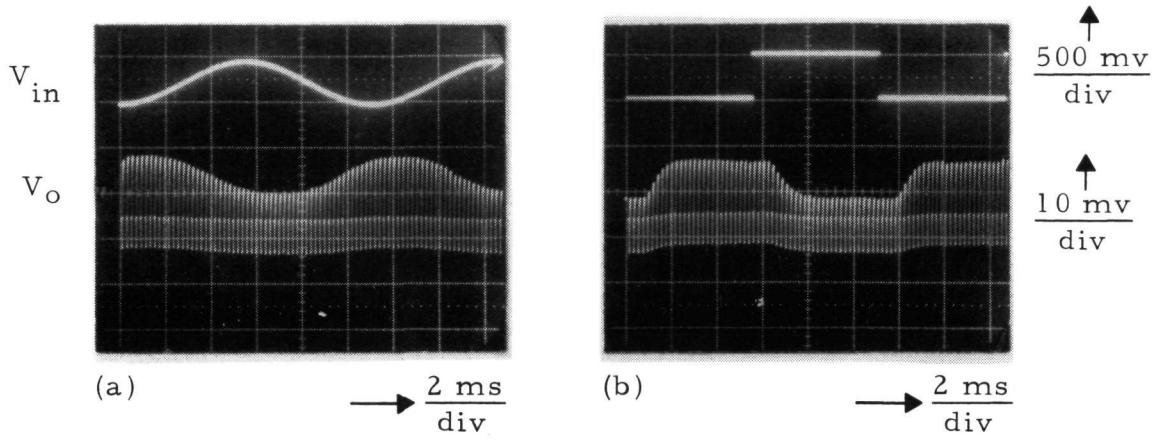


Figure 4-9. Clocking Modes

The CCDs were also operated with three input circuit variations. The first method utilizes the direct injection of a signal into the input diffusion (V_{INDC}), with the two input gates ϕ_{INS} and ϕ_{INB} appropriately dc-biased above their thresholds to couple the charge into the register. This input circuit may be analyzed as a MOSFET-mode, common-gate configuration. A common-drain configuration was found to give improved input control. In this method (Figure 4-8), the input diffusion is biased to a dc-potential (adjusted for fat zero), a signal voltage is applied to the first input gate ϕ_{INS}, and the second input gate ϕ_{INB} is dc biased to form a virtual drain. A third variation is similar, but with the signal voltage applied to ϕ_{INB}.

Figure 4-10 shows input/output waveforms for an 8580 four-bit InSb CCD clocked at 5 kHz, with (a) sine wave input, and (b) square-wave input. The simulated two-phase clock mode was used in this case along with a ϕ_{INB} input. The output, which is a sampled and delayed replication of the low-frequency input signal, is delayed by $N_B T_C$, the number of bits times the clock period or $4 \times 200\ \mu s = 0.8$ msec. *

*Note: The output waveform is inverted with respect to the input waveform on these and subsequent oscilloscope photographs.



Device 340-2-14
f_c = 5 kHz
Clock Mode (c)
ϕ_{INBM} Input
T = 77°K, 0° FOV

Figure 4-10. InSb CCD Output Waveforms

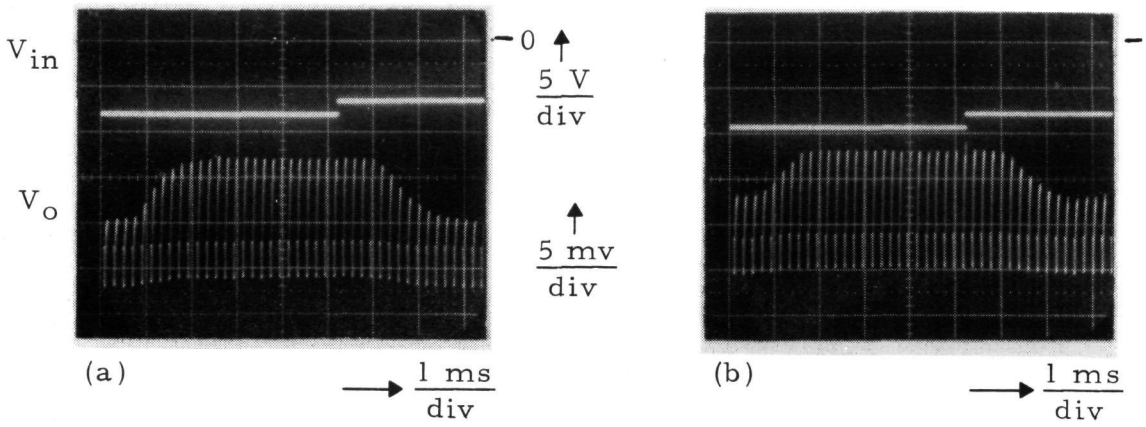
The transfer efficiency of the 8580 devices was determined from the output waveform using a square-wave input as shown in Figure 4-11(a). In the ideal case, the output should consist of a series of ones of constant amplitude. In a real device, transfer inefficiency results in loss of charge from one or more leading signal pulses, and, after the last correctly-transferred output signal, the emergence of one or more trailing output pulses. If the CCD has efficiency per transfer η, and if this is constant for each transfer gate in the device, then the net transfer efficiency of the device is η^n, where n is the number of transfers. From an output waveform as in Figure 4-11(a), if B = magnitude of first output pulse and A = maximum value of signal output, then

$$\eta^n = B/A \qquad (4\text{-}4)$$

from which η may be readily determined since n is known. In Figure 4-11(a), clock mode (c) was used so that n = 2 transfers per bit × 4 bits = 8 transfers. From the figure, B = 8 units*, A = 31.5 units giving $\eta = (8/31.5)^{1/8}$ =

*Signal magnitudes were measured with an optical comparator on the original oscilloscope photographs, with accuracy of ±0.5 unit.

0.843 ± 0.01 per transfer. This is a typical result for η of the 8580 device in this clock mode, with values observed ranging from 0.82 to 0.86 at 5 kHz.



Device 340-2-14
f_c = 5 kHz
ϕ_{INSM} Input

Figure 4-11. Output Waveform, Clock Mode (c)

The sum of the losses (charge deficiencies) in the leading signal pulses and the sum of the trailing signal outputs also are related to the device efficiency, but in a more complicated way. It can be shown that* the sum of the charge deficits δ_j in the leading signal outputs (normalized to the maximum signal output), or the sum of the normalized trailing signal outputs δ_j', is given by

$$\sum_{j=1}^{M} \delta_j = \sum_{j=M+1}^{\infty} \delta_j' = \eta^n \left\{ \frac{n\epsilon}{(1-\epsilon)^{n+1}} - \sum_{k=M+1}^{\infty} (k-M) \binom{n+k-1}{n-1} \epsilon^k \right\} \qquad (4\text{-}5)$$

where M = number of pulses in input string, ϵ = transfer inefficiency = 1 - η, η and n are as defined previously, and $\binom{a}{b}$ denote binomial coefficients. It can be shown that, for most values of n and ϵ encountered in practice, and if a suitably large number M of pulses is used in the measurement, the

*J. D. Phillips, private communication.

sum on the right-hand side of equation 4-5 may be neglected and, to good accuracy, equation 4-5 becomes:

$$S_L = S_T \cong \frac{n\epsilon\,(1 - \epsilon)^n}{(1 - \epsilon)^{n+1}} = \frac{n\epsilon}{(1 - \epsilon)} \qquad (4\text{-}6)$$

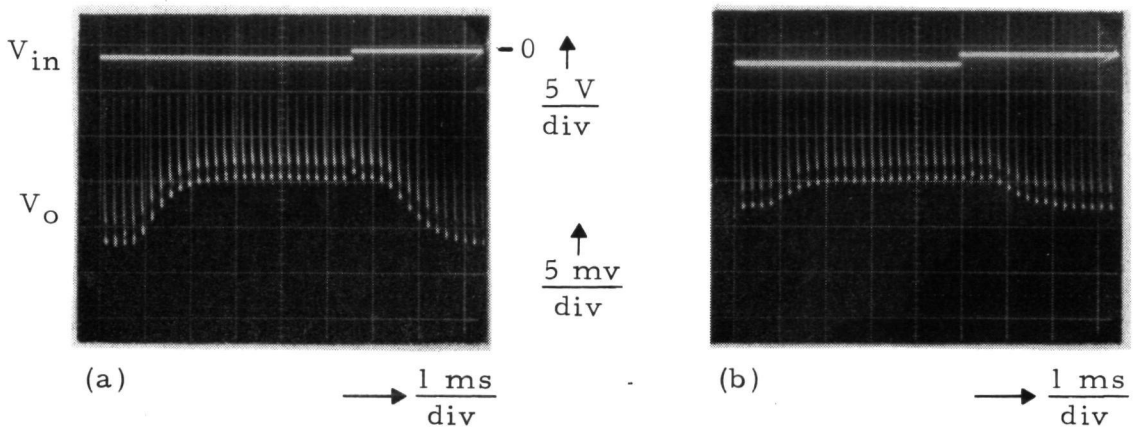
where S_L and S_T have been used to denote the leading and trailing sums, respectively.

Applying equation 4-6 to the output waveform of Figure 4-11(a), one obtains a leading sum $S_L = 1.7 \pm 0.2$ which gives $\eta = 0.825 \pm 0.017$ in reasonable agreement with the result of equation 4-4. In all devices examined, the values of η determined by means of S_L and equation 4-6 were within 4% of the values obtained using equation 4-4. However, good agreement was not obtained using the trailing pulse sum S_T when using clock mode (c) (as in Figure 4-11) or clock mode (b). For example, the output in Figure 4-11(a) exhibits $S_T = 2.7 \pm 0.2$ corresponding to $\eta = 0.75 \pm 0.014$, lower than the result of the two previous methods. Trailers generally exceeded loss in the leaders for the above two clock modes.

The result of Figure 4-11(a) is typical of the 8580 devices operating with zero or very small fat zero level. The efficiency improves slightly with a large FZ. Figure 4-11(b) shows the same device as in Figure 4-11(a) but with about a 40% FZ level. The indicated efficiency is 0.85 ± 0.01 and a corresponding slight "squaring" of the output waveform is observed.

Clock mode (a), simple four-phase clocking, resulted in the highest transfer efficiency observed for the device most thoroughly tested, No. 340-2-14. Figure 4-12(a) shows an output waveform for this device using clock mode (a). In this mode, n = 4 transfers per bit × 4 bits = 16. From Figure 4-12(a), $\eta = (B/A)^{1/16} = (5/34.5)^{1/16} = 0.886 \pm 0.006$ per transfer. In this clock mode, S_L and S_T are more nearly equal than in the other modes. In Figure 4-12(a), $S_L = 2.6 \pm 0.2$ leading to $\eta = 0.860 \pm 0.01$ per transfer by this technique. From the trailers, $S_T = 2.9 \pm 0.2$ giving $\eta = 0.847 \pm 0.01$. Figure 4-12(b) shows an output in the same clock mode but with a large FZ,

approximately 50%. In this case, η has improved to 0.919 ± 0.009 per transfer determined from the first output pulse, and 0.880 ± 0.01 per transfer from the leading and trailing sums. An average of several measurements showed that $\eta \cong 0.90$ was typical of the device operating in clock mode (a).



Device 340-2-14
f_c = 5 kHz
ϕ_{INBM} Input

Figure 4-12. Output Waveform, Clock Mode (a)

Using clock mode (b), efficiencies comparable to mode (c) were observed. η was measured to be in the range from 0.84 to 0.88. (Several devices from wafer 340-2 were tested in this mode with similar results.) Clock frequencies were varied from 2.5 to 12.5 kHz with no change in efficiency values within experimental error.

It is concluded, therefore, that the transfer efficiency of the 8580 devices in the 5-kHz clock frequency range is η = 0.82 to 0.92 per transfer, depending on the clock mode, fat zero level, and measurement technique used. This efficiency is correlated with theoretical expectations in Section 5. As discussed in that section, considerable improvement in efficiency is anticipated on future devices with shorter gate lengths.

Section 5

InSb CCD TRANSFER EFFICIENCY ANALYSIS

The transfer efficiency of a charge-coupled device is a measure of the information (i.e., charge) lost during the transfer from one storage well to the next in the CCD structure. At least three prime mechanisms can limit device transfer efficiencies. These are: 1) loss of signal charge directly to the substrate, 2) loss of charge in interface state traps, and 3) loss of charge to traps and/or barriers formed by irregularities in the potential well profiles formed by the transfer electrodes of the device. The loss of charge to the substrate can result from improper doping of the substrate, from a defective gate insulator, or from failure of the device design to ensure a deep depletion, majority-carrier-free region for proper storage of the signal charge. The loss of charge to interface states is obviously dependent on the existence of such states and on their density. Other parameters which affect loss to these states are: 1) the capture times of the states, 2) the emission time of the states, and 3) the area of the storage well over which interface state trapping will be most significant. Other parameters also exist and discussions of these are given in the treatments of Tompsett[4] and Mohsen, et al.[5] Finally, the loss of charge to irregularities in the potential profiles of the device can be quite significant for designs having gaps between adjacent gates in the CCD. The magnitude of this effect for any given design can only be determined by a complete solution of the two-dimensional Poisson equation which describes the CCD design.

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[4]M. F. Tompsett, "The Quantitative Effects of Interface States on the Performance of Charge-Coupled Devices," IEEE Trans. on Elect. Devices, Vol. ED-20, No. 1, p. 45, January 1973.

[5]A. M. Mohsen, T. C. McGill, Y. Daimon, and C. A. Mead, "The Influence of Interface States on Incomplete Charge Transfer in Overlapping Gate Charge-Coupled Devices," IEEE J. of Solid-State Circuits, Vol. SC-8, No. 2, p. 125, April 1973.

The devices studied in the present effort were of the overlapping gate type. As a result, limits to transfer efficiency due to potential profile irregularities are expected to be quite small. As stated above, this expectation can only be checked further by detailed calculation. Such a calculation is planned for the near future, but in the interim it may be noted that computations for silicon substrate devices with small gaps do support the assumption. Similarly, studies on the 8580 device have thus far not indicated difficulties due to substrate injection. The investigation of this potential loss mechanism will be maintained in all future studies, however, to ensure that maximum transfer efficiencies and optimum device design are achieved.

It can be argued, therefore, that the principal loss mechanisms now limiting high transfer efficiencies in the existing InSb CCD structures are: 1) interface state losses, and 2) excessively long gates. The latter problem is related to the simple fact that CCDs are designed on the principle of coupling of storage wells for two adjacent gates. The greater this coupling (i. e., the higher the "fringe fields"), the more rapid the transfer of charge from one well to the next. If the gates are wide ($\gtrsim$0. 5 mil for typical silicon CCD structures), then the field strengths in the middle of a storage gate become insignificant. In such an operating mode, the charge ultimately must be transferred solely by diffusion which is inherently slow as the charge to be transferred decreases. The devices under study are thus expected to be restricted in their transfer characteristics by interface state losses and diffusion limitations. It is difficult to carry out explicit computations predicting the effects of interface states since such a task requires a full dynamic solution of the CCD structure and detailed knowledge of the interface states. As a result, it is worthwhile to consider an approach which yields qualitative data while preserving the option of quantitative computations for the future. Such approaches have been considered by Tompsett,[4] Mohsen, et al.,[5] as well as Lee and Heller.[6]

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[6]H-S Lee and L. G. Heller, "Charge-Control Method of Charge-Coupled Device Transfer Analysis," IEEE Trans. on Elect. Devices, Vol. ED-19, No. 12, p. 1270, December 1972.

The calculations in this section were based on the work of Lee and Heller.[6] The basic assumptions in their approach include: 1) instantaneous charge redistribution during the transfer period, and 2) the use of an effective time constant, τ_s, to describe the effect of interface states. Although these assumptions lead to certain limitations in the formulation, the approach does provide a qualitative understanding of the effect of interface states on transfer efficiency, which was the goal of this study.

The principle conclusions of Lee and Heller's work are summarized by the formulae:

$$\text{Transfer efficiency} \equiv \eta = 1 - F(t, \tau_s) - F_{loss}(t, \tau_s)$$

$$\text{Fraction of mobile charge left in storage well at time, t} \equiv F(t, \tau_s) = \frac{K \exp\left[-Kt/t_r\right]}{K + \left(\frac{\pi^2}{8}\Delta V\right)\left(1 - \exp\left[-Kt/t_r\right]\right)}$$

$$\text{Fraction of charge trapped in interface states} \equiv F_{loss}(t, \tau_s) = \frac{\ell n\left(\frac{1}{F(t, \tau_s)}\right) - Kt/t_r}{\left(\frac{\pi^2}{8}\Delta V\right)\left(\tau_s/t_r\right)} \quad (5\text{-}1)$$

$$\Delta V = \frac{\text{average charge/unit area in storage well}}{\text{average capacitance/unit area in storage well}}$$

$$K = \frac{t_r}{\tau_s} + \frac{\pi^2}{4}\left(\frac{kT}{q}\right)$$

$$t_r = \frac{L^2}{\mu} \quad \text{where} \quad L \equiv \text{gate length for discharging storage well}$$

$\mu \equiv$ minority carrier mobility (holes for n-type substrates)

$\tau_s \equiv$ effective time constant for charge loss to interface states

To apply this result, the time, t, at which the inefficiencies are computed is taken as one-quarter of a clock period (= 1/4 f_c) or one-half of a clock period (1/2 f_c) depending on whether true four-phase or simulated two-phase operation is used. Here f_c is the CCD clock frequency. The following values were used in the calculations, unless noted otherwise:

$$\mu = 250 \text{ cm}^2/\text{volt}\cdot\text{sec}$$
$$(kT/q) = 6.6392 \times 10^{-3} \text{ volts}$$
$$N_{SS} = 10^{12} \text{ cm}^{-2}\text{-eV}^{-1}$$
$$C_o = 3.2 \times 10^{-8} \text{ f cm}^{-2}$$

To consider the effect of diffusion limited processes with no interface state loss, the above results are applied in the limit $\tau_s \rightarrow \infty$. For the 8580 device operating in a two-phase mode, the relevant value for L is 100 μm. Using this value in equation 5-1 and using for ΔV the values of 0.1, 1, 2, and 8 volts, the results of Figure 5-1(a) are obtained. A similar two-phase computation for the 8582 device, which has 1-mil gates, is shown in Figure 5-1(b). Since the 8582 has a smaller effective L (50 μm) than the 8580, it is expected to exhibit a higher transfer efficiency or, equivalently, a smaller inefficiency. This expectation is validated by the results of Figure 5-1. For the same operating frequencies, it is clear that the 8582 device is predicted to have higher transfer efficiencies. Note that as the voltage swing of the storage well, basically the storage well depth, increases, then the efficiency increases. This is true since ΔV is proportional to the amount of charge (q_{av}) in the well. As q_{av} increases, the ratio of the amount of charge left behind (this is approximately constant if transfer is diffusion limited) to q_{av} must decrease. But, it is the ratio q_{left}/q_{av} which defines the charge loss F (t, τ_s). Hence, as q_{av} (α ΔV) increases, it is expected that F (t, τ_s) will decrease as indicated in Figure 5-1.

Figure 5-1 reveals that transfer inefficiency increases rapidly with frequency but, at 5-kHz operation, an efficiency of >0.998 is expected in the diffusion limit for the 8580 device provided that ΔV is 0.1 volt or higher. From the observed 8580 device output signals and device parameters, it can

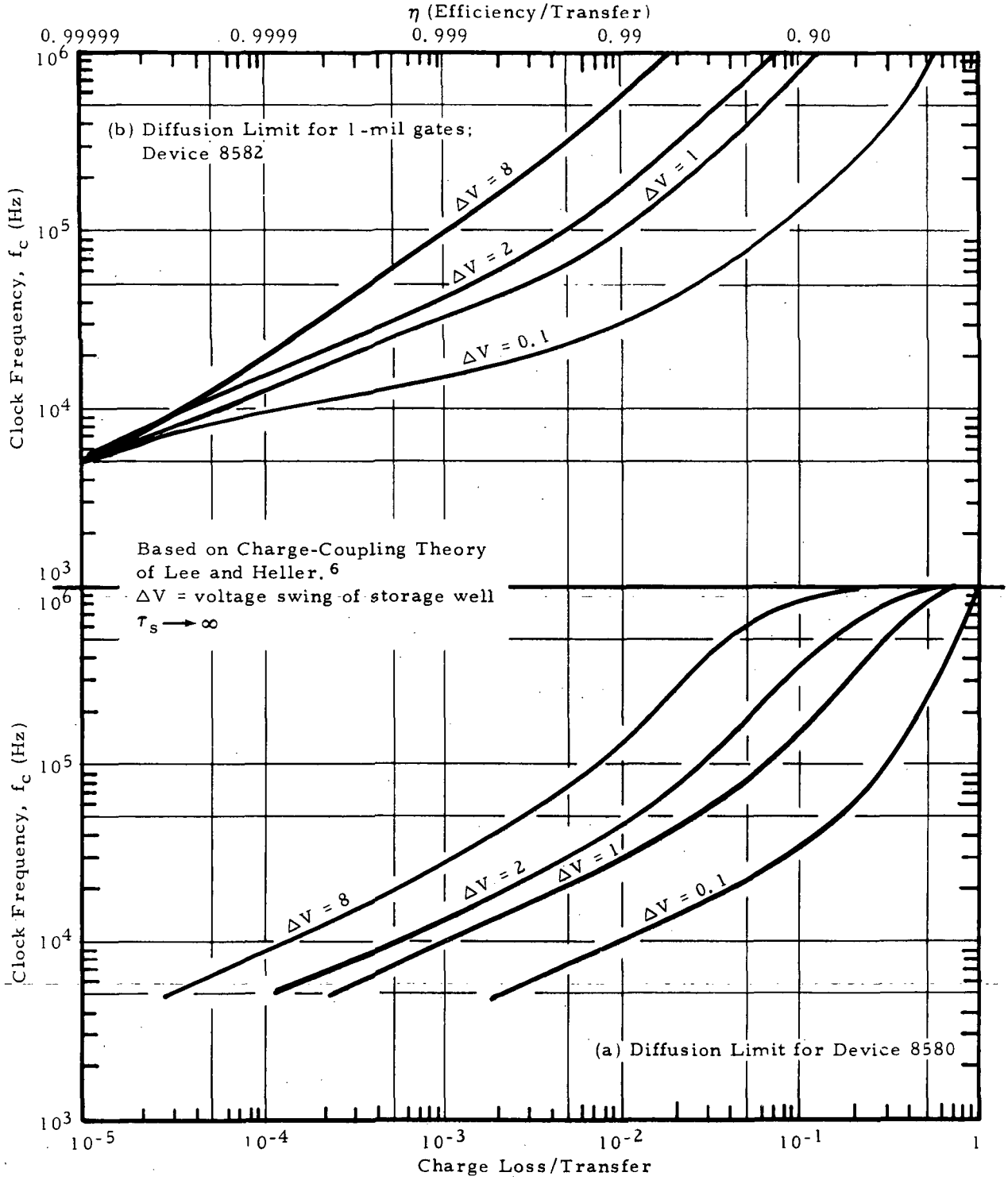


Figure 5-1. Mobile Charge Loss/Transfer [F (t, τ_s)] for Devices 8580, 8582 as Functions of Storage Well Depth (ΔV)

be shown that the actual ΔV is in the range $\Delta V = 0.3$ to 0.6 volt. From Figure 5-1, this would indicate an efficiency of almost 0.999 at 5 kHz. Since the observed efficiency is about 0.90, it is concluded that the diffusion-limited efficiency is not being obtained in the 8580 device.

Previous measurements[1] have indicated InSb interface state densities of $N_{SS} \simeq 10^{12}/cm^2$ -eV. Such a value is high by silicon standards, and it is to be expected that this value will impact CCD operation in InSb as well as in silicon. This value for N_{SS} can be qualitatively confirmed by the 8580 CCD results using Tompsett's[4] formulation of inefficiency contributions by interface states. For no background charge in the CCD, Tompsett shows that the inefficiency due to interface trapping is, for two-phase operation:

$$\epsilon = \frac{q\,kT\,N_{SS}}{C_o\,\Delta V}\,\ell n3 \qquad (5\text{-}2)$$

Using $C_o = 3.2 \times 10^{-8}$ f cm^{-2} and $N_{SS} = 10^{12}$ cm^{-2} $-eV^{-1}$, the results in Table 5-1 are obtained.

Table 5-1. Transfer Efficiency Versus Stored Charge Voltage Equivalent for $N_{SS} = 10^{12}$ cm^{-2} $-eV^{-1}$

ϵ	η	ΔV
0.36494	0.63506	0.1
0.12165	0.87835	0.3
0.091235	0.90876	0.4
0.072588	0.92741	0.5
0.036494	0.96350	1
0.018247	0.98175	2
0.007299	0.99270	5

The observed value for η of $\simeq 0.90$ corresponds to $\Delta V \simeq 0.4$ volt. If $N_{SS} \simeq 10^{13}/cm^2$ -eV, however, then a value of $\eta \simeq 0.90$ would require $\Delta V \simeq$ 4 volts. Similarly, $N_{SS} \simeq 10^{11}/cm^2$ -eV would require $\Delta V \simeq 0.04$ volt. As noted previously, the value of ΔV observed for the 8580 is in the range of 0.3 to 0.6 volt. Therefore, the observed efficiencies are consistent with N_{SS} in the range:

$$7.5 \times 10^{11} \lesssim N_{SS} \lesssim 1.5 \times 10^{12} \text{ cm}^{-2} \text{ -eV}^{-1}$$

Although this argument is somewhat simplified, it does provide a bound in agreement with the data measured directly by other techniques. The use of this as a quick method of estimating interface state density is certainly suggested.

To obtain more information on the characteristics of interface trapping in limiting CCD transfer efficiency, the values of $F(t, \tau_s)$ and $F_{loss}(t, \tau_s)$ are considered at different frequencies and different τ_s. The results of such calculations are given in Figures 5-2 and 5-3. Figure 5-2 gives the charge loss $F(t, \tau_s)$ as a function of frequency and τ_s values of 10^{-4}, 10^{-5}, and 10^{-6} sec. The devices considered were the 8582 (1-mil gates) in four-phase operation and a projected device with 0.5-mil gates, also in four-phase operation. In comparing these results, it is clear that for the device with the shorter gates, the charge loss is again reduced. There is, however, little variation of the fractional mobile charge loss due to differing τ_s values. A consideration of Figure 5-3 demonstrates that this is definitely not the case for the interface loss function $F_{loss}(t, \tau_s)$. An order of magnitude variation in this function is obtained for each such variation in the τ_s value. Due to this large variation and the difficulty of choosing the correct τ_s value for a $10^{12}/cm^2$ -eV density and unknown distribution in the band gap, it is preferred to choose τ_s in such a way as to obtain the best fit to the observed efficiency of $\eta \simeq 0.90$. Before proceeding, however, it is important to note that the loss $F_{loss}(t, \tau_s)$ is less — at each τ_s value and frequency — for the 0.5-mil device than the 1-mil device. This fact emphasizes the reduction in interface state trapping that can be achieved by reducing the gate lengths.

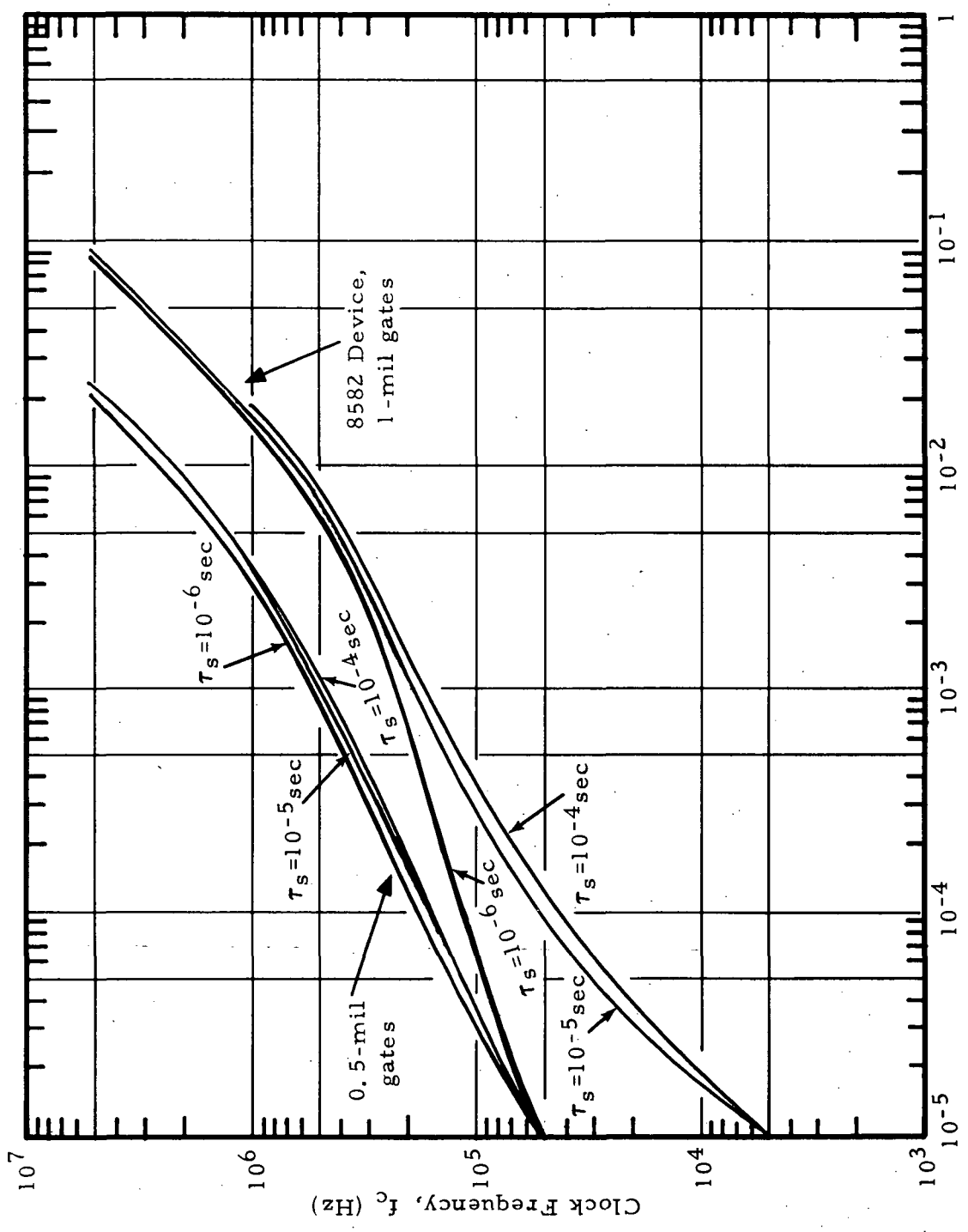


Figure 5-2. Mobile Charge Loss/Transfer [F (t, τ_s)] for 1-mil Gate (8582) and 0.5-mil Gate Devices as a Function of Effective Time Constant (τ_s) for Interface States (no fringe field)

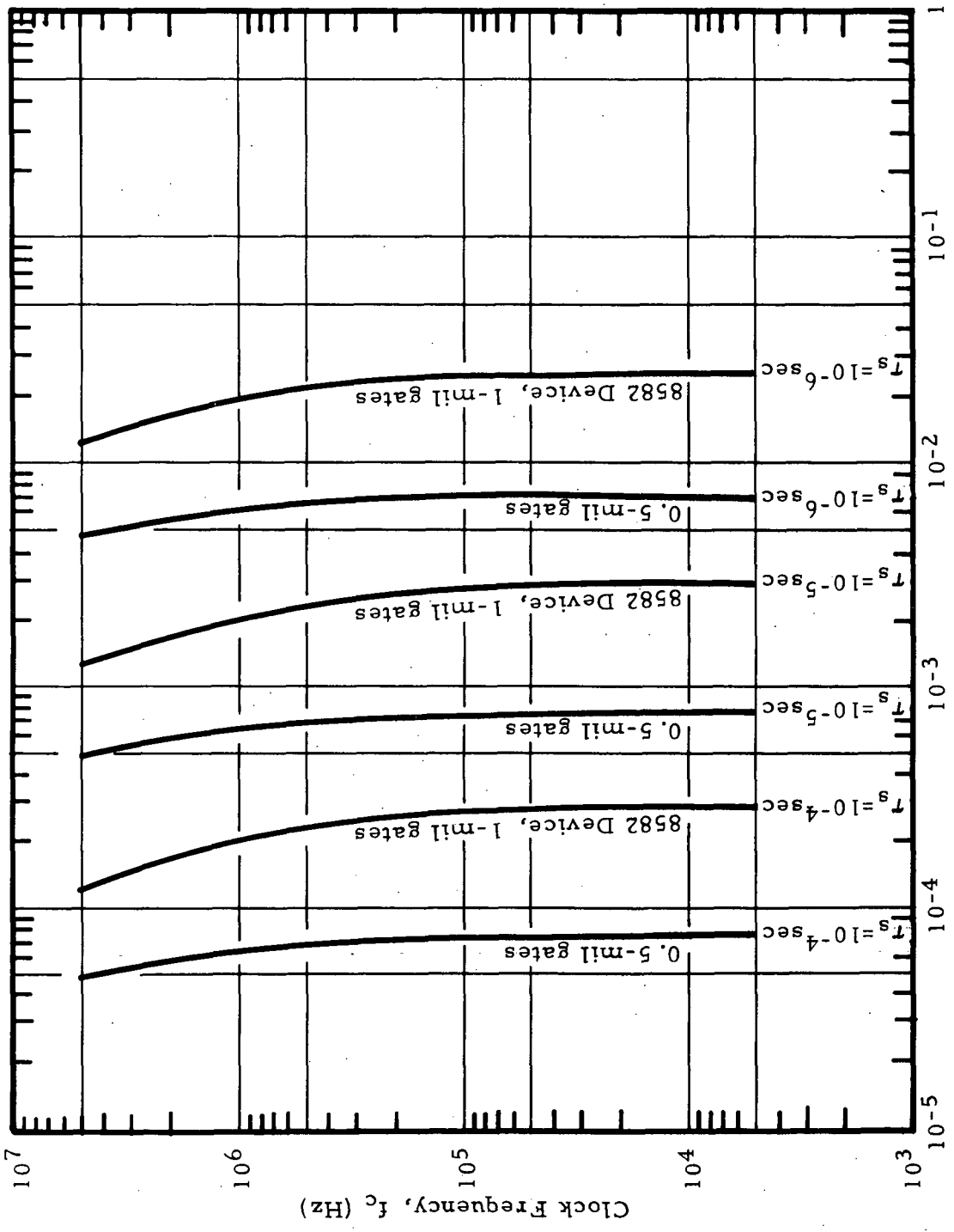


Figure 5-3. Charge Loss/Transfer to Interface States $[F_{loss}(t, \tau_s)]$ for 1-mil Gate (8582) and 0.5-mil Gate Devices as a Function of Effective Time Constant (τ_s) for Interface States (no fringe field)

To obtain a best fit with the observed $\eta = 0.90$ value, a series of computations was carried out for the 8580 device structure operating in the two-phase mode. Using values of $\Delta V = 2$ volts (maximum possible in 8580 device) and $f_c = 5$ kHz, a value of $\tau_s = 5 \times 10^{-6}$ sec was obtained. This result for τ_s was then applied to the 8582 1-mil structure, as well as to projected 0.5-mil and 7.5-μm structures (all lengths refer to gate lengths). The results of these calculations are summarized in Table 5-2.

Table 5-2. Transfer Efficiency Versus Gate Length for 5-kHz Clock Frequency

$F(t, \tau_s)$	$F_{loss}(t, \tau_s)$	η	Gate Length	Device
1.3×10^{-12}	0.11	0.894	2.5/1.5 mil	8580
2.3×10^{-18}	3.4×10^{-2}	0.966	1.0 mil	8582
5.9×10^{-40}	9.64×10^{-3}	0.990	0.5 mil	Projected
--	9.1×10^{-4}	0.999	7.5 μm	Projected
$t = 1/2\ f_c$; $f_c = 5$ kHz; $\tau_s = 5 \times 10^{-6}$ sec; no fringe field				

This table gives the improvement expected in shorter gate-length devices based on the 8580 device results, and the interface characteristics resulting from present processing procedures. Since continued effort to reduce the interface states is planned, the interface state loss factors may be reduced; Table 5-2 should not be construed as giving ultimate performance limits for InSb CCDs. Moreover, future analytical and experimental work will improve the device modelling and expand on the knowledge of the interface states so that more quantitative calculations can be made.

The results of this preliminary analysis, to be expanded and confirmed by future analytical work, are:

1. Transfer efficiencies of the current devices are limited by an interface state density of $\sim 10^{12}/cm^2$ -eV.

2. Significant improvement in transfer efficiency is predicted for future devices with decreased gate lengths, for the same interface conditions. Reducing gate length has the effect of decreasing interface trapping and also decreasing time required to empty the wells.

3. Improved transfer efficiency can be obtained by increasing charge handling capability of the device (i.e., ΔV); reducing substrate impurity concentration on future devices will accomplish this.

As a final note, fringe fields have been assumed to be absent in all the foregoing calculations. Experience with silicon CCDs has demonstrated that by designing the devices to be fringe-field limited, rather than diffusion-limited, the speed of device operation and the transfer efficiency is significantly increased. A sample calculation for an InSb CCD was carried out using the Lee and Heller model and assuming a very small fringe field of 10 v cm^{-1} to investigate the magnitude of the effect. The mobile charge loss $F(t, \tau_s)$ was found to decrease dramatically (~40 orders of magnitude) and the interface state loss $F_{loss}(t, \tau_s)$ about 25% compared to the diffusion-limited values. The larger values of fringe fields which would be obtained in actual devices designed to be fringe-field limited would result in further efficiency improvements. Future work is planned to determine the fringe fields present in the InSb CCD designs.

Section 6
SYSTEMS APPLICATIONS OF InSb CCDs

POTENTIAL APPLICATIONS

There are several applications in the fields of remote sensing of the earth and planetary exploration for which InSb CCD monolithic focal plane arrays are potentially useful. One particularly important advanced focal plane concept that could be implemented with InSb CCDs is the time delay and integration (TDI) readout technique. A partial list of space applications which could utilize InSb CCD arrays using TDI to give significant performance advantages is given below. This list is not all-inclusive, and many other NASA applications where near-infrared (1- to 5-μm) sensors are needed would undoubtedly benefit from implementation of these monolithic arrays.

1. Forest Fire Surveillance and Mapping

   This is an especially well adapted application since the blackbody radiance peak of a typical forest fire is well matched to the InSb spectral responsivity.

2. Atmospheric Temperature Sounding in 4.3-μm CO_2 Band

   Improved meteorology and weather forecasting requires that the atmospheric temperature profile of regions of interest be available on a repetitive basis; both the 4.3-μm band (accessible with InSb) and the 15-μm CO_2 bands are suitable for this function.

3. Pollution Monitoring

   Most pollutants of concern have strong signatures in the near infrared making this a promising applications area.

4. Geology

   As an example, for mineral exploration the presence of hydrated iron oxides and clays (products of hydrothermal alteration) are useful secondary indicators, and experimental data indicate that spectral bands at 1.3, 1.6, and 2.2 μm provide the best amplitude discriminant bands.

5. Distinguishing Between Clouds and Water Surfaces

   Since the maximum difference between cloud and water surface emittance occurs near 4 μm, mapping in the 3.6- to 4.1-μm atmospheric window would provide a means to estimate fractional cloud cover.

6. Missions to Comets

A major scientific question in cometary astrochemistry is to identify parent compounds present in comets with the near infrared a logical measurement region.

TIME DELAY AND INTEGRATION (TDI)

The principle of TDI is illustrated in Figure 6-1. The functional unit of a focal plane array utilizing TDI is a linear subarray of N detectors aligned in the direction of image motion as shown in the figure. The signals from the detectors are input to a CCD shift register and shifted along the CCD in synchronism with the target motion along the subarray so that the individual detector signals are added in the register. The signal at the CCD output is in the ideal case a factor of N larger than that from each detector, while the rms output noise is increased by $\sqrt{N}$ over that of an individual detector for the photon noise limited case. The signal-to-noise ratio (SNR) is consequently increased by the factor $\sqrt{N}$, with no increase in bandwidth, over that of an individual detector element.

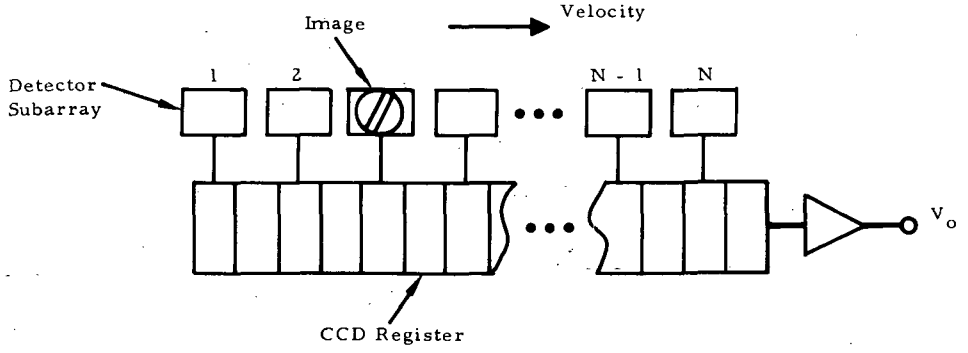


Figure 6-1. Time Delay and Integration of Infrared Detector Signals

In this concept, several columns of N-element subarrays are fabricated monolithically on one semiconductor chip (e.g., InSb) to form a focal plane array. A single large monolithic chip may satisfy some system requirements; others may require the assembly of several such (identical) chips on the focal plane depending on field of view (FOV) and other factors.

A major feature of TDI processing is a resultant improvement in array uniformity, which is a significant factor in infrared imaging. A basic difference between the visible and infrared spectral bands is the low scene contrast in the latter. For example, in the 3- to 5-μm spectral band, the scene contrast is approximately 3.7% per degree centigrade for a 300°K background. Since system requirements usually specify a distinguishable temperature difference of <1°C, stringent uniformity specifications are placed on the detector arrays. Since TDI averages (approximately) the responsivity of the individual detectors in the subarray, the uniformity between subarrays is improved.

TDI processing of InSb detector signals with background photon-limited performance has been demonstrated using assemblies of photovoltaic InSb detector arrays and silicon CCD chips mated to each other by means of an advanced interconnection concept. The $\sqrt{N}$ SNR improvement was shown to be achievable in this development. The implementation of InSb CCD technology would enable fabrication of such focal planes in truly monolithic format, without the need for hybrid interconnection techniques.

EXAMPLE TDI FOCAL PLANE UTILIZING InSb CCDs

An example focal plane design is discussed in this section which uses InSb CCDs in a TDI configuration. The application selected for this example is to perform infrared imaging in the 3.6- to 4.1-μm spectral interval (an atmospheric window), such as would be required for mapping and/or forest fire surveillance. A medium altitude, polar orbit is assumed such as that of LANDSAT, formerly identified as the Earth Resources Technology Satellite (ERTS). Scanning in the perpendicular-to-track direction is used to obtain a 0.2-radian cross-talk swath width and implement TDI. Orbital and telescope parameters assumed are given in Table 6-1. A 90-μrad

IFOV was selected (assumed square) which represents excellent resolution in the infrared. (For comparison, the LANDSAT Multispectral Scanner achieves α = 86 μrad for the four short-wavelength spectral bands in this instrument.)

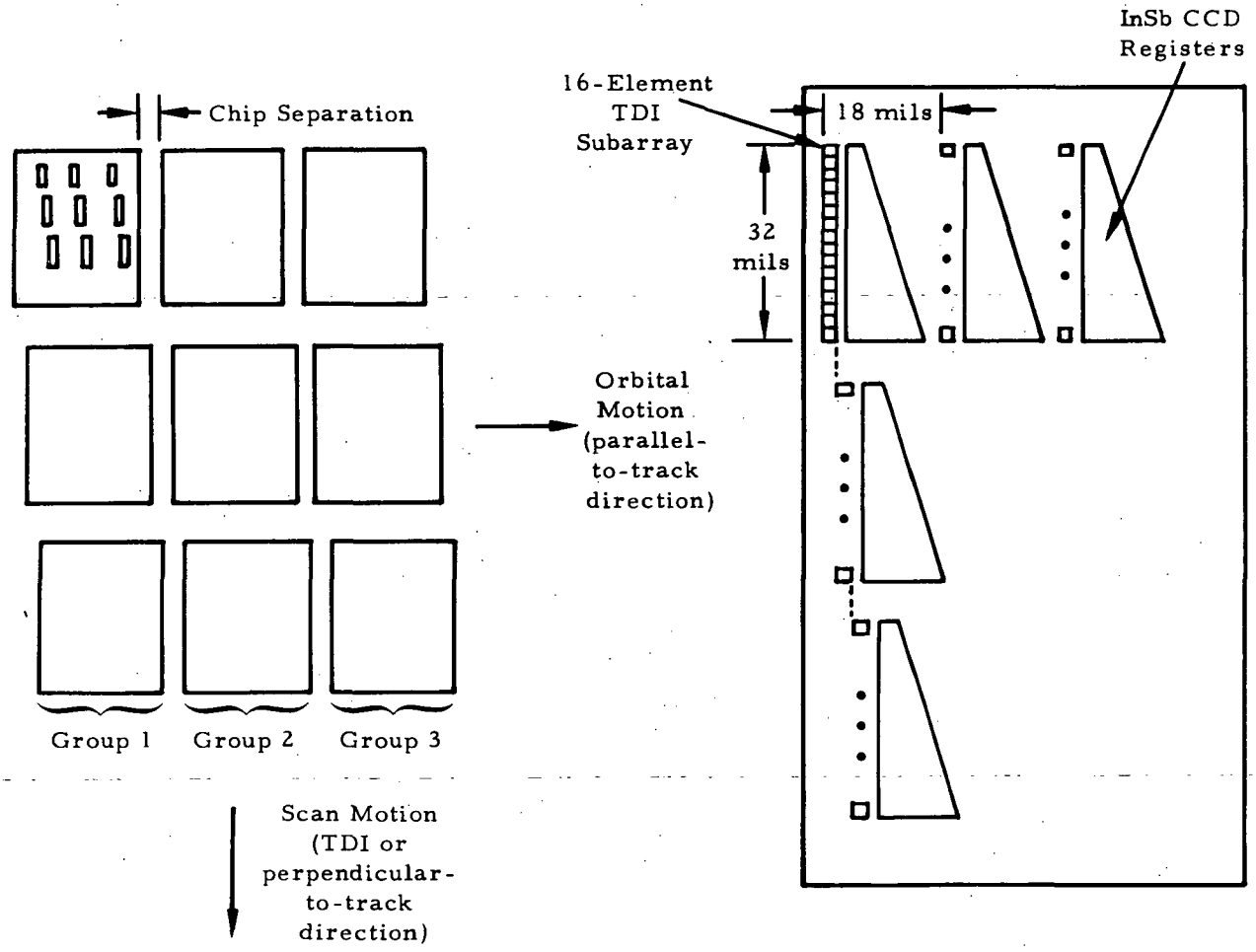
Table 6-1. Example System Parameters

Altitude of Orbit	H	925 km
Orbital Period	P_o	103.5 minutes
Cross-track Swath Width	$W_\perp$	0.2 rad
Instantaneous FOV (IFOV)	α	90 μrad
Telescope f-number	f/no.	f/4
Entrance Aperture Diameter	D	5 inches
Spectral Bandpass	$\Delta\lambda$	3.6 - 4.1 μm
Optics Transmittance	T_o	0.6
Scan Efficiency	k_s	0.4

A 16-element TDI subarray was chosen for the calculations to follow. This selection is not necessarily optimum but represents a good compromise between the subarray detectivity (SNR) improvement of $\sqrt{16} = 4$ in the ideal case, and the larger size and decreased yield associated with long CCD registers. Since the performance improvement is proportional to the square root of subarray length, relatively small gains are achieved by using numbers of detectors greater than about 30.

The focal plane organization is shown in Figure 6-2(a). Several chips are used to build up a focal plane of size determined by the integration time, sensitivity, and FOV desired. The organization assumed for each chip is shown in Figure 6-2(b). Each chip contains 144 detectors, or nine TDI subarrays of 16 elements each. The nine subarrays are aligned with the perpendicular-to-track direction and offset with respect to each other in the parallel-to-track direction as shown in the figure. With this arrangement

and particular dimensions assumed in this example, three chips arrayed in the perpendicular-to-track direction [denoted as a group in Figure 6-2(a)] are required to "fill in" the scan pattern and provide contiguous sampling in the along-track direction. Several groups [three shown in Figure 6-2(a)] may be added as required. These groups may be identical or may perform different functions; for example, each group may be used to sample a different spectral band.



(a) Focal Plane Organization

(b) Chip Organization

Figure 6-2. Example InSb CCD Focal Plane

The configuration of each subarray is shown in Figure 6-3. For the focal length and IFOV in Table 6-1, the detector size is 1.8 mils square. The detectors are laid out with pitch p = 2.0 mils. The CCD register is tapered to accommodate the accumulated charge and so as to maintain a relatively constant fat zero in each bit of the CCD.

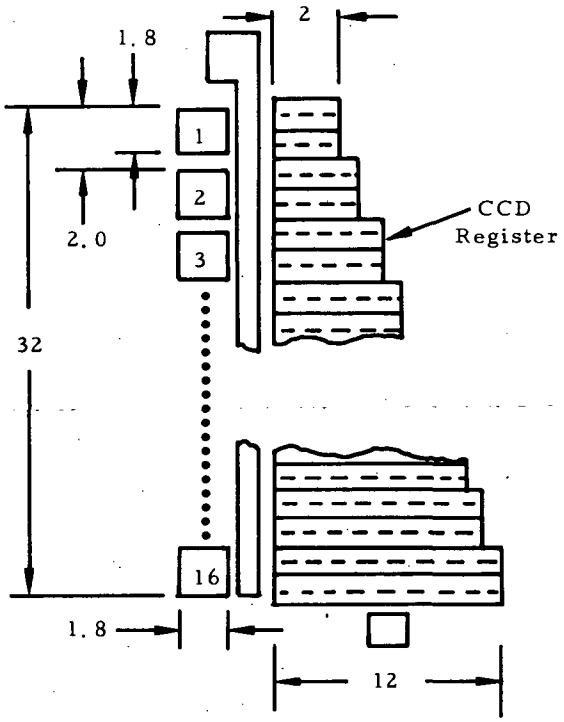


Figure 6-3. TDI Subarray Configuration

Using the system parameters defined in Table 6-1, the number of detectors required to achieve a given signal integration time per sample may be determined as follows. Since the satellite velocity with respect to the earth's surface is $2\pi R_e/P_o$, where R_e is the radius of the earth = 6.37×10^3 km, the satellite moves forward an IFOV $\alpha_{||}$ in $t_{||} = \alpha_{||} H P_o / 2\pi R_e$ seconds. For a swath width of $W_\perp$ radians, the dwell time per IFOV for a single detector is then $t_D = t_{||}\alpha_\perp / W_\perp = \alpha_{||}\alpha_\perp H P_o / 2\pi R_e W_\perp$. Since square detectors have been assumed here, $\alpha_{||}\alpha_\perp = \alpha^2$. For multiple detectors in TDI then

$$t_D = \frac{n_{||} n_{\perp} \alpha^2 H P_o k_s}{2\pi R_e W_{\perp}} \tag{6-1}$$

where

$n_{||}$ = number of detectors in the parallel-to-track direction

$n_{\perp}$ = number of detectors in the perpendicular-to-track direction = 16

and where the scan efficiency, k_s, has been introduced. If the detectors are sampled n_s samples per dwell time, then the integration time is

$$t_{INT} = \frac{n_{||} n_{\perp} \alpha^2 H P_o k_s}{2\pi R_e W_{\perp} n_s} \tag{6-2}$$

For the array assumed in Figure 6-3, $n_s = n_b W/P \simeq 1$, where n_b = number of CCD bits per detector = 1, and W is the detector width. This represents the Nyquist minimum sampling rate; although this would give rise to some aliasing resulting from inadequate along-scan spatial sampling, this choice is sufficient for the example calculation carried out here. The determination of sampling rate is addressed in detail when a specific system is designed, and is usually selected to compromise between frequency response requirements and the necessity to minimize telemetry rates in most cases. The sampling rate may be increased by increasing the number of CCD bits per detector. Substituting the parameters of Table 6-1 into equation 6-2 yields:

$$t_{INT} = (2.58 \times 10^{-6})\, n_{||} n_{\perp} \text{ (sec)} \tag{6-3}$$

In TDI, the CCD clock frequency is related to the integration time by

$$f_c = \frac{1}{t_{INT}} \tag{6-4}$$

Using equations 6-3 and 6-4, the cases listed in Table 6-2 can be considered for the example system. Other factors being equal, the longest possible integration time is desired. Case 3 is a reasonable compromise between array size and t_{INT}. The clock frequency is sufficiently high to avoid a large dark current charge in the register, and the size of the focal

plane is compatible with the imaging capability of the optics. The 27 TDI subarrays of Case 3 correspond to the three CCD chips shown as Group 1 in Figure 6-2(a).

Table 6-2. Possible Configurations for Sample System

Case	Number of TDI Subarrays $n_{\|\|}$	Total Number of Detectors	t_{INT}	f_c
1	1	16	41 μs	24 kHz
2	3	48	124 μs	8 kHz
3	27	432	1.1 ms	900 Hz
4	81	1,296	3.3 ms	300 Hz

The performance of the focal plane of Case 3 may be estimated by consideration of the noise sources and responsivity expected in the TDI subarray, leading to calculation of detectivity (D*) and the noise equivalent temperature difference (NEΔT), which is the principal performance parameter of a thermal imaging system. The parameters used in the calculation are shown in Table 6-3.

Table 6-3. InSb Detector/CCD Parameters

Number of Detectors in TDI	N	16
Detector Area	A_D	2.1×10^{-5} cm^2
Background Photon Flux	Q_B	8×10^{13} phot sec^{-1} cm^{-2}
Quantum Efficiency	η	0.5
CCD Clock Frequency	f_c	900 Hz
CCD Bit Length	L	2 mils
Bit Area (average)	$\bar{A}_B$	9×10^{-5} cm^2
Thin Oxide Capacitance	C_o	4×10^{-8} f cm^{-2}
Clock Voltage	V	5 V
Dark Current	J_D	0.25 μa cm^{-2}
Interface State Density	N_{SS}	10^{12} cm^{-2} eV^{-1}
Output Capacitance	C_{out}	5 pF
Temperature	T	80°K

The background photon flux at the focal plane establishes the fat zero charge in the CCD register as well as the photon noise contribution to the device output noise. The array is assumed to be cold-shielded as is required in most high-performance infrared sensors. The effective cold shielding solid angle is dependent on the size of the focal plane array and the location and configuration of the cold stop; for the purposes of this example, an effective f/2 solid angle was assumed for the cold shield, which is representative of what can be achieved in actual systems. For an ambient instrument and scene temperature of 295°K, the background flux at the focal plane is calculated using:

$$Q_B = \frac{\tau\, Q_{\Delta\lambda}}{4\,(\text{f/no.})^2_{EFF}} \tag{6-5}$$

where $Q_{\Delta\lambda}$ is the radiant photon emittance of the background in the bandwidth $\Delta\lambda$, $Q_{\Delta\lambda} = 1.36 \times 10^{15}$ photons $\text{sec}^{-1}\ \text{cm}^{-2}$, and τ is the transmittance of the bandpass filter and other cooled optical elements over the focal plane $\cong 0.95$. Equation 6-5 then gives

$$Q_B = 8 \times 10^{13} \text{ photons sec}^{-1}\ \text{cm}^{-2}$$

The integrated number of background charges per detector is

$$N_B = \eta\, Q_B\, A_D\, T_c \tag{6-6}$$

$$= 9.32 \times 10^5 \text{ charges}$$

The summed charge at the output of the CCD is then

$$N_{BT} = N\eta\, Q_B\, A_D\, T_c \tag{6-7}$$

$$= 1.5 \times 10^7 \text{ charges}$$

The CCD storage capacity is designed to maintain a relatively constant fat zero in the tapered register. The well capacity per unit area is given by

$$\frac{N_{MAX}}{A} = \frac{C_o V}{e} = 1.25 \times 10^{12} \text{ charges cm}^{-2} \tag{6-8}$$

Considering the last (16th) bit of the device, the required area of this bit is then:

$$A_B\,(16) = \frac{4N_{BT}}{(0.3)\,(N_{MAX}/A)} \qquad (6\text{-}9)$$

$$= 1.6 \times 10^{-4}\ \text{cm}^2$$

where we have assumed a 30% fat zero level at the output and a storage area = 1/4 A_B, where A_B is the total bit area. Here and throughout the calculations, a two-phase, stepped-oxide CCD structure is considered with 1/2-mil gate length, or total bit length of 2 mils. From equation 6-9 the required width of the last bit is 12 mils. The CCD is tapered to 2 mils at the first bit (n = 1).

Next, the charge due to dark current is considered. The dark charge generated in each detector is given by

$$N_D = \frac{J_D\, A_D\, T_c}{e} \qquad (6\text{-}10)$$

where J_D is the dark current density. Dark current densities have been determined experimentally from measurements of storage time in InSb MIS samples. The storage time is proportional to the quantity of stored charge and inversely related to the average dark current, i. e.,

$$\tau_s \cong \frac{Q_p}{J_g} \cong \frac{C_o \Delta V}{J_g} \qquad (6\text{-}11)$$

For witness devices from the 8580 CCD wafers measured during this program, with $C_o = 3 \times 10^{-8}$ f cm^{-2} and $\Delta V = 2$ V, storage times of up to 500 msec have been measured. From equation 6-11, then $J_g \cong 0.12$ μa cm^{-2}. For a more conservative estimate, we take $\tau_s = 250$ msec, or $J_g \cong 0.25$ μa cm^{-2}. Using this latter value in equation 6-10, the dark charge generated per detector is $N_D = 3.6 \times 10^4$ charges, and the total at the register output is $N_{DT} = 5.8 \times 10^5$ charges. This is less than 5% of the summed background charge.

The dark charge generated in the CCD may be determined similarly. It is given approximately by

$$N'_{DT} = \frac{N J_D \overline{A}_B}{2ef_c} \qquad (6\text{-}12)$$

yielding $N'_{DT} = 1.25 \times 10^6$ charges. This is about 8% of the total background charge.

The predicted noise voltage spectrum may be calculated from the known background and dark charge levels, the interface state density, and other parameters. The noise spectral density of Si CCD devices has been extensively studied, with particular regard to readout of infrared detectors with these devices.[7] The principal sources of noise in the 16-element TDI subarray considered here are expected to be: 1) photon noise in the infrared background flux; 2) shot noise in the dark current; 3) fast interface state (FIS) noise in the InSb CCD; and 4) 1/f noise in the output circuit.

Photon noise is due to the random emission rate of background photons and determines the limiting noise for any infrared detector. When a detector is limited by photon noise, it is said to be operating under background limited infrared photodetector (BLIP) conditions. Photon noise is a Poisson process so that the variance in the average number of carriers is that average number; i.e., the variance in the background charge at the CCD output is:

$$\overline{N_p^2} = N\eta Q_B A_D T_c \qquad (6\text{-}13)$$

The rms carrier fluctuation due to the infrared background is then, from the result of equation 6-7, $N_p = 3900$ charges. Note that this is a large number relative to the typical silicon CCD noise electron counts (~100), a result of the large background flux present in the infrared and the TDI summing process.

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[7] D. M. Erb and K. Nummedal, Proceedings of CCD Applications Conference, NELC, San Diego, California, p. 157, September 1973.

A number of noise sources become negligibly small compared to N_p, for example, the noise of the reset output circuit

$$\overline{N_o^2} = \frac{kTC_{out}}{e^2} \tag{6-14}$$

gives N_o = 465 charges even for the large output capacitance used in this example, C_{out} = 5 pF.

The noise spectral density is determined from the variance by

$$V_n^2(f) = \frac{2e^2\overline{N^2}}{f_c C_{out}^2} F(f)\, G(f) \tag{6-15}$$

where $V_n(f)$ is the output noise voltage in volts/$\sqrt{Hz}$, F(f) a correlation function describing the correlation in the charge fluctuation, and G(f) the transfer function of the output integrator. For photon noise F(f) = 1, and assuming a sample-hold circuit which holds the sampled signal for a time $\simeq T_c$, equations 6-13 and 6-15 may be combined to give

$$V_p \cong \frac{e}{f_c C_{out}} \left(2N\eta\, Q_B\, A_D\right)^{1/2} \frac{\sin(\pi f T_c)}{(\pi f T_c)} \tag{6-16}$$

The result for the example design parameters is plotted in Figure 6-4. The sin x/x rolloff as $f \rightarrow f_c$ is due to the inherent CCD sampling process.

Dark current, similar to the photon case, produces shot noise with variance

$$\overline{N_D^2} \cong \frac{NJ_D}{ef_c}\left(A_D + \frac{\overline{A_B}}{2}\right) \tag{6-17}$$

The resulting spectrum of thermal generation noise V_D is shown in Figure 6-4.

Fast interface state noise is due to random filling and emptying of interface states as the charge packets transfer down the CCD register.[8] This source will be an important contribution to the InSb CCD noise because of

[8] J. E. Carnes and W. F. Kosonocky, RCA Review 33, 327 (1972).

the higher interface state densities currently characteristic of these devices compared to silicon CCDs.

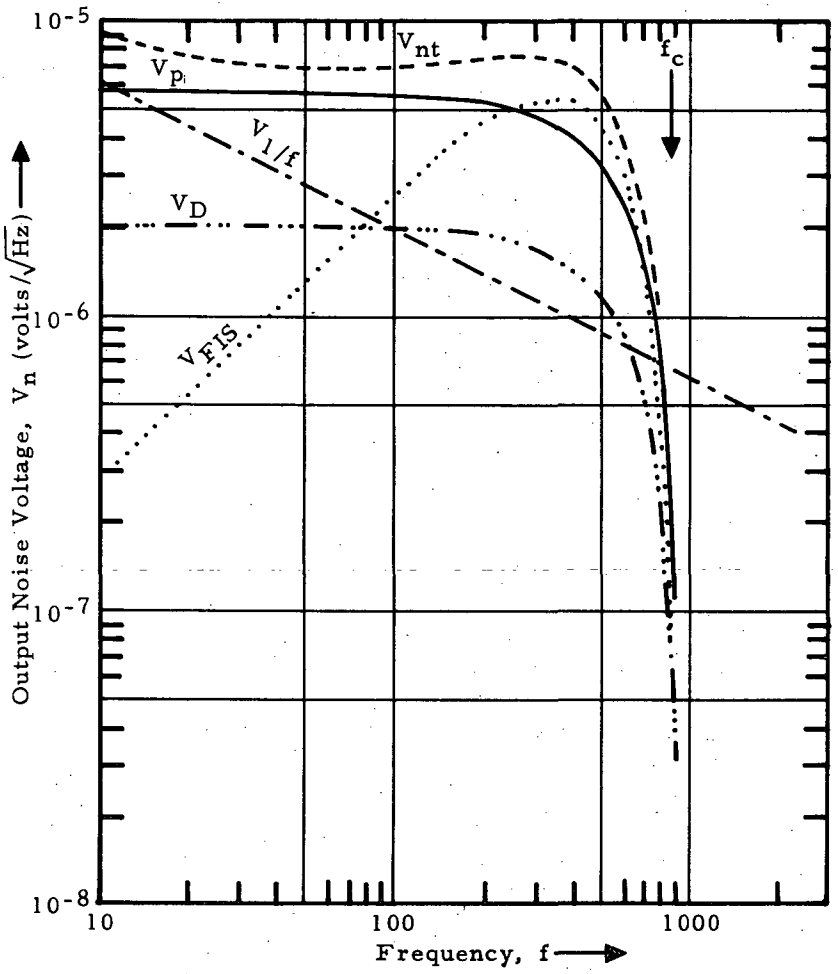

Figure 6-4. Calculated Noise Spectral Density for Example Design

The variance due to FIS noise is given by

$$\overline{N_{FIS}^2} = 2\ell n2kTAN_{SS}PN_B \qquad (6\text{-}18)$$

$$= 2.8kTAN_{SS}N$$

where k is Boltzmann's constant = 8.62×10^{-5} eV/°K, A = 1/2 CCD bit area, N_{SS} = interface state density in states cm^{-2} eV^{-1}, P is the number of phases = 2, and N_B the number of bits = N. In the case of FIS noise, the

quantity of noise charge added to a given charge packet is highly correlated with that in the preceding and following packets with correlation function $F(f) = 2\sin^2(\pi f T_c)$. From equations 6-18 and 6-15, one obtains

$$V_{FIS} = \frac{e}{f_c C_{out}} (5.6kTAN_{SS}Nf_c)^{1/2} [1 - \cos(2\pi f T_c)]^{1/2} \frac{\sin(\pi f T_c)}{(\pi f T_c)} \quad (6\text{-}19)$$

For $N_{SS} = 10^{12}$ cm^{-2} eV^{-1} and the other parameters as previously defined, $V_{FIS}(f)$ is plotted in Figure 6-4. The FIS noise is seen to peak at the Nyquist frequency = $f_c/2$ and become negligibly small at lower frequencies.

A final noise source considered here is output amplifier 1/f noise. A reset output circuit fabricated on silicon chips mounted adjacent to the InSb chips is assumed. An empirical fit to the observed 1/f noise component on existing Si reset outputs is given by

$$V_f = V_o/\sqrt{f}, \quad V_o = 20\ \mu V \quad (6\text{-}20)$$

where V_f is the output noise voltage in volts/$\sqrt{Hz}$. This is plotted as a fourth noise component in Figure 6-4.

The sum of the photon, thermal generation, FIS, and 1/f noise components is plotted as V_{nT} in Figure 6-4.

A figure-of-merit commonly used to characterize infrared detectors is the detectivity (D*), a normalized signal/noise ratio defined by[9]

$$D^* = \left(\frac{\Delta f}{A_d}\right)^{1/2} \frac{V_s}{H_d V'_{nT}} \text{ cm (Hz)}^{1/2} \text{ watt}^{-1} \quad (6\text{-}21)$$

where Δf is the equivalent noise bandwidth, H_d the rms signal irradiance, and V_s and V'_{nT} the detector rms signal and noise voltage in bandwidth Δf, respectively. For the present case, the cumulative D* of each signal channel can be expressed as:

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[9] R. D. Hudson, Jr., "Infrared System Engineering," Wiley-Interscience, New York, 1969.

$$D^*_\lambda(f) = \frac{(A_d)^{1/2} R_\lambda N |Z_s(f)|}{V_{nT}(f)} \qquad (6\text{-}22)$$

where:

$R_\lambda = \frac{e\lambda\eta}{hc}$ = single detector spectral responsivity, amps/watt

$|Z_s(f)| \cong (f_c C_{out})^{-1} \frac{\sin(\pi f T_c)}{(\pi f T_c)}$ = CCD transfer function

$V_{nT}(f)$ = total output noise spectral density at frequency f

λ = wavelength, μm

hc = 1.99×10^{-23} joule-cm

Consider first the photon noise limit (BLIP) in the low frequency limit, for $\lambda = 4$ μm. Then from the above and equation 6-16:

$$R_\lambda = 1.61 \text{ amps/watt}$$
$$|Z_s(0)| = 2.22 \times 10^8 \ \Omega$$
$$V_p(0) = 5.83 \times 10^{-6} \text{ V}/\sqrt{\text{Hz}}$$

giving a cumulative BLIP $D^*_\lambda = 4.5 \times 10^{12}$ cm $(\text{Hz})^{1/2}$ -watt^{-1}. Because of the other noise sources present in the device, D* is slightly lower than BLIP. From Figure 6-4, D* peaks in midband, about 70 Hz, where $V_{nT} = 6.76 \times 10^{-6}$ V/$\sqrt{\text{Hz}}$ giving

$$D^* (4\ \mu\text{m},\ 70\ \text{Hz},\ \text{TDI}) = 3.88 \times 10^{12} \text{ cm } (\text{Hz})^{1/2} \text{ watt}^{-1} \qquad (6\text{-}23)$$

which is 85% of the cumulative BLIP limit for a detector quantum efficiency of $\eta = 0.5$. The increased performance of the TDI processing is seen by comparing this result with the BLIP limit for a single detector of similar A_d and η under the same background conditions:

$$D^*_\lambda (\text{BLIP, Single Detector}) = \frac{\lambda}{hc}\left(\frac{\eta}{2Q_B}\right)^{1/2} \qquad (6\text{-}24)$$

$$= 1.12 \times 10^{12} \text{ cm } (\text{Hz})^{1/2} \text{ -watt}^{-1}$$

Comparing equation 6-23 to equation 6-24 shows a factor of 3.5 sensitivity improvement or close to the ideal $\sqrt{16} = 4$ improvement possible with TDI.

Finally, the noise equivalent temperature difference NEΔT of the example sensor may be calculated. The NEΔT is defined as that value of scene temperature difference that will generate a detector signal equal to the total output noise voltage of the signal channel. It is given by:

$$NE\Delta T = \frac{4\,(A_d \Delta f)^{1/2}}{\alpha^2 D^2 \int_{\lambda_1}^{\lambda_2} \frac{\partial W(\lambda)}{\partial T}\, D^*_\lambda\,(f_o)\, T_o(\lambda)\, T_a(\lambda)\, d\lambda} \qquad (6\text{-}25)$$

where:

Δf = equivalent noise bandwidth of signal channel, Hz

$W(\lambda)$ = spectral emittance of extended area target, watts/cm^2 μm

$D^*_\lambda(f_o)$ = spectral detectivity at frequency f_o

$T_a(\lambda)$ = atmosphere transmittance

and the other parameters have been defined previously. For simplicity in the example, averages over the spectral bandpass are used, resulting in:

$$NE\Delta T \cong \frac{4\,(A_d \Delta f)^{1/2}}{\alpha^2 D^2 \overline{D^*_\lambda\,(f_o)}\;\overline{T_o(\lambda)}\; W'} \qquad (6\text{-}26)$$

where $W' = \int \left[\partial W(\lambda)/\partial T\right] d\lambda$ watts/cm^2 °K, and where it has been assumed $T_a(\lambda) \cong 1$. The equivalent noise bandwidth is found from the total noise spectrum of Figure 6-4.

$$\Delta f = \frac{\overline{V^2}}{\overline{V_{nT}{}^2\,(f_o)}} \qquad (6\text{-}27)$$

where V^2 is the total output noise and $V_{nT}{}^2(f_o)$ is the noise spectral density at frequency f_o. Taking $V_{nT} = 6.76 \times 10^{-6}$ V/$\sqrt{\text{Hz}}$ at $f_o = 70$ Hz, Δf is found to be 541 Hz. Then using

$$\overline{D^*_\lambda(f_o)} = 3.74 \times 10^{12}\ \text{cm}\ (\text{Hz})^{1/2}\ \text{-watt}^{-1}$$

$$\bar{\lambda} = 3.85\ \mu\text{m},\ f_o = 70\ \text{Hz}$$

and $W' = 2.75 \times 10^{-6}$ w/cm^2 °K for T = 295°K and a 3.6- to 4.1-μm bandwidth, equation 6-26 yields

$$NE\Delta T = \frac{4\,(2.1 \times 10^{-5})^{1/2}\,(541)^{1/2}}{(9 \times 10^{-5})^2\,(12.7)^2\,(3.74 \times 10^{12})\,(0.6)\,(2.75 \times 10^{-6})}$$

$$= 0.053\ ^{\circ}K$$

This is an excellent NEΔT and demonstrates the level of thermal imaging performance that is predicted for future sensors using InSb CCDs for on-focal-plane TDI.

Some assumptions have been made to simplify the mathematical complexity of the calculations used in this section, but the assumptions do not significantly affect the magnitude of the results. First, noise folding has not been incorporated in the noise spectra, which increases the total noise for frequencies near f_c. Second, the effects of transfer inefficiency have been neglected. Charge from the i^{th} detector undergoes 2i transfers to reach the register output, so that the relative responsivity of the i^{th} detector is $R_i = (i - \epsilon)^{2i}$ where ϵ is the inefficiency per transfer. Calculations in Section 5 showed that $\epsilon \leq 0.01$ is anticipated for 0.5-mil gates at a 5-kHz clock frequency, assuming the present interface conditions; at 900 Hz, ϵ would be lower. Using $\epsilon = 0.01$, the cumulative responsivity of a subarray with i = 16 would be 0.85 of the ideal responsivity. NEΔT would, therefore, be increased to about 0.06°K, assuming no change in the output noise of the device.

Incorporation of inefficiency effects in the noise and responsivity formulation is planned in future efforts. Another effect of transfer inefficiency is to give rise to inter-element crosstalk within each subarray. For the configuration considered in this example, the principal crosstalk term will be proportional to ϵ. It can be shown that by increasing the number of CCD bits per detector to two, crosstalk is substantially reduced, with the principal crosstalk term proportional to ϵ^2.

The example focal plane discussed in this section has shown the potential utility of InSb CCDs in a TDI application. These calculations indicate that cumulative detectivities in the 10^{12} cm $(Hz)^{1/2}$ watt^{-1} range and NEΔTs $< 0.1^{\circ}C$ are attainable with the InSb CCD technology.

Section 7
CONCLUSIONS

An InSb charge-coupled device has been successfully developed in this program. The demonstration of charge-coupling in InSb represents an important advance in the technology of this narrow-bandgap semiconductor material. This development offers the potential of a future generation of 1- to 5-μm charge-coupled infrared imaging devices (CCIRIDs), wherein infrared detectors and CCD signal processing circuits are fabricated monolithically on the same InSb semiconductor chip.

Based on the results of this contract effort, the following conclusions may be made:

1. A process technology has been developed for fabricating the required multilayer metal-insulator structure on an InSb substrate to achieve a CCD device.
2. Multilayer MIS structures with up to seven metal-insulator levels, plus diffusions, have been achieved. Overlapping gate CCDs have been successfully processed which require step coverage over two buried metallizations as well as compound steps.
3. Critical metallization line widths of 1 mil with comparable spacing have been demonstrated on the 8580 CCD devices. Line widths and spacings of 0.5 mil and 0.25 mil, respectively, have been processed on the 8582 CCD mask.
4. MOSFETs fabricated in InSb as test devices have shown field-effect mobilities comparable to silicon MOS devices, ranging from 150 to 300 $cm^2\ V^{-1}\ sec^{-1}$ for the SiO_x insulator used in the present CCD structures.
5. Four-phase, overlapping-gate CCDs (8580 mask) with sixteen transfer gates (four bits) have been operated as shift registers with correctly delayed signals observed at the output.
6. Transfer efficiency of the 8580 CCDs has been measured to be approximately 85% to 90% per transfer at a 5-kHz clock frequency. This inefficiency is ascribed to the interface state density characteristic of the present devices ($\sim 10^{12}\ cm^{-2}\ eV^{-1}$) and long gate lengths on the 8580 mask design. Calculations indicate that, for the same interface conditions, transfer efficiencies of 0.99 or higher should be attainable on future devices with 0.5-mil gates.

7. An example focal plane design utilizing InSb CCDs in a 3.6- to 4.1-μm earth remote-sensing application illustrated the potential performance of these devices in a time delay and integration mode. A noise equivalent temperature of better than 0.1°C was calculated for the example design, indicative of the high performance predicted.

With continued development, InSb CCDs will provide an optimal solution to several types of 1- to 5-μm detection problems, particularly where high SNRs, maximum array uniformity, and low weight and power per signal channel are required — all typical requirements for NASA payloads.