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SOLID–STATE, X–BAND COMBINER STUDY

Final Report

O. Pitzalis, Jr. and K.J. Russell

August 1979

JPL Contract No. 955–223

Hughes Research Laboratories
3011 Malibu Canyon Road
Malibu, California 90265

This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, sponsored by the National Aeronautics and Space Administration under Contract NAS7–100.

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ABSTRACT

A study of the feasibility of developing solid-state amplifiers at 4 and 10 GHz for application in spacecraft altimeters is reported. Bipolar-transistor, field-effect-transistor, and IMPATT-diode amplifier designs based on 1980 solid-state technology are investigated. Several output power levels of the pulsed, low-duty-factor amplifiers are considered at each frequency. Proposed transistor and diode amplifier designs are illustrated in block diagrams. Projections of size, weight, and primary power requirements are given for each design.

INTRODUCTION

The need for small, lightweight, reliable, high-efficiency microwave power amplifiers for use in spacecraft radar-altimeter transmitters is the basis for investigating solid-state device alternatives to the beacon-magnetron tube. Pulsed power amplifiers for use in 4- and 10-GHz transmitters were studied. At the lower frequency, the most effective solid-state power amplifier would use bipolar transistors exclusively. At the X-band frequency, a 2-W, 33-dB-gain GaAs FET driver amplifier would be used with a multistage IMPATT-diode power amplifier. At both frequencies, projections for radar altimeter solid-state amplifier size, weight, and primary power requirements are developed for several output power levels chosen by JPL and HRL.

SECTION 1

THE 4-GHz RADAR ALTIMETER TRANSMITTER POWER AMPLIFIER

A. TRANSMITTER SYSTEM

The 4-GHz radar altimeter transmitter, illustrated in Figure 1, is planned for pulsed operation with chirp modulation. The surface acoustic wave (SAW) pulse-compression network produces a 6-MHz chirp modulation of the 200-MHz pulse source. The modulated 200-MHz pulses are mixed with the output from a 4.2-GHz frequency source to produce the desired 4-GHz chirp-modulated pulses at a peak power level of between 1 and 10 mW. The pulses are amplified by the solid-state amplifier. The circulator provides the amplifier with a low-VSWR load termination and provides a signal path from the spacecraft antenna to a switch (not shown) that engages the altimeter receiver between pulses.

The minimum signal-to-noise ratio (S/N) of 35 dB specified for the radar-altimeter system will be met with an average output power of 30 mW from the solid-state amplifier. In addition to a 30-mW average output, we have considered practical amplifier designs with average output power levels of 60 and 120 mW, which would improve system S/N by 3 and 6 dB, respectively.

The pulse sequence for the radar altimeter is shown in Figure 2. The transmitted output consists of pulse trains repeated every 550 msec. Each pulse train consists of 50 pulses spaced at 1-msec intervals for a total pulse train duration of $\sim$50 msec. The pulse width may be selected from a broad range of values to best utilize the characteristics of the solid-state amplifier.

The solid-state power amplifier could be designed with bipolar transistors or GaAs FETs or with a combination of transistors in the lower-power stages and IMPATT diodes in the higher-power stages. Transistors can be applied most effectively to this application using moderate peak powers at wide pulse widths. IMPATT diodes are limited to narrow pulse widths but are suitable for much higher peak power than are the transistors.

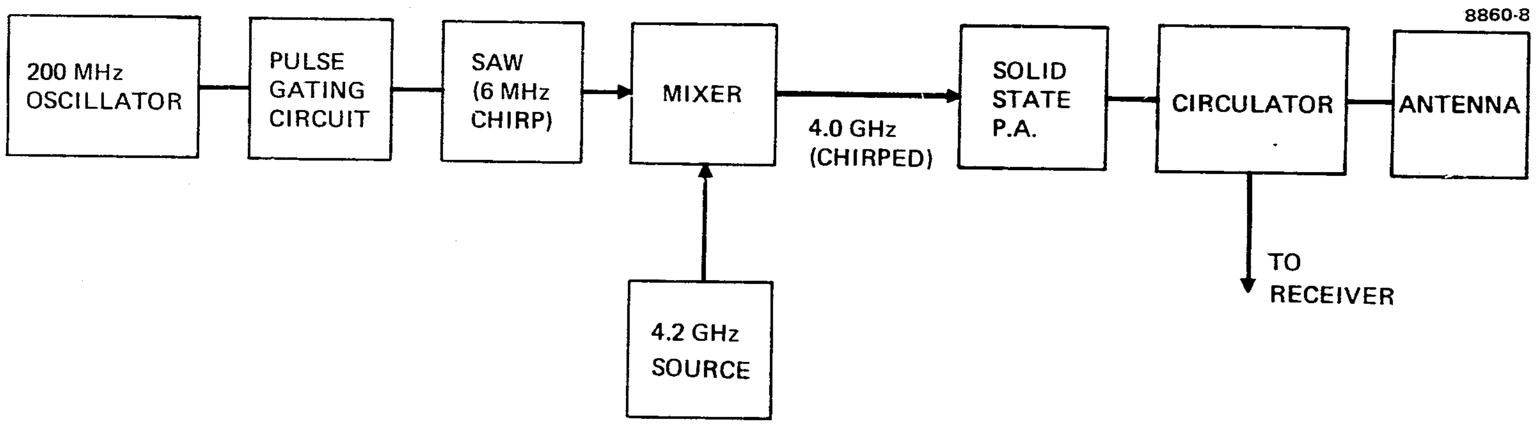

Figure 1. 4-GHz solid-state radar-altimeter transmitter.

B. BIPOLAR-TRANSISTOR POWER AMPLIFIER

1. General

A bipolar amplifier can best meet the transmitter amplifier average power requirements by operating with a modest peak power at a relatively large pulse width. In conformance with the pulse sequence shown in Figure 2, a 5-W peak power with 67-μsec-wide pulses would deliver the 30 mW of average power required for the amplifier. It is useful to consider increasing the peak power output to 10 and 20 W values. This would improve system S/N by 3 and 6 dB, respectively.

Bipolar power transistors are operable with class-C biasing, which results in negligible amplifier standby power consumption. Bipolar stages operating at approximately 200 mW and lower output powers require class-A or -AB biasing to have usable gain. Therefore, the lower power stages of the amplifier consume bias power during standby unless circuitry to remove bias power is provided.

2. Bipolar Transistors

The upper operating frequency limit for commercially available bipolar transistors is 4.2 GHz. The Nippon Electric Co. (NEC), currently the leading source, has a family of bipolar transistors with a range of peak power outputs from 1.6 to 5.0 W with typical operating efficiencies of 25%. The transistors are designed to meet the reliability requirements for space applications. A performance summary of the NEC family of transistors is given in Table 1.

Table 1. Power Bipolar Transistors for 4.0 GHz

Manufacturer	Device Type	Class of Operation	P_{out}, W	Power Gain, dB	V_{cc}, V
NEC	NE4205	C	5.0	4.0	20
NEC	NE4203	C	3.0	5.0	20
NEC	NE4201	C	1.4	7.5	20
HP	HXTR-5101	A	0.16	7.5	18

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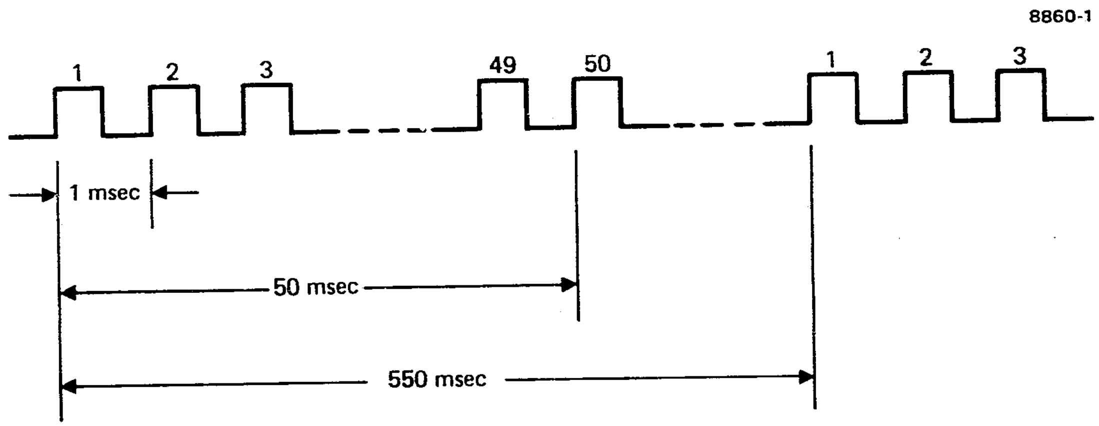

PULSE WIDTH: FIXED $\leqslant 67\ \mu$sec
PULSE TRAIN OF 50 PULSES; PRT = 1 msec
PERIOD OF PULSE TRAINS = 550 msec

Figure 2. 4-GHz radar-altimeter pulse timing diagram.

Microwave Semiconductor Corp. (MSC) also manufactures a family of 4.2-GHz power bipolars. Their highest power transistor, MSC 4003, is specified to deliver a 2.5-W minimum power output with 3 W specified as typical.

TRW Semiconductors has a developmental 6-W, 4.2-GHz bipolar power transistor which they intend to produce commercially within the next year.

Class-A biased transistors must be used in amplifier stages with outputs less than 200 mW. Hewlett Packard is the leading source of Class-A transistors for 4.0-GHz operation. The HXTR-5101, which is usable to 160 mW with 7.5 dB gain when operated at a quiescent bias of 30 mA from an 18-V supply, would be used in the proposed amplifier design.

3. Amplifier Designs

The transistors available from NEC permit designing a 10-W bipolar power amplifier by combining a pair of NE4205 transistors in the output stage. The 3-dB quadrature hybrids are used to combine pairs of transistors in the higher power stages. The hybrids provide interstage isolation which greatly improves the stability and pulse fidelity of cascaded class-C stages.

Figure 3 illustrates the proposed layout for a 10-W, 4-GHz bipolar power amplifier in which seven stages are used for 42 dB of power gain. The first three class-A stages provide 21 dB of gain and produce 76 mW of output power. All other stages operate with class-C bias. The last three stages use quadrature-hybrid combined pairs of transistors. The amplifier has isolator protection at the input and output. All transistors are operated conservatively within the manufacturer's specifications. The output stage NE4205 transistors are each indicated to deliver 5.6 W of output power. NEC advises that a power output of 6 W at 4 GHz is attainable by increasing the dc supply voltage to 26 V.

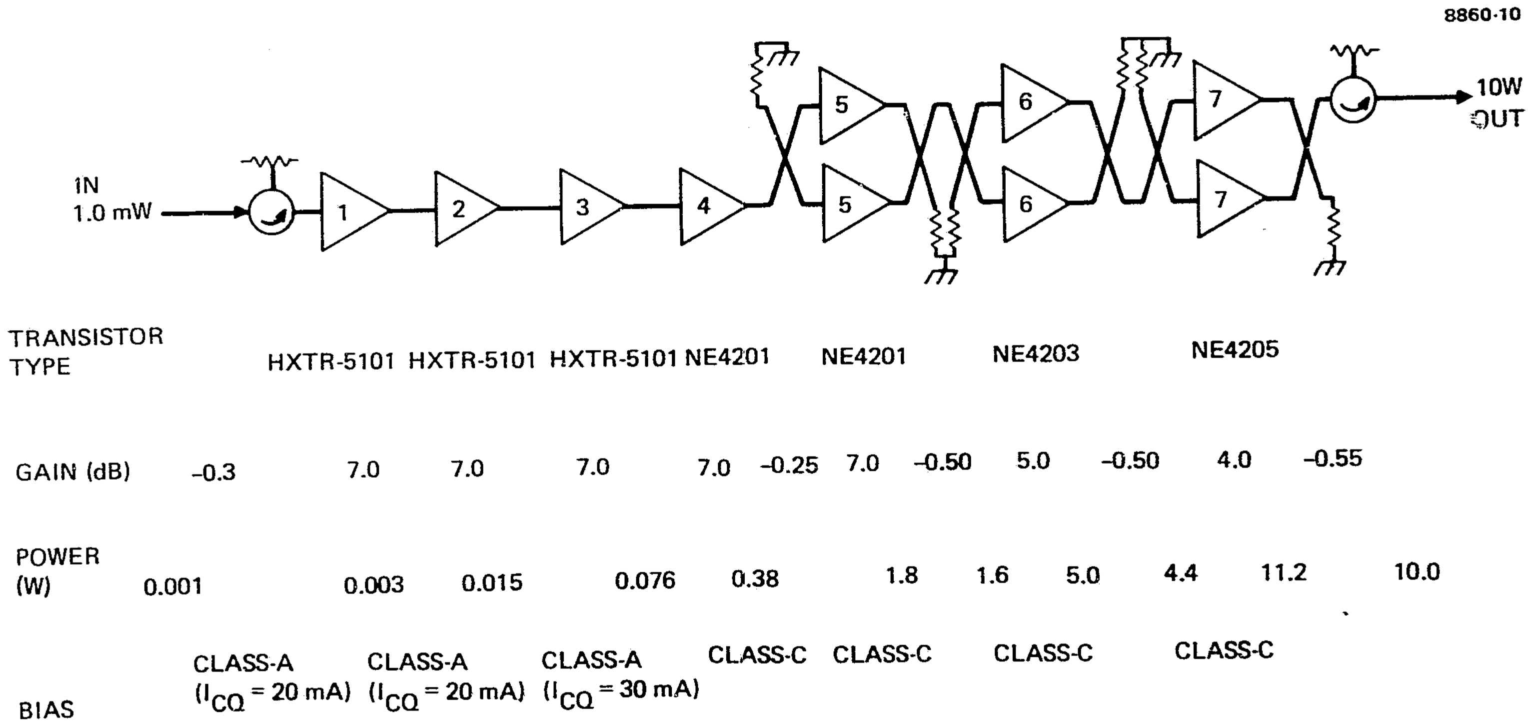

Figure 3. 10-W, 4-GHz bipolar-transistor amplifier.

It is feasible to construct a 20-W bipolar power amplifier at 4 GHz by adding a four-transistor stage to the preceding 10-W power amplifier. The transistors would be combined with hybrids as illustrated in Figure 4. Assuming losses of 0.25 dB for the circulator and for each hybrid level, 24 W would be required from the four transistors to produce a 20-W output. Therefore, each transistor must provide 6 W of output power. With 4 dB of power gain for each transistor, the input power would be 2.4 W. After considering losses in the two levels of input hybrids, the total input power for the stage would be 10.8 W.

4. Device Failure/Amplifier Degradation

Quadrature hybrids would be used in most stages of the transistor amplifiers. Should one device in a hybrid-combined pair fail completely, the output power from the stage would be reduced to 25% of its former output. Therefore, for a failure in any quadrature-hybrid-combined stage of the amplifier, the output would be reduced to 25% of the previous output. In general, the total output of a quadrature-hybrid-combined pair is given by:

$$P_{out} = \frac{P_1 + P_2}{2} + \sqrt{P_1 P_2} \quad ,$$

where P_1 and P_2 are the output powers of the individual transistors. Although the loss in power output would be much less drastic if one of the devices degraded rather than failed completely, this is unlikely to happen. Once a transistor begins to degrade, complete failure normally follows in a few hours.

The use of four transistors in the output stage of the 20-W, 4-GHz bipolar-transistor amplifier would provide more graceful degradation. Should one of the four transistors in the output stage fail completely, the power output would decrease to 11.25 W, or 56% of normal. Should two of the four transistors fail completely, the power

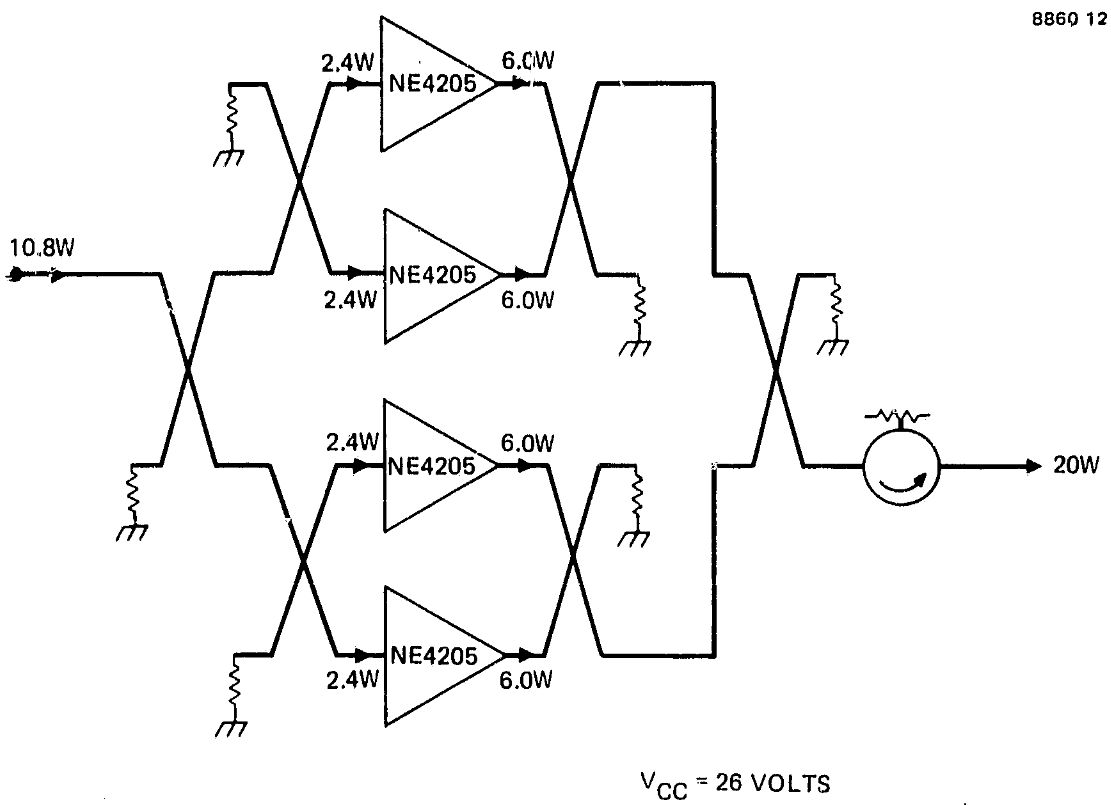

Figure 4. 20-W, 4-GHz bipolar-transistor output stage.

output would decrease to 5 W, or 25% of the normal value. (The output would also be reduced to 5 W if any single transistor in one of the hybrid-combined driving stages should fail.)

5. Primary Power Requirements

The amplifier would operate from 26 V dc, which would assure the best performance from the output stage. The three class-A stages will draw a total quiescent supply current of 130 mA (of which 60 mA is allocated for bias control circuitry). Operating from 26 V, the class-A stages would consume 3.38 W if biased continuously. We would plan to use a bias control switch, which would provide bias power during the 50-msec period of the pulse train and remove the bias power during the 500 msec between pulse trains. This corresponds to a bias power duty factor D of 0.091, which would reduce the average power consumption of the class-A stages to 308 mW.

The bias control switch is illustrated in Figure 5. A Darlington transistor, Q2, is used as a series-pass current-switching transistor between the power supply and the transistor amplifier. The series pass transistor has a nominal current gain of 5000. This means that as much as 5 A of current can be switched on and off with only 1 mA of control current from the power supply. The control current, which is provided by the resistive divider (R_1 and R_2) from the power supply to the base of the Darlington transistor, is easily switched by the inverter transistor Q1. A positive voltage pulse of 1 V to the input of Q1, derived from the logic control circuitry for the radar altimeter, switches off the supply current. The series pass transistor introduces a 1- to 2-V series drop from collector to emitter when carrying 5 A. The amplifier bias current can be switched on or off in less than 1 μsec with this circuit.

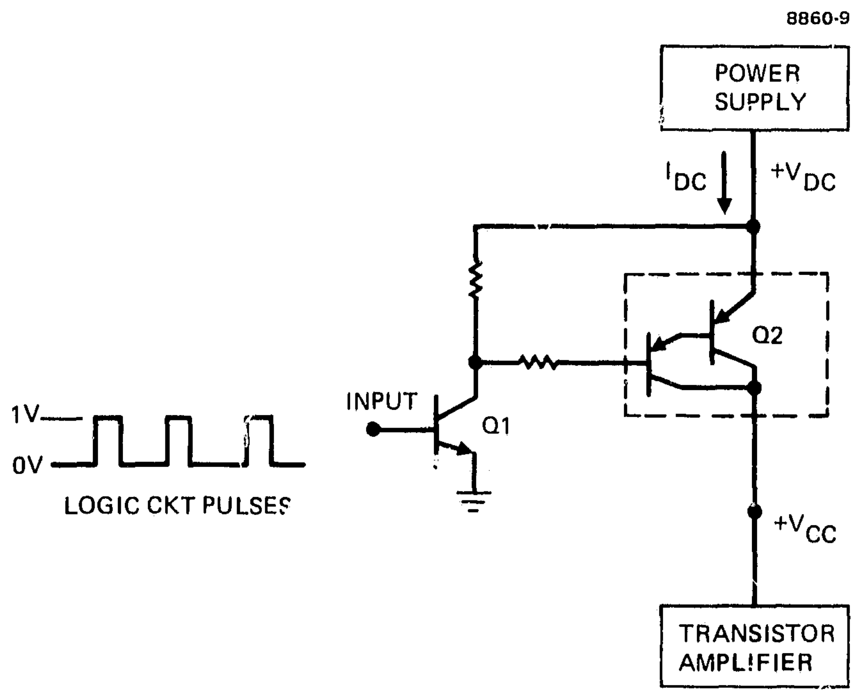

Figure 5. Bias switching control circuit.

The class-C transistor stages will operate with between 20 and 25% collector efficiency η_c, where $\eta_c = P_{out}/P_{DC}$ for each transistor, while consuming no power between pulses other than that corresponding to a total collector leakage current of no more than 2 mA for the seven class-C biased transistors. This amounts to 52 mW of total class-C standby bias power from the 26 V supply.

As Figure 3 shows, the sum of the peak collector output power from the seven class-C transistors is 18.4 W. Assuming pessimistically a 20% collector efficiency for these stages, the peak dc input power is 92 W. The duty factor D for the class-C stages is:

$$D = \frac{\text{(no of pulses) x (pulse width)}}{\text{(pulse period)}}$$

$$= \frac{(50)\ (67 \times 10^{-6})\ \text{sec}}{(0.550)\ \text{sec}}$$

$$= 0.0061.$$

The product of the peak dc power and this duty gives 560 mW, which is the average dc power consumed. Including the power considered for the class-A stages and collector leakage power, the total power drain for the 10-W transistor amplifier is 0.920 W, which requires an average dc current of 24 mA from the 26-V supply.

The complete 20-W amplifier also operates from 26 V. Allowing an additional 2 mA of total collector leakage for this four-transistor stage with each device operating at 20% collector efficiency, the average dc power and current for the complete amplifier is 1.40 W and 54 mA, respectively. The total primary power requirements are summarized in Table 2 together with the projected power requirements of 10- and 20-W GaAs FET power amplifiers.

Table 2. Projected Primary Power Requirements for the 4-GHz Transistor Power Amplifiers

Type of Amplifier	Output Power	Supply Voltage, Vdc	Supply Current		Supply Power, W
			Peak, A	Average, mA	
Bipolar Transistor	10 W (40 dB gain)	+26	3.67	35	0.920
	20 W (43 dB gain)	+26	8.29	63	1.628
Field-Effect Transistor	10 W (40 dB gain)	+12	2.75	250	3.00
		-12	0.30	300	3.60
	Total				6.60
	20 W (43 dB gain)	+12	5.75	523	6.27
		-12	0.35	350	4.20
	Total				10.47

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6. Size and Weight

The projected size and weight for the 10- and 20-W transistor amplifiers are given in Table 3. The input and output circulators account for 2 in. of the length and 4 oz of the weight of each amplifier. The dimensions indicated are revised projections from the original quotation from Microwave Power Devices, Inc., (MPD) for the building of prototype amplifiers.

C. GaAs-FET POWER AMPLIFIER

GaAs-FET devices with power outputs up to 5 W at 4 GHz are available (from NEC, Fujitsu, and MSC), but as yet there are no space-qualified power GaAs FETs available. Also, space qualification for GaAs FETs is expected to take longer than for the bipolar-transistor design,which can be space qualified in about 12 months.

Table 3. Projected Size and Weight of the Bipolar Power Amplifiers

Amplifier Power Level	Length,[a] in.	Width, in.	Height, in.	Volume, $in.^3$	Weight, oz
10 W (40 dB gain)	8.0	2.0	1.0	16.0	10
20 W (43 dB gain)	10.0	2.0	1.0	20.0	12

[a]Includes the physical projection of the input and output connectors. The length excluding connectors is 1 in. less.

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A 10-W peak power FET amplifier designed for operation at 4 GHz would have a configuration similar to the bipolar amplifier in Figure 3. The higher-power FET stages would be balanced pairs combined with 3-dB quadrature hybrids as would be used in the last three stages of the bipolar amplifier design. Since the FET would have 1 to 2 dB higher power gain than the bipolars, only six stages of gain would be necessary. This would correspond to eliminating the first stage of the amplifier in Figure 3.

A 20-W FET amplifier stage consisting of four devices would have a configuration similar to that of the bipolar transistor 20 W stage of Figure 4. The bipolar amplifier predominately consists of class-C biased stages, which dissipate no power between pulses. The FET amplifier design must use class-A biasing for all stages. Even with the elimination of the class-A bias power between pulse trains, the power consumption of the FET amplifier is still projected to be more than six times that of the equivalent amplifier designed with class-C bipolar transistors. The projected primary power requirements are indicated in Table 2. The size and weight of FET power amplifiers, which are projected to be the same as the bipolar equivalents, are indicated in Table 3.

D. IMPATT-DIODE POWER AMPLIFIER

1. General

The IMPATT-diode amplifier would operate at a much narrower pulse width (4 μsec maximum) and a proportionately higher peak power than the transistor amplifiers in developing the same average power. The IMPATT-diode amplifier configurations shown in Figure 6 obviously do not provide a simple way of fulfilling the 4-GHz power amplifier requirements. Each diode amplifier configuration would require a transistor driver/amplifier of from 1.9 to 8.4 W peak output.

The IMPATT amplifier would use the pulse timing shown in Figure 2. There will be 50 pulses per pulse train equally spaced over a 50 msec period. The pulse trains are repeated every 550 msec. The only change from the transistor pulse timing is the change in pulse width to 4 μsec to better satisfy the characteristics of the 4-GHz IMPATT diode. To produce average powers of 30, 60, and 120 mW as before requires peak powers of 84, 168, and 336 W, respectively. The configurations for these three peak power outputs are illustrated in Figure 6.

2. IMPATT Diodes

A NEC IMPATT diode was selected for use at 4 GHz. The diode is a silicon, double-drift-region device mounted on a diamond heat sink. The diode is rated at 60 W peak power output operating at a 1-μsec pulse width and 10% duty factor. NEC states that the diode will perform reliably operating with 4-μsec widths at 60-W peak power with a 10% minimum power-added efficiency. The diode operates from a 150-Vdc supply.

3. Bias Modulators and Pre-Pulse Diode Heating

The bias modulators for these stages will operate from a 165-Vdc input to provide 150 V to each diode at the diode operating current of ∿4 A. Because of the low duty cycle operation, dc current bias will

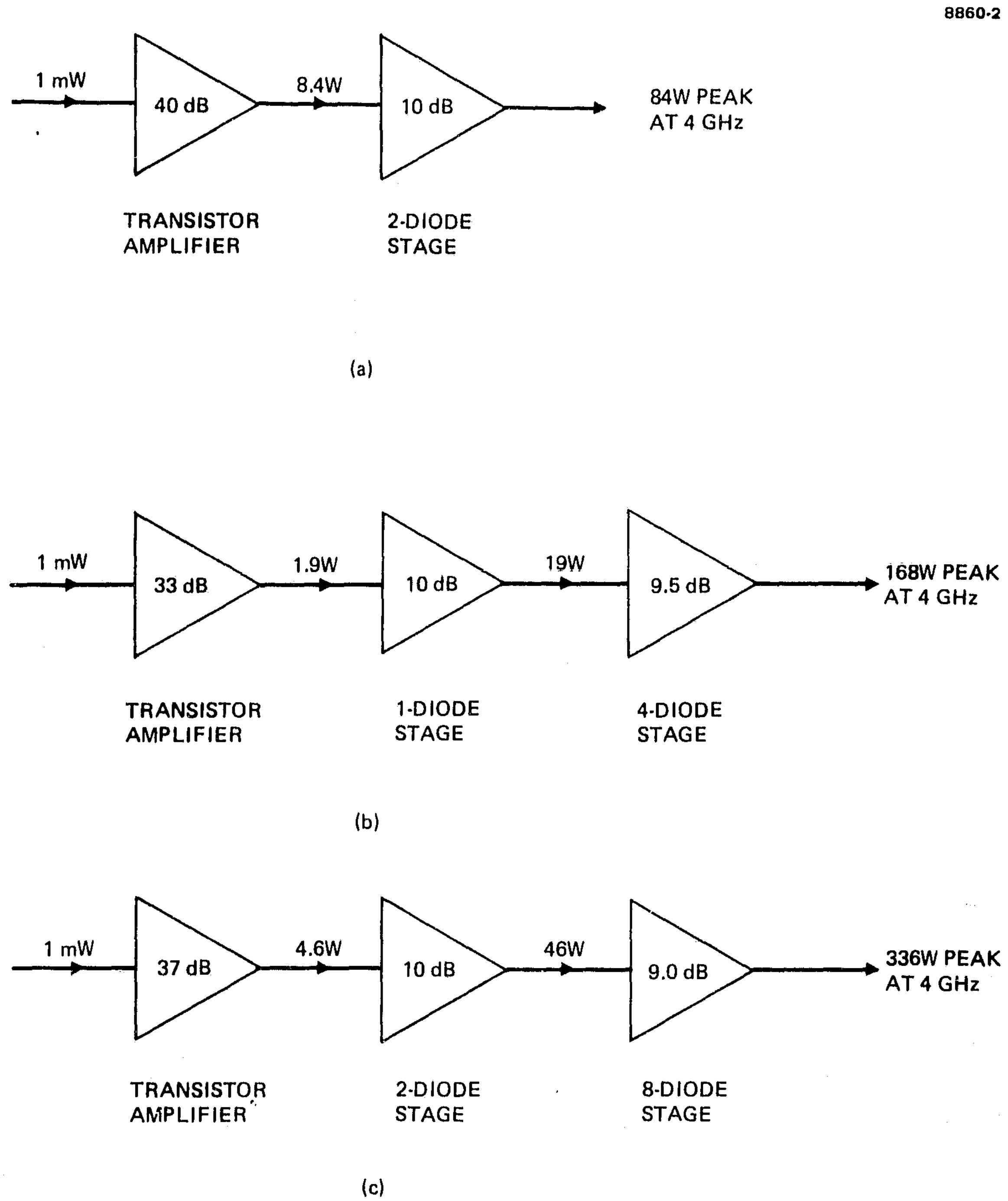

Figure 6. Block diagrams of the 4-GHz IMPATT-diode power amplifier configurations.

actually be applied 5 to 10 μsec prior to each rf pulse and continue to the end of each 4-μsec pulse. The 1-msec interval between consecutive pulses is long when compared to the less than 10-μsec thermal time constant of the IMPATT diodes. This means the diode junction cools from an operating temperature of nearly 200°C to about 60°C, the diode case temperature between pulses. To realize good amplification during a pulse, the diode junction must be at a reasonably high temperature (typically a minimum of between 100 and 140°C). Therefore, in this application the cool junction must be pre-heated before the start of each rf pulse for good amplification throughout the pulse. The preheating can be accomplished by applying the normal operating dc current bias to the diode for between 5 and 10 μsec immediately preceding each operating pulse. This is easily accomplished with a logic control signal to the bias modulators.

The bias modulators are compactly constructed using thick-film hybrid transistor circuits. A modulator for controlling the bias to four individual diodes is projected to be 2.2 in. by 2.2 in. by 0.25 in. and to weigh 2 oz. One energy storage capacitor — estimated to be 2.2 in. by 2.2 in. by 0.25 in. and to weigh 3 oz — is required with each four-diode bias modulator.

4. IMPATT-Diode Circuit Design

The most effective combining of from four to as many as 64 IMPATT diodes has been accomplished with the Hughes cylindrical resonant-cavity combiner at frequencies of 10 GHz and higher. The smallest resonant cavity that can be used at a given frequency operates in the TM_{010} mode. Assuming a 10-GHz operating frequency, a TM_{010}-mode cavity would provide sufficient circumference for mounting up to 16 single diodes or 32 diodes as twin-diode modules (TDMs). The overall dimensions of a 10-GHz, TM_{010}-mode resonant-cavity combiner are 1.6 in. in diameter by 3.25 in. long. Combining efficiencies greater than 90% have been attained in combining 16 single-diode modules in this combiner using pulsed diodes (up to ∿100% combining efficiency has been observed using cw diodes).

The equivalent TM_{010}-mode resonant-cavity combiner designed for 4-GHz operation requires a cavity diameter 2.5 times larger than was required at 10 GHz. The 4-GHz combiner would be 2.92 in. in diameter and 3.23 in. long with a weight of 30 oz. Although this combiner would be too cumbersome to consider for combining a small number of diodes, it should be instructive to project its potential power-combining capability at 4 GHz.

The number of diodes that can be combined in the resonant-cavity combiner for low-average-power applications is determined only by the number of diodes that can be physically mounted around the circumference of the cavity. (In high-average-power applications, the thermal design of the combiner must be considered to ensure that adequate dissipative heat flow is provided.) The cavity dimensions at 4 GHz would permit mounting 40 of the 60-W diodes for a peak power capability conservatively estimated at 1.8 kW. Assuming 40 TDMs were used, the estimated output power would double to 3.6 kW (peak). If more power were necessary, the combiner could be designed for operation in the TM_{020} mode. This would provide room for 90 diodes or 90 diode pairs (TDMs), which would produce 4.1 or 8.1 kW of peak output power, respectively. This combiner would be 5.7 in. in diameter, 3.25 in. long, and weigh about 40 oz.

Considering that only from two to eight diodes are to be combined in the output stage of the 4-GHz power amplifier, the most effective means for power combining would follow from direct paralleling of diodes and/or combining with 3-dB quadrature hybrids.

Direct paralleling of two diodes has been successfully demonstrated at 10 GHz in a twin-diode amplifier (TDA). The impedance matching circuitry consisted of a multi-section coaxial transmission line transformer. The amplifier size and weight at 4 GHz could be reduced by using microstrip transmission line on a high-dielectric-constant substrate such as alumina or Epsilam 10. Paralleling of three and four diodes is also feasible.

The 3-dB quadrature hybrid is another means for efficiently power combining pairs of elements which could be single or multi-diode amplifiers. These hybrids are often arranged in a corporate structure for combining four or eight amplifying elements. Microstrip on alumina (or Epsilam) is commonly used to realize high-performance 3-dB quadrature hybrids that can easily fit within the dimensions of 0.05 in. by 0.3 in.

5. Size and Weight Projections

Using a combination of multi-diode amplifiers having matching circuitry and 3-dB quadrature hybrids constructed in microstrip, the projected volumes and weights of the three IMPATT-diode amplifiers are given in Table 4. The projected volume and weight of each transistor driver amplifier is included in the table as a separate item.

6. Primary Power Requirements

The projected dc power requirements of the IMPATT-diode amplifier configurations shown in Figure 6 are given in Table 5. The estimates include the dc power needs for the class-C bipolar-transistor driver amplifier. Since the exact time for the junction preheat is unknown, the power consumption is indicated for both 5- and 10-μsec pre-heat times.

E. CONCLUSIONS AND RECOMMENDATIONS

A comparative evaluation of 4-GHz solid-state power amplifier designs for use in a spacecraft radar altimeter transmitter indicated that a 10- or 20-W bipolar transistor power amplifier is clearly the best choice at this time. IMPATT-diode power amplifiers and GaAs-FET power amplifiers were the other possibilities in this application.

The IMPATT-diode amplifier approaches are least attractive for the present 4-GHz application since they include transistor driver amplifiers that, if operated independently, could satisfy all power

Table 4. Projected Volumes and Weights for the 4-GHz IMPATT-Diode Amplifiers

Amplifier Output, W	Description	Volume, $in.^3$	Weight, oz
84	84-W diode amplifier	5	6
	8.4-W transistor driver	16	12
	Total	21	18
168	168-W diode amplifier	11	15
	1.9-W transistor driver	12	8
	Total	23	23
336	336-W diode amplifier	24	28
	4.6-W transistor driver	14	9
	Total	38	37

Note: These estimates include circulators, bias modulators, and connecting cables.

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Table 5. Projected Primary Power Requirements for the 4-GHz IMPATT Diode Power Amplifiers

Amplifier Output, W	Description of Stages	Potential, Vdc	Peak Current, A	5-μsec Preheat		10-μsec Preheat	
				Average Current, mA	Average Power, W	Average Current, mA	Average Power, W
84	84-W diode amplifier	165	6.7	6	0.99	9	1.54
	8.4-W transistor driver	26	3.5	30	0.78	30	0.78
	Total				1.77		2.32
168	168-W diode amplifier	165	13.6	11	1.82	17	2.83
	1.9-W transistor driver	26	1.0	9	0.22	9	0.22
	Total				2.04		3.05
336	336-W diode amplifier	165	27.7	23	3.80	35	5.91
	4.6-W transistor driver	26	1.8	17	0.45	17	0.45
	Total				4.25		6.36

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amplifier requirements by going to the 67-μsec pulse width instead of 4 μsec (configuration b of Figure 6 would not produce adequate power, but adding one more transistor stage would be simpler than adding an IMPATT stage, or stages, and IMPATT modulators). Hence, using IMPATT diodes would merely add to the complexity of the power amplifier at this frequency.

A GaAs FET power amplifier design must use class-A biased stages. Despite the application of the FET bias power at a 9% duty cycle, the class-C bipolar-transistor amplifier would give equal performance at less than one-sixth of the dc power consumption. With respect to size, weight, and the remaining electrical performance factors, the bipolar and field-effect forms were equivalent. At this time, no power GaAs FETs have been space qualified. This might present uncertainties in the scheduled development of a space-qualified GaAs-FET power amplifier in the next year.

We recommend that a bipolar amplifier design using NEC power transistors be developed. Although 5-, 10-, and 20-W peak power levels were considered, the two higher power levels afford the most practical designs at this time. MPD has quoted the development of prototype 10- and 20-W designs. MPD specializes in the development and manufacture of bipolar and field-effect transistor power amplifiers. They have experience in producing space-qualified amplifiers within NASA specifications. MPD is suggested as the best known source for the design and development of the 4-GHz bipolar-transistor power amplifier. Amplica, Inc., is considered a possible second source. The quotations received from both companies are included in the ROM cost report.

No technology developments are needed for the development of the power amplifiers. The NEC bipolar transistors are designed to meet high-reliability space applications. We suggest that procurement of the space-qualified NEC transistors be initiated at least 12 months before the required date of completion for the space-qualified power amplifier.

SECTION 2

X-BAND RADAR ALTIMETER TRANSMITTER POWER AMPLIFIER

A. SYSTEM DESCRIPTION

The 10-GHz radar altimeter system is illustrated in Figure 7. A pulsed 10-GHz source is phase-shift keyed by a single-bit phase shifter. The ∿10-mW peak power pulses are amplified to a 2-W peak power level with a linear GaAs-FET driver/amplifier. An IMPATT-diode amplifier then amplifies the FET amplifier output to a 50-, 100-, 200-, or 500-W peak power output, which passes through an isolator to the transmitter antenna.

The 50-W peak power amplifier output would meet the minimum S/N for the system. The 100-, 200-, and 500-W peak power levels, which would provide an increase in the signal-to-noise ratio of 3-, 6-, and 10-dB, respectively, are also evaluated for feasibility with respect to spacecraft operation.

The pulsed output of the X-band transmitter is depicted in Figure 8. Each pulse consists of 13 phase-shift-keyed binary bits in a Barker code sequence. The 2- to 4-μsec-wide pulses are transmitted in a train of 1000 pulses with a pulse repetition time of 4 msec. There is a duration between successive pulse trains of between 1 sec and 1 hr.

B. GaAs-FET DRIVER AMPLIFIER

The X-band GaAs FET amplifier consists of six stages, as illustrated in Figure 9. The design indicates currently available transistors from NEC, but FETs of equivalent electrical performance are also available from Fujitsu and MSC.

The class-A amplifier operates with 4.5 A from a +15-Vdc supply and 0.3 A from a -15-Vdc supply. The input and output ports are isolator protected.

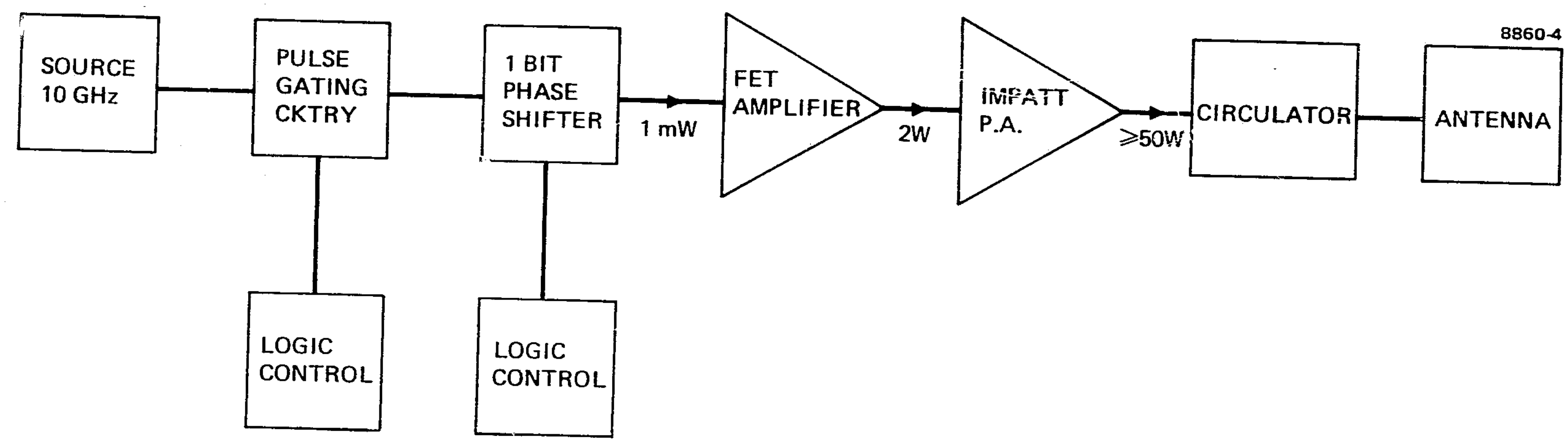


Figure 7. X-band solid-state radar altimeter transmitter.

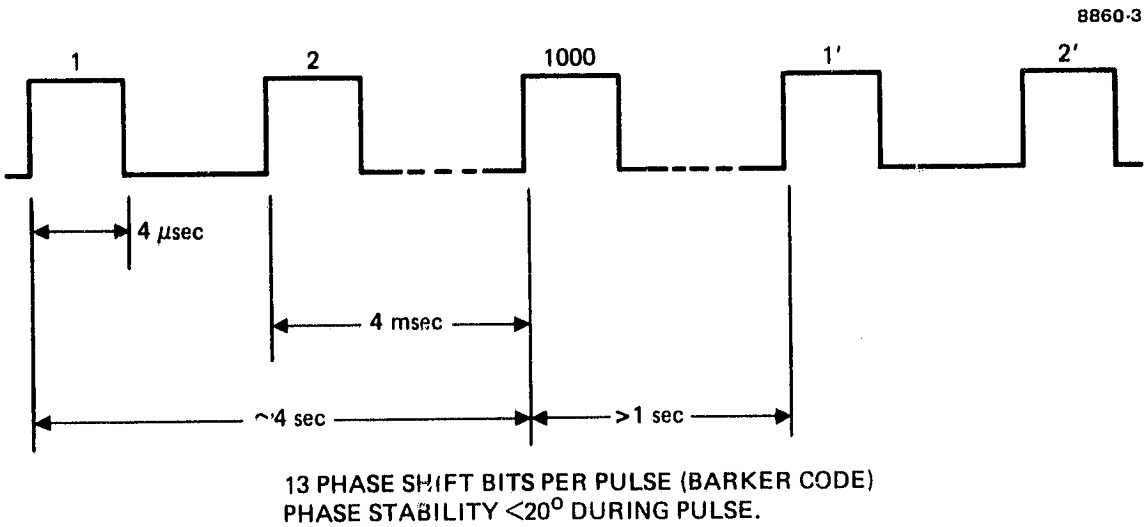


Figure 8. X-band radar altimeter pulse timing diagram.

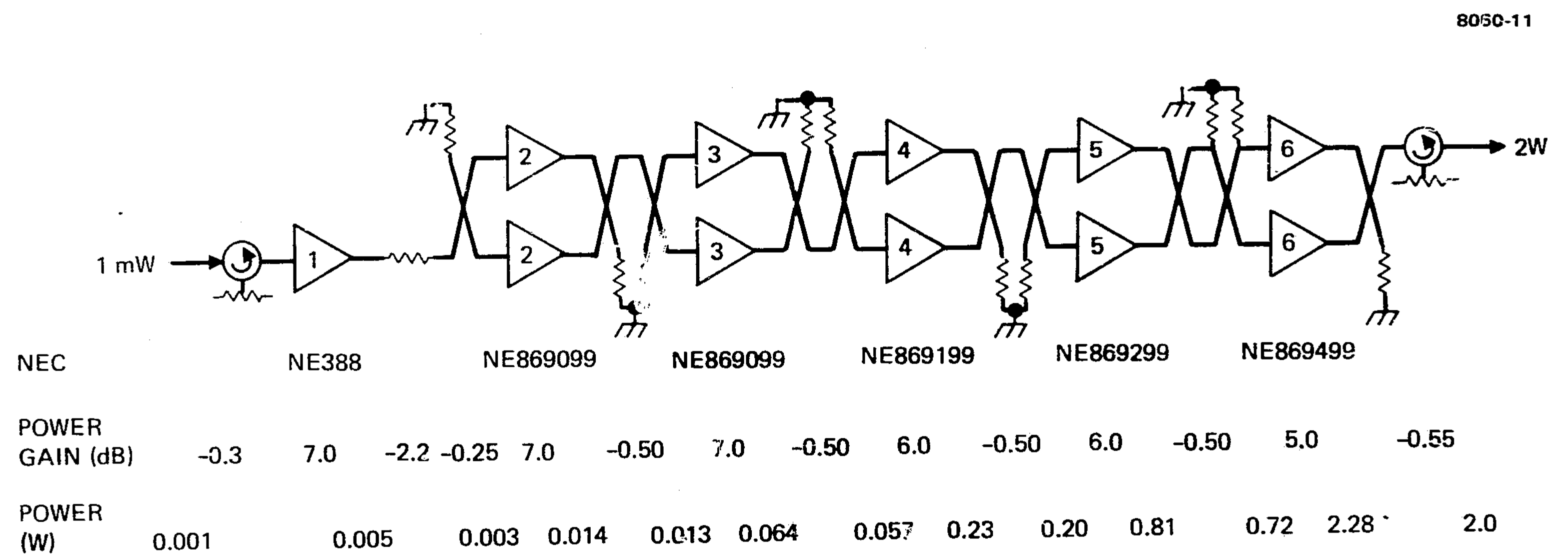


Figure 9. 2-W X-band FET driver/amplifier.

The quiescent class-A dissipation can be reduced by at least 97.5% during the pulse train by using a bias switching circuit in each dc supply input. The circuit of Figure 5 is used to switch the bias power on for a 100-μsec period surrounding each of the 1000 pulses in the pulse train. Bias power is applied for a total of 0.2 sec during the 4-sec pulse train. This results in a power consumption of 1.80 W average over the 4-sec period. (It may be possible to switch the bias on and off for only 20-μsec periods surrounding each pulse, which would further reduce the average power consumption for the amplifier to 0.350 W.) The average dc supply currents are 113 mA from the +15 V supply input and 8 mA from the -15-V supply input.

All stages other than the first use 3-dB quadrature hybrids to combine pairs of transistors in a balanced configuration that offers three important qualities. First, the hybrids provide 15 to 20 dB of low-loss interstage isolation, which improves amplifier stability and phase linearity. Second, balanced-pair power combining is essential for the 2-W amplifier output since the largest power currently available from a single device is only 1 W. Third, the operating reliability of the amplifier is improved. Should either device in a balanced pair fail, the stage will continue to produce one-half the output of the remaining transistor. This means that if a device in any balanced stage of the amplifier fails, the amplifier will produce one-fourth of the normal 2-W output power (i.e., a 0.5-W output).

The NE869499 output transistors are operating well within the manufacturer's minimum specification for power output and power gain. The amplifier produces a 2-W output when driven with a 1-mW input. The size of this amplifier is projected to be within the dimensions of 5.0 in. long, 1.5 in. wide, and 0.5 in. high including connectors. The projected weight of the 2-W FET amplifier is 8 oz.

C. IMPATT-DIODE POWER AMPLIFIER

1. IMPATT Diodes

The two diodes planned for use in the X-band power amplifier are manufactured by NEC. Each diode is a silicon, double-drift-region IMPATT mounted on a diamond heat sink for optimal thermal performance in wide-pulse applications. The ND81510-5H is rated at 18 W peak power output at 10 GHz with 10% power-added efficiency. This device will be used at peak power outputs of 12 W or less in the lower power stages of the proposed amplifiers. The ND84010-6K diode is rated for 40 W peak power output at 10 GHz with 10% power-added efficiency. This diode will be used when peak power outputs between 12 and 29 W are required. The dc operating voltage for the diodes is 145 V for the smaller diode and 150 V for the larger.

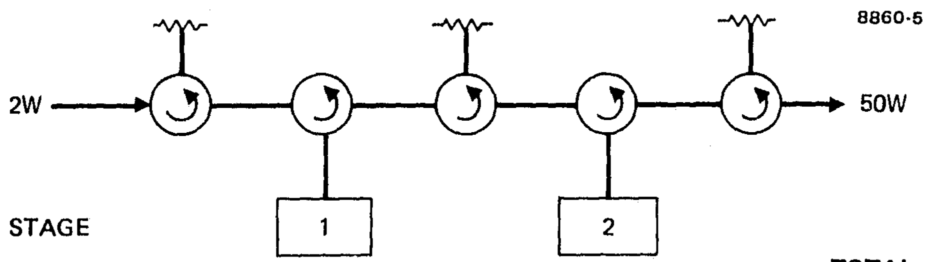
2. Amplifier Designs

a. 50-W Diode Amplifier

The 50-W peak power amplifier block schematic is shown in Figure 10. Two stages are used for 14 dB of overall gain. Isolators are used at the input, output, and between stages. The 2 W input to the amplifier is amplified to 10.5 W with a single-diode coaxial amplifier (SDA) first stage. The output is a TDA coaxial stage which develops 53.8 W peak power output.

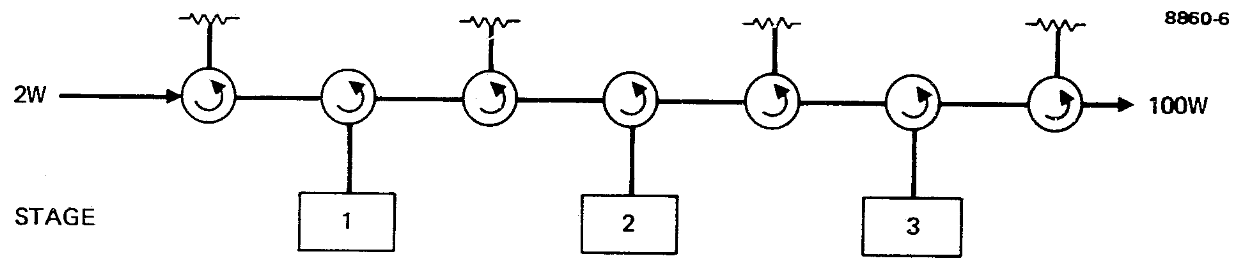
b. 100-W Diode Amplifier

The 100-W diode amplifier will provide 17 dB gain using three stages of amplification. The block schematic and gain parameters for this amplifier are shown in Figure 11. The design uses four isolator junctions for input, output, and interstage isolation. The output uses a four-diode resonant-cavity combiner stage (4-PAC) with 6-dB gain to deliver 107 W into the output isolator. The first and second stages each use SDAs producing 6.4 W and 28.9 W peak outputs, respectively.



						TOTAL
GAIN OR LOSS, dB	-0.3	7.5	-0.3	7.4	-0.3	14
POWER OUT, dBW	2.7	10.2	9.9	17.3	17.0	17.0
POWER OUT, W	1.87	10.5	9.8	53.8	50.2	50.2
POWER ADDED, W		9.46		48.5		
NUMBER OF DIODES		1		2		3
POWER/DEVICE, W		11.2		24.2		
RATED DIODE POWER		18		40		
DIODE TYPE		NEC ND81510-5H		NEC ND84010-6K		

Figure 10. 50-W, X-band diode power amplifier.



STAGE		1		2		3		TOTAL
GAIN OR LOSS, dB	-0.3	6.1	-0.3	6.1	-0.3	6.0	-0.3	17.0
POWER OUT, dBW	2.7	8.8	8.5	14.6	14.3	20.3	20.0	20.0
POWER OUT, W	1.87	7.6	7.1	28.9	27.0	107.4	100	100
POWER ADDED, W		6.4		24.4		89.9		
NUMBER OF DIODES		1		1		4		7
POWER/DEVICE, W		6.4		24.4		22.5		
RATED DIODE POWER,W		18		40		40		
DIODE TYPE		NEC ND81510-5H		NEC ND84010-6K		NEC ND84010-6K		

Figure 11. 100-W, X-band diode power amplifier.

c. <u>200-W Diode Amplifier</u>

This amplifier uses three stages for 20 dB of overall gain. The block schematic and gain parameters are given in Figure 12. The output stage uses an 8-diode resonant-cavity combiner (8-PAC) to produce 214 W with 7 dB of gain. The second stage TDA produces 45.8 W. The input stage SDA produces 9.6 W of output with 2.0 W of input power.

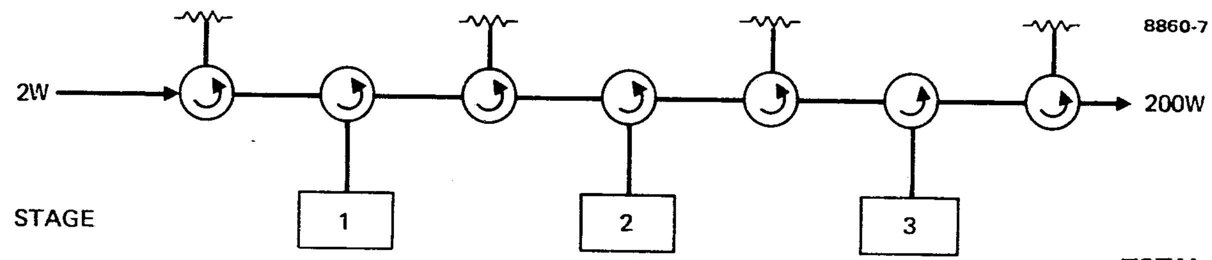
d. <u>The 500-W Diode Amplifier</u>

This design is described in block form in Figure 13. The first three stages are identical with the 100-W power amplifier design of Figure 11. The fourth stage uses a 16-diode resonant-cavity combiner (16-PAC) to develop the 500 W peak output power.

3. <u>Pre-Pulse Diode Junction Heating</u>

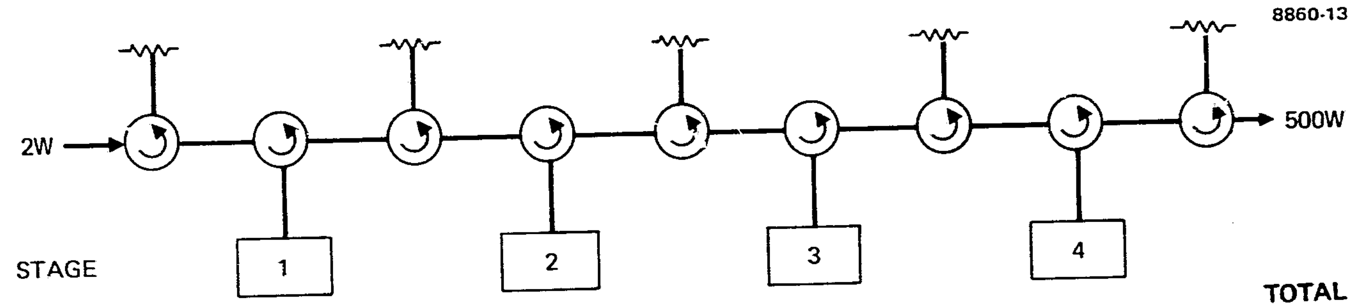
During a pulse while power is being amplified, the junction of an IMPATT diode operating at rated output power will be about 200°C. During the time interval between pulses, since no power is dissipated at the diode junction, the junction temperature decreases approaching the diode case temperature. When the inter-pulse interval is 20 μsec or more, the diode junction will have cooled to a temperature that will degrade the pulse turn-on characteristics for the following pulse. The circuit impedance, which is chosen to match the diode at the higher operating junction temperature, provides a poor match to the markedly different diode impedance at the lower junction temperature. The poor transfer of input power to the diode during the early portion of the pulse when the diode junction temperature is lower than normal reduces the output power. This can be corrected if the diode junction is pre-heated to a suitable operating temperature prior to each rf pulse.

The X-band radar altimeter system with a pulse repetition time of 4 msec requires pre-pulse diode junction heating. The diode junction can be pre-heated by applying a dc bias current for a short time prior to the arrival of the rf pulse. This approach has been demonstrated



STAGE		1		2		3		TOTAL
GAIN OR LOSS, dB	-0.3	7.1	-0.3	7.1	-0.3	7.1	-0.3	20
POWER OUT, dBW	2.7	9.8	9.5	16.6	16.3	23.3	23.0	23.0
POWER OUT, W	1.87	9.6	8.9	45.8	42.8	214	200	200
POWER ADDED, W		8.52		40.8		189.7		
NUMBER OF DIODES		1		2		8		11
POWER/DEVICE, W		8.5		20.4		23.7		
RATED DIODE POWER, W		18		40		40		
DIODE TYPE		NEC ND81510-5H		NEC ND84010-6K		NEC ND84010-6K		

Figure 12. 200-W, X-band diode power amplifier.



STAGE		1		2		3		4		TOTAL
GAIN OR LOSS, dB	-0.3	6.4	-0.3	6.4	-0.3	6.4	-0.3	6.3	-0.3	25.5
POWER OUT, dBW	2.7	9.1	8.8	15.2	14.9	21.3	21.0	27.3	27.0	27.0
POWER OUT, W	1.87	8.1	7.6	33.2	30.1	135	126	538	500	500
POWER ADDED, W		6.9		28.5		117		458		
NUMBER OF DIODES		1		1		4		16		22
POWER/DEVICES, W		6.9		28.5		29		28.6		
RATED DIODE POWER, W		18		40		40		40		
DIODE TYPE		ND81510-5H		ND84010-6K		ND84010-6K		ND84010-6K		

Figure 13. 500-W, X-band diode power amplifier.

with X-band diodes at HRL. A bias current equal 70% of the normal operating bias current value for the diode was applied for about 12.5 μsec to increase the diode junction temperature from 18°C to an acceptable operating temperature of 140°C. The diode tested, a Hewlett Packard 5082-0710, is a silicon, double-drift-region IMPATT rated for 14 W output at X-band. The time required for the pre-pulse junction heating of the NEC devices to be used in the radar altimeter should be about the same. In calculating the power consumption of the diode amplifier, we assume that the pre-pulse junction heating will require the application of bias currents of 1.4 and 2.5 A (the respective rated operating currents for the ND81510-5H and ND84010-6K diodes) for between 5 to 10 μsec prior to each pulse.

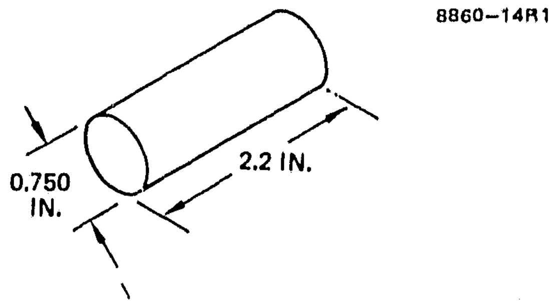
4. Bias Modulators

The modulators for the diode stages will be fabricated as hybrid circuit modules using bipolar transistors together with thick film conductors and resistors deposited on ceramic substrates. One modulator hybrid module would contain four bias channels (each channel would bias one IMPATT diode). The module is projected to measure 2.2 in. by 2.2 in. by 0.25 in. and to weigh 2 oz. An energy storage capacitor is mounted above the modulator hybrid. This capacitor is projected to be 2.2 in. by 2.2 in. by 0.25 in. and weigh 2 oz. The bias modulators will operate from 165 Vdc and deliver ∿4 A at 150 V to each of four diodes during bias periods. During the bias period, each modulator channel is delivering ∿600 W of dc power while dissipating 40 to 60 W, corresponding to an operating efficiency of 91%.

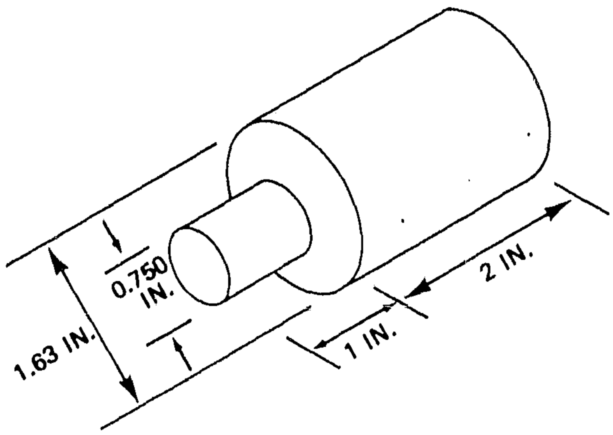
5. Amplifier Size and Weight

a. Diode Combiners

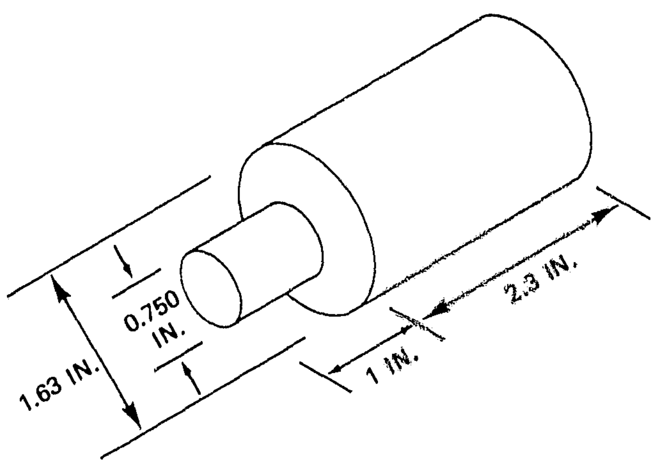
All stages will be cylindrical and contain from 1 to 16 diodes. The stage outlines are illustrated in scale with dimensions shown in Figure 14. The simplest stage is a coaxial SDA. Two diodes



SINGLE DIODE OR TWIN DIODE COAXIAL AMPLIFIERS



4-DIODE (OR 8-DIODE) RESONANT CAVITY COMBINER



16-DIODE RESONANT CAVITY COMBINER

Figure 14. Dimensional outlines for the IMPATT diode amplifier stages.

can be operated in parallel in a TDA. Both amplifiers are identical externally, being 0.75 in. in diameter and 2.2 in. long (including the protrusion of the amplifier connector) and weighing 0.5 oz. All other stages use resonant-cavity-combiner amplifiers. The 4-PAC and 8-PAC stages of Figure 14(b) are identical in size and weight — 1.62 in. in diameter, 3.00 in. long (including a connector stem protrusion of 1 in.), and 5.3 oz in weight. The 16-PAC, shown in Figure 14(c), is 1.63 in. in diameter and 3.3 in. long (including a 1.00 in. connector protrusion). The 16-PAC weighs 6.2 oz. The size and weight of each diode stage are summarized in Table 6.

b. Circulators

The circulators for each amplifier design are an integrated assembly of circulator junctions. The projected size and weight of each circulator assembly are given in Table 7.

c. Size and Weight Projections for the Complete Power Amplifier

The diode stages, modulators, and FET driver amplifier may be physically arranged a variety of ways in assembling the complete power amplifier. Therefore, only the overall volume will be used to summarize the physical size of each amplifier. The volume and weight of each of the four amplifiers are derived from the data on the elemental assemblies given in Tables 8 through 11.

6. Primary Power Requirements

The projected primary power requirements for the X-band power amplifiers are given in Table 12. Three supply voltages are required: +15 and -15 Vdc for the 2-W FET driver amplifier and 165 Vdc for the IMPATT diode amplifier. Although the IMPATT diodes require only 145 to 150 Vdc, the additional voltage is required for the operation of the pulse bias modulators. All calculations assume a diode operating efficiency of 10%, which is conservative. The rated operating currents for the ND81510-5H and the ND84010-6K diodes are 1.4 and 2.5 A, respectively. The calculated range of values for power consumption

Table 6. Projected Size and Weight of the X-Band Diode Combiner Stages

Stage Design	Length, in.	Diameter, in.	Volume, $in.^3$	Weight, oz
SDA, TDA	2.20	0.75	0.97	0.53
4-PAC, 8-PAC	3.00	1.63	6.26	5.3
16-PAC	3.30	1.63	6.89	5.8
Note: Dimensions indicated include the extremities of the connector protrusions. Bias modulators, circulators, and connecting cables are not included in these values.				

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Table 7. Projected Size and Weight of the Circulators for the X-Band Diode Amplifiers

Amplifier Power, W	Length, in.	Width, in.	Height, in.	Volume, $in.^3$	Weight, oz
50	5.1	1.10	0.50	2.81	6
100	7.1	1.10	0.50	3.91	8
200	7.1	1.10	0.50	3.91	8
500	8.4	1.40	0.50	5.88	11
Dimensions include physical projections of the connectors.					

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Table 8. Projected Volume and Weight of the 50-W Power Amplifier

Component	Volume, in.^{3}	Weight, oz
2-W FET amplifier	3.8	8.0
First stage (SDA)	1.0	0.5
Second stage (TDA)	1.0	0.5
Circulator	2.8	6.0
Bias modulators	0.8	1.3
Capacitors	0.8	1.3
Totals	10.2	17.6

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Table 9. Projected Volume and Weight of the 100-W Power Amplifier

Component	Volume, in.^{3}	Weight, oz
2-W FET amplifier	3.8	8.0
First stage (SDA)	1.0	0.5
Second stage (SDA)	1.0	0.5
Third stage (4-PAC)	6.3	5.3
Circulator	3.9	8.0
Bias modulators	2.0	3.0
Capacitors	2.0	3.0
Connecting cables	1.0	1.0
Totals	21.0	28.3

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Table 10. Projected Volume and Weight of the 200-W Power Amplifier

Component	Volume, in.^{3}	Weight, oz
FET amplifier	3.8	8.0
First stage (SDA)	1.0	0.5
Second stage (TDA)	1.0	0.5
Third stage (8-PAC)	6.3	5.3
Circulator	3.9	8.0
Bias modulators	3.6	6.0
Capacitors	3.6	6.0
Connecting cables	1.0	2.0
Totals	24.2	36.3

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Table 11. Projected Volume and Weight of the 500-W Power Amplifier

Component	Volume, in.^{3}	Weight, oz
FET amplifier	3.8	8.0
First stage (SDA)	1.0	0.5
Second stage (TDA)	1.0	0.5
Third stage (4-PAC)	6.3	5.3
Fourth stage (16-PAC)	6.9	5.8
Circulator	5.9	11.0
Bias modulators	7.3	12.0
Capacitors	7.3	12.0
Connecting cables	3.0	5.0
Totals	42.5	60.1

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Table 12. Estimated DC Power for the X-Band Power Amplifiers

Output Power, W	Supply Voltage, Vdc	Peak Supply Current, A	5-μsec Preheat		10-μsec Preheat	
			Average Current, mA	Average Power, W	Average Current, mA	Average Power, W
50 W	165	6.4	12	1.98	20	3.30
	15	3.5	88	1.31	88	1.31
	-15	0.3	8	0.11	8	0.11
Total				3.40		4.72
100 W	165	13.9	25	4.20	43	7.06
	15	3.5	88	1.31	88	1.31
	-15	0.3	8	0.11	8	0.11
Total				5.62		8.48
200 W	165	26.4	49	8.08	82	13.53
	15	3.5	88	1.31	88	1.31
	-15	0.3	8	0.11	8	0.11
Total				9.50		14.95
500 W	165	53.9	108	17.82		28.95
	15	3.5	88	1.31	88	1.31
	-15	0.3	8	0.11	8	0.11
Total				19.24		30.37

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includes applying the rated operating current to each diode for 5 to 10 μsec prior to each rf pulse for pre-pulse junction heating.

D. RELIABILITY AND GRACEFUL DEGRADATION

The solid-state devices in the proposed amplifier designs are operated well below their rated capability to assure moderate operating junction temperatures for long-life operation. For example, the ND84010-6K diode rated at 40 W peak output power is operated at less than 25 W peak in three of the proposed designs. (In the 500-W amplifier design, the maximum power output per diode is 29 W peak.) At the rated output, the diode junction temperature rise above the ambient is 130°C. Operation at 25 W reduces the rise to 105°C. This increases the mean time to failure (MTTF) of the diodes by a factor of 5.5. At an ambient temperature of 75°C, the diode junction temperature is 180°C, which corresponds to an extrapolated MTTF of 1.6×10^9 hr (1.8×10^5 years) for each diode.

The multi-diode resonant-cavity combiner stages in the amplifiers provide for the gradual, or graceful, degradation of power output as diodes fail. Considering N to be the number of diodes in the combiner, each diode provides 1/N of the combined output. Should a diode fail, the total output will be reduced by $\sim 2N$, or twice the normal output of the device. Using the 8-diode resonant-cavity combiner in the 200 W amplifier as an example, each of the 8 diodes contributes one-eighth, or about 25 W, to the combined output of 200 W. Assuming a diode fails, the output power will be reduced by about one-quarter of the total output,or 50 W.

Should a modulator channel fail, the effect on power output will be the same as a diode failure. That is, the power from a diode combiner of N-diodes will be reduced by a factor of 2/N.

As discussed previously, should a GaAs in any balanced stage of the 2-W driver amplifier fail, a 0.5-W amplifier output power is assured.

E. INTRA-PULSE PHASE CHARACTERISTICS

The phase-shift modulation to be used in the pulsed X-band power amplifier requires the uncompensated intra-pulse phase variation to be less than 20°. Any linear phase variation with time that occurs during every pulse can be fully compensated through the signal-processing system. Nonlinear and random variations in phase would not be compensated.

Tests of X-band IMPATT diodes of similar construction (i.e., silicon, double-drift-region design) indicate that the nonlinear intra-pulse phase component is well within the 20° specification. The tests were made using a three-stage, 100-W peak power output amplifier operating at 10 GHz using a 3.2-μsec pulse width. The design consisted of an SDA driving a 4-PAC, which in turn was driving a 16-PAC output stage. The diode used throughout was the Hewlett Packard 5082-0710. The intra-pulse phase variation through the three stages and over a 3.2-μsec pulse was 68° at a 100-W peak output power. The nonlinear component was less than 5°. Pulse-to-pulse phase variations were smaller than 1°. This intra-pulse phase variation is representative of the magnitude expected to be present in the proposed three-stage amplifiers. The 500-W amplifier requires a fourth stage and can be expected to have about one-third more nonlinear phase variation than the three-stage designs, or a total of about 7°.

The nonlinear intra-pulse phase variations for the proposed IMPATT-diode amplifiers are expected to be well within the 20° maximum specified.

F. CONCLUSIONS AND RECOMMENDATIONS

The requirements for an X-band power amplifier for a spacecraft radar altimeter can be met using solid-state devices. The power amplifier would use IMPATT diodes and operate at peak output powers of 50 W or greater using a frequency-shift key modulation of 4-μsec pulses. A GaAs FET driver amplifier with 33-dB power gain and 2-W peak output power would drive the IMPATT-diode stages. It is practical to build amplifiers for this application with peak powers as high as 500 W. The choice must be concerned principally with eater size, weight, and primary power consumption, which are traded for S/N improvement.

The GaAs FETs and IMPATT diodes best suited to this application are manufactured by NEC. The devices are designed for high-reliability space applications. Although neither the FETs nor the diodes have yet been qualified, no qualification problems are anticipated. The initial qualification program is expected to take about six months. The delivery of qualification-tested devices is expected to take an additional nine to twelve months.

A quote for designing the 2-W GaAs-FET driver/amplifier has been received from Microwave Power vices (MPD), a company specializing in custom and production transistor power amplifiers. MPD has previously delivered space-qualified transistor power amplifiers under JPL contracts.

Microwave Semiconductor Corp. (MSC) was sought as an alternate source for the 2-W GaAs FET driver. They are not interested in a small quantity, custom amplifier design. MSC uses their own GaAs FETs in their designs. And although the MSC FETs perform well, the devices are flip-chip mounted, which would prevent or complicate final or pre-cap visual inspection of the device metalization. Since this visual inspection must be resolved for the space qualification of these FETs, qualification of the MSC FETs could take considerably longer than would be required for the NEC FETs.

The proposed X-band IMPATT-diode amplifiers represent designs that utilize previously developed diode amplifier stages. The 4-, 8-, and 16-diode stages use resonant-cavity combiners, which afford reliability through gra ul degradation of output power as diodes fail. The single-diode and twin-diode amplifier stages do not afford graceful degradation. If graceful degradation is absolutely necessary in all stages, multiple-diode resonant-cavity combiners could be used throughout the amplifier. But this would considerably increase the size, weight, and power consumption of the amplifiers.

The prototype X-band IMPATT diode power amplifier development should be preceded by two preliminary 12- to 15-month development efforts:

- A diode evaluation to include the design and development of the SDA and TDA stages.

- The pulse bias modulator circuit.

The new NEC 18- and 40-W IMPATT diodes have not been evaluated for this application. We recommend that the basic single-diode and twin-diode amplifier circuits for the diodes be developed. The power gain, power output, efficiency, stability, intra-pulse phase variations, peak operating junction temperature, and operational ruggedness of the diodes will be evaluated.

Existing pulse bias modulators are capable of controlling about 200 W of dc power over 2-μsec pulse widths. For this application, the pulse bias modulator must control 400 W of dc power over a 4-μsec pulse width, requiring circuit redesign and performance evaluation. In addition, the development of circuitry for the bias pre-heat and protective modulator shut down (should the diode fail) must be considered.

SECTION 3

NEW TECHNOLOGY

The following new technology is being reported. "Multistage Solid-State X-Band IMPATT Amplifier," K.J. Russell and O. Pitzalis, Section 2 of this report, July 26, 1979.

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NEC

MICROWAVE POWER SERIES

NE4200

NE4201 1.5 WATTS, 8dB & 30% EFFICIENCY

NE4203 3.0 WATTS, 5dB & 25% EFFICIENCY

NEM4205 5.0 WATTS, 4dB & 25% EFFICIENCY

FEATURES

- ADVANCED SET* TECHNOLOGY
- POWER TO 5 WATTS AT 4.2GHz
- TITANIUM-PLATINUM-GOLD METALLIZATION FOR HIGH RELIABILITY
- MIL HERMETICALLY SEALED PACKAGES
- LOW OPERATING VOLTAGES V_{CC}=20V
- INDUSTRIAL, MILITARY AND SPACE APPLICATIONS
- INTERNALLY MATCHED FOR SUPERIOR PERFORMANCE
- LOW OPERATING JUNCTION TEMPERATURES
- PACKAGED OR CHIP

DESCRIPTION

The NE4200 Series are hermetically sealed S-Band NPN power transistors which operate Class C up to 4.2GHz with output powers from 1 to 5 watts. This performance is made possible by NEC's new Stepped Electrode Transistor (SET) technology which provides high gain, efficiency and power at reliability levels unattainable with conventional state-of-the-art devices. Standard devices are common base but other biasing arrangements and packages are available on special request.

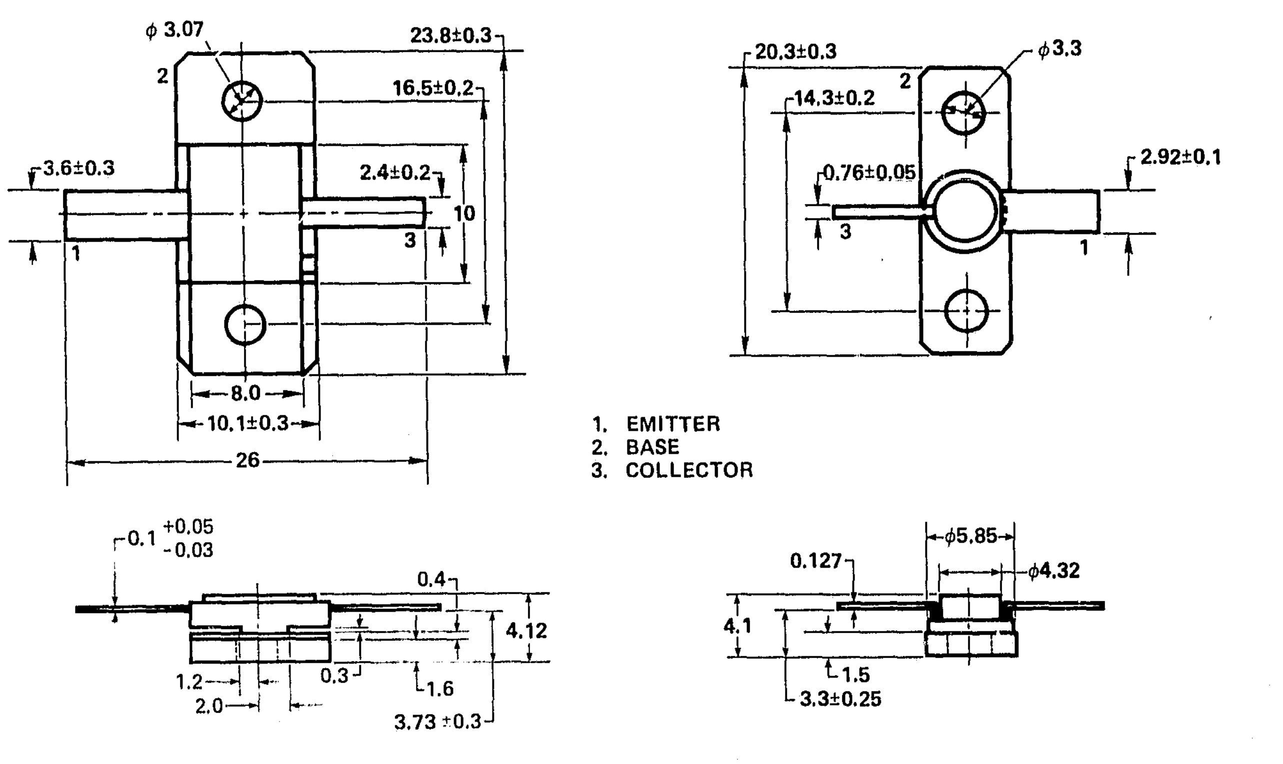
While the 5 watt device requires an internal matching network (IMN), it is optional on the 1 and 3 watt devices. Computer-aided design techniques are used to optimize device performance, input-output match, low power consumption and other electrical parameters. The Series eliminates the metal migration problem by using NEC's famous Pt-Si/Ti/Pt/Au system rather than conventional aluminun or tungsten-gold metallization. This unique system provides several orders or magnitude better reliability than conventional metallization systems, even at rated values. The Series is designed to meet the reliability requirements from industrial to military and space applications. Even the standard Grade D Industrial devices are manufactured and screened to levels of reliability unique to standard parts. Reliability is achieved from the highest grade materials, tightly controlled production processes and many years of world renown experience. Our devices offer the engineer the very best in performance, ruggedness and reliability.

*Patent pending

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

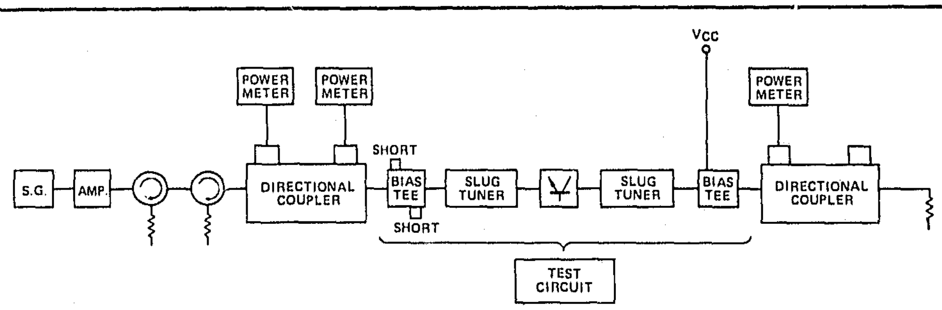
NE PART NUMBER / OTHER PART NUMBER / PACKAGE STYLE			NE4201 #705	NEM4201 T-2-A	NE4203 #705	NEM4203 T-2-A	NEM4205 T-2-A
SYMBOL	CHARACTERISTIC	UNITS					
V_{CBO}	Collector-Base Voltage	V	40	40	40	40	40
V_{CER}	Collector-Emitter Voltage (R_{BE} = 10Ω)	V	40	40	40	40	40
V_{EBO}	Emitter-Base Voltage	V	3.5	3.5	3.5	3.5	3.5
I_C	Collector Current	A	0.6	0.6	1.2	1.2	2.4
$R_{TH(J-C)}$	Thermal Resistance	°C/W	20	20	10	10	6
P_T	Total Device Dissipation	W	8.7	8.7	17.5	17.5	29
T_j	Operation Junction Temperature	°C	200	200	200	200	200
T_{stg}	Storage Temperature	°C	−65~+200	−65~+200	−65~+200	−65~+200	−65~+200

PHYSICAL DIMENSIONS (Units in mm)



T-2-A 705

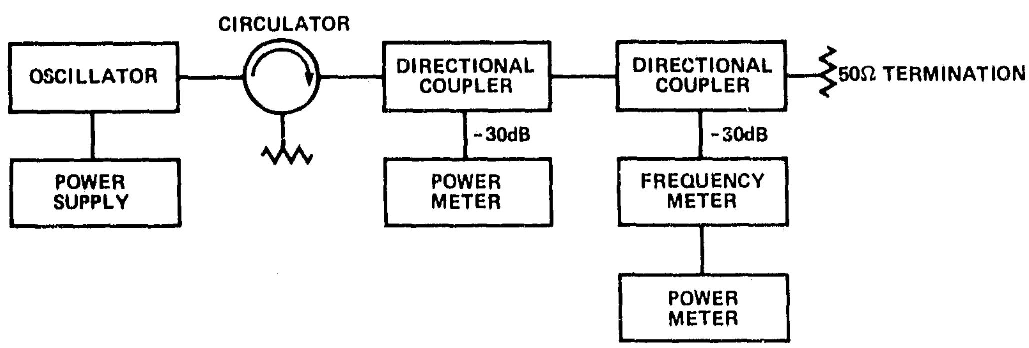
TEST CIRCUIT FOR POWER MEASUREMENT



PERFORMANCE SPECIFICATIONS (T_a=25°C)

SYMBOL	NE PART NUMBER / OTHER PART NUMBER / PACKAGE STYLE — PARAMETERS AND CONDITIONS	UNITS	NE4201 #705 MIN	TYP	MAX	NEM4201 T-2-A MIN	TYP	MAX	NE4203 #705 MIN	TYP	MAX	NEM4203 T-2-A MIN	TYP	MAX	NEM4205 T-2-A MIN	TYP	MAX
V_{OP}	Operating Voltage	V		20			20			20			20			20	
P_{OUT}	Output Power at V_{CC} = 20V, f = 4.2 GHz																
	P_{IN} = 24 dBm	dBm	31	32		31	31.5										
	P_{IN} = 30 dBm	dBm							34	35		34	35				
	P_{IN} = 33 dBm														36	37	
η_C	Collector Efficiency at V_{CC} = 20V, f = 4.2 GHz																
	P_{IN} = 24 dBm	%	25	30		20	25										
	P_{IN} = 30 dBm	%							25	30		20	25				
	P_{IN} = 33 dBm	%													20	25	
I_{CBO}	Collector Cutoff Current at V_{CB} = 20V	mA			0.25			0.25			0.5			0.5			1.0
h_{FE}	Forward Current Gain at																
	V_{CE} = 10V, I_C = 100 mA		15	40	120												
	V_{CE} = 3V, I_C = 600 mA					15	40	120									
	V_{CE} = 10V, I_C = 200 mA								15	40	120						
	V_{CE} = 3V, I_C = 1.2A											15	40	120			
	V_{CE} = 3V, I_C = 2.4A														15	40	120
C_{CB}	Output Capacitance at V_{CB} = 20V, I_E = 0V, f = 1.9 MHz	pF		2.6	3.5					4.2	5.6						

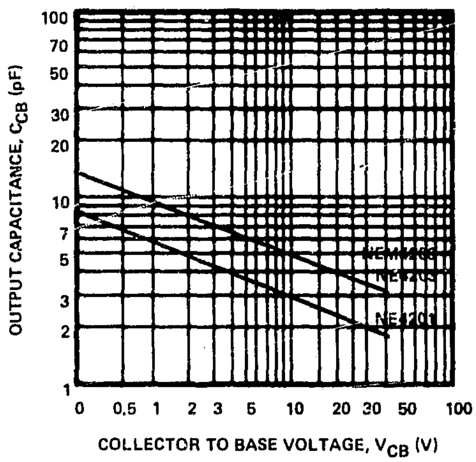
TEST CIRCUIT *FOR 4.2 GHz OSCILLATOR*



RELIABILITY SCREENING *(HES-32200; MIL-STD-750)*

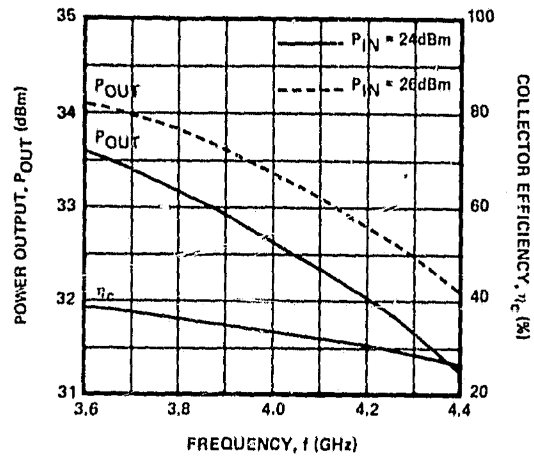
GRADE D (Industrial)	GRADE C (Military)
400°C Wafer Bake 100% DC Wafer Probe 100% Visual Inspection (Chip) Pre-cap Inspection (sample basis) 100% High Temperature Storage (200°C-24Hrs) 100% Gross Leak Tests 100% Mechanical Shock Tests 100% Group A Test	400°C Wafer Bake 100% DC Wafer Probe 100% Visual Inspection (Chip) 100% Pre-cap Inspection 100% Vacuum Bake (300°C-2Hrs) 100% High Temperature Storage (200°C-48Hrs) 100% Environmental Tests (Heat Cycle, Gross and Fine Leak, Centrifuge, Shock) 100% 168 Hour Power Burn-in at $P_c$max and T_a=25°C or $T_j$max 100% Group A Test

TYPICAL OUTPUT CAPACITANCE VS. COLLECTOR TO BASE VOLTAGE (I_E=0V, f=1.0MHz)

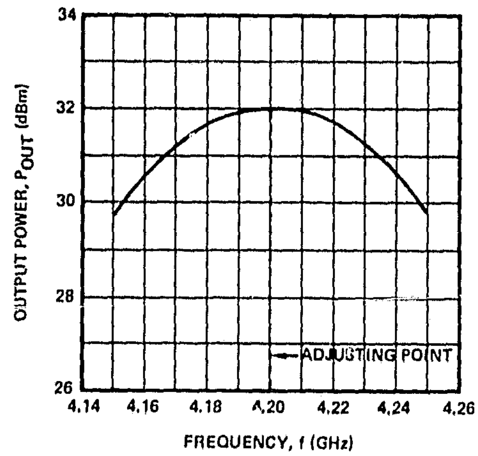


PERFORMANCE CHARACTERISTICS (T_a=25°C, CLASS C, GROUNDED BASE)

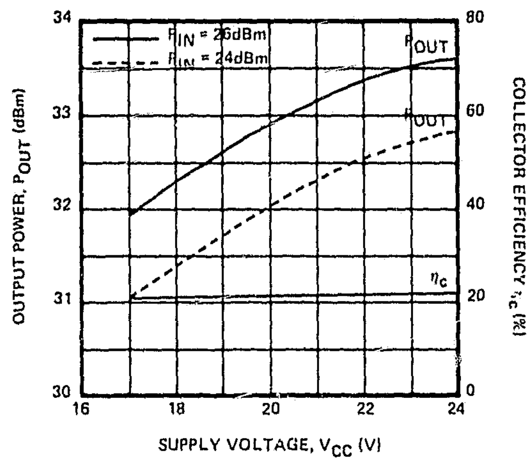
TYPICAL OUTPUT POWER AND COLLECTOR EFFICIENCY VS. FREQUENCY AT V_{CC}=20V



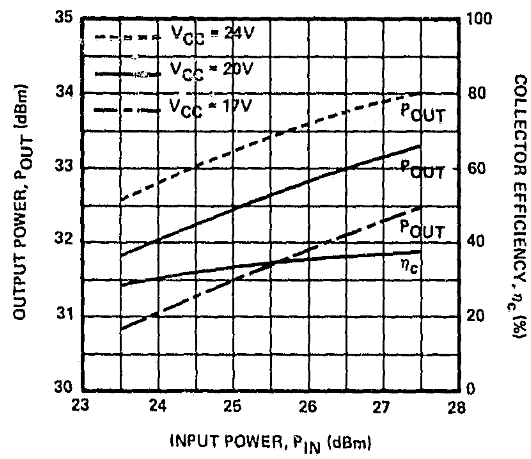
TYPICAL OUTPUT POWER VS. BANDWIDTH AT V_{CC}=20V AND P_{IN}=24dBm



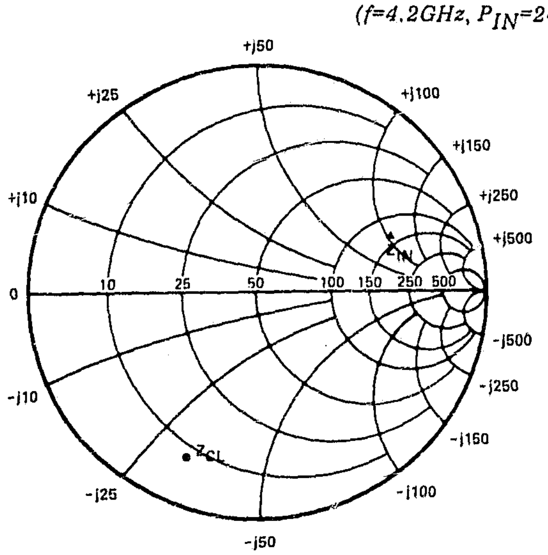
TYPICAL OUTPUT POWER AND COLLECTOR EFFICIENCY VS. SUPPLY VOLTAGE AT 4.2GHz

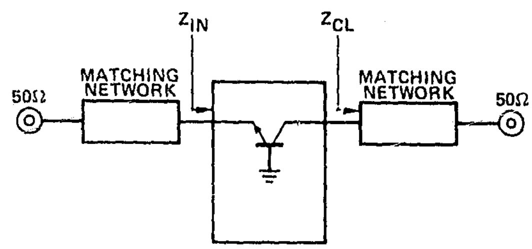


TYPICAL OUTPUT POWER AND COLLECTOR EFFICIENCY VS. INPUT POWER AT 4.2GHz AND VARIOUS SUPPLY VOLTAGES



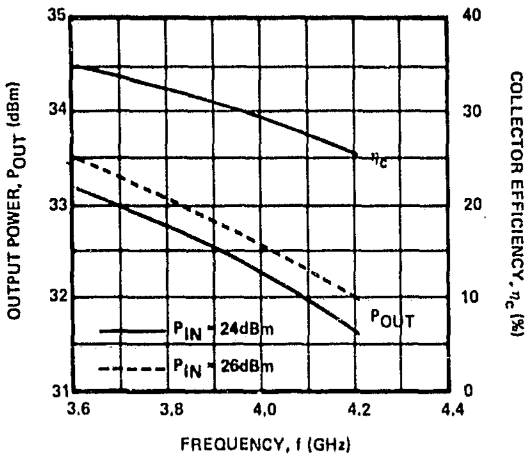
TYPICAL INPUT AND LOAD IMPEDANCE (f=4.2GHz, P_{IN}=24dBm, V_{CC}=20V, Z_{OUT}=50Ω)



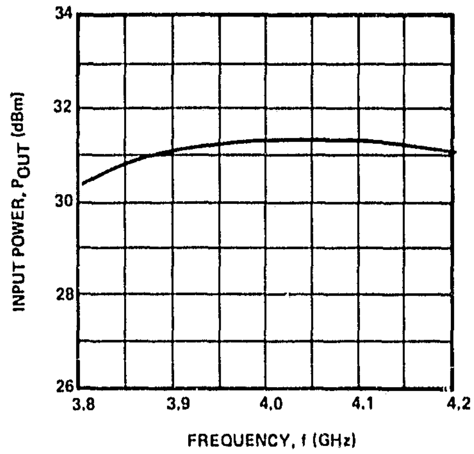


PERFORMANCE CHARACTERISTICS (T_a=25°C, CLASS C, GROUNDED BASE)

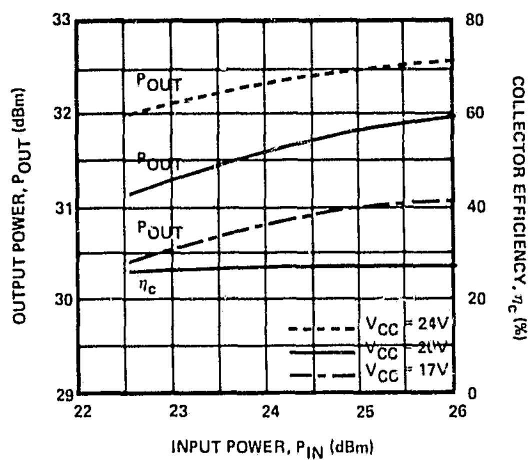
TYPICAL EFFICIENCY AND POWER OUTPUT AT V_{CC}=20V



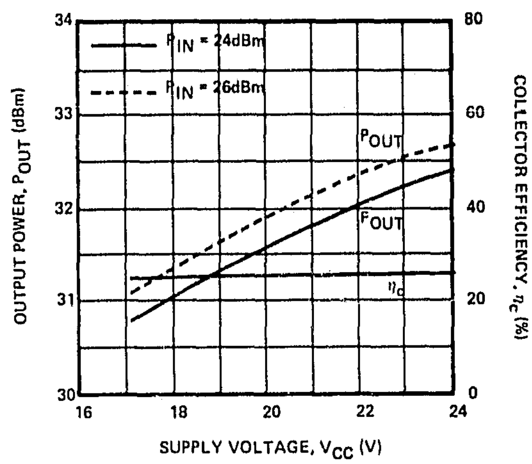
TYPICAL POWER OUTPUT VS. BANDWIDTH (V_{CC}=20V, P_{IN}=24dBm)



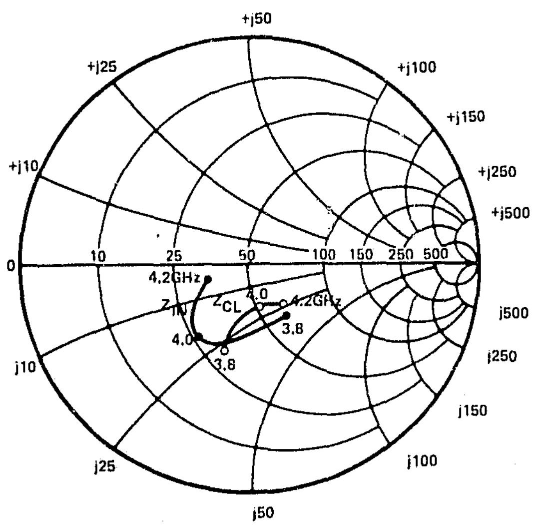
TYPICAL EFFICIENCY AND POWER OUTPUT VS. INPUT POWER AT 4.2GHz

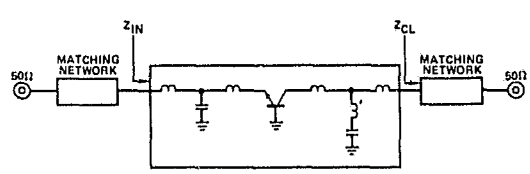


TYPICAL EFFICIENCY AND POWER OUTPUT VS. SUPPLY VOLTAGE AT 4.2GHz



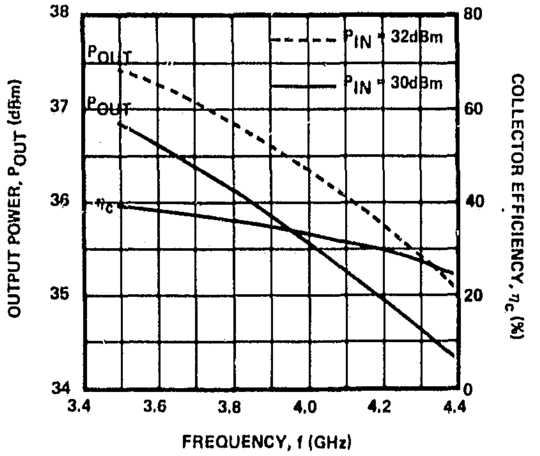
TYPICAL INPUT AND LOAD IMPEDANCES (V_{CC}=20V, P_{IN}=24dBm, Z_{OUT}=50Ω)



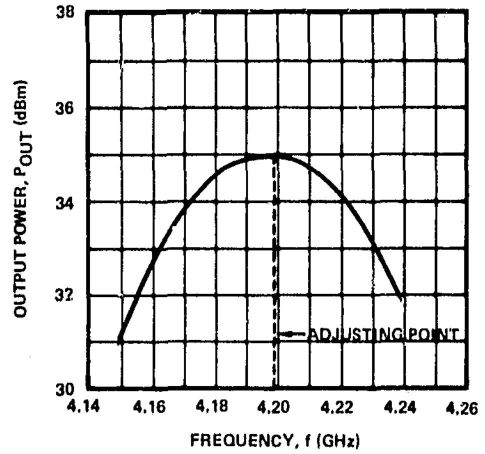


PERFORMANCE CHARACTERISTICS (T_a=25C, CLASS C, GROUNDED BASE)

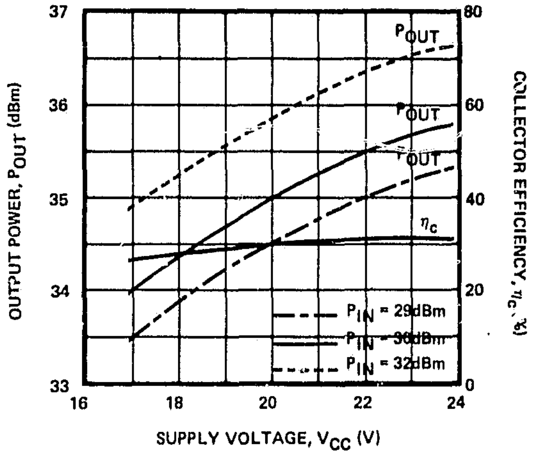
TYPICAL OUTPUT POWER AND COLLECTOR EFFICIENCY VS. FREQUENCY AT V_{CC}=20V



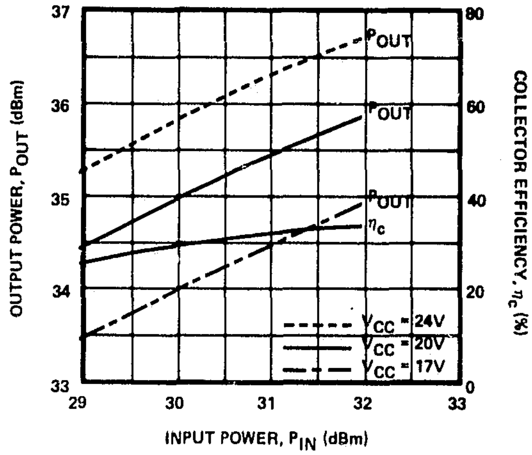
TYPICAL OUTPUT POWER VS. BANDWIDTH AT V_{CC}=20V AND P_{IN}=30dBm



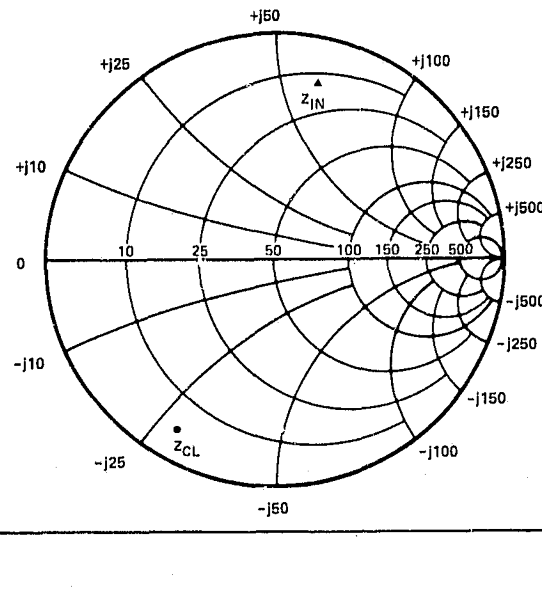
TYPICAL OUTPUT POWER AND COLLECTOR EFFICIENCY VS. SUPPLY VOLTAGE AT 4.2GHz AND VARIOUS POWER INPUTS

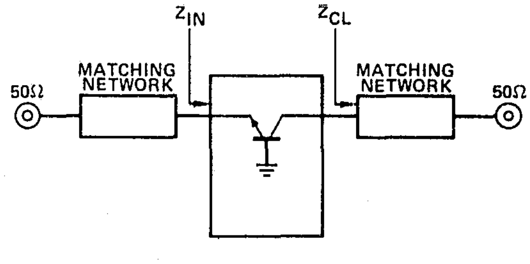


TYPICAL OUTPUT POWER AND COLLECTOR EFFICIENCY VS. INPUT POWER AT 4.2GHz



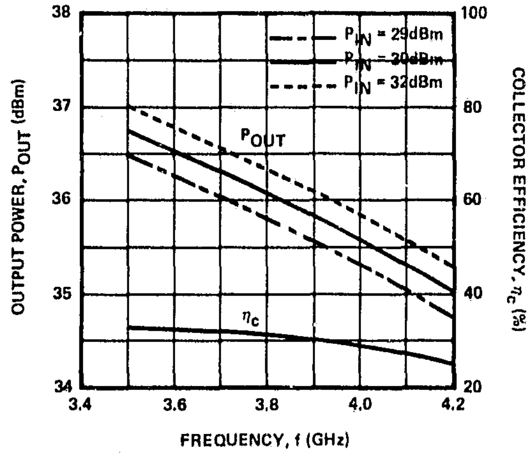
TYPICAL INPUT AND LOAD IMPEDANCES
f=4.2GHz (P_{IN}=30dBm, V_{CC}=20V, Z_{OUT}=50Ω)



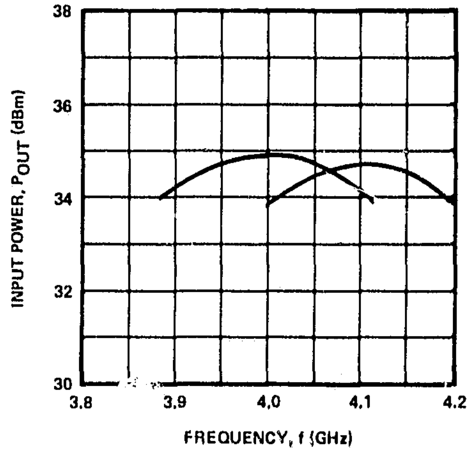


PERFORMANCE CHARACTERISTICS (T_a=25°C, CLASS C, GROUNDED BASE)

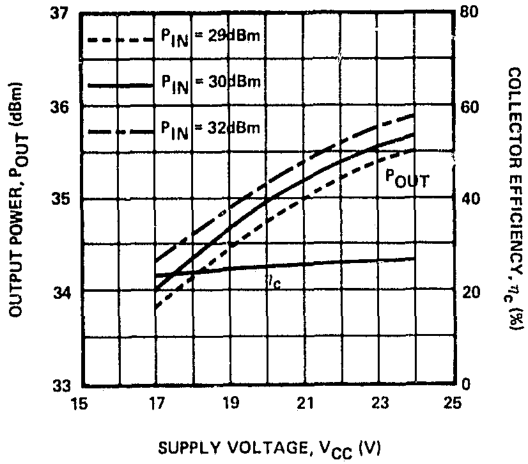
TYPICAL EFFICIENCY AND OUTPUT POWER VS. FREQUENCY AT V_{CC}=20V



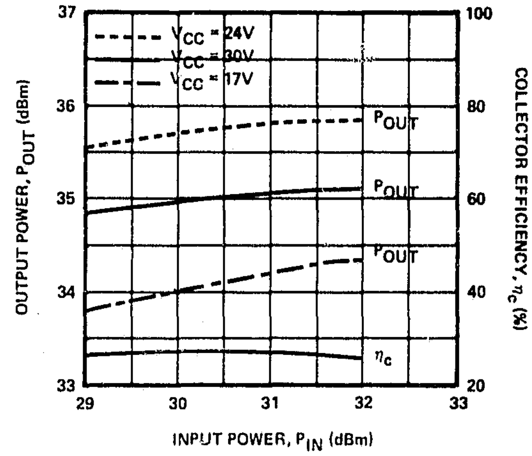
TYPICAL POWER OUTPUT AND BAND-WIDTH AT TWO DIFFERENT CENTER FREQUENCIES (V_{CC}=20V, P_{IN}=30dBm)



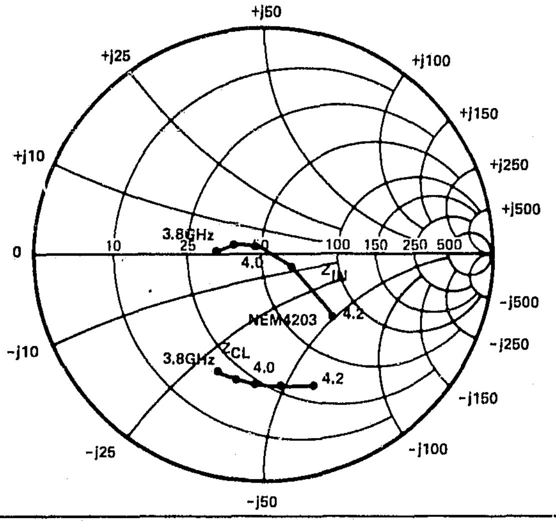
TYPICAL EFFICIENCY AND OUTPUT POWER VS. SUPPLY VOLTAGE AT 4.2GHz

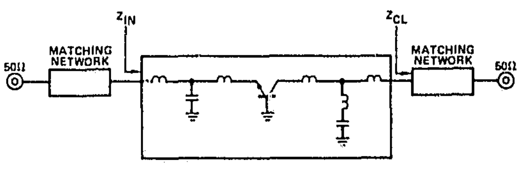


TYPICAL EFFICIENCY AND OUTPUT POWER VS. INPUT POWER AT 4.2GHz



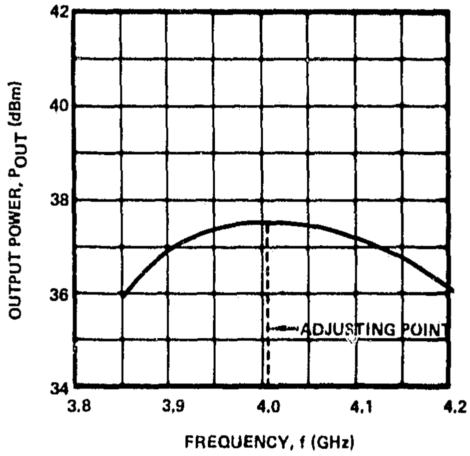
TYPICAL INPUT AND LOAD IMPEDANCES (V_{CC}=20V, P_{IN}=30dBm, Z_{OUT}=50Ω)



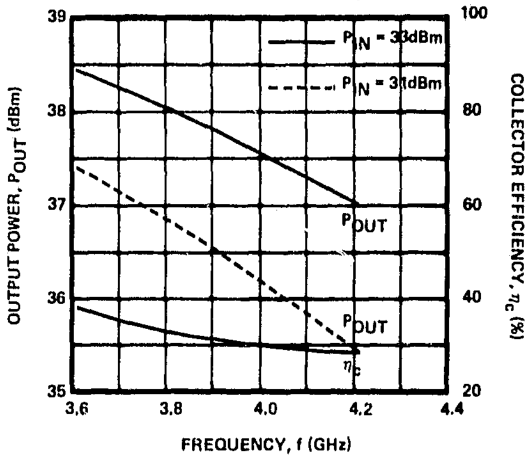


PERFORMANCE CHARACTERISTICS (T_a=25°C, CLASS C, GROUNDED BASE)

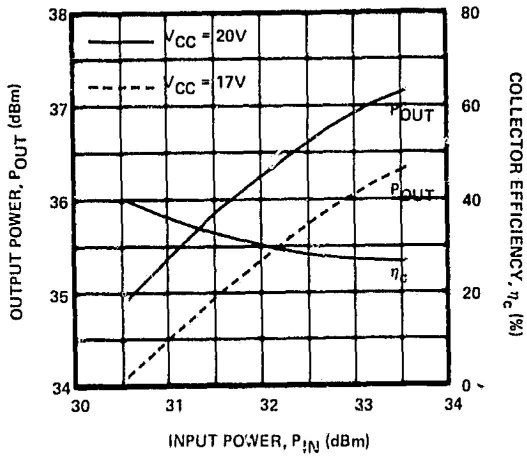
TYPICAL OUTPUT POWER VS. BANDWIDTH AT V_{CC}=20V AND P_{IN}=33dBm



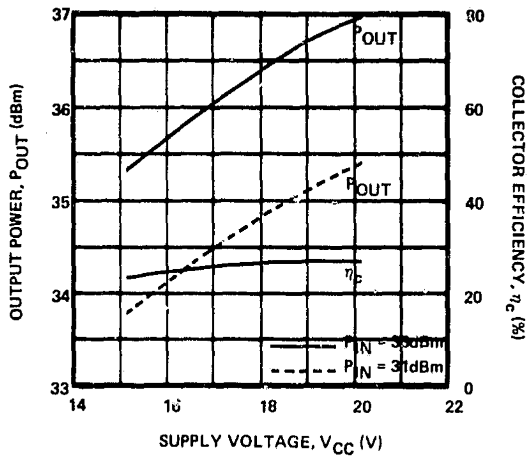
TYPICAL OUTPUT POWER AND COLLECTOR EFFICIENCY VS. FREQUENCY AT V_{CC}=20V



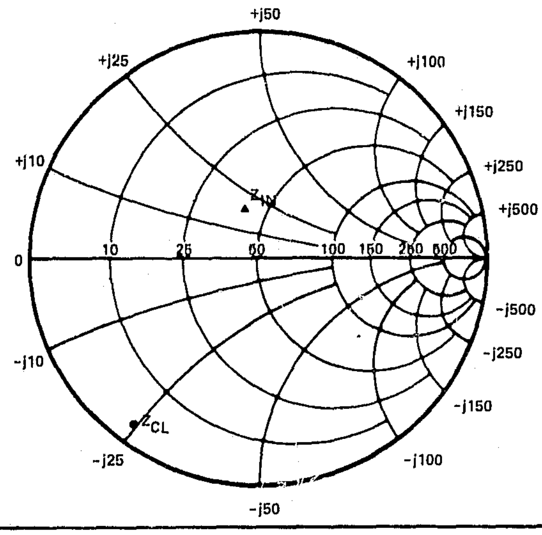
TYPICAL OUTPUT POWER AND COLLECTOR EFFICIENCY VS. INPUT POWER AT 4.2GHz

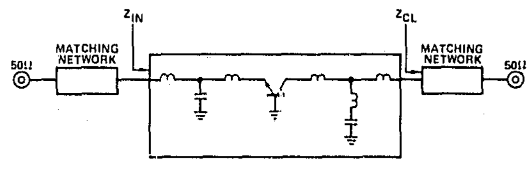


TYPICAL OUTPUT POWER AND COLLECTOR EFFICIENCY VS. SUPPLY VOLTAGE AT 4.2GHz



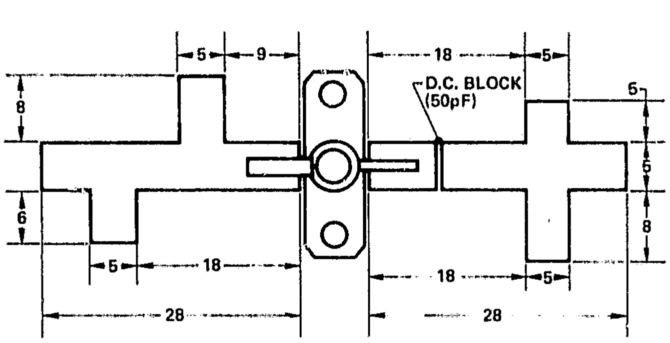
TYPICAL INPUT AND LOAD IMPEDANCE (f=4.2GHz, P_{IN}=33dBm, V_{CC}=20V, Z_{OUT}=50Ω)



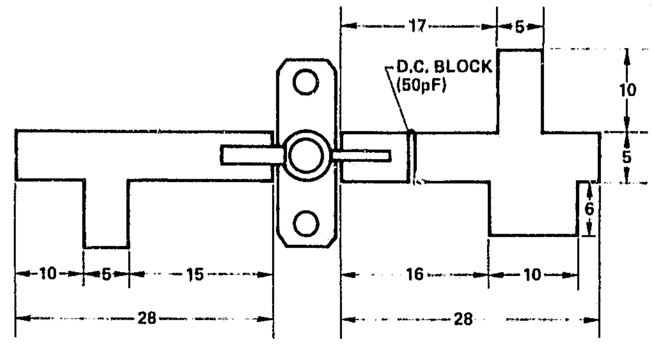


APPLICATIONS

PC BOARD LAYOUTS FOR 4.2 GHz AMPLIFIER APPLICATIONS



NE4203

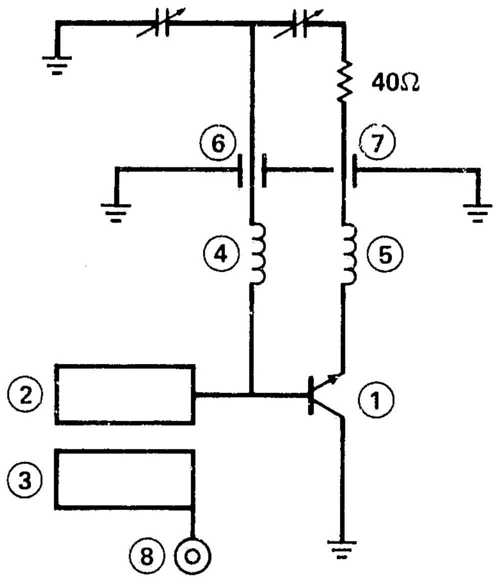


NE4201

DIMENSIONS IN MILLIMETERS

CIRCUIT LAYOUTS FOR 4.2 GHz OSCILLATOR APPLICATIONS

(#755 PACKAGE)



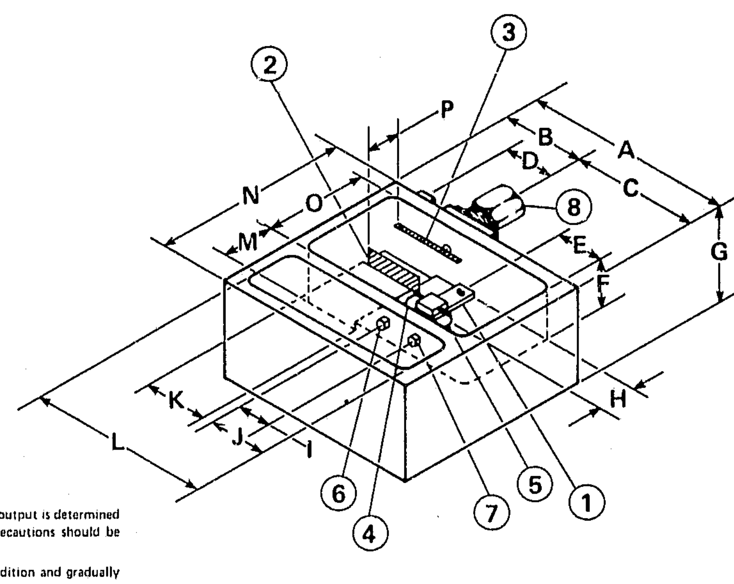
CIRCUIT

COMPONENTS

	NE4201	NE4203
(1)	Transistor	Transistor
(2)	L_1: 11x5mm Silver Plated Copper Ribbon	L_1: 10x4mm Silver Plated Copper Ribbon
(3)	L_2: 11x5mm Silver Plated Copper Ribbon	L_2: 13x1mm Silver Plated Copper Ribbon
(4)	RFC	RFC
(5)	RFC	RFC
(6)	Feed-thru Cap	Feed-thru Cap
(7)	Feed-thru Cap	Feed-thru Cap
(8)	OSM-M	OSM-M

OSCILLATOR DIMENSIONS (mm)

	NE4201	NE4203
A	38	43
B	19	18
C	19	25
D	–	10
E	10	13
F	10	10
G	25	25
H	9	9
I	8	8
J	15	14
K	–	14
L	30	33
M	10	11
N	40	40
O	16	16
P	5	6.5
Q	4	2.5



CONSTRUCTION

The frequency of oscillation is determined by the length of L_1. The maximum power output is determined by the shape of L_2, spacing between and heights of L_1 and L_2. The following precautions should be observed.

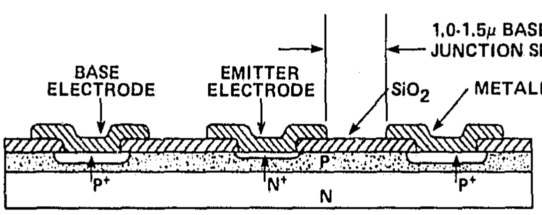
1. The measurement of the oscillator power output should start at a low bias condition and gradually increase to the operating condition to prevent possible destruction of the transistor.
2. The oscillators must have the metal covers attached for proper measurement.

NEC'S SET TECHNOLOGY

The Stepped Electrode Transistor (SET) structure was developed to primarily reduce the base-collector capacitance and base resistance by realizing a virtual "zero-gap" between the emitter junction and base metallization. In conventional processes, the distance between electrodes is limited by the alignment tolerance of various masks used for the emitter and base diffusion contact window masking and final etching. Even the most sophisticated masking and alignment techniques presently used are limited to about 1μ electrode spacing under the best laboratory conditions, but more typically about 1.5μ on a production basis.

The figure compares NEC's new patented SET structure to that of a conventional device. As indicated, each emitter electrode is built up on a truncated mesa of polysilicon with an over-hanging edge for the emitter metallization. The spacing between the emitter junction and base metallization is reduced to 0.3-0.4μ. The entire process is accomplished without a metal etch and has eliminated the requirement for separate contact windows.

The new transistors use a double epitaxial structure with the top layer much thinner than the bottom layer. The collector depletion layer "reaches through" the first layer with normal collector biasing. This results in a greater safe-operating area. The base diffusion area is formed in the conventional manner, followed by the disposition of a layer of arsenic doped poly-crystalline silicon and then a layer of undoped polysilicon. Using the fact that As doped polysilicon (As DOPOS) has a higher rate of etching than undoped polysilicon, the resulting truncated electrode structure is formed, using the silicon dioxide film as a self-aligning etching mask.

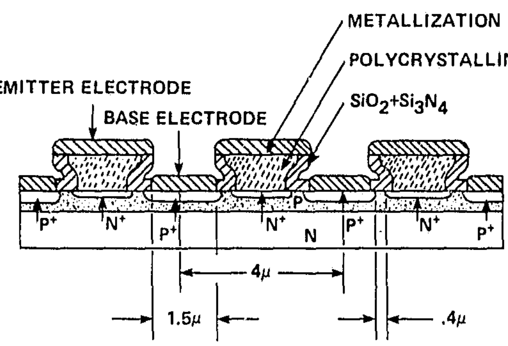


CONVENTIONAL POWER TRANSISTOR STRUCTURE USING EITHER ALUMINUM OR TUNGSTEN GOLD METALLIZATION (MTTF MEASURED IN THOUSANDS OF HOURS)

Various emitter ballasting techniques are used to improve temperature uniformity and sharing between and within each base area. Conventional techniques use thin-film or diffused resistors in series with each emitter electrode. As a localized non-uniformity forces more current to be drawn to a given electrode, the increased voltage drops across its ballast resistor and effectively de-biases that electrode, reducing its current, resulting in a more uniform distribution of current and heat. The new SET structure performs this task inherently with high current and with no fear of migration. Diffused resistors also have the drawback of providing feed-back between the emitter and the collector when used in common-based configurations.

The new SET emitter structure of polycrystalline silicon is a far superior way of distributing emitter current. It reduces the need for separate emitter ballasting resistors, and in some cases, eliminates them entirely. This results in SET devices operating at lower junction temperatures than conventional devices; ergo, much better reliability.

Another noteworthy technique also used is in the reduction of the MOS capacitance formed by the electrode pads. The MOS capacitance acts as feedback capacitance and lowers the high frequency characteristics. To reduce this, NEC has introduced an insulating film of low-dielectric contant porous silicon dioxide under the base and emitter pads. This technique reduces the parasitic capacitance of the pads by 50%. This also allows for better, less complicated internal matching which was previously responsible for the loss of as much as 1 to 2dB power gain in conventional power devices.



NEC'S SET TECHNOLOGY (MTTF MEASURED IN 10^5-10^6 HOURS)

To optimize device and circuit characteristics for input-output, match and lowest power consumption and other electrical parameters, internal matching networks (IMN) are employed. IMNs can be tailored by computer aid design techniques to fit customer's band-width performance requirements.

The networks are incorporated in a new BeO hermetically sealed stripline package designed to withstand the rigors of space qualification. Specifically, IMN is designed to allow for greater bandwidth, higher efficiency, lower junction temperatures and higher reliability.

Data subject to change without notice.

HEWLETT hp PACKARD

COMPONENTS

LINEAR POWER MICROWAVE TRANSISTOR

HXTR-5101

TENTATIVE DATA JUNE 1978

Features

HIGH P_{1dB} LINEAR POWER
23 dBm Typical at 2 GHz
22 dBm Typical at 4 GHz

HIGH P_{1dB} GAIN
13 dB Typical at 2 GHz
7.5 dB Typical at 4 GHz

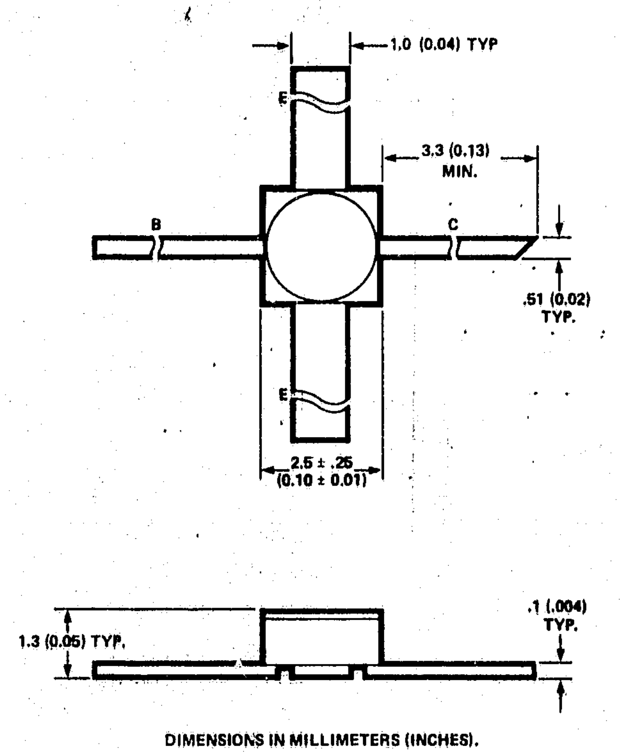
LOW DISTORTION

HIGH POWER-ADDED EFFICIENCY

MATCHING CONDITIONS INDEPENDENT OF OUTPUT POWER

INFINITE SWR TOLERANCE ABOVE 2 GHz

RUGGED HERMETIC PACKAGE



HPAC-100 Package Outline

Description/Applications

The HXTR-5101 is an NPN bipolar transistor designed for high output power and gain up to 5 GHz. To achieve excellent uniformity and reliability, the manufacturing process utilizes ion implantation, self-alignment techniques and Ti/Pt/Au metallization. The chip has a dielectric scratch protection over its active area and Ta_2N ballast resistors for ruggedness.

The superior gain, power, and distortion performance of the HXTR-5101 commend it for applications in radar, ECM, space, and commercial and military telecommunications. The HXTR-5101 features both guaranteed power output and associated gain at 1 dB gain compression.

The HXTR-5101 is supplied in the HPAC-100, a metal/ceramic hermetic package, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

Electrical Specifications at T_{CASE} = 25°C

Symbol	Parameters and Test Conditions	Test MIL-STD-750	Units	Min.	Typ.	Max.
BV_{CBO}	Collector-Base Breakdown Voltage at I_C = 3mA	3001.1*	V	40		
BV_{CEO}	Collector-Emitter Breakdown Voltage at I_C = 15mA	3011.1*	V	24		
BV_{EBO}	Emitter-Base Breakdown Voltage at I_B = 30μA	3026.1*	V	3.3		
I_{EBO}	Emitter-Base Leakage Current at V_{EB}=2V	3061.1	μA			2
I_{CES}	Collector-Emitter Leakage Current at V_{CE}=32V	3041.1	nA			200
I_{CBO}	Collector-Base Leakage Current at V_{CB}=20V	3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio at V_{CE}=18V, I_C = 30mA	3076.1*		15	40	75
P_{1dB}	Power Output at 1dB Gain Compression f= 2GHz 4GHz		dBm	 21	23 22	
G_{1dB}	Associated 1dB Compressed Gain 2GHz 4GHz		dB	 6.5	13 7.5	
P_{SAT}	Saturated Power Output (8dB Gain) 2GHz (3dB Gain) 4GHz		dBm		25.5 25	
η	Power-Added Efficiency at 1dB Compression 2GHz 4GHz		%		35 24	
IMD	Third Order Intermodulation Distortion (Reference to either tone), at Po(PEP)= 22dBm 4GHz		dB		-30	
	Tuned for Maximum Output Power at 1dB Compression V_{CE}=18V, I_C=30mA					

*300μsec wide pulse measurement at ≤2% duty cycle.

Maximum Ratings at T_{CASE} = 25°C

Symbol	Parameter	Limits
V_{CBO}	Collector to Base Voltage	40V
V_{CEO}	Collector to Emitter Voltage	22V
V_{EBO}	Emitter to Base Voltage	3.3V
I_C	D.C. Collector Current	50mA
P_T	Total Device Dissipation*	700mW
T_J	Junction Temperature	200°C
T_{STG}	Storage Temperature	-65°C to +200°C
—	Lead Temperature (Soldering, 10 seconds each lead)	+250°C

*See Figure 1 for derating conditions.

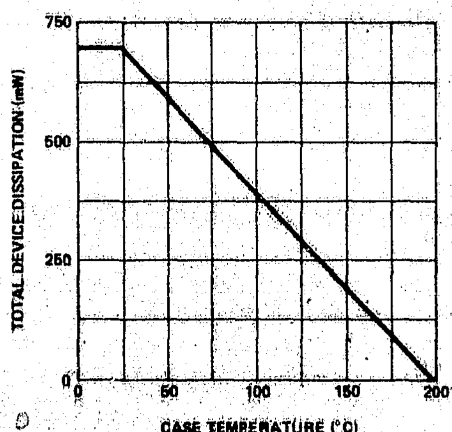


Figure 1. Maximum Power Dissipation Curve for θ_{jc} = 250°C/W, T_{JMAX} = 200°C.

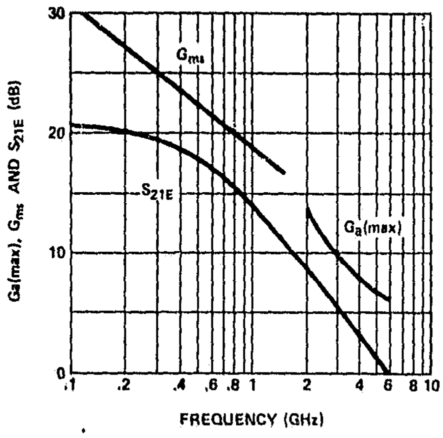


Figure 2. Typical G_a(max), Maximum Stable Gain (G_{ms}), and S_{21E} vs. Frequency for V_{CE} = 18V, I_C = 30mA.

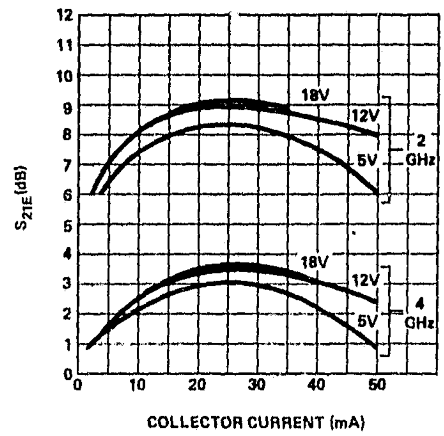


Figure 3. Typical S_{21E} vs. Current at 2 and 4GHz.

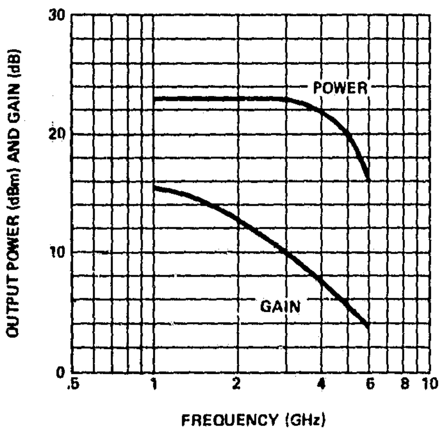


Figure 4. Typical P_{1dB} Linear Power and Associated 1dB Compressed Gain vs. Frequency at V_{CE} = 18V, I_C = 30mA.

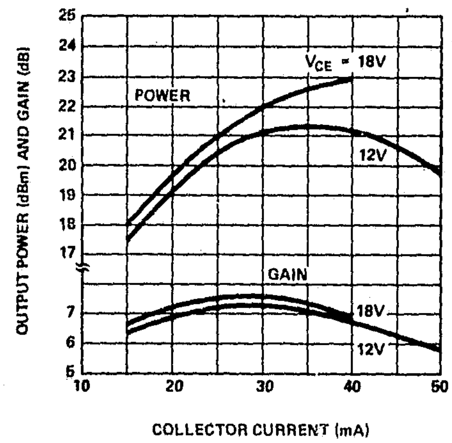


Figure 5. Typical P_{1dB} Linear Power and Associated 1dB Compressed Gain vs. Current at V_{CE} = 12 and 18V at 4GHz.

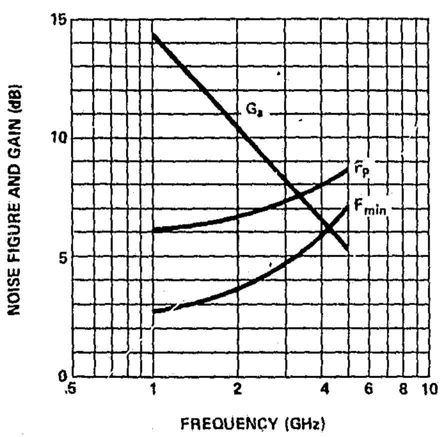


Figure 6. Typical Noise Figure (Fmin) and Associated Gain (G_a) when tuned for Minimum Noise vs. Frequency at V_{CE} = 18V, I_C = 10mA. Typical Noise Figure (Fp) when tuned for Max P_{1dB} at V_{CE} = 18V, I_C = 30mA.

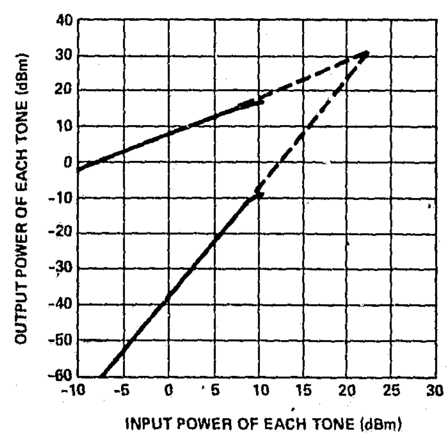


Figure 7. Typical Two Tone 3rd Order Intermodulation Distortion at 4GHz for a frequency separation of 5MHz at V_{CE} = 18V, I_C = 30mA.

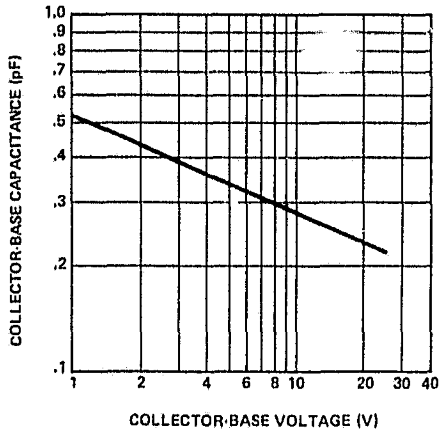


Figure 8. Typical Collector-Base Capacitance (emitter guarded) vs. Collector-Base Voltage, at 1 MHz.

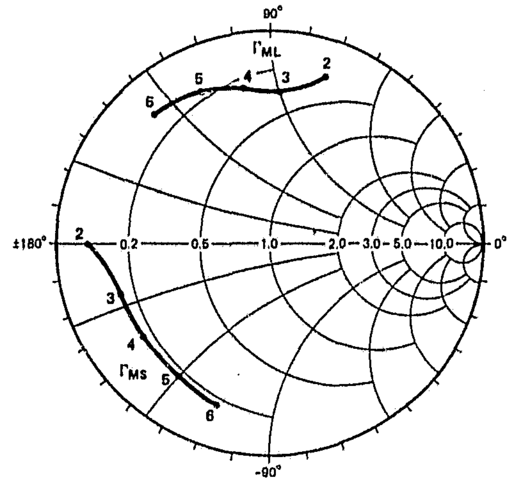


Figure 9. Typical Γ_{MS}, Γ_{ML}, (calculated from the average S-parameters) in the 2 to 6GHz frequency range, for V_{CE} = 18V, I_C = 30mA.

Typical S-Parameters V_{CE} = 18V, I_C = 30mA

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (GHz)	**Mag.**	**Ang.**	**(dB)**	**Mag.**	**Ang.**	**(dB)**	**Mag.**	**Ang.**	**Mag.**	**Ang.**
0.100	0.80	-19	20.6	10.7	165	-37	0.01	77	0.98	-8
0.200	0.78	-37	20.1	10.2	154	-31	0.02	67	0.94	-15
0.300	0.75	-53	19.5	9.44	143	-28	0.03	60	0.88	-21
0.400	0.72	-68	18.7	8.63	133	-27	0.04	53	0.83	-26
0.500	0.68	-81	17.9	7.87	124	-26	0.05	47	0.78	-30
0.600	0.66	-92	17.0	7.15	117	-25	0.05	42	0.73	-33
0.700	0.64	-102	16.2	6.52	110	-24	0.06	39	0.69	-36
0.800	0.62	-111	15.5	5.96	104	-24	0.06	36	0.66	-38
0.900	0.61	-119	14.8	5.49	99	-23	0.06	33	0.64	-41
1.000	0.60	-126	14.1	5.08	94	-23	0.06	31	0.61	-43
1.500	0.56	-151	11.2	3.64	75	-23	0.07	25	0.55	-51
2.000	0.55	-169	8.9	2.80	59	-22	0.08	22	0.52	-61
2.500	0.56	179	7.2	2.29	45	-21	0.08	21	0.53	-72
3.000	0.55	168	5.7	1.93	33	-21	0.09	21	0.52	-79
3.500	0.56	158	4.5	1.69	21	-20	0.09	20	0.55	-89
4.000	0.54	148	3.5	1.50	10	-19	0.10	19	0.58	-96
4.500	0.54	137	2.5	1.33	0	-19	0.11	18	0.58	-106
5.000	0.52	128	1.6	1.21	-11	-18	0.12	16	0.62	-113
5.500	0.54	115	1.0	1.12	-23	-17	0.13	14	0.60	-122
6.000	0.54	108	0.0	1.01	-32	-17	0.14	11	0.64	-132

Typical S-Parameters V_{CE} = 15V, I_C = 15mA

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (GHz)	**Mag.**	**Ang.**	**(dB)**	**Mag.**	**Ang.**	**(dB)**	**Mag.**	**Ang.**	**Mag.**	**Ang.**
0.100	0.80	-18	19.4	9.35	166	-37	0.01	78	0.98	-7
0.200	0.78	-35	19.1	9.07	155	-31	0.02	69	0.95	-14
0.300	0.76	-50	18.5	8.44	145	-28	0.03	61	0.91	-20
0.400	0.73	-64	17.8	7.79	135	-26	0.04	55	0.86	-25
0.500	0.69	-77	17.1	7.16	127	-25	0.05	49	0.81	-29
0.600	0.67	-88	16.3	6.56	119	-24	0.06	44	0.76	-32
0.700	0.64	-97	15.5	6.02	113	-23	0.06	40	0.72	-35
0.800	0.62	-107	14.8	5.54	107	-23	0.06	37	0.69	-38
0.900	0.60	-115	14.2	5.13	10[illegible]	-23	0.07	34	0.66	-40
1.000	0.60	-122	13.5	4.76	96	-23	0.07	32	0.63	-43
1.500	0.57	-148	10.8	3.47	76	-22	0.08	24	0.57	-53
2.000	0.55	-166	8.6	2.69	60	-21	0.08	21	0.54	-63
2.500	0.56	-178	6.9	2.21	46	-21	0.09	19	0.55	-75
3.000	0.56	171	5.1	1.80	36	-20	0.09	21	0.50	-85
3.500	0.56	160	4.3	1.65	21	-20	0.10	18	0.56	-91
4.000	0.53	151	3.3	1.47	10	-19	0.11	18	0.59	-99
4.500	0.53	141	2.3	1.30	0	-19	0.11	17	0.59	-108
5.000	0.50	130	1.5	1.18	-10	-18	0.12	15	0.62	-116
5.500	0.52	118	0.8	1.10	-22	-17	0.14	13	0.61	-124
6.000	0.53	110	0.0	0.99	-31	-16	0.15	11	0.64	-135

NEC

NE869

PRELIMINARY DATA SHEET

K-Band GaAs Power FET Series

FEATURES

- HIGH LINEAR POWER
- LOW DISTORTION
- HIGH RELIABILITY
- HIGH POWER-ADDED EFFICIENCY
- HIGH BREAKDONW VOLTAGE
- RECESSED GATE
- MIL HERMETIC PACKAGES

DESCRIPTION AND APPLICATIONS

The NE869 Series of power GaAs FET's employ the latest advances in semiconductor technology. A unique recessed gate structure provides the FET's with high breakdown and operating voltages which in turn provide high power, gain and efficiency. The chips are capable of operating with drain voltages up to 13V. The Series use the NE869100 as a building block to achieve a variety of ratings. The engineer can choose his particular power ratings by having multiple chips included in a single hermetically sealed package. The Series provide excellent performance for use in K-Band amplifier and oscillator applications from industrial to hi-rel space.

PERFORMANCE SPECIFICATIONS (T_a=25°C)

NE PART NUMBER			NE869099*			NE869199*			NE869299*			NE869499*		
PACKAGE CODE			99			99			99			99		
SYMBOL	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
I_{DSS}	Drain Current at V_{DS} = 3V	mA	80	120	160	160	220	280	320	450	600	800	950	1200
V_P	Pinch-off Voltage													
	at V_{DS} = 3V, I_{DS} = 2mA	V	-3.5	-5.5										
	I_{DS} = 5mA	V				-3.5	-5.5							
	I_{DS} = 10mA	V							-3.5	-5.5				
	I_{DS} = 20mA	V										-3.5	-5.5	
gm	Transconductance													
	at V_{DS} = 3V, I_{DS} = 30mA	m℧	15	20										
	I_{DS} = 50mA	m℧				25	40							
	I_{DS} = 100mA	m℧							55	80				
	I_{DS} = 250mA	m℧										110	160	
P_{OUT}	Power Output at 1 dB Compression Point at V_{DS} = 10V, f = 11 GHz													
	P_{IN} = 12.0 dBm	W		0.10										
	P_{IN} = 18.0 dBm	W					0.25							
	P_{IN} = 21.5 dBm	W								0.50				
	P_{IN} = 24.5 dBm	W											1.00	
P_{SAT}	Saturated Power Output at V_{DS} = 10V, f = 11 GHz													
	I_{DS} = 40mA	W		0.25										
	I_{DS} = 70mA	W					0.44							
	I_{DS} = 150mA	W								0.87				
	I_{DS} = 300mA	W											1.74	
G_P	Linear Power Gain at V_{DS} = 10V, f = 11 GHz													
	I_{DS} = 40mA	dB		8.0										
	I_{DS} = 70mA	dB					7.0							
	I_{DS} = 150mA	dB								6.5				
	I_{DS} = 300mA	dB											6.5	

*Available in chip form.

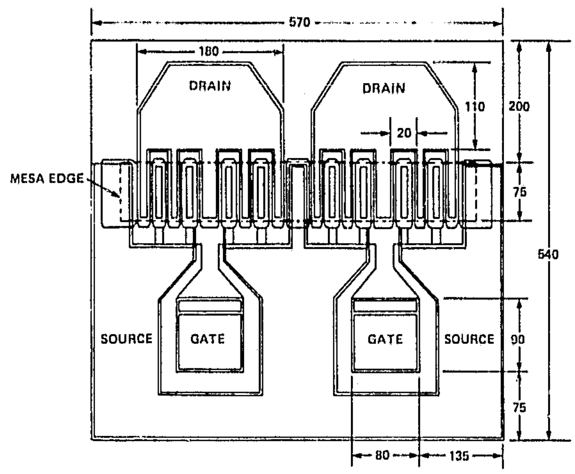
ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

NE PART NUMBER NUMBER OF CHIPS NUMBER OF CELLS PACKAGE CODE			NE869099* 99	NE869199* 1 1 99	NE869299* 1 2 99	NE869499* 1 4 99
SYMBOL	CHARACTERISTICS	UNITS				
V_{DS}	Drain to Source Voltage	V	20	20	20	20
V_{GS}	Gate to Source Voltage	V	-12	-12	-12	-12
I_{DS}	Drain to Source Current	mA	160	280	600	1200
$R_{th(C\text{-}A)}$	Thermal Resistance	°C/W	120	100	60	30
P_T	Total Power Dissipation (T_c = 25°)	W	1.25	1.5	2.5	5.0
T_{ch}	Channel Temperature	°C	175	175	175	175
Tstg	Storage Temperature	°C	-65 ~ +175	-65 ~ +175	-65 ~ +175	-65 ~ +175

*Available in chip form.

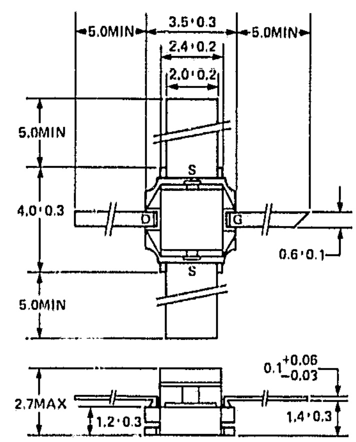
PHYSICAL DIMENSIONS

*CHIP**
(Units in μm)



*One chip containing two cells (NE869200)

99 PACKAGE
(Units in mm)

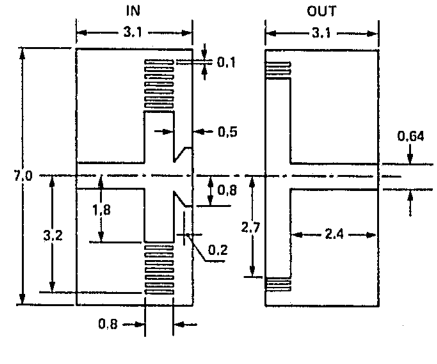


RELIABILITY SCREENING *(HES-32325-02)*

GRADE D (Industrial) 200-1200 Failures in 10^9 Device Hours (FIT)	GRADE C (Military) 50-300 Failures in 10^9 Device Hours (FIT)
100% DC Wafer Probe Pre-Cap Inspection (sample basis) 100% Gross Leak Test 100% Mechanical Shock Test 100% Group A Tests (Tests may vary depending upon package style.)	100% DC Wafer Probe 100% Pre-Cap Inspection 100% Vacuum Bake (150°C - 1 hr) 100% Gross Leak Test 100% High Temperature Storage (125°C – 24 hrs) 100% Environmental Tests 100% Power Burn-in at P_c max (T_{ch} = 125°C, T_a = 100°C – 168 hrs) 100% Group A Tests

TEST CIRCUIT *(Units in cm)*

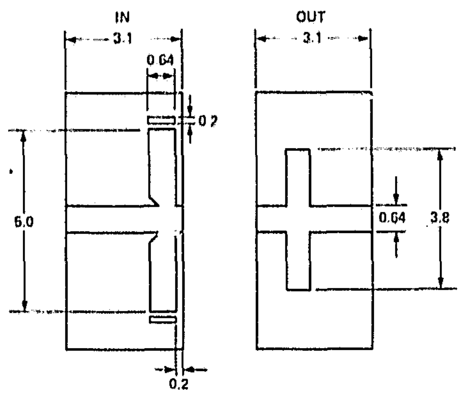
11 GHz TEST CIRCUIT FOR THE NE8694



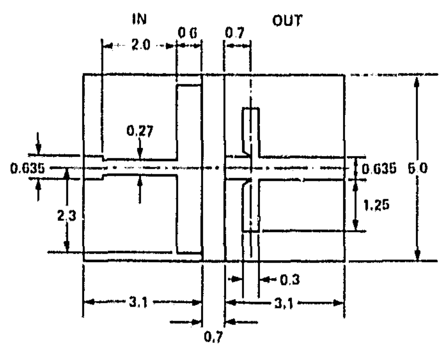
74

TEST CIRCUIT *Continued (Units in cm)*

11 GHz TEST CIRCUIT FOR THE NE8692

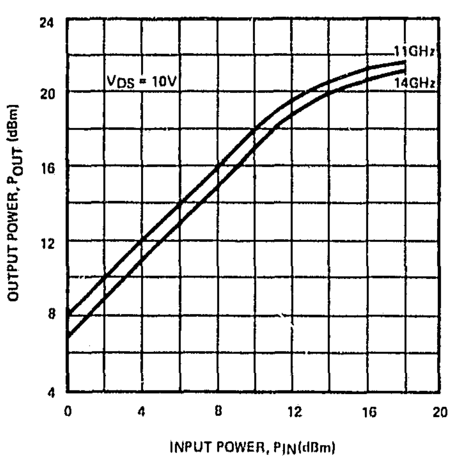


14 GHz TEST CIRCUIT FOR THE NE8692

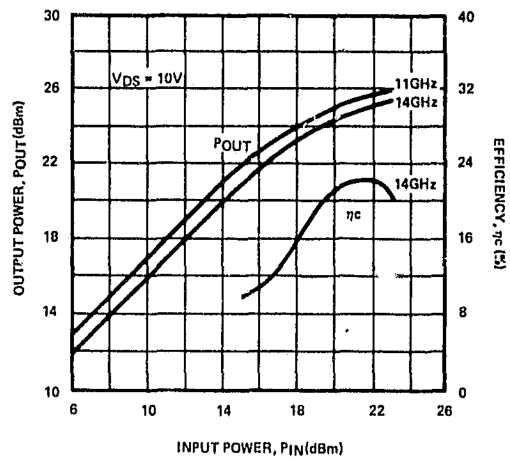


PERFORMANCE CHARACTERISTICS (T_a = 25 C

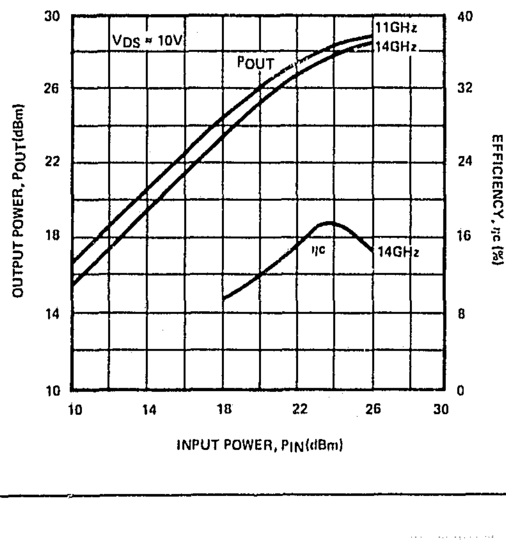
TYPICAL OUTPUT POWER VS INPUT POWER FOR THE NE8690



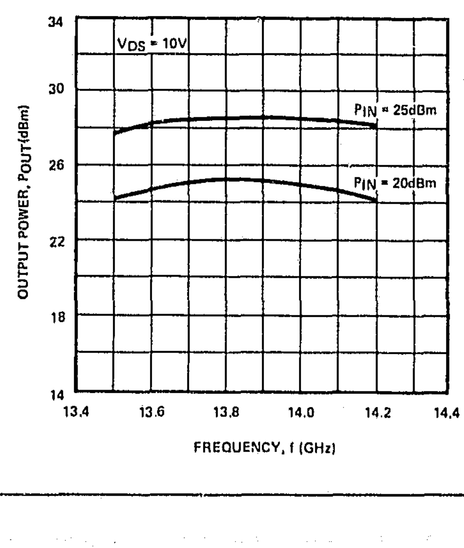
TYPICAL OUTPUT POWER AND EFFICIENCY VS INPUT POWER FOR THE NE8691



TYPICAL OUTPUT POWER AND EFFICIENCY VS INPUT POWER FOR THE NE8692

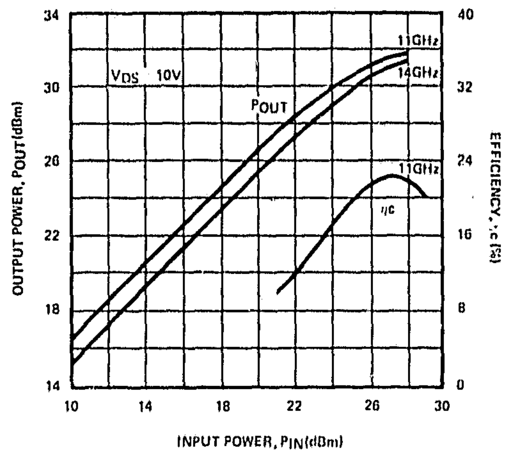


TYPICAL OUTPUT POWER VS FREQUENCY FOR THE NE8692

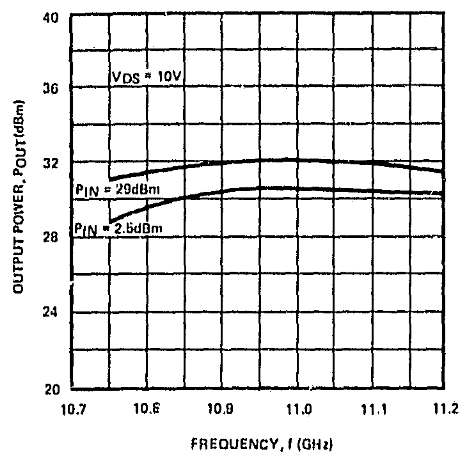


PERFORMANCE CHARACTERISTICS ($T_a = 25°C$)

TYPICAL OUTPUT POWER AND EFFICIENCY VS INPUT POWER FOR THE NE8694



TYPICAL OUTPUT POWER VS FREQUENCY FOR THE NE8684



HANDLING PRECAUTIONS

DIE ATTACHMENT

The backs of the NE869000, NE869100, NE869200 and NE869400 are metallized with about 1.5 microns of pure gold. Attachment can be accomplished with either Au-Ge (390±10°C) or Au-Sn (290±10°C) preforms. The particular method used would depend upon the bonding technique used and what the maximum temperatures the chip-substrate assembly would be exposed to. NEC uses Au-Ge preforms because the package is capped and sealed with Au-Sn. The thermal resistance of the NE869000 is 115°C/W, 95°C/W for the NE869100, 55°C/W for the NE869200 and 25°C/W for the NE869400, so if gold or silver epoxy is used, care should be taken to minimize the total resistance.

BONDING

When the chip is connected to the substrate, it must be done in such a manner that maximizes the chip's performance while not degrading its reliability. Since lead inductance effects the performance dramatically, it is recommended that the gate and drain bonding wires be half-hard gold wire (3-8% elongation) less than or equal to 30 microns in diameter. The lengths should be as short as possible. The source should be connected with either gold tape (ribbon) or mesh.

Bonding should be accomplished with a wedge tip with a taper of approximately 15%. Die attach and bonding time should be kept to a minimum, thus the FET chips should be the last components to be bonded on the circuit. As a general rule, the bonding operation should be kept within a 300°C – 10 minute curve. If longer periods are required, the temperature should be lowered.

EQUIPMENT

The user must operate in a clean, dry environment. The chip channel is glassivated for mechanical protection only and does not preclude the necessity of a clean environment.

The bonding equipment should be periodically checked for sources of surge voltage and should be properly grounded at all times. In fact, all test and handling equipment should be grounded to minimize the possibilities for static discharge.

NEC MICROWAVE DIODE SERIES
ND8 Si DDR PULSED IMPATT

PRELIMINARY DATA SHEET

HIGH PULSED POWER SILICON DOUBLE DRIFT IMPATT DIODES

ND80196-1T	1.0 WATTS	AT	96GHz	&	4.0%	EFFICIENCY
ND80535-1P	5.0 WATTS	AT	35GHz	&	5.0%	EFFICIENCY
ND81015-5H	13.0 WATTS	AT	15GHz	&	9.0%	EFFICIENCY
ND81510-5H	18.0 WATTS	AT	10GHz	&	10.0%	EFFICIENCY
ND84010-6K	40.0 WATTS	AT	10GHz	&	10.0%	EFFICIENCY

FEATURES

- HIGH PULSED POWER
- HIGH EFFICIENCY
- DIAMOND HEAT SINKS
- HIGH RELIABILITY

RICHARD CONANT
CALIFORNIA EAST LABS
2659 TOWNSGATE R
WESTLAKE VILLAGE, CA 91361
213 - 991-4436

DESCRIPTION AND APPLICATIONS

The NEC ND8 Si DDR Pulsed IMPATT (Impact Ionization Avalanche Transit Time) diode Series offer high pulsed power at frequencies up to 96 GHz for industrial and military applications. The Series use a double drift region arranged in a ring structure, consisting of p^+nn^+ and n^+pp^+ type elements with a common avalanche junction. The wider pulsed diodes use diamond heat sinks which allow for more efficient heat dissipation. This results in lower junction temperatures and longer life.

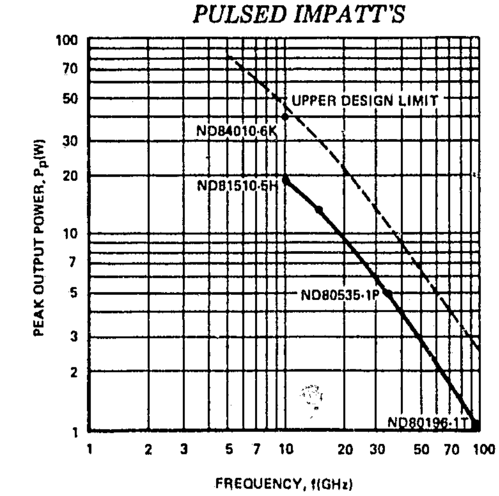
NEC can presently provide pulsed power levels up to 80 watts at 4 GHz and 1.0 watts at 96 GHz. Customer requirements and specifications can be tailor made to the design limits shown below. The ND 8 Si DDR Pulsed IMPATT applications include missile guidance systems, light weight man-pack radar and active phased array radar.

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

SYMBOL	PARAMETERS	UNITS	RATINGS
P_d	Power Dissipation	W	$(250-T_c)/R_{th(j-c)}$
T_j	Junction Temperature	°C	250
T_{stg}	Storage Temperature	°C	-65 ~ +250

DESIGN CAPABILITIES

DESIGN CAPABILITIES FOR THE ND8 Si DDR PULSED IMPATT'S



Nippon Electric Co.,Ltd.

PERFORMANCE SPECIFICATIONS (T_a=25 C, FOR S-BAND APPLICATIONS)

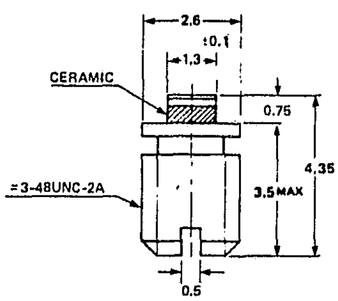
ND PART NUMBER			ND80196			ND80535			ND81015			ND81510			ND84010		
PACKAGE CODE			1T			1P			5H			5H			6K		
SYMBOL	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
V_{BR}	Breakdown Voltage I_R=1mA	V		15			44			75			110			110	
V_F	Forward Voltage I_F=300mA	V		1.15			0.98			0.95			0.94			0.93	
V_{op}	Pulsed Operating Voltage	V		18			55			100			145			150	
I_{op}	Pulsed Operating Current	A		1.4			1.8			1.3			1.4			2.5	
P_P	Peak Output Power at [1]	W															
	f=10 GHz, PW=1 μsec, DC=10%												18			40	
	f=15 GHz, PW=1 μsec, DC=10%									13							
	f=35 GHz, PW=100 nsec, DC=1%						5.0										
	f=96 GHz, PW=100 nsec, DC=1%			1													
η	Efficiency at	%															
	f=10 GHz, PW=1 μsec, DC=10%												9.0			10.5	
	f=15 GHz, PW=1 μsec, DC=10%									10							
	f=35 GHz, PW=100 nsec, DC=1%						5.0										
	f=96 GHz, PW=100 nsec, DC=1%			4.0													
$\Delta T_{j(AVE)}$	Junction Temperature Rise (AVE)[2]	°C								80			120			125	
R_{th} (j-c)	Thermal Resistance	°C/W								5.0			4.5			2.5	
C_j	Junction Capacitance at V_B-1V	pF								1.0			1.1			2.2	

NOTES:

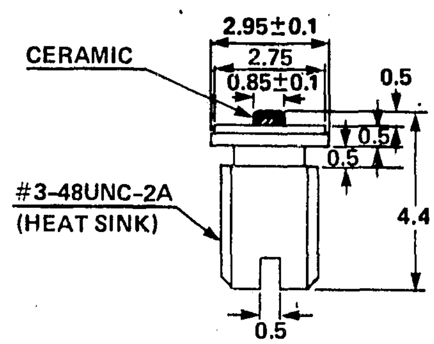
1. $P_p = \frac{P_{AVG}}{DC}$
2. $\Delta T_{j(AVE)} = (V_{op} \cdot I_{op} - P_{OUT})\ (R_{th}(j\text{-}c) + R_{th}(c\text{-}a))\ (DC)$, $R_{th}(c\text{-}a) = 1.5°C/W$

PHYSICAL DIMENSIONS *(Units in mm)*

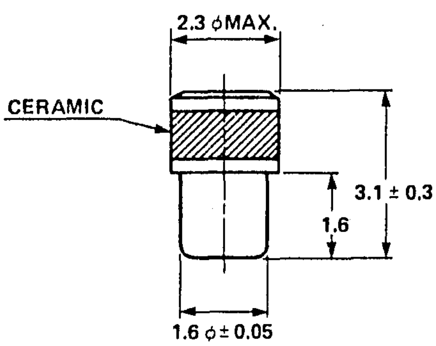
1P PACKAGE



1T PACKAGE

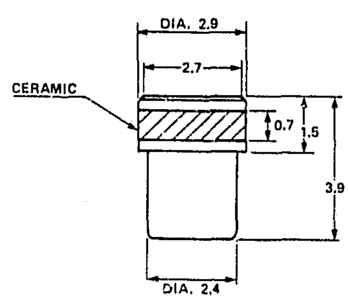


5H PACKAGE



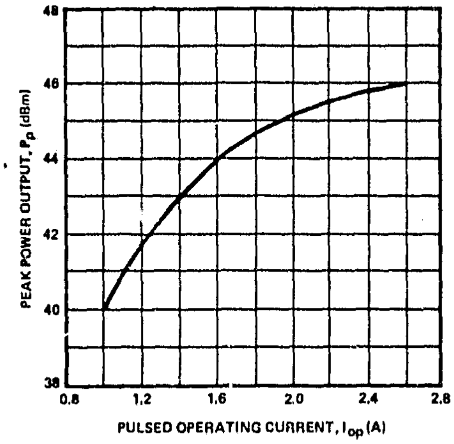
C_c = 0.4 pF

6K PACKAGE

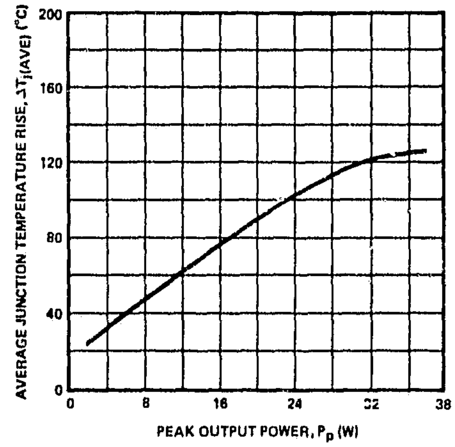


PERFORMANCE CHARACTERISTICS (T_a=25°C)

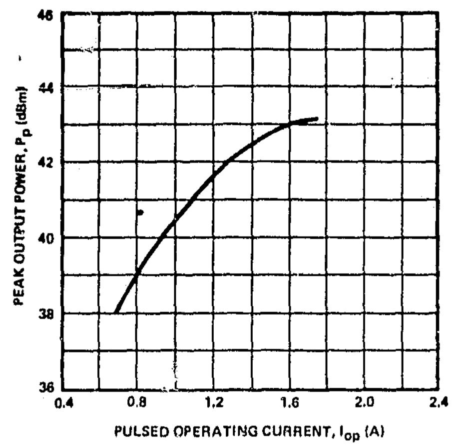
TYPICAL PEAK POWER OUTPUT VS. PULSED OPERATING CURRENT FOR THE ND84010-6K AT 10 GHz



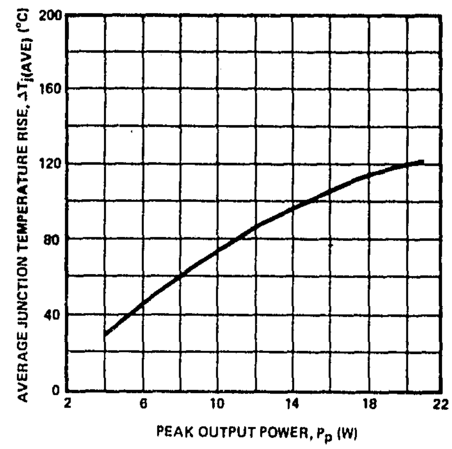
TYPICAL AVERAGE JUNCTION TEMPERATURE RISE VS. PEAK OUTPUT POWER FOR THE ND84010-6K AT 10 GHz



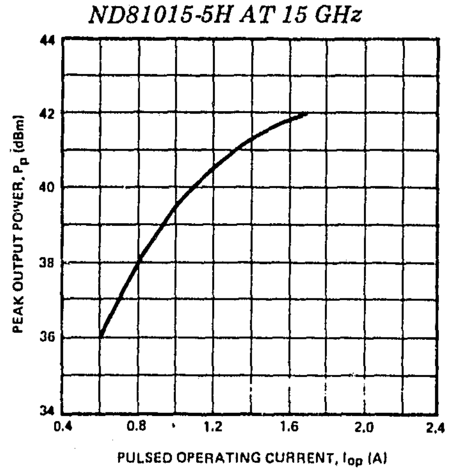
TYPICAL PEAK OUTPUT POWER VS. PULSED OPERATING CURRENT FOR ND81510-5H AT 10 GHz



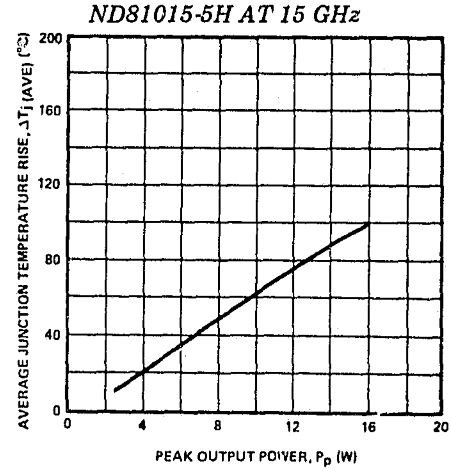
TYPICAL AVERAGE JUNCTION TEMPERATURE RISE VS. PEAK OUTPUT POWER FOR THE ND81510-5H AT 10 GHz



TYPICAL PEAK OUTPUT POWER VS. PULSED OPERATING CURRENT FOR ND81015-5H AT 15 GHz

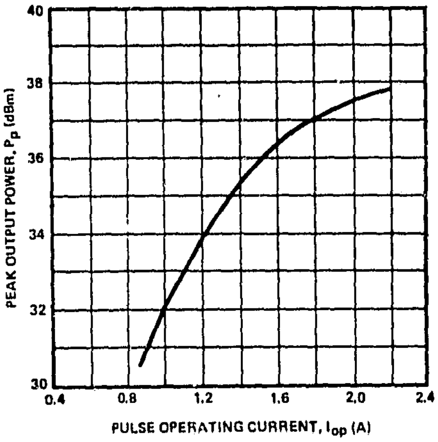


TYPICAL AVERAGE JUNCTION TEMPERATURE RISE VS. PEAK OUTPUT POWER FOR THE ND81015-5H AT 15 GHz



PERFORMANCE CHARACTERISTICS (T_a=25°C)

TYPICAL PEAK OUTPUT VS. PULSED OPERATING CURRENT FOR THE ND805351P AT 35 GHz



TYPICAL PEAK OUTPUT POWER VS. PULSED OPERATING CURRENT FOR THE ND801961T AT 96 GHz