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MSC - 06779

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

INFORMATION SYSTEMS DIVISION INTERNAL NOTE

AN INTRODUCTION TO THE BANNING DESIGN AUTOMATION SYSTEM FOR SHUTTLE MICROELECTRONIC HARDWARE DEVELOPMENT

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MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

APRIL 3, 1972

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AN INTRODUCTION TO THE BANNING DESIGN AUTOMATION SYSTEM FOR SHUTTLE MICROELECTRONIC HARDWARE DEVELOPMENT

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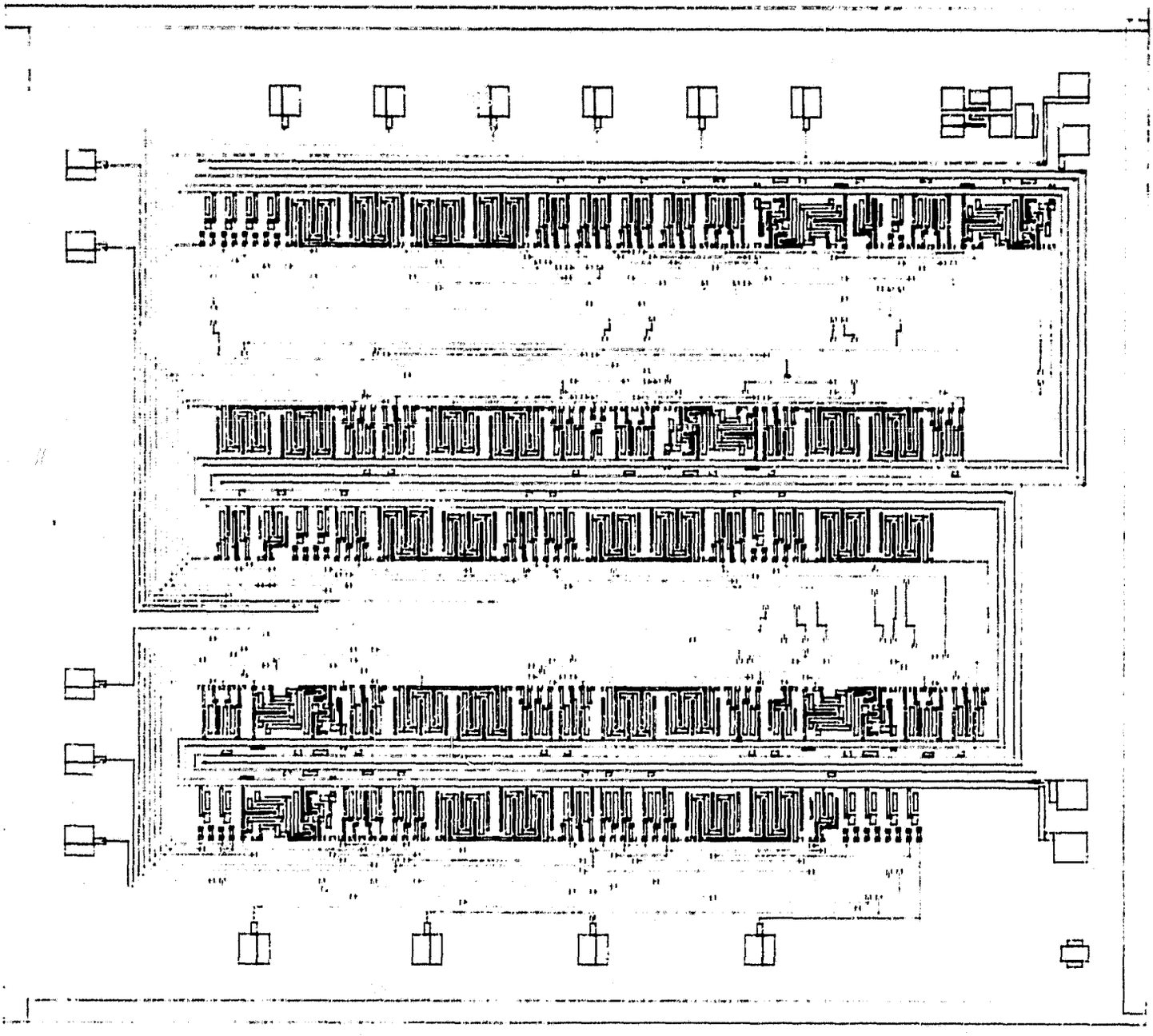

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1.0 ABSTRACT

This paper describes the BANNING MOS (Metal-Oxide-Semiconductor) design system that has recently been implemented at MSC on the Univac 1108 computers in the Computation and Analysis Division. This system has been designed to complement rather than supplant the normal design activities associated with the design and fabrication of low-power digital electronic equipment. BANNING is user-oriented and requires no programming experience to use effectively. It provides the user a simulation capability to aid in his circuit design and it eliminates most of the manual operations involved in the layout and artwork generation of integrated circuits. This report is organized to answer in as few words as possible five of the most commonly asked questions about BANNING. An example of its operation is given and some additional background reading is provided in the Appendices. Appendix A gives a very brief explanation of how an MOS transistor works and Appendix D contains a glossary of the more important terms used in this report.

"He was slowly going mad
Designing circuits pad by pad.
He screamed and woke,
Then thanked the bloke
Whose fertile mind had fathered CAD"

--- Anonymous

2.0 INTRODUCTION

The Banning computer-aided design (CAD) programs were written to prevent nightmares such as this one. This brochure was prepared to familiarize the reader with the Banning design system without presenting a detailed description of its operation. There are several volumes of documentation available which describes Banning at any level of detail desired, but they are user-oriented and are not suitable for someone desiring only a general overview of the subject. The material presented here is intended primarily for potential users of the system, and this includes almost anyone involved in the design and/or fabrication of avionic hardware. The format of this brochure should make it useful to managers and decision-makers as well. If, after reading the material presented here, the reader desires further information about Banning, he is encouraged to consult any member of the Microelectronics Section.

3.0 WHAT IS BANNING?

Banning is a collection of five major computer programs which translate a logic design, such as that shown in Figure 1, into precision photomasks, or artwork, for producing P-channel MOS (Metal-Oxide-Semiconductor) LSI (Large-Scale-Integrated) circuits.[1] These programs are written in Fortran V for the Univac 1108 computer and consist of the following:

- Placement-Routing-Folding (PRF) Program
- Artwork Program
- Signal Trace Program
- Logic Block Simulator (LOGSIM)
- Transient Analysis Program

MOS technology was selected for use with Banning because it is basically a simple process and therefore very economical. The fabrication process requires only four masks compared with five, six or more for competing technologies. MOS artwork preparation is by far the most critical as well as the most time-consuming step in the fabrication of MOS

[1] Appendix D contains a glossary of most of the terms used in this report plus many others commonly used by integrated circuit users.

circuits. It is therefore, a step requiring as much automation as is practical. As will shortly be seen, Banning does an admirable job in attaining this goal.

For those without a clear understanding of what is meant by an MOS mask, Appendix B is offered, which shows a four mask set that overlay, or register, to form one of the simpler Banning cells. By way of comparison, Figure 2 is a checkplot of an MOS circuit which shows how exactly 65 Banning cells similar to this one are interconnected to achieve a desired function. Note that to save plotting time the cells are represented by boxes since the cell structure itself is invariant.

4.0 WHY IS BANNING NEEDED?

Banning permits the logic designer to convert his logic designs into working microminiaturized systems in a minimum of time with the highest possible probability of success. Factors which make this possible and other advantages to the user of Banning are:

- Improved turnaround time

  Final precision artwork is available in several days compared to the month or more required for the manual procedure.

- Elimination of layout design rule violations

  Each cell has already been designed, fabricated, and tested, and has accumulated many device - hours in the field. It is guaranteed to perform according to the specifications on its data sheet (see figure 3). In addition, each cell design has been digitized, check-plotted and stored on tape. Subsequent uses of a given cell are therefore free of human error.

- Improved accuracy

  The manual operations associated with digitizing or rubylith cutting are completely eliminated. Complex manual artwork frequently has errors that escape detection until much time and money have been invested in the design.

- Simulation availability

  Signal Trace and LOGSIM perform in minutes highly accurate time analyses for the designer which would otherwise take him weeks to perform, if indeed that level of simulation could be done at all by hand calculations.

- Low cost

  MOS fabrication is a relatively inexpensive process compared with the fabrication of other semiconductor devices such as NPN or PNP transistors. Device processing time is on the order of a few days under optimum conditions.

5.0 HOW DOES BANNING WORK?

Banning uses a library of 120 different building blocks, or standard cells, that are interconnected to form working systems. An example of one of these cells is shown in Figure 3 which shows the schematic and logic symbols for the cell as well as its truth table and input-output capacities. Table I summarizes the electrical characteristics of the Banning cells. A complete list of the logic cells available to Banning users is given in Appendix C. The engineer designs his logic using the standard cells contained in the library and then codes up a deck of data cards. The logic block simulator (LOGSIM) checks the input cards looking for coding errors and then calculates rise and fall times, delays, node voltages, etc. The designer then analyzes the printed output in order to verify whether or not his logic performs as expected.

If the LOGSIM results agree with his design goals, then data cards are prepared and entered into the PRF program which selects the required standard cells, places them on a coordinate system, and interconnects them according to the designer's input data. After all wiring has been completed, Signal Trace, essentially a subroutine of PRF, then uses the node capacitance loading data calculated by PRF to calculate rise and fall times for each node in the circuit. The results are output on a printer plot which the designer must then study to determine if any of his cells have been overloaded. If a

particular cell has been overloaded he must either reduce the capacitance of that net, insert a cell with more driving capability[2], or else re-design his logic.

The PRF program outputs its data to the Artwork program which then converts the PRF coordinate data into commands to drive an automatic plotting machine. There are two plotting machines available and in use at present - a Gerber Series 1000 equipped with a photohead and a D. W. Mann Pattern Generator. The Artwork program also performs various utility functions such as adding cells to the library or deleting them. An example of a typical circuit which has been plotted is shown on the cover of this document. The plot shown is the metal mask (level 4). Note that the structure of each cell is visible, whereas in Figure 2 only the outlines are shown.

The Transient Analysis Program is used primarily for standard cell design to evaluate their response times. Although this program is not yet available at MSC, a much better program is available for performing this same function. SCEPTRE (System for Circuit Evaluation and Prediction of Transient Radiation Effects) was written to analyze radiation effects

2 The standard cell library has both 2 picofarad and 4 picofarad cells plus output drivers with various driving capabilities.

on electronics and contains an excellent transient analysis routine. SCEPTRE is now available on the Univac 1108. Figure 4 is a flowchart that shows the relationships between the various programs.

6.0 WHO CAN USE BANNING?

Anyone who does logic design and testing. A complete set of user manuals is available which describes the step-by-step procedure for turning a logic design into a working set of photomasks. No programming experience is necessary to use Banning. In addition, the Microelectronics Laboratory is now set up to process the Banning output and can have sample quantities of chips ready for testing within a few weeks of final artwork submittal.

7.0 WHERE DID MSC GET THE BANNING PROGRAMS?

The basic Banning programs were given to NASA by another Government agency which prefers to remain anonymous. Due to the fact that these programs originally were running on a GE 625 computer, initial efforts to run them on the the Univac 1108 met with limited success. These early problems have been overcome and the basic programs have been updated and considerably expanded to meet MSC's own particular requirements.

TABLE I

ELECTRICAL CHARACTERISTICS OF THE
BANNING CELLS

PARAMETER	SYMBOL	MINIMUM	MAXIMUM
Power Supply	V_{DD}	-13.3	-15.5
Clock Voltage	V_{GG}	-23.8	-27.4
Threshold Voltage	V_T	-3.5	-4.5
Case Temperature	T_{AMB}	-55°C	+125°C
Clock Frequency	--	--	860 kHz
Clock Pulse Width	--	510 nsec	--
Logic "1"	V_1	-9.0	-15.3
Logic "0"	V_0	+0.3	-3.5

8.0 CONCLUSIONS

This report has briefly summarized the salient characteristics of the BANNING MOS design system and has attempted to show the interrelationships between the various programs. No attempt has been made to give input and output formats since they are highly dependent on options selected by the user and would only require further explanation. It is hoped that the reader will inquire about further documentation on all or part of the BANNING system and also about plans for further development.

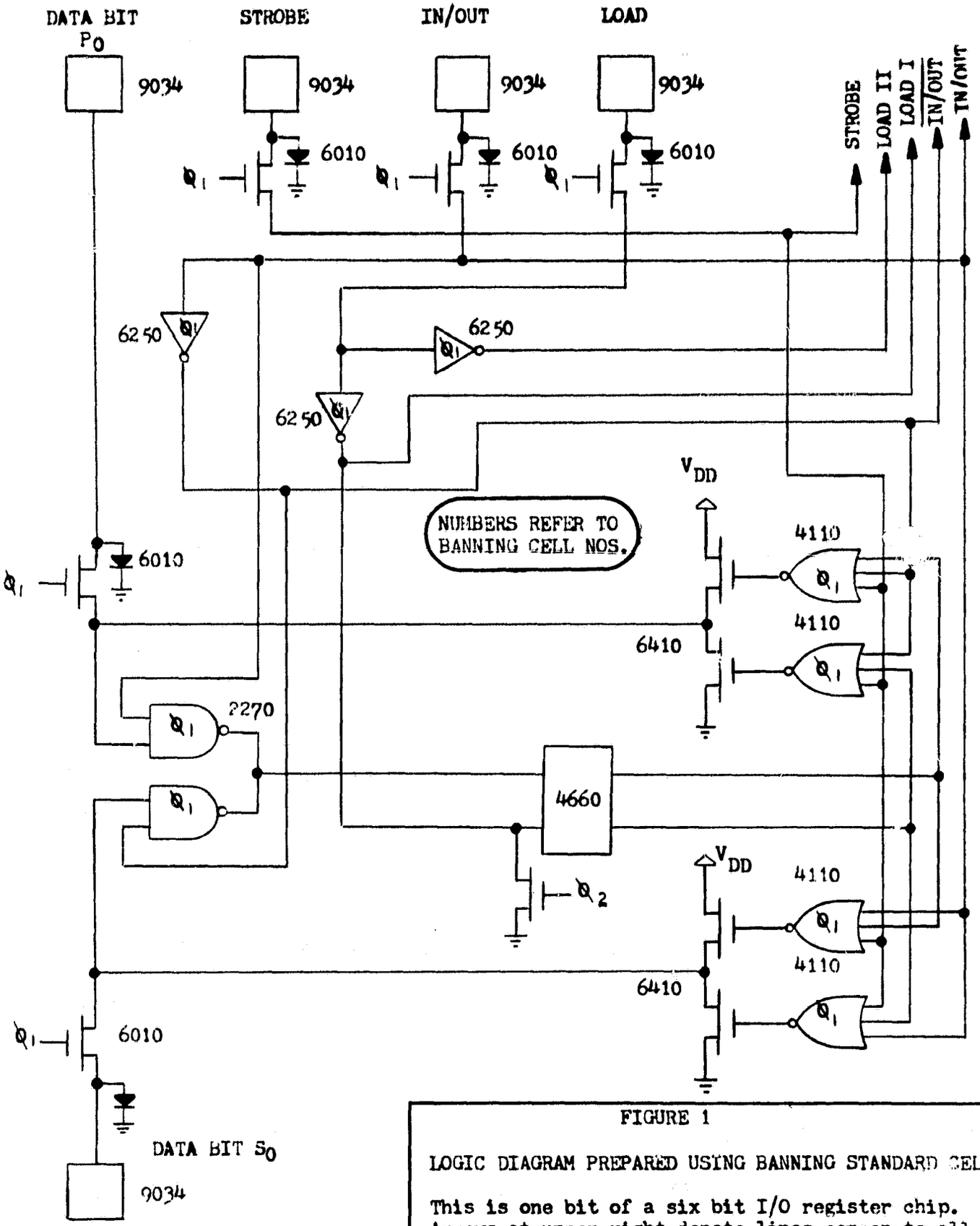

FIGURE 1

LOGIC DIAGRAM PREPARED USING BANNING STANDARD CELLS

This is one bit of a six bit I/O register chip. Arrows at upper right denote lines common to all six bits. See Figure 2 for a complete plot of this chip as produced by Banning.

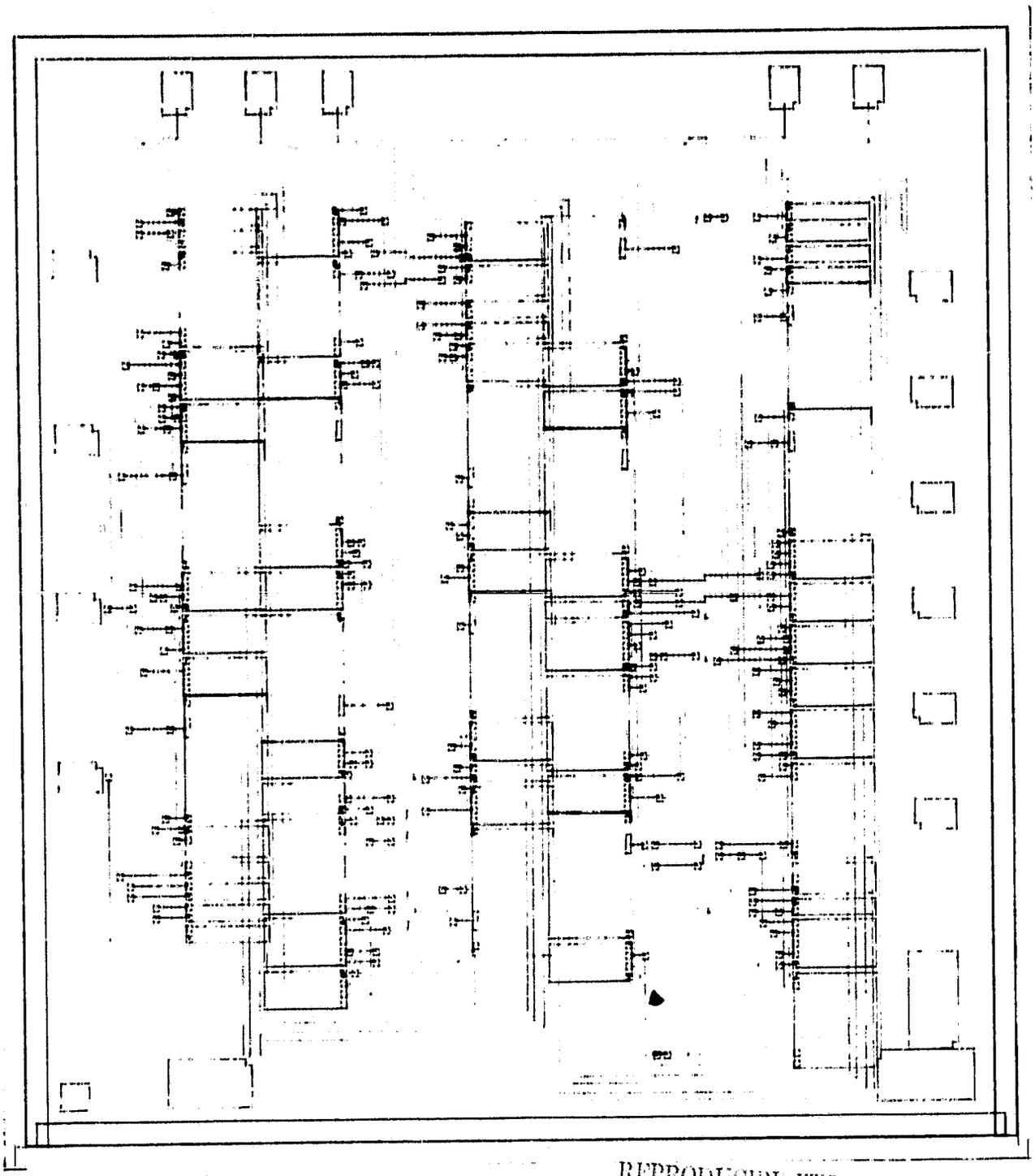

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FIGURE 2

BOX PLOT OF I/O REGISTER CHIP
DRAWN AT A SCALE OF 50:1 BY A GERBER 600 PLOTTER

BANNING THICK OXIDE STANDARD CELL

STATIC REGISTER, 4pF
"1" OUTPUT

PATTERN NO. 4600 (ϕ_1 ϕ_2)

FIGURE 3A

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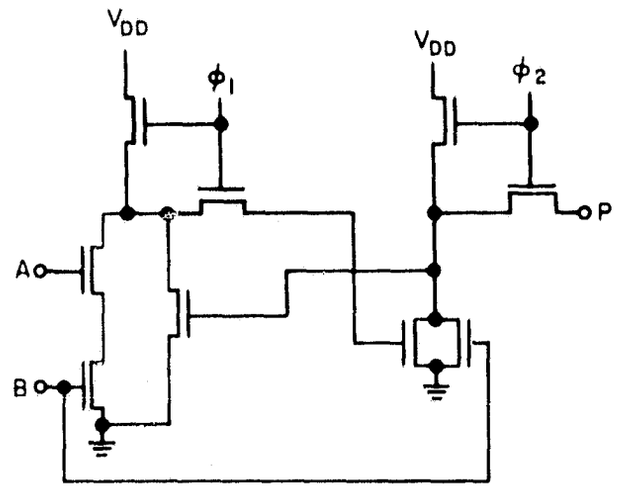
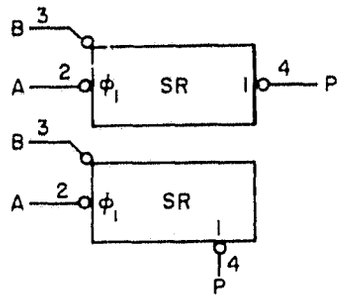
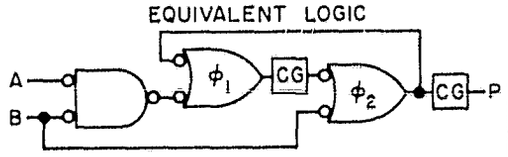
SCHEMATIC



LOGIC SYMBOL



EQUIVALENT LOGIC



TRUTH TABLE

A_{t-1}	B_{t-1}	ϕ_1	B	ϕ_2	P
*	*	*	*	0	P_{t-1}
*	0	0	0	1	P_{t-1}
0	1	0	0	1	0
1	1	0	0	1	1

*MEANS EITHER STATE

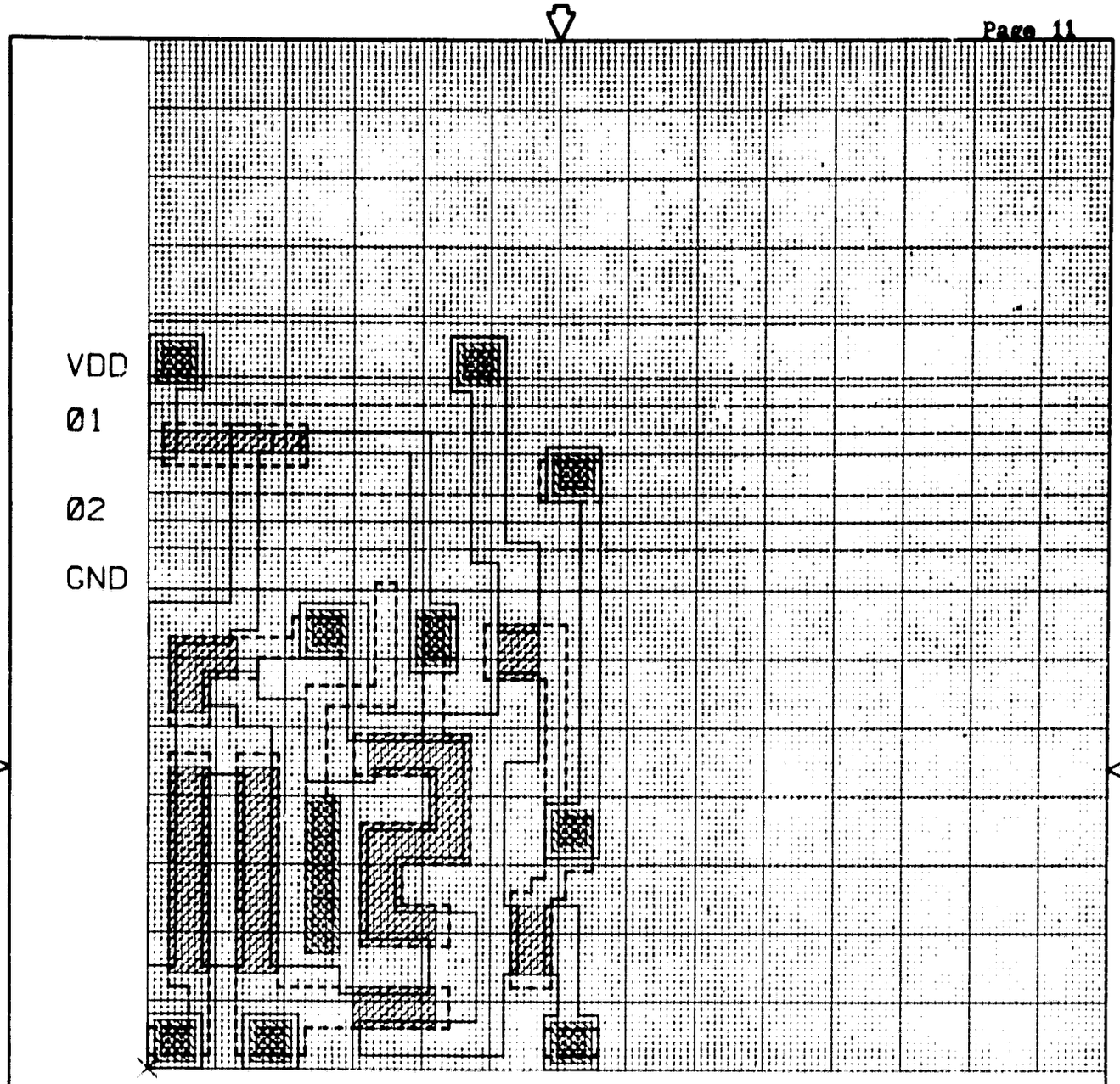
B IS THE SAMPLE INPUT
DURING ϕ_2 B MUST EQUAL ZERO

LOGIC EQUATIONS

$$P = P_{t-1} \cdot \overline{\phi}_2 + \phi_2 \cdot \overline{B} \left[A_{t-1} B_{t-1} + \overline{B_{t-1}} P_{t-1} \right]$$

CELL I/O CAPACITIES

CAPACITOR	PIN	CAPACITY IN fF
C_A	2	420
C_B	3	580
C_P	4	600
PATTERN NO.		4600



4600

FIGURE 3B

SIZE	CODE IDENT.NO.	DWG.NO.
A	98230	STATIC REGISTER Q OUTPUT
SCALE 0.1 mil/div		SHEET

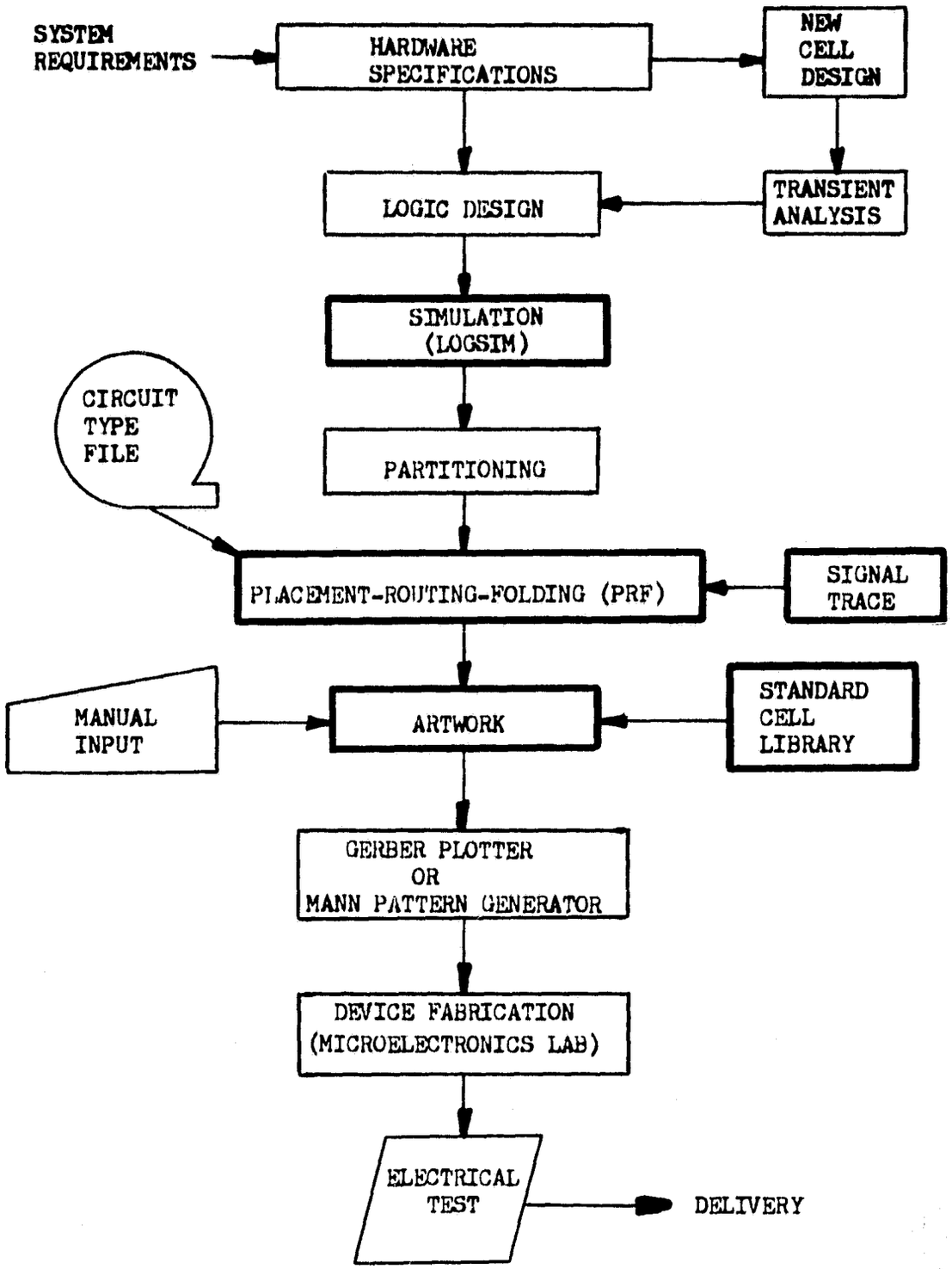
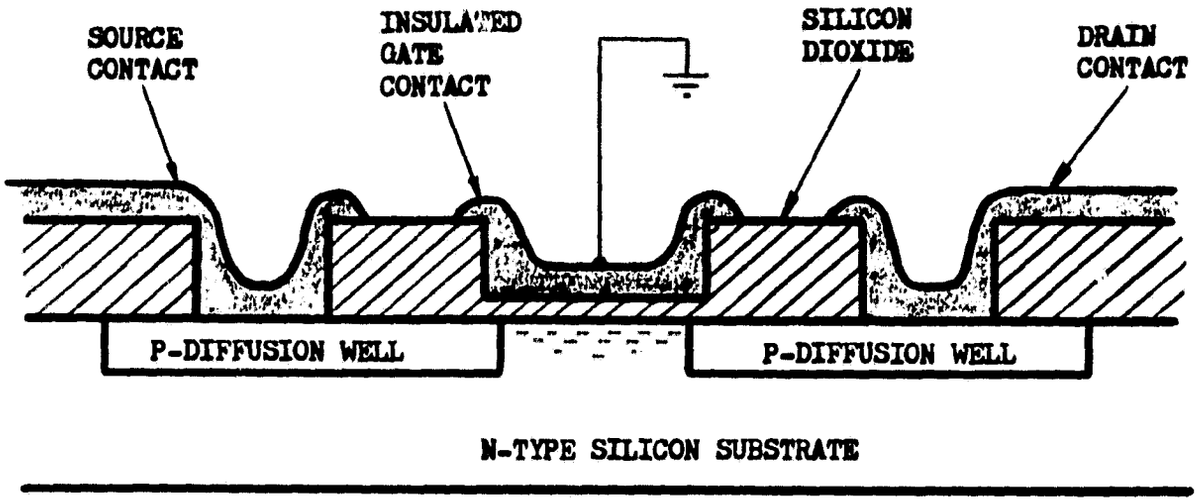


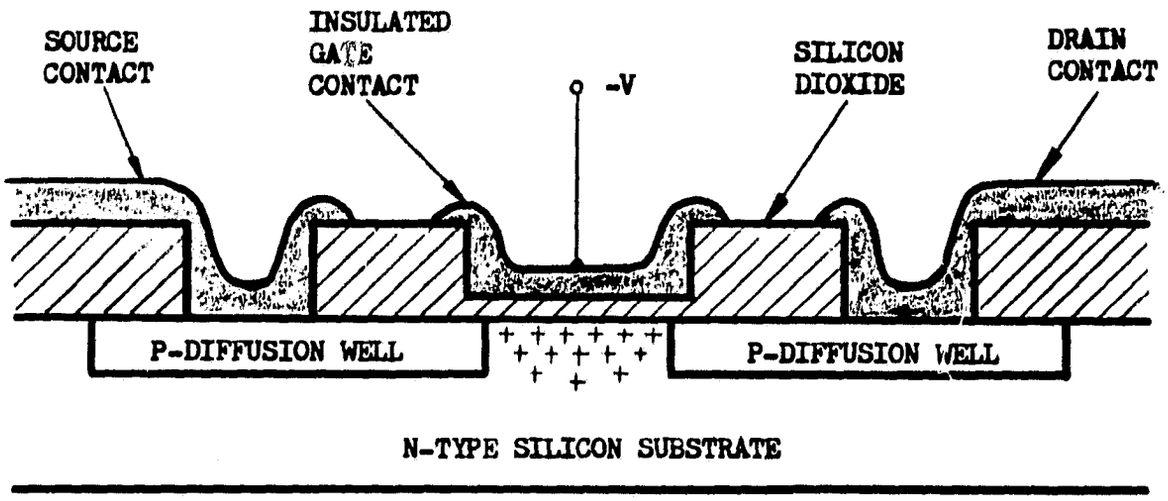
FIGURE 4

GENERAL FLOWCHART FOR HARDWARE FABRICATION USING THE BANNING DESIGN PROGRAMS (SHOWN WITH HEAVY OUTLINES)



(b)

High resistance from source to drain



(a)

Low resistance from source to drain

FIGURE 5

SIMPLIFIED DIAGRAM OF AN MOS INSULATED-GATE

FIELD-EFFECT TRANSISTOR

9.0 APPENDICES

APPENDIX A
WHAT IS MOS?

MOS is the abbreviation for a metal-oxide-semiconductor sandwich which functions much like an ordinary transistor, with the exception that an MOS transistor has a much higher input impedance and can be built much smaller and at a lower cost. A glance at Figure 5 will reveal the reason for the high input impedance. The input signal is applied to the electrode labelled "gate" which is insulated from the semiconductor surface by the non-conducting silicon dioxide. The term "insulated gate field effect transistor" is sometimes used to describe this structure.

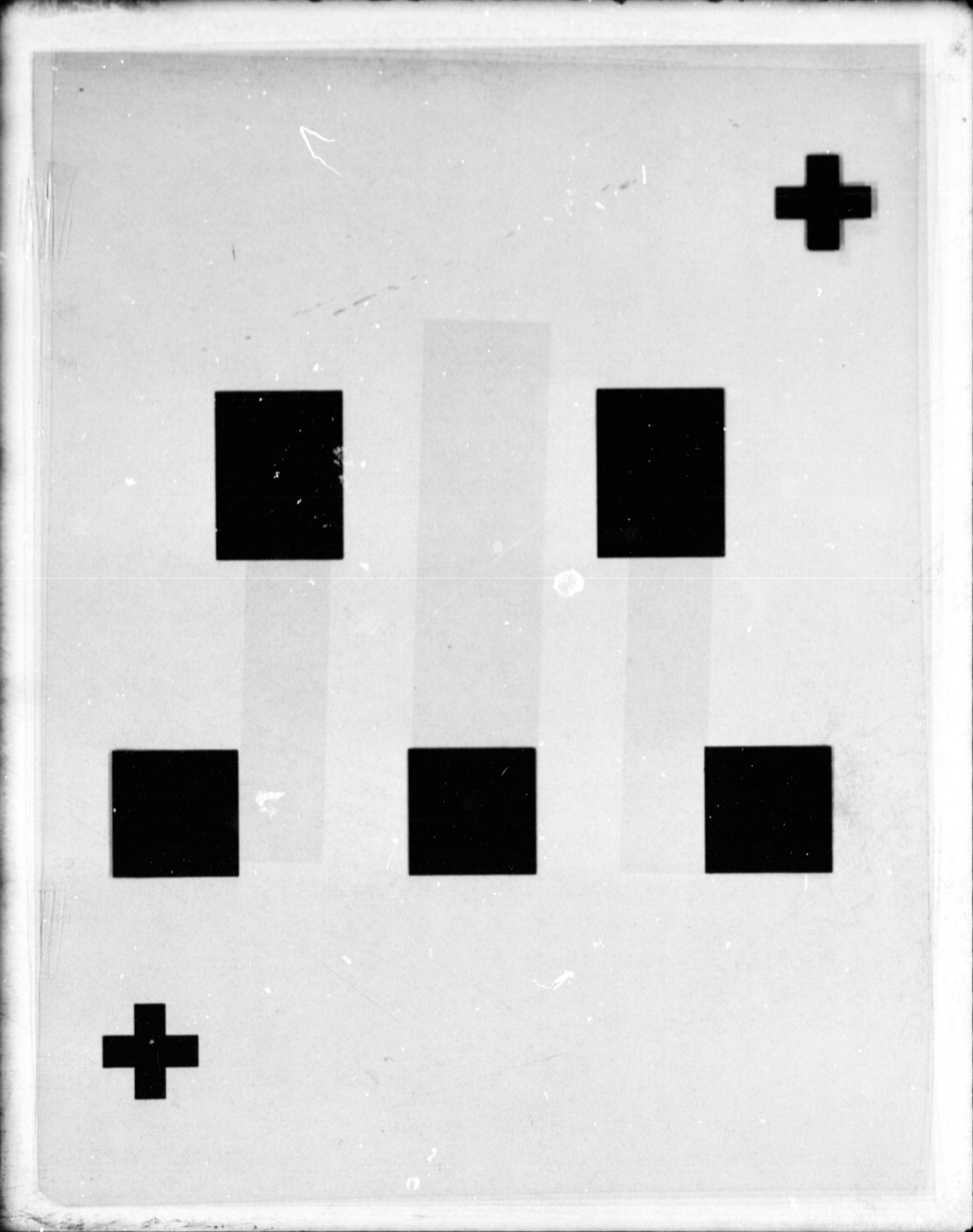
The "gate" electrode of the device is appropriately named because it controls the flow of current from the region labelled "source" to the region labelled "drain". The source, obviously, is connected to a source of positive charge such as the plus terminal of a power supply or battery. When current flows from the source it is "collected" by the drain region. Note that the source-body and the drain-body P-N diodes are normally back-biased and hence do not pass current. This is insured merely by connecting the body to the most positive potential in the circuit.

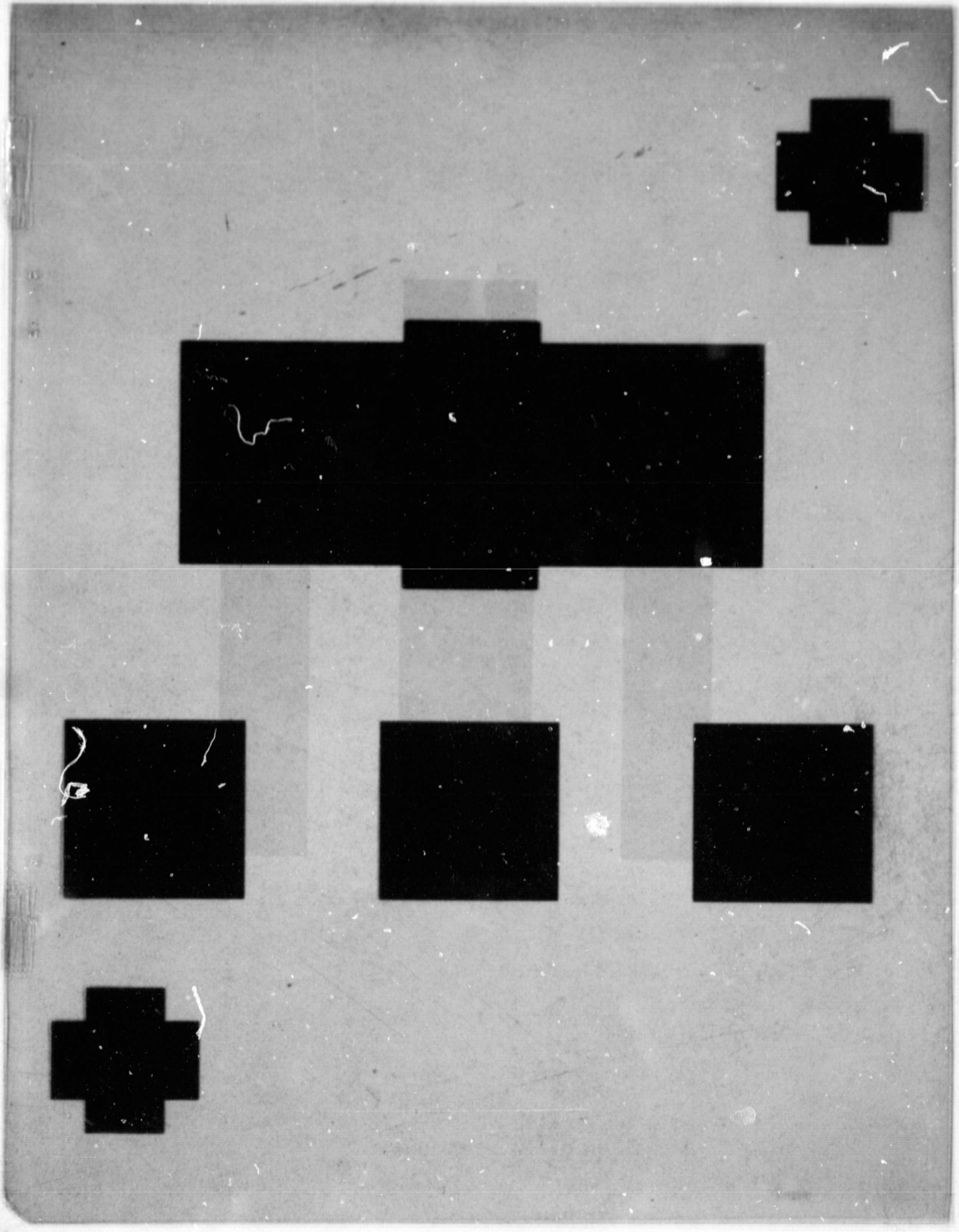
The reader may have surmised already that the gate is analogous to the base of an ordinary transistor, the source to the emitter, and the drain to the collector. It is here

that the analogy ends since the flow of current from source to drain is controlled by the electric field at the surface of the silicon and and not by the injection of electrons or holes into the silicon. This leads to the secret of operation of an MOS transistor, and that is the manner in which the gate electrode controls the flow of current from source to drain. As indicated above, the flow is controlled or modulated by an electric field established between the gate and the semiconductor. By definition, a semiconductor such as silicon can be easily switched from a conducting to a non-conducting state by the application of an electric field. For example, with no voltage applied to the gate no current can flow, since the intervening silicon is N-type, or contains an excess of electrons. Now if a negative voltage is applied to the gate, the electrons in the silicon are repelled and a thin region of silicon at the surface is converted to P-type, thus "shorting" out the source and drain. The resistance of this path is determined by the magnitude of voltage on the gate and hence the ability of the gate voltage to modulate the current flow.

APPENDIX B

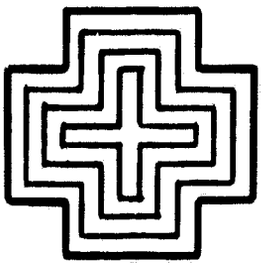
EXAMPLE OF MOS ARTWORK SHOWING OVERLAY SCHEME

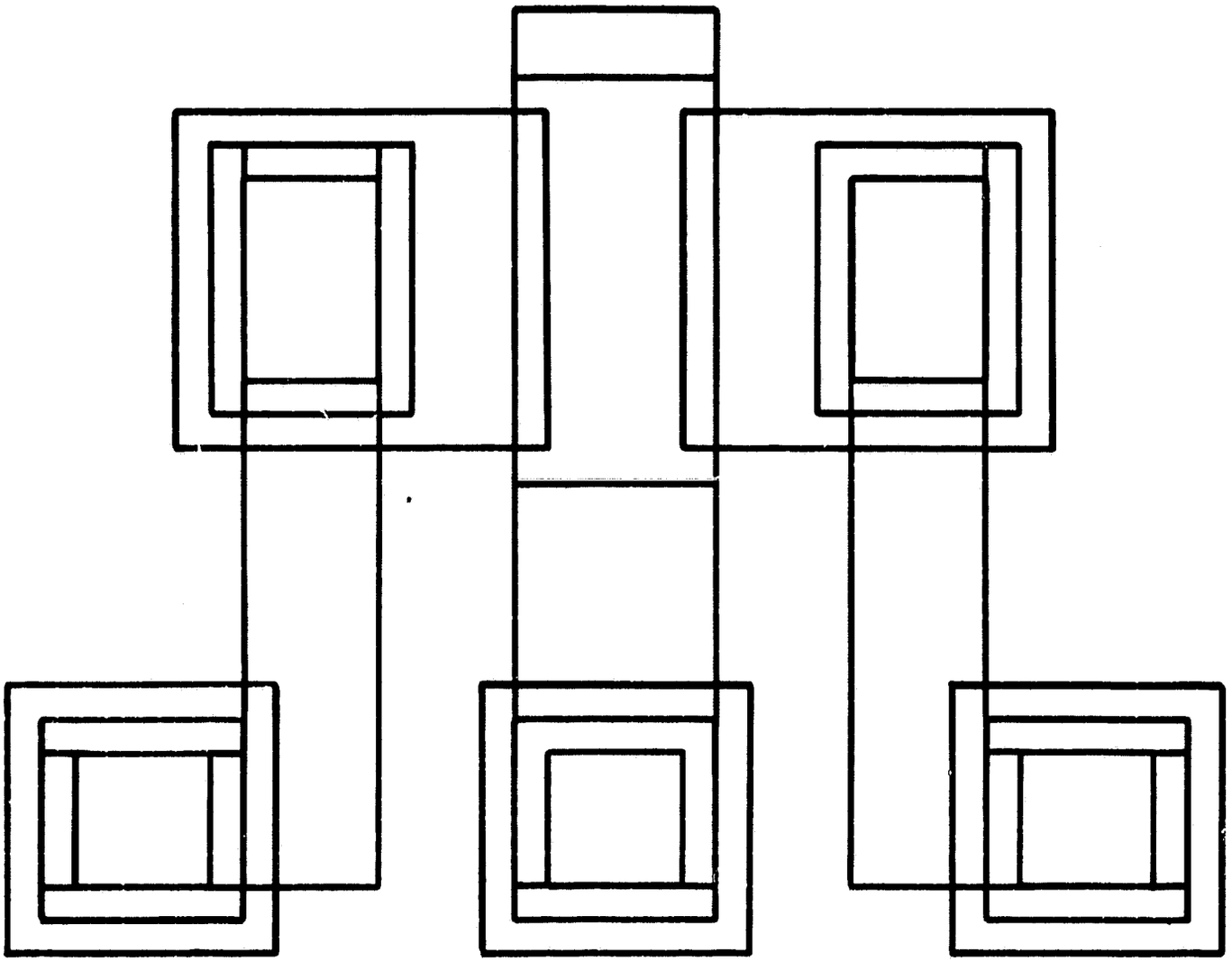




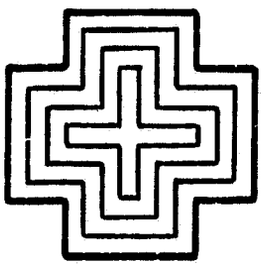
BANNING CELL NO. 6270

ϕ_n CLOCK GATE





SOURCE GATE DRAIN



ALIGNMENT MARK (2 EACH)

MASK NO. 1 - SOURCE AND DRAIN (RED)

MASK NO. 2 - GATE AND PRE-CONTACTS (BLUE)

MASK NO. 3 - LARGE CONTACTS (GREEN)

MASK NO. 4 - ALUMINUM (YELLOW)

APPENDIX C

LIST OF BANNING STANDARD CELLS

Cell Number	Cell Name
2070-2080	2-Input NOR, 2pF
2090-2100	2-Input NOR, with delay, 2 pF
2110-2120	3-Input NOR, 2 pF
2130-2140	3-Input NOR, with delay, 2pF
2150-2160	4-Input NOR, 2pF
2190-2200	2-Input NAND, 2pF
2210-2220	2-Input NAND with delay, 2pF
2230-2240	3-Input AND NOR, 2pF
2250-2260	3-Input AND NOR with delay, 2pF
2270-2280	4-Input NAND OR, 2pF
2290-2300	4-Input AND NOR, 2pF
2310-2320	4-Input AND NOR with delay, 2pF
2330-2340	3-Input OR NAND, 2pF
2350-2360	3-Input Switch, 2pF (optional EXCLUSIVE OR)
2370-2380	Dynamic Shift Register, 2pF, with 1/2 bit and 1 bit delay outputs
2390-2400	Dynamic Shift Register, 2pF, 1 bit delay output, with set
2410-2420	Dynamic Shift Register, 2pF, 1 bit delay output, with reset
2440	Static Register, 2pF, "1" output with set
2460	Static Register, 2pF, "0" and "1" outputs
2480	Static Register, 2pF, "0" and "1" outputs
2500	Static Register, 2pF, "0" and "1" outputs set and kill
2520	Dual Sample Register, 2pF, "0" and "1" outputs
2560-2570	Schmitt Trigger
2580	Dynamic Shift Register, 2pF, 1 bit delay output, with reset
2600	Static Register, 2pF, "1" output
2620	Static Register, 2pF, "1" output with reset
2640	Static Register, 2pF, "0" and "1" outputs with set

Cell Number	Cell Name
2660	Static Register, 2pF, "0" and "1" outputs with kill
2680	Static Register, 2pF, "0" and "1" outputs, reset and kill
2700	Binary, 2pF, "0", carry and carry not outputs
2720	Dual Sample Register, 2 pf, "1" output
4010-4020	Inverter, 4pF
4050-4060	Inverter with delay, 4pF
4070-4080	2-Input NOR, 4pF
4090-4100	2-Input NOR with delay, 4pF
4110-4120	3-Input NOR, 4pF
4130-4140	3-Input NOR with delay, 4pF
4150-4160	4-Input NOR, 4pF
4170-4180	4-Input NOR with delay, 4pF
4190-4200	2-Input NAND, 4pF
4210-4220	2-Input NAND with delay, 4pF
4230-4240	3-Input AND NOR, 4pF
4250-4260	3-Input AND NOR with delay, 4pF
4350-4360	3-Input Switch, 4pF (optional EXCLUSIVE OR)
4370-4380	Dynamic Shift Register, 4pF, with 1/2 bit and 1 bit delay outputs
4390-4400	Dynamic Shift Register, 4pF, 1 bit delay output, with set
4410-4420	Dynamic Shift Register, 4pF, 1 bit delay output, with reset
4430	Static Register, 4pF, "1" output w/reset, w/o int. C. G.
4440	Static Register, 4pF, "1" output with set
4450	Static Register, 4pF, "0" and "1" outputs w/reset,w/o int. C.G.
4460	Static Register, 4pF, "0" and "1" outputs
4480	Static Register, 4pF, "0" and "1" outputs with reset
4500	Static Register, 4pF, "0" and "1" outputs, set and kill
4520	Dual Sample Register, 4pF, "0" and and "1" outputs

Cell Number	Cell Name
4530-4540	RS Flip-Flop, no delay, 4pF "0" and "1" outputs
4580	Dynamic Shift Register, 4pF, 1 bit delay output, with reset
4600	Static Register, 4pF, "1" output
4620	Static Register, 4pF, "1" output with reset
4640	Static Register, 4pF, "0" and "1" outputs with set
4660	Static Register, 4pF, "0" and "1" outputs with kill
4680	Static Register, 4pF, "0" and "1" outputs, reset and kill
5020	Protective Diode
5030-5040	Two Input NOR, 9pF
5090	Killer, ϕ, controlled
6000-6010	Protected Clock Gate
6020-6030	Clock Gate
6040	Killer, ϕ_2 controlled
6050	Killer, signal controlled
6060	DC Buffer, 25 pF
6070-6080	Precharge Buffer, 53pF
6090-6100	Precharge Buffer, 78pF
6110-6120	Precharge Buffer, 103pF
6140	Static Register String Start
6160	Static Register String Middle
6180	Static Register String End
6200	Dynamic Register String Start
6220	Dynamic Register String Middle
6240	Dynamic Register String End
6250-6260	Inverter, 10pF
6270	ϕ_n Clock Gate
6280	ϕ_n Protected Clock Gate
6290-6300	Precharge Buffer, 30pF

Cell Number	Cell Name
6400	Output Driver, 30 pf
6410	Push-Pull Driver, 30 pf
7020	Tunnel end
7030	Tunnel end
7510	On-chip alignment mark
8040	Thick-oxide test transistor
8070	$\Phi 1$, V_{DD} pad pattern
8080	$\Phi 2$, GND pad pattern
9034	Pad
9620	Off-Chip alignment mark

APPENDIX D

GLOSSARY OF TERMS

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ACCEPTOR - See DOPANT.

ARTWORK - A precise geometrical representation of a PC board, integrated or hybrid circuit, or any other assembly to be constructed which requires a precise layout. The layout is usually made on cut-and-strip rubylith, photographic film, or by applying tape to a transparent background. Artwork is usually done at 10-100 times final size and then photographically reduced.

BALL BOND - A micro-connection to a micro-miniaturized circuit. The bond gets its name from the gold ball which is formed by surface tension when a fine gold wire (0.001 inch) is flame-cut. The gold ball is then bonded to an aluminum pad on the microcircuit with the application of heat and pressure. This bond is for the purpose of connecting the chip to the package and then to the outside world.

BONDING PAD - A metallized area on the surface of a microcircuit chip (or die) to which a bond will be made. This pad is usually formed of aluminum and is usually about 5 mils on a side. See PROBE PADS.

BIPOLAR TRANSISTOR - The common NPN or PNP transistor whose action depends upon majority carrier (be it holes or electrons) flow that is modulated by the injection of minority carriers into the base region of the transistor.

CHANNEL - See either P-CHANNEL or N-CHANNEL.

CHIP - Also called a die. It refers to a single microcircuit function, such as a gate or flip flop, on a piece of silicon typically 100 miles on a side and about 12 mils thick. A silicon wafer about 1-2 inches in diameter usually contains hundreds of these chips which are then separated from each other by scribing the wafer and then breaking it.

DIE - See CHIP.

DIFFUSION - A process for injecting dopant atoms into the silicon crystal lattice to achieve the required impurity level. Dopant atoms close to the silicon surface will, at elevated temperatures on the order of 1000°C, migrate into the silicon because of the concentration gradient. An analogous situation is the dispersion of a drop of colored dye in a glass of water.

DONOR - See DOPANT.

DOPANT - A substance such as boron, arsenic on phosphorus which is placed in the silicon lattice in controlled amounts to achieve the required conductivity. The two types of dopants are donors, which "donate" an electron to the crystal, and acceptors which "accept" an electron when introduced into the silicon crystal. Diffusion and epitaxy are the most common methods for "doping" the silicon.

DRAIN - A highly doped diffused region in a MOS transistor in which the flow of majority carriers terminate. The drain is analogous to the collector of a conventional, or bipolar, transistor or the plate of a vacuum tube.

EPITAXY - The growing of one material on another. In the stricter sense, the growing of single crystal material on a single crystal substrate, the crystal orientation of the new material depending on the orientation of the host material (also called the substrate). Normally the crystal is doped while it is growing to permit the growth of N-type material on a P-type substrate, or vice-versa.

FIELD EFFECT - See MOS.

FORTRAN - A user-oriented programming language which is an acronym for FORmula TRANslation. Fortran statements are translated by the system compiler into a more basic language that the machine can understand. Machine language, though more efficient, is harder to learn and use than is Fortran.

GATE - The region of a MOS transistor that lies between the source and drain and controls the majority current flow. The gate is analogous to the base of a conventional, or bipolar, transistor or to the control grid of a vacuum tube.

HOLE - A position in the crystal lattice which can be filled by an electron, thus influencing current flow. Acceptors such as boron accept an electron when introduced into the lattice because their valence is +3 while that of silicon is +4. At room temperature most of the boron atoms are negatively ionized and a hole exists wherever the electron came from.

INTEGRATED CIRCUIT - An electronic device containing several active and/or passive elements which perform all or part of some function. An example is a silicon chip containing several transistors and diffused resistors which are interconnected to form a TTL gate.

LSI - The abbreviation for Large-Scale-Integration, which refers to a recent technology development which allows many different gating functions to be placed on a single chip. Any chip containing 100 or more equivalent gates is generally referred to as LSI. An "equivalent gate" contains about three or four transistors and an equivalent number of resistors. Resistors are rarely found in LSI circuits, their function being performed by properly biased transistors. See MSI.

METALLIZATION - A conductive coating which serves to interconnect components, for example, on a hybrid substrate or on an integrated circuit wafer. On integrated circuits the metallization is usually aluminum which has been evaporated over the entire wafer (in a vacuum by heating) and then selectively etched.

MICROCIRCUIT - An ultra-small functional electronic circuit or assembly which contains many resistors and transistors in a package usually no larger than a single transistor can. These packages are commonly known as flat packs, TO-cans, dual-inline packages, etc. The technology which made microcircuits possible is generally referred to as microelectronics.

MICROELECTRONICS - That branch of the electronics art which has to do with the development of microminiature electronic components, circuits and systems.

MIL - A unit of measurement commonly used in microelectronic parlance and is equal to one-thousandths (0.001) of an inch.

MOS - An acronym for metal-oxide-semiconductor. An MOS transistor operates on the field effect principle and has an insulated gate, a source, and drain as electrodes. The gate is insulated from the source and drain by a thin oxide layer which gives it a very high input impedance. Another type of field effect transistor is the junction field-effect (JFET) in which the drain-to-source conduction is controlled by a P-N junction located between the source and drain. The voltage applied to the P-N junction varies the width of its depletion region which, in turn, controls the source-to-drain conduction.

MSI - The abbreviation for Medium-Scale-Integration. It refers to integrated circuit chips which contain approximately 50-100 equivalent gates. Die with less than 50 gates are referred to as SSI (Small-Scale-Integration). See LSI .

N-CHANNEL - A thin conductive path on the silicon surface in which conduction occurs primarily by majority-type free electrons. In other words, the region near the surface is normally P-type silicon but has been "inverted" due to either positive charges in the oxide or to an applied positive potential. See P-CHANNEL.

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N-TYPE - Refers to silicon that has been doped with a donor, such as phosphorus, which adds a free election to the lattice structure, thus altering its conductivity. See P-TYPE.

P-CHANNEL - A thin conductive path on the silicon surface in which conduction occurs primarily by majority-type free holes. In other words, the region near the surface is normally N-type silicon but has been "inverted" due to either negative charge in the oxide or to an applied negative potential. See N-CHANNEL.

PHOTOMASK - A photographically produced device used to "shadow", or shield, either a substrate during a vacuum deposition process, on a wafer coated with photosensitive resist.

PICOFARAD - A unit of capacitance equal to 10^{-12} farads (1 farad = 1 coulomb/volt).

PROBE PADS - Special metal contacts on an integrated circuit designed for electrical probing rather than for bonding. A probe is a fine steel rod that tapers to a point with a tip about one mil in diameter. It is attached to micropositioners for very fine control.

P-TYPE - Refers to silicon that has been doped with an acceptor, such as boron, which ties up an electron thereby creating an extra hole in the crystal. The conductivity is altered to an extent dependent on the boron concentration. (See N-TYPE).

RESIST - Also known as photoresist. A photosensitive liquid that has the ability to "resist" the attach of most etchants used in semiconductor processing. A few drops of the resist are applied to the oxidized wager using an eye dropper and the excess removed by spinning the wafer at high speed. Only a thin film of resist remains which is then dried and cured. The entire wafer is exposed to light through a photomask and the areas that are exposed harden. The areas that are not exposed rinse away, thus exposing a hole or via to the material beneath. After etching, the remaining resist is stripped away leaving the desired oxide pattern.

SCRIBING - The process of scoring the silicon in special lanes dividing the active areas. The lanes are called scribe lanes and the scribing is usually done with a very hard substance such as a diamond point.

SILICON - An element classed as a semiconductor since its conductivity can be changed over several orders of magnitude by introducing controlled impurities with concentrations no greater than a few parts per million.

SILICON DIOXIDE - A compound formed by the oxidation of silicon whose chemical formula is SiO_2. The oxidation takes place very slowly at room temperature but can be accelerated by heating the silicon to high temperatures (800 - 1200°C) in the presence of steam or oxygen. Silicon dioxide acts as a barrier to the passage of dopants such as boron or phosphorous and thus can be used to selectively create N or P regions in the silicon.

SUBSTRATE - A material upon which epitaxial layers, thick film depositions, or thin film depositions are made, or within which diffusions are made. The substrate gives mechanical rigidity to the structure and aids in conducting heat away from the active regions.

THRESHOLD VOLTAGE - The voltage which must be applied to the gate of an MOS transistor to initiate conduction between the source and drain.

WAFER - A substrate that is thin with surface areas that are parallel. An example is a silicon slice about 2 inches in diameter and 12 mils thick.

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