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SPACELAB INTERFACE DEVELOPMENT TESTS
SOFTWARE DESCRIPTION

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SOFTWARE DESCRIPTION

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16. Abstract

This document describes the software requirements for the Spacelab Interface Development Tests. The software operates in two modes. The multiplexer-demultiplexer (MDM) mode transmits operator-controlled information to the Spacelab. The Pulse Coded Modulation (PCM) mode records and displays operator-selected PCM data for visual analysis.

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ACRONYMS

ACK	acknowledge
BCE	bus control element
BITE	built-in test equipment
BSRR	BITE status register request
CHW	command header word
CRT	cathode ray tube
FDW	fill data word
GMT	Greenwich mean time
LSB	least significant bit
MDM	multiplexer-demultiplexer
MIA	multipler interface adapter
MSB	most significant bit
PC	program control
PCM	pulse coded modulation
RDW	response data word
SIO	serial input/output
VDW	valid data word

1. INTRODUCTION

This document describes the software requirements for the Spacelab Interface Development Tests. The software operates in two modes. The multiplexer-demultiplexer (MDM) mode transmits operator controlled data to the Spacelab. The reply can be displayed on a cathode ray tube (CRT) for immediate visual analysis or can be printed on a matrix printer for later analysis. The pulse coded modulation (PCM) mode also records and displays operator selected PCM data via a CRT and a matrix printer. The operator interfaces and the data displays are described in this document.

The software was designed to give the user maximum control over the Spacelab Interface Development Tests. It was designed for ease of use and requires changes only to those parameters that are different from one test to the next. The correction of operator input errors is also a simple matter. Thus only a minimum of operator training is necessary.

2. USER INTERFACE GENERAL DESCRIPTION

Upon operator entry, the computer responds with a CRT display:

MODE MDM(M) PCM(P)

The appropriate response is:

M for multiplexer-demultiplexer (MDM) or
P for pulse coded modulation (PCM)

After the mode is defined, an exclamation (!) is displayed requesting parameters to define the command.

The operator responds with a one character instruction and in most cases a set of parameters. The formats of the instructions are as follows. Operator input is underlined.

!Z	PARAMETER 1 . . . . . i_1 $\underline{I_1}$
	PARAMETER 2 . . . . . i_2 $\underline{I_2}$
	⋮
	PARAMETER m . . . . . i_m $\underline{I_m}$
	PARAMETER n . . . . . i_n $\underline{I_n}$

The character Z is the command. The character string PARAMETER m is an alphanumeric description of the m*th* parameter; i_m and I_m are the current value and operator input for the m*th* parameter respectively. The input is terminated by a line feed (LF), up arrow (^), or carriage return (CR). The line feed causes the descriptor and the current value of the next parameter to be displayed. The operator may input a value for this parameter. The up arrow causes the preceding parameter to be displayed and like the line feed the operator may input a value. The carriage return terminates the instruction and causes the exclamation mark (!) to be displayed. If the up arrow terminates the input for the first parameter or the line feed terminates the input for the last parameter, the command is terminated and the exclamation mark (!)

is displayed. If a line feed, carriage return, or up arrow is input without a preceding parameter value, the current value is not changed.

Appropriate responses are described in the parameter descriptor. If a numeric parameter is limited to a range of values, the limits are displayed in the following format.

$$\text{PARAMETER N } (L_N - H_N)$$

where L_N is the minimum value and H_N is the maximum value. All numeric values are decimal unless otherwise noted in the parameter descriptor. Except for the T (text) instruction, alphanumeric parameters require a one character input. Appropriate responses are also described in the parameter descriptor. An incorrect response causes a question mark (?) to be displayed. The operator input for that parameter is cleared, and the operator should input the correct response. Two instructions are common to both the MDM and PCM modes. A definition of the two instructions follows:

TERMINATE MODE

!0

Program control is returned to the supervisor and the mode is requested by displaying:

MODE MDM(M) PCM(P)

TEXT
!T

The appropriate response is an alphanumeric string of 150 characters or less. Lines in the string are delineated by a line feed or carriage return. The string is terminated by a backward slash (\).

3. MDM MODE

3.1 OPERATOR INTERFACE

The following instructions are used to define the operation of the MDM mode. Operator input is underlined; the initial parameter values are also displayed.

INITIALIZE

```
!I      BCE (1 - 8) . . . . . . . . . . . . . . . . . . . . 1 N
        MIA (0 - 31). . . . . . . . . . . . . . . . . . . . 0 A
        RECORD TIME, YES(Y) NO(N) . . . . . . . . . . . . . Y Q
        MODULE (0 - 15) . . . . . . . . . . . . . . . . . . 0 M
        CHANNEL (0 - 31). . . . . . . . . . . . . . . . . . 0 C
```

This instruction initializes the bus control element (BCE) number (N), the multiplexer interface adapter (MIA) address (A), the record time flag (Q), the module (M), and the channel (C). These parameters are constant for each test and need to be entered only once. A Y(yes) response for record time causes the time of execution of the first sequence to be recorded.

MDM COMMAND

```
!M      NUMBER OF DATA WORDS (1 - 32). . . . . . . . . 32 N
        MDM MODE (0 - 15). . . . . . . . . . . . . . . . 0 C
```

This instruction sets the number of data words (N) to transmit or receive and the MDM operation code (C) in the current parameter list.

DATA BUFFER

```
!D      ACKNOWLEDGE (0 - 1) . . . . . . . . . . . . . . . . 0 K
        OPCODE (0 - 15) . . . . . . . . . . . . . . . . . . 1 P
        SPARE BIT 5 (0 - 1) . . . . . . . . . . . . . . . . 0 5
        RECORD NUMBER (0 - 1) . . . . . . . . . . . . . . . 0 R
        C/O IND (0 - 3) . . . . . . . . . . . . . . . . . . 0 I
        SPARE BIT 9 - 10 (0 - 3). . . . . . . . . . . . . . 0 S
        NUMBER OF VALID DATA WORDS (0 - 31) . . . . . 31 V
```

9-10

ENTER DATA IN HEX		COMMAND HEADER WORD XXXX
2	0002	B_2
3	0003	B_3
	⋮	
a	ba	B_a
	⋮	
31	001F	B_{31}
32	0020	B_{32}

This instruction defines the command header word and the following command data word in the current parameter list. The command header word is defined by the acknowledge (K), operation code (P), spare bit 5 (S_5), record number (R), checkout indicator (I), spare bits 9-10 (S_{9-10}), and number of valid command data words (V). The data is defined by the hexidecimal number B_a where a is the buffer address.

WAIT

!W DELAY . . . . . 0 W

This instruction defines a pause in execution of W milliseconds at the completion of the command execution for the current parameter list.

!E SEQUENCE (1 - 20) . . . . . 1 S

This instruction enters the current parameter list as the S*th* command of the list. After the command is entered, the sequence count is incremented by one.

COPY COMMAND

!C SEQUENCE (1 - 20) . . . . . 1 S

This instruction copies the parameters for the S*th* command into the current parameter list.

VALIDATE

!V

This instruction causes the commands and data to be printed. The format is described on page 3-4.

!H COMMAND HEADER WORD HEX . . . . . 4800 H

This instruction is an alternate method of defining the command header word. Bits 9-22 of the command header word are defined as one 16 bit hexidecimal parameter.

EXECUTE

!X NUMBER OF SEQUENCES . . . . . 1 S
NUMBER OF CYCLES. . . . . 1 X

The sequence list of S sequences is executed until manually terminated via sense switch 0 or the list has been executed X times. If X = 0, the list is executed until manually terminated.

3.2 SENSE SWITCH SETTINGS

The following sense switch setting controls execution of the MDM command list. (The ON position indicates the description is true).

Sense Switch	Description
0	Termination execution
1	Matrix printer is online

3.3 DISPLAYS

At the completion of execution, the result of the last transfer for each of the commands executed is displayed. The format of the displays is shown in figure 3-1.

The parameter descriptions are:

MDM EXAMPLE = alphanumeric test description
SEQUENCE# = sequence number

```
MDM TEST                                                    PAGE  1
MDM EXAMPLE


        SEQUENCE#  1      DELAYS#      0     BCE STATUS# 0006
**********************************************************************
*      COMMAND WORD *        *   CMW OR RMW    *      WORD       *      *
* T-R S-SS  MIR WDS * DATA   * MC CD EC CO NV *IDENTIFICATION* STAT *
*--------------------------------------------------------------------*
*  T  1061    3  32 *        *                 *                  *      *
*                 1 * 4801   * 0  9  0  0  1  *  CMW  ACK       *      *
*                 2 * 0002   *                 *  VDW             *      *
*                 3 * 0003   *                 *  FDW             *      *
*                 4 * 0004   *                 *  FDW             *      *
*                 5 * 0005   *                 *  FDW             *      *
*                 6 * 0006   *                 *  FDW             *      *
*                 7 * 0007   *                 *  FDW             *      *
*                 8 * 0008   *                 *  FDW             *      *
*                 9 * 0009   *                 *  FDW             *      *
*                10 * 000A   *                 *  FDW             *      *
*                11 * 000B   *                 *  FDW             *      *
*                12 * 000C   *                 *  FDW             *      *
*                13 * 000D   *                 *  FDW             *      *
*                14 * 000E   *                 *  FDW             *      *
*                15 * 000F   *                 *  FDW             *      *
*                16 * 0010   *                 *  FDW             *      *
*                17 * 0011   *                 *  FDW             *      *
*                18 * 0012   *                 *  FDW             *      *
*                19 * 0013   *                 *  FDW             *      *
*                20 * 0014   *                 *  FDW             *      *
*                21 * 0015   *                 *  FDW             *      *
*                22 * 0016   *                 *  FDW             *      *
*                23 * 0017   *                 *  FDW             *      *
*                24 * 0018   *                 *  FDW             *      *
*                25 * 0019   *                 *  FDW             *      *
*                26 * 001A   *                 *  FDW             *      *
*                27 * 0018   *                 *  FDW             *      *
*                28 * 001C   *                 *  FDW             *      *
*                29 * 001D   *                 *  FDW             *      *
*                30 * 001E   *                 *  FDW             *      *
*                31 * 001F   *                 *  FDW             *      *
*                32 * 0020   *                 *  FDW             *      *
**********************************************************************

MASTER TIMING UNIT  101  13:37:02  954:750  FOR THE FIRST SEQUENCE
```

Figure 3-1.— Sample of MDM format display.

DELAYS# = delay in milliseconds between this and the following command

BCE STATUS# = BCE status (see table 3-1)

I/O = direction of transfer: transmit (T) or receive (R)

9-22 = bits 9-22 of the command word in hexidecimal

MIA = MIA address in hexidecimal

WDS = in the first line, the number of words to transmit or receive.

WDS = in the following lines, the data word entry number

A/C = acknowledge bit

CD = operation code

RC = record number

CO = checkout indicator

NV = number of valid data words

WORD IDENTIFICATION

- CHW = command header word
- ACK = acknowledge (AC = 0)
- NACK = no acknowledge (AC = 1)
- VDW = valid data word
- FDW = fill data word

STAT = data word status (see table 3-2)

Master timing unit indicates the day of the year, hours, minutes, seconds, milliseconds, and microseconds for the execution of the first sequence.

3.4 OPERATOR INTERFACE EXAMPLE

Figure 3-2 is an example of the operator interface entries for one MDM sequence. The T (text) command defines the alphanumeric test descriptor.

The I (initialize) command defines the BCE number, the MIA address, the record time option, the module, and the channel. This instruction needs to be entered only once for each test.

TABLE 3-1.- BCE STATUS CODES

Bit no.	Description	Logic level
(MSB) 0*	Received data with response data word (RDW)	0 = no, 1 = yes
1*	Transmission error	0 = no, 1 = yes
2*	Parity error	0 = no, 1 = yes
3	Received data overflow error	0 = no, 1 = yes
4*	MIA address error	0 = no, 1 = yes
5	"S" error ($\overline{S}$)	0 = no, 1 = yes
6	"E" error	0 = no, 1 = yes
7	"V" error ($\overline{V}$)	0 = no, 1 = yes
8	Parity error	0 = no, 1 = yes
9	Manchester error	0 = no, 1 = yes
10*	Word count error	0 = no, 1 = yes
11	Time out error	0 = no, 1 = yes
12	BCE program control (PC) status	0 = IDLE, 1 = $\overline{\text{IDLE}}$
13	Receiver status	0 = DISABLE, 1 = ENABLE
14	Transmitter status	0 = DISABLE, 1 = ENABLE
(LSB) 15*	Go/no-go status. "OR" of bits 0-11	0 = go, 1 = no-go

*Once they occur, these bits are latched until the status register is saved (SAVST) or a start is detected.

TABLE 3-2.- DATA WORD STATUS CODES

Bit no.	Description	Logic level
(MSB) 0	Spare (All spare bits are zero)	
1	Spare (All spare bits are zero)	
2*	Received data overflow error	0 = no, 1 = yes
3	MIA address error	0 = no, 1 = yes
4*	"S" error (S)	0 = no, 1 = yes
5*	"E" error	0 = no, 1 = yes
6*	"V" error (V)	0 = no, 1 = yes
7*	Manchester error	0 = no, 1 = yes
8*	Parity error	0 = no, 1 = yes
9	Word count error	0 = no, 1 = yes
10	Time out error	0 = no, 1 = yes
11*	MIA address from bus: MSB	
12*	MIA address from bus	
13*	MIA address from bus	
14*	MIA address from bus	
(LSB) 15*	MIA address from bus: LSB	

*The indicators in this word are instantaneous; i.e., they indicate the current status at the time a word is received by the MIA.

```
MODE MDM(M) PCM(P) M

COMMAND      PARAMETER                                              ENTRY

!T
MDM EXAMPLE

!I           BCE (1 - 8).....................................         1
             MIA (0 - 31)....................................         3
             RECORD TIME YES(Y) NO(N)........................         Y
             MODULE (0 - 15).................................         3
             CHANNEL (0 - 31)................................         1

!M           NUMBER OF DATA WORDS (1 - 32)...................        32
             MDM MODE (0 - 15)...............................         8

!D           ACKNOWLEDGE (0 - 1).............................         0
             OPCODE (0 - 15).................................         9
             SPARE BIT 5 (0 - 1).............................         0
             RECORD NUMBER (0 - 1)...........................         0
             C/O IND (0 - 3).................................         0
             SPARE BIT 9 - 10 (0 - 3)........................         0
             NUMBER OF VALID DATA WORDS (0 - 31).............         1

ENTER DATA IN HEX      COMMAND HEADER WORD 4801
     2   0002
     3   0003
     4   0004
     5   0005
     6   0006
     7   0007
     8   0008
     9   0009
    10   000A

!W           DELAY...........................................         0

!H           COMMAND HEADER WORD, HEX........................      4801

!E           SEQUENCE (1 - 20)...............................         1

!C           SEQUENCE (1 - 20)...............................         2   1

!X           NUMBER OF SEQUENCES.............................         1
             NUMBER OF CYCLES................................         0   1
```

Figure 3-2.— Example of operator interface entries for one MDM sequence.

The M (MDM command) defines the number of data words to transmit or receive as well as the MDM mode control field. The D (data) command defines the command header word and the data for a transmittal. The command header word is defined by the acknowledge, operation code, spare bit 5, record number, checkout indicator, spare bits 9-10, and number of valid data words. In the example, a carriage return was input after displaying the tenth data word.

The delay in milliseconds is defined by the W (wait) instruction. The delay follows execution of the associated command. The H (header) command defines the command header word in hexidecimal.

The E (enter) command places the currently defined command in the command list. Normally the commands are entered in the order in which they are to be executed – sequence 1, sequence 2, etc. – but the order may be varied by the operator.

4. PCM MODE

The PCM mode operates on a 1-second cycle. On entry, the BITE status register request (BSRR) is activated every second. Two thousand fetch commands are processed during the cycle. A nominal set of fetch commands may be defined by software. The operator may modify the fetch command set via the operator interface. The operator may also cause the time length of the cycle to drift until it has been increased or decreased by 20 milliseconds. The cycle time may also be varied by adding or deleting null fetch sequences at the end of the cycle (see section 4.4).

All data with physical errors are saved for later analysis. Normally homogeneous data and save data are also stored for analysis.

4.1 OPERATOR INTERFACE

INITIALIZE

```
!I      BCE (1 - 8). . . . . .  1 N
        ERROR THRESHOLD (0 - 100). . . . . 100 E
        GMT TAG YES(Y) NO(N) . . . . . .  N G
        FETCH TABLE ZERO(Z) INITIALIZE(I) NO(N). .  N F
        SET SAVE FLAG YES(Y) NO(N) . . . . . .  N T
        PRINT FETCH TABLE YES(Y) NO(N) . . . . . .  N P
        TEST NORM(0) BCE(1) FORM(2) TRIGGER(3) . .  0 R
        CYCLE MODIFY LONG(L) SHORT(S) NORMAL(N). .  N M
        NUMBER OF SEQUENCES (0 - 4). . . . . .  0 S
```

The I instruction initializes the BCE number (N), the error threshold (E), the Greenwich mean time (GMT) tag (G), the fetch table (F), the fetch command type (T), the data test routine (R), and the number of sequences to add or delete from the cycle (M and S). The fetch table may also be printed by an appropriate response to the PRINT FETCH TABLE instruction. The nominal entries are given in table 4-1.

TABLE 4-1.— SAMPLE OF FETCH SEQUENCE

SEQUENCE	WD ADD(16)	WD ADD(10)	WORDS	TYPE
3	0000	0	10	N
4	000A	10	10	N
22	00A8	168	8	N
23	0000	0	10	N
24	000A	10	6	N
41	0014	20	10	N
42	00B0	176	10	N
43	0000	0	10	N
44	000A	10	6	N
61	001E	30	10	N
62	00BA	186	10	N
63	0000	0	10	N
64	000A	10	6	N
81	0028	40	8	N
82	00C4	196	10	N
83	0000	0	10	N
84	000A	10	6	N
101	0030	48	10	N
102	00CE	206	10	N
103	0000	0	10	N
104	000A	10	10	N
121	003A	58	10	N
122	00D8	216	10	N
123	0000	0	10	N
124	000A	10	6	N
141	0014	20	10	N
142	00E2	226	10	N
143	0000	0	10	N
144	000A	10	6	N
161	001E	30	2	N
162	00EC	236	10	N
163	0000	0	10	N
164	000A	10	6	N
181	0044	68	10	N
182	00F6	246	10	N
183	0000	0	10	N
184	000A	10	6	N
201	004E	78	10	N
202	0100	256	10	N
203	0000	0	10	N
204	000A	10	10	N
221	0058	88	10	N
222	010A	266	10	N
223	0000	0	10	N
224	000A	10	6	N
241	0014	20	10	N
242	0114	276	10	N
243	0000	0	10	N
244	000A	10	6	N
261	001E	30	10	N
262	011E	286	10	N
263	0000	0	10	N
264	000A	10	6	N
281	0028	40	8	N
282	0128	296	10	N
283	0000	0	10	N
284	000A	10	6	N
301	0062	98	10	N
302	0132	306	10	N
303	0000	0	10	N

TABLE 4-1.- SAMPLE OF FETCH SEQUENCE (Continued).

SEQUENCE	WD ADD(16)	WD ADD(10)	WORDS	TYPE
304	000A	10	10	N
321	006C	108	10	N
322	013C	316	10	N
323	0000	0	10	N
324	000A	10	6	N
341	0014	20	10	N
342	0146	326	10	N
343	0000	0	10	N
344	000A	10	6	N
361	001E	30	2	N
362	0150	336	10	N
363	0000	0	10	N
364	000A	10	6	N
381	0076	118	10	N
382	015A	346	7	N
383	0000	0	10	N
384	000A	10	6	N
401	0080	128	10	N
402	0180	384	10	N
403	0000	0	10	N
404	000A	10	10	N
421	008A	138	10	N
422	018A	394	10	N
423	0000	0	10	N
424	000A	10	6	N
441	0014	20	10	N
442	0194	404	10	N
443	0000	0	10	N
444	000A	10	6	N
461	001E	30	10	N
462	019E	414	10	N
463	0000	0	10	N
464	000A	10	6	N
481	0028	40	8	N
482	01A8	424	10	N
483	0000	0	10	N
484	000A	10	6	N
502	01B2	434	10	N
503	0000	0	10	N
504	000A	10	10	N
521	0094	148	10	N
522	01BC	444	10	N
523	0000	0	10	N
524	000A	10	6	N
541	0014	20	10	N
542	01C6	454	10	N
543	0000	0	10	N
544	000A	10	6	N
561	001E	30	2	N
562	01D0	464	10	N
563	0000	0	10	N
564	000A	10	6	N
581	009E	158	10	N
582	01DA	474	10	N
583	0000	0	10	N
584	000A	10	6	N
601	01E4	484	10	N
602	01EE	494	10	N
603	0000	0	10	N
604	000A	10	10	N

TABLE 4-1.- SAMPLE OF FETCH SEQUENCE (Continued).

SEQUENCE	WD ADD(16)	WD ADD(10)	WORDS	TYPE
621	01F8	504	10	N
622	0282	514	10	N
623	0000	0	10	N
624	000A	10	6	N
641	0014	20	10	N
642	028C	524	10	N
643	0000	0	10	N
644	000A	10	6	N
661	001E	30	10	N
662	0216	534	10	N
663	0000	0	10	N
664	000A	10	6	N
681	0028	40	8	N
682	0220	544	10	N
683	0000	0	10	N
684	000A	10	6	N
701	022A	554	10	N
702	0234	564	10	N
703	0000	0	10	N
704	000A	10	10	N
721	023E	574	10	N
722	0248	584	10	N
723	0000	0	10	N
724	000A	10	6	N
741	0014	20	10	N
742	0252	594	10	N
743	0000	0	10	N
744	000A	10	6	N
761	001E	30	2	N
762	025C	604	10	N
763	0000	0	10	N
764	000A	10	6	N
781	0266	614	10	N
782	0270	624	10	N
783	0000	0	10	N
784	000A	10	6	N
801	027A	634	10	N
802	0287	647	5	N
803	0000	0	10	N
804	000A	10	10	N
821	028F	655	5	N
822	0298	664	10	N
823	0000	0	10	N
824	000A	10	6	N
841	0014	20	10	N
842	02A2	674	10	N
843	0000	0	10	N
844	000A	10	6	N
861	001E	30	10	N
862	02AC	684	10	N
863	0000	0	10	N
864	000A	10	6	N
881	0028	40	8	N
882	02B6	694	10	N
883	0000	0	10	N
884	000A	10	6	N
901	02C0	704	10	N
902	02CA	714	10	N
903	0000	0	10	N
904	000A	10	10	N

TABLE 4-1.– SAMPLE OF FETCH SEQUENCE (Continued).

SEQUENCE	WD ADD(16)	WD ADD(10)	WORDS	TYPE
921	02D4	724	10	N
922	02DE	734	10	N
923	0000	0	10	N
924	000A	10	6	N
941	0014	20	10	N
942	02E8	744	10	N
943	0000	0	10	N
944	000A	10	6	N
961	001E	30	2	N
962	02F2	754	10	N
963	0000	0	10	N
964	000A	10	6	N
981	02FC	764	10	N
982	0306	774	10	N
983	0000	0	10	N
984	000A	10	6	N
1001	0310	784	10	N
1002	031A	794	10	N
1003	0000	0	10	N
1004	000A	10	10	N
1022	0324	804	10	N
1023	0000	0	10	N
1024	000A	10	6	N
1041	0014	20	10	N
1042	032E	814	10	N
1043	0000	0	10	N
1044	000A	10	6	N
1061	001E	30	10	N
1062	0338	824	10	N
1063	0000	0	10	N
1064	000A	10	6	N
1081	0028	40	8	N
1082	0342	834	10	N
1083	0000	0	10	N
1084	000A	10	6	N
1101	0030	48	10	N
1102	034C	844	10	N
1103	0000	0	10	N
1104	000A	10	10	N
1121	003A	58	10	N
1122	0356	854	10	N
1123	0000	0	10	N
1124	000A	10	6	N
1141	0014	20	10	N
1142	0360	864	10	N
1143	0000	0	10	N
1144	000A	10	6	N
1161	001E	30	2	N
1162	036A	874	10	N
1163	0000	0	10	N
1164	000A	10	6	N
1181	0044	68	10	N
1182	0374	884	10	N
1183	0000	0	10	N
1184	000A	10	6	N
1201	004E	78	10	N
1202	037E	894	6	N
1203	0000	0	10	N
1204	000A	10	10	N
1221	0058	88	10	N

TABLE 4-1.- SAMPLE OF FETCH SEQUENCE (Continued).

SEQUENCE	WD ADD(16)	WD ADD(10)	WORDS	TYPE
1222	0384	900	10	N
1223	0000	0	10	N
1224	000A	10	6	N
1241	0014	20	10	N
1242	038E	910	10	N
1243	0000	0	10	N
1244	000A	10	6	N
1261	001E	30	10	N
1262	0398	920	10	N
1263	0000	0	10	N
1264	000A	10	6	N
1281	0028	40	8	N
1282	03A2	930	10	N
1283	0000	0	10	N
1284	000A	10	6	N
1301	0062	98	10	N
1302	03AC	940	10	N
1303	0000	0	10	N
1304	000A	10	10	N
1321	006C	108	10	N
1322	03B6	950	10	N
1323	0000	0	10	N
1324	000A	10	6	N
1341	0014	20	10	N
1343	0000	0	10	N
1344	000A	10	6	N
1361	001E	30	2	N
1363	0000	0	10	N
1364	000A	10	6	N
1381	0076	118	10	N
1383	000A	0	10	N
1384	000A	10	6	N
1401	0080	128	10	N
1403	0000	0	10	N
1404	000A	10	10	N
1421	008A	138	10	N
1423	0000	0	10	N
1424	000A	10	6	N
1441	0014	20	10	N
1443	0000	0	10	N
1444	000A	10	6	N
1461	001E	30	10	N
1463	0000	0	10	N
1464	000A	10	6	N
1481	0028	40	8	N
1483	0000	0	10	N
1484	000A	10	6	N
1503	0000	0	10	N
1504	000A	10	10	N
1521	0094	148	10	N
1523	0000	0	10	N
1524	000A	10	6	N
1541	0014	20	10	N
1543	0000	0	10	N
1544	000A	10	6	N
1561	001E	30	2	N
1563	0000	0	10	N
1564	000A	10	6	N
1581	009E	158	10	N
1583	0000	0	10	N

TABLE 4-1.– SAMPLE OF FETCH SEQUENCE (Concluded).

SEQUENCE	WD ADD(16)	WD ADD(10)	WORDS	TYPE
1584	000A	10	6	N
1603	0000	0	10	N
1604	000A	10	10	N
1623	0000	0	10	N
1624	000A	10	6	N
1641	0014	20	10	N
1643	0000	0	10	N
1644	000A	10	6	N
1661	001E	30	10	N
1663	0000	0	10	N
1664	000A	10	6	N
1681	0028	40	8	N
1683	0000	0	10	N
1684	000A	10	6	N
1703	0000	0	10	N
1704	000A	10	10	N
1723	0000	0	10	N
1724	000A	10	6	N
1741	0014	20	10	N
1743	0000	0	10	N
1744	000A	10	6	N
1761	001E	30	2	N
1763	0000	0	10	N
1764	000A	10	6	N
1783	0000	0	10	N
1784	000A	10	6	N
1803	0000	0	10	N
1804	000A	10	10	N
1823	0000	0	10	N
1824	000A	10	6	N
1841	0014	20	10	N
1843	0000	0	10	N
1844	000A	10	6	N
1861	001E	30	10	N
1863	0000	0	10	N
1864	000A	10	6	N
1881	0028	40	8	N
1883	0000	0	10	N
1884	000A	10	6	N
1903	0000	0	10	N
1904	000A	10	10	N
1923	0000	0	10	N
1924	000A	10	6	N
1941	0014	20	10	N
1943	0000	0	10	N
1944	000A	10	6	N
1961	001E	30	2	N
1963	0000	0	10	N
1964	000A	10	6	N
1983	0000	0	10	N
1984	000A	10	6	N

If the error threshold is greater than zero, transmission errors are counted, and if the error count equals or exceeds the threshold, execution is terminated. If E = 0, execution is not terminated by the error count. The GMT tag flag set to yes (Y) causes the data to be time tagged. The fetch command table may be set to null (zeros), initialized to nominal values, or left unchanged. If it is set to nominal, the type of each fetch command is null. The SET SAVE FLAG instruction sets all fetch command types to save.

The type of processing is specified by the test parameter. The commands NORM (0) and BCE (1) interrogate the BCE status and save the data if an error is detected. Save and homogeneous data are also preserved for display. The commands FORM (2) and TRIGGER (3) are similar and work in conjunction with the FORMAT (F) instruction. A sequence number and bit pattern are specified by the FORMAT instruction. The command FORM compares the bit pattern with the first data word of the specified sequence. If they differ, the data are saved for display and the error count incremented. Save, homogeneous, and error data are also saved.

In the trigger test mode, save and homogeneous data normally are not saved. The TRIGGER instruction compares the bit pattern with the first data word of the specified sequence. If they are unequal, the data replaces the compare bit pattern. Save and homogeneous data are saved until the next trigger compare. If they are equal, save and homogeneous data are not preserved. The CYCLE MODIFY instruction specifies a long cycle (greater than 2000 fetches), a short cycle (less than 2000 fetches), or a normal cycle (2000 fetches). The NUMBER OF SEQUENCES instruction specifies the number of null fetches to lengthen or shorten the cycle.

PCM COMMAND

```
!P      SEQUENCE (1 - 2000). . . . . .          1 S
        NUMBER OF RESPONSE DATA WORDS (1 - 32) . .  1 N
        MODE CONTROL FIELD (0 - 7) . . . . . .  1 M
        STARTING ADDRESS, HEX (0 - 3FF). . . . . 0000 A
        RCVR ADDRESS (0-31). . . . . .          0 R
        TYPE SAVE(S) HOMOGENEOUS(H) NO(N). . . . .  N T
```

This instruction defines the number of response data words (N), the mode control field (M), the starting address (A), the receiver address (R), and data type (T) for sequence (S).

DRIFT

```
!D      DRIFT POSITIVE(+) NEGATIVE(-) NO(N). . . . . .   N Q
```

The drift rate (Q) may be set positive (+), negative (-), or no drift (N). For a positive drift, the PCM sequence time is increased by 1 microsecond per sequence until an error is detected or the sequence time reaches 520 microseconds. The drift is then reversed and the sequence time is decreased at 1 microsecond per cycle until the nominal value of 500 microseconds is reached. For a negative drift, the operation is similar. The sequence time is decreased until an error is detected or a sequence time of 480 microseconds is reached. The drift is then made positive. No drift (N) causes the sequence time to remain at 500 microseconds throughout the test.

RECORD

```
!R      START CYCLE . . . . . .          1 C
        NUMBER OF CYCLES. . . . . .          0 N
        TYPE ALL(A) ERROR(E) HOMOGENEOUS(H) SAVE(S) . .   A T
```

The fetch commands and data of the specified type (T) between cycle C and C + N - 1 are displayed. If C = 0, then the starting cycle is 1. If N = 0, then data for all cycles from C until the last cycle in the display is printed.

FORMAT

```
!F      NUMBER OF FORMATS (0 - 10). . . . . .    0 N
        SEQUENCE NUMBER (PREVIOUS VALUE - 2000) . . .    1 S1
        FORMAT, HEX . . . . . . . . . . . . . . . . 0000 F1
        SEQUENCE NUMBER (PREVIOUS VALUE - 2000) . . .    2 S2
        FORMAT, HEX . . . . . . . . . . . . . . . . 0000 F2
                                :
        SEQUENCE NUMBER (PREVIOUS VALUE - 2000) . . .    m Sm
        FORMAT, HEX . . . . . . . . . . . . . . . . 0000 Fm
```

The first data word of each of the specified sequences (S) is tested for a specified bit pattern (F) if the form or trigger test is operational. See the explanation of these two tests under the initialize instruction.

EXECUTE

!X

DRIFT DDD
CYCLE CCC

```
        NUMBER OF CYCLES. . . . . .    0 C
```

The PCM fetch command list is executed C times. If C = 0, the cycle is executed until manually terminated or until the 12 thousand word data buffer is filled. The character string DDD specifies the condition of the drift parameter as positive, negative, or off. The character string CCC specifies the condition of the CYCLE MODIFY instruction as short, long, or normal.

4.2 SENSE SWITCH SETTINGS

Setting sense switch zero to on terminates recording at the completion of the current fetch cycle execution. Sense switch one set to on indicates the matrix printer is online.

4.3 OPERATION INTERFACE EXAMPLE

Figure 4-1 is an example of the operator interface entries for the PCM mode. Three fetch commands are defined. Sequence 3 has

```
MODE MDM(M) PCM(P) P

COMMAND      PARAMETER                                              ENTRY

!T
PCM EXAMPLE

!P           SEQUENCE (1 - 2000).....                                 1   3
             NUMBER OF RESPONSE DATA WORDS (1 - 32) .....             1   11
             MODE CONTROL FIELD (0 - 7).....                          0
             STARTING ADDRESS, HEX (0 - 3FF).....                  0000   3
             RCVR ADDRESS (0 - 31).....                               0
             TYPE SAVE(S) HOMOGENEOUS(H) NO(N).....                   N   S

!P           SEQUENCE (1 - 2000).....                                 3   21
             NUMBER OF RESPONSE DATA WORDS (1 - 32).....              1   11
             MODE CONTROL FIELD (0 - 7).....                          0
             STARTING ADDRESS, HEX (0 - 3FF).....                  0000   21
             RCVR ADDRESS (0 - 31).....                               0
             TYPE SAVE(S) HOMOGENEOUS(H) NO(N).....                   N   H

!P           SEQUENCE (1 - 2000).....                                21   24
             NUMBER OF RESPONSE DATA WORDS (1 - 32) .....             1   11
             MODE CONTROL FIELD (0 - 7).....                          0
             STARTING ADDRESS, HEX (0 - 3FF).....                  0000   24
             RCVR ADDRESS (0 - 31).....                               0
             TYPE SAVE(S) HOMOGENEOUS(H) NO(N).....                   N

!X
DRIFT OFF
CYCLE LENGTH NORMAL
             NUMBER OF CYCLES .....                                   0   5

!R           START CYCLE.....                                         1
             NUMBER OF CYCLES.....                                    5
             TYPE ALL(A) ERROR(E) HOMOGENEOUS(H) SAVE(S).....         A
```


Figure 4-1.– Example of the operator interface entries for the PCM mode.

a save fetch, 21 is a homogeneous command, and 24 is neither. All three transfer 11 words. During execution, five cycles are processed, and the data for the five cycles are printed. The display is shown in figure 4-2.

The start time of each cycle is shown as day of the year, hours, minutes, seconds, milliseconds, and microseconds. Bits 9-22 of the fetch command are displayed in hexidecimal. The response time between the command word and the first data word is shown in microseconds. The first 10 words of data are displayed in hexidecimal with the word status shown below the word. The BCE status is shown, and if an error is indicated by the status, a question mark is displayed to the right of the status.

4.4 OPERATION

When the PCM mode is entered, the interval timer clock is set for a 1-second interrupt. When this interrupt occurs, a BSRR is issued. The interrupt occurs every second until the execute (X) command is initiated. When execute is initiated, the next interval timer interrupt causes the BSRR to be issued and the interval timer is set to 500 microsecond. Execution of the fetch command sequence begins with sequence 2 of the fetch command sequence.

The fetch command sequence consists of two thousand sequences organized in blocks of twenty. Each block, except for the first, consists of four sequences, which may contain fetch commands or nulls followed by 16 null sequences. Sequences 1 and 2 of the first block are reserved respectively for the BSRR and the interval timer modification if drift is activated. If drift is not initiated, sequence 2 contains a null.

During the 16 null sequences, the data transferred during the first four sequences is processed.

```
PCM TEST                                                                    PAGE  1
PCM EXAMPLE


*****************************************************************************************
*CYCLE FETCH  NO  R-T   DATA/STATUS TAG              DATA ERROR DISPLAYS = ?          ECE   *
*  #    CMD  WRDS          0     1     2     3     4     5     6     7     8     9  STATUS*
*****************************************************************************************
   1                          MASTER TIMING UNIT    102  11:32:40  560.625                 *
*  1   0003  11  14.2  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC         *
*                      0039  0010  0010  0010  0010  0010  0010  0010  0010  0010  000E  *
*  1   0021  11  14.2  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC         *
*                      0039  000F  000F  000F  000F  000F  000F  000F  000F  000F  000E  *
*  2                          MASTER TIMING UNIT    102  11:32:41  560.750                 *
*  2   0003  11  13.7  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC         *
*                      0037  0010  0010  0010  0010  0010  0010  0010  0010  0010  000E  *
*  2   0021  11  13.7  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC         *
*                      0037  0010  0010  0010  0010  0010  0010  0010  0010  0010  000E  *
*  3                          MASTER TIMING UNIT    102  11:32:42  560.750                 *
*  3   0003  11  13.7  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC         *
*                      0037  0010  0010  0010  0010  0010  0010  0010  0010  0010  000E  *
*  3   0021  11  13.7  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC         *
*                      0037  0010  0010  0010  0010  0010  0010  0010  0010  0010  000E  *
*  4                          MASTER TIMING UNIT    102  11:32:43  560.750                 *
*  4   0003  11  14.0  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC         *
*                      0038  0010  0010  0010  0010  0010  0010  0010  0010  0010  000E  *
*  4   0021  11  13.7  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC         *
*                      0037  0010  0010  0010  0010  0010  000F  000F  000F  000F  000E  *
*  5                          MASTER TIMING UNIT    102  11:32:44  560.750                 *
*  5   0003  11  14.0  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC         *
*                      0038  0010  0010  0010  0010  0010  0010  0010  0010  0010  000E  *
*  5   0021  11  14.0  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC  54CC         *
*                      0038  0010  0010  0010  0010  0010  0010  0010  0010  0010  000E  *
OUT OF DATA
*****************************************************************************************
          TOTAL FETCHES =  10
          TOTAL ERRORS  =   0
```

Figure 4-2.— Sample of PCM format display.

If the command CYCLE MODIFY is active, the last block of the cycle is made shorter for a MODIFY SHORT instruction or longer for a MODIFY LONG instruction by the specified number of sequences.

On completion of a sequence, execution of the fetch sequence is terminated if one or more of the following is true.

- Sense switch 0 is on
- The specified number of cycles has been executed
- The number of detected errors equals or exceeds the error threshold
- The 12 thousand word data buffer is full.

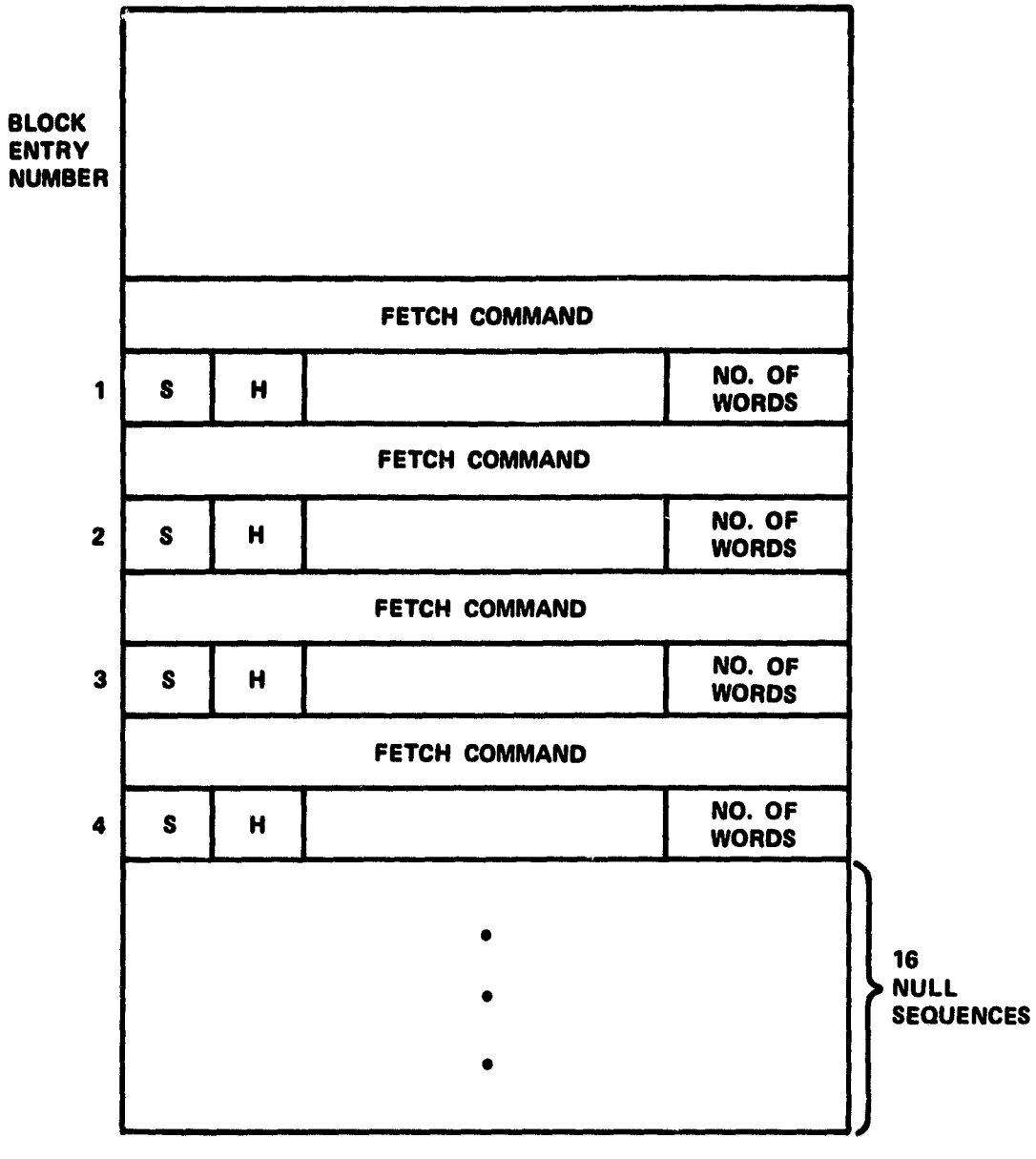
Otherwise the fetch cycle is executed again. On completion of fetch cycle execution, a BSRR is transmitted and the 1-second interrupt is activated. Control is returned to the PCM operator interface.

4.5 FETCH COMMAND CYCLE

The format of the fetch command sequence is given in figure 4-3. The cycle is made up of 100 blocks of 20 sequences each. Each block except the first consists of four sequences which may contain either fetch or null commands followed by 16 null sequences. Sequences 1 and 2 of block one are reserved for the BSRR and interval timer modify, respectively.

4.6 DATA TABLE FORMAT

A maximum of 12,000 words of data may be preserved for processing and display. The format is given in figure 4-4. The BSRR subtable precedes the entries for each cycle. If no entries are saved for a given cycle, the BSRR entry is not saved. The time subtable is preserved as a user option but like the BSRR subtable is only saved if data for that cycle is saved.



S = SAVE DATA

H = HOMOGENEOUS DATA (IF THE HOMOGENEOUS BIT IS SET, THE SAVE DATA BIT WILL ALSO BE SET.)

Figure 4-3.— Fetch command block.

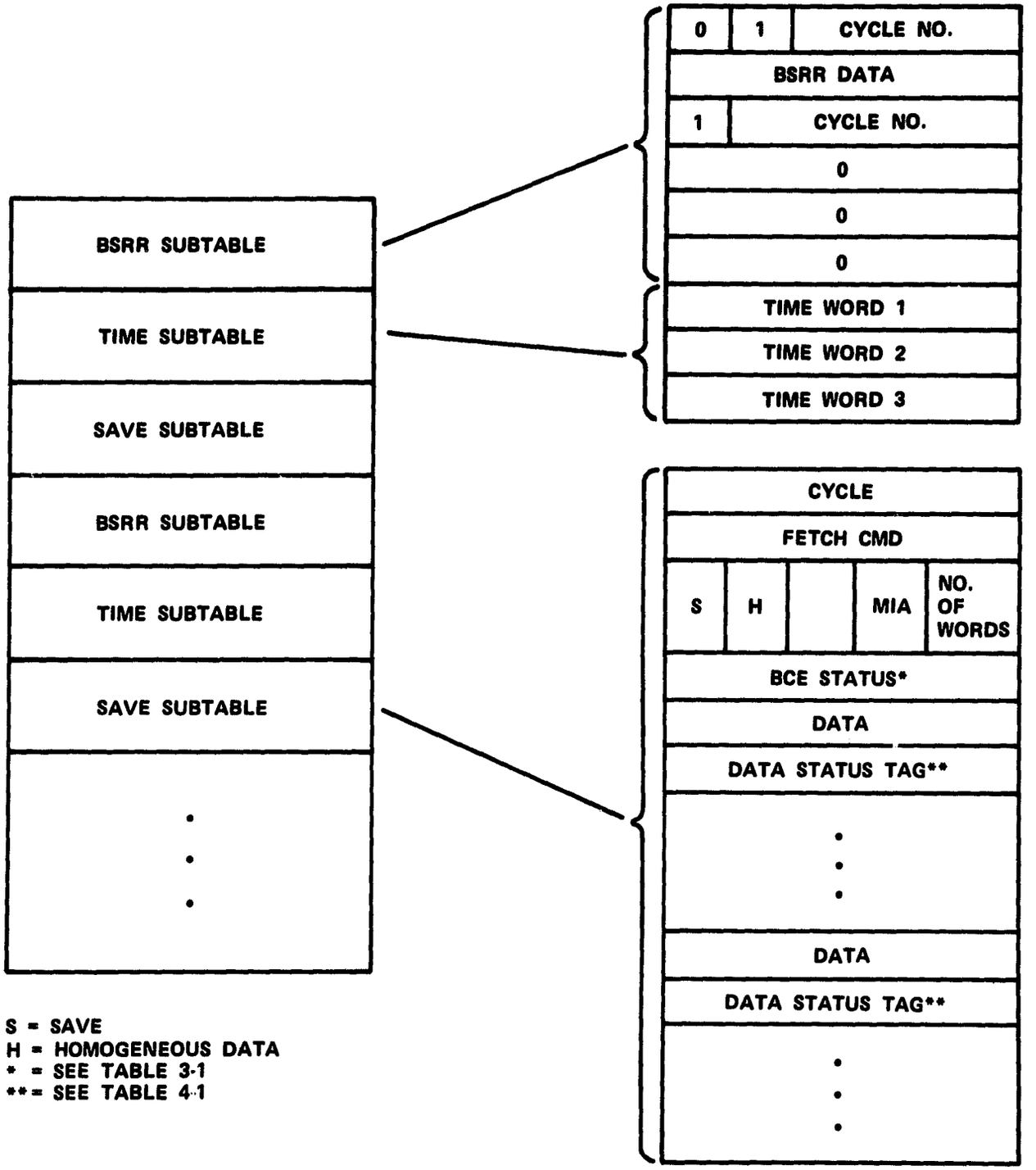


Figure 4-4.– Data table format.

4.7 DISPLAYS

The format of the PCM displays is illustrated in figure 4-2. The time for each displayed cycle is given in day of the year, hours, minutes, seconds, milliseconds, and microsecond. The cycle number, bits 9-22 of the fetch command, the number of words transferred, and the response time between the command and the first data word are shown. Also displayed are the data words, the data status tag, and the BCE status. The format of the data status tag is given in table 4-2. If the BCE status indicates an error, a question mark (?) is displayed to its right. If more than 10 words are transferred, only the first 10 are displayed.

TABLE 4-2.– DATA STATUS TAG

Bit No.		Description	Logic level
(MSB)	0	Spare	
	1	Spare	
	2	Error ("OR" of bits 3 to 8)	0 = no, 1 = yes
	3	Manchester error	0 = no, 1 = yes
	4	Parity error	0 = no, 1 = yes
	5	Word bit count error	0 = no, 1 = yes
	6	"S" error (subsystem power cycle)	0 = no, 1 = yes
	7	"E" error (serial input/output)	0 = no, 1 = yes
	8	"V" error (validity)	0 = no, 1 = yes
	9	Gap time, 16 µs	
	10	Gap time, 8 µs	
	11	Gap time, 4 µs	
	12	Gap time, 2 µs	
	13	Gap time, 1 µs	
	14	Gap time, 0.500 µs	
(LSB)	15	Gap time, 0.250 µs	

NOTES: Bits 2 through 15 indicate instantaneous status at the time the total word is received by the MIA. All spare bits are zero. Maximum gap time equals 31.75 µs.