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TMS Communications Hardware Volume I: Computer Interfaces

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ABSTRACT

MITRE has designed and installed a prototype coaxial cable bus communications system for NASA evaluation at the Johnson Space Center. The bus is to be used in the Trend Monitoring System (TMS) to connect intelligent graphics terminals (based around a Data General NOVA/3 computer) to a MODCOMP IV host minicomputer. This report gives details of the direct memory access (DMA) interfaces which were utilized for each of these computers. For the MODCOMP, an off-the-shelf board was suitable, while for the NOVAs, custom interface circuitry was designed and implemented.

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INTRODUCTION

1.0 BACKGROUND

In preparation for the Operational Flight Tests (OFT) of the Space Shuttle, NASA's Johnson Space Center (JSC) determined that near real time monitoring of key thermal parameters would be needed during the tests. The Structures and Mechanics Division (SMD) requested that the Institutional Data Systems Division (IDSD) develop an interactive graphics display capability to make available plots of the desired thermal data as soon as possible after the data arrived at JSC.

In response to this requirement, IDSD's Engineering and Special Development Branch (FD7) developed the Trend Monitoring System (TMS), which is built around a MODCOMP IV/35 host minicomputer and a number of MEGATEK 5000 intelligent graphics terminals. MITRE was first assigned responsibilities in the development of the initial design [1]. Since the MODCOMP and the MEGATEKS are to be located in different JSC buildings, the TMS project was viewed as an opportunity to install a prototype bus communications system for evaluation by NASA/JSC, and MITRE was assigned this responsibility as well. The resulting communications system and supporting graphics software are described in a series of MITRE reports ([2], [3], [4], [5], [6], [7]).

1.1 Overview of Report

An important part of the installation of the prototype bus communications system was the development of hardware interfaces to the

MODCOMP and the MEGATEKs. In each case, a 16-bit parallel direct memory access (DMA) interface was chosen for speed reasons. In the MODCOMP, a standard (unmodified) Model 4805-1 General Purpose Data Terminal board was cabled to a BIU, which was then programmed to support the existing I/O protocol. In the MEGATEKs, which are based around Data General NOVA 3 computers, interface logic was added to a Data General Model 4040 General Purpose Interface Board to support a MITRE-developed board-to-BIU protocol. This report describes each of these hardware interfaces in sufficient detail to allow maintenance of the prototypes by NASA or to permit construction of additional copies of the prototype, if desired. For the 4805, switch settings and cabling are described, while for the 4040, cabling specifications and detailed circuit descriptions are given for the added logic. Protocol discussions are given in [5]. The discussion in the remainder of the report assumes a basic familiarity with MODCOMP and NOVA I/O operation and terminology; background information of this sort can be found in documents such as [8] and [9].

SECTION II

MODCOMP 4805 GENERAL PURPOSE DATA TERMINAL BOARD

2.0 INTRODUCTION

The MODCOMP Model 4805-1 General Purpose Data Terminal board is offered by MODCOMP as a means of interfacing a variety of custom devices to the computer. The board contains 16 bidirectional data lines, a 6-bit command register, and 7 lines for external device status. A line is also provided to allow the external device to cause an I/O interrupt. A detailed description of the theory of operation and of interfacing considerations is given in [10].

In the Trend Monitoring System, the 4805 is used unmodified, and the symbiont in the MODCOMP interfaces with the 4805 through the standard CL I/O handler. The BIU communicates with the MODCOMP through the handshaking lines shown in Table 2.0-I and with the symbiont through the status lines shown in the same tables.

2.1 Switch Settings

The 4805 boards as supplied by MODCOMP are of three different hardware revision levels -- revision E, EA, and F. Revision EA and F appear to be identical; in revision E, the 4805 is considered as a Class I/II Controller, whereas in revision EA it is considered as a Class II/III Controller. This difference affects the setting of one switch (XU2D switch 1).

The revision E 4805 is considered to be the normal TMS interface board, while the revision EA board is reserved for use as a backup board. The revision F board is installed in the Special Telemetry Conversion System (STCS) computer for possible backup use if TMS is run on that system. Table 2.1-I shows how the DIP switches on the boards should be set in each computer.

Table 2.0-I

TMS MODCOMP 4805 Status and Handshaking Lines

Status Lines Set by BIU

MODCOMP Signal Name	TMS Signal Name	Meaning
IST13N	S5	More data available from BIU for MODCOMP
IST11N	S4	Timer has expired in BIU
IST05N	S3	[Wired, but not used presently]

Handshaking Lines Used by BIU

MODCOMP Signal Name	Meaning
ODSTBN	Output Data Strobe
ODACCN	Output Data Accepted
LDIBFN	Load Input Buffer
INBMTN	Input Buffer Empty
BUSYN	Busy
EXTSIN	External Service Interrupt Request

Table 2.1-1

Switch Settings for MODCOMP 4805 Boards

DIP Switch Coordinate	Switch	TMS	STCS	Interpretation
XU2D	1	*	*	Controller class
	2	On	Off	
	3	On	On	DMP channel number
	4	Off	Off	
	5	On	Off	
XU1D	1	Off	Off	Register file/memory file DMP
	2	On	On	
	3	Off	Off	
	4	Off	Off	I/O priority
	5	On	On	
XV7D	1	Off	Off	Status bit 3 high is Okay
	2	Off	Off	I/O priority 16
	3	On	On	
	4	On	On	
	5	On	Off	Device address
	6	On	On	
	7	Off	Off	
	8	On	Off	
XU1P	All	Off	Off	
XV1S	All	On	On	
XV1T	All	On	On	

NOTES: 1. Switches in asterisked locations are on for revision E boards and off for revision EA and F boards.

2. On switch position corresponds to "closed", or binary zero. Off corresponds to "open", or binary one.

2.2 Cabling and Installation

The 4805 board is normally connected to its BIU using a flat cable composed of twisted pairs of wire. At the BIU, the cable is terminated in Amphenol 50-pin male connection (part number 57-30500), while at the 4805, the cable is terminated in three 26-pin female connectors (MODCOMP part number 667-200003-001) marked P1, P2, and P3. The connector P1 is attached at 4805 board position C3, P2 at C2, and P3 at C1. Table 2.2-I gives the connections for the cables; for ease of signal tracing, edge connection pins in the BIU have also been shown.

For running the MODCOMP-supplied diagnostic programs (part number 181-605892-001) for the 4805 board, the cable must be replaced with a standard MODCOMP cable (part number 560-100004-XXX, where the XXX specifies only cable length and is irrelevant for this test), to which a diagnostic terminator (part number 551-100180-001) has been attached.

Table 2.2-I

MODCOMP 4805 to BIU Cable

MODCOMP Signal Name	4805 Connector	BIU's Amphenol Connector	BIU Edge Connector
IBD00N	P1 pin 1	43	67
IBD01N	P1 pin 2	42	68
IBD02N	P2 pin 3	41	69
IBD03N	P1 pin 4	40	70
IBD04N	P1 pin 5	39	71
IBD05N	P1 pin 6	38	72
IBD06N	P1 pin 7	37	73
IBD07N	P1 pin 8	36	74
IBD08N	P1 pin 9	33	80
IBD09N	P1 pin 10	32	81
IBD10N	P1 pin 11	31	82
IBD11N	P1 pin 12	30	83
IBD12N	P1 pin 13	29	84
IBD13N	P2 pin 1	28	85
IBD14N	P1 pin 2	27	86
IBD15N	P2 pin 3	26	87
ODSTBN	P2 pin 8	34	75
ODACCN	P2 pin 5	35	76
LDIBFN	P2 pin 7	44	88
INBMTN	P2 pin 6	45	89
SIGNAL GROUND		25, 46-50	61
CHASSIS GROUND		1	
PWRN	P2 pin 12	12	56
BUSYN	P2 pin 10	19	49
IST13N (S5)	P3 pin 5	8	42
IST11N (S4)	P3 pin 3	7	43
IST05N (S3)	P2 pin 2	6	44
EXTSIN	P2 pin 11	9	41

SECTION III

DATA GENERAL MODEL 4040 GENERAL PURPOSE INTERFACE BOARD

3.0 INTRODUCTION

The NOVA DMA Interface has been implemented on a Data General 4040 General Purpose Interface board. The virgin 4040 contains the required busy, done, interrupt and DMA logic, device decoding, etc. for interfacing to the NOVA's I/O bus. In general, the user who wishes to utilize these functions must implant his own logic on the designated user space on the board, and tie to the Data General built logic on the other side.

In the TMS project, the full capabilities of the 4040 have been utilized to create an interface that can perform DMA I/O to anywhere in NOVA address space, with full interrupt capability and done/busy logic. The unit also handshakes with a BIU, through the latter's parallel 16 bit bidirectional interface [3].

3.1 Functional Description

The DMA operation on the 4040 interface board occurs as follows:

The DMA Word Count register is set under program control to represent the number of words to be transferred [see paragraph 3.3, which deals with such programming]. The starting NOVA address for the transfer is then loaded into the DMA Address Register. The DMA is activated via an appropriate command with suitable bits set in the accumulator, to establish the direction of the transfer. The transfer rate is then controlled by the speed with which the BIU handshakes with the DMA interface (which is slower than the NOVA memory cycle). DMA cycle requests are made to the NOVA memory control from the DMA interface as each NOVA-BIU handshake (16-bit transfer) is made. The interface Word Count register and Address Register are incremented for each word transferred. Two 16-bit registers in the Data General supplied logic buffer data going to and from the BIU.

Assuming the DMA has been initialized properly, the NOVA Busy flag will be set when the DMA is activated. This lets the NOVA CPU (and the BIU) be aware of the DMA transfer in progress. Following DMA block transfer completion, the Word Counter on the interface will reach zero, and consequently will cause an interrupt. At the same time, the NOVA Done flag is set and the Busy flag is reset.

During times when the DMA is running or idle, the word count address count, or BIU status may be read into the accumulator under program control. [Be aware of some data inversions, see paragraph 3.3.]

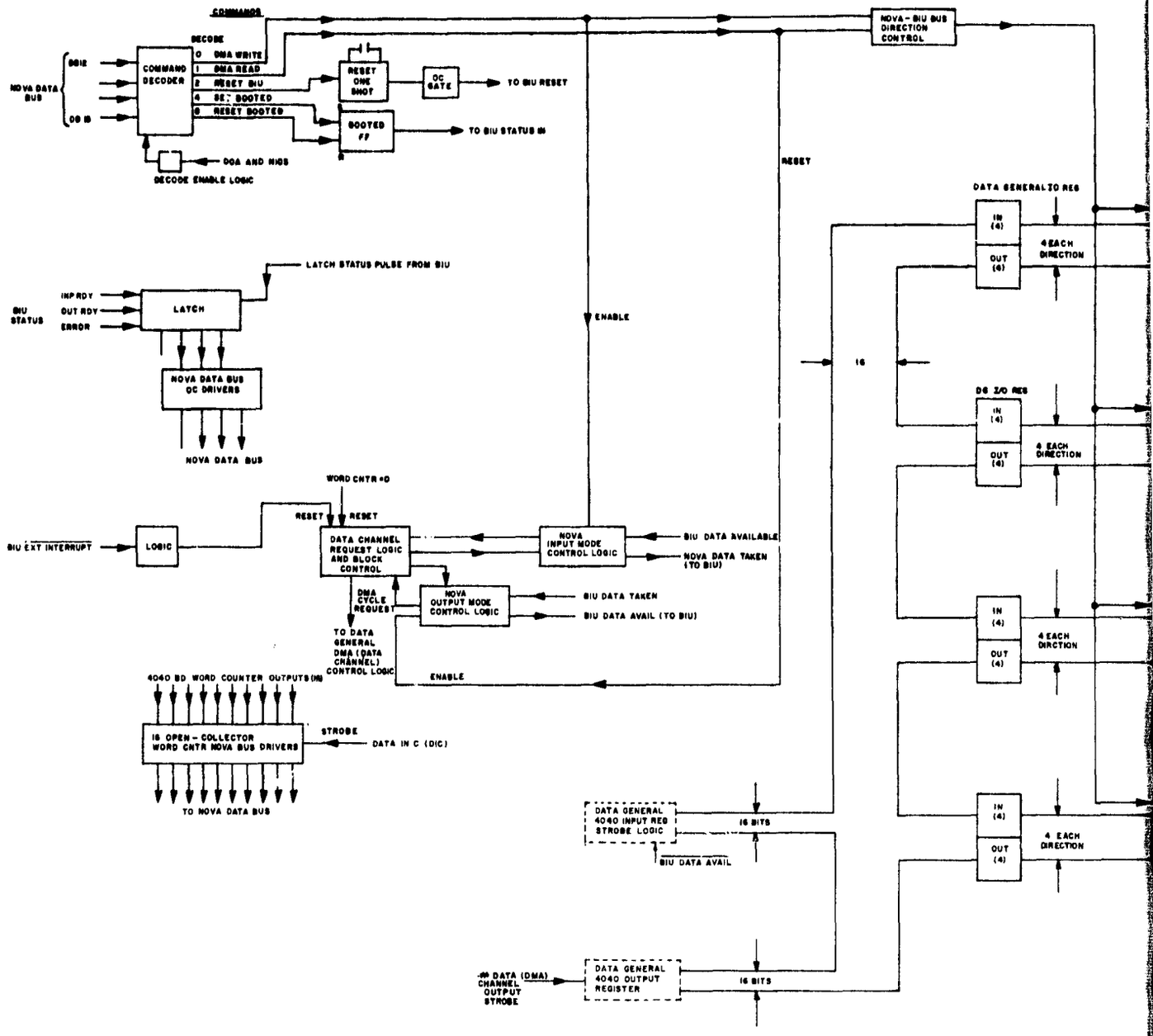
Since the NOVA interface handshakes with the BIU to exchange 16-bit bidirectional data, the direction of the NOVA-BIU data transfer is controlled via the NOVA program instruction that activates the interface.

3.2 Technical Description

The following description is made with respect to the DMA interface schematic (Figure 3.2-2). Referral to Figure 3.2-1, a functional block diagram, will be helpful. Figure 3.2-3, a description of how the added logic chips are laid out on the custom interface portion of the 4040 board, is useful in relating the schematic to the actual board.

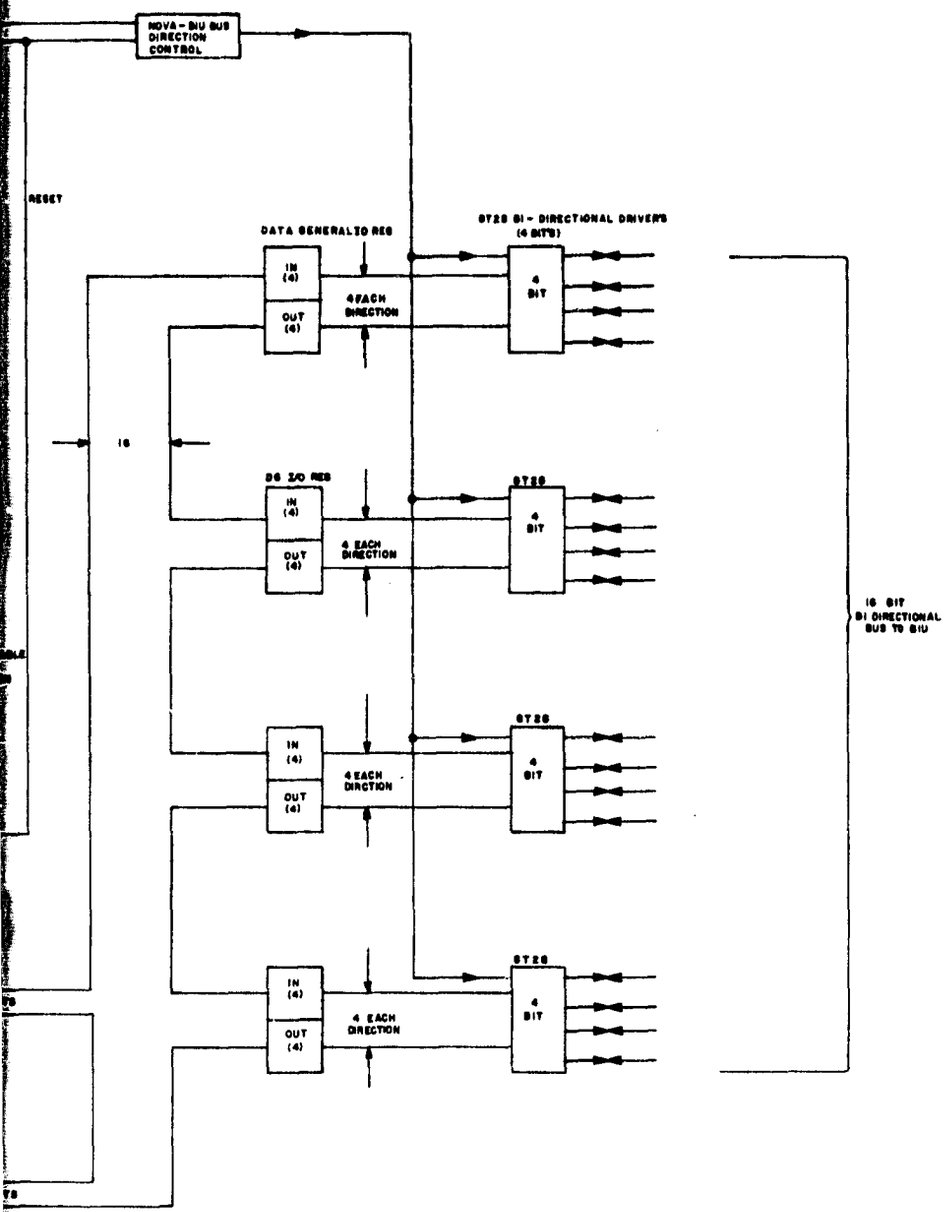
(A) NOVA-BIU Data Bus. The data path between the NOVA and the BIU consists of a 16-bit bidirectional bus. Four 8T28 tri-state buffer integrated circuits (ICs) at slots 1H, 1J, 1K, and 1L perform the buffering and directional control. NOVA-BIU data lines have 200-ohm pullup resistors (to +5V) which reside on packages 4H, 4J, 2K, and 2L. The pullups are intended to reduce line ringing by approximately terminating each line (within the capabilities of the 8T28).

The bus direction is controlled by running pins 15 and 1 of each 8T28 to the bus direction control logic consisting of the Data Channel Mode flip-flop in Slot 2D (DCH MODE). A high on the Q output of this flip-flop (2D pin 9) causes the NOVA to send (output) data on these lines to the BIU.



FOLDOUT FRAME

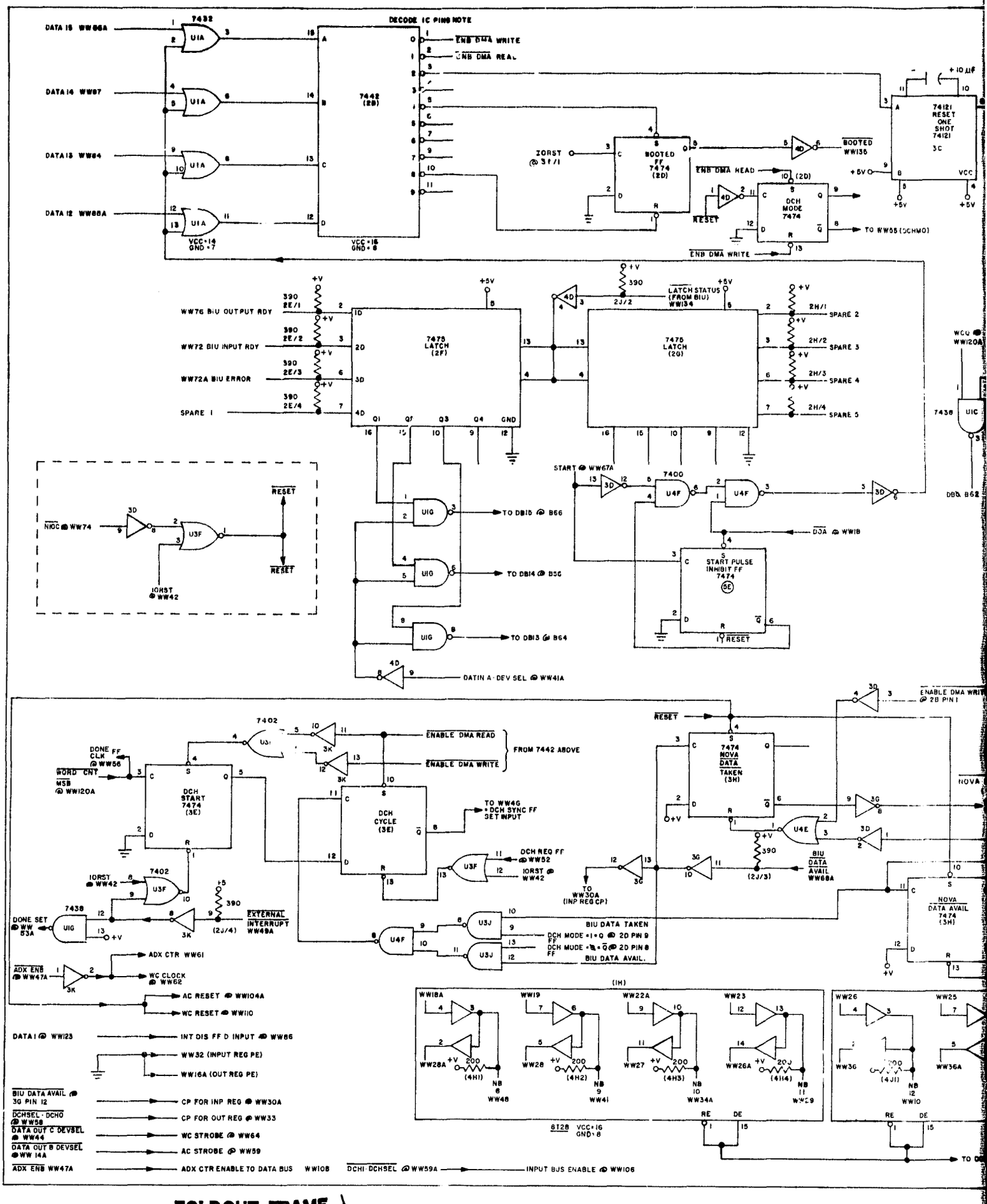
Figure 3.2-1. NOV



GROUP	FIND NO	QTY REQ	DESCRIPTION	PART NO	MATERIAL
	DRAFTER	S BROWN	DATE 9/27/71	MITRE	BEDFORD MASSACHUSETTS
	CHECKER	JOHNSON	10-11-71		
	ENGINEER			TITLE	DMA INTERFACE FUNCTIONAL DIAGRAM
	RELEASE				
	PROJECT	847C	QD0721	SIZE	DRAWING NUMBER
	CODE IDENT NUMBER			E	000635-1
NEXT ASSEMBLY	DO NOT SCALE			SCALE	SHEET

Figure 3.2-1. NOVA DMA Interface Functional Block Diagram

FOLDOUT FRAME 2



FOLDOUT FRAME

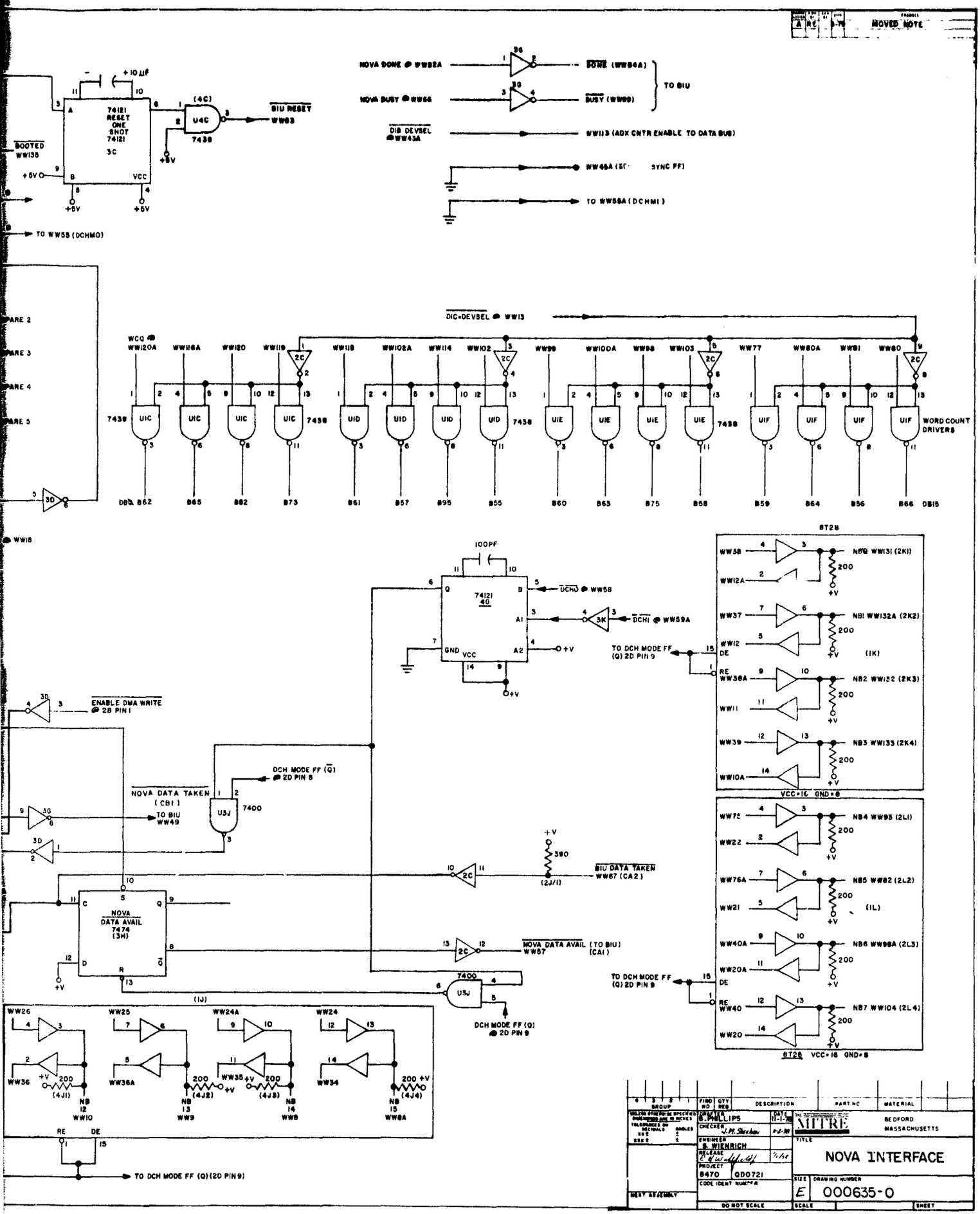
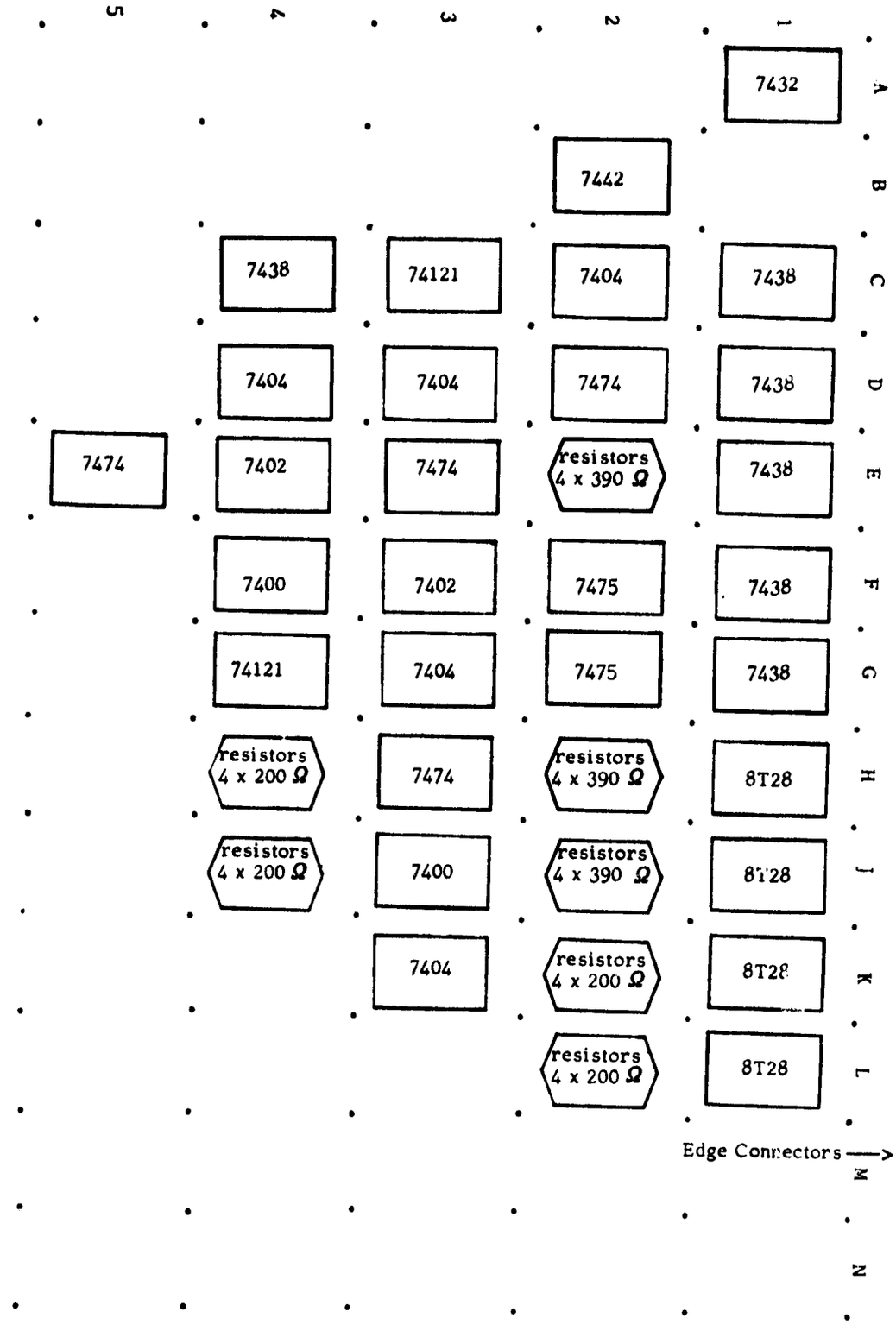


Figure 3.2-2. NOVA DMA Interface Schematic

FOLDOUT FRAME 2



Note: View is of upper surface of board.

Figure 3.2-3 Chip Layout On Custom-Wired Portion of Data General 4040 Board

Output data to the 8T28 bus drivers is supplied from the Data General Output Register (Option 4041 - see the Data General schematic in Section VI of [9]). Input data from the BIU for the NOVA is loaded into the Data General Input Register (ICs U17-U20).

The Data General Input Register is strobed on the falling edge of $\overline{\text{BIU DATA AVAILABLE}}$. Data for the Output Register, being supplied by the DMA from the NOVA memory, is loaded into this register by a DMA-related signal, DCHO . DCHSEL, which is the selected DCHO for this interface (Data General CPU signal). This information is summarized in Figure 3.2-4. The abbreviation WWxx used in this and other figures refers to the 4040 Wire-Wrap pin specified by the xx.

(B) BIU-NOVA Handshake Logic.

(1) NOVA DMA Read (Data Out to BIU). For transfers in which data are to go from the NOVA to the BIU, two handshaking signals are involved. These are NOVA DATA AVAILABLE and BIU DATA TAKEN and are passed between the NOVA and BIU as active low signals.

NOVA-to-BIU handshaking begins when the NOVA loads data into the Output Register (via DMA), which consequently causes $\overline{\text{NOVA DATA AVAILABLE}}$ to transition from high to low. Figure 3.2-5 shows that the one shot at 4G issues a positive pulse on 3J pin 4 (because of the DMA DCHO signal) which causes the $\overline{\text{NOVA DATA AVAILABLE}}$ flip-flop to make this transition. (At this time the logic level on 3J pin 5 must previously have been set high, since this description is of a data output operation by the NOVA.)

When the BIU responds by taking the offered data, it transitions $\overline{\text{BIU DATA TAKEN}}$ from high to low. This consequently sets $\overline{\text{NOVA DATA AVAILABLE}}$ high, thereby completing the handshake cycle. Note that the high to low transition of $\overline{\text{BIU DATA TAKEN}}$ also pulses the DMA logic such that a subsequent DMA read (NOVA data output) cycle is requested if the interface Word Counter had not reached zero as a result of the most recent DMA cycle.

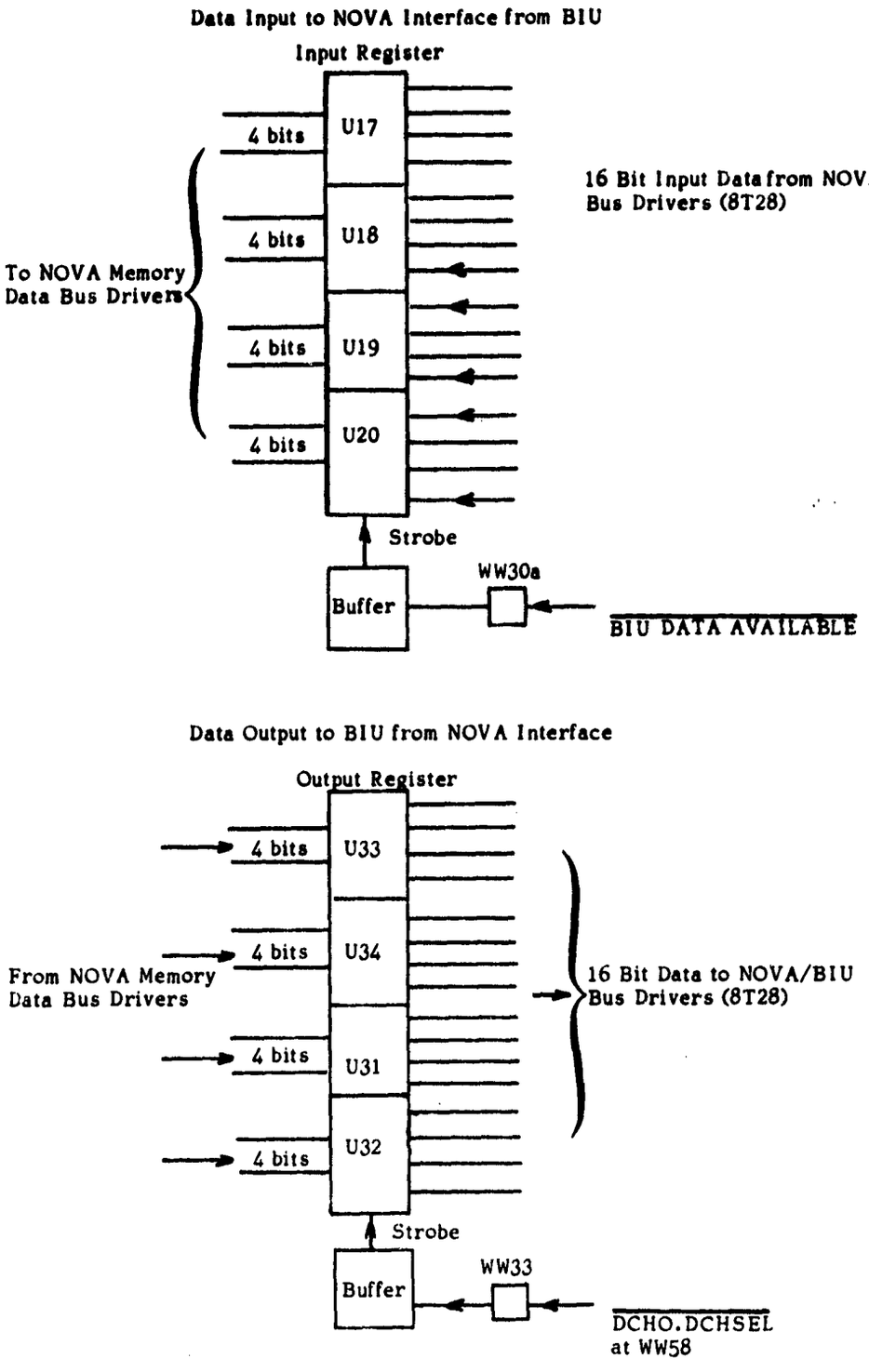


Figure 3.2-4. Data General I/O Registers

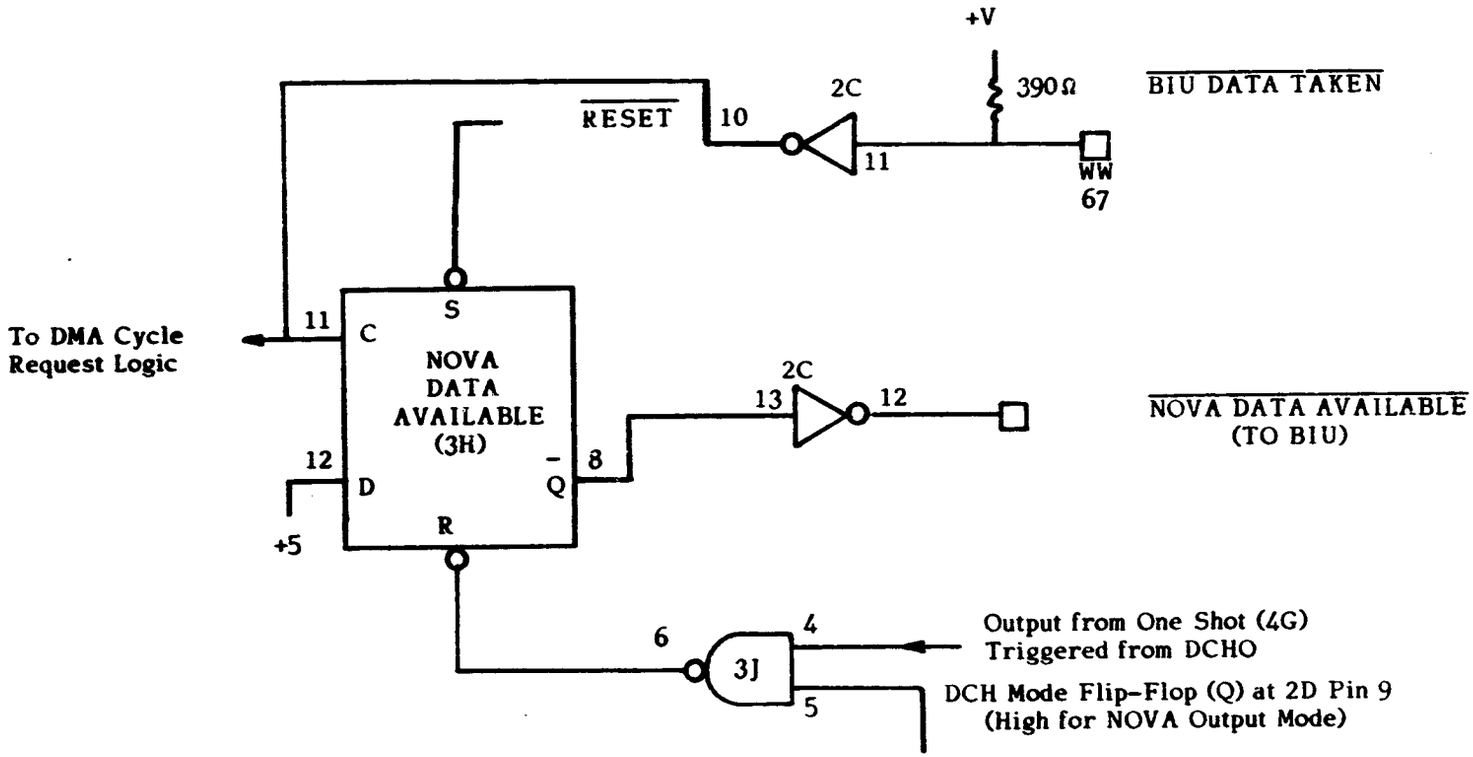


Figure 3.2-5 NOVA Output Handshake Logic

(2) NOVA DMA Write (Data in from BIU). Figure 3.2-6 shows the circuitry involved in this transfer. The handshake signals used are BIU DATA AVAILABLE and NOVA DATA TAKEN. The transfer begins with NOVA DATA TAKEN being high. When the interface is suitably enabled for this NOVA Input Mode, a pulse occurs at inverter 3D pin 3 which causes NOVA DATA TAKEN to transition to low before the BIU does any handshaking. This transition is initially required by the 6522 parallel port in the BIU and is an artifice. Subsequently, the first high to low transition on the BIU DATA AVAILABLE signal resets NOVA DATA TAKEN high, and causes the first DMA cycle request. Subsequently, the NOVA DATA TAKEN flip-flop is reset by the one shot (4G) pulse appearing at 3J pin 1; this pulse is generated by the DMA when the BIU data has been DMA-ed into NOVA memory. A subsequent data transfer occurs for the next transition of BIU DATA AVAILABLE if the Word Counter has not reached zero.

Note that for either NOVA DMA input or output, the respective handshake flip-flops NOVA DATA TAKEN and NOVA DATA AVAILABLE are always initialized high when either of the I/O commands IORST or NIOC is issued by the NOVA.

(C) DMA Cycle Control Logic. Figure 3.2-7 shows the details of this area as taken from the schematic. The DCH START flip-flop (Data Channel Start) is normally reset either by the IORST (I/O Reset) signal, a BIU-generated External Interrupt, or by the previous DMA activity which caused the interface word counter to reach zero.

When the DMA interface is enabled for either NOVA output (DMA read) or NOVA input (DMA write) the DCH START flip-flop will be set through its "set" input. Its Q output (pin 5) feeds a logical "one" to the DCH CYCLE flip-flop, thereby enabling the clock input (on pin 11) to clock the DCH CYCLE flip-flop high.

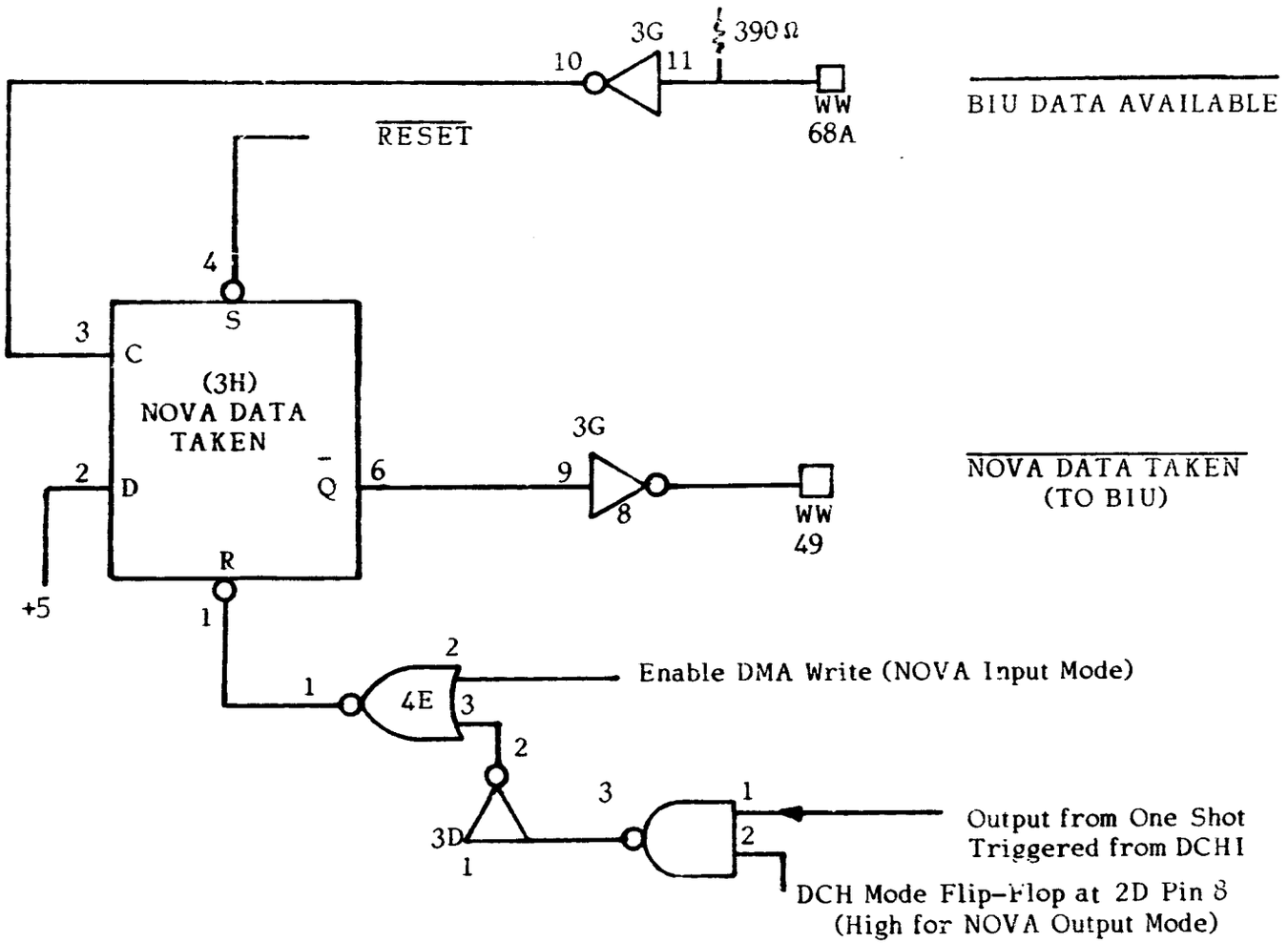


Figure 3.2-6. NOVA Input Handshake Logic

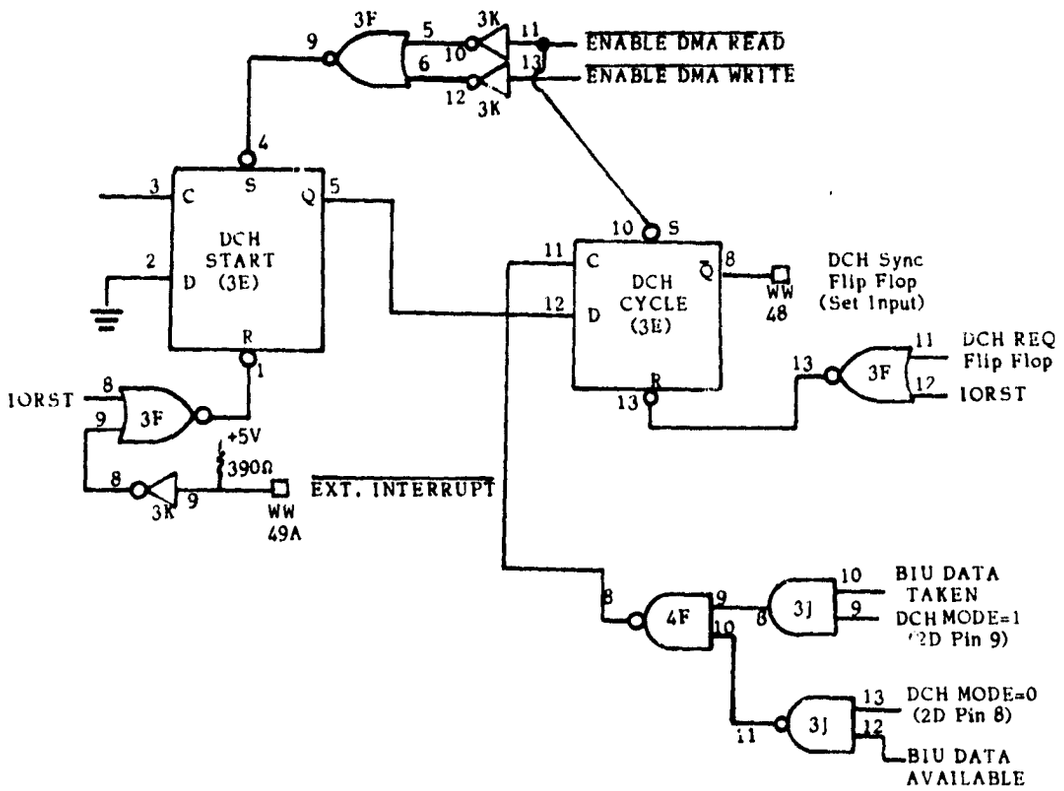


Figure 3.2.7. DMA Cycle Control Logic

When DCH CYCLE flip-flop is set, its $\overline{Q}$ output on pin 8 will be low; this is connected to the Data General SYNC flip-flop on the other side of the board. When the NOVA CPU starts the DMA cycle corresponding to this request, it will turn the Data General DCH REQ flip-flop high, thereby resetting DCH CYCLE flip-flop through its reset input.

The individual DMA cycles occur only when the NOVA and BIU have performed a handshake corresponding to a 16-bit data transfer. In NOVA input mode (NOVA DMA write) the steering logic shown in Figure 3.2-7 allows BIU DATA AVAILABLE to request a DMA cycle, since 3J pin 13 is high (DCH MODE flip-flop reset). Similarly, in NOVA output mode (NOVA DMA read) the steering logic enables BIU DATA TAKEN to request the next DMA cycle.

In the NOVA output mode a DMA cycle must be artifically induced at the block transfer start. This is because BIU DATA TAKEN will only go high if the BIU has actually received data. Therefore, whenever the NOVA output mode is initiated, the signal ENABLE DMA READ sets the DCH CYCLE flip-flop once.

Corresponding to each DMA cycle the Word Count register is incremented once. When this register reaches zero, its most significant bit transitioning from high to low will clock a zero into the DCH Start flip-flop. This will inhibit further DCH CYCLE flip-flop DMA transfer requests.

(D) Interface Board Command Decoder. Figure 3.2-8 shows the segment of logic involved in this function. The NOVA program starts a DMA transfer with a DOA instruction (in which a NOVA accumulation contains the desired command) or a NIOS instruction, after the transfer count and transfer address have been set up by DOC and DOB instructions, respectively. In the command bit pattern, only the least significant four accumulator bits (DATA 12 - DATA 15) are involved. (DATA 12 is the most significant in this "nibble".) Figure 3.2-8 shows that the DOA pulse

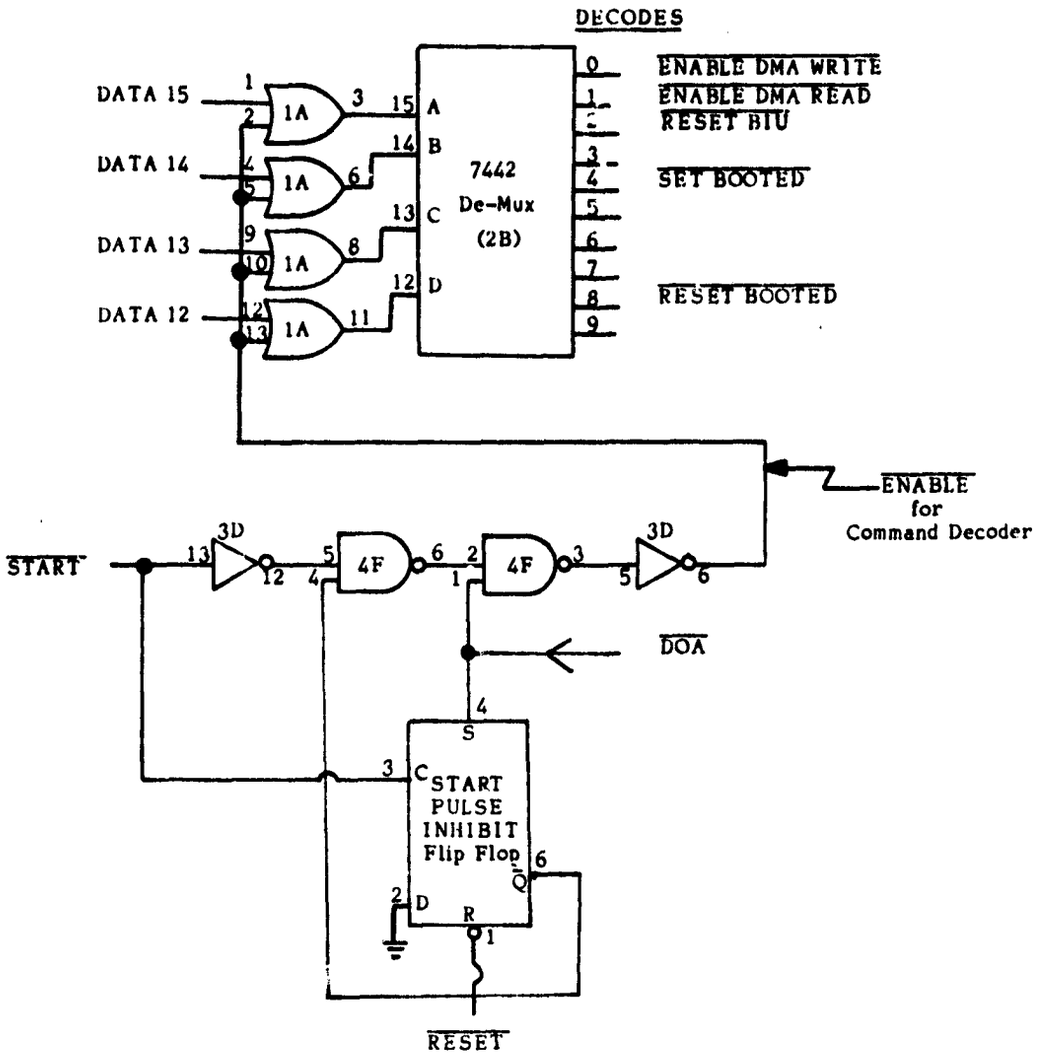


Figure 3.2-8. Interface Board Command Decoder

causes the START PULSE INHIBIT flip-flop to set and also 3D pin 6 to pulse low.

The OR gates that precede the 7442 demultiplexer chip allow the accumulator data to be decoded. The decoding results in one of 10 lines being set (for 4-bit patterns representing numbers above 9, nothing is decoded). Following the departure of the DOA pulse, the decoder is again inhibited by 3D pin 6 going high. The START pulse which follows the DOA in time is effectively blocked from enabling the 7442 by the START PULSE INHIBIT flip-flop. At the trailing edge of START this flip-flop is cleared, thereby restoring original conditions.

In the TMS application, the MEGATEK terminals (of which the NOVA is a part) must be booted over the communications bus. This bootstrapping is accomplished by a 32-word program in NOVA ROM which, among other things, issues an IORST followed by NIOS commands to read in the program to be loaded. The 4040 logic is defined, therefore, so that NIOS pulses the START line discussed above. The NIOS instruction does not use an accumulator, so DATA 12-15 will not be driven and the four bits will appear to the interface as all zero. This will result in activation of the NOVA DMA write (input) mode.

Because the BIU needs to be able to distinguish between times when the NOVA is booted and when it is not, a BOOTED flip-flop (at 2D) is provided. The flip-flop is reset whenever an IORST instruction is executed by the NOVA and can be set by the NOVA under program control (see paragraph 3.3). The TMS terminal program sets the BOOTED flip-flop to true as one of its first operations after the program is started. More detail on the use of the BOOTED flip-flop in BIU operation is given in [5].

(E) Status Latch Logic. When BIU data exists for the NOVA, the BIU must inform the NOVA interface control program whether it is ready to accept NOVA data for network transmission or whether some error con-

dition exists. It accomplishes this by setting an appropriate line active high and pulsing the $\overline{\text{LATCH STATUS}}$ line low while holding this data.

As shown in Figure 3.2-9 there are 8 latch bits on the interface, although only three are presently connected to the BIU and NOVA bus. The NOVA program may read the status bits uninverted if it issues a DIA instruction. Note that there is no lockout between the BIU LATCH STATUS signal and DIA. Therefore, the BIU program must not hold its signal asserted for more than about 1 us if errant status is not to be misread by the program accidentally. Preferably, the NOVA program should read the BIU status only after the BIU has interrupted the NOVA following the change in status. Paragraph 3.3 dealing with programming, includes bit descriptions in the status word.

The fact that LATCH STATUS is active low prevents the interface from being strobed with what would be all ones as status, in the event that the BIU-NOVA cable is disconnected.

(F) Interrupt Capability. Interrupts from the DMA board tie to the NOVA CPU through the logic implemented on the Data General side of the 4040 board; consequently, interrupt issuing is similar to that for other Data General I/O peripherals.

The circuit schematic in Figure 3.2-? shows that the $\overline{\text{EXTERNAL INTERRUPT}}$ line from the BIU is logically tied to the set input of the Done flip-flop; the latter is a Data General logic flip-flop. Provided that the BIU uses a very short pulse here, there will be no problem with a set pulse conflicting with any flip-flop reset.

Tied to the Done flip-flop clock input is the most significant bit of the DMA word counter. When this line transition from a one to a zero (as it will when the word counter is incremented from a large negative number to zero) the clock input of the Done flip-flop sets it to logic "one."

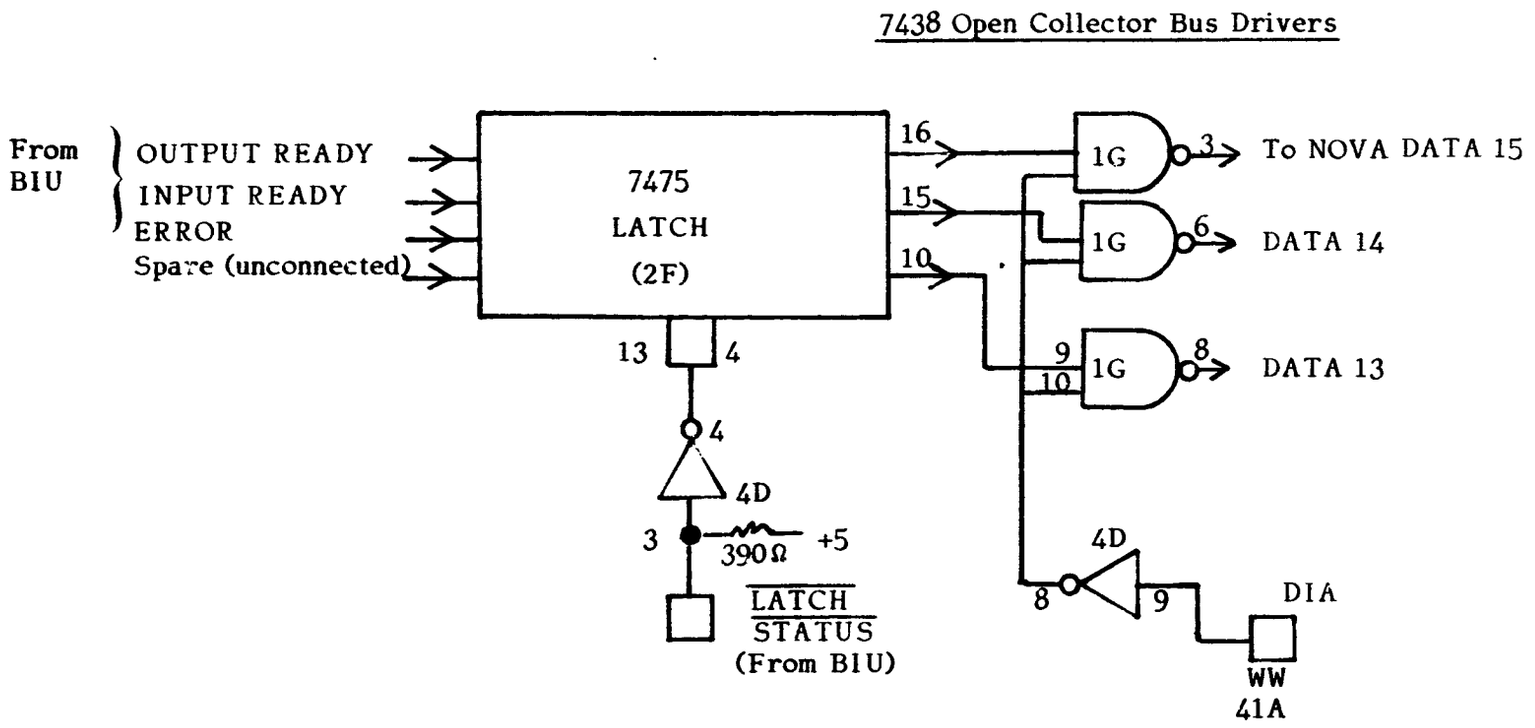


Figure 3.2-9. Station Latch Logic

In either of the two instances above, if the DMA interface board INTERRUPT DISABLE flip-flop has not been set under NOVA program control (by an INTDS instruction or mask bit 1 being set in a MSKO instruction), and if the processor has been enabled for interrupts, the DMA board will cause a NOVA interrupt. In the interrupt service routine an Interrupt Acknowledge (INTA) instruction will yield device code 6 in the accumulator. (This is a non-permanent strapping option.)

The Done flip-flop is cleared in any of the following ways:

1) IORST - Either by program instruction or NOVA front panel reset switch.

2) NIOC instruction or any DMA board instruction with a "C" suffix. (DOAC, DOBC, etc.)

3) Restarting the Interface - This is not totally sufficient to reinitialize the DMA board, though it will clear Done and set Busy.

3.3 DMA Interface Programming

The following commands are implemented:

NOVA Instruction	Accumulator Contents	Function
DOAS	Ø	DMA (NOVA) input [BIU to NOVA transfer]
NIOS	Don't Care	
DOAS	1_8	DMA (NOVA) output [NOVA to BIU transfer]
DOAC	2_8	Reset BIU
DOAC	4_8	Set BOOTED flip-flop
DOAC	10_8	Reset BOOTED flip-flop
DOB	NOVA buffer starting address	Initialize DMA-to-NOVA transfer buffer
DOC	Two's complement of (number of 16-bit words to be transferred plus 1)	Initialize DMA for output from NOVA
DOC	Number of 16-bit words transferred in two's complement	Initialize DMA for input to NOVA
DIA	BIU status: Bit 15 = BIU Output (ready for output from NOVA) 14 = BIU Input Ready 13 = BIU Error	Read BIU status
DIB	NOVA DMA address pointer	Obtain DMA pointer address
DIC	Logically complemented current word count	Obtain DMA word count
MSKO	1_8	Set interrupt disable
INTA	6_8*	Read interrupting device's code (assumed this one)

*No response will be given if this board did not cause an interrupt

The DOA instruction should not be used without either the C or S suffix. If the DOA is issued alone, the DMA interface will hang in an undesirable dormant state.

3.4 NOVA-to-BIU Cabling

The cable to connect the NOVA to the BIU was constructed using twisted wire pairs terminated in an Amphenol 50-pin male connector (part number 57-30500) at the BIU and in two Minicomputer Accessories Co. 102-pin female connectors (part number 922-A) at the NOVA back plane. The two 922-A connectors are identified as A and B in the cable specification shown in Table 3.4-1.

3.5 Installation of NOVA 4040 Interface Board

The 4040 board must be inserted into a convenient slot on the NOVA printed circuit mother board, and it must be verified that the board is tied to the NOVA's interrupt daisy chains. The signals of concern are INTP (the interrupt priority chain) and DCHP (the data channel priority chain).

If there are no unused slots below the position of the 4040 board, the board is automatically attached to the chains. If, however, an unused slot lies below the board, two wires must be installed from the last used board slot to the 4040 board slot. In that case, the following back plane connections should be made:

1. From 4040 back plane pin A96 ($\overline{\text{INTP}}$ In) to back plane pin A95 ($\overline{\text{INTP}}$ Out) of the last board below.
2. From 4040 back plane pin A94 ($\overline{\text{DCHP}}$ In) to back plane pin A93 ($\overline{\text{DCHP}}$ Out) of the last board below.

Table 3.4-I

NOVA-to-BIU Cable Specification

Signal Name	BIU Edge Connector	BIU Amphenol Connector		NOVA Backplane Connector	
		Signal	Associated Ground	Signal	Associated Ground
DATA 0 (MSB)	67	43	48	B34	B92
DATA 1	68	42	47	B36	B92
DATA 2	69	41	47	B38	B92
DATA 3	70	40	47	B40	B92
DATA 4	71	39	47	B27	B50
DATA 5	72	38	47	B31	B50
DATA 6	73	37	46	B49	B100
DATA 7	74	36	46	B51	B100
DATA 8	80	33	46	A71	A99
DATA 9	81	32	46	A67	A33
DATA 10	82	31	46	A61	A33
DATA 11	83	30	25	A63	A33
DATA 12	84	29	25	A47	A2
DATA 13	85	28	25	A49	A2
DATA 14	86	27	25	A59	A34
DATA 15 (LSB)	87	26	25	A57	A34
$\overline{\text{NOVA DATA AVAIL}}$	75	34	48	A79	A100
$\overline{\text{BIU DATA TAKEN}}$	76	35	48	A81	A100
$\overline{\text{BIU DATA AVAIL}}$	88	44	48	A83	A100
$\overline{\text{NOVA DATA TAKEN}}$	89	45	48	A73	A99
$\overline{\text{NOVA DONE}}$	51	17	49	B23	B2
$\overline{\text{NOVA BUSY}}$	50	18	49	B25	B50
$\overline{\text{BOOTED}}$	49	19	49	B53	B99
$\overline{\text{BIU RESET}}$	57	24	49	B19	B2
BIU ERROR	44	6	49	B11	B1
BIU OUTPUT READY	43	7	50	B15	B1
BIU INPUT READY	42	8	50	B13	B1
$\overline{\text{EXT INTERRUPT}}$	41	9	50	A75	A99
$\overline{\text{LATCH STATUS}}$	118	10	50	B52	B99
Cable Shield	-	1	-	-	-

The installation of the NOVA-to-BIU cable requires that back plane connector A be placed on the A side of the back plane (left side, as one faces the back plane) and B on the B side of the back plane. Each connector should be inserted so that its left side is aligned with the first back plane pin in the respective group; one unused connector position will then extend beyond the right-hand edge of the back plane pin group.

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