SPECTROLAB

FINAL TECHNICAL PROGRESS REPORT

ON THE

DEVELOPMENT OF IMPROVED WRAPAROUND CONTACTS FOR SILICON SOLAR CELLS

NAS3-20065

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ABSTRACT

A developmental process for fabricating 2 X 4 cm back surface field silicon solar cells featuring wraparound contacts and screen printed dielectric isolation is described. This process evolved out of experimental investigations which were designed to determine if the wraparound dielectric process, developed under NASA contract NAS3-20029, could be applied to shallow junction silicon solar cells using vacuum deposited metal contacts in a wraparound configuration. The process was then used to fabricate a number of cells for evaluation and study, as well as to establish the validity of the process sequence. While a number of cells exhibiting relatively good conversion efficiencies were produced, nearly all had low I-V curve factors for the level of efficiencies attained. Cells with conversion efficiencies of more than 15% (AMO and 25^{o}C) had fill factors of only 0.76. Evidence as to the cause of this has not been conclusive, but is most probably linked to isolation failure in the wraparound dielectric and associated shunting problems.

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SUMMARY

This program, initially intended to demonstrate and evaluate various techniques for applying wraparound contacts to shallow junction solar cells, excluding screen printing methods, was redirected after an exploratory investigation of screen printed wraparound dielectrics. The modified program was designed to develop a processing sequence for fabricating 2 x 4 cm back surface field, shallow junction solar cells with vacuum deposited metallization and wraparound dielectric isolation applied by screen printing.

The exploratory investigations were successful in producing 2 X 2 cm cells having greater than 14% conversion efficiencies at 25°C and AMO illumination. A process sequence was developed and a final cell design for 2 X 4 cm cells was evolved. A fabrication phase then followed during which seven lots of cells were processed and evaluated. The first six lots produced 46 cells with conversion efficiencies higher than 13.5% with some cells higher than 15%. The seventh lot produced 25 cells greater than 13.5%. Analysis of the process used indicated a yield of cells into electrical test of 68.9%.

While these cells appear promising, all had electrical characteristics with relatively low I-V curve fill factors. The major problem encountered appeared to be associated with shunting effects caused by inadequate isolation, although this has not been established with total certainty.

Additional lots, fabricated to provide additional cells for experimentation and data for evaluating the process, failed to accomplish these purposes.

1.0. INTRODUCTION

1.1. Background

This program was initially intended to demonstrate and evaluate various techniques for applying wraparound contacts to shallow junction solar cells. These cells were to have diffused junctions having sheet resistance values of at least 120 ohms per square, and the wraparound methods to be studied were to be suitable for use on high efficiency solar cells having a base resistivity of one ohm-cm. The metallization was to be capable of producing gridline widths of approximately 0.05 mm, and were to utilize typical collector bars of about 0.5 mm, dimensions that are commonly used for high efficiency silicon solar cells.

Four main techniques were chosen to be of potential interest. These were: 1) thin wraparound insulating layers, 2) thick wraparound insulating layers, 3) deep edge junctions, and 4) alloyed wraparound contacts. Screen printing techniques for applying the wraparound insulating layers were specifically excluded. Screening tests were to be devised and performed, using rudimentary cell structures which were not necessarily complete solar cells in order to establish the most promising approaches. After having chosen the best of the methods developed, this method was to be used to fabricate a limited number of solar cells which were then to be tested and evaluated for electrical performance and tolerance to environmental conditions using tests in accordance with the standard practices used for the space qualification of solar cells.

At the time Spectrolab started work on this program development had just been completed of a process sequence for the automated

fabrication of back surface field silicon solar cells with screen printed wraparound contacts using screen printed dielectric isolation. This work, under contract NAS3-20029, had succeeded in producing very promising wraparound contact cells. The use of fired-on screen printed contacts, however, required that the cells have relatively deep junctions in order to avoid shunting problems brought on by the interaction between the contact materials and the silicon during the firing cycle.

It appeared logical to perform a few investigative experiments with screen printed wraparound dielectric isolation to ascertain what conversion efficiencies might be achieved with shallow junction structures and fine resolution vacuum deposited metal contacts. Permission for performing an exploratory investigation was requested and received from the NASA Program Manager. Spectrolab was directed to cease the activities under the work requirements of NAS3-20065, and for a period of six weeks evaluate the merits of solar cells having screen printed dielectric isolation and wraparound evaporated metallizations. The results of this effort were promising enough to allow the investigative period to be extended for another six weeks.

The results of these preliminary investigations were sufficiently promising that Spectrolab recommended that NAS3-20065 be redirected. Using improvised masks for the wraparound contacts it had been possible to make cells that generally exhibited good conversion efficiencies. One 2 X 2 cm cell had a maximum power output of 83 milliwatts at 25^{o}C under AMO illumination. It was noted that nearly all cells had relatively low curve fill factors for the I-V curves. This was attributed to high series resistance, possibly due to residual masking material left on the cells after an HF oxide removal step performed after glassing and prior to metallization.

The contract was then modified, and Spectrolab was directed to optimize the processes, parameters, and sequences for fabrica-

ting silicon solar cells with vacuum deposited wraparound contacts over a screen printed insulator. The baseline cell was to be a 2 X 4 cm, 0.2 mm thick, ten ohm-cm, texturized, back surface field cell. Goals of a 14% AMO minimum conversion efficiency and a 70% process yield were established. Once a satisfactory process sequence had been developed and established, a cell design was to be evolved and submitted to NASA for approval. After approval, a minimum of 250 cells were to be fabricated and tested.

1.2. Redirected Effort

Most of the process optimization and development was directed towards the screen printed wraparound dielectric insulating layers. Commercially available materials were utilized and modified processing was devised for applying them in a solar cell fabrication sequence. Because of the presence of such layers, some of the conventional cell processes had to be modified to accomodate them. While most of the cell structure was conventional, it was necessary to introduce additional masking steps to permit conventional operations, such as edge etching, to be carried out without damage to the dielectric. It was necessary to develop techniques for performing vacuum metallization for wraparound contacts. These techniques had to be revised and modified part way through the program because of changes in the availability of equipment.

The process sequence had evolved sufficiently so that when a design review was held a group of cells was delivered to the NASA Lewis Research Center that were generally capable of conversion efficiencies greater than 13% at 25^{o}C and AMO. The I-V curve fill factors, however, were still relatively low for this level of efficiency, and were generally between 0.70 and 0.75. The poor fill factors had initially been ascribed to

high series resistance, but measurements of R_{series} gave values that did not appear sufficiently high to be a problem. Approval was given to go ahead with the fabrication phase of the program using the process sequence that had been developed.

A series of lots were then processed according to the approved process sequence. While process yields were not completely satisfactory, they were not out-of-the-ordinary for a pilot fabrication effort that lacked the maturity of a production process. Part way through this phase a change was made to use a different dielectric material. This was brought about by the discovery of microscopic cracking in the isolation layers during and after the metallizations. The material that was substituted also exhibited some microcracks, but not nearly as often, or as severe, as the original dielectric.

Additional funding was made available for fabricating several additional lots of cells. This was because the initial funding of the program was depleted before reliable yield data had been obtained and also because of the midstream change in the dielectric material that was used. The purchase of replacement evaporation masks for the metallizations was not included. The additional lots yielded cells that were of poor quality, both electrically and mechanically.

The overall results of the program were to develop a process sequence that produced wraparound contact cells with tantalizingly high performance, but with less than satisfactory fill factors. This continues to be a problem with this cell design, and is most probably due to deficiencies in the wraparound dielectric layers.

2.0. TECHNICAL DISCUSSION

2.1. Exploratory Investigations

With the permission of the NASA Program Manager a series of exploratory investigations were undertaken to ascertain whether it would be worth-while to combine screen printed dielectric isolation structures with vacuum deposited metallization and shallow junctions. Use of evaporated metal contacts would permit the use of shallow junctions. Under contract NAS3-20029 a process had been developed to produce wraparound contact cells with screen printed dielectric isolation and contacts. Because of the penetration of the screen printed contact material into the silicon during the firing cycle, junctions had to be relatively deep, which gave a reduction in cell conversion efficiency.

These preliminary experiments were to be of limited scope, and were confined to a period of six weeks. They were aimed at establishing whether a viable process sequence might be developed to take advantage of high resolution vacuum deposited contacts and shallow junctions without encountering serious problems in a wraparound dielectric structure. It was not known whether shallow junctions would be adversely affected by unknown impurities in the dielectric paste when it was fired on. It was also possible that the evaporated metal would penetrate any porosity in the isolation layer, thus degrading the electrical behavior. In spite of the cell efficiencies attained in NAS3-20029, there were some doubts as to the feasability of screen printing cell structures with shallow junctions without mechanical damage, particularly for texturized front surfaces. There was also speculation as to whether a single layer of dielectric would be adequate, or whether a double layer would be required.

The initial experiments were therefore designed to establish the feasability of screen printing a dielectric layer on a texturized shallow junction cell, whether a single or a double layer would be required to give the necessary electrical isolation for vacuum metallizations, and whether such contacts could be applied in a wraparound configuration around a glassed edge. Because of the short time available, investigations were aimed at showing promise and feasability, rather than towards developing a final process sequence.

2.1.1. Wraparound Dielectric Structures

Initial experiments quickly established that a dielectric paste could be screen printed onto the edge of a cell and over a portion of the back surface to accomodate a gridline contact pad. Evaporated dots of titanium-silver indicated that isolation required a double layer of the dielectric, and that such dots adhered well to the glass when tested with Scotch brand #600 tape. The dielectric also appeared to adhere well to the silicon. Electrically about 20% of the evaporated metal dots gave less than perfect isolation, with varying degrees of shunting present in the dots that failed.

With this relatively low, but finite, probability of good electrical isolation, a small group of cells were fabricated in the wraparound configuration. Titanium-silver was used for the front gridlines which were wrapped around the glassed edge of the cells. The evaporation masks were improvised from tooling that was immediately at hand. The cell structure was a relatively deep (36 ohms per square) n-diffused junction on a 0.25 mm thick, 10 ohm-cm, p-type base. A texturized front surface was used, and an aluminum paste back surface field layer was included. The backs of the cells were covered with the alloyed-on aluminum metal which was left intact.

Several of the completed cells were found to have sufficient electrical isolation to permit testing under a solar simulator and I-V curves were obtained. These 2 X 2 cm cells were found to have short circuit currents of about 150 mA, which appeared quite promising considering the depth of the junction, the lack of any AR coating, and the relatively wide gridlines (0.13 mm). All of the I-V curves displayed a degraded curve shape, which was attributed to high series resistance.

Because of the presence of the dielectric layer none of the above cells had been stripped of the oxide layer on the front surface prior to applying the front contact metal. It was soon established that the dielectric layer could not withstand treatment with hydrofluoric acid, normally done immediately before metallization. An ink masking technique was devised to protect the glass during an HF treatment. This masking was then removed before contacting.

Microscopic examination of the dielectric also indicated the presence of some cracking in the layer. This was more evident after the samples had been metallized than before. It was not known whether this was due to differences in the thermal expansion coefficients between the glass and the silicon, or whether the handling during masking, etching, mask removal and evaporation had mechanically damaged the dielectric. Microscopic examination of cross sections of the wrapped edges of the cells revealed that the dielectric was quite thick along the edge of the silicon and that a marked "bead" had formed. The dielectric also appeared to have some voids and a more or less porous structure. It was not known whether this was due to air trapped in the paste during the screen printing operation, or whether the bubbles were formed by improper firing methods.

An attempt was then made to limit the amount of dielectric paste at the wraparound edge. Edge sanding was used to assure

a rectangular silicon edge. Cells were printed using a dummy silicon cell placed on the printing post close to, but not touching the edge to be wrapped. The dielectric paste was thus forced down into the crevice in a quantity that could be controlled by the width of the crevice. This technique had only limited success. The thickness and size of the glass bead could be reduced, but control was poor, and in the worst cases the dielectric assumed a saddle-shaped cross section with the glass becoming very thin along the centerline of the die. In some cases bare silicon could be seen along this centerline.

The addition of a fifteen minute vacuum treatment at forepump pressure and a slightly higher firing temperature produced dielectric layers that looked quite good. Electrical checks with evaporated metal dots gave about 75% high resistance and the cross sections appeared uniform. The bead was relatively thin, and there were only scattered bubbles. A few cracks were found, but these did not appear with high enough frequency to offer a serious problem.

2.1.2. Experimental Cell Fabrication

At this point it was decided to concentrate on fabricating actual cells, carrying the processing through contacting and electrical test. While the wraparound dielectric layer was not satisfactory, the process appeared to be sufficiently improved to permit obtaining some actual solar cells for evaluation

2 X 2 cm cells were then fabricated using the crevice technique for printing the dielectric and including a vacuum pull prior to drying and firing. Chromium-silver wraparound gridlines were evaporated using improvised masks and tooling. The group was then divided into two parts, with one being ink masked and

oxide stripped with HF prior to contacting, while the other cells omitted this process. All of the cells not treated with HF were found to have excessive series resistance. The treated cells yielded two-thirds with peak power values greater than 70 milliwatts at 25°C and AMO. These cells were then given a standard tantalum pentoxide AR coating, which increased the short circuit currents to about 170 mA, but all still had I-V curves with relatively low fill factors.

An experiment was then performed to establish whether the heating during the dielectric firing was causing any problems. 2 X .2 cm cells without any dielectric were heated along with dielectrically isolated cells through the glass firing cycle. These cells were then given conventional vacuum deposited contacts, putting non-wraparound contacts on both glassed and non glassed cells. The cells, when tested, gave essentially the same performance, indicating that the firing cycle was not a problem and the dielectric was not detrimental.

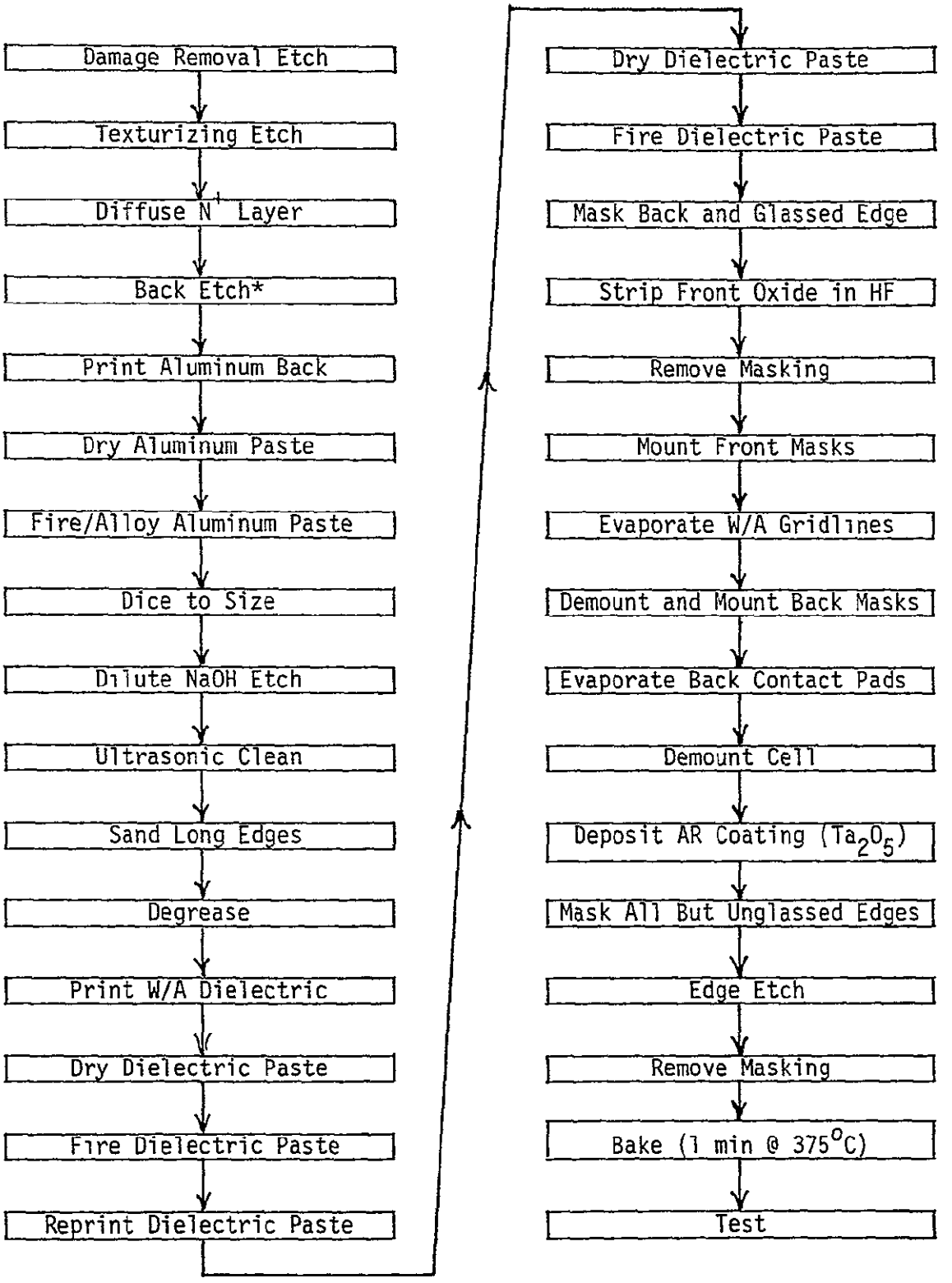
Mixed evidence was then found concerning the suspected high series resistance blamed for the poor curve shape that had been found for all wraparound cells made. A wraparound cell was tested, then masked and a front collector bar evaporated across the ends of the gridlines. The dielectric glassed edge was then removed with a dicing saw. This produced a marked improvement of the I-V curve shape when the cell was tested as a conventional cell. This experiment was then repeated, dicing off the fired on dielectric edge and contacting the cells conventionally. In this case the cells still exhibited poor curve shapes. Measurements of the series resistance of wraparound cells gave values of about 0.07 ohm, which was low enough to not produce the degradation of curve shape that was being observed. Series resistance thus appeared to be less a cause than shunting effects due to inadequate isolation.

Up to this point all of the cells fabricated had had quite deep junctions. A new group was then processed with relatively shallow junctions (sheet resistance of 70 - 75 ohms/square). These were processed using a screen printed dielectric that fired at a slightly lower temperature, namely Transene #1000. The dielectric material used previously, Thick Film Systems #1126RCB, which had been used on NAS3-20029, was fired at 650°C, while the Transene material was fired at 575°C. These cells were metallized using narrower gridlines and chromium-silver contact metallizations. Of eight cells surviving from the twelve starts, the lowest 2 X 2 cm cell gave a peak power output of about 76 mW, while the best gave about 78 mW.

It thus appeared that this non-optimized process was capable of producing cells with conversion efficiencies of more than 14%. One cell had been made with an efficiency of more than 15%. While the curve fill factors were lower than desirable, cell efficiencies were still relatively high, and additional improvements in the processing might well raise fill factors to satisfactory levels. These data were then presented to the NASA Program Manager, along with a recommendation for redirection of the program effort.

2.2. Baseline Process

The baseline process sequence that was initially used was quite similar to that developed under contract NAS3-20029. Since the contact metallization was to be vacuum deposited the diffusion program was modified to produce shallow junctions with sheet resistance levels ranging from 75 to 100 ohms/square. Also, since the contact metallizations did not require a high temperature firing cycle, it was possible to consider the use of dielectric materials that fired at somewhat lower temperatures as there would be no subsequent firing where the dielectric might be remelted. A block diagram of the process sequence is shown in Figure 1.



* Later eliminated

Figure 1 Block Diagram of Baseline Process

2.2.1. Starting Material and Surface Preparation

The silicon material used was 10 ohm-cm, p-type wafers having a diameter of 51 mm and thicknesses from 0.35 to 0.45 mm. The wafers are first etched in a 30% sodium hydroxide solution at about 100°C to remove mechanical damage from the wafering saws and to bring them nearly down to the desired final thickness. A warm, dilute solution of sodium hydroxide and isopropyl alcohol is then used to obtain the final thickness of 0.20 mm and to produce the surface texturization. This orientation dependant etch is characterized by a rather slow etch rate, allowing for good control of the final thickness tolerances.

2.2.2. Junction Formation

The wafers are then diffused in phosphine gas at 850°C to obtain a sheet resistance of about 75 ohms/sq. They are then back etched in an acid etch to remove the diffused N^+ layer from the backs prior to forming the P^+back surface field layer. A water curtain system was used to confine the etch to only the back surface of the wafers.

Formation of the P^+ layer for the back surface field utilizes the process developed under contract NAS3-20029. A layer of aluminum paste is screen printed onto the etched back of the wafer, dried, and then fired. The firing is of short duration at a sufficiently high temperature to assure the formation of a molten silicon-aluminum eutectic layer at the peak temperature attained, and a thin silicon regrowth layer on cooling that is saturated with aluminum. The actual firing times and temperatures used will be functions of the silicon base resistivity, the thermal mass of the wafers themselves, and the thermal mass of the boat used. Generally for the low mass boat used, this wafer size, and this resistivity, it was established that a firing time of about 20 seconds at a tube temperature of 875°C

was optimum for producing a back surface field that gave the greatest enhancement of short circuit current and open circuit voltage.

When the wafers are cooled rapidly the silicon regrowth layer is quite thin, and the $P-P^+$ junction formed will be very abrupt. The eutectic, on cooling, forms primarily a layer of metallic aluminum containing tiny crystallites of silicon. This layer is left in place to serve as a low resistance back contact. It may, however, be etched away in hot hydrochloric acid exposing the polycrystalline silicon regrowth layer. This may then be contacted by conventional metallization techniques.

2.2.3. Dielectric Application

The round wafers are then diced to size (in this case 2 X 4 cm) on a conventional high speed dicing saw. The dice are then prepared for the dielectric isolation deposition by removing the aluminum oxide powder formed during the alloy firing cycle. This is done by a short duration etch in 1% sodium hydroxide at about $85^{o}C$ which loosens the powder, and then a short ultrasonic agitation in water, which leaves a bright metallic aluminum surface. The long edges of the cells are then sanded to provide a rectangular edge for the wraparound process. After degreasing, the cells are ready for screen printing the dielectric paste.

Two layers of dielectric isolation are necessary to assure minimal pinhole effects. The dielectric may be applied using a print-dry-print-dry-fire cycle, which requires only one high temperature step. Or a print-dry-fire-print-dry-fire schedule may be used. The latter was used throughout this program, since some early experiments indicated that the probability of pinhole problems seemed to be somewhat less for that cycle.

The same overprint technique developed under contract NAS3-20029 was used. Drying was done in air in a mechanical convection

oven at 150°C for a period of 10 minutes. The firing was done in a tube furnace at the temperature recommended by the paste manufacturer for 10 minutes. A high thermal mass boat was used to support the wafers during firing to minimize thermal shock during the cooling cycle. The tube firing, not normally used for dielectric pastes, had to be utilized because of the lack of availability of the belt furnace used during contract NAS3-20029.

2.2.4. Final Fabrication Operations

Spray-on ink masking is then used to protect the back of the cell. The dielectric wraparound edge is coated in the ink resist by dipping the edge into a freshly sprayed layer of the ink. The masking is then baked to dryness at 85°C for ten minutes and the cells are etched in a 10% hydrofluoric acid solution for one minute to remove any oxides from the front surfaces that may have formed during earlier steps in the processing. After washing, the cells are then cleaned in solvents and ultrasonic baths to remove the masking ink. This procedure assures that the fronts of the cells are as free of oxides as possible when the contact metallization is applied.

The cells are then mounted with the gridline masks in such a way that the gridlines extend over the wraparound dielectric edge. By locating the evaporation fixture at an angle in the high vacuum coater, the deposited gridlines will thus achieve the wraparound configuration. The silver portion of the chromium-palladium-silver metallization is evaporated for about twice the normal time to compensate for the angle of incidence used, which would otherwise be reduced in thickness. Once the gridlines have been deposited the front gridline masks are demounted and the cell is reversed and covered with the masks for depositing the back contact pads, which are also chromium-palladium-silver evaporated onto the cells.

An antireflection coating of tantalum pentoxide is then evapor-

ated onto the front surfaces of the cells. The cells are then spray coated, front and back, with an etch resist ink, and then the glassed edge is again dipped into a freshly sprayed ink layer. After the resist is dried, the three non-glassed edges of the cells are cleaned to remove the ink masking and the cells are given a short edge etch in an acid solution. After the masking has been removed, the cells are then given a short bake at 375°C. The cells are now ready for testing.

2.3. Developmental Studies

2.3.1. Wraparound Dielectrics

The screen printed dielectric isolation used on a previous contract (NAS3-20029) was specifically chosen to produce adequate isolation for screen printed wraparound contact systems. The glass used, Thick Film Systems #1126RCB, required firing at somewhat elevated temperatures in the neighborhood of 650°C, and was intentionally chosen so that it would remain solid during subsequent firings of the screen printed metallizations. This program, utilizing vacuum deposited metal contact systems, permits the use of dielectric pastes having lower firing temperatures. This should be a decided advantage when used on cell structures having P^+ back surface field layers where the aluminum is left in place, since the dielectric can be fired without remelting the aluminum-silicon interface. The aluminum-silicon eutectic temperature is about 577°C.

Early in the program Transene #1000 dielectric crossover paste was tried, since the manufacturer's recommended firing temperature is 500° to 575°C. These early efforts resulted in cells that exhibited AMO conversion efficiencies higher then 14% at 25°C in some cases, however the I-V curve fill factors were seldom higher then 0.75. This was ascribed to high series resistance, although measurements of this parameter usually gave values of 0.1 ohm or less. Thus it began to appear that shunting was the major problem.

The presence of random pinholes, present even after printing a second dielectric layer, was a possible cause of such shunting. Therefore a series of tests were performed to establish the relative merits of several types of paste. These experiments were also used to establish the optimal printing, drying, and firing procedures for each paste type. Because of the lack of a conveyor belt furnace, as had been used on NAS3-20029, it was necessary that all dielectric paste firing be conducted in a diffusion tube furnace.

Firing thick film pastes in a tube furnace offered some formidable problems, since such furnaces have temperature profiles that make it nearly impossible to follow the time-temperture firing schedules recommended by the manufacturers. The steep fall-off in the temperature profile at the end of the hot zone make it difficult to achieve a slow ramp-up in temperature at the start of the cycle, and also make it impossible to provide a slow cool-down procedure. Even when the material is withdrawn very slowly the dielectric/aluminum/silicon layered system is subjected to a sizable thermal shock, just in the process of removing the samples from the furnace.

Attempts were made to minimize the thermal shock by using very slow withdrawal rates, by the use of boats having very high thermal mass, and by letting the boat sit in the cooler entry to the furnace tube for a time before bringing it out into room temperature surroundings. Attempts were also made to raise and lower the temperature of the entire furnace very slowly, but this made the firing cycle so long as to be impractical, and was not seriously considered as a useful procedure.

A series of dielectric paste evaluations were made using 2 X 6 cm rudimentary cell structures. These were silicon blanks that had been etched, printed with aluminum paste, alloy fired, and then cleaned, to give simulated cell backs essentially the same as those used for actual cells. Rectangular test patches of the different dielectrics were screen printed on these structures

and then dried and fired according to various schedules. Both single and double layers were evaluated. A series of chromium-silver dots measuring 3 mm in diameter were then evaporated onto the sample structure. A sketch of the test structure is shown in Figure 2.

The dielectric pastes initially investigated were Transene #1000, Thick Film Systems #1126RCB, and Thick Film Systems #1141. Later Transene #780 and #980 were tested. The first tests indicated that about 60% of the test contacts on Transene #1000 had isolation greater than 10 megohms. TFS #1126RCB, which had to be fired at a temperature higher than the aluminum-silicon eutectic temperature, gave only a few dots with measurable isolation. 80% of the test dots gave isolation for TFS #1141, which also appeared to have the least number of pinholes and microcracks when examined visually.

Work was therefore concentrated on the lower firing Transene #1000 and TFS #1141 materials. A workable procedure was evolved that gave dielectric layers exhibiting minimal pinholes and microcracks. The Transene #1000 yielded a uniform, matte surface without visible flaws. The TFS #1141 after firing was somewhat more transparent, had a glossy surface, but also had a surface covered with a mosaic of fine microcracks. While these cracks did not seem to extend completely through the layer, they were considered to be a source of potential problems, and thus the effort was confined to the Transene material.

A sample of Owens-Illinois dielectric paste was received from the NASA Program Manager, and was also tested during these experiments. This material required a relatively high firing temperature of 750^{o}C. The limited amount of material available gave layers with high gloss, glassy surfaces. These layers were almost transparent, but were filled with tiny bubbles. Insufficient material was available for developing an optimized firing procedure. It was found that this material gave markedly less cell bowing, indicating that it was a much better match for the silicon in terms of thermal expansion.

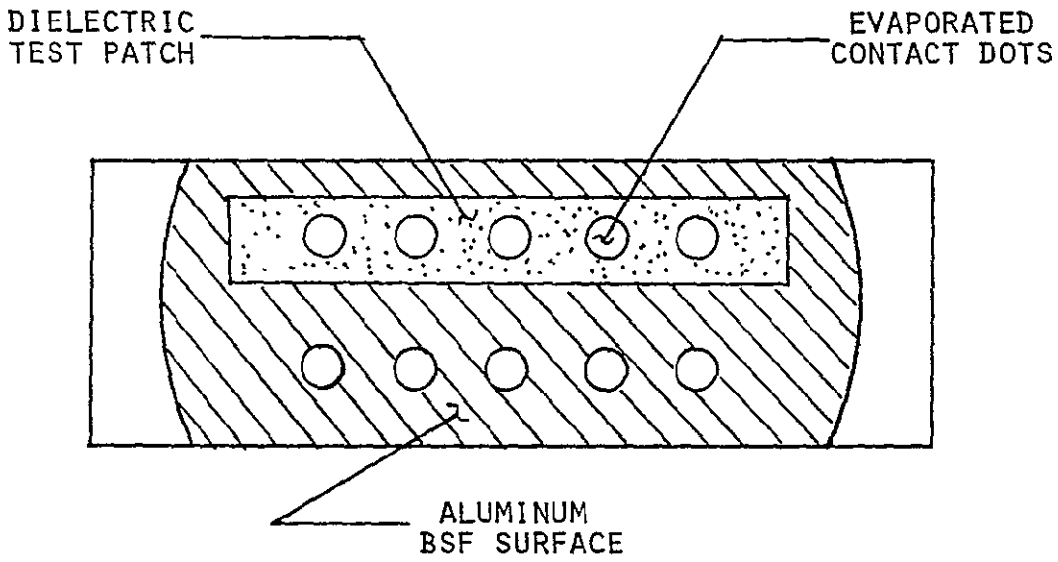


Figure 2

Test Structure for Evaluating
Dielectric Pastes

Actual cells were then made from all three types of dielectric wraparound materials. In the case of the Owens-Illinois material it was necessary to etch away all of the aluminum from the backs of the cells and replace it with a layer of evaporated titanium-silver which could withstand the higher glass firing temperature. A control group of conventional cells was made at the same time with the same lot of NPP^{+} silicon material but with no wraparound contact configuration. The control cells were found to have an average efficiency of 13.5% at 25°C under AMO illumination and gave fill factors of 0.77. All of the wraparound cells exhibited considerable shunting. These cells had been cropped to a 2 X 2 cm dimension after metallizing. A microscopic examination revealed visible damage to the dielectric layers where they had been cropped. It was thus necessary to provide printing screens and evaporation masks that would eliminate the need for any cropping after metallization.

Two additional materials from Transene were also investigated. These were #780, which had a firing temperature of 375° to 400°C, and #980, with a firing temperature of 450°to 475°C. Both of these materials were tested because of the desirable lower firing temperatures. The tests indicated that both had serious microcracking problems and gave indications of a thermal expansion mismatch with silicon when fired in the tube furnace.

Generally it was found that the glasses that had the lower firing temperatures produced the greatest mismatch in thermal expansion. The higher firing materials give much less cell bowing, but generate serious problems in the necessary thermal treatment of the silicon, probably due to detrimental effects on the minority carrier diffusion length. The presence of a back layer of metallic aluminum also limits what can be done in terms of the maximum firing temperature that can be used.

It is possible to screen print a second layer of dielectric after the first layer has been dried, but not fired. The two layers can then be fired together to produce a single isolation layer. There is a possibility of damaging the first layer, however when printing

the second. Therefore it was decided to use a print-dry-fire-print-dry-fire cycle for applying the dielectric wraparound layer.

Using Transene #1000 dielectric, a group of cells was then fabricated which averaged about 13.5% efficiency at AMO and 25°C, but with an average fill factor of 0.71. These cells had the 2 X 4 cm dimension and had average V_{oc}'s of 604 mV and I_{sc}'s of 333 mA. When tested at the NASA - Lewis Research Center the resulting data gave maximum power values of about 7% less than that found by Spectrolab. Open circuit voltages were about 2% lower, but the fill factors were roughly 1% higher.

With these results, it was recommended that the Transene #1000 material be used as the dielectric for the following cell fabrication phase of the program.

2.3.2. Back Surface Field P^+ Layer Development

The process used for generating a P^+ layer on the wafer backs was essentially identical with that used under contract NAS3-20029. A layer of aluminum paste was screen printed on the back of the wafer. This was dried for 15 minutes at 250°C in air and then fired to form an alloyed layer with a very thin regrowth layer that was doped to saturation with aluminum.

Initially the baseline process included a back etch step after diffusion prior to printing the aluminum paste. As the program developed it was decided to try eliminating the back etch step and to print the aluminum paste directly onto the diffused wafer backs. An HF dip was used to remove any oxide layers formed during diffusion to assure uniform alloying. This procedure proved to be successful, and back etching was dropped from the process sequence.

The aluminum paste used contained no glass frit, which appears to inhibit the alloying process. Initially the paste was formulated in-house, but it was later found that Engelhard #A3484 Squeegee

Alumalloy Ink was satisfactory. One problem during the alloying appeared to be associated with non-uniform wetting of the silicon at the start of the alloy process. Some lots would be fired from time to time that exhibited random lumps in the aluminum back layer. It was reasoned that these lumps were locations where the aluminum-silicon eutectic formed first, before the rest of the wafer back became molten. It was found that the addition of 2% aluminum oxide powder to the aluminum paste improved the uniformity of the sheet alloying process, and eliminated nearly all of these lumps.

Several factors were found that had marked effects in the alloying process as carried out in a tube furnace. The above mentioned addition of aluminum oxide powder minimized the formation of lumps, possibly by inhibiting material flow in the molten eutectic and keeping the alloying action localized. It was also found helpful to place the wafers horizontally during the alloying cycle to avoid gravitation effects. Low mass quartz boats were designed and used to assure that the regrowth layer was relatively thin and to minimize the length of the cooling cycle to make the $P\text{-}P^{+}$ junction as abrupt as possible.

A "spike" heating cycle was used, with the wafers being inserted and withdrawn from the furnace in a matter of a few seconds. The temperature attained by the wafers was somewhat less than that of the furnace, depending on the length of the cycle. Since the penetration of the alloy into the silicon, and the thickness of the regrowth layer is a function of the highest temperature attained, it was necessary to establish the firing time and temperature by experiment. A series of wafers having the same thermal mass, base resistivity, and thickness of aluminum paste were fired at different temperatures for times ranging from 10 to 40 seconds. It was found that the short circuit current would improve as the time-temperature product was increased. The maximum enhancement will be reached before the open circuit voltage has increased to its maximum. For a given temperature the firing times are increased until the V_{OC} has reached its maximum. Longer times yield lower open circuit voltages again. A

temperature is then chosen which permits a long enough firing time to be used that allows good control. Generally for the wafer size, boat, and paste thickness used it was found that a firing time of 20 seconds at 850°C furnace temperature gave the best back surface field effects.

2.4. Final Cell Design

In keeping with the requirements of the program the final cell design utilized vacuum deposited wraparound contacts in conjunction with screen printed dielectric isolation. Cell dimensions were established at 20 X 40 X 0.2 mm, although the presence of the slight bead along the insulated edge added approximately 0.05 mm to the cell thickness right at the edge. A back surface field was incorporated in the cell structure, and the residual metallic aluminum layer, left after alloying in the $P\text{-}P^+$ junction, was left in place to cover the entire back of the cell.

The dielectric material decided upon for the proposed final design was Transene #1000. The metallization was vacuum deposited through appropriate shadow masks and consisted of the conventional chromium-palladium-silver contact system. The illuminated surfaces of the cells were texturized and a tantalum pentoxide antireflection layer was deposited over the entire front of the cells. The silicon used had a nominal bulk resistivity of 10 ohm-cm, and the diffused N^+ layer was approximately 80 ohms/sq.

2.4.1. Cell Configuration

The configuration of the contact geometry, contact pads, and dielectric layers is shown in Figure 3. A gridline density of twelve lines per centimeter was used, somewhat higher than needed for the diffused junction depth, but not sufficiently high to offer excessive loss in active area. Gridline widths were about 0.025 mm, but

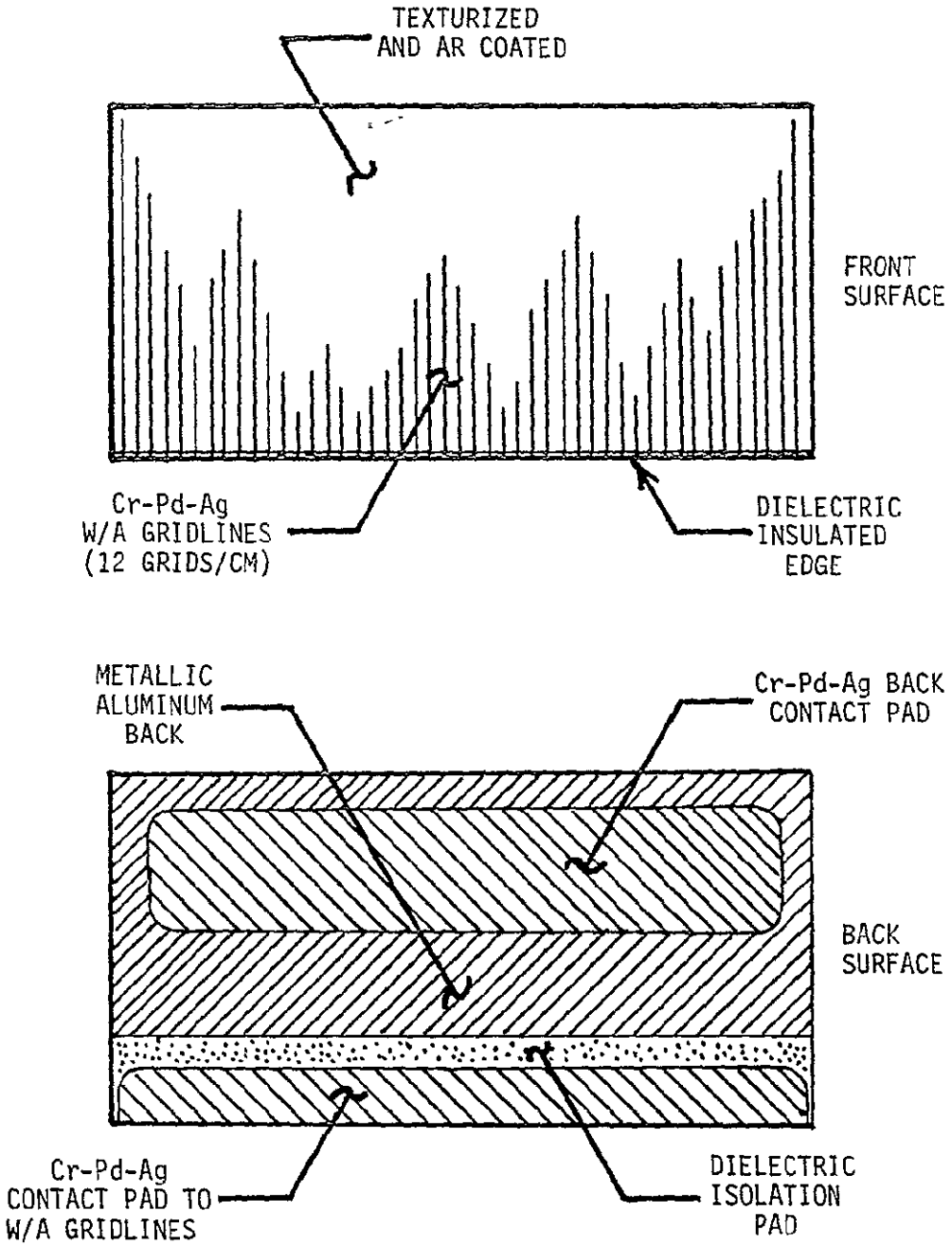


Figure 3

Configuration of 2 X 4 cm Wraparound
Contact Cell with Dielectric Isolation

these were somewhat wider in the immediate vicinity of the wrap-around edge, since the presence of the dielectric bead kept the masks from close contact with the cell front surfaces during the vacuum depositions.

The dielectric isolation consisted of a 50 mm wide strip on the back cell surface, running along, and wrapping around one of the long dimension edges of the cell. The bead along the edge extended about 0.04 mm onto the front of the cell. The thickness of the dielectric layer on the back of the cell was approximately 0.025 mm.

The gridline contact pad, deposited on the dielectric on the back of the cell, ran in a strip 3 mm wide along the edge of the cell and extended about half way around the insulated edge to meet the wraparound gridlines. The base contact was rectangular and measured 8 X 35 mm. This was deposited onto the metallic aluminum layer covering the cell back. The size and location of these contact pads particularly for assembly into an array, but were designed only for ease in fabrication and convenience in contacting the cells for evaluation.

2.4.2. Process Sequence

The process sequence proposed and used for the fabrication portion of the program was essentially that shown in Figure 1 of this report. Minor changes were made as the program progressed, such as the elimination of the back etch step, but such changes were only made after feasability had been clearly established. The most important change made in the processing was done towards the end of the fabrication phase. It was noted that the dielectric material being used appeared to undergo devitrification of the first layer during the firing of the second with a resulting loss of isolation. This was very possibly brought about by the necessity for performing the firing operations in a tube furnace, with the sizable thermal shocks caused by such methods. It was noted that TFS #1126RCB appeared to withstand this treatment with less

evidence of microcracking. Therefore approval was sought from and granted by the NASA Program Manager to make this substitution.

2.4.3. Cell Testing Program

Cell performance was tested under a Spectrolab Mark III Solar Simulator, which was adjusted to an AMO incident radiation level of 135.3 mW per cm^2 using a NASA calibrated standard cell. It was necessary to design a special test fixture to provide vacuum hold-down on a thermal sink held at the test temperature to a tolerance of less than one degree Centigrade. This fixture also provided spring loaded phosphor-bronze contacts to the contact pads on the back side of the cell.

Ten cells were randomly selected from each lot processed and were tested at AMO and 25°C. I-V characteristic curves were plotted for each of these cells and values measured for open circuit voltage, short circuit current, and maximum power point. The cell conversion efficiency and fill factor were calculated from these data.

The contact adherence was tested on one cell from each lot by the standard procedures used for space type cells. In these tests a 26 gauge wire is soldered to each of the contact pads using liberal amounts of solder and flux. These wire were then subjected to pull tests using a Chatillon DPP-1kg dial push-pull gauge.

One cell from each fabrication lot was subjected to rubbing with a Pink Peral eraser for 20 strokes with a force of 20 ounces. The cell was then examined for any evidence of peeling of the AR Coating. After an electrical performance test, one cell from each lot was subjected to immersion in boiling water for 30 minutes. After drying both front and back surfaces were covered with Scotch Brand #810 tape, which was pressed until transparent, and then stripped from the cell. The cell was then retested for electrical performance.

Five cells from each lot were subjected to ten temperature cycles at a maximum thermal rate of 90°C per minute between -196°C and +100°C. The cells were held at these temperatures for 2 minutes. They were then checked for electrical performance.

A total of ten cells were tested for tolerance to both humidity and temperature storage by placing them in a chamber at 65°C and 90% relative humidity for seven days. They were then subjected to a tape peel test as described above.

2.5. Cell Fabrication

Once approval had been received to go ahead with the fabrication of cells using the process sequence proposed at the Design Review, lots were started into processing on an average of one per week. Starting lots consisted of one hundred 51 mm diameter, p-type, 10 ohm-cm wafers. Wafers were 0.35 to 0.40 mm thick, and were sliced so that the plane of the wafer was perpendicular to the <100> crystallographic axis. All wafers were started as received from the slicing saws.

Because of the limited time remaining in the program, processing was often concurrent, with new lots being started before previous lots were completed. A total of six lots were processed through metallization, but the availability of equipment caused some lag in applying the AR coatings and in electrical testing. Part way through the fabrication phase a malfunction in the dicing equipment caused another unexpected delay. The dicing saw had to be returned to the manufacturer for repair and was not returned to service for a period of six weeks. Since all cells had to be cut to size on this piece of equipment, the delay was a serious one.

Because of the losses due to mechanical breakage incurred in the edge sanding operation, used to provide a rectangular edge for the subsequent wraparound screen printing operations, an alternate

technique was devised for dicing the round wafers to the final cell size which also produced squared-off edges. After the removal of the surface powder remaining on the wafers after alloying in the aluminum P^+ back surface field layer, the round wafers were wax mounted on slightly larger diameter dummy wafers. The 2 X 4 cm cells could then be cut completely through on the dicing saw and then edge etched in place before demounting. This eliminated the edge sanding, masking, and edge etching steps used in the approved process sequence. Approval for adopting this method was requested of the NASA Program Manager, but since this method was not worked out early enough, it was not used on the first six lots.

Microscopic examinations of the wraparound dielectric isolation on finished cells indicated that microcracking was present on a majority of the units. Further investigation indicated that this occurred generally at the time of firing the second dielectric layer. Cells made early in the program using TFS #1126RCB dielectric paste, which had been abandoned because this paste was fired at a temperature $100^{\circ}C$ higher than the Transene #1000, seemed to exhibit markedly fewer microcracks. Therefore permission was requested of the NASA Program Manager to substitute TFS #1126RCB for the Transene #1000 dielectric. This change was also approved, but again the modification was not made in the process until the last lot of cells.

The better cells from each lot were individually evaluated for their electrical performance and then shipped to the NASA Program Manager. Environmental tests were performed on cells selected at random from the remaining units in each lot. Finally the rest of the cells in each lot were tested to obtain I-V curves for each. They were then shipped to NASA.

2.5.1. Process Evaluation

Data taken from each of the lot travelers indicating the yields for each step in the process are given in Table 1. It should be noted

Table 1

Process Sequence and Yields for First Six Lots

Step No.	Process Step	Step Yield	Cumm. Yield
1	30% NaOH Etch	100.0	100.0
2	2% NaOH Etch (texturize)	99.7	99.7
3	Phosphorous Diffusion	99.8	99.5
4	Check Sheet Resistance	100.0	99.5
5	Apply Mask Resist to Fronts	100.0	99.5
6	Back Etch	99.7	99.2
7	Print Aluminum Paste	98.5	97.7
8	Dry Aluminum Paste	100.0	97.7
9	Alloy Aluminum Paste	100.0	97.7
10	Probe Check V_{oc}	100.0	97.7
11	Dice to 2 X 4 cm Size	96.9	94.7
12	Sand Long Edges	88.6	83.9
13	Remove Aluminum Powder	99.4	83.3
14	Ultrasonic Clean	95.7	79.8
15	Mask Front and Back	100.0	79.8
16	Edge Etch	99.8	79.6
17	Remove Masking	99.6	79.3
18	Print 1st Dielectric	98.5	78.1
19	Dry 1st Dielectric	100.0	78.1
20	Fire 1st Dielectric	99.1	77.4
21	Print 2nd Dielectric	96.5	74.7
22	Dry 2nd Dielectric	100.0	74.7
23	Fire 2nd Dielectric	100.0	74.7
24	Mask Front and Back	100.0	74.7
25	Dip Mask Dielectric Edge	100.0	74.7
26	HF Etch Front Surface	97.6	72.9
27	Remove Masking	99.7	72.7
28	Mount Front Metal Masks	99.7	72.5
29	Evaporate Front Metal	99.3	72.0
30	Mount Back Metal Masks	98.6	71.0
31	Evaporate Back Metal	99.0	70.3
32	Penumbra Etch	99.2	69.7
33	Apply AR Coating	98.8	68.9
34	Bake	100.0	68.9

that some operations (i.e., applying the AR coating) were performed in relatively small sub-lot groups in the Production Facility, and the lot travelers were not properly kept up-to-date and in the case of some lots not noted. This produced some discrepency between the cummulative yield data calculated from the available data on the lot travelers, particularly in the final process steps, and the actual number of cells fabricated. The calculated cummulative yield from the lot travelers for the entire process chain was 68.9%, while the six lots produced 326 cells for electrical test, which gave a line yield of 54.3% up to that point.

The last lot of wafers processed during the normal course of the program incorporated the modified dicing method and used the different dielectric material. This lot was found to have better than average electrical characteristics, although the actual line and electrical yields could not be determined because of the lack of proper record keeping for this particular lot.

2.5.2. Cell Electrical Evaluation

The cells were tested for electrical performance using a Spectrolab Spectrosun^{R} Solar Simulator, Model X-25 Mark III, which produced the required AMO illumination. The test fixture incorporated a brass block, held at 25^{o}C by passing water from a constant temperature tank through the block, and a vacuum hold-down which kept the cell under test held tightly against the block. Buried phosphor-bronze spring contacts were so arranged as to press against the cell contact pads on the back (down) surface. The intensity level of the solar simulator was adjusted to 135.3 mW/cm^{2} using a NASA calibrated standard cell. Values of V_{oc} and I_{sc} were measured using a Spectrolab Production Test Set, Model 380-31B and a DANA Digital Voltmeter, Model 5400. The I-V curves were then made using a Spectrolab Model D-550 Electronic Load and a Hewlett-Packard Model 7035B X-Y Recorder.

It was found during the electrical testing that some care had to be exercised when shifting the leads of the test fixture from the Production Test Set to the Electronic Load. Cells might be checked for V_{oc} and I_{sc} on the Test Set, but would appear either shorted, or badly shunted when the I-V curve was made, even though the values obtained for V_{oc} and I_{sc} appeared satisfactory. On checking these values again on the Test Set the cells appeared to be still shorted or shunted. A possible cause for this was a breakdown of the dielectric isolation by transients set up in the circuitry when the leads were changed. Thus it became necessary to remove the cell from the test fixture when the leads were shifted.

Data for the average electrical performance of all of the lots processed under the main program are shown in Table 2. Again it was found that even though cells might have very satisfactory electrical outputs, with good conversion efficiencies, the I-V curve shapes were relatively low. Spot checks of the cell series resistance, using a graphical analysis, gave values ranging from 0.058 ohm to 0.2 ohm, which appeared to be satisfactory, thus the low values of CFF were ascribed to varying degrees of electrical shunting due to inadequate isolation by the wraparound dielectric layer. Typical I-V curves for a "good" cell and for a substandard cell are shown in Figure 4.

One cell from each lot was tested for contact adherence by soldering a 26 gauge wire to the gridline contact pad and to the base contact pad and then measuring the amount of "pull" necessary to break the wire loose. The results are shown below:

Lot No.	Cell No.	Gridline Pad	Base Pad
1	12	310 g.	320 g.
2	13	390	615
3	5	330	570
4	21	540	1150
5	6	310	585
6	39	330	550

All cells broke during the pull test with the exception of the back

Table 2

Average Electrical Performance of All Lots Made Under Main Program

Lot No.	Wafer Starts	Qty Into Elec.Test	Cells With Elec.Output	Percentage Elec.Yield	V_{oc} (mV)	I_{sc} (mA)	V_{mp} (mV)	I_{mp} (mA)	P_{max} (mW)	Max.Pwr. Density (mW/cm^2)	Calc. Eff.%	Calc. CFF
1	100	53	19	19	601	343	462	285	131.67	16.46	12.26	.64
1*			5	5	610	347	490	311	152.21	19.03	14.01	.72
2	100	64	33	33	607	340	475	294	139.61	17.48	12.92	.67
2*			17	17	610	344	487	310	151.08	18.89	13.96	.72
3	100	49	30	30	597	332	477	279	133.08	16.64	12.30	.67
3*			5	5	601	343	488	304	148.16	18.48	13.66	.72
-4	100	66	35	35	608	342	478	289	138.17	17.28	12.77	.67
4*			17	17	608	346	490	307	150.65	18.83	13.92	.72
5	100	44	20	20	593	340	445	265	117.93	14.79	10.89	.59
5*			2	2	600	343	485	312	151.32	18.92	13.98	.74
6	100	50	38	38	586	336	436	260	113.36	14.24	10.52	.58
6*			0	0	---	---	---	---	------	-----	-----	---
6B	?	?	34	?	606	340	488	303	147.86	18.48	13.66	.72
6B*			25	?	607	346	494	312	154.13	19.27	14.24	.74

* Cells having conversion efficiencies greater than 13.5%.

NOTE: Lots No. 1 and 3 had cells lifted from processing part way through processing, thus yields not correct.

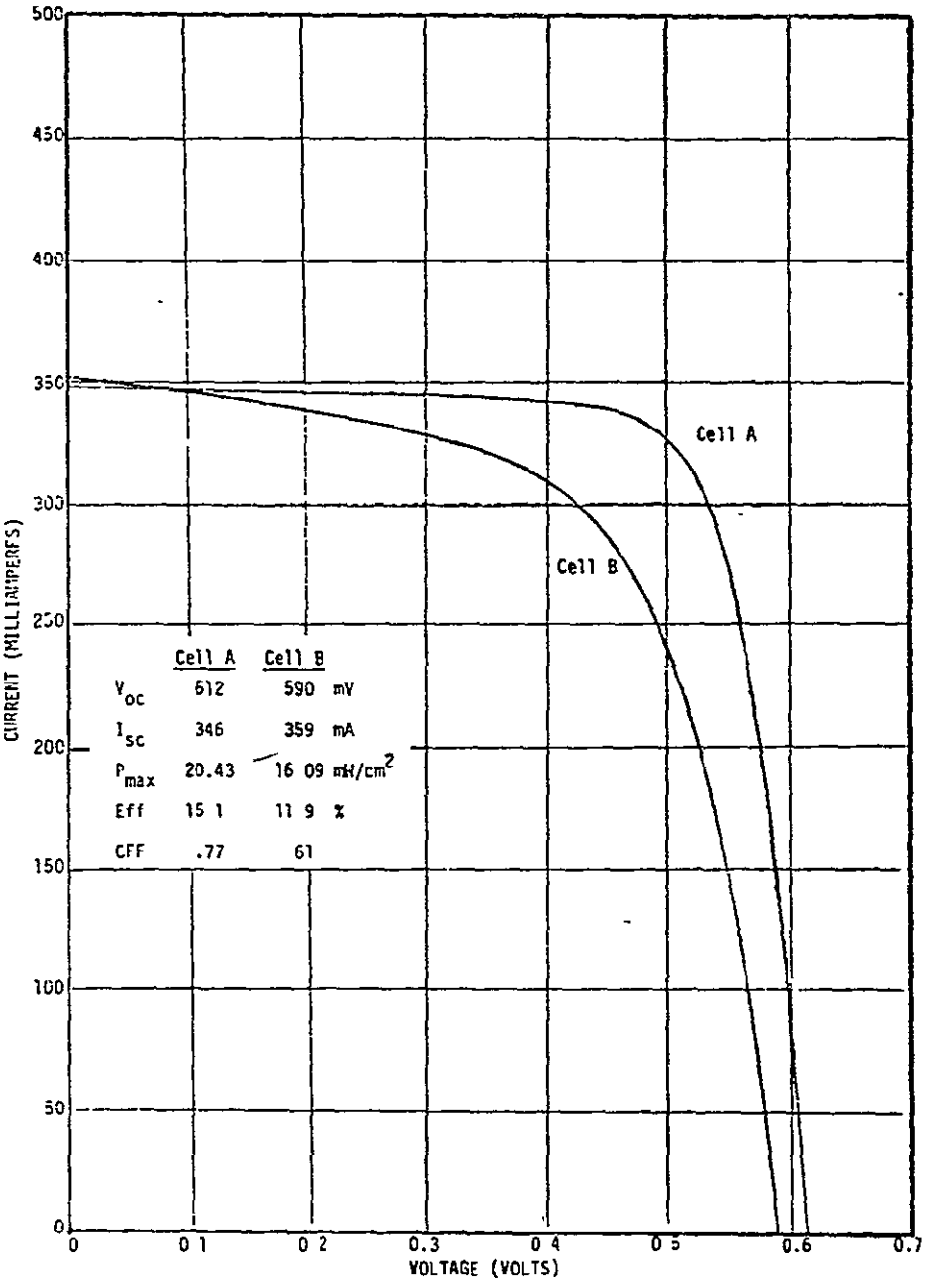


Figure 4

Typical I-V Curves for "Good" and Substandard Cells

contact of the cell selected from Lot #4, which remained intact.

One cell from each lot was subjected to rubbing with a Pink Pearl eraser for 20 strokes with a force of 20 ounces. This was a test to determine the adherence and quality (mechanical) of the AR coating. There was no evidence of any peeling or loss of AR coating adherence after this treatment.

One cell from each lot was immersed in boiling water for a period of 30 minutes. These cells were then tested by pressing Scotch brand #810 tape against the surface, pressing until transparent, and then stripping the tape from the cell. It was found that this treatment generally broke the cells, but in all cases but one the contact pads were not affected. Cell #5 from Lot #4 exhibited a slight loss of contact along one edge of the pad when the tape was removed.

Five cells from each lot were tested for electrical performance and then subjected to ten temperature cycles at a maximum rate of 90^{o}C per minute between -196^{o}C and +100^{o}C. The cells were held at these temperature extremes for two minutes. After the temperature cycling the cells were again tested for electrical performance and the changes noted. It was found that the average cell experienced a 3.8% degradation in conversion efficiency (i.e., dropped from 13.7% to 13.2%). There seemed to be no indication of cells with lower efficiencies degrading more than those with higher efficiencies.

Two cells from each of the first five lots were subjected to eight days of storage in a chamber at 65^{o}C and 90% relative humidity. In all cases the front gridlines of the cells showed indications of flaking and peeling. The contact pads on the backs of the cells were all still intact, but all were badly discolored and exhibited definite signs of deterioration. The condition of the contacts was so poor that the tape peel test was not performed.

2.5.3. Additional Cell Fabrication

Since the modifications in the process sequence and the change in the dielectric material had been incorporated only in the last lot fabricated, which appeared to have better-than-average cell performance, it was decided to fabricate three additional lots. It was planned that these three lots would be processed without changes in any of the fabrication steps. This additional processing would not only provide additional finished cells for experimentation but would permit the modified process sequence to be evaluated for yield information.

A considerable time interval occurred between completion of Lot 6B and the start of activities on the three additional lots. During this period there was a major change in the personnel assigned to this program. It was thus necessary to spend additional time to train technical support personnel in the screen printing operations and in the steps peculiar to the wraparound configuration. Also, since time and funding was limited, it was decided to continue using the metal masks used for the vacuum metallization. This caused major difficulties, since the masks were in poor condition, thus producing wider than normal grid lines and because of the interrelationship with the geometry of the screen printed wraparound dielectric, required trimming of the cells after metallization. This caused additional handling and mechanical damage and losses not experienced previously.

The cells resulting from this additional effort were disappointing in nearly all respects. The cummulative line yield was only 46%, reflecting the inexperience of the personnel, as well as the losses incurred during the additional trimming operations. The electrical performance of the cells also indicated the substandard workmanship and metallizations. Of approximately 250 wafer starts only 19 cells were completed that had an average conversion efficiency of only 12.6% at AMO and 28^{o}C. Only one cell of the nineteen could be considered satisfactory with an efficiency of 14.5%. These cells also exhibited the relatively low I-V curve factor, averaging.0.68.

3.0 CONCLUSIONS

This program has evolved a process capable of fabricating silicon solar cells with vacuum deposited wraparound contacts and screen printed dielectric isolation. Some of the cells produced during the program exhibited relatively high output efficiencies, greater than 15% at 25°C under AMO illumination, however nearly all cells made were found to have low I-V curve fill factors ranging from 0.60 to 0.78. The lack of good curve shape has been ascribed to shunting effects due to varying degrees of electrical integrity of the dielectric. A single experiment appears to confirm this, since a cell which had a low CFF was markedly improved by slicing off the wraparound dielectric edge and adding a conventional gridline contact bar on the front surface.

The application of the dielectric by screen printing methods has not proven to be particularly difficult, with less than anticipated mechanical breakage for this operation. The compatibility of the dielectric material with the silicon offers, however, a serious problem due to the mismatch between the thermal expansion coefficient of the isolation and the silicon. Dielectric materials that match the thermal expansion of the silicon must generally be fired at temperatures sufficiently high to present other problems, particularly on BSF cells where the aluminum is left in situ on the back surface of the cell. Dielectrics that can be properly fired at low temperatures have a large thermal mismatch with the silicon.

All of the thick film firing operations for this effort have been carried out by firing in a tube furnace, which results in time/temperature cycles that are quite different than those recommended by the paste manufacturers. Some reduction of the rapid cooling and solidification of the dielectric can be

avoided by use of firing boats having high thermal mass, but the cooling dielectric is still subjected to a relatively rapid cool-down. The use of a conveyor belt furnace would minimize this problem. Since the thermal expansion of the silicon is much less than the glass, the isolation, on cooling, is under tension. This condition offers the greatest possibility of cracking since nearly all glassy materials are less strong under tension than compression.

The program has been successful in producing some cells with relatively high conversion efficiencies, which establishes feasibility beyond any doubt. The proper dielectric wraparound isolation has not been found, however, those used on the program offered only marginal performance due to thermal expansion problems. If these problems can be overcome, these cells will prove particularly attractive for use in the low-cost automated assembly of solar cell arrays.

4.0 RECOMMENDATIONS

Further effort toward achieving a viable cell design for a wraparound contact cell using dielectric isolation should be centered on solving the problem of finding a screen printable dielectric that is compatible with silicon. Such a material must offer adequate isolation to prevent shunting, must be capable of proper firing at temperatures that will not adversely affect the minority carrier diffusion length in the silicon, or the junctions in the silicon. Testing of candidate dielectric materials must also establish that they do not contain contaminating dopants detrimental to the cell structure, and that the screen printing method of application does not damage the cell junction structure.

Sufficient processing of wraparound cells needs to be undertaken to assure that cells produced are characteristic of the process sequence, and not of the degree of skill of the personnel producing the cells. The actual design of the cell contact configuration should be modified to reflect the requirements of the potential end user, particularly as to the arrangement and location of contact pads. Wherever possible the process should be simplified in order to reduce the number of steps in the sequence, since this program has re-emphasized the fact that a very large number of steps, each with a high yield, still results in a sequence with an overall low yielded output.

Once a dielectric material has been found that satisfies the above requirements, and a fabrication process sequence has been established, further work should be concentrated on producing relatively large numbers of such cells, to provide cells for evaluation and qualification, and to establish the characteristics viability of the production processes.