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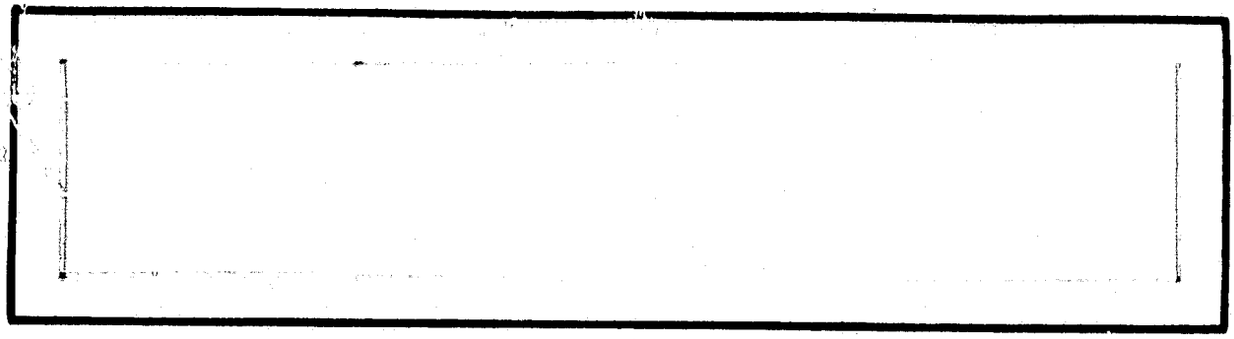

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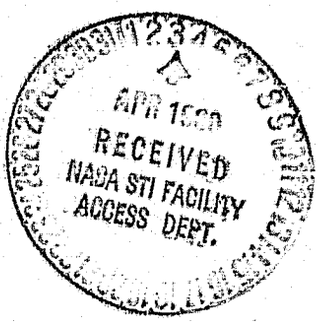

CRITIQUE OF A HUGHES SHUTTLE KU-BAND DATA SAMPLER / BIT SYNCHRONIZER

Contract No. NAS 9-15795

Interim Report

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1.0 SUMMARY AND CONCLUSIONS

A bit synchronizer proposed by P. H. Conway of Hughes Aircraft is analyzed in a noise-free environment. This task is accomplished by considering the basic operation of the loop via timing diagrams and by linearizing the bit synchronizer as an equivalent, continuous, phased-lock loop (PLL).

It was determined that the basic approach was a good design which, with proper implementation of the accumulator, up/down counter and logic should provide accurate mid-bit sampling with symmetric bits.

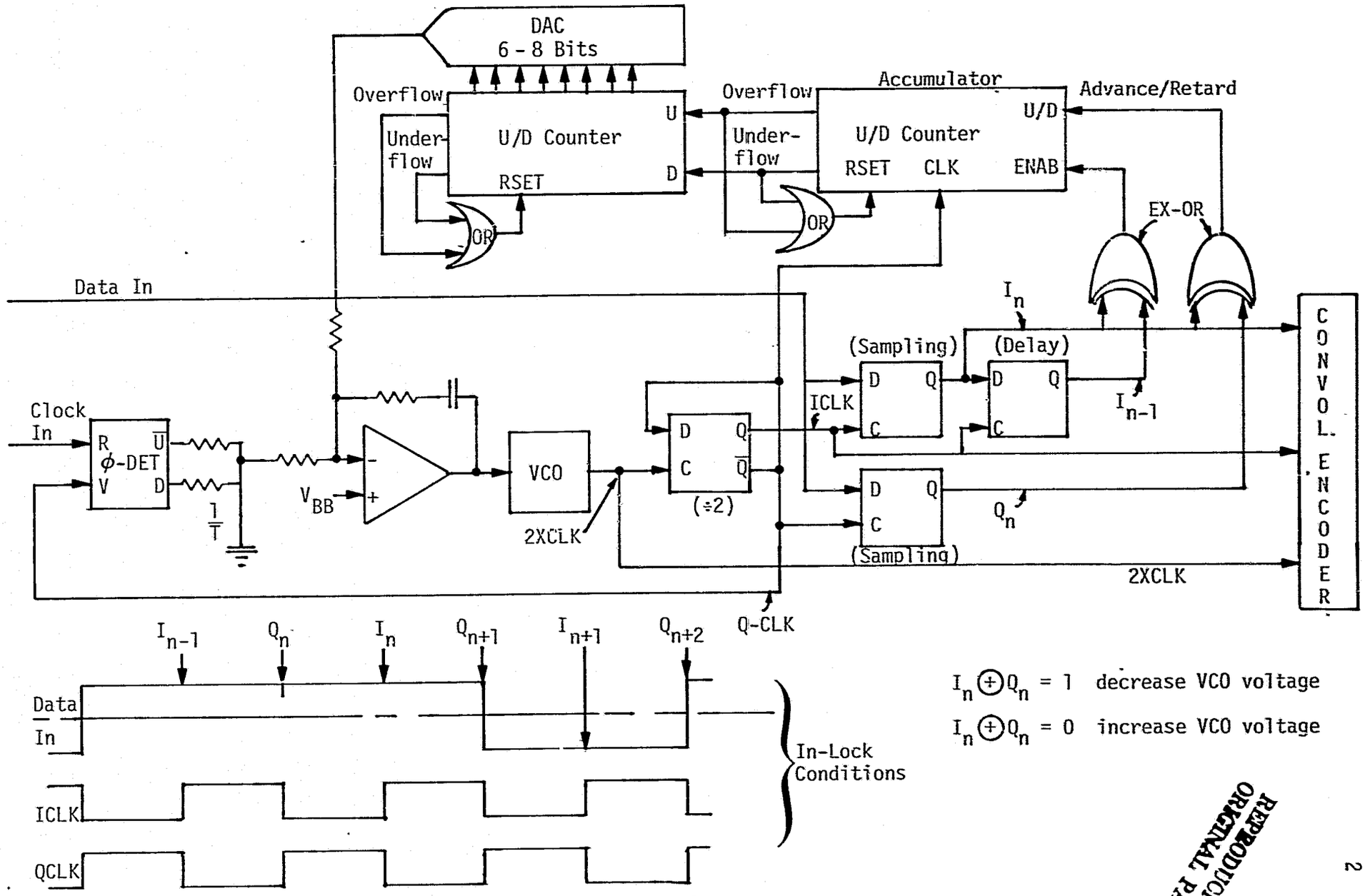
However, when bit asymmetry occurs, the bit synchronizer can lock up with a large timing error, yet be quasi-stable (timing will not change unless the clock and bit sequence drift). This will result in incorrectly detecting some bits. The apriori probability of falling into this quasi-stable region is equal to the asymmetry (defined in Section 6.0) expressed as a fraction. This assumes a uniform distribution over T sec. Thus, except for the case of no asymmetry, there is always some possibility of remaining in lock but incorrectly detecting some bits.

As a final comment, if the timing difference between the bit stream and the clock can be held to less than $\pm \frac{1-ASY}{2}$ T sec (T is the undistorted bit duration), the bit synchronizer loop will never get into the third zone, where bit errors are made but the loop holds lock.

2.0 INTRODUCTION AND DESCRIPTION OF THE NEW BIT SYNCHRONIZER

The purpose of this report is to discuss one "fix" to the operation of a Shuttle Ku-band bit synchronizer which utilizes both clock and data inputs. The present bit synchronizer has a jitter problem and, consequently, occasionally will sample the same bit twice and skip the following bit.

An alternative bit synchronizer suggested by P. H. Conway of Hughes Aircraft [1] is shown in Figure 1. The loop is composed of a Motorola high-frequency phase-frequency detector (ϕ-DET) [2-4] which is capable of detecting both phase and frequency errors and is used to track the clock, and a bit transition detector which attempts to track the transitions of the data bits.



I samples are midbit; Q samples are at the data transitions

Figure 1. Ku-Band Data Sampler With PLL Clock Tracking

The Q clock signal shown in Figure 1 is compared with the received clock (clock in) which, by virtue of the phase/frequency detector, produces a signal which has a dc component proportional to the frequency error (if there is one). Then, when in frequency lock, it produces a signal which has a dc component proportional to the phase error between the input clock and the VCO output.

Now, if the digital-to-analog converter (DAC) output was not hooked up to the loop filter, the bit synchronizer would track the received clock with negigible phase error. However, since the received clock and data are at the same frequency but are not phase coherent, it is necessary to bump the clock phase so that data samples are taken at mid-bit. The function of the DAC is to provide samples of the data at the mid-bit point. The VCO clock runs at twice the rate of the received clock and is divided down to the clock rate by the D flip-flop following the VCO. Actually, this flip-flop provides both an I and a Q clock which are phased one-half a bit apart, as shown in the lower left corner of Figure 1.

The I and Q clocks are used to sample the data one-half of a bit apart, when synchronized. This sampling is effected by the two D flip-flops following the divide by 2 flip-flop. By using the "exclusive-OR" of two successive data samples, a transition detector is created, thereby producing a binary one with a transition and a binary zero when there is no transition. This control enables or disables the up/down counter to count either up or down. By comparing the I and Q data samples (I_n and Q_n in Figure 1), an estimate of the error in the actual transition sample (Q_n) and the data transition location is obtained. It is to be noted that the exclusive-OR output yields only the algebraic sign of the error, not the magnitude. This error, assuming a data transition, will be accumulated in the up/down (U/D) counter until it either underflows or overflows. The accumulator actually has two functions. The first is to reduce the speed to the DAC; the second is to control the quantization of the loop phase error control. The second up/down counter feeds into a DAC which converts the accumulated count into an analog voltage, which drives the bit synchronizer loop filter. In effect, the up/down counter acts upon the bit timing error signal the same way

an integrator would. This integration is precisely what is needed to force the mid-bit data sampler into the mid-bit position! This fact will be made clearer in Section 5.0.

In conclusion, the bit synchronizer shown in Figure 1 is designed to track the clock and sample the data sequence at the mid-bit point. We now consider the phase/frequency detector and the bit detector in more detail in the following sections.

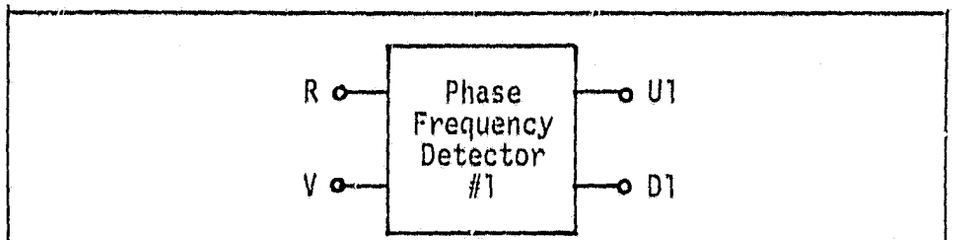
3.0 DESCRIPTION OF THE MOTOROLA PHASE/FREQUENCY DETECTOR

Both the MC4344/MC4044 [3] and MC12040 [4] Motorola phase/frequency detectors can be used in a broad range of phased-lock loop applications. Both sets of detectors are functionally equivalent, however, the MC12040 is capable of operating at higher clock speeds. Because of the functional equivalence, we shall confine our discussion to the MC4344/MC4044 unit.

The Motorola MC4344/MC4044 phase/frequency detector is composed of a phase/frequency detector, a quadrature phase detector, a charge pump and an amplifier. It is the function of the charge pump to convert the pulses out of the phase/frequency detector to a DC value which is essentially proportional to either the phase or frequency error.

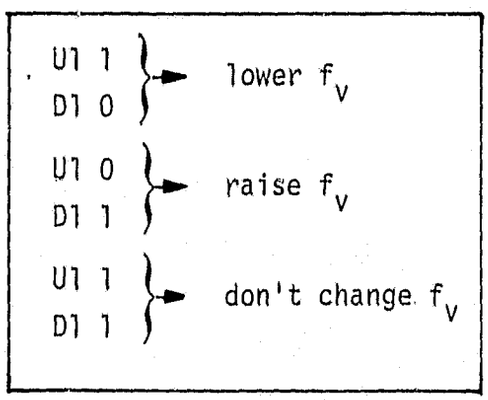
In Figure 2, the phase/frequency flow table for the phase/frequency detector is given, along with the charge pump/amplifier frequency control.

In order to understand the usage of Figure 2, we shall consider an example. Assume that the received clock (R input to the ϕ-frequency detector) lags the local reference (V input to the ϕ-frequency detector) by one-twelfth of a square wave clock cycle, as shown in Case I of Figure 3. Starting at state 8 in Figure 3 which corresponds to the R,V pair being in state 1,0, we go to Figure 2a and note that state (8) (with the parentheses) produces an output U1 = 1 and D1 = 1. Now, in the time interval denoted by (7), we note that R,V = 1,1. Moving horizontally in the same row to the left, one column (under R-V = 1,1), we find a seven. Therefore, we look vertically in the column for (7) which we find one row higher, with a corresponding output of U1 = 1 and D1 = 1. The next input is R = 0, V = 1. Moving horizontally in the fifth row, we find a 2. Moving vertically to the second row, we find the (2), which has a



R-V	R-V	R-V	R-V	U1	D1
0-0	0-1	1-1	1-0		
(1)	2	3	(4)	0	1
5	(2)	(3)	8	0	1
(5)	6	7	8	1	1
9	(6)	7	12	1	1
5	2	(7)	12	1	1
1	2	7	(8)	1	1
(9)	(10)	11	12	1	0
5	6	(11)	(12)	1	0

(a) Phase Frequency Detector Flow Table



(b) Charge Pump-Amplifier Control

Figure 2. Phase/Frequency Detector Flow Table and the Charge Pump-Amplifier Frequency Control

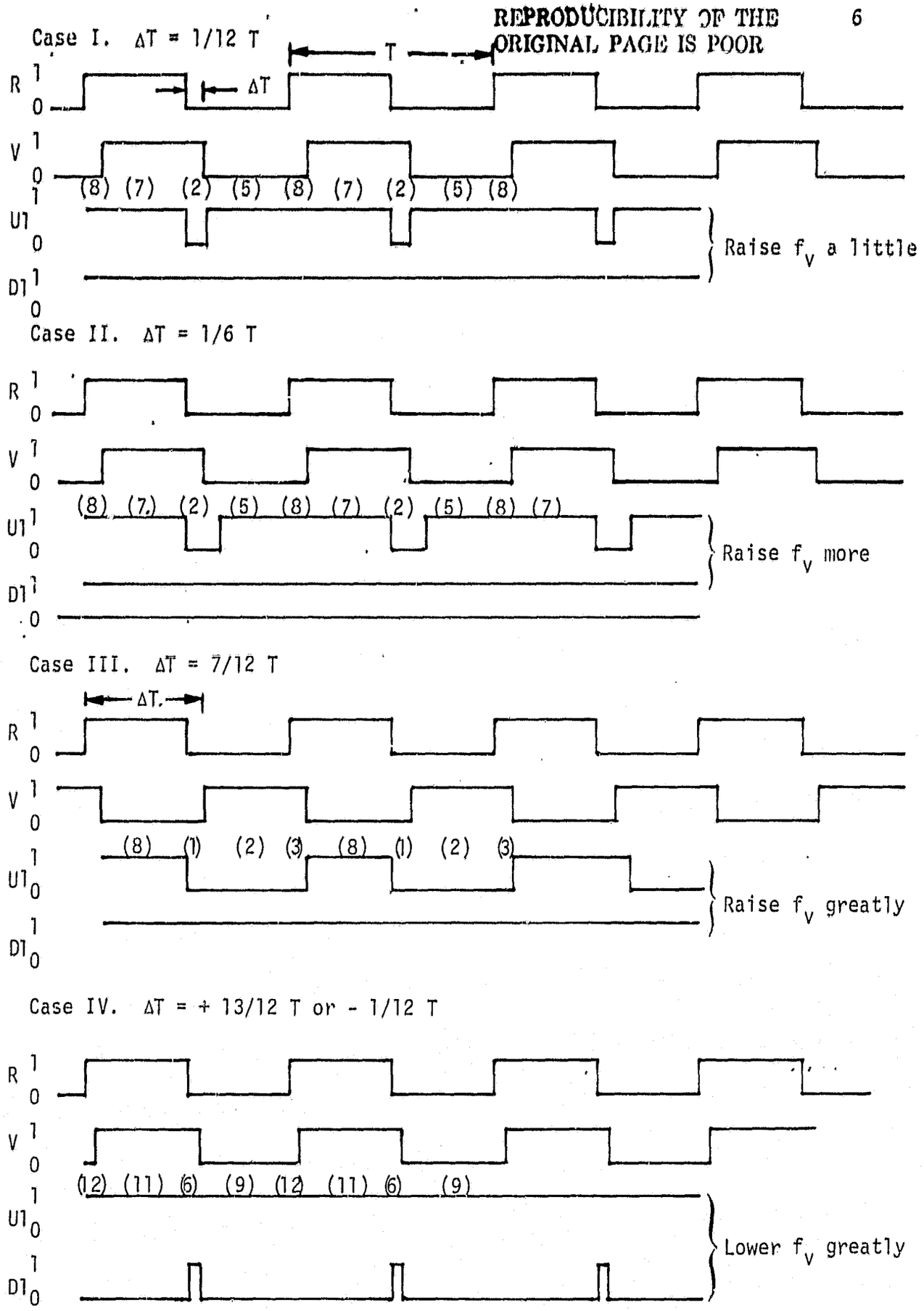


Figure 3. Performance of the Phase/Frequency Detector for Various Phase Errors

corresponding output of U1 = 0, D1 = 1. Hence, at this point, the U1 output drops to zero while the V1 remains at one, as shown in Figure 3. Continuing in this manner, we find that the phase/frequency detector goes through the states (5), (8), (7), (2), (5), (8), etc., generating the waveforms U1 and D1 shown in Case I, Figure 3. Now, by considering Figure 2b, we see that, when U1,D1 = 0,1, the DC voltage out of the charge pump/amplifier is increased and, when U1,D1 = 1,1, the DC voltage does not change. As a consequence, the DC voltage applied to the loop filter-amplifier increases to the VCO input, causing the local reference to catch up to the received clock.

By viewing Figure 3 cases II and III, it is seen that a large timing or phase error produces a larger DC voltage out of the charge pump. By virtue of the way the charge pump works, the error control signal, when properly smoothed, is proportional to the timing error over the region $\pm T$, where T is the clock or bit period. In viewing the error to be phase rather than timing, we find the error signal to be linear over $\pm 2\pi$.

In case IV of Figure 3, the situation when the timing error is increased to $\frac{13}{12}$ T $\left(\text{or } -\frac{1}{12}\text{ T}\right)$ is shown. Even though the error is equivalent to case I of Figure 3, the error signal derived from the flow table of Figure 2 yields a different error control voltage. The reason for this difference is obvious when one considers the S-curve of Figure 4.

Because of the memory in the phase/frequency detector, there are two error control signals for each error position, or phase error, ϕ. The arrows in Figure 4 indicate how the the loop behaves as the phase increases, first to 2π and then to 4π on a different branch, then returns to zero on the new branch. The original stable point was 0 rad on the first branch but the second branch is stable at 2π rad (T sec).

The above discussions were concerned with phase or timing errors. We now consider frequency errors. Using the flow table of Figure 2a, we can establish that, when $f_R/f_V = 10$ or when $f_V/f_R = 10$, error control amplitude is monotonically increasing with increasing frequency error (it is not linear). The results are plotted in Figure 5 for the case of 10:1 frequency error and Figure 6 for 3:1 errors.

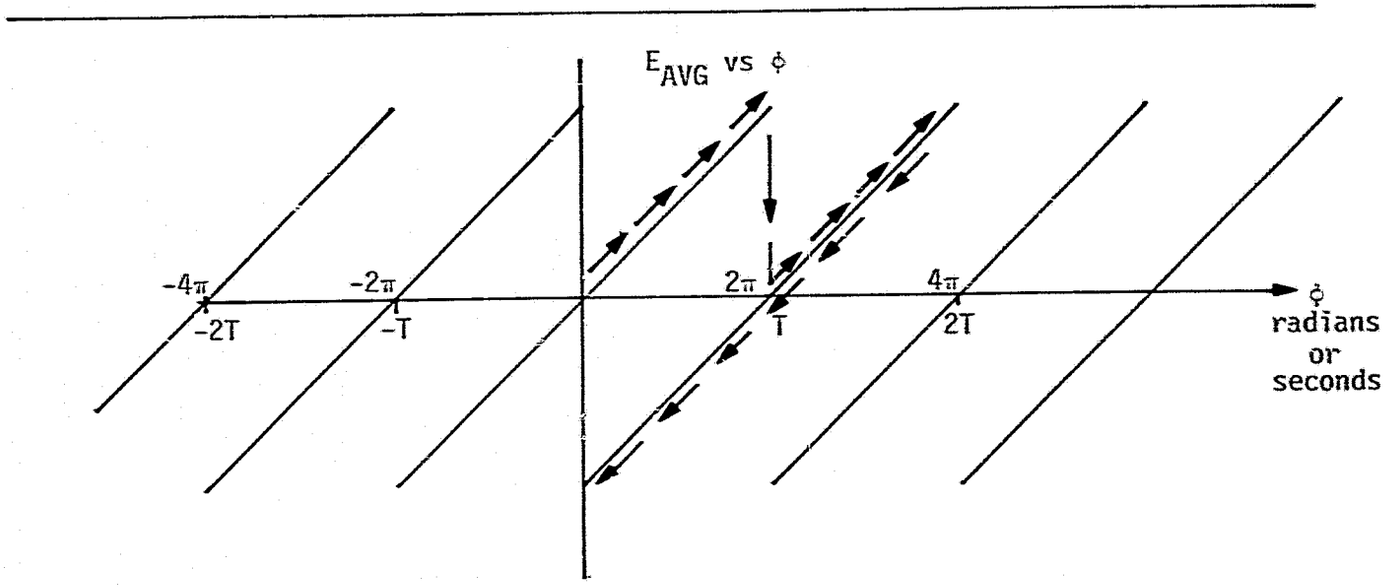


Figure 4. S-Curve of the Phase/Frequency Detector (Frequency Locked)

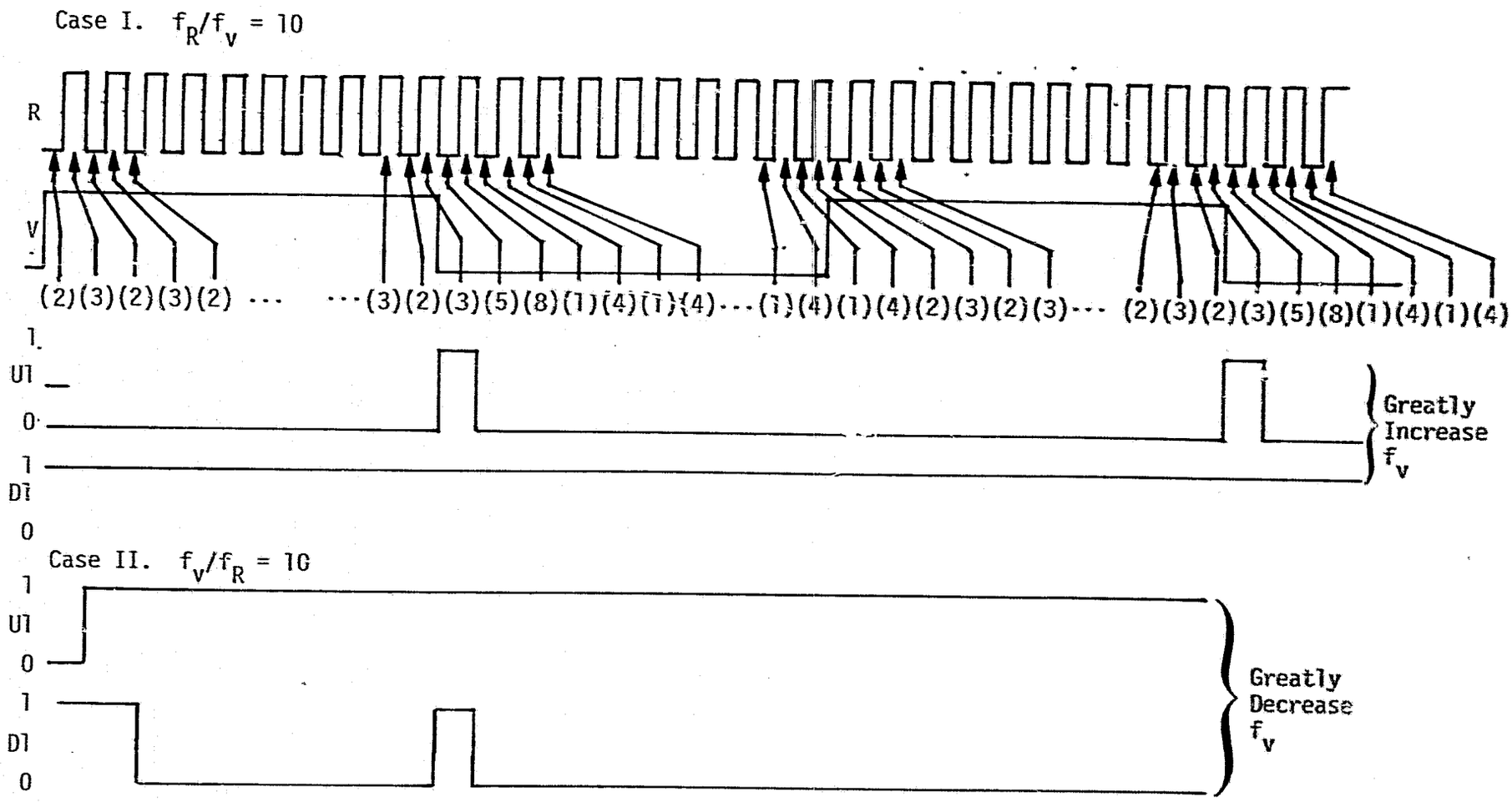


Figure 5. Phase/Frequency Detector When a Large Frequency Error Exists

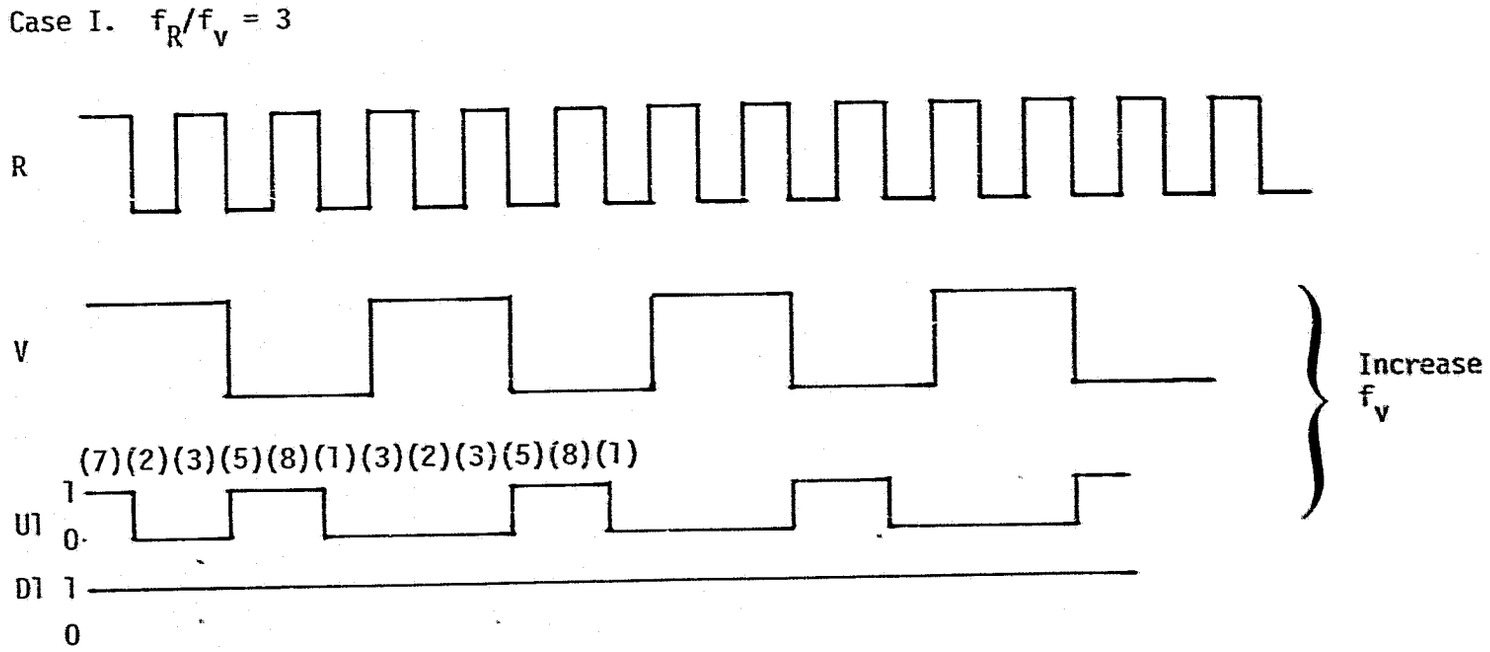


Figure 6. Phase/Frequency Detector for a 3:1 Frequency Error

4.0 DECRIPTION OF THE DATA DETECTOR

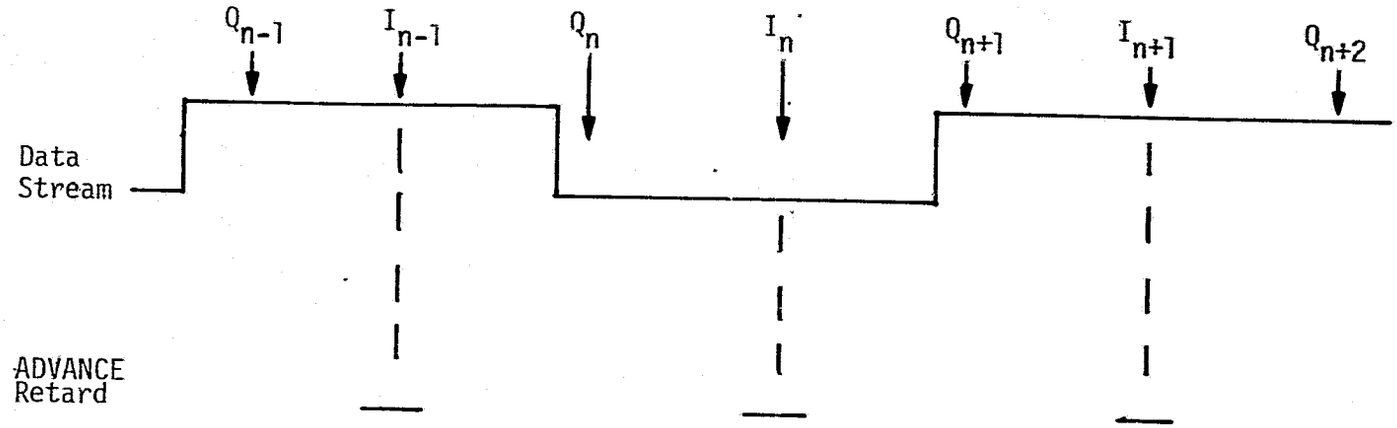
As was mentioned previously, the phase/frequency detector provides an error signal to track the clock while the data detector provides a perturbation error signal to force the data sampling to be mid-bit. The divide-by-two D flip-flop of Figure 1 produces both the I and Q samples which are one-half a bit apart in time when the loop is in frequency lock. The in-phase samples are delayed one bit in the second D flip-flop, labeled "delay" in Figure 1. Using an exclusive-OR gate, the present data bit is modulo-two added with the previous data bit. When the past and present data bits are of the same algebraic sign, obviously no transition could have occurred; hence, sampling the transition point could yield no useful timing information so that the accumulator is not enabled. On the other hand, when a transition occurs, the previous and past data bits do not agree and useful information can be obtained from a transition sample. The exclusive-OR gate enables the accumulator only when a transition occurs.

Data bit timing error information is obtained by comparing the present I and Q samples via an exclusive-OR gate. As shown in Figure 7, when the clock timing samples are either late or early, the modulo-two sum of I_n and Q_n is either 0 or 1, respectively. Therefore, $I_n \oplus Q_n$, where $\oplus$ denotes modulo-two addition, determines in which direction the loop timing should be adjusted in order that the Q samples lie very near the transition of the bits. Therefore, the I samples will be in the mid-point of the data bits, which is the result desired to avoid missing bit samples.

By using an accumulator with overflow, an up/down counter can be used to reduce the speed of the up/down counter driving the DAC. Furthermore, the accumulator sets the quantization error in the bit time tracking accuracy. The DAC converts the up/down counter output to an analog voltage which, in turn, adds with the phase/frequency detector to produce the loop filter input signal.

When the bit synchronizer is not frequency locked, it produces no useful information. Although it is not necessary, inhibiting the bit detector DAC output during acquisition would improve acquisition time.

I. Timing Late



II. Timing Early

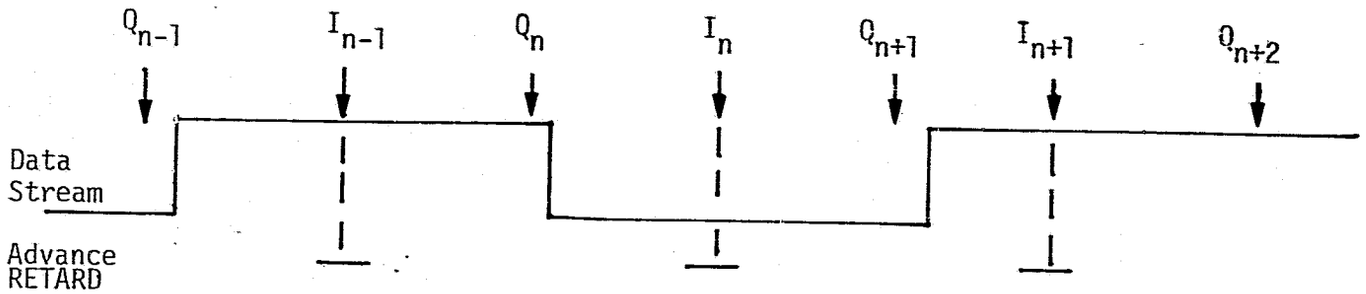


Figure 7. I-Q Relationship for Bit Sampling Showing Bit Timing Control

5.0 LINEARIZED ANALOG EQUIVALENT LOOP ANALYSIS

In this section, we model the loop of Figure 1 in a simplified, linearized, loop structure shown in Figure 8. First we replace the phase/frequency detector with a phase detector (multiplier). Next, we replace the data detector with a phase detector (multiplier). Finally, the accumulator and up/down counter are replaced with an integrator since, in effect, that is the function they perform.

In order to utilize this model, the clock and the data must be replaced with sinusoidal signals, as shown in Figure 8. We have assumed that the phase of the data is arbitrary with respect to the clock which is indicated by the phase angle ψ.

The phase error is defined to be the error between the data clock and the VCO reference, r(t). thus,

$$\phi(t) = \theta + \psi - \hat{\theta}(t) \tag{1}$$

We shall now show that, for any value of ψ, $\phi(t) \to 0$ as $t \to \infty$. Note that $\phi(t)$ is proportional to $\varepsilon_4(t)$. Now,

$$\varepsilon_1(t) = \mathrm{CLK}(t)\cdot r(t) = \sqrt{2}A \sin\left(\omega_0 t+\theta\right) \sqrt{2}B \sin\left(\omega_0 t +\hat{\theta}\right) \tag{2}$$

or

$$\varepsilon_1(t) = AB \sin (\theta-\hat{\theta}) \tag{3}$$

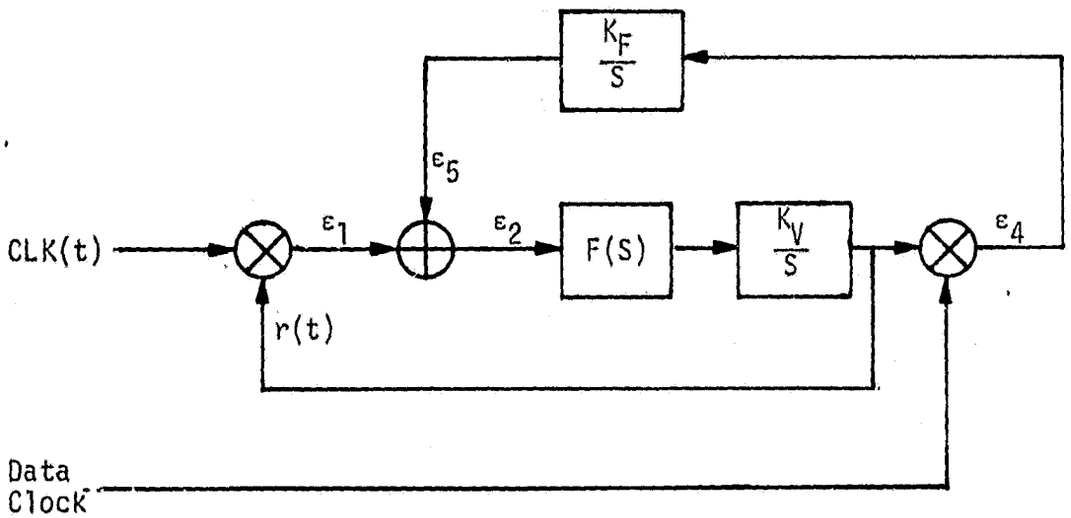
where we have neglected the $2\omega_0$ term which will be filtered out by the loop filter and VCO. Now,

$$\varepsilon_2(t) = AB \sin(\theta-\hat{\theta}) + \frac{K_F}{S} \varepsilon_4(t) \tag{4}$$

where

$$\frac{1}{S} \varepsilon_4(t) = \int_{-\infty}^{t} \varepsilon_4(u)\, du \tag{5}$$

with S being the Heaviside operator. We use the Heaviside operator notation in what follows. Now we have



$$CLK(t) = \sqrt{2}\, A \sin(\omega_0 t + \theta)$$

$$r(t) = \sqrt{2}\, B \cos(\omega_0 t + \hat{\theta})$$

$$DCLK(t) = \sqrt{2}\, A \sin(\omega_0 t + \theta + \psi)$$

Figure 8. Simplified, Linearized Model of the Bit Synchronizer

$$\varepsilon_4(t) = r(t)\cdot DCLK(t) = \sqrt{2}B\cos(\omega_0 t+\hat{\theta})\ \sqrt{2}A\sin(\omega_0 t+\theta+\psi) \quad (6)$$

or

$$\varepsilon_4(t) = AB\sin(\theta+\psi-\hat{\theta}) = AB\sin\phi \quad (7)$$

If we linearize (3) and (7), we obtain

$$\varepsilon_1(t) = AB(\theta-\hat{\theta}) \quad (8)$$

$$\varepsilon_4(t) = AB(\theta-\hat{\theta}+\psi) = \varepsilon_1(t) + AB\psi \quad (9)$$

Now we can also linearize (4) to yield

$$\varepsilon_2(t) = AB(\theta-\hat{\theta}) + \frac{K_F}{S}AB\phi \quad (10)$$

The phase estimate out of the VCO, $\hat{\theta}(t)$, in Heaviside operator notation is given by

$$\hat{\theta} = F(S)\frac{K_V}{S}\varepsilon_2 = F(S)\frac{K_V}{S}\left\{AB(\theta-\hat{\theta}) + \frac{K_V}{S}AB\phi\right\} \quad (11)$$

where F(S) is the loop filter represented as a function of the LaPlace variable S. Now, $\hat{\theta}$ also satisfies, from (1),

$$\hat{\theta} = \theta + \psi - \phi \quad (12)$$

so that

$$\theta + \psi - \phi = F(S)\frac{K_V}{S}\left\{AB(\theta-\psi) + \frac{K_F}{S}AB\phi\right\} \quad (13)$$

Since θ is unimportant in our analysis, we can let it be zero, producing from (13)

$$\Phi(S) = \frac{\left(1 + \frac{ABK_V F(S)}{S}\right)\Psi(S)}{\left[\frac{ABK_V F(S)}{S} + \frac{ABK_V K_F F(S)}{S^2} + 1\right]} \quad (14)$$

where $\Psi(S)$ is the LaPlace transform of $\psi(t)$, i.e.,

$$\Psi(S) = \mathscr{L}\{\psi(t)\} \tag{15}$$

and $\Phi(S)$ is the LaPlace transform

$$\Phi(S) = \mathscr{L}\{\phi(t)\} \tag{16}$$

In order to evaluate how well the loop samples the midpoint of the bit, we must consider the phase error, $\phi(t)$, as time increases without bound. Letting the $\Psi(S)$ be modeled as a phase step in time so that

$$\Psi(S) = \frac{\psi_0}{S} \quad , \tag{17}$$

where ψ_0 is a uniform random variable taking on values in the range $(-\pi, \pi)$ and using the final value theorem of LaPlace transforms, we have

$$\lim_{t\to\infty} \phi(t) = \lim_{S\to 0} [S\Phi(S)] \tag{18}$$

Hence, using (17) and (18) produces

$$\lim_{t\to\infty} \phi(t) = \lim_{S\to 0} \left[\frac{\left(1 + \frac{ABK_V F(S)}{S}\right) \psi_0}{\frac{ABK_V F(S)}{S} + \frac{ABK_V K_F F(S)}{S^2} + 1} \right] \tag{19}$$

Assuming a second-order loop requires that the loop filter be of the form

$$F(S) = \frac{1 + \tau_2 S}{\tau_1 S} \tag{20}$$

so that (19) can be evaluated as

$$\lim_{t\to\infty} \phi(t) = 0 \quad , \quad |K_F| > 0 \tag{21}$$

which means that, in our simplified and unquantized model, the data samples are always taken midbit, as desired, irrespective of the phase relationship between the clock and the data. It should be noted that, if θ were not zero, the result of (21) would still hold. It is interesting to consider the tracking error, $\phi(t)$, when the feedback integrator is removed, corresponding to $K_F = 0$. In this case, we find that

$$\lim_{t\to\infty} \phi(t) = \lim_{S\to 0} \left[\frac{\psi_0 \left[S^2 + ABK \frac{(1+\tau_2 S)}{\tau_1} \right]}{\frac{ABK_V}{\tau_1}(1+\tau_2 S) + S^2} \right] = \psi_0 \tag{22}$$

Therefore, without the integrator (or accumulator up/down counter), the bit synchronizer is incapable of controlling the location of the data bit samples. This fact satifies one's intuition.

We now establish that, while $\varepsilon_2(t)\to 0$ as $t\to\infty$, neither $\varepsilon_5(t)$ nor $\varepsilon_1(t)$ approach zero as $t\to\infty$. From Figure 8, it is obvious that

$$\varepsilon_5(t) = \frac{K_F}{S}\varepsilon_4(t) \cong \frac{K_F}{S} AB(\theta+\psi-\hat{\theta}) \tag{23}$$

Also, the oscillator output phase estimate is given by [using (11) and (23)]

$$\hat{\theta} = F(S)\frac{K_V}{S}\left\{AB(\theta-\hat{\theta}) + \varepsilon_5\right\} \tag{24}$$

Rearranging, we obtain

$$\hat{\theta} + \frac{ABK_V F(S)}{S}\hat{\theta} = AB\frac{K_V}{S}F(S)\theta + \frac{K_V}{S}F(S)\,\varepsilon_5 \tag{25}$$

Solving (25) for $\hat{\theta}$, we obtain

$$\hat{\theta} = \frac{\frac{AK_V}{S} F(S)\ \theta(S) + \frac{K_V}{S} F(S)\ \varepsilon_5(S)}{\left[1 + \frac{ABK_V F(S)}{S}\right]} \tag{26}$$

Rearranging (23) produces

$$\varepsilon_5 = \frac{ABK_F}{S} (\theta(S) + \Psi(S)) - \frac{ABK_F}{S} \hat{\theta} \tag{27}$$

Using (27) in (26) produces, after some algebra, the result (again letting $\theta = 0$)

$$\varepsilon_5(S) = \frac{\frac{ABK_F}{S} \Psi(S)}{\left[1 + \frac{ABK_F K_V F(S)/S^2}{1 + ABK_V F(S)/S}\right]} \tag{28}$$

Again using the final value theorem, we obtain

$$\lim_{t\to\infty} \varepsilon_5(t) = \lim_{S\to 0} \left[S\varepsilon_5(S)\right] \tag{29}$$

so that, assuming $\psi(t)$ is a step in phase of ψ_0 rad, we have, using (28) and the fact that $\Psi(S) = \psi_0/S$, that

$$\lim_{t\to\infty} \varepsilon_5(t) = AB\psi_0 \tag{30}$$

It can be shown that (30) also holds for a first-order loop (where F(S)=1) and it also holds for a step in phase of θ.

Now consider the steady-state value of $\varepsilon_1(t)$. We use linearized equations in the following. From (8), we have

$$\varepsilon_1 = AB(\theta - \hat{\theta}) \tag{31}$$

and from (10) we have

$$\varepsilon_2 = AB(\theta-\hat{\theta}) + \frac{K_F}{S}\varepsilon_4 \tag{32}$$

Also from (9), we have

$$\varepsilon_4 = \varepsilon_1 + AB\psi \tag{33}$$

Now, since

$$\hat{\theta} = \frac{K_V}{S}F(S)\,\varepsilon_2 = F(S)\,\frac{K_V}{S}\left[\varepsilon_1 + \frac{K_F}{S}\varepsilon_4\right] \tag{34}$$

we can use (33) in (34) to yield

$$\hat{\theta} = F(S)\,\frac{K_V}{S}\left[\varepsilon_1 + \frac{K_F}{S}(\varepsilon_1 + AB\psi)\right] \tag{35}$$

From (31), we have

$$\hat{\theta} = \theta - \frac{\varepsilon_1}{AB} \tag{36}$$

Now equating (36) and (35) produces (letting $\theta = 0$)

$$\varepsilon_1(S) = \frac{-\dfrac{ABK_VK_F}{S^2}\,\Psi(S)}{\left[\dfrac{K_VF(S)}{S} + \dfrac{K_VK_F}{S^2} + \dfrac{1}{AB}\right]} \tag{37}$$

Again assuming a step in the phase term $\psi(t)$ yields

$$\varepsilon_1(S) = \frac{-\frac{ABK_VK_F}{S^2}\frac{\psi_0}{S}}{\left[\frac{K_VF(S)}{S} + \frac{K_VK_F}{S^2} + \frac{1}{AB}\right]} \tag{38}$$

using

$$\lim_{t\to\infty} \varepsilon_1(t) = \lim_{S\to 0} S\varepsilon(S) \tag{39}$$

produces

$$\lim_{t\to\infty} \varepsilon_1(t) = -AB\psi_0 \tag{40}$$

From (30) and (40) and Figure 8, we deduce that $\varepsilon_2(t)\to 0$. Therefore, when tracking, the bit synchronizer operates in such a manner that $\varepsilon_2(t) \cong 0$ and $\varepsilon_1(t) \cong -\varepsilon_5(t)$. Without the feedback, of course, the loop would drive $\varepsilon_1(t) \cong 0$.

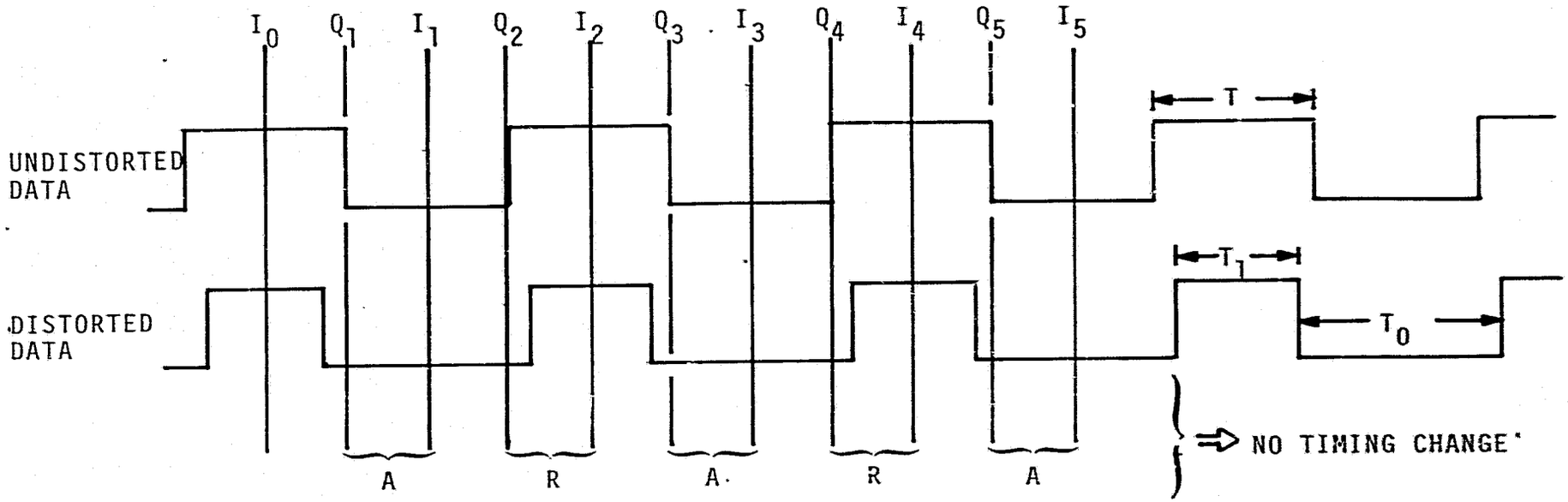
6.0 THE EFFECTS OF ASYMMETRY ON BIT DETECTION

In this section, we address the problem of bit asymmetry on both synchronization and bit demodulation. Bit asymmetry percentage is defined by

$$ASY = \frac{|T_1 - T_0|}{T_1 + T_0} \times 100\% \tag{41}$$

where T_1 is the bit duration of a "one" when preceded and followed by a zero, and T_0 is the bit duration of a "zero" when preceded and followed by a one. It is predicted that the total asymmetry due to rise time and transmitted asymmetry will be in the region of 25-35% when the bit rate is at 50 Mbps.

In Figures 9a-c, the case of 25% asymmetry is shown for an alternating one/zero sequence, running at 50 Mbps, with three distinct timing error regions. Since T_1 = 15 ns and T_0 = 25 ns, we see that, in



Bit Synchronizer Timing Error Circuit Legend:

A = advance timing (increase VCO frequency)

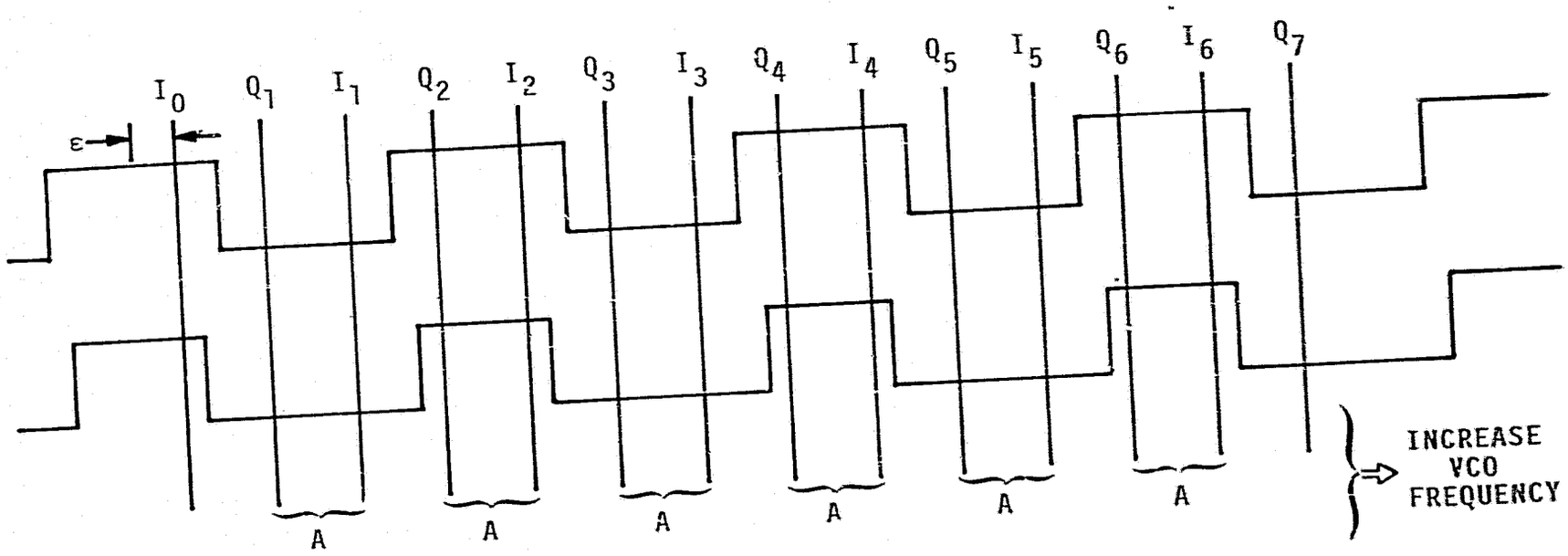
R = retard timing (lower VCO frequency)

INH = inhibit accumulator (don't change VCO frequency)

R_b = 50 Mbps

CONCLUSION: With timing errors up to ±2.5 ns, no timing change, and bits are correctly detected.

Figure 9a. One/Zero Bit Sequence with 25% Asymmetry and 0 to ±2.5 ns Timing Error



Bit Synchronizer Timing Error Circuit Legend:

A = advance timing (increase VCO frequency)

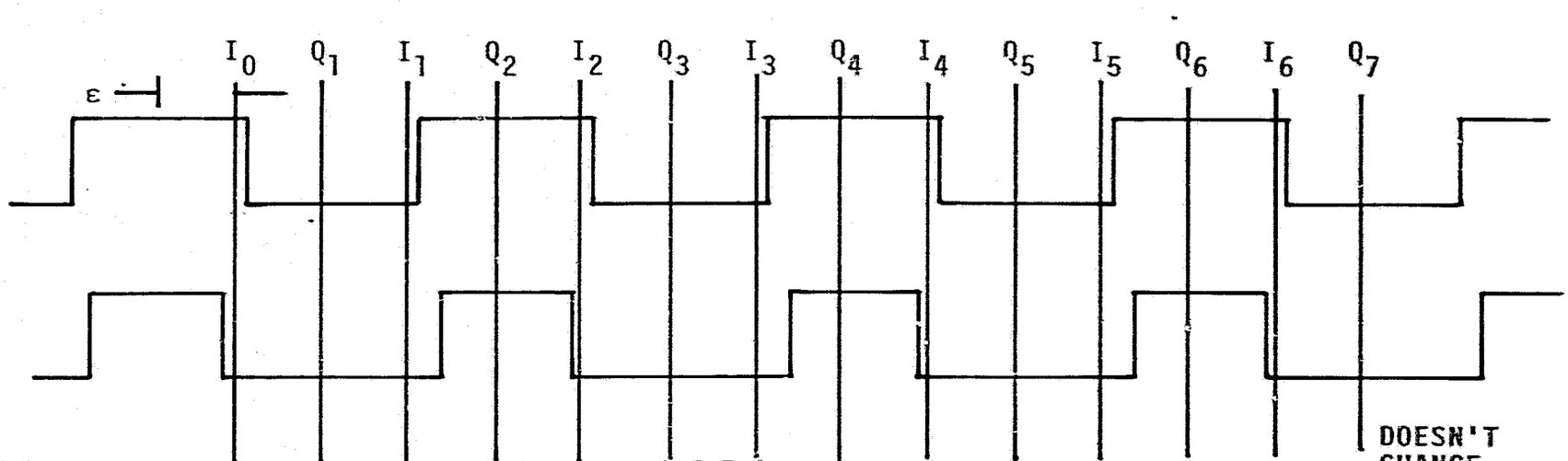
R = retard timing (lower VCO frequency)

INH = inhibit accumulator (don't change VCO frequency)

R_b = 50 Mbps

CONCLUSION: With timing errors in the region ±2.5 ns to ±7.5 ns, the loop reduces the timing error and correctly detects the bits.

Figure 9b. One/Zero Bit Sequence with 25% Asymmetry and ±2.5 to ±7.5 ns Timing Error



INH = INHIBIT

Bit Synchronizer Timing Error Circuit Legend:

A = advance timing (increase VCO frequency)
R = retard timing (lower VCO frequency)
INH = inhibit accumulator (don't change VCO frequency)
R_b = 50 Mbps

CONCLUSION: With timing errors in the region ±7.5 ns to ±10 ns, the loop does <u>not</u> change its timing but it does incorrectly detect some bits (50% error rate for the square-wave data sequence).

Figure 9c. One/Zero Bit Sequence with 25% Asymmetry and ±7.5 to ±10 ns Timing Error.

fact, ASY=25%. For the vertical lines, the Q_1,I_1 pairs determine which way to adjust the phase of the VCO according to $I_n + Q_n = 0 \rightarrow$ ADVANCE (INCREASE VCO VOLTAGE) and $I_n + Q_n = 1 \rightarrow$ RETARD (DECREASE VCO VOLTAGE) when $I_n + I_{n-1} = 1$, and no bit timing change when $I_n + I_{n1} = 0$. For example, in Figure 9a, region I errors are illustrated. For this timing relationship, the input to the accumulator up/down counter would be the sequence advance (A), retard (R), advance (A), etc. or, equivalently, ones and minus ones to the accumulator which would not change the sample points relative to the bit stream. In Figure 9b, the error is ±5 ns, which produces a sequence of advances. In this region (±2.5-±7.5 ns), the loop would pull in to the ±2.5 ns region and correctly decode the data bits. When a shift of 8 ns (7.5-10 ns) is considered in Figure 9c, we find that there would be a sequence of A's and R's which would not reduce the error but would cause bit errors to be made in the bit sampling process. For the case of alternating one/zero shown, the detected bits are all zeros, resulting in errors on every other bit. By carefully considering Figures 9a-c, it can be concluded that, with 25% asymmetry, the following is true (timing error is defined as timing difference between sampling at the center of the bits and the actual sampling point):

1. With timing errors up to ±2.5 ns, no timing change is effected by the loop and no bit errors are made.

2. With timing errors between ±2.5 ns and ±7.5 ns, loop error control will reduce timing error and no bit errors will occur.

3. With timing errors between ±7.5 ns and ±10 ns, the loop will not adjust the timing, but bit errors will occur.

The case of 35% bit asymmetry is illustrated in Figure 10 for an alternating one-zero sequence. After careful study, we conclude that the following is true:

1. With timing errors up to ±3.5 ns, no timing change is effected by the loop and no bit errors are made.

2. With timing errors between ±3.5 ns and ±6.5 ns, loop error control will reduce the timing error and no bit errors will occur.

3. With timing errors between ±6.5 ns and ±10 ns, the loop will not adjust timing, however, bit errors will occur.

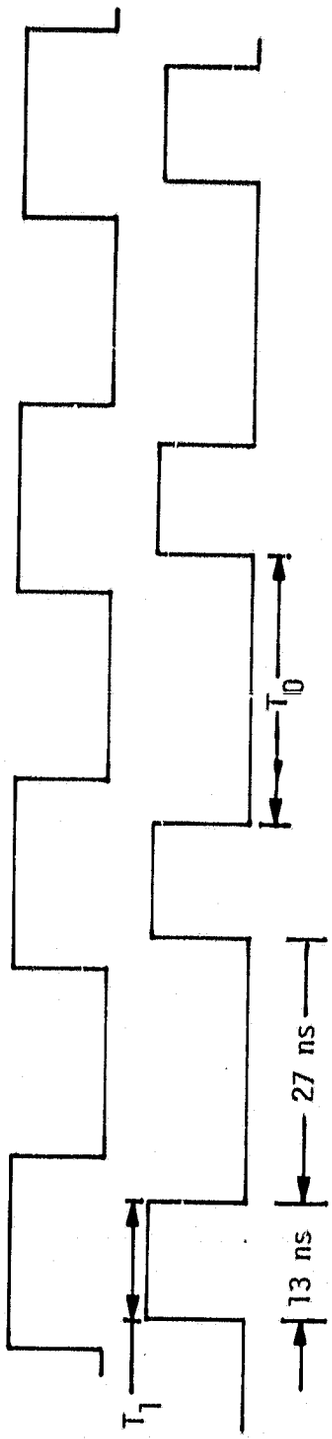


Figure 10. One/Zero Sequence With 35% Asymmetry

Sequences other than the one-zero alternating sequence were considered and the result was basically the same for any level of asymmetry.

In conclusion, we see that three "zones" or timing error regions will apply. The first region is a dead zone in the sense that the no-error control signal is generated in the accumulator because the error signals alternate back and forth in algebraic sign. This region extends in magnitude from zero timing error to $\frac{ASY \cdot T}{2}$ seconds, where T is the undistorted bit symbol duration. The bits are correctly detected in this region.

The second region extends from $\frac{ASY \cdot T}{2}$ seconds to $\left(\frac{1-ASY}{2}\right)T$ seconds. In this region, the loop provides an error control signal from the bit timing error detector which reduces the error to the outer edge of zone 1. The bits are correctly detected in this region.

In the third zone, the error ranges from $\left(\frac{1-ASY}{2}\right)T$ seconds to T/2 seconds. This region causes the bit timing error detector to produce a sequence of alternating ones and minus ones which will therefore not exceed the accumulator threshold and, consequently, not update the loop (i.e., a quasistable lock point). Bit errors will occur in this region. When the one-zero sequence is considered, only zeros or all ones will be detected depending on whether the one bits or the zero bits are of greater duration due to asymmetry. For arbitrary sequences of ones and zeros, errors will occur although not at a 50% rate.

As a final comment, if we assume that the a priori probability of the initial timing just after acquistion is uniformly distributed, the probability of locking in the third region, where bit errors occur, is given by

$$P_{FL} = \frac{\frac{T}{2} - \left(1 - ASY\right)\frac{T}{2}}{\frac{T}{2}} = ASY$$

and therefore, only with zero asymmetry does this problem disappear. If the timing error between clock and bit stream could be held to be less than $\left(\frac{1-ASY}{2}\right)T$ seconds in magnitude, it is possible to avoid the troublesome third region.

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