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MIL-M-38510/470 TEST VECTORS: FAULT DETECTION EFFICIENCY MEASUREMENT VIA HARDWARE FAULT SIMULATION

FINAL REPORT

BY

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PREFACE

The work described in this report was performed by Timoc International Co. during the period between November 1979 and March 1980. The work was performed for JPL under contract number 955502. Messrs. C.M. Hess and R.W. Scott from JPL LSI Parts Group provided technical direction and engineering management.

ABSTRACT

The overall objective of this program is to provide the means for testing microprocessors so as to assure nearly fault-free operation. A more specific objective is to measure the stuck fault detection efficiency of the test vectors developed by JPL/Hughes for the MIL-M-38510/470 NASA.

A hardware stuck fault simulator for the 1802 microprocessor was implemented and the stuck fault detection efficiency of the test vectors developed by JPL/Hughes for the MIL-M-38510/470 NASA were measured in three phases as follows:

Phase 1. Build a breadboard system to perform the fault-free function of the 1802.

Phase 2. Add fault simulation capabilities to the fault-free breadboard.

Phase 3. Measure the stuck fault detection efficiency of the test vectors

A total of 874 faults were injected into the combinatorial and sequencial parts of the RCA 1802 microprocessor and it was found that 39 stuck faults were not detected. Therefore, the measured stuck fault detection efficiency of the MIL-M-38510/470 NASA is 95%. Since the 39 undetected faults can create catastrophic errors in equipment designed for high reliability applications, it is recommended that the MIL-M-38510/470 NASA be enhanced with additional test vectors so as to achieve 100% stuck fault detection efficiency.

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1. INTRODUCTION

Fault detection in microprocessors can be accomplished by manually or automatically developed test vectors. An optimum set of test vector should detect 100% of all faults with a minimum number of vectors. In order to measure the fault detection efficiency of a test set (i.e., percent of faults detected) it is necessary to perform fault simulation of the microprocessor.

Automatic fault simulation can be accomplished either by software or hardware. One of the major problems with state-of-the-art software fault simulators is their relatively low speed. If we compare the speed of the software fault simulators to the actual speed of a microprocessor we will find software fault simulation approximately 10^5 to 10^{10} times slower than the real microprocessor. It is not unusual to expect in excess of 100 hours of continuous fault simulation on a large main frame computer, assuming a test program consisting of 100,000 test vectors.

Fault simulation can also be implemented into hardware [References 1 and 2]. Stuck faults at the inputs and outputs of logical gates can be injected by means of special circuitry. The hardware fault simulator for the RCA 1802 microprocessor reported herein was developed to measure the fault detection efficiency of the MIL-M-38510-470 test vectors. Practical results show that a hardware fault simulator can be approximately two orders of magnitude more cost effective than software fault simulators.

A hardware fault simulator for a microprocessor component can be implemented in two phases. First, a breadboard of the microprocessor is built from the gate level logic diagram of the component. Since the local memory and registers can be thoroughly tested without any requirements for fault simulation, no provision for fault injection should be made for said memory and registers. The remaining logic is implemented with elementary gates and latches. Next, using additional circuits to inject faults at the pins of these chips we can actually inject faults at the inputs and outputs of elementary gates and latches.

Assuming a set of test vectors developed to test a microprocessor, the fault detection efficiency of the test vectors can be measured with a hardware fault simulator connected to a VLSI tester. With the fault simulator plugged

into the tester head, a fault is injected into the hardware fault simulator and the entire test set is being applied to the fault simulator that looks as if it were just another bad chip. The fault detection efficiency of the test set is calculated by dividing the number of faults detected by the total number of faults simulated.

2. TECHNICAL DISCUSSION

2.1 Hardware Fault Simulation

A hardware fault simulator for an AND gate with primary inputs X1 and X2, is shown in Fig. 1. The only faults necessary to be injected are input X1 stuck-at-one (X1-1), input X2 stuck-at-one (X2-1), and input X1 or X2 stuck-at-zero (X1-0, X2-0). The circuit shown in Fig. 1 is capable of simulating a good two-input AND gate and any of the single stuck faults associated with an AND gate as follows.

To simulate the behavior of a good two-input AND gate the serial-in and parallel-out shift register should contain all "0"s in its three shift register latches (SRL1 through SRL3). To simulate X1-1 (Z-1, a "1" is stored in SRL1 and "0"s are stored in SRL2 and SRL3. As it can be seen a "1" from SRL1 will permanently force a stuck-at-one at input X1. In the same manner, X2-1, Z-0, and Z-1 can be simulated by shifting a "1" preceded and followed by "0"s. The fault simulator shown in Fig. 1 requires an SRL and a two-input OR or NOR gate for each fault injector. Moreover, the signal from X1 to Z and X2 to Z is delayed by one and two gates, respectively, in addition to the original AND gate.

It is worth noting that the fault simulator depicted in Fig. 1 is capable of simulating single and multiple stuck faults by storing the appropriate logic values in the shift register.

2.2 Hardware Fault Simulator for the RCA 1802

The implementation of a hardware fault simulator for a commercially available microprocessor is described next. A block diagram of the RCA 1802 microprocessor is shown in Fig. 2, comprising four major parts

(a) Timing unit.

(b) Control unit.

(c) Execution (E) unit.

(d) Instruction (I) unit.

The implementation into hardware of the fault simulator for the RCA 1802 microprocessor and the measurement of fault detection efficiency of the test vectors was accomplished in three phases as follows:

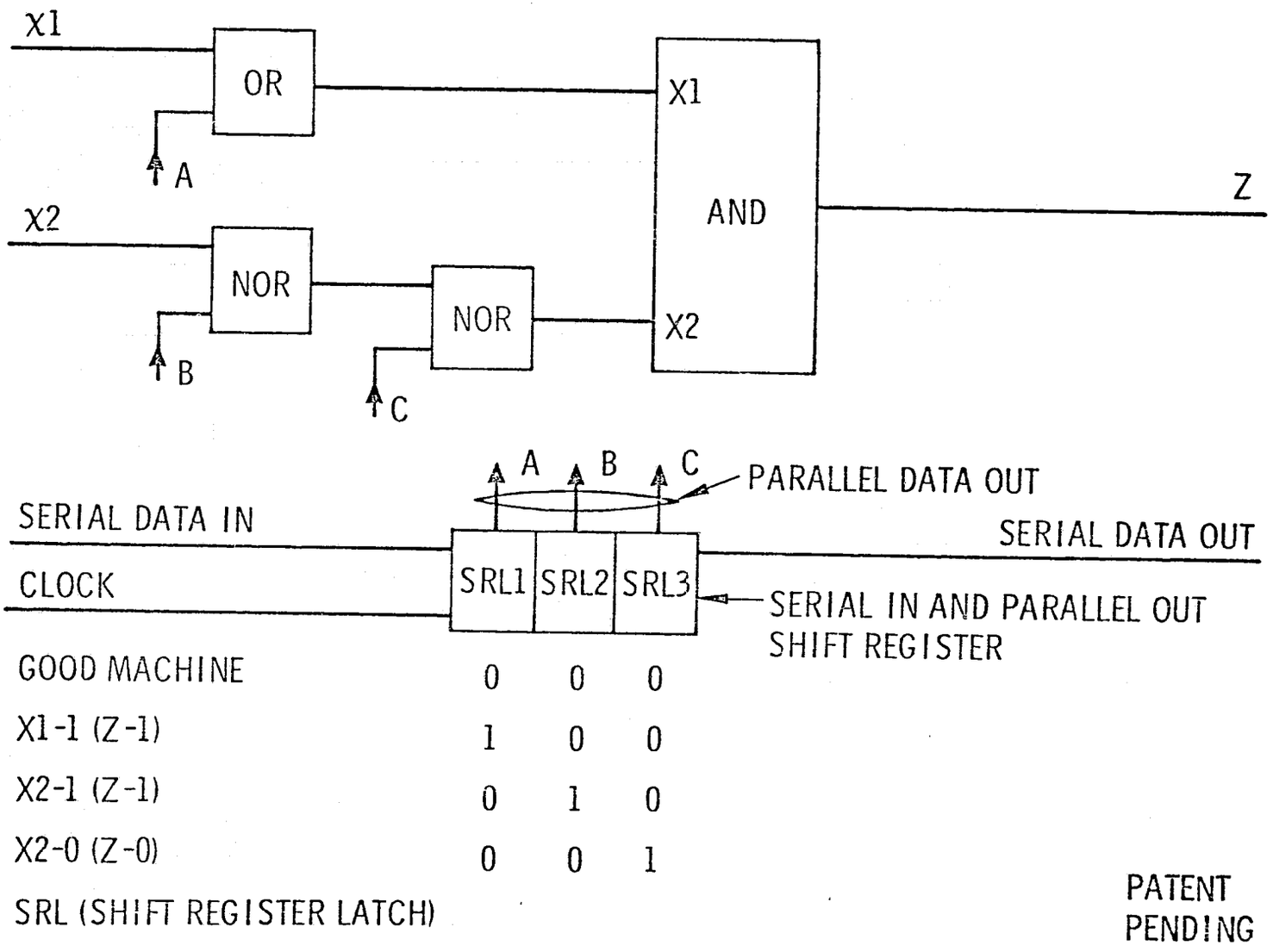

Fig. 1. Hardware Fault Simulator For an AND Gate

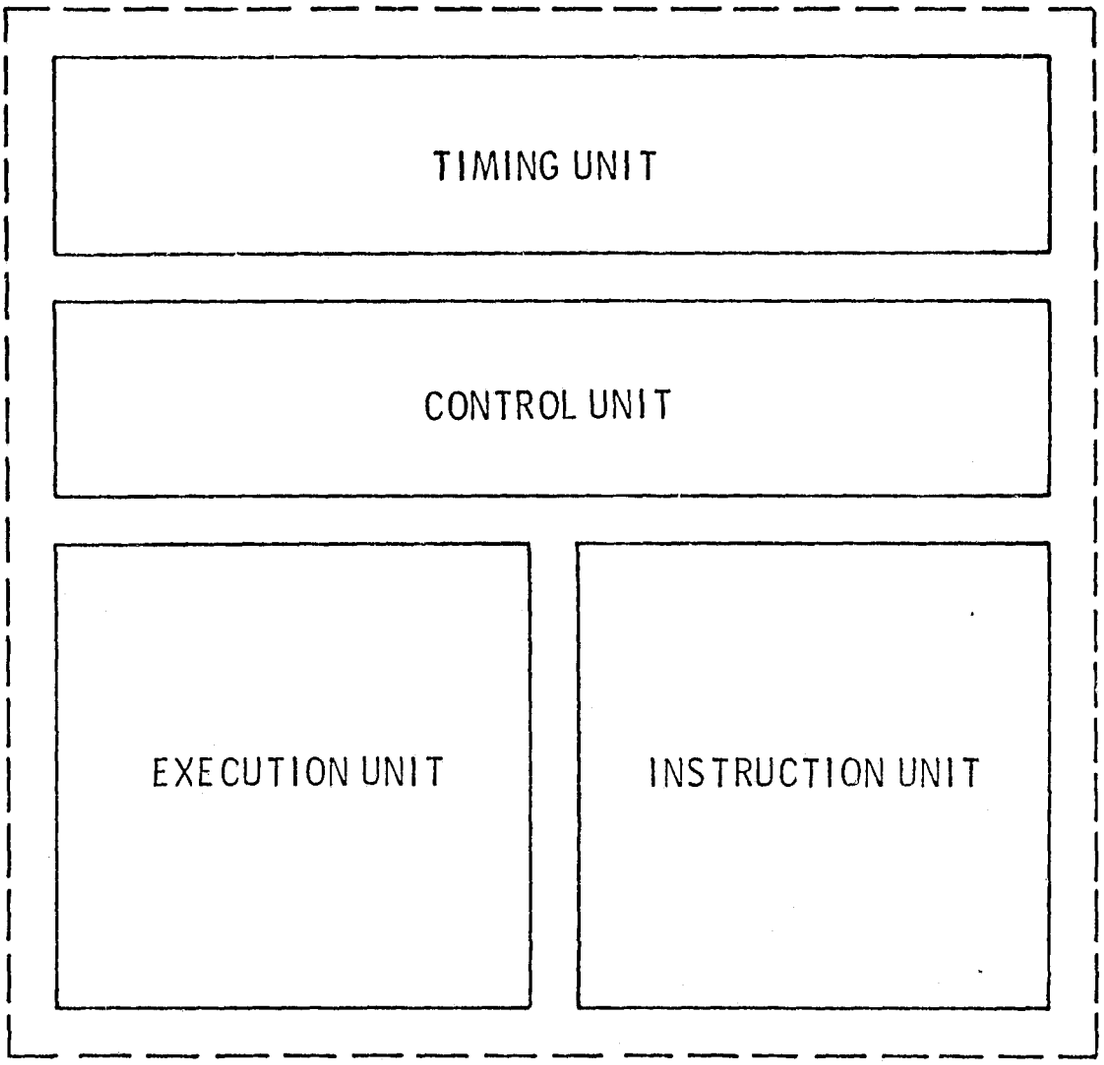

Fig. 2. RCA 1802 Microprocessor Block Diagram

Phase 1

The objective of this phase was to build a breadboard system that performs the fault-free function of the RCA 1802. Each subsystem (e.g., shift register, decoder, etc.) will be implemented on a wire-wrap board using standard CMOS chips. The fault simulation capability was not provided in this phase in order to simplify the implementation of a correct fault-free system. Each wirewrap board was tested separately to ensure that it perform its specified function. (Functional testing of each board is possible because of the known simple function that each board must perform.) The fault-free breadboard was tested on the COSMAC development system. Complete testing of the fault-free board was

accomplished with an LSI tester. The registers and the register array are implemented with MSI CMOS chips while the rest of the microprocessor logic is implemented using only SSI chips (i.e., simple gates and D-latches).

The registers and the register array were tested by using a GALPAT set of vectors. Therefore, no stuck faults were simulated for the registers and the register array. However, the function of the remaining part of the microprocessor is implemented with SSI chips that perform elementary logic functions and D-latches. Thus, by injecting single stuck faults at the pins of these chips we actually inject faults at the input and output of elementary gates and D-latches.

Phase 2

The objective of this phase was to add fault simulation capabilities to the fault-free breadboard built in Phase 1. This is being accomplished by replacing each elementary gate and latch chip by its corresponding fault injection module. Each fault injection module is implemented following the concept of hardware fault simulation described in Fig. 1. When all gates and latch chips were replaced by the appropriate fault injection modules, then the shift registers of the fault injection modules were cascaded, thus forming a long shift register. Therefore, by storing a "1" in the appropriate position of the shift register, a particular gate or latch input is selected and the appropriate stuck fault is simulated (Fig. 3).

The hardware fault simulator was first tested on the COSMAC development system. Complete testing of the fault simulator was accomplished with an LSI tester during the measurement of stuck fault detection efficiency of the test vectors.

The hardware fault simulator of the RCA 1802 microprocessor described above required approximately 800 standard commercially available chips. The number of fault injection points is 874.

Phase 3

The objective of this phase was to measure the stuck fault detection efficiency of the test vectors developed for MIL-M-38510/470 NASA.

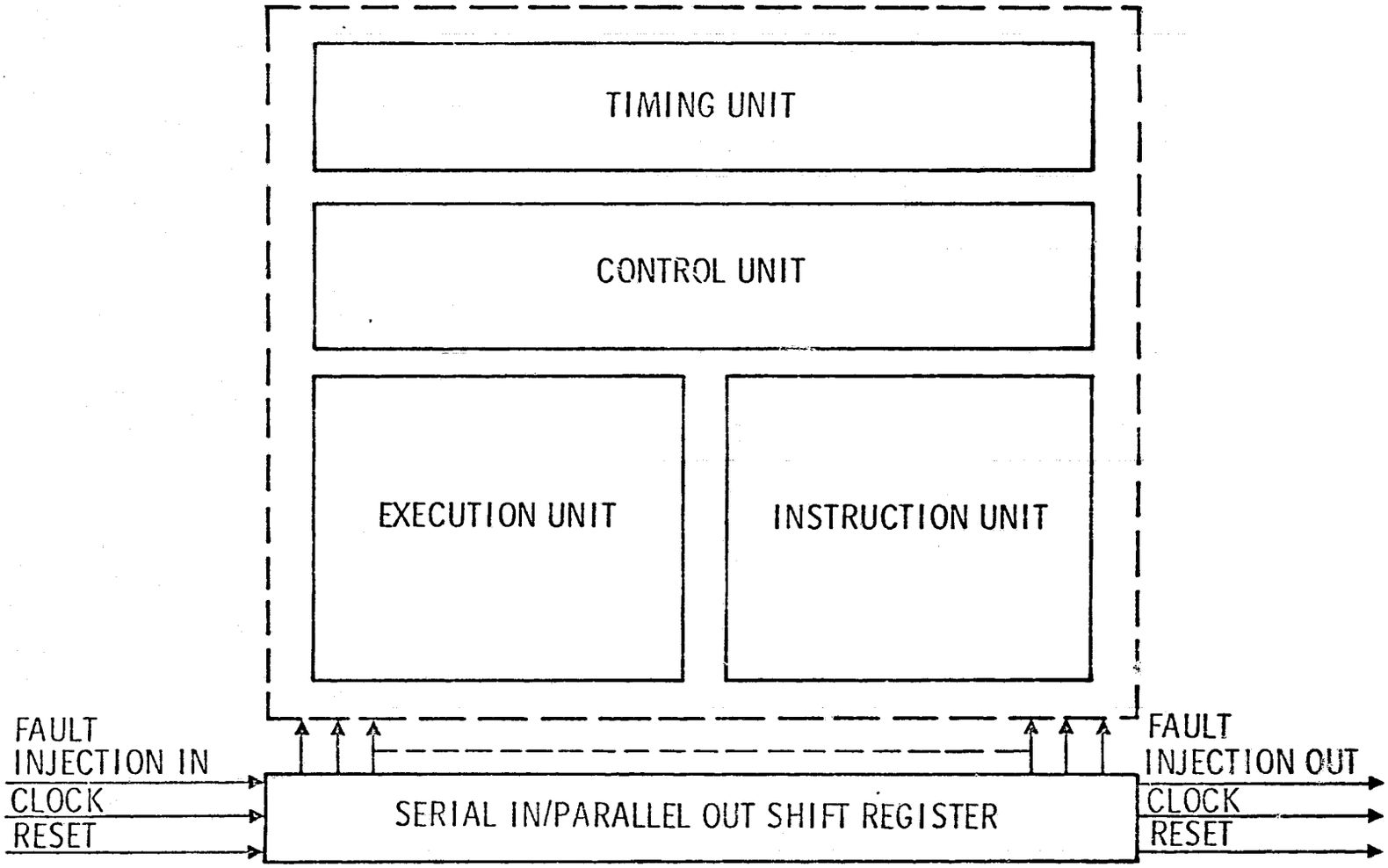

Fig. 3. Hardware Fault Simulator for RCA 1802 Microprocessor

With the hardware fault simulator plugged into the test head of the LSI tester, the fault detection efficiency of the test vectors was measured as follows (Fig. 4):

A fault list with 874 faults that represents the total number of stuck faults in the 1802 was prepared first.

Step 1: Select one fault from the fault list and simulate it by storing the appropriate pattern into the fault injection shift register.

Step 2: Apply all test patterns to determine whether or not the fault simulated in Step 1 is detected . If the tester signals NOGO then the fault is detected, else is not detected.

Step 3: Repeat steps 1 and 2 until all faults were simulated.

Step 4: Calculate the fault detection efficiency by dividing the number of detected faults by the total number of faults in the fault list.

2.3 Fault Simulation Results

The hardware fault simulator for the RCA 1802 microprocessor is capable of automatically injecting a fault at the input and output of any gate of the combinatorial and sequential logic. Since the registers are tested with a specialized test set, no provisions were made to inject faults in the registers. A

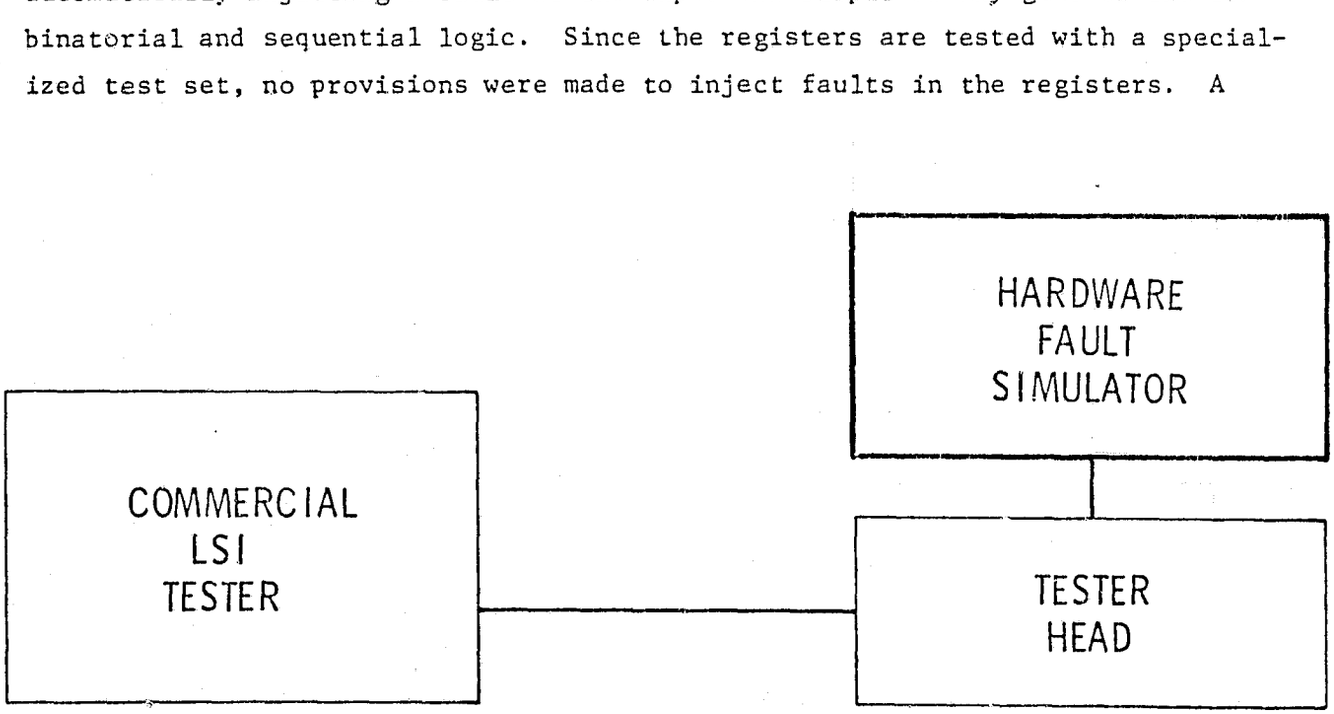

Fig. 4. Measurement of MIL-M-38510/470 NASA Test Vectors Stuck Fault Detection Efficiency with a Commercial Tester and a Hardware Fault Simulator.

total of 874 necessary and sufficient single stuck faults were injected of which 29 were not detected (see Chapter 7, Supporting Data). Therefore, the stuck fault detection efficiency of the MIL-M-38510/470 NASA was measured at 95%. A detailed description of fault simulation results at unit level is presented in Table 1.

The Arithmetic and Logic Unit (ALU) is a combinatorial network that required a total of 130 faults to be injected. Since the ALU is commonly used in most of the microprocessor operations only 3 faults remained undetected. In other words, 95% of the faults were detected. Although the number of undetected faults is only 3, it is worth analyzing their impact on the function of the microprocessor

Table 1. Fault Simulation Summary

UNIT	NUMBER OF FAULTS INJECTED	NUMBER OF FAULTS UNDECTED	PERCENT OF FAULTS DETECTED	UNDETECTED FAULTS
ALU	130	3	97.6	683, 724, 729
INC/DEC	105	7	93.3	773, 782, 805, 808, 838, 823, 828
STATE LOGIC	63	4	93.6	63, 88, 91, 95
DECODER	311	12	96.1	149, 169, 190, 355, 384, 388 396, 426, 427, 441, 443, 454
SEQUENCER	181	12	93.3	459, 466, 489, 524, 525, 531, 558, 559, 565, 634, 635, 636
CONDITION TEST LOGIC TOTAL	84	1	98.8	139
TOTAL	874	39	95.5	

if a real chip would have passed final testing with at least one of these faults going undetected. Let us take for example fault 729 which is a stuck-at-zero at the input of a 8-input OR gate. A real chip with fault 729 would have had passed final testing unnoticed since the MIL-M-38510/470 NASA test vectors are not capable of detecting this fault. However such a "good" chip due to the presence of fault 729 would have taken a jump on condition accumulator equal zero even though the content of the accumulator was 2, thus non-zero. Specifically, the instructions affected would have been SHORT BRANCH IF D = 0 (BZ;32), LONG BRANCH IF D = 0 (LBZ;C2), and LONG SKIP IF D = 0 (LSZ;CE). Therefore, here is an example of one fault (i.e., 729) that can cause catastrophic errors in a system since it is not detected at final testing.

The incrementer/decrementer is a unit that increments or decrements the contents of the program counter, stack pointer, and data registers. The absolute number of undetected faults is 7 from 105 faults injected, yielding 93% of faults detected. At least 3 of the 7 undetected faults have catastrophic consequences should they exist on a real chip and thus passing unnoticed final testing. Any of the 3 catastrophic faults would make the RCA 1802 microprocessor fetch an instruction or data from a wrong address. For example, the undetected presence of fault 808 would cause an instruction or data to be fetched from the wrong hexadecimal address ØØ8Ø instead of the right address ØØCØ. Faults 805 and 838 would cause similar catastrophic errors.

The State Logic Unit is a sequential logic that together with the Decoder, the Sequencer and the Condition Test Logic form the Control Unit. The Static Logic determines one of the four possible major states of the microprocessor called S_0, S_1, S_2, and S_3. The microprocessor is forced to one of the four states by one of the following conditions: RESET, DMA, INTERRUPT, LOAD, and IDLE. A total of 63 faults were injected of which 4 are undetected yielding 93% of faults detected. Any one of these faults would cause catastrophic errors if it exited on a real chip. For example fault 88 would take the microprocessor from state S_1 (i.e., execute cycle) into the wrong state S_0 (i.e., fetch cycle) instead of state S_3 (i.e., interrupt cycle) for an appropriate sequence of requests. The remaining three faults have similar catastrophic effects.

The Decoder is a relatively large combinatorial network that decodes the operation code of each instruction. A total of 12 faults were found undetected from 311 injected resulting in 96% of faults detected. The existence of these

faults would affect the correct execution of a sequence of instructions. In other words, the presence of one of these faults would execute the correct sequence of instructions SETP, SAVE, RETURN as a faulty sequence SETP, SAVE, DISABLE. One possible fault that would cause a faulty behavior as described above would be fault 427.

The Sequencer faulty behavior would be analogous to that described above for the Decoder i.e., certain instruction sequences will be transformed by the faults into unwanted instruction sequences or meaningless sequences. Here again the percent of faults detected is 93% with a total number of 181 injected and 12 undetected.

The Condition Test Logic resulted in 99% faults detected with 84 injected and 1 undetected. Fault 139 would cause errors in the execution of SHORT BRANCH, instructions 34 through 37.

A frequency distribution of the detected faults is depicted in Fig. 5. On the horizontal axis are listed the pattern numbers while on the vertical axis is listed the frequency of occurrence of detected faults. One pattern contains approximately 1,000 vectors. Most of the faults are detected for the first time in pattern 1 while patterns 5 and 8 detect very few new faults. Since these results do not contain information about the faults detected in the register i' necessary to verify whether or not patterns 5 and 8 are directed toward testing the registers before deciding to eliminate them from the test set.

Another way of presenting the fault simulation results are in the form of a cumulative frequency distribution as shown in Fig. 6. More than 60% of the faults are detected in the first 2 patterns while patterns 3 through 9 detect only 15% new faults. Careful analysis of these results is required before a decision is made to compress the test vectors since some of the patterns that detect few stuck faults may be designed for testing the registers.

In summary, fault simulation results of the MIL-M-38510/470 NASA test vectors reveal that undetected faults can cause catastrophic system failures due to changes induced in single instructions, sequence of instructions, and addressing of instruction and data. Although the overall percent of faults detected appears quite high (i.e., 95%), the absolute number of undetected faults is also large (i.e., 39). Thus, to judge the quality of the test vectors only from the percent of faults detected point of view without consideration to the absolute number of faults, may lead to decisions with catastrophic consequences.

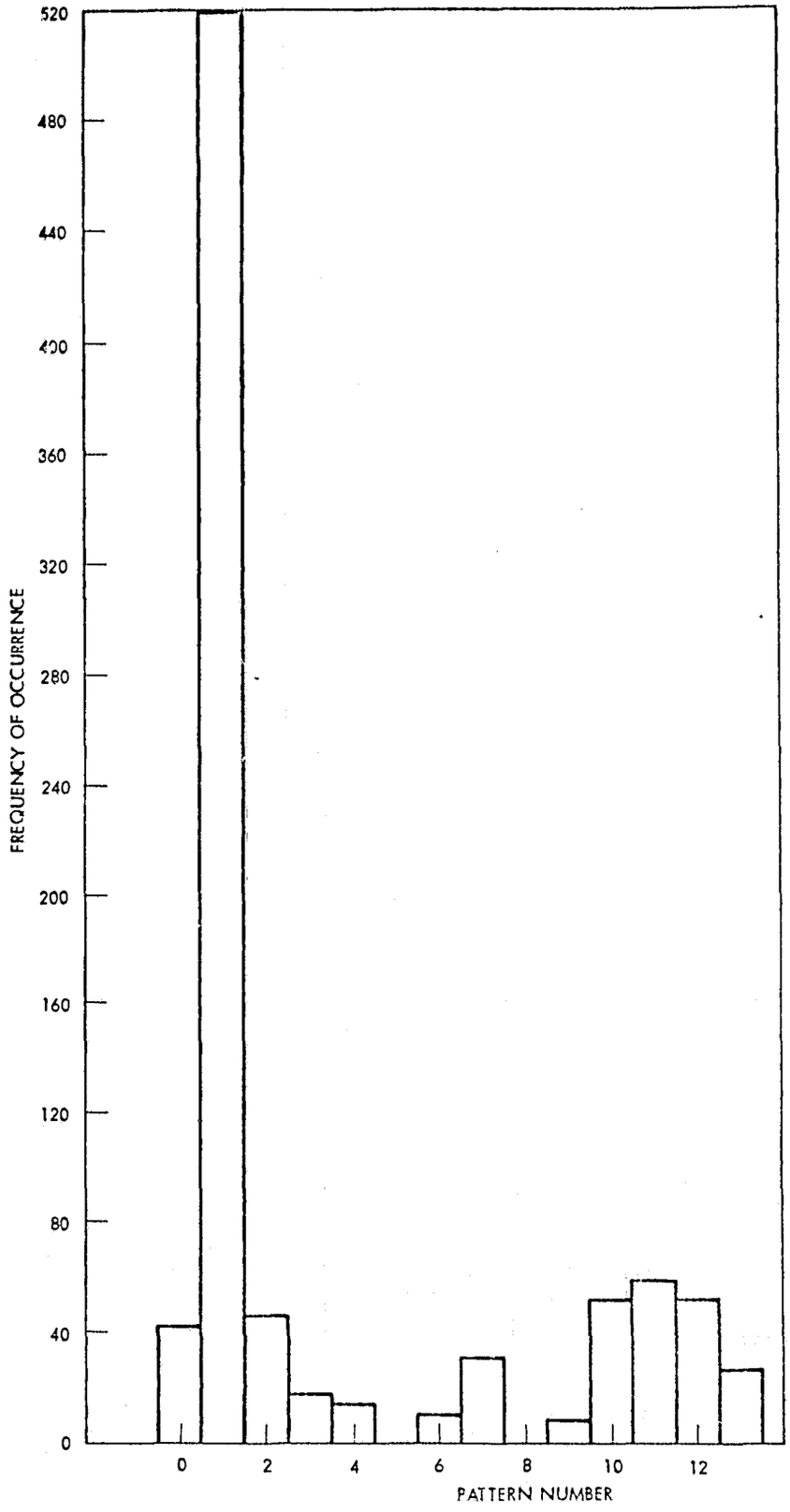

Fig. 5. Frequency Distribution of the Detected Faults. The number of detected faults is 835 and the total number of faults injected is 874.

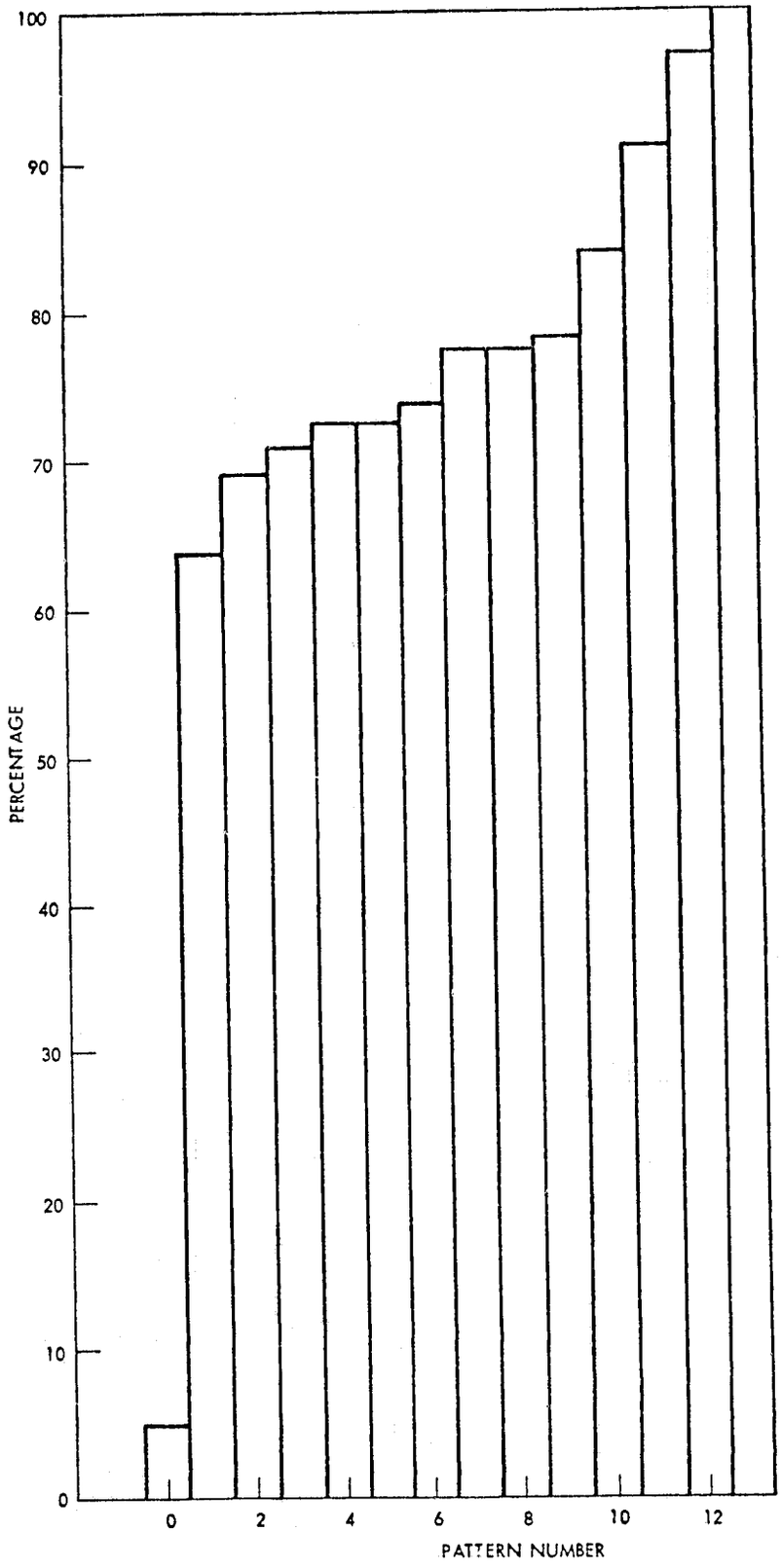

Figure 6. Cumulative Frequency Distribution of Detected Faults. The number of detected faults is 835 and the total number of faults injected is 874.

3. CONCLUSIONS

The purpose of this project was two fold: (1) to perform a measurement of the stuck fault detection efficiency of the MIL-M-38510/470 NASA test vectors and (2) to demonstrate the feasibility of fault simulating a microprocessor in hardware and determine whether or not hardware fault simulation is cost-effective.

Overall stuck fault detection efficiency of the MIL-M-38510/470 NASA test vectors is presently 95%, or in absolute numbers, 39 faults are undetected from 874 total necessary and sufficient single stuck faults simulated. It is shown in this report that although 95% faults detected may appear high, it is clearly insufficient for high reliability applications. The actual number that should also be used in characterizing the quality of test vectors is the absolute number of undetected faults. Most of the undetected faults would cause catastrophic system failures when present in a real chip. These failures affect single instructions, sequences of instructions, and absolute addresses of instructions and data.

Another benefit from the fault simulation described in this report is the possibility of reducing the number of vectors by eliminating those vectors that do not detect any new faults. It is shown that 65% of the faults are being detected in the first two patterns and only 15% of the new faults are being detected by the following five patterns. Therefore, the MIL-M-38510/470 NASA test vector may be compressed after a careful analysis so that compression does not have negative effect upon the detection of faults in the registers.

It has been shown that a fault simulator implemented entirely in hardware is feasible. The effort required to build the hardware fault simulator for the RCA 1802 is comparable to that of modeling the microprocessor for a software fault simulator. The verification and validation of the hardware fault simulator is much simpler than that of the software model since the logical behavior and structure in hardware form does not require any specialized and highly skilled people as it would be required for a software fault simulator. To operate the hardware fault simulator it is much simpler than to operate a software fault simulator. Moreover, the major advantage of the hardware fault simulator over its software counterpart is that a simulation run for all 874 faults takes one hour on a commercial LSI tester while a state-of-the-art software fault

simulator (e.g., D4-LASAR or TEGAS) would take in excess of 10 hours on a large computer. The availability and portability of the hardware fault simulator makes it convenient to use. Therefore, it is apparent from this work that hardware fault simulators are at least one order of magnitude and possible two orders of magnitude more cost-effective than software fault simulation.

4. RECOMMENDATIONS

In view of the intended applications for the RCA 1802 microprocessor the following improvements are recommended for the MIL-M-38510/470 NASA:

(a) Enhance the test vector set so as 100% of the faults will be detected. Here, one has to consider that certain faults are undetectable by any vectors due to redundancies in the logic design. Therefore, the enhanced test vector set should detect 100% of the detectable faults.

(b) Eliminate test vectors if upon analysis of the fault simulation results it is found that they do not detect any new faults in the logic and in the registers. The elimination process may not be required since the present vector set is only 14,000 vectors, however if the enhanced vector set exceeds approximately 100,000 vectors then the reduction may be cost-effective.

5. NEW TECHNOLOGY

The fault injection modules used to convert the breadboard into a fault simulator were invented and reduced to practice independently of the present contract [Reference 3]. The design of the fault injection modules is proprietary to Timoc International Company, and a patent application has been filed thereon. As stated in the proposal for this work, Timoc International Company has granted to JPL at the time of delivery of said fault injection modules a free and non-exclusive license for using the fault injection modules.

6. REFERENCES

1. Tsiang, S. H., and Ulrich, W., "Automatic Trouble Diagnosis of Complex Logic Circuits," The Bell Systems Technical Journal, Vol. XLI, No. 4, July, 1962.

2. Timoc, C. C., and Hess, L. M., "Fault Simulation: An Implementation into Hardware," 1979 Cherry Hill Test Conference, October, 1979.

3. Timoc, C. C., "Proposal for Hardware Fault Simulator for RCA 1802 Microprocessor," December, 1978.

7. SUPPORTING DATA

The following computer printout is being used as fault simulation data performed on the MIL-M-38510/470 NASA. On each line the fault number that was injected is listed as <fault number>. If the fault is recorded by the tester as PASSED that means that the fault is undetected and if it is listed as FAILED it was detected. The following 39 faults are undetected:

63, 88, 91, 95, 139, 149, 169, 190, 355, 384,
388, 396, 426, 441, 461, 443, 454, 459, 466, 489,
524, 525, 531, 558, 559, 565, 634, 635, 636, 683,
724, 729, 773, 782, 805, 808, 823, 828, 838.

Fault <0> means no faults injected or in other words this is a good machine.

1802 HARDWARE FAULT SIMULATOR DATE: 28 FEB 80 14:11:38

FUNCTIONAL TEST CONDITIONS

VCC	VDD	FREQUENCY	CLOCK Pw.
5.00 V	5.00 V	300. KHZ	1.67US

<0> PASSED

<1> FAILED IN PATTERN 0 AT VECTOR 12
FAILED PINS : MRD

<2> FAILED IN PATTERN B AT VECTOR 55
FAILED PINS : MA3 MA2 MRD

<3> FAILED IN PATTERN B AT VECTOR 13
FAILED PINS : MA3 MA2 MRD

<4> FAILED IN PATTERN B AT VECTOR 13
FAILED PINS : MA3 MA2 MRD

<5> FAILED IN PATTERN B AT VECTOR 618
FAILED PINS : MRD

<6> FAILED IN PATTERN 0 AT VECTOR 12
FAILED PINS : MRD

<7> FAILED IN PATTERN 0 AT VECTOR 20
FAILED PINS : MA0

<8> FAILED IN PATTERN B AT VECTOR 628
FAILED PINS : MA0

<9> FAILED IN PATTERN B AT VECTOR 73
FAILED PINS : MA0

<10> FAILED IN PATTERN 1 AT VECTOR 101
FAILED PINS : MA2 MA1 MA0

<11> FAILED IN PATTERN 1 AT VECTOR 629
FAILED PINS : MA2 MA1

<12> FAILED IN PATTERN 5 AT VECTOR 509
FAILED PINS : MA2

<13> FAILED IN PATTERN 1 AT VECTOR 101
FAILED PINS : MA2 MA1 MA0

<14> FAILED IN PATTERN 1 AT VECTOR 629
FAILED PINS : MA2 MA1

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FAILED PINS : MA3 MA1 MA0

<16> FAILED IN PATTERN 0 AT VECTOR 934
FAILED PINS : MA2 MA1

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 19> FAILED IN PATTERN 0 AT VECTOR  934
FAILED PINS :  MA2 MA1

<20> FAILED IN PATTERN 1 AT VECTOR  485
FAILED PINS :  MA2 MA1 MA0

<21> FAILED IN PATTERN 0 AT VECTOR  854
FAILED PINS :  MA3 MA0

<22> FAILED IN PATTERN 0 AT VECTOR  36
FAILED PINS :  MRD

<23> FAILED IN PATTERN B AT VECTOR  37
FAILED PINS :  MRD

<24> FAILED IN PATTERN B AT VECTOR  618
FAILED PINS :  MRD

<25> FAILED IN PATTERN B AT VECTOR  55
FAILED PINS :  MA3 MA2 MRD

<26> FAILED IN PATTERN 0 AT VECTOR  12
FAILED PINS :  MRD

<27> FAILED IN PATTERN B AT VECTOR  618
FAILED PINS :  MRD

<28> FAILED IN PATTERN 0 AT VECTOR  3
FAILED PINS :  SC0

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FAILED PINS :  SC0

<30> FAILED IN PATTERN B AT VECTOR  617
FAILED PINS :  SC0

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FAILED PINS :  SC1

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FAILED PINS :  SC1

<33> FAILED IN PATTERN B AT VECTOR  55
FAILED PINS :  SC1

<34> FAILED IN PATTERN 0 AT VECTOR  188
FAILED PINS :  MA2 MA1

<35> FAILED IN PATTERN 0 AT VECTOR  124
FAILED PINS :  MA3 MA2

<36> FAILED IN PATTERN 0 AT VECTOR  380
FAILED PINS :  MA3 MA2 MA1
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<37> FAILED IN PATTERN 0 AT VECTOR  60
FAILED PINS :  MA3 MA2 MA1

<38> FAILED IN PATTERN 0 AT VECTOR  38
FAILED PINS :  MA3 MA2

<39> FAILED IN PATTERN A AT VECTOR  909
FAILED PINS :  MA1 MA0

<40> FAILED IN PATTERN 0 AT VECTOR  30
FAILED PINS :  MA1 MA0

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FAILED PINS :  MA2 MA1 MA0

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FAILED PINS :  MA3 MA1 MA0

<43> FAILED IN PATTERN 1 AT VECTOR  549
FAILED PINS :  MA3 MA2 MA1 MA0

<44> FAILED IN PATTERN 0 AT VECTOR  934
FAILED PINS :  MA2 MA1

<45> FAILED IN PATTERN 0 AT VECTOR  854
FAILED PINS :  MA3 MA0

<46> FAILED IN PATTERN 0 AT VECTOR  694
FAILED PINS :  MA3 MA1 MA0

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FAILED PINS :  MA3 MA2 MA1 MA0

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FAILED PINS :  MA3 MA0

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FAILED PINS :  MA3 MA2

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FAILED PINS :  MA3 MA2

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FAILED PINS :  MA0 MRD

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FAILED PINS :  MA1

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FAILED PINS :  MA1 MA0

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FAILED PINS :  MA1 MA0

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FAILED PINS :  MA0

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FAILED PINS :  MRD
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FAILED PINS : MRD

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FAILED PINS : MA3 MA2

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FAILED PINS : MA1 MA0

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