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DEVELOPMENT AND FABRICATION OF A SOLAR CELL JUNCTION PROCESSING SYSTEM

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THE JPL LOW-COST SOLAR ARRAY PROJECT IS SPONSORED BY THE U.S. DEPARTMENT OF ENERGY AND FORMS PART OF THE SOLAR PHOTOVOLTAIC CONVERSION PROGRAM TO INITIATE A MAJOR EFFORT TOWARD THE DEVELOPMENT OF LOW-COST SOLAR ARRAYS. THIS WORK WAS PERFORMED FOR THE JET PROPULSION LABORATORY, CALIFORNIA INSTITUTE OF TECHNOLOGY BY AGREEMENT BETWEEN NASA AND DOE.

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TABLE OF CONTENTS

LIST OF FIGURES

SECTION 1
CONTRACT OBJECTIVES

The basic objectives of the program are the following:

1. To design, develop, construct and deliver a junction processing system which will be capable of producing solar cell junctions by means of ion implantation followed by pulsed electron beam annealing.

2. To include in the system a wafer transport mechanism capable of transferring such wafers into and out of the vacuum chamber where the ion implantation and pulsed electron beam annealing processes take place.

3. To integrate, test and demonstrate the system prior to delivery to JPL.

4. To estimate component lifetimes and costs, as necessary for the contract, for the performance of comprehensive analyses in accordance with the solar array manufacturing industry costing standards (SAMICS).

In achieving these objectives, Spire will perform five tasks:

Task 1 - Pulsed Electron Beam Subsystem Development

Task 2 - Wafer Transport System Development

Task 3 - Ion Implanter Development

Task 4 - Junction Processing System Integration

Task 5 - Junction Processing System Cost Analyses

An artist's conception of the junction processing system is shown in Figure 1. Silicon wafers, preloaded in cassettes, are input to the machine through a vacuum lock; the transport system carries the wafers first to the ion implanter and then to the pulsed electron beam annealer where the junctions are formed and annealed. The wafers are then automatically reloaded into cassettes through the output vacuum lock.

The ion implanter will provide a 16-mA beam of $^{31}P^{+}$ ions with an energy of 10 keV and produce a junction dose of 2.5×10^{15} cm^{2} on 10-cm-diameter wafers at an average rate of 10^{7} wafers per year. The pulsed electron beam annealer will anneal the entire surface of the wafer at the same rate, representing an operational throughput of 1800 per hour.

At the present time, only Task 1 of the program is active. The remaining tasks are now scheduled to start as follows:

Task 2 - October 1, 1980
Task 3 - January 1, 1981
Task 4 - July 1, 1981
Task 5 - October 1, 1981

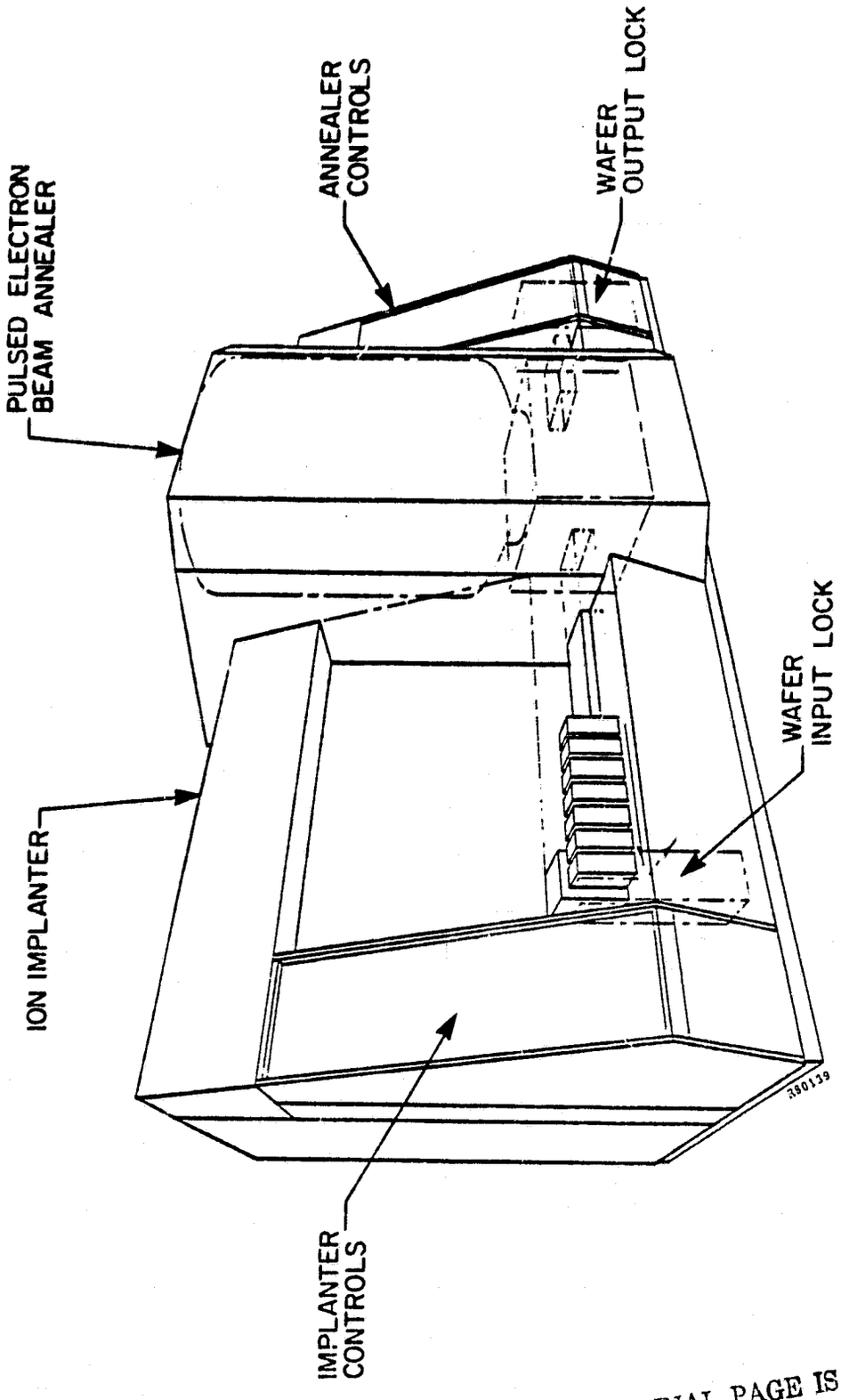

FIGURE 1. ARTISTS CONCEPTION OF SOLAR CELL JUNCTION PROCESSOR

SECTION 2
SUMMARY OF WORK PERFORMED

2.1 DEVELOPMENTAL TESTING

Experiments were completed which indicate that single-pulse, liquid-phase epitaxial regrowth is the optimum technique for pulsed electron beam annealing of ion implantation damage in silicon wafers. An electron beam which covers the entire area of the wafer has been chosen for the solar cell processor.

Beam control experiments to improve beam propagation and to test the concept of partial space charge and current neutralization have been initiated. Results from these tests will be available during the next reporting period. Other experiments on beam control and annealing optimization have been defined and will be performed when the pulsed electron beam subsystem is put into operation.

2.2 PULSER DESIGN

The electrical parameters of the pulsed electron beam subsystem have been chosen on the basis of computer calculations and Spire's past experience in pulsed electron accelerator design and operation. The pulser, designated SPI-PULSE 7000, is designed to anneal 10-cm-diameter silicon wafers at a rate of 30 per minute.

The preliminary design of the major elements of the SPI-PULSE 7000 has been completed, and the detailed design of many of the components has begun. These elements include a capacitive energy store and charging system, an electron accelerator, a beam control system, a wafer handling system and pressure and vacuum assemblies.

SECTION 3

PROGRESS ON TASK 1 - DEVELOPMENT OF PULSED ELECTRON BEAM SUBSYSTEM

3.1 DEVELOPMENTAL TESTING

Experiments have been completed to investigate techniques for pulsed electron beam annealing of 10-cm-diameter, ion-implanted silicon wafers. We have concluded from these experiments that a single pulse of electrons capable of producing liquid-phase epitaxial regrowth of the ion-implanted layer is the best annealing technique for the junction processor. Multiple pulsing by electron beams, either to induce solid-phase regrowth or to create partially overlapped, higher fluence beams, has been found to produce lower efficiency solar cells than those with junctions formed by a single pulse covering the full surface area of the silicon wafer.

A series of tests to control the beam of the pulse annealer has been initiated. These experiments are designed to test Spire's concept of using a low-pressure background gas to produce partial space charge and current neutralization by the plasma generated by electron-atom collisions. If these experiments are successful, the reduction of space charge should improve the propagation of the beam to the surface of the wafer, and partial current neutralization would reduce the diode return current carried by the wafer and its mounting system.

3.1.1 Annealing by Solid-Phase Epitaxial Regrowth

Experiments were carried out to determine the feasibility of pulse-annealing ion implantation damage by a series of low-fluence pulses from a large-area electron beam. This method of annealing would have the advantage of requiring a smaller beam energy per pulse than single-step, liquid-phase regrowth of the amorphous layer formed by ion implantation.

It was found experimentally that multiple pulses by an electron beam with a fluence less than about 0.5 $J\text{-}cm^{-2}$ produced polycrystalline regrowth of the amorphous layer if the wafer was allowed to cool between pulses. Increasing the total fluence by using a pulse duration greater than 100 ns (up to 1 microsecond) resulted in damage to the wafer by surface cracking. This effect could be avoided only by heating the wafer to $300^{\circ}C$ or greater during the pulse annealing process.

We conclude that solid-phase annealing by a series of short, low-fluence pulses or by single, low-power pulses of microsecond duration is not practical for the pulsed electron beam processor. Liquid-phase annealing, on the other hand, has been demonstrated conclusively to form solar cell junctions which are of nearly equal performance to those formed by furnace annealing.

3.1.2 Overlapping of Pulse-Annealed Regions

An experiment was conducted to evaluate the effect of overlapping high-fluence pulses of electrons on ion-implanted silicon solar cell junctions. The experiment simulated the conditions which would be encountered in the fabrication of solar cells which were annealed by multiple pulses of overlapping electron beams. Wafers of 10-ohm-cm, p-type silicon were implanted with 2.5×10^{15} cm^{-2} of 10-keV $^{31}P^{+}$ ions and pulse annealed at a fluence of 1 J cm^{2}. Half the wafers were subjected to a second pulse of the same fluence. The annealed regions of the wafers were then formed into 2x2-cm solar cells and the voltage-current characteristics of the cells were measured under AM0 illumination. For test purposes, these cells were not constructed with an antireflection coating or a back-surface-field structure. The efficiency of the single- and double-pulsed cells was as follows:

Single-Pulsed Cells	
Cell No.	Efficiency (%)
1	8.1
2	8.3
3	8.2
Double-Pulsed Cells	
4	6.7
5	6.7
6	6.3

The voltage-current characteristics of cells No. 3 and No. 4 are shown in Figure 2. The efficiency of the single-pulsed cells, although low because the cell formation process was not optimized, is clearly greater than the efficiency of the double-pulsed cells. The loss of efficiency is attributed to increased junction depths and damage from thermal stresses caused by the second pulse onto the already annealed structure of the cell. It seems clear from these and earlier experiments at Spire that solar cells with large overlapping areas of pulsed electron beam annealing would be inferior to single-pulsed cells.

We have also observed that implanted wafers annealed by several abutting, nonoverlapping pulses have a high risk of shorting the photovoltaic junction. The shorting occurs along grain boundaries of the polycrystalline region which is formed at the low-fluence edge of the pulsed electron beam. Complete regrowth of the polycrystalline region between the abutting areas would require special processing which would greatly increase the cost and complexity of the annealer.

We conclude from these tests that the use of a single pulse of electrons to cover the entire surface of the wafer is the preferable technique for pulse annealing in the junction processor. On this basis, we have made the decision to develop a pulsed electron beam subsystem which is capable of annealing 10-cm-diameter wafers in a single pulse.

3.1.3 Beam Control Experiments

A problem in the single-pulse electron beam annealing of large areas may be the conduction of the beam current away from the wafers. Currents approaching 50 kA must be carried to ground in annealing a 4-inch-diameter wafer, and arcing can take place at the edges or back of the wafer. If the electron beam could propagate in a low-density plasma, partial space charge and current neutralization of the beam would be provided by the low-energy ions and electrons in the plasma. Thus, a lower net current would be carried to the surface of the wafer.

A series of experiments has been initiated in which argon gas at a pressure of a few millitorr is introduced into the diode region of the SPI-PULSE 5000 electron beam pulser. The high-energy electrons ionize the argon and form a neutralizing plasma. Measurements of beam characteristics, total current and beam homogeneity are being made as a function of diode pressure, to determine the optimum conditions for beam propagation and partial current neutralization.

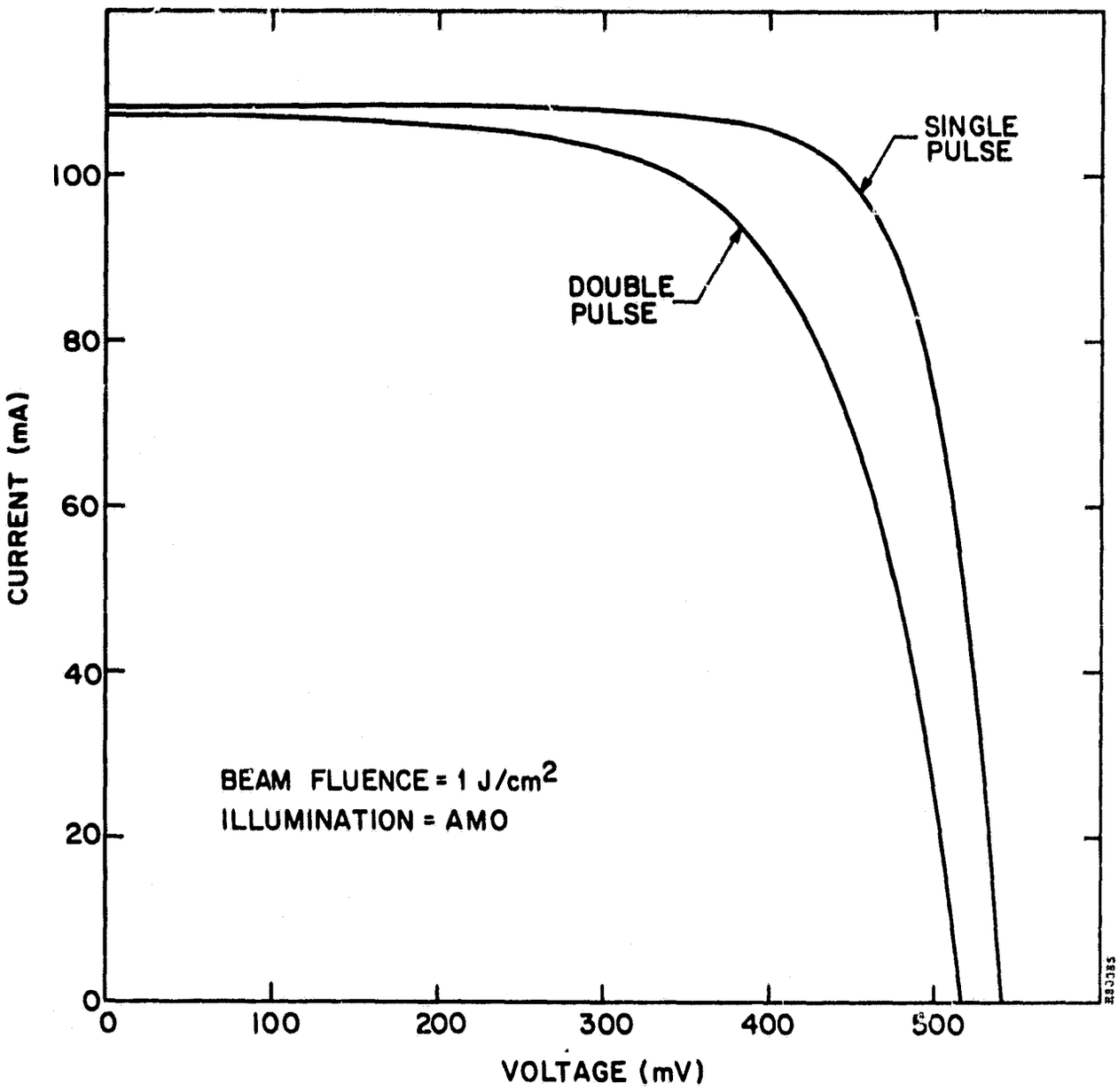

FIGURE 2. VOLTAGE-CURRENT CHARACTERISTICS OF SINGLE- AND DOUBLE-PULSE ANNEALED SOLAR CELLS

Experiments have been chosen to determine optimum magnetic field geometries and wafer-holding techniques to control beam homogeneity and to eliminate arcing at the edges of the wafers. A series of cathode designs and magnetic pole pieces will be tested in the SPI-PULSE 7000 to produce beams with diameters which somewhat exceed or are slightly smaller than the test wafers. The configuration of the imposed magnetic field, the shape of the cathode and the properties of the wafer holder will strongly influence the behavior of the electron beam at the edge of the wafer. These experiments are designed to find optimum conditions to produce uniform annealing of the entire area of the wafer without arcing at the edges.

3.1.4 Wafer Holder Optimization

A problem related to that of beam current neutralization is the design of the grounded wafer-mounting supports of the annealer, which provide the current return path for the electron beam. The wafer-mounting system must not only accurately position the wafer in front of the electron beam, but also have a large enough area of good electrical contact to carry the total beam current without sparking.

In a series of experiments with the SPI-PULSE 7000 machine, we shall test wafer-mounting designs and evaluate different materials for the wafer-holder interfaces. Clamping designs for wafer carriers are presently being developed which will provide positive mechanical pressure on an electrically conducting backing. This backing may be graphite, conductive rubber or a metallic material.

3.1.5 Preheating and Postheating Annealed Wafers

The effects of heating the wafers to several hundred degrees Celsius before and/or after pulse annealing will be determined. During ion implantation in a large-volume production line, the wafers will be heated to a temperature close to 100°C by the ion beam. This heating can influence the annealing process; we suspect that improvements of cell efficiency may be realized if further heating before, during and possibly after the pulse-annealing step is performed.

These experiments will be designed to evaluate the effects on cell performance of heating implanted wafers to 400-500°C before pulse annealing, and then heating them after annealing. Experiments on pulse-annealing heated wafers will be postponed until a heated substrate holder for the pulser is available. Performance will be evaluated by measurements of open-circuit voltage and conversion efficiency after forming a solar cell structure. Parameters to be varied during this test include temperature and time of heating before and/or after the pulse-annealing process. The SPI-PULSE 5000 accelerator will be used for these tests when an infrared heater is completed.

3.2 PULSER DESIGN

The preliminary design of the pulsed electron beam subsystem, designated SPI-PULSE 7000, has been completed. The pulser includes a capacitive energy store and an electron accelerator which can be charged and discharged every 2 seconds to produce single-pulse annealing of 10-cm-diameter silicon wafers. An interim wafer-handling system will be included in the pulsed electron beam annealer to introduce wafers into the vacuum chamber which houses the electron accelerator and beam control apparatus.

3.2.1 Design Calculations

The electrical parameters of the pulse annealer have been investigated using a simple computer model which has been shown to predict the operation of existing accelerators at Spire rather closely. Lumped circuit parameters were used to model the pulser system, and the electron beam accelerator is represented as a space-charge-limited diode with an anode-cathode gap which closes at constant speed. The circuit model used in the calculations is shown in Figure 3, where R, L, C and V_o are, respectively, the series resistance, inductance, capacitance and initial charging voltage of the capacitor. The field-emission diode has a radius, a, a gap, g, and an expansion velocity of the cathode plasma, v.

Results of calculations of the energy fluence at the surface of a 10-cm-diameter wafer as a function of store capacitance (inductance held fixed) and series inductance (capacitance held fixed) is shown in Figure 4. The crossover point at a fluence of 1.8 $J\text{-}cm^{-2}$ is the design-point chosen for the SPI-PULSE 7000. The computer model indicates that the average energy of the electrons is 18.6 keV under these conditions.

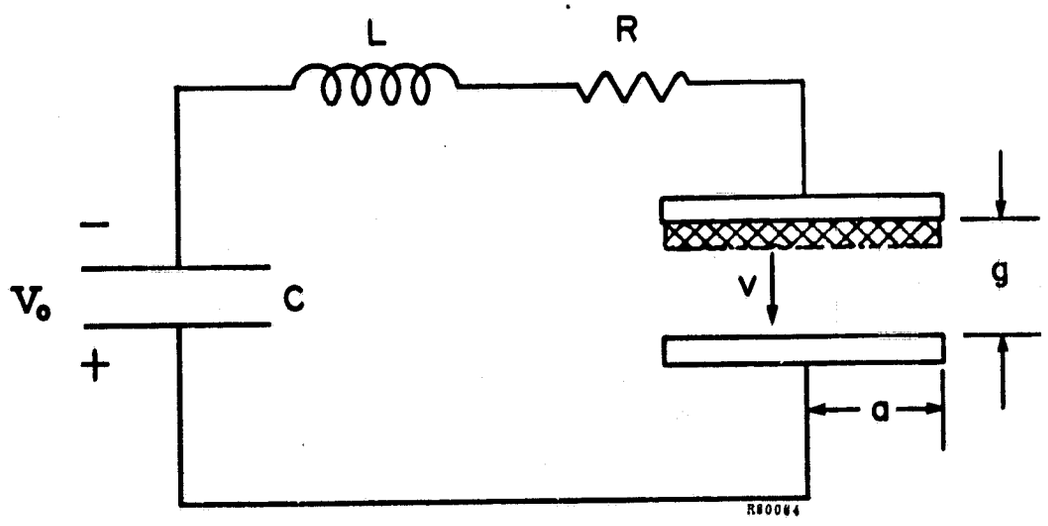

FIGURE 3. LUMPED PARAMETER CIRCUIT MODEL OF PULSED ELECTRON BEAM ANNEALER

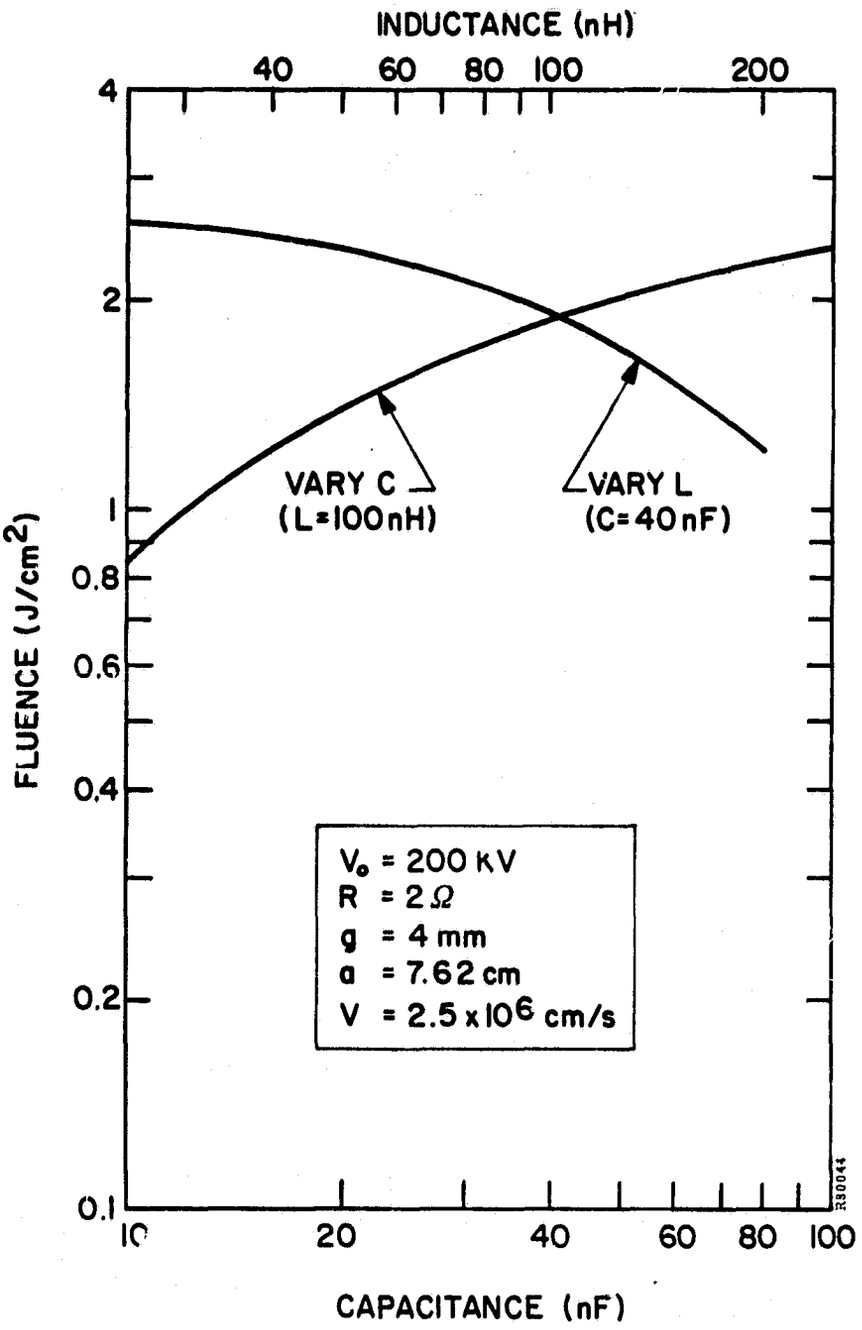

FIGURE 4. RESULTS OF ELECTRICAL MODELING OF PULSED ELECTRON BEAM ANNEALER

On the basis of the computer calculations and the past experience at Spire in annealing smaller diameter wafers, the tentative electrical parameters of the SPI-PULSE 7000 are as follows:

Total Capacitance:	40 nF
Front-End Inductance:	100 nH (approx.)
Maximum Charging Voltage:	300 kV
Operating Charging Voltage:	< 200 kV
Maximum Charging Current:	15 mA
Pulse Repetition Rate:	0.5 to 1 s^{-1}

3.2.2 Design of Energy Store

The capacitive energy store consists of 13 to 19 parallel-charged transmission lines. The characteristics of the individual lines are as follows:

Capacitance:	2.9 nF
Inductance:	14.2 nH
Electrical Length:	104 cm
Overall Length:	135 cm
Diameter:	24.1 cm
Dielectric Thickness:	0.79 cm

The dielectric material of the line is a high-strength epoxy which is cast around an aluminum cylinder, the central electrode of the coaxial line. The outer conductor is a conductive coating placed on the dielectric after casting.

The lines will be placed vertically in a hexagonal arrangement in a vessel which can be pressurized with dielectric gas. The capacitor array will be charged by a high-voltage electronic power supply and discharged into the accelerator by a mechanically actuated switch. The preliminary designs of all the components of the energy store have been completed.

3.2.3 Design of Accelerator, Beam Control and Wafer-Handling Systems

The electron beam accelerator consists of a field-emission diode with a cathode diameter up to 15.2 cm and a metallic mesh anode. The anode-cathode gap can be adjusted from 1 mm to 10 mm. The beam from the accelerator will propagate about 5 mm to the wafer, which is lifted into place below the anode by a pneumatic actuator.

An electromagnet and a soft-iron yoke will provide a magnetic field up to 5000 gauss in the beam drift space and diode region. The strength and shape of the field will be adjustable over a wide range, to provide an optimized beam control system.

The diode, wafer handling system and pole-pieces of the magnetic yoke will be housed in a vacuum chamber which will be evacuated by a cryogenic pump. The test wafers will be introduced into and removed from the processing chamber through differentially pumped vacuum locks, so that the chamber can remain under vacuum at all times.

An interim wafer-handling system will be designed and built to Spire's specifications by Brooks Associates, Inc., of North Billerica, Massachusetts, for the electron beam pulser. The interim system will pass a single wafer from a vacuum lock on the processing chamber to the diode region and will then remove the wafer through an exit lock. This system, which can be easily upgraded during the later tasks of the program, will be adequate for testing and optimizing the pulse annealer.

Preliminary designs of all the above components of the annealer have been completed, and detailed designs have been initiated for most of them.