High-Power Transmitter Automation

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This report describes the current status of the transmitter automation development. The work being done is applicable to all transmitters in the DSN. New interface and software designs are described that improve reliability and reduce the time required for subsystem turn-on and klystron saturation to less than 10 minutes.

I. Introduction

The benefits of transmitter automation are the reduction of life-cycle costs and increased availability. Life-cycle costs will be reduced not only by the requirement for fewer operators, but also by more effective preventive maintenance through increased and more accurate reporting of critical subsystem parameters. Increased availability will be provided by eliminating the need for operations personnel on evening and weekend shifts. Automatic fault diagnosis and programmed recovery procedures will also increase availability.

The development work currently being done for the DSS 13 high-power S-band transmitter is applicable to all other known or planned transmitters in the Deep Space Network including the X-band uplink development at DSS 13. The difference in operational parameters of the various transmitters is provided for by including a configuration table (see Fig. 1 for a typical set) for each transmitter in the program. Each klystron has its own table. The upper block contains the klystron serial numbers for which the program contains a configuration data block. The middle block contains maximum and minimum operating values. The lower block contains the analog channels full-scale meter values. Instrumentation amplifiers convert all analog channel inputs to 5 volts full scale. The target values are used as adjustment goals and are changed as required during operation of the transmitter. Each channel has a delta value used as an out-of-adjustment tolerance. It should be noted that the data are easily understood even though it is actually part of the program code. Provision for operating in an unsaturated mode has been included. All commands, analogs, interlocks, and indicators (from the program listing) are shown in Figs. 2 through 5.

II. History

Prior automation efforts for the transmitter subsystem met with limited success. The first attempt used a PDP-11 minicomputer for the controller. Poor hardware reliability was encountered and the only high-level language available (Basic) was unsuitable for real-time control. Memory requirements and computing time limited the degree of automation that could be performed. With the development of microprocessors and the availability of a high-level language suitable for control applications (*PL/M*), the next effort used a JPL packaged microprocessor and provided a controller that has proved satisfactory although improvements in some areas are desirable. About 30 percent of the software was written in assembly language and a floating point math package was used

that slowed the execution time considerably. The time required to turn on and calibrate the transmitter was about 35 minutes. In addition, special interface logic was built that would be too difficult and expensive to maintain in the field. Thus, it was decided to rewrite the software entirely in *PL/M* and use integer arithmetic for all computing. All analog quantities are represented internally by an eight-bit binary fraction of the full-scale value. In addition, it was decided to eliminate all custom designed circuitry and use only commercially available off-the-shelf items of proven performance, reliability, and availability.

III. New Hardware

The new controller is based on the Intel industrial control series using an 8080 microprocessor and standard CCM approved modules. These include the 80/20-4 CPU with 8 kbytes of RAM and provision for 24 digital output lines and a PROM card for program storage. Communication is provided by an SBC-534 module with four RS-232C ports. An SBC-519 input-output card provides for 72 digital input signals. A 32-channel differential input multiplexer and analog-to-digital converter is used for analog inputs (only 16 channels are used). A block diagram of the transmitter controller appears in Fig. 6. This controller is located in the High Power Test Facility at DSS 13 near the Local Control Console. A second controller (without the signal interfaces) is in the control room near the Remote Control Console. This controller acts solely as a communications buffer for the 15-line standard interface to the station controller. The interface between the transmitter controllers is a serial interface (RS-232C) through short-haul modems. The interface modules are also part of Intel's industrial control line, and provide for filtering and level shifting with optoisolators. Most of the transmitter control and indicator circuitry is 28 volts. A photograph of the transmitter controller showing the vertically mounted interface modules is shown in Fig. 7.

A transmitter simulator was constructed using TTL logic and operational amplifiers to facilitate checkout of the new controller. The device simulates all major functions of the transmitter including interlock logic and realistic klystron characteristics, and has been invaluable in the checkout of the controller and evaluation of new algorithms. A photograph of the transmitter simulator appears in Fig. 8.

IV. Software

The software conforms to top-down structured methodology and is 100 percent *PL/M*. The programs (both controllers) require about 6000 lines of code that produce 40 kbytes when assembled. A composite top-level flowchart is shown in Fig. 9. The time between successive passes through the monitor is about 600 ms. The time required for turn on and calibration is now about 10 minutes (using the simulator). A photograph of the maintenance display is shown in Fig. 10.

V. Present Status

Testing of the controller with the simulator has been completed and currently the controller is being installed at DSS 13 for further evaluation and support of unattended operation demonstrations.

```
/**** CONFIGURATION DATA STRUCTURE  04/09/80 ********/
CONFIG$DAT: DO;
DECLARE SERIAL$NO$DAT(8) STRUCTURE(DAT(14) BYTE) PUBLIC DATA (
  /*  0  */  'SIMULATOR      ' ,
  /*  1  */  'L5- 3-R1 DSS63' ,
  /*  2  */  'L5-34-R1 DSS63' ,
  /*  3  */  'K5-24-R1 DSS43' ,
  /*  4  */  'A6-17-R2 DSS13' ,
  /*  5  */  'J5-24-R2 DSS14' ,
  /*  6  */  'H5-30-R2 DSS43' ,
  /*  7  */  'B8- 1-R1 DSS14' );

DECLARE CFG1(64) STRUCTURE (DAT(4) BYTE ) PUBLIC DATA (   /**  DSS-13  **/

  /*         NAME                    LIMIT       */

  /* SERIAL NUMBER REF          */  '   4' ,
  /* TBEMCB - CB TEST V         */  '  20' ,
  /* TBEMLO - MIN PWR BM V      */  '  20' ,
  /* TBEMMI - MAX BM I          */  ' 4.4' ,
  /* TBEMMV - MAX BM V          */  '  25' ,
  /* TDRIVL - MIN DRIVE         */  ' 300' ,
  /* TDRVMX - MAX DRIVE         */  ' 996' ,
  /* TFILMX - MAX FIL V         */  '  11' ,
  /* TMAGMX - MAX MAG I         */  '  18' ,
  /* TPERVI - PERVEANCE BM I    */  ' 4.4' ,
  /* TPWRMN - MIN PWR OUT       */  '  10' ,
  /* TPWRMX - MAX PWR OUT       */  '  30' ,
  /* TBM10                      */  '19.9' ,
  /* TBM20                      */  '22.1' ,
  /* TBM30                      */  '23.4' ,
  /* NULL                       */  '   0' ,

  /*  NAME      FULLSCALE     TARGET      DELTA    */

  /*  OUTPW  */  ' 100' , '  10' , '   1' ,
  /*  BEAMV  */  ' 100' , '   0' , ' 0.5' ,
  /*  BEAMI  */  '  25' , '   0' , ' 0.5' ,
  /*  DRIVP  */  '1000' , '   0' , ' 100' ,
  /*  REFLC  */  '1000' , ' 500' , ' 100' ,
  /*  BODYI  */  '1000' , ' 600' , ' 300' ,
  /*  COLEC  */  '  25' , '   0' , ' 0.3' ,
  /*  FILAV  */  '  25' , ' 9.0' , ' 0.3' ,
  /*  FILAI  */  '  25' , '10.5' , ' 0.3' ,
  /*  MAGNT  */  '  25' , '17.4' , ' 0.2' ,
  /*  VACUM  */  '  50' , ' 1.5' , ' 1.5' ,
  /*  CRWBR  */  '  50' , '  10' , '   5' ,
  /*  NULL   */  '   0' , '   0' , '   0' ,
  /*  NULL   */  '   0' , '   0' , '   0' ,
  /*  NULL   */  '   0' , '   0' , '   0' ,
  /*  NULL   */  '   0' , '   0' , '   0' );
```

Fig. 1. Typical configuration table

```
PL/M-80 COMPILER


ISIS-II PL/M-80 V3.1 COMPILATION OF MODULE COMMANDDAT
OBJECT MODULE PLACED IN :F1:CMDEFT.OBJ
COMPILER INVOKED BY:  PLM80 :F1:CMDEFT.PLM DEBUG XREF IXREF SYMBOLS



                /******** COMMAND DATA DEFINITION   03/25/80 *******/

   1            COMMAND$DAT: DO;

   2    1       DECLARE CMND$BUF(3) BYTE EXTERNAL;
   3    1       DECLARE CMND$DAT(21) STRUCTURE (
                  BYTE$NUM BYTE, BIT$NUM BYTE,
                  COL BYTE, ROW BYTE,
                  NAME(6) BYTE ) PUBLIC DATA (

                    2,7,47,1,     'ARCDT ',
                    1,3,47,2,     'BEMLO ',
                    1,5,47,3,     'BEMOF ',
                    1,4,47,4,     'BEMON ',
                    1,2,47,5,     'BEMRA ',
                    1,7,47,6,     'BEMRL ',
                    0,4,47,7,     'CBTST ',
                    0,7,47,8,     'CPSOF ',
                    2,0,47,9,     'CPSON ',
                    2,5,47,10,    'DRVLO ',
                    2,6,47,11,    'DRVRA ',
                    2,4,47,12,    'FILLO ',
                    2,3,47,13,    'FILRA ',
                    1,6,47,14,    'ILRST ',
                    0,5,47,15,    'MAGLO ',
                    0,6,47,16,    'MAGRA ',
                    0,3,47,17,    'PROGR ',
                    1,0,47,18,    'PMPOF ',
                    1,1,47,19,    'PMPON ',
                    2,1,47,20,    'SYNOF ',
                    2,2,47,21,    'SYNON '  );
```

Fig. 2. Command table

```
142   1       DISPLAY$FORMAT: PROCEDURE;
143   2         DECLARE ANALOG$LABEL(12) STRUCTURE (LBL(11) BYTE ) DATA (
                  'OUTPUT    KW',
                  'BEAM V    KV',
                  'BEAM I     A',
                  'DRIVE     MW',
                  'REFLECT    W',
                  'BODY I    MA',
                  'COLL I     A',
                  'FILA V     V',
                  'FILA I     A',
                  'MAGNET I   A',
                  'VACUUM I  UA',
                  'CROWBAR   US' );
```

Fig. 3. Analog channels

```
            /********** DIGITAL DATA DEFINITIONS 04/22/80 ******/

1           DIGITAL$DEF: DO;

2   1       DECLARE DIGITAL$DAT(72) STRUCTURE (
                BYTE$NUM BYTE, BIT$NUM BYTE,
                COL BYTE, ROW BYTE,
                NAME(6) BYTE,
                DESCRIPT(16) BYTE) PUBLIC DATA (

            /** INTERLOCKS **/

                0,3,54,1,     'ALIHEF',     'ALI HE FLOW I-L ', /* 00 */
                2,4,54,2,     'ALIHET',     'ALI HE O-T I-L  ', /* 01 */
                4,0,54,3,     'ARCDT1',     'ARC DET #1 I-L  ', /* 02 */
                5,7,54,4,     'ARCTD2',     'ARC DET #2 I-L  ', /* 03 */
                2,2,54,6,     'BODYFL',     'BODY FLOW I-L   ', /* 04 */
                4,7,54,7,     'BODYOC',     'BODY O-C I-L    ', /* 05 */
                1,0,54,8,     'CBFIRE',     'C-B FIRED I-L   ', /* 06 */
                3,2,54,9,     'CBLKBF',     'CBL KBF I-L     ', /* 07 */
                3,1,54,10,    'CBLKBS',     'CBL KBS I-L     ', /* 08 */
                1,1,54,11,    'CBLKMS',     'CBL KMS I-L     ', /* 09 */
                2,7,54,12,    'CBLTES',     'CBL TEST I-L    ', /* 10 */
                2,3,54,13,    'COLLFL',     'COLECTR FLOW I-L', /* 11 */
                6,0,54,14,    'COLLOC',     'COLLECTR O-C I-L', /* 12 */
                3,0,54,15,    'DCOCUR',     'DC O-C I-L      ', /* 13 */
                1,7,54,16,    'DCOVLT',     'DC O-V I-L      ', /* 14 */
                5,3,54,17,    'DOORAN',     'DOOR ANTENNA I-L', /* 15 */
                3,5,54,18,    'DOORPE',     'DOOR PEDESTL I-L', /* 16 */
                5,4,54,19,    'DOORVA',     'DOOR VALULT I-L ', /* 17 */
                2,1,54,20,    'DRIFTT',     'DRIFT T FLOW I-L', /* 18 */
                5,2,54,21,    'ELEVAT',     'ELEVATION I-L   ', /* 19 */
                0,7,54,22,    'FILAMA',     'FIL-MAG FLOW I-L', /* 20 */
                4,3,54,23,    'FILATD',     'FILAMENT T-D I-L', /* 21 */
                4,5,54,24,    'FILAUC',     'FILAMENT U-C I-L', /* 22 */
                2,6,61,1,     'GENERA',     'GEN LOCKOUT I-L ', /* 23 */
                1,4,61,2,     'HVZERO',     'H-V ZERO I-L    ', /* 24 */
                3,7,61,3,     'IGNITR',     'IGNITRON PWR I-L', /* 25 */
                4,6,61,5,     'MAGNUC',     'MAGNET U-C I-L  ', /* 26 */
                3,0,61,6,     'MAPOWE',     'MET AMP POW I-L ', /* 27 */
                1,5,61,7,     'MOTORL',     'MOTR LOCKOUT I-L', /* 28 */
                1,3,61,8,     'MOTORS',     'MOTOR START I-L ', /* 29 */
                1,6,61,9,     'RECTPH',     'REC PHAS O-C I-L', /* 30 */
                4,2,61,10,    'REFLP1',     'REFL PWR #1 I-L ', /* 31 */
                4,1,61,11,    'REFLP2',     'REFL PWR #2 I-L ', /* 32 */
                5,6,61,12,    'REFLPM',     'REFL PWR MET I-L', /* 33 */
                5,5,61,13,    'TRFLOW',     'TRN-REC FLOW I-L', /* 34 */
                1,2,61,14,    'TRROIL',     'TRN-REC OIL I-L ', /* 35 */
                0,5,61,15,    'TXRCON',     'TXR CONFIG I-L  ', /* 36 */
                4,4,61,16,    'VACUOC',     'VACUUM O-C I-L  ', /* 37 */
                5,1,61,17,    'VACUPW',     'VACUUM PWR I-L  ', /* 38 */
                2,0,61,18,    'WATRLO',     'WATER LOAD F I-L', /* 39 */
                3,6,61,19,    'WAVPRE',     'WAVE-G PRESS I-L', /* 40 */
                0,6,61,20,    'WAVSWS',     'WAVEGUIDE SW I-L', /* 41 */
```

Fig. 4. Interlocks

```
/** INDICATORS **/

    7,0,54,5,     'AUXHEO',     'AUX H-E          ',  /* 42 */
    2,5,61,4,     'MAINHE',     'MAIN H-E         ',  /* 43 */
    7,4,61,22,    'ALIHEO',     'ALIDADE H-E      ',  /* 44 */
    3,4,61,23,    'ANTENA',     'ANT POSITION IND',   /* 45 */
    7,2,61,24,    'BEAMOF',     'BEAM OFF IND     ',  /* 46 */
    8,5,68,1,     'BEAMLO',     'BEAM LOWER IND   ',  /* 47 */
    8,4,68,2,     'BEAMRA',     'BEAM RAISE IND   ',  /* 48 */
    6,4,68,3,     'BEAMRD',     'BEAM READY IND   ',  /* 49 */
    6,5,68,4,     'CNTROF',     'CONTROL P-S IND  ',  /* 50 */
    6,6,68,5,     'CNTRON',     'CONTROL P-S IND  ',  /* 51 */
    6,2,68,6,     'DRIVLO',     'DRIVE LOWER IND  ',  /* 52 */
    6,3,68,7,     'DRIVRA',     'DRIVE RAISE IND  ',  /* 53 */
    8,3,68,8,     'FILALO',     'FILA LOWER IND   ',  /* 54 */
    6,1,68,9,     'FILARA',     'FILA RAISE IND   ',  /* 55 */
    7,1,68,10,    'GENFIE',     'GEN FIELD PS IND',   /* 56 */
    0,4,68,11,    'HEFANS',     'H-E FANS         ',  /* 57 */
    7,3,68,12,    'ILOPEN',     'I-L OPEN IND     ',  /* 58 */
    0,2,68,13,    'NORMAL',     'NORMAL IND       ',  /* 59 */
    0,1,68,14,    'PROGRA',     'PROGRAM IND      ',  /* 60 */
    8,2,68,15,    'PUMPOF',     'PUMPS IND        ',  /* 61 */
    8,1,68,16,    'PUMPON',     'PUMPS IND        ',  /* 62 */
    6,7,68,17,    'SYNCOF',     'SYNC MOTOR IND   ',  /* 63 */
    8,0,68,18,    'SYNCON',     'SYNC MOTOR IND   ',  /* 64 */
    7,7,68,19,    'V5UAMP',     'V5UA SCALE IND   ',  /* 65 */
    8,6,68,20,    'V50UAM',     'V50UA SCALE IND  ',  /* 66 */
    7,6,68,21,    'V500UA',     'V500UA SCALE IND',   /* 67 */
    7,5,68,22,    'V5MAMP',     'V5MA SCALE IND   ',  /* 68 */
    8,7,68,23,    'V50MAM',     'V50MA SCALE IND  ',  /* 69 */
    3,3,68,24,    'WATRPO',     'WATER-LD POS IND',   /* 70 */
    0,0,61,21,    'SPARE ',                       ');/* 71 */
```

Fig. 5. Indicators

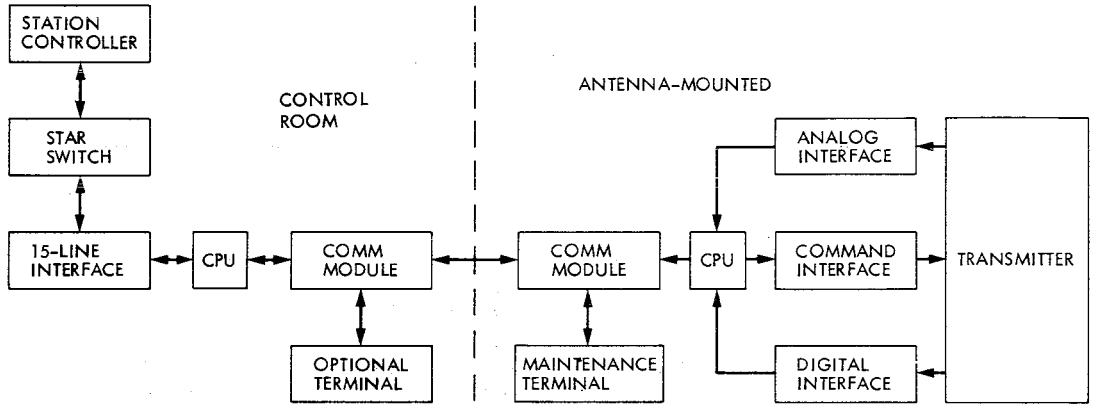

Fig. 6. Transmitter controller block diagram

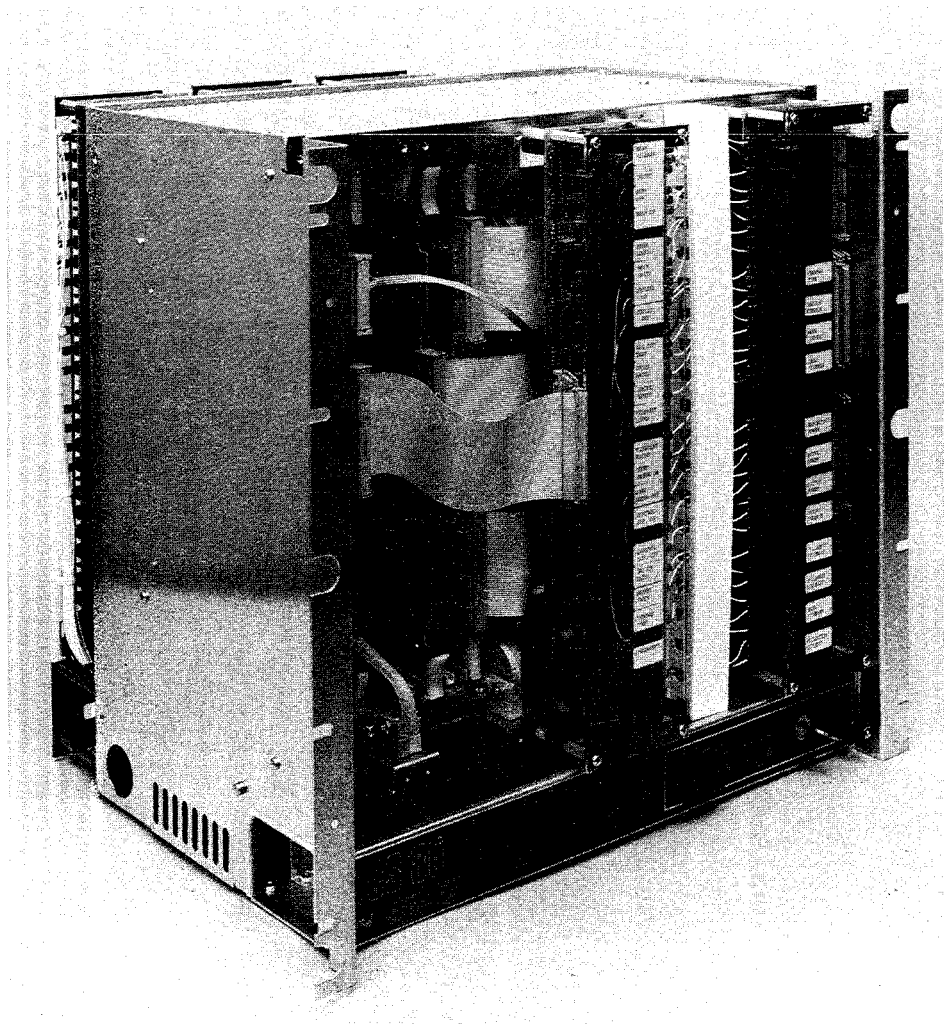

Fig. 7. Transmitter controller

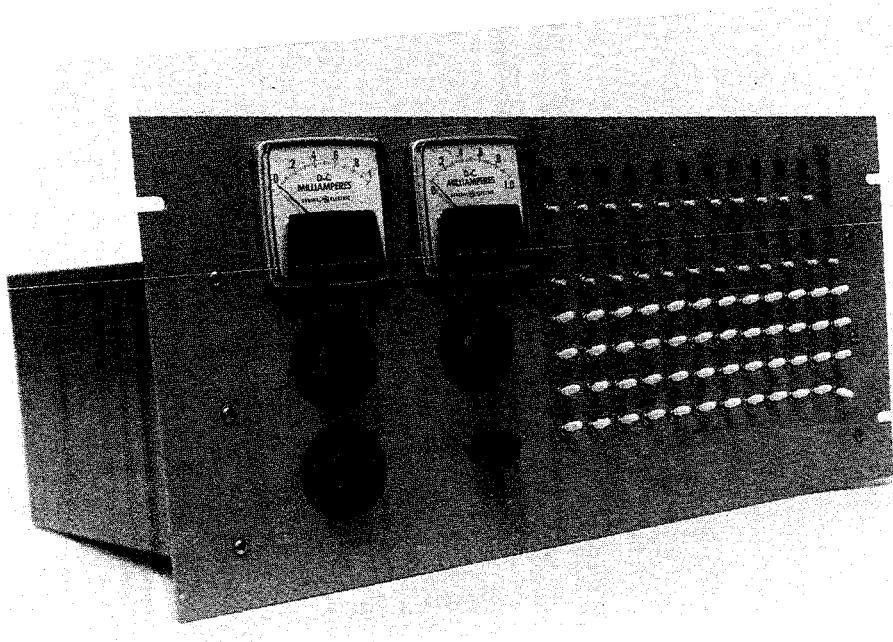

Fig. 8. Transmitter simulator

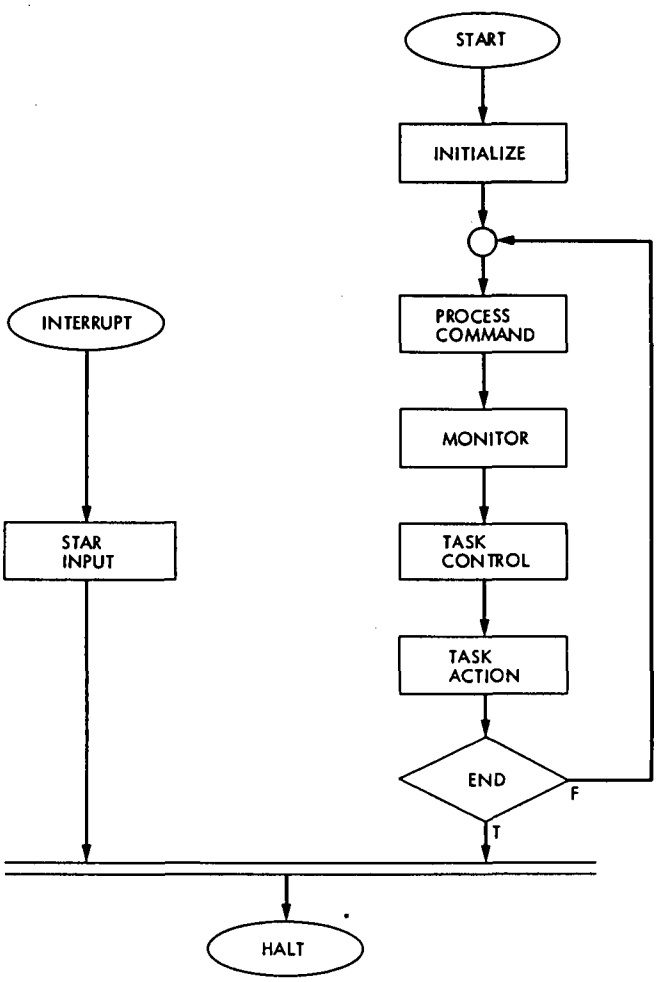

Fig. 9. Transmitter control program top-level flowchart

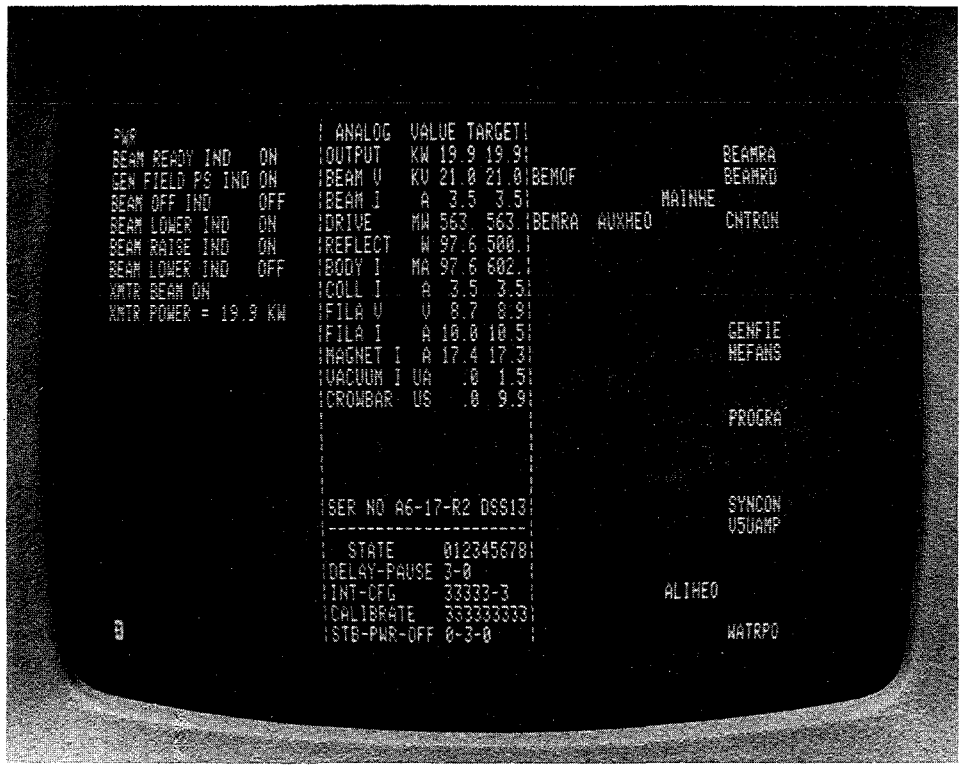

Fig. 10. Maintenance display