N O T I C E

THIS DOCUMENT HAS BEEN REPRODUCED FROM
MICROFICHE. ALTHOUGH IT IS RECOGNIZED THAT
CERTAIN PORTIONS ARE ILLEGIBLE, IT IS BEING RELEASED
IN THE INTEREST OF MAKING AVAILABLE AS MUCH
INFORMATION AS POSSIBLE

(NASA-CR-150607) CHARACTERIZATION OF SILICON-GATE CMOS/SOS INTEGRATED CIRCUITS PROCESSED WITH ION IMPLANTATION Final Report, 1 Jul. 1976 - 30 Jun. 1977 (RCA Solid State Technology Center) 52 p

N80-26603

Unclas
G3/33 23582

NASA CONTRACTOR REPORT

NASA CR-150607

CHARACTERIZATION OF SILICON-GATE CMOS / SOS INTEGRATED CIRCUITS PROCESSED WITH ION IMPLANTATION

By D. S. Woo
RCA Corporation
Solid State Technology Center
Somerville, NJ 08876

Final Report

August 1977

Prepared for

NASA - George C. Marshall Space Flight Center
Marshall Space Flight Center, Alabama 35812

1. Report No. CR-150607	2. Government Accession No.	3. Recipient's Catalog No.
4. Title and Subtitle CHARACTERIZATION OF SILICON-GATE CMOS/SOS INTEGRATED CIRCUITS PROCESSED WITH ION IMPLANTATION		5. Report Date August 1977
		6. Performing Organization Code
7. Author(s) D. S. Woo		8. Performing Organization Report No. PRRL-77-CR-40
9. Performing Organization Name and Address RCA Corporation Solid State Technology Center Somerville, NJ 08876		10. Work Unit No.
		11. Contract or Grant No. NAS8-31986
12. Sponsoring Agency Name and Address National Aeronautics and Space Administration Washington, D. C. 20546		13. Type of Report and Period Covered Final Report (7/1/76 - 6/30/77)
		14. Sponsoring Agency Code

15. Supplementary Notes

This work was done under the sponsorship of Marshall Space Flight Center, Alabama 35812, John Gould, COR.

16. Abstract

This final report describes progress in developing the application of ion-implantation techniques to silicon-gate CMOS/SOS processing. All of the conventional doping techniques such as *in situ* doping of the epi-film and diffusion by means of doped oxides were replaced by ion implantation.

Various device and process parameters are characterized to generate an optimum process by the use of an existing SOS test array. As a result, excellent circuit performance was achieved. A general description of the all-ion-implantation process is presented.

17. Key Words (Selected by Author(s))

Ion implantation
CMOS/SOS
Silicon gate

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price*
Unclassified	Unclassified	52	NTIS

TABLE OF CONTENTS

Section		Page
LIST OF SYMBOLS		vii
SUMMARY		1
I.	INTRODUCTION	2
II.	APPLICATION OF ION IMPLANTATION	4
	A. Introduction	4
	B. Equipment	4
	C. Impurity Control	7
	1. Impurity Distribution	7
	2. Implant Dose	8
	3. DOSE#	8
	D. Radiation Damage and Anneal	12
III.	SUBSTRATE IMPLANTATION	14
	A. Introduction	14
	B. Ion-Implant (I^2) Process	14
	1. I^2(I/N) Process	16
	2. I^2(N/N) Process	16
	3. $2I^2$(P/N) Process	16
	4. $2I^2$(NP/N) Process	17
IV.	GATE IMPLANTATION	18
	A. Introduction	18
	B. Experiment	18
	C. Results	19
V.	SOURCE-DRAIN IMPLANTATION	22
	A. Introduction	22
	B. Experiment	22
	C. Results	22
VI.	TEST VEHICLE	26
VII.	ALL-ION-IMPLANTATION PROCESS	29
	A. Introduction	29
	B. Process	29

TABLE OF CONTENTS (Continued)

Section		Page
VIII.	RESULTS	35
	A. General	35
	B. Transistor Characteristics	35
	C. Stage Delay	42
IX.	CONCLUSIONS	43

LIST OF ILLUSTRATION

Figure		Page
1.	Accelerators, Inc., Model MP-200 ion implanter	5
2.	Impurity profile after ion implantation, plotted in semi-log scale	7
3.	Rp and ΔRp for ^{11}B and ^{31}P as a function of implantation energy	10
4.	Single-ion-implantation process	15
5.	Double-ion-implantation process	15
6.	Cross-sectional view of a POS sample designed to study impurity penetration through the polysilicon film	18
7.	Sheet resistance of 500-nm polysilicon film implanted with 60-keV boron	20
8.	Sheet resistance of 500-nm polysilicon film implanted with 180-keV phosphorus	21
9.	Sheet resistance of 600-nm SOS film implanted with 60-keV boron	24
10.	Sheet resistance of 600-nm SOS film implanted with 180-keV phosphorus	25
11.	Photomicrograph of the test chip TCS 010	26
12.	32-stage ring oscillator	28
13.	Cross-sectional view of all-ion-implantation process for silicon-gate CMOS/SOS process	30
14.	Device characteristics of test transistors from Lot S1456	39
15.	Device characteristics of test transistors from Lot S1609	40
16.	Gate transfer characteristic for both NMOS and PMOS transistors	41

LIST OF TABLES

Table		Page
1.	Performance Specifications of Accelerators, Inc., Model MP-200 Ion Implanter	6
2.	Performance Specifications of Extrion, Inc., Model 200-1000	6
3.	Range and Spread of Boron and Phosphorus Implanted in SOS Wafer	9
4.	Boron Implantation (with E = 60 keV) on 500-nm Polysilicon Film	19
5.	Phosphorus Implantation (with E = 180 keV) on 500-nm Polysilicon Film	20
6.	Boron Implantation with E = 60 keV on 600-nm SOS and n-Type Bulk-Silicon Wafers	23
7.	Phosphorus Implantation with E = 180 keV on 600-nm SOS and p-Type Bulk-Silicon Wafers	23
8.	Test Vehicles on SOS Chip	27
9.	Implantation Data for Lot S1456	36
10.	Implantation Data for Lot S1609	36
11.	Individual-Lot Analysis (SOS) of Lot S1456	37
12.	Individual-Lot Analysis (SOS) at Lot S1609	38

LIST OF SYMBOLS

Symbol	Definition
A	Area, cm^2
B	Boron
^{11}B	Isotope of Boron with Mass Number 11
BV_{ox}	Oxide Breakdown Voltage, V
BV_{sd}	Source-Drain Breakdown Voltage, V
CMOS	Complementary Metal Oxide Silicon
CV	Capacitance Voltage
E	Acceleration Energy of Ions, keV
ε_o	Permittivity of Free Space (8.86×10^{-14} F/cm)
H_2	Hydrogen
HCl	Hydrochloric Acid
HF	Hydroflouric Acid
H_2O	Water or Steam
I	Electrical Current, A
I^2	Ion Implant
I_d	Drain Current
I_{dss}	Drain to Source Leakage Current with Gate Shorted
K	$K = \frac{W \varepsilon_o \kappa_{ox} \mu}{2 L T_{ox}}$
κ_{ox}	Dielectric Constant of Silicon Dioxide (3.82)
KOH	Potassium Hydroxide
L	Channel Length, μm
LSI	Large Scale Integration
MOS	Metal Oxide Silicon
MIN	Minimum
MAX	Maximum
μ	Mobility, cm^2/V-s
n	n-Type or Number of Charges per Ion

N	N-Channel
N_2	Nitrogen
NMOS	N-Channel Metal Oxide Silicon
N_s	Surface Concentration, cm^{-3}
N_{ss}	Surface State Density, cm^{-2}
p	p-Type
P	P-Channel or Phosphorus
PMOS	P-Channel Metal Oxide Silicon
POS	Polysilicon Oxide Silicon
q	$q = 1.602 \times 10^{-19}$ C
Q_{ss}	Surface State Charge Density, C/cm^2
R	Range, μm
R_p	Projected Range, μm
ΔR	Spread, μm
R_s	Sheet Resistance, Ω/□
SiH_4	Silane
Si_3N_4	Silicon Nitride
SiO_2	Silicon Dioxide
SOS	Silicon On Sapphire
t	Time, s
Tr	Transistor
V_d	Drain Voltage
V_{FB}	Flat-Band Voltage, V
V_t	Threshold Voltage, V
W	Channel Width, μm
X_j	Diffusion Junction Depth, μm
X_1	Lateral Diffusion Length, μm

LIST OF UNITS

Symbol of Prefix	Prefix	Factor
M	mega	10^{6}
k	kilo	10^{3}
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}

Symbol of Units	Definition
A	ampere
C	Coulomb or Celsius
eV	Electron Volt
F	Farad
in.	inch
m	meter
mil	10^{-3} inch
min	minute
Ω	ohm
Ω/□	ohm per square
s	second
V	Volt

CHARACTERIZATION OF SILICON-GATE CMOS/SOS INTEGRATED CIRCUITS PROCESSED WITH ION IMPLANTATION

by

D. S. Woo

RCA Corporation
Solid State Technology Center
Somerville, NJ 08876

SUMMARY

This final report describes progress in developing the application of ion-implantation techniques to silicon-gate CMOS/SOS processing. All of the conventional doping techniques such as *in situ* doping of the epi-film and diffusion by means of doped oxides were replaced by ion implantation.

Various device and process parameters are characterized to generate an optimum process by the use of an existing SOS test array. As a result, excellent circuit performance was achieved. A general description of the all-ion-implantation process is presented.

I. INTRODUCTION

The SOS technology developed at the David Sarnoff Research Center, Princeton, NJ, was transferred to the Solid State Technology Center, Somerville, NJ, in 1972. RCA's current complementary metal-oxide semiconductor/silicon-on-sapphire (CMOS/SOS) technology uses self-aligned silicon gates. A two-step silicon-film double-epitaxial (epi) process was used for CMOS/SOS fabrication, and this was later changed to a single-layer process applying ion implantation for the lightly doped substrate or channel area.* However, doped oxides have been routinely used for the polysilicon and source-drain diffusions.

A high-beam-current Extrion** ion implanter was installed at RCA and is in routine operation. Wafer throughput of this machine is comparable to results obtained with the conventional diffusion technique for high doping concentrations to the degenerate level and makes it feasible to use the machine in the normal production line.

Five implantation steps were used to complete the process: two low-dosage implantations for threshold voltage control and three high-dosage implantations for polysilicon and source-drain doping. The device characteristics are entirely comparable to those from devices made by conventional processing. The circuit probe yield of the test chip was 94%. The stage delay of the ring oscillator is 2.46 to 4.12 ns; it is much faster than that (5.5 ns) of the conventional process.

This final technical report covers the work performed by RCA Solid State Technology Center, Somerville, NJ, under Contract NAS8-31986 from July 1, 1976 to June 30, 1977. H. Borkan, manager, custom monolithics, had overall supervision of the program. The contract was administered

*The work was developed under Contract No. F33615-73-C-5043, "Manufacturing Methods for Silicon Devices on Insulating Substrates," for Air Force Materials Laboratory, Wright-Patterson Air Force Base.
**Varian-Extrion Division, Blackburn Industrial Park, Gloucester, MA.

under the technical direction of John Gould and Donald Routh, Marshall Space Flight Center, Alabama, 38512.

Contributors to this work are J. S. Mack for silicon film deposition, S. G. Policastro for processing, and A. C. Lindabery and R. Widuta for ion implantation.

II. APPLICATION OF ION IMPLANTATION

A. Introduction

Ion implantation is a process that introduces controlled amounts of selected impurity atoms into the surface of a semiconductor substrate by bombardment with ions in the keV energy range. Compared with doped layers produced by other techniques, ion-implanted regions are generally shallower, are formed at lower temperatures, and can be masked by a wider range of materials, such as photoresist, SiO_2, Si_3N_4, and aluminum. However, the exact doping distribution may be difficult to predict, not all implanted atoms may be electrically active, and a high density of defects may remain in the implanted region.

Recently, ion implantation has been introduced in semiconductor technology as a means of providing better control of doping density and uniformity than can be achieved with conventional doping and diffusion techniques. The application of ion implantation to CMOS/SOS technology has been successfully accomplished, simplifying the processing. In addition, more reproducible device characteristics have been obtained by the use of ion implantation.

B. Equipment

An Accelerators, Inc.* (AI) Model MP-200 low-beam-current ion implanter has been used to control threshold voltages; the equipment is shown in Fig. 1. This equipment has both high-volume and development capabilities. Variable ion sources are available, such as boron, phosphorus, arsenic, aluminum, nitrogen, helium, and argon. In our development on SOS processing, only boron and phosphorus were used exclusively. The performance specifications of the equipment are summarized in Table 1.

A high-beam-current ion implanter, Extrion Model 200-1000, has been used to dope polysilicon gates and source drains. The actual operating range of the implanter is shown in Table 2.

*Accelerators, Inc., Austin, TX.

ORIGINAL PAGE IS
OF POOR QUALITY

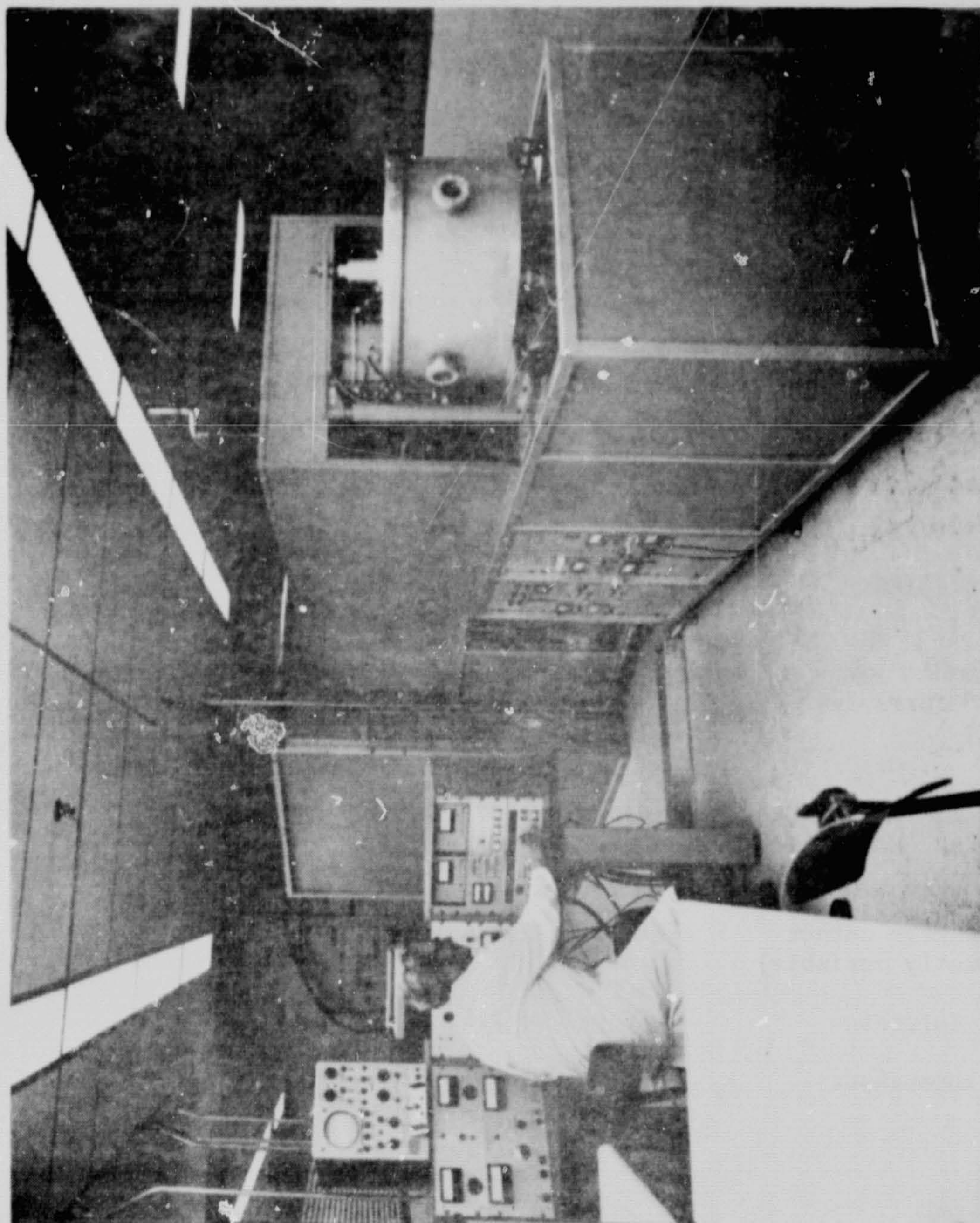


Figure 1. Accelerators, Inc., Model MP-200 ion implanter.

TABLE 1. PERFORMANCE SPECIFICATIONS OF ACCELERATORS, INC., MODEL MP-200 ION IMPLANTER

High voltage output (continuously variable)	10 to 200 keV
Output current	1.5 mA
RMS ripple (full voltage and full load)	0.05%
Regulation (for 10% line variation)	1.0%
Isolation transformer	3 kVA
Insulation	Oil
Beam scan	x-y scan, hybrid scan
Wafer throughput	300 wafers/hour (2 in. at 10^{12} ions/cm^2 dose)
Dose uniformity	2% across wafer
Dose reproducibility	2% wafer to wafer 2% batch to batch
Pumpdown time (to 2×10^{-6} Torr)	6 min

TABLE 2. PERFORMANCE SPECIFICATIONS OF EXTRION, INC., MODEL 200-1000

High voltage output (constantly variable)	5 to 200 keV
Output current	0.1 to 1.5 mA
Wafer throughput	13 wafer-lots/40 min at 1×10^{16} ions/cm^2 dose

C. Impurity Control

1. Impurity Distribution

The impurity profile of ions into amorphous material (such as SiO_2, Si_3N_4, or photoresist) or single crystal in a nonchanneling direction will be Gaussian, as shown in Fig. 2. The Gaussian profile can be described by the formula

$$N(x,E) = N_{max} \times \exp \left\{ -\frac{1}{2} \left[\frac{x - R(E)}{\Delta R(E)} \right]^2 \right\} \qquad (1)$$

where N_{max} is the peak concentration, $R(E)$ is the projected range, and $\Delta R(E)$ is the spread. This last term is also known as the straggle or standard deviation.

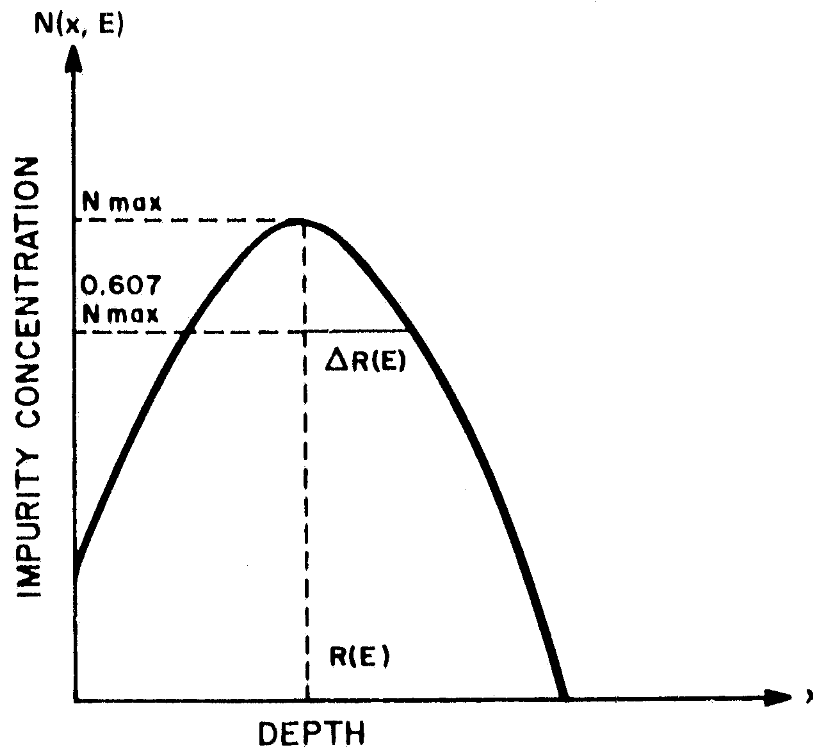


Figure 2. Impurity profile after ion implantation, plotted in semi-log scale.

The range and the spread of these implanted atoms depend on the mass of the bombarding ion and the mass of the substrate atoms. R(E) and ΔR(E) can be calculated from data compiled by nuclear physicists when the substrate is amorphous or a nonchanneling direction is used. The normal of wafers mounted on the carrousel is inclined 7° from the beam direction in order to avoid channeling effects. The distribution data for boron and phosphorus on a silicon substrate are presented in Table 3 and are plotted in Fig. 3.

2. Implant Dose

The dose of atoms received by the wafer is given by the formula

$$\text{DOSE} = \frac{I\ t}{q\ n\ A} \tag{2}$$

where

DOSE is the dose in number of ions per cm^2

I is the beam current in amperes

t is the implant time in seconds

$q = 1.602 \times 10^{-19}$ coulombs

n is the number of charges per ion (1 for B^+, 2 for B^{2+}, etc.)

A is the area implanted in cm^2

The implant dose is also calculated from the area underneath the profile curve. If the Gaussian distribution is assumed, then

$$\text{DOSE} = \int_0^\infty N(x,E)dx = \sqrt{\frac{\pi}{2}} \times N_{max} \times \Delta R \times \left[1 + \text{erf}\left(\frac{R}{\sqrt{2}\ \Delta R}\right)\right] \tag{3}$$

3. DOSE#

On the AI ion implanter, the integrated dose (i.e., total incident charge) is displayed by a four-digit readout which works in conjunction

TABLE 3. RANGE AND SPREAD OF BORON AND PHOSPHORUS IMPLANTED IN SOS WAFER

Beam Energy (keV)	Boron in Silicon		Phosphorus in Silicon	
	Range (R) (μm)	Spread (ΔR) (μm)	Range (R) (μm)	Spread (ΔR) (μm)
10	0.0351	0.0166	0.0137	0.0052
20	0.0702	0.0276	0.0246	0.0088
30	0.1057	0.0369	0.0353	0.0121
40	0.1404	0.0445	0.0461	0.0152
50	0.1748	0.0511	0.0571	0.0182
60	0.2087	0.0570	0.0684	0.0212
70	0.2417	0.0621	0.0797	0.0241
80	0.2735	0.0665	0.0912	0.0269
90	0.3038	0.0703	0.1027	0.0295
100	0.3330	0.0736	0.1142	0.0321
110	0.3617	0.0767	0.1258	0.0346
120	0.3898	0.0796	0.1375	0.0370
130	0.4173	0.0822	0.1492	0.0394
140	0.4442	0.0846	0.1609	0.0417
150	0.4704	0.0868	0.1727	0.0440
160	0.4960	0.0889	0.1844	0.0461
170	0.5209	0.0907	0.1961	0.0482
180	0.5451	0.0925	0.2078	0.0502
190	0.5689	0.0941	0.2194	0.0521
200	0.5922	0.0956	0.2310	0.0540
220	0.6378	0.0984	0.2542	0.0576
240	0.6819	0.1009	0.2774	0.0611
260	0.7248	0.1032	0.3007	0.0645
280	0.7663	0.1052	0.3238	0.0678
300	0.8067	0.1070	0.3469	0.0710
320	0.8459	0.1087	0.3698	0.0740
340	0.8841	0.1102	0.3925	0.0769
360	0.9211	0.1116	0.4150	0.0796
380	0.9573	0.1129	0.4373	0.0822
400	0.9926	0.1142	0.4592	0.0847
420	1.0272	0.1153	0.4809	0.0870
440	1.0611	0.1164	0.5021	0.0892
460	1.0944	0.1174	0.5230	0.0912
480	1.1270	0.1183	0.5434	0.0932
500	1.1590	0.1192	0.5637	0.0950
550	1.2367	0.1212	0.6139	0.0995
600	1.3112	0.1229	0.6632	0.1037
650	1.3830	0.1245	0.7116	0.1075
700	1.4523	0.1259	0.7591	0.1111
750	1.5193	0.1271	0.8056	0.1144
800	1.5843	0.1283	0.8511	0.1175
850	1.6474	0.1293	0.8955	0.1204
900	1.7089	0.1302	0.9888	0.1230
950	1.7687	0.1311	0.9811	0.1254
1000	1.8271	0.1319	1.0226	0.1277

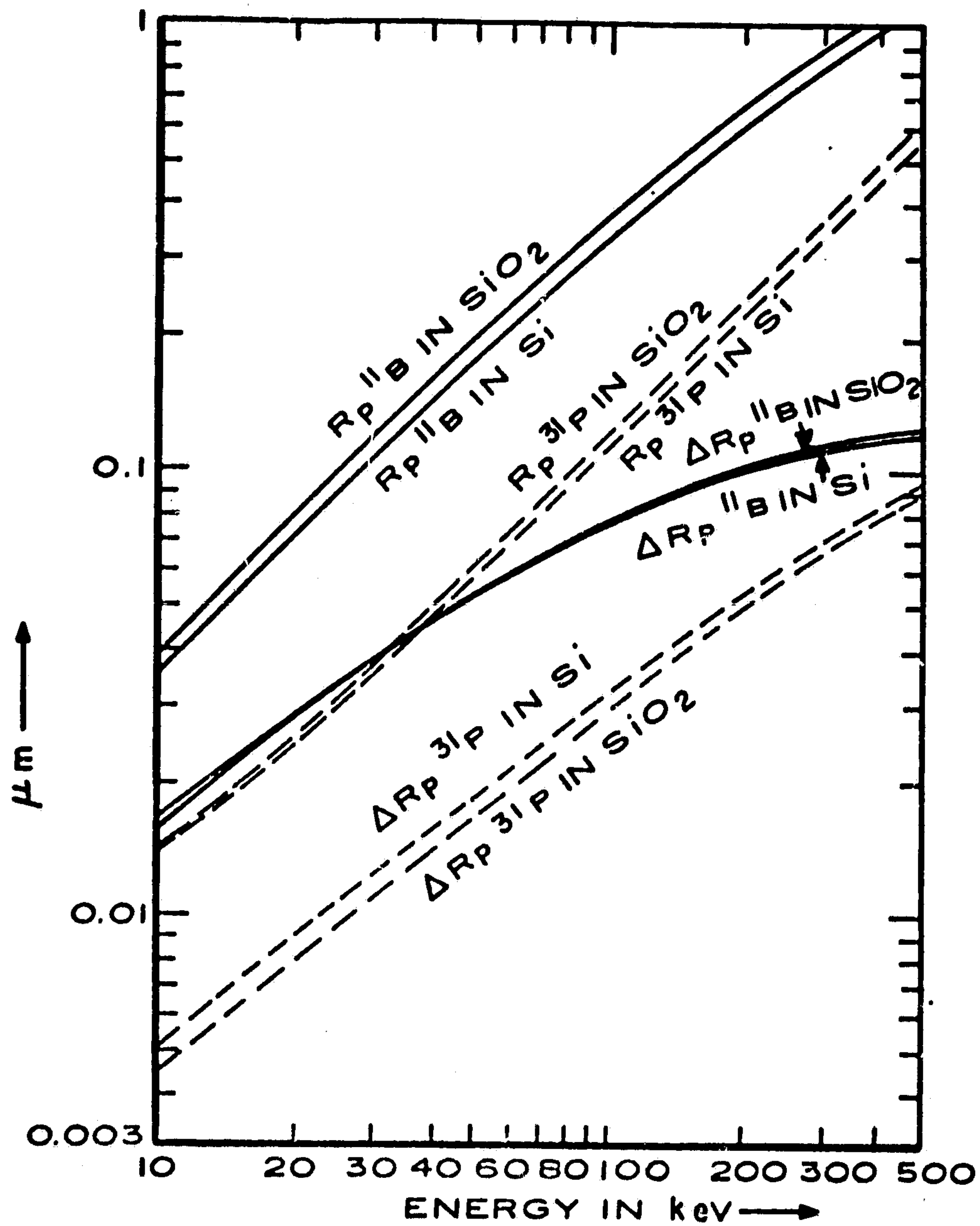


Figure 3. Rp and ΔRp for ^{11}B and ^{31}P as a function of implantation energy.

with the SCALE switch. The displayed number is called DOSE# and is given by

$$\text{DOSE\#} = \frac{Q}{\text{SCALE}} \tag{4}$$

where Q, the total charge that should be implanted, is given by

$$Q = q \times A \times \text{DOSE} \tag{5}$$

Therefore,

$$\begin{aligned} \text{DOSE} &= \frac{1}{qA} \times \text{SCALE} \times \text{DOSE\#} \\ &= F \times \text{SCALE} \times \text{DOSE\#} \end{aligned} \tag{6}$$

where F is a proportional constant and is given by

$$F = \frac{1}{q \times A} \tag{7}$$

The area of the target for a 2-in. carrousel is

$$A = \begin{cases} 30.05\ \text{cm}^2 & \text{for x-y scan} \\ 973.7\ \text{cm}^2 & \text{for hybrid scan} \end{cases}$$

$$\therefore \quad F = \begin{cases} 2.077 \times 10^{17}/\text{C-cm}^2 & \text{for x-y scan} \\ 6.411 \times 10^{15}/\text{C-cm}^2 & \text{for hybrid scan} \end{cases}$$

The F-values of the AI implanter for the various wafer-size carrousels are shown below:

Wafer Diam (in.)	x-y Scan ($\times 10^{16}$/C-cm^2)	Hybrid Scan ($\times 10^{15}$/C-cm^2)
2	20.77	6.411
2.25	16.11	6.002
3	9.769	4.711

Numerical Example: Let us compute DOSE# to implant a $1.4 \times 10^{11}\ cm^{-2}$ dose on 2-in. wafers at 2-μC scale. From Eq. (6):

$$DOSE\# = \frac{DOSE}{F \times SCALE}$$

$$= \begin{cases} 0.337 \text{ count for x-y scan} \\ 10.92 \text{ count for hybrid scan} \end{cases}$$

D. Radiation Damage and Anneal

One of the most important considerations in ion-implantation processes is the depth (range) and distribution of the implanted ions. It is possible to adjust the depth of the implant by varying the accelerating voltage and the concentration of the implant by varying the dose. These factors are dialed into the machine. The range distribution in single-crystal substrates depends strongly on the orientation of the crystal with respect to the implantation direction, i.e., on the channeling effects. Other problems inherent in the use of implantation techniques arise from the lattice-disorder and radiation-damage effects produced by the incident ion. As an implanted ion slows down and comes to rest, it makes many violent collisions with lattice atoms, displacing them from their lattice site. These displaced atoms can, in turn, displace others; the net result is the production of a highly disordered region around the path of the ion. At sufficiently high doses, these individual disordered regions may overlap, and a noncrystalline or amorphous layer is formed.

The isolated disordered regions and the amorphous layer have widely different anneal behaviors. In the case of silicon, the isolated disordered regions anneal at moderate temperatures of approximately 300°C. The amorphous layers anneal at an appreciably higher temperature, i.e., at approximately 600°C. The annealing which is necessary to activate the implanted atoms will cause some diffusion.

If one uses bulk diffusion coefficients, the impurity profile due to the diffusion during the annealing cycle can be calculated.

Radiation damage of SOS wafers will be annealed out during the high-temperature process steps, such as channel oxide growth and diffusion. Most of the implanted impurities are also activated during the high-temperature processes and require no extra anneal.

III. SUBSTRATE IMPLANTATION

A. Introduction

The CMOS/SOS double-epi process requires two successive epitaxial depositions (p- and n-type) and two photoresist and etching steps to define epi-islands. The concentrations of both epitaxial films are in the range of 3 to 5×10^{15} cm^{-3}. Extremely careful control is needed because the doping levels are very light and the circuit performance is critically dependent upon them. An important aspect of the application of ion implantation into the semiconductor is that the number of implanted ions is controlled by the external system. This lets us use the same starting material for various processes and applications.

Application of ion implantation to the CMOS/SOS process has several potential advantages: (1) It requires only one epitaxial film growth. The film can be intrinsic and requires no impurity doping during the deposition cycle. Therefore, the same starting SOS wafers can be used for various processes. (2) Both p- and n-islands can be defined with one mask which eliminates a critical photoresist and etching step and allows closer spacing of the islands. (3) The doping is uniform across the wafer and reproducible from run to run.

B. Ion-Implant (I^2) Process

Excellent results have been obtained on ion-implantation runs, and two basic processes for doping the epitaxial films were devised: single-ion implant (I^2 or $1I^2$) and double-ion implant ($2I^2$). Many variations can be achieved by the use of ion implantation. Four processes proved to be satisfactory for the p-gate CMOS/SOS process; the schematic diagrams are shown in Figs. 4 and 5.

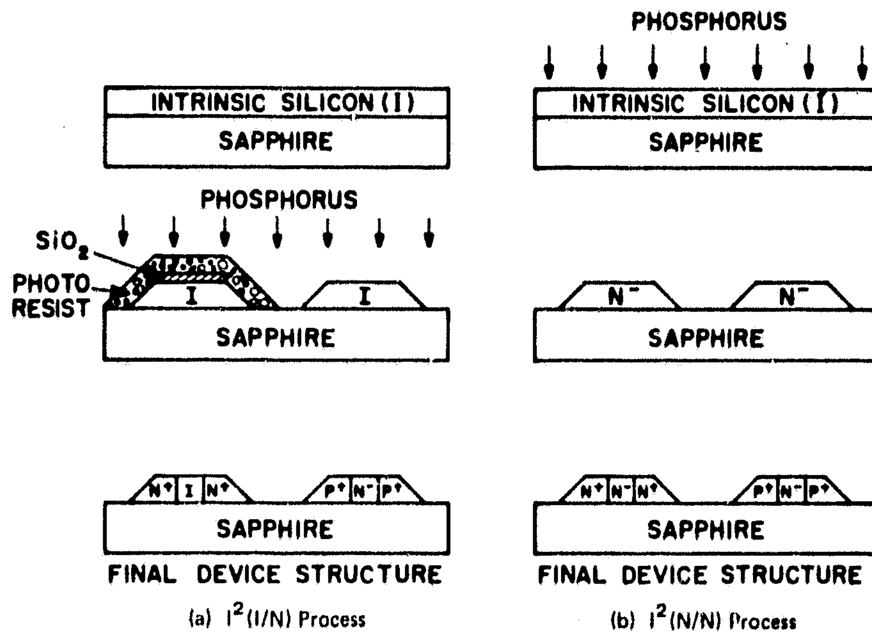


Figure 4. Single-ion-implantation process.

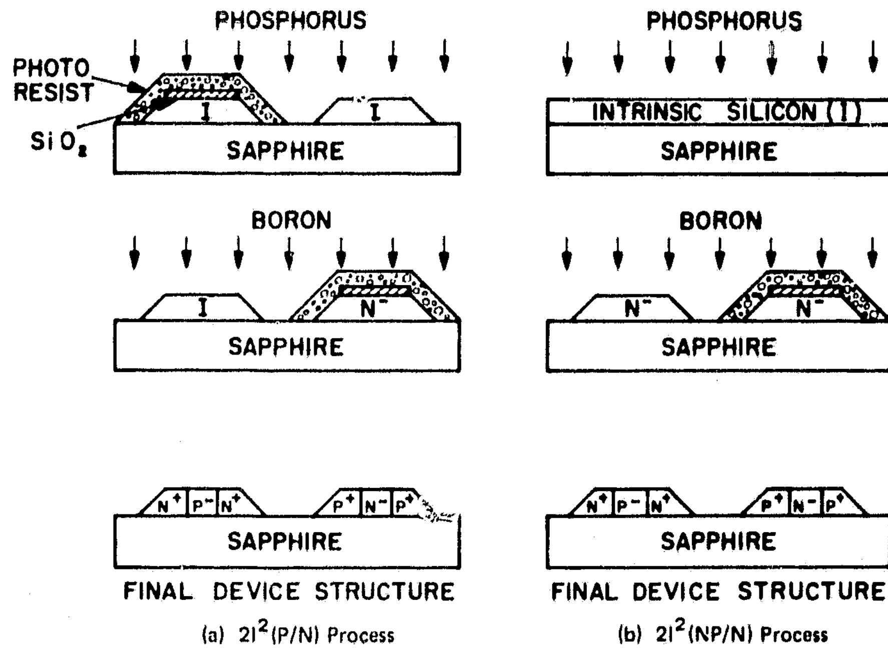


Figure 5. Double-ion-implantation process.

1. $I^2(I/N)$ Process

The intrinsic SOS film is grown in the standard manner with no intentional doping. A thermal oxide is grown and is etched by means of a mask to form the device islands for both n- and p-channel transistors. The epi-islands are etched by use of the thermal oxides as an etch mask.

In the implantation-photoresist step, the oxide etching on the p-channel island is followed by an ion-implantation step, using phosphorus at a dose of 1.4×10^{11} cm^{-2} with a beam energy of 150 keV. This places the dopant peak approximately 0.17 μm below the surface. After stripping the photoresist and removing the oxide, we are ready for the growth of the channel oxide. At this step the n-channel island is intrinsic (I) and the p-channel island is n-type (N). Therefore, this single implant process is named the $I^2(I/N)$ process.

Next, the "standard" process is applied to complete the device fabrication.

2. $I^2(N/N)$ Process

The above-mentioned $I^2(I/N)$ process was satisfactory for the low-threshold-voltage circuits; however, it takes two photoresist steps. Two attempts were made to reduce one photoresist step by (1) implanting phosphorus over the entire surface of the film, and then defining the epi-islands, and (2) defining the islands and then implanting the phosphorus.

Both islands have identical concentrations and are of the same type (N/N). Even though the substrate of the n-channel transistor is n-type, the device is in enhancement mode due to deep depletion of the substrate by the polysilicon-gate work function.

3. $2I^2(P/N)$ Process

The single-ion-implantation (I^2) process restricts itself to a low-threshold-voltage process. To increase both reliability and

radiation resistance, it is desirable to increase the threshold voltage of both channels. This can be achieved by a double-implant process ($2I^2$).

The same intrinsic SOS films can be used for the double-implant process; i.e., both epi-islands are etched using the same photoresist step as in the single-implantation process. n-Channel islands are shielded by means of the second photoresist step and by implanting with phosphorus. Similarly, p-channel islands are shielded by the third photoresist step and implanting with boron. The photoresist and oxide are removed, and the "standard" process follows.

4. $2I^2$(NP/N) Process

The above-mentioned $2I^2$(P/N) process gives the best control over both channels; however, it requires three photoresist steps to prepare the epi-islands. An attempt was made to simplify the process by implanting phosphorus over the entire surface of the SOS wafer, defining the islands, and then implanting boron on n-channel islands by shielding the p-channel islands. The n-channel islands are exposed to two implantations, n-type and p-type (NP), resulting in a net p-type impurity. In this way true enhancement-mode devices are obtained on both channels with one photoresist step less than is needed in the $2I^2$(P/N) process.

IV. GATE IMPLANTATION

A. Introduction

The control of ion implantation into polysilicon on POS (polysilicon-oxide-silicon) structure and subsequent heat treatment is very critical to wafer processing. The intent is to dope the impurities as close to the polysilicon-oxide interface as possible after the necessary thermal cycles. The penetration of impurity ions into the channel oxide and substrate through polysilicon will be detrimental to the device characteristics, stability, and reliability. If the penetration of the impurity ions is too shallow and the poly-SiO_2 interface is not doped adequately, this will degrade V_t control and also introduce undesirable capacitance.

B. Experiment

Implantation of boron and phosphorus ions into polysilicon film was performed. In order to study the penetration of ion species through polysilicon, polysilicon was deposited on a stepped oxide. The stepped oxides were grown on the same bulk-silicon wafer by the use of photoresist techniques. The cross-sectional view of a sample is shown shown in Fig. 6.

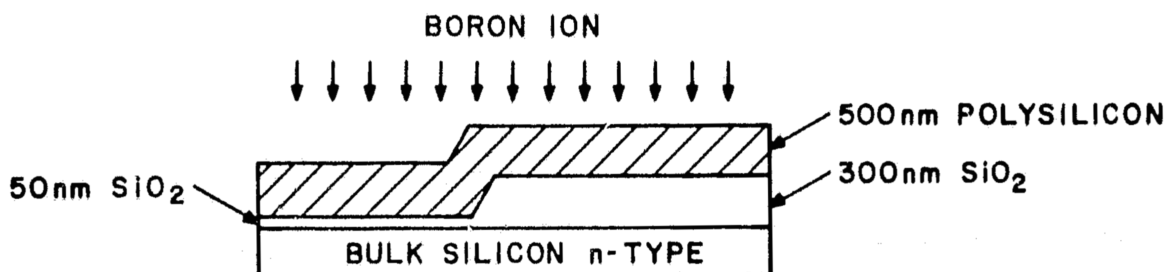


Figure 6. Cross-sectional view of a POS sample designed to study impurity penetration through the polysilicon film.

Four different implant dosages were used for both boron and phosphorus. The accelerating energies were picked so that the projected range is 210 nm. The implanted wafers were exposed in one of two annealing cycles. The ion-implantation schedules used and the subsequent annealing are shown below:

	Boron	Phosphorus
Energy (keV)	60	180
Projected range (nm)	210	210
Dose (cm^{-2})	2 to 16 × 10^{15}	2 to 16 × 10^{15}
Anneal 1	90 min in N_2 at 850°C	
Anneal 2	15 min in N_2 at 1050°C	

C. Results

Sheet resistances were measured on all wafers as a function of dosage and annealing cycle. The results of boron and phosphorus implantation are summarized in Tables 4 and 5, and are plotted in Figs. 7 and 8.

TABLE 4. BORON IMPLANTATION (WITH E = 60 keV) ON 500-nm POLYSILICON FILM

Dose (#/cm^2)	Sheet Resistance (Ω/□) 90 min N_2 at 850°C	15 min N_2 at 1050°C
2 × 10^{15}	151.6 ±1.95	100.8 ±0.84
4 × 10^{15}	100.0 ±1.23	51.7 ±0.41
8 × 10^{15}	69.2 ±0.47	32.9 ±0.54
16 × 10^{15}	65.2 ±1.95	29.8 ±1.67

TABLE 5. PHOSPHORUS IMPLANTATION (WITH E = 180 keV) ON 500-nm POLYSILICON FILM

Dose ($\#/cm^2$)	Sheet Resistance ($\Omega/\square$)	
	90 min N_2 at 850°C	15 min N_2 at 1050°C
2×10^{15}	204.2 ±14.87	134.2 ±5.50
4×10^{15}	77.5 ±2.14	63.8 ±2.17
8×10^{15}	40.2 ±1.31	31.9 ±0.53
16×10^{15}	25.5 ±0.36	16.5 ±0.31

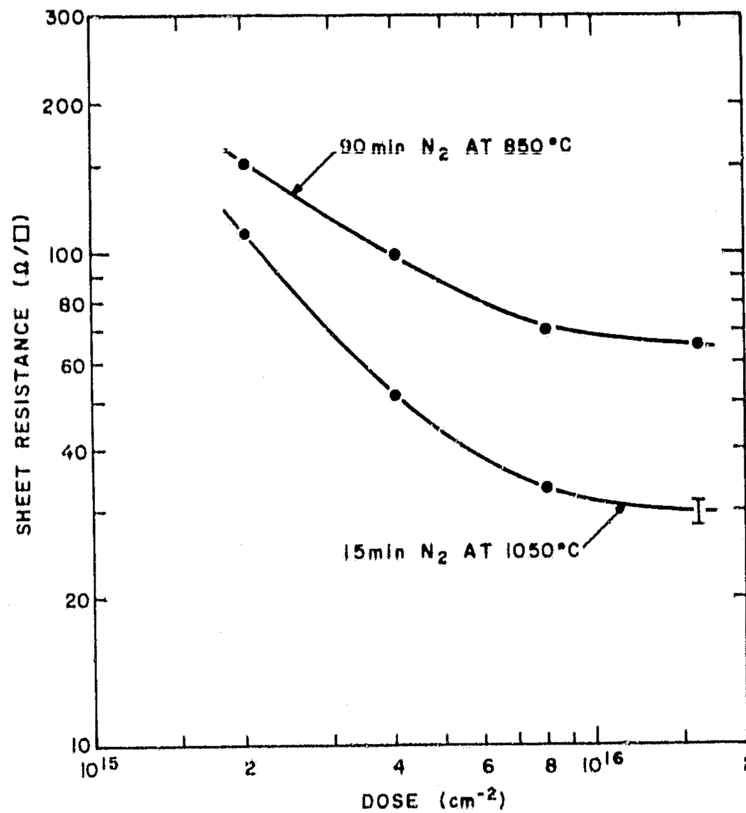


Figure 7. Sheet resistance of 500-nm polysilicon film implanted with 60-keV boron.

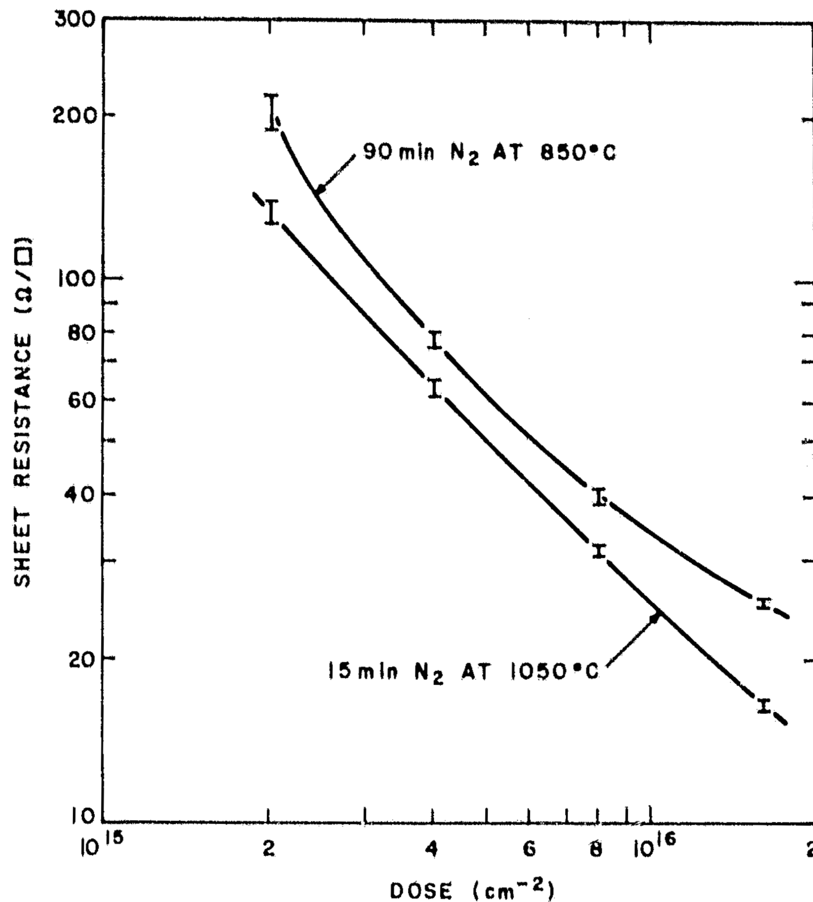


Figure 8. Sheet resistance of 500-nm polysilicon film implanted with 180-keV phosphorus.

After the sheet resistance of polysilicon films was measured, the poly and stepped oxide were stripped. The wafers were evaluated using spreading-resistance and four-point probes to check the penetration of the impurity species. It was found that the bulk-silicon surface resistivity was uniform over the entire wafer, indicating that no impurity ions had penetrated through the 500-nm polysilicon films.

These results indicate that ion-implantation technique can be applied for the doping of polysilicon films for either boron- or phosphorus-doped gates.

V. SOURCE-DRAIN IMPLANTATION

A. Introduction

Source-drain implantation is well understood, and the range (penetration depth) of impurity ions is not as critical as the poly-gate implant as long as penetration is deep and the silicon-sapphire interface is reached.

B. Experiment

A total of 16 SOS wafers and 8 bulk-silicon control wafers were implanted with various doses using 60 keV of boron and 180 keV of phosphorus. Activation was performed in nitrogen ambient for 90 min at 850°C or 30 min at 1050°C. After the activation the sheet resistance was measured on all wafers (SOS and bulk silicon), and the junction depth was measured on bulk-silicon wafers by a grooving and strain technique (Ref. 1).

C. Results

The sheet resistance and junction depth of the PMOS and NMOS source-drain experiments are measured as a function of implant dose and activation cycles. The results are presented in Tables 6 and 7 and are plotted in Figs. 9 and 10.

1. B. McDonald and A. Goetzberger, "Measurement of the Depth of Diffusion Layer in Silicon by Grooving Method," J. Electrochem. Soc. 109, 141 (1962).

TABLE 6. BORON IMPLANTATION WITH E = 60 keV ON 600-nm SOS AND n-TYPE BULK-SILICON WAFERS

Dose (cm^{-2})	90 min N_2 at 850°C			30 min N_2 at 1050°C		
	SOS	Bulk-Si		SOS	Bulk-Si	
	R_s (Ω/□)	R_s (Ω/□)	xj (nm)	R_s (Ω/□)	R_s (Ω/□)	xj (nm)
1×10^{15}	130	140	740	103	94	1000
2×10^{15}	100	107	820	55	50	1020
4×10^{15}	61	81	840	33	31	1120
8×10^{15}	46	65	850	18	14	1440

TABLE 7. PHOSPHORUS IMPLANTATION WITH E = 180 keV ON 600-nm SOS AND p-TYPE BULK-SILICON WAFERS

Dose (cm^{-2})	90 min N_2 at 850°C			30 min N_2 at 1050°C		
	SOS	Bulk-Si		SOS	Bulk-Si	
	R_s (Ω/□)	R_s (Ω/□)	xj (nm)	R_s (Ω/□)	R_s (Ω/□)	xj (nm)
1×10^{15}	88	67	870	85	67	1040
2×10^{15}	48	40	970	46	36	1090
4×10^{15}	25	22.3	1140	24	19	1130
8×10^{15}	15	12.6	1200	14	11.7	1240

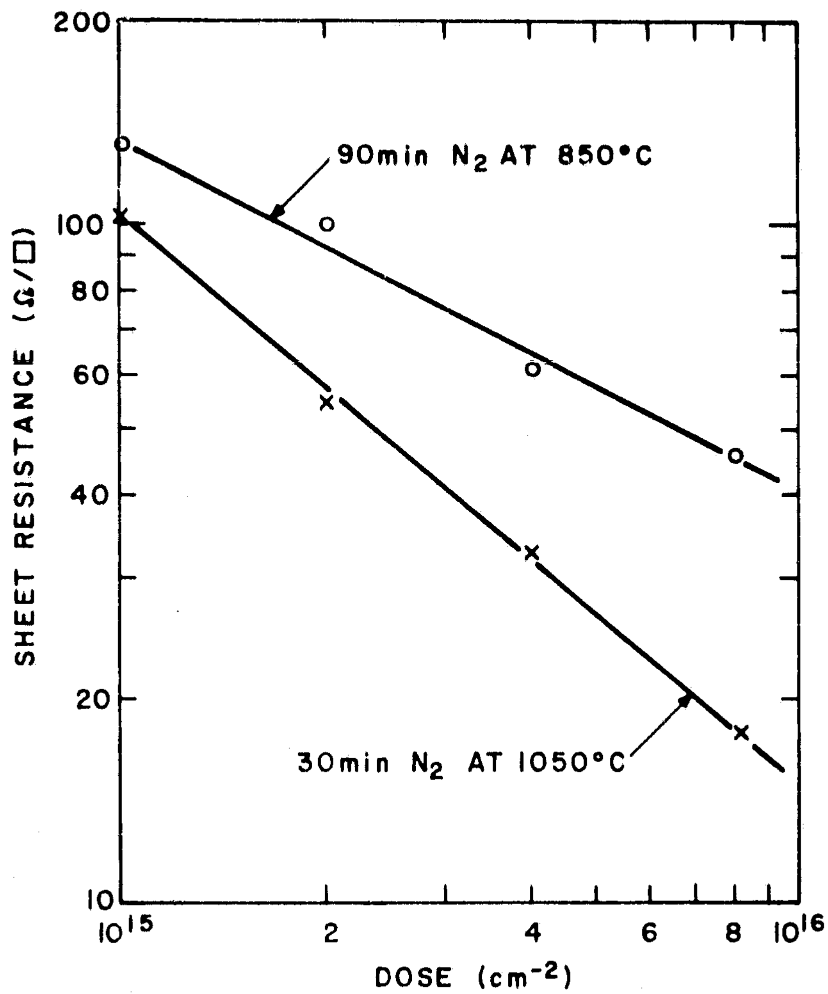


Figure 9. Sheet resistance of 600-nm SOS film implanted with 60-keV boron.

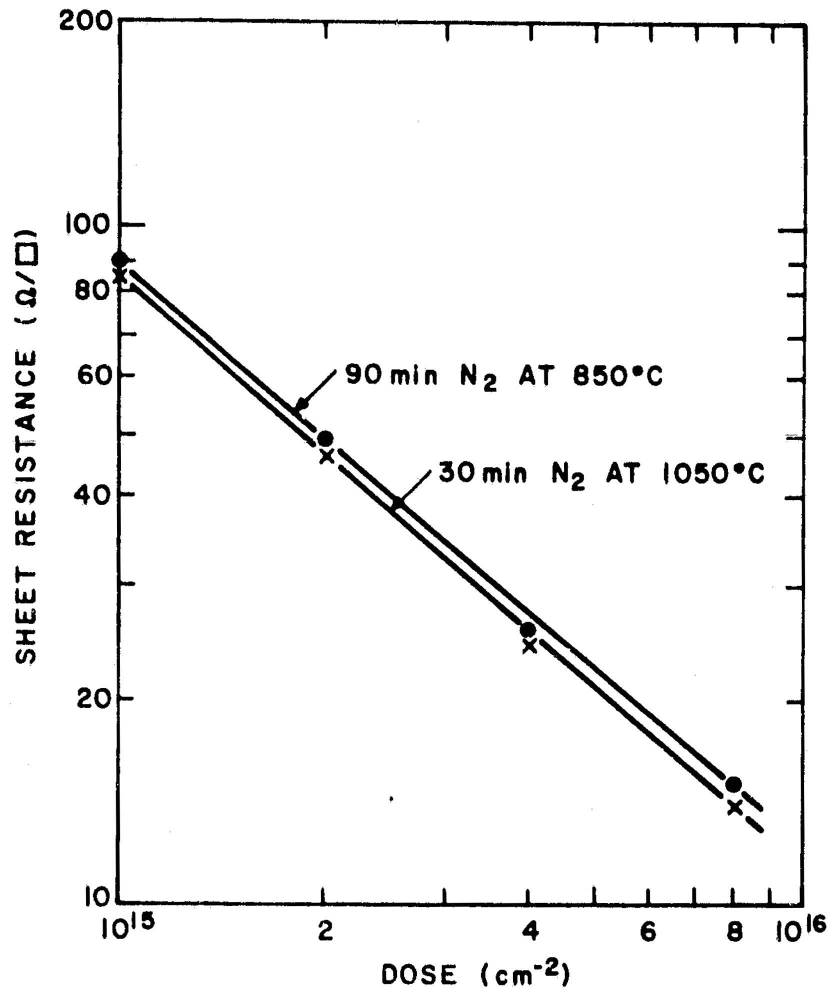


Figure 10. Sheet resistance of 600-nm SOS film implanted with 180-keV phosphorus.

VI. TEST VEHICLE

The SOS test chip (TSC 010) contains sufficient devices and sufficient accessibility to measure all device characteristics, process parameters, and circuit performance without becoming cumbersome. Figure 11 shows the test chip which contains 138 transistors on a 70 x 70 mil chip area with 24 I/O pads. As shown in Table 8, it

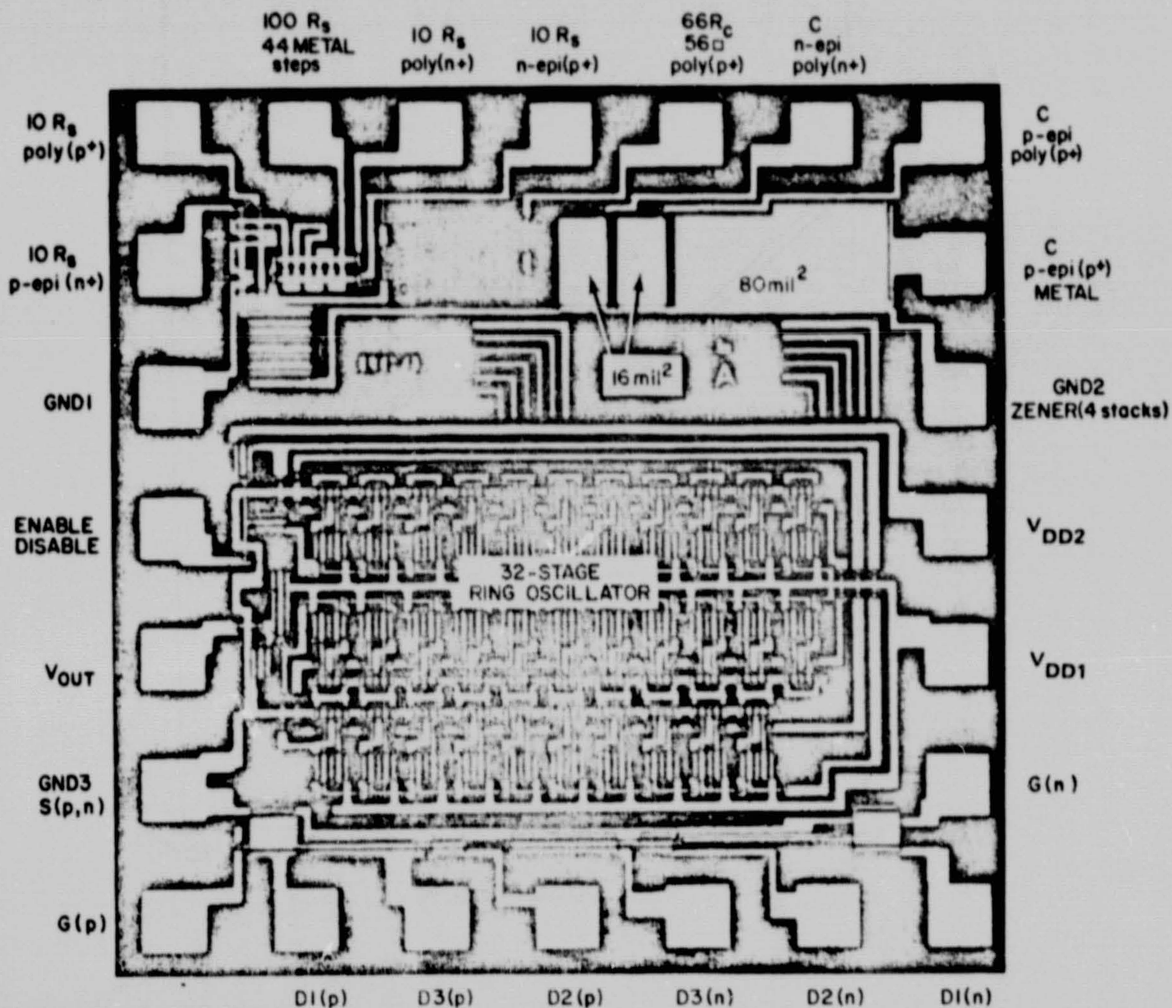


Figure 11. Photomicrograph of the test chip TCS 010.

ORIGINAL PAGE IS
OF POOR QUALITY

TABLE 8. TEST VEHICLES ON SOS CHIP

Test Vehicle	Quantity	Type	Parameter
Transistor	3 NMOS 3 PMOS	L1=2.0 mil W1=2.8 mil L2=0.3 mil W2=2.0 mil L3=0.3 mil W3=6.0 mil	V_t, I_{dss}, BV_{ds} BV_{ox}, K', X_1
Diffusion Test	4	n^+ on NMOS p^+ on PMOS Poly gate on NMOS Poly gate on PMOS	R_S (N-DS) R_S (P-DS) R_S (N-poly) R_S (P-poly)
Metallization Test	2	Continuity over step, Contract	R_S, step coverage R_c
Capacitor	3	Poly on n-epi Poly on p-epi Metal on p-epi	t_{ox}, BV(SiO_2) Q_{ss}, C_{ox}, N_S
Zener Diode	1	Four-stack	BV (Zener)
Ring Oscillator	1	32-stage	Speed, life

includes three NMOS and three PMOS transistors with various width/length ratios, four resistors, two devices to test metal continuity and contact resistance, three capacitors, one four-stack Zener diode, and one 32-stage ring oscillator. These permit measurement of threshold voltage (V_t), leakage current (I_{dss}), source-drain breakdown voltage (BV_{ds}), channel-oxide breakdown voltage (BV_{ox}), channel conductance (K'), and lateral diffusion (X_1). Sheet resistance test patterns exist for source-drain diffusion and the polysilicon gate of both channels.

The metal pattern crosses over 44 silicon-epi and polysilicon steps, giving a good indication of whether or not a metal step-coverage problem exists. There is also a series of 56 metal-to-epi and

metal-to-poly contacts to ensure the quality of metal contacts. A Zener diode has been included so that breakdown voltage can be measured.

For qualitative, off-line evaluations of the processing, three MOS capacitors have been included. These will permit measurement of oxide thickness, breakdown voltage, surface-state density and substrate doping (N_S). These data will aid in more exact interpretation of the MOS transistor data.

A four-stack Zener diode is included to test the gate input protective device. The Zener breakdown voltages (BV) are measured at different current levels.

The SOS test chip includes a 32-stage ring oscillator, each stage consisting of a two-input NOR gate. Its schematic diagram is shown in Fig. 12. The output waveform is periodic and has a one-zero-zero repeating pattern. This vehicle is intended primarily for speed and circuit performance measurements.

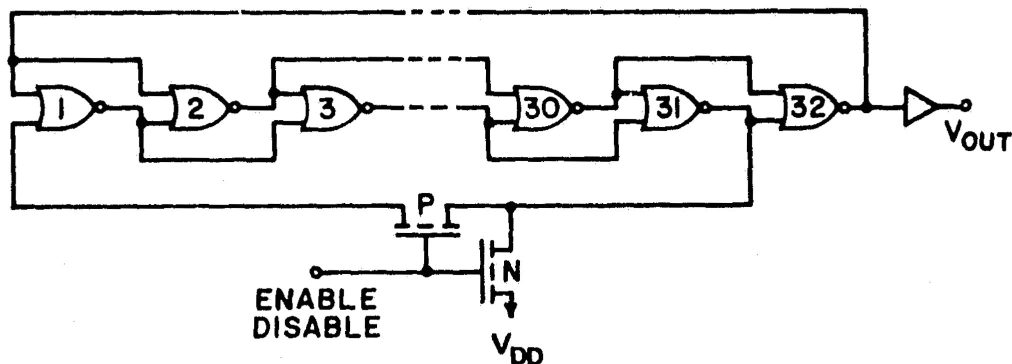


Figure 12. 32-stage ring oscillator.

VII. ALL-ION-IMPLANTATION PROCESS

A. Introduction

It is the object of this study to develop an all-ion-implantation process for the fabrication of CMOS devices on SOS wafers so as to obtain p^+ silicon-gate enhancement devices. The major advantages of this process lie in the elimination of the two-step epi deposition and reproducibility of implant doping levels. Source-drain implantation should make a significant impact on yield, since both etching and doping control of deposited oxides can be a problem with SOS circuits.

Processing of two lots (Lot S1456 and S1605) was completed by means of the TCS 010 test chip. The process parameters and the circuit performance of the first lot (Lot S1456) were analyzed, and a slight modification was done on the second lot (Lot S1605) to improve the device characteristic.

B. Process

The qualitative description of the process used for the above two lots is shown in Fig. 13. The silicon film is grown in the standard manner with no intentional doping. The layer is normally 500 to 600 nm thick. In the implantation step that follows, phosphorus is used at a dose of 1.4 to 2.4×10^{11} cm^{-2} and an energy of 150 keV. This places the dopant peak at approximately 170 nm below the silicon surface. A thin oxide is then grown and etched with the both-islands mask to form the epi-substrates for both n- and p-channel transistors. This thermal oxide is used as the etch mask for the KOH-isopropanol silicon etch. Epi-islands of PMOS devices are shielded with photoresist, and boron is implanted to control the NMOS threshold voltage at a dose of 1.4 to 2.4×10^{11} boron/cm^2 and an energy of 100 keV. The photoresist and mask oxide are then stripped.

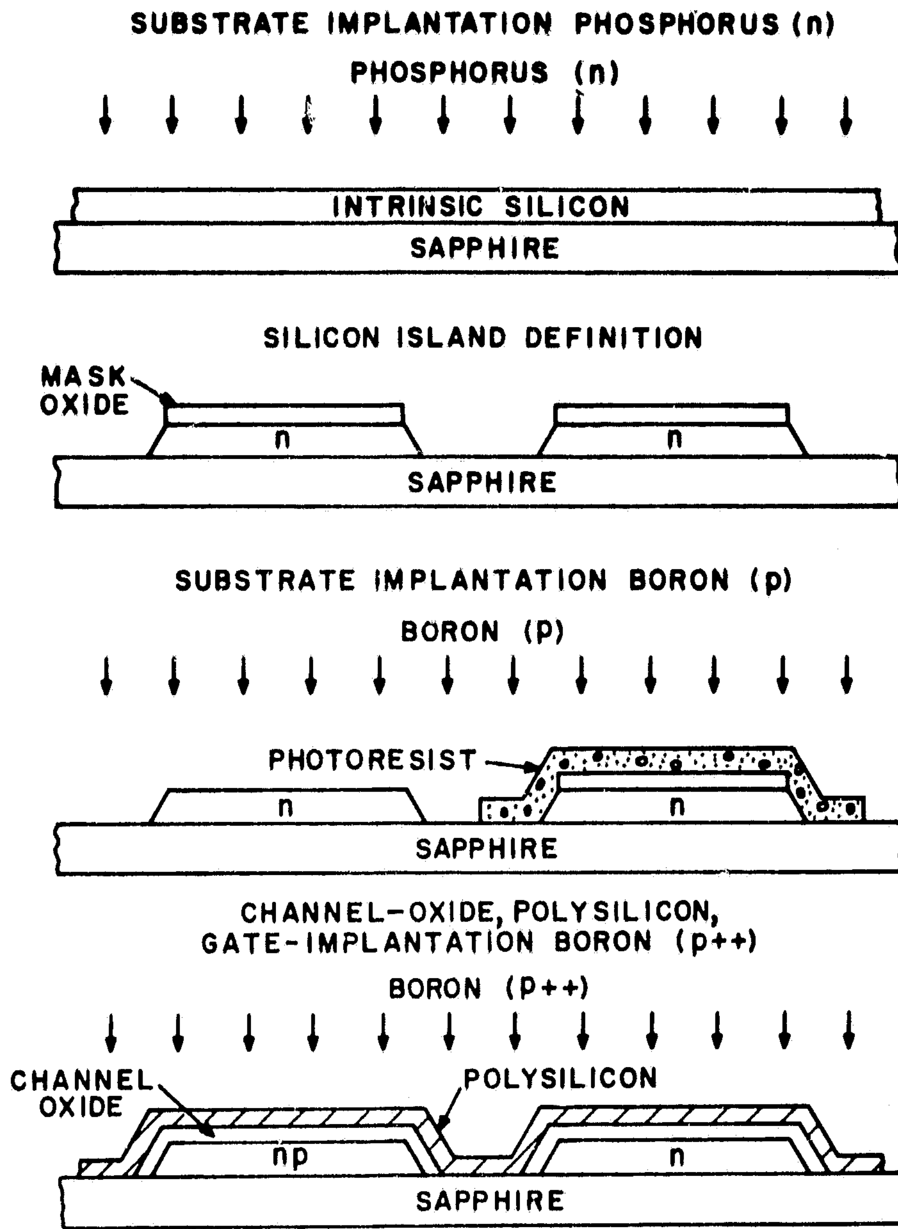


Figure 13. Cross-sectional view of all-ion-implantation process for silicon-gate CMOS/SOS process.

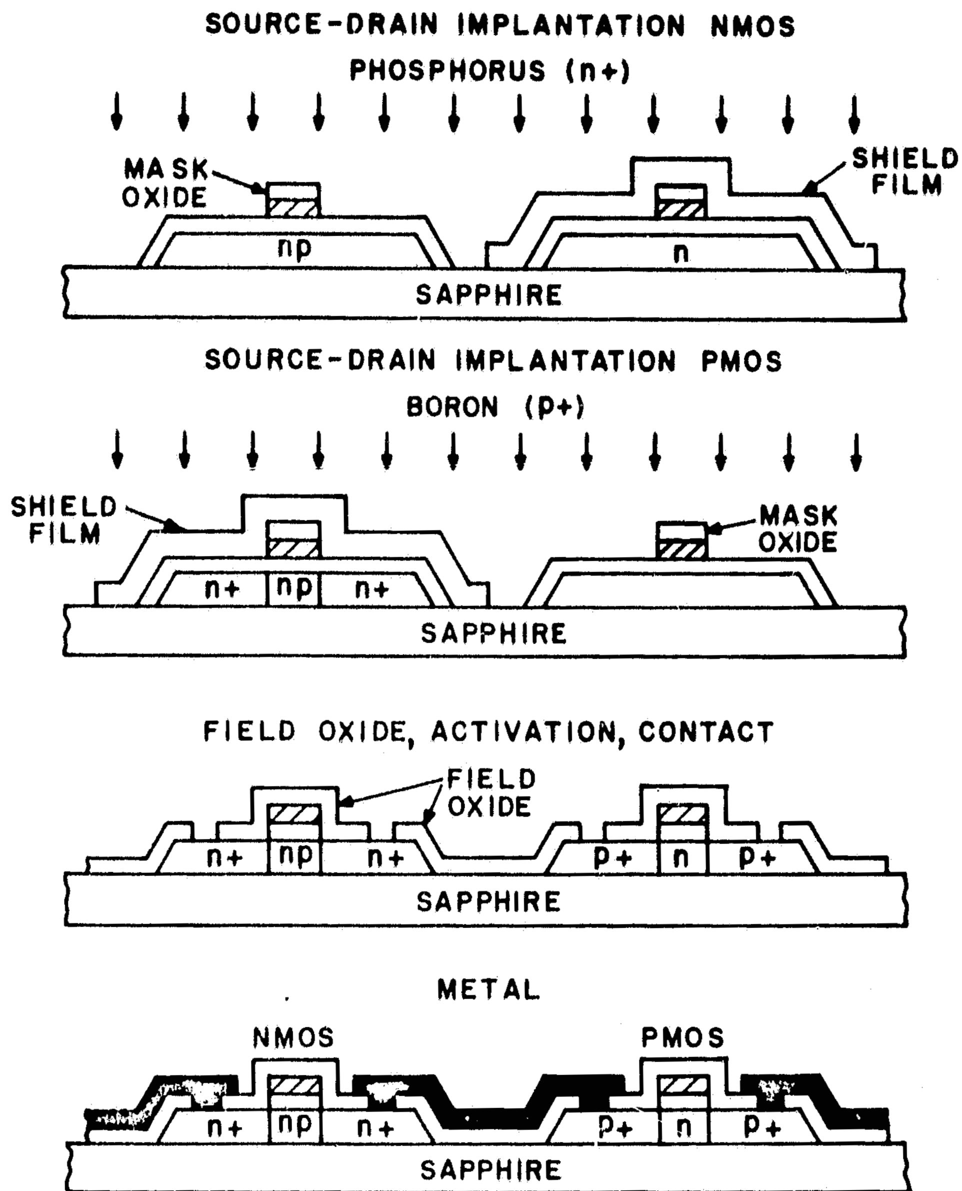


Figure 13. (Continued).

The 110 $\pm$5-nm channel oxide is then grown in steam-HCl at 940°C. The 500-nm-thick polysilicon layer is grown without intentional doping. The gate was implanted with a dose of 4 to 5 x 10^{15} boron/cm^2 at an energy of 50 keV. The 250 $\pm$25-nm-thick oxide is deposited and patterned by means of a poly mask, and then polysilicon is etched by means of plasma.

A shield film is deposited and etched by use of the n^+ mask. The source-drain implantation for the NMOS is then performed with a dose of 1 to 2 x 10^{15} phosphorus/cm^2 at an energy of 170 keV. The PMOS islands are shielded during the above implantation. The p^+ photoresist pattern is performed so that shield film is left on NMOS islands. The source-drain implantation for the PMOS is performed with 3 to 4 x 10^{15} boron/cm^2 at an energy of 70 keV. The energy for both the phosphorus and boron is chosen so that the depth of the peak concentration occurs at approximately 200 nm below the surface of the silicon film.

After stripping of the shield film, 800-nm-thick field oxide is deposited. All of the implanted impurities are activated simultaneously for 15 min at 1050°C, and then oxides are densified and surface states are annealed at lower temperatures. Contacts are etched by means of the contact mask; then the metal mask is used to deposit and etch 1.2 $\pm$0.2-µm-thick aluminum. A protective oxide is deposited and then etched by means of a bond-pad mask. The process is then completed, and the wafers are ready for evaluation.

A more detailed description of these processing steps is presented in outline form below:

A. Sapphire wafer
   1. Incoming inspection
   2. Sapphire clean
   3. Predeposition anneal (30 min H_2 at 1200°C)
   4. Sapphire inspection

B. Silicon-film deposition
   1. Deposit intrinsic silicon film (0.6 $\pm$0.1 μm) (20 s SiH_4 at 960°C)
   2. Visual inspection
   3. Evaluate resistivity
   4. Measure thickness variation

C. Phosphorus implantation
   Implant phosphorus (n)
   Dose = 1.8×10^{11} cm^{-2} at E = 150 keV

D. Both islands
   1. Standard clean
   2. Grow silicon dioxide (15 min steam at 940°C)
   3. Photoresist with islands mask
   4. Etch oxide, visual inspection
   5. Remove photoresist
   6. Etch silicon (KOH-alcohol), visual inspection

E. Boron implantation
   1. Photoresist with well mask
   2. Etch oxide; do not remove photoresist
   3. Implant boron (p)
      Dose = 2×10^{11} cm^{-2} at E = 100 keV
   4. Remove photoresist
   5. Etch oxide

F. Channel oxide/polysilicon deposition
   1. Standard clean
   2. Grow channel oxide (25 to 30 min HCl-steam at 940°C)
   3. Deposit polysilicon (0.5 $\pm$0.05 μm)

G. Gate implantation/definition
   1. Scrub wafers
   2. Implant boron (p^{++})
      Dose = 5×10^{15} cm^{-2} at E = 50 keV
   3. Standard clean
   4. Deposit oxide (0.2 to 0.25 μm)
   5. Photoresist with polysilicon mask
   6. Etch oxide (buffered HF)
   7. Remove photoresist
   8. Etch polysilicon (plasma)

H. N^+ implantation
   1. Standard clean
   2. Deposit aluminum (1.2 $\pm$0.2 μm)
   3. Photoresist with n^+ mask
   4. Etch aluminum; do not remove photoresist
   5. Bake photoresist

6. Implant phosphorus (n^+)
   Dose 1 = 1×10^{15} cm^{-2} at E1 = 180 keV
   Dose 2 = 1×10^{15} cm^{-2} at E2 = 70 keV
7. Remove photoresist and aluminum

I. P^+ implantation
1. Standard clean
2. Deposit aluminum (1.2 $\pm$0.2 μm)
3. Photoresist with p^+ mask
4. Etch aluminum; do not remove photoresist
5. Bake photoresist
6. Implant boron (p^+)
   Dose = 5×10^{15} cm^{-2} at E = 70 keV
7. Remove photoresist and aluminum
8. Etch oxide on polysilicon (carefully)

J. Field oxide/diffusion
1. Standard clean
2. Deposit oxide (0.8 to 0.85 μm)
3. Scrub wafers
4. Standard clean
5. Diffuse (15 min N_2 at 850°C)
6. Densify (15 min steam at 940°C)
7. Anneal (15 min forming gas at 500°C)

K. Contact
1. Photoresist with contact mask
2. Etch oxide (buffered HF); visual inspection
3. Remove photoresist

L. Metallization
1. Standard clean
2. Dip in H_2O-HF (50:1)
3. Deposit aluminum (1.2 $\pm$0.2 μm)
4. C-V test
5. Photoresist with metal mask
6. Etch metal; visual inspection
7. Remove photoresist

M. Bond pad
1. Standard clean
2. Deposit protective oxide (0.55 to 0.65 μm)
3. Alloy aluminum (15 min forming gas at 450°C)
4. Photoresist pad mask
5. Etch oxide (buffered HF-acetic ac.); visual inspection
6. Remove photoresist

N. Wafer map

O. Circuit probe

VIII. RESULTS

A. General

Five ion-implantation steps were utilized on Lots S1456 and S1609: (1) phosphorus implantation for PMOS substrate, (2) boron implantation for NMOS substrate, (3) high-dosage boron implantation for polysilicon gate, (4) high-dosage phosphorus implantation for NMOS source-drain, and, finally, (5) high-dosage boron implantation for PMOS source-drain. The implantation data of the above two lots are presented in Tables 9 and 10.

After completion of the process, TCS 010 data were taken on each wafer by means of the Datatron Tester.* Statistical analyses of various parameters are presented in Tables 11 and 12.

B. Transistor Characteristics

Device characteristics for NMOS and PMOS from Lots S1456 and S1609 are shown in Figs. 14 and 15. The curves are entirely comparable with those from devices made by conventional processing using diffusions from doped oxides. The gate dielectric breakdown voltage was in the 60- to 70-V range. The sheet resistance of NMOS source-drain is 162.45 Ω/□ for Lot S1456; this is slightly high and produced undesirable source-drain contact problems on the NMOS transistor. The phosphorus implantation dosage was 1.0×10^{15} cm^{-2}. The dosage was doubled on the second lot (S1609), and, thus, the sheet resistance was dropped to 99.28 Ω/□.

The gate-transfer characteristics of the test transistors from Lot S1609 are shown in Fig. 16. The drain current is obtained on transistors with L = 6.35 μm (0.25 mil) and W = 50.8 μm (2.0 mil) as a function of gate voltage at V_d = 10 V. The devices illustrated here are enhancement mode with V_{tn} = 0.85 V and V_{tp} = 1.0 V at I_d = 1 μA, and they are well balanced because ΔV_t is only 0.15 V. The source-drain leakage current is I_{dssn} = 18 pA and I_{dssp} = 45 pA.

*Datatron Inc., Santa Ana, CA.

TABLE 9. IMPLANTATION DATA FOR LOT S1456

Implantation	Target	Impurity Source	Dose (cm^{-2})	E (keV)	Results
Substrate	PMOS	Phosphorus	1.8×10^{11}	150	V_{tp} = 0.60 V EM
	NMOS	Boron	2.0×10^{11}	100	V_{tn} = 0.97 V EM
		(Phosphorus)	(1.8×10^{11})	(150)	
Gate	Poly	Boron	4.0×10^{11}	50	R_S = 63.55 Ω/□
Source-Drain	NMOS	Phosphorus	1.0×10^{15}	180	R_S = 162.45 Ω/□
	PMOS	Boron	3.0×10^{15}	70	R_S = 44.54 Ω/□

EM = Enhancement mode.

TABLE 10. IMPLANTATION DATA FOR LOT S1609

Implantation	Target	Impurity Source	Dose (cm^{-2})	E (keV)	Results
Substrate	PMOS	Phosphorus	1.8×10^{11}	150	V_{tp} = 0.79 V EM
		Boron	2.0×10^{11}	100	
	NMOS	(Phosphorus)	(1.8×10^{11})	(150)	V_{tn} = 1.06 V EM
Gate	Poly	Boron	5.0×10^{15}	50	R_S = 51.90 Ω/□
Source-Drain	NMOS	Phosphorus	1.0×10^{15}	170	R_S = 99.28 Ω/□
	PMOS	Boron	1.0×10^{15}	70	R_S = 32.65 Ω/□
			5.0×10^{15}	70	

EM = Enhancement mode.

TABLE 11. INDIVIDUAL-LOT ANALYSIS (SOS) OF LOT S1456

LOT=S1456	TYPE=TCS010	PROC =ALL-I^2	RCA
EPI=0.6μm	DATE=02/23/77-04/06/77	#CHIP= 22	SSTC
		YIELD=413/439 (94%)	

DEVICE PARAMETERS

		N-CHANNEL			P-CHANNEL		
		AVG	STDV	#WC	AVG	STDV	#WC
TR1	VT (OA,V)	1.04	0.19	22	0.68	0.09	22
	IDSS (NA)	2.42	1.43	22	2.43	0.55	22
	BVDS (V)	31.26	1.32	22	31.07	0.14	22
	K (μA/V2)	12.95	1.31	22	5.36	0.32	22
TR2	VT (OA,V)	0.97	0.08	21	0.60	0.07	22
	IDSS (NA)	17.50	15.99	22	1.22	0.79	22
	BVDS (V)	30.69	1.39	22	30.65	0.40	22
	K (μA/V2)	111.99	17.64	21	50.62	9.45	22
TR3	VT (OA,V)	0.95	0.08	22	0.54	0.07	22
	IDSS (NA)	20.84	20.47	19	3.51	1.14	22
	BVDS (V)	30.48	1.97	22	31.02	0.06	22
	K (μA/V2)	318.38	60.88	22	139.70	23.77	22

L1=2.0 MIL   L2=0.3 MIL   L3=0.3 MIL
W1=2.8 MIL   W2=2.0 MIL   W3=6.0 MIL

PROCESS PARAMETERS AND STAGE DELAY

		AVG	STDV	#WC
METAL STEP COVERAGE (OHM) 100*RS + 44 METAL STEPS		3.28	0.25	22
CONTACT RESISTANCE (OHM) FOR POLY-TO-METAL 0.2 MIL x 0.4 MIL CONTACT AREA		34.53	7.56	22
RS (OHM/SQ)	N-DS	162.45	9.19	22
	P-DS	44.54	2.53	22
	N-POLY	132.14	10.81	22
	P-POLY	63.55	2.22	22
ZENER DIODE BV (V)	AT 10μA	23.51	0.92	20
	AT 100μA	25.00	0.46	20
32-STAGE RING OSC (VDD=10V)	FREQUENCY (MHZ)	6.49	1.06	22
	STAGE DELAY (NS)	2.46	0.36	22

TABLE 12. INDIVIDUAL-LOT ANALYSIS (SOS) AT LOT S1609

LOT=S1609	TYPE=TCS010	PROC =ALL-I^2	RCA
EPI=0.6μm	DATE=05/17/77-06/21/77	#CHIP= 11	SSTC

DEVICE PARAMETERS

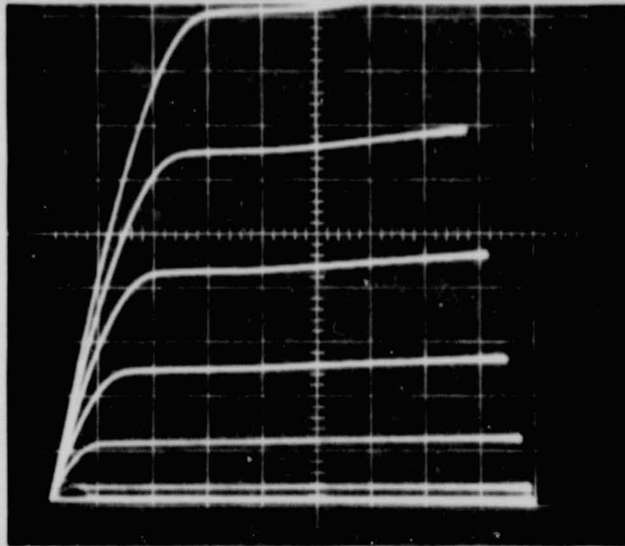
		N-CHANNEL			P-CHANNEL		
		AVG	STDV	#WC	AVG	STDV	#WC
TR1	VT (OA,V)	1.11	0.12	11	0.87	0.04	11
	IDSS (NA)	1.60	1.09	11	4.33	3.41	10
	BVDS (V)	30.73	1.76	11	31.10	0.09	11
	K (μA/V2)	9.62	1.63	11	5.42	0.18	11
TR2	VT (OA,V)	1.06	0.13	11	0.79	0.06	11
	IDSS (NA)	1.76	1.10	11	6.33	7.54	11
	BVDS (V)	25.82	0.72	11	31.10	0.0	11
	K (μA/V2)	55.30	4.49	11	32.62	1.44	11
TR3	VT (OA,V)	1.03	0.13	11	0.75	0.05	11
	IDSS (NA)	1.83	0.86	11	18.45	23.97	11
	BVDS (V)	25.27	0.62	11	30.25	0.46	11
	K (μA/V2)	157.32	19.47	11	94.05	3.50	11

L1=2.0 MIL	L2=0.3 MIL	L3=0.3 MIL
W1=2.8 MIL	W2=2.0 MIL	W3=6.0 MIL

PROCESS PARAMETERS AND STAGE DELAY

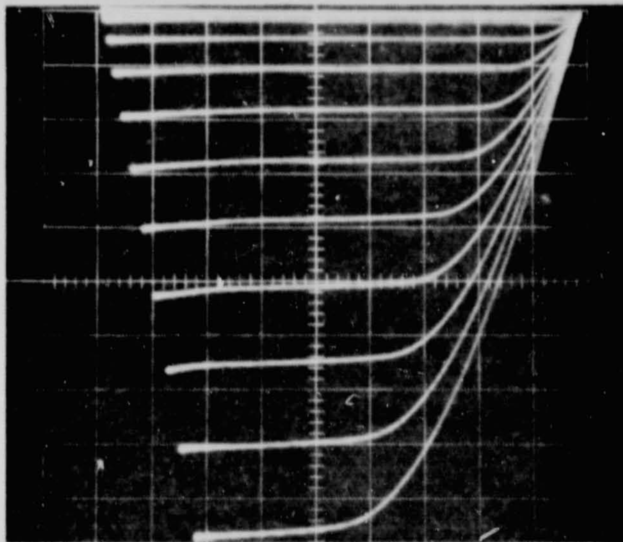
		AVG	STDV	#WC
METAL STEP COVERAGE (OHM) 100*RS + 44 METAL STEPS		9.49	2.44	11
CONTACT RESISTANCE (OHM) FOR POLY-TO-METAL 0.2 MIL x 0.4 MIL CONTRACT AREA		11.14	2.17	11
RS (OHM/SQ)	N-DS	99.28	4.92	11
	P-DS	32.65	2.38	11
	N-POLY	71.25	4.59	11
	P-POLY	51.90	2.68	11
ZENER DIODE BV (V)	AT 10μA	17.97	0.39	11
	AT 100μA	22.36	0.18	11
32-STAGE RING OSC (VDD=10V)	FREQUENCY (MHZ)	3.80	0.21	11
	STAGE DELAY (NS)	4.12	0.22	11

ORIGINAL PAGE IS
OF POOR QUALITY



VERT: 50μA/DIV
HORIZ: 2V/DIV
STEPS: 7 STEPS AT 1V/STEP

(a) NMOS TRANSISTOR

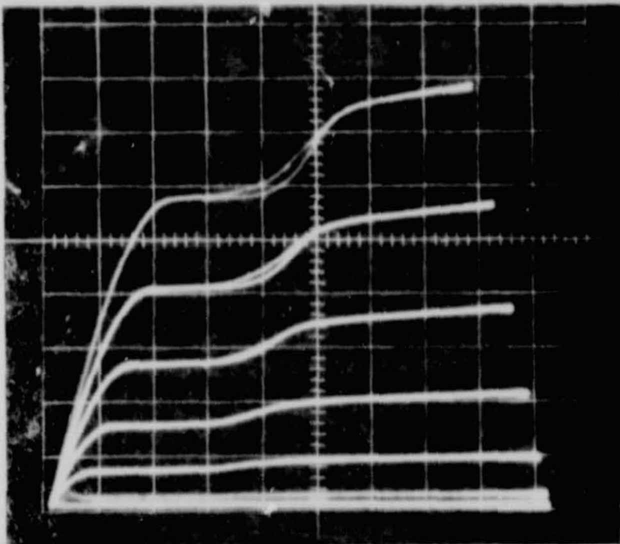


VERT: 50μA/DIV
HORIZ: 2V/DIV
STEPS: 11 STEPS AT 1V/STEP

(b) PMOS TRANSISTOR

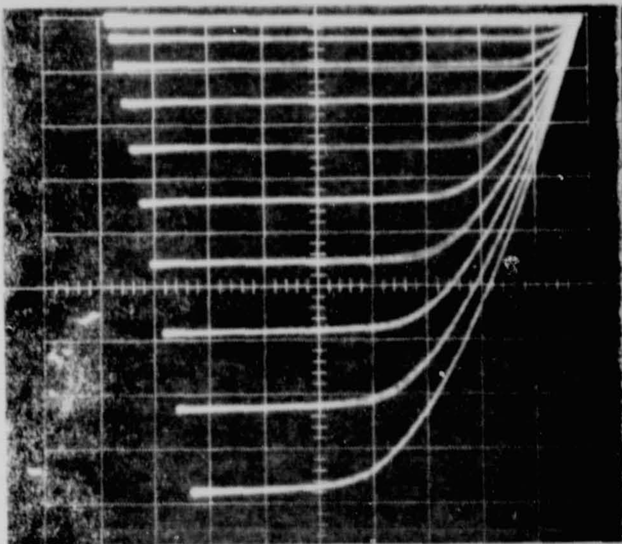
Figure 14. Device characteristics of test transistors from Lot S1456.

ORIGINAL PAGE IS
OF POOR QUALITY



VERT: 50μA/DIV
HORIZ: 2V/DIV
STEPS: 7 STEPS AT
1V/STEP

(a) NMOS TRANSISTOR



VERT: 50μA/DIV
HORIZ: 2V/DIV
STEPS: 11 STEPS AT
1V/STEP

(b) PMOS TRANSISTOR

Figure 15. Device characteristics of test transistors from Lot S1609.

ORIGINAL PAGE IS
OF POOR QUALITY

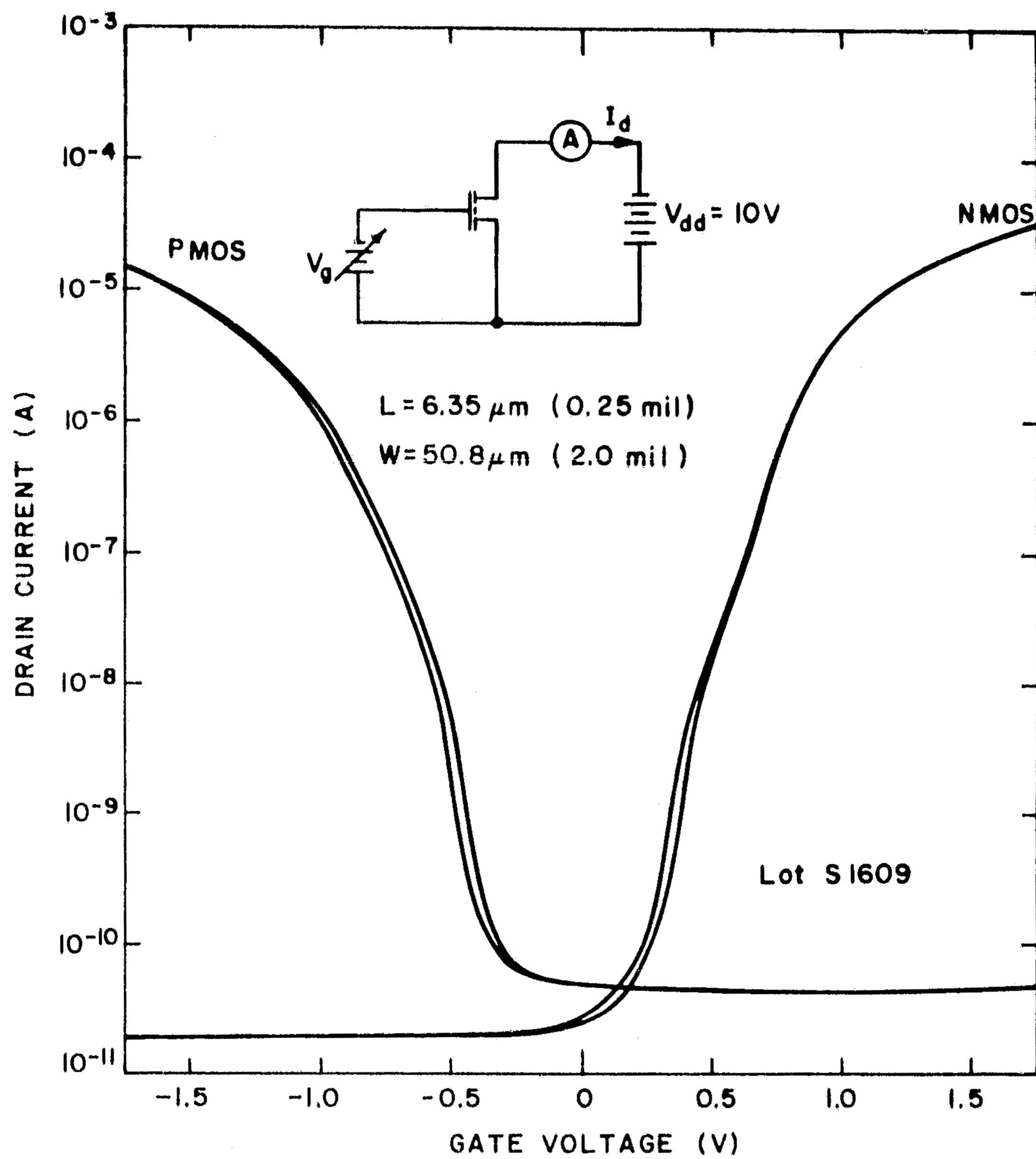


Figure 16. Gate transfer characteristic for both NMOS and PMOS transistors.

C. Stage Delay

The stage delay of the ring oscillator is 2.46 ns (normally 5.5 ns) for Lot S1456; this is approximately two times faster than that of the standard process. This is partly due to the shorter channel length 4.8 μm (0.19 mil). The channel length of the normally processed chip is 6.3 to 7.6 μm (0.25 to 0.3 mil).

The stage delay of the second lot (Lot S1609) is 4.12 ns which is 33% faster than that of the standard process.

IX. CONCLUSIONS

The objective of this program is to establish techniques for the fabrication of high-performance silicon-gate CMOS arrays on SOS substrates which utilize ion-implantation technology as an alternative to conventional diffusion sources.

Application of ion implantation to SOS substrates has several advantages over the conventional *in situ* doped double-epi process. (1) It requires only one epitaxial film growth. The film can be intrinsic and requires no impurity doping during the deposition cycle. Therefore, the same starting SOS wafers can be used for various processes. (2) Both p- and n-islands can be defined with one mask; this eliminates a critical photoresist and etching step and permits closer spacing of the islands. (3) The doping is uniform across the wafer and reproducible from run to run.

The doping of gate and source-drain by ion-implantation techniques is adequate for device fabrication and is easier to control than the conventional doping-oxide technique. The sheet resistance of polysilicon film can be reduced easily to 30 Ω/□ for p-gate and 15 Ω/□ for n-gate and is adequate for the silicon-gate CMOS circuits. The implanted polysilicon was etched by means of plasma rather than the self-limiting preferential KOH-alcohol etch and, therefore, required more attention. However, plasma etching is becoming more practical and reliable due to improvements in technology.

The device characteristics are entirely comparable to those of devices made by processes based on conventional diffusion techniques. With limited number of lots, the operating speed has been improved by at least 33%. The all-ion-implant process on silicon-gate CMOS/SOS will be viable once the life-test data on LSI circuits are established.

☆ U. S. GOVERNMENT PRINTING OFFICE 1978—740-193/12 REGION NO. 4